

University of Copenhagen

Niels Bohr Institute

Center for Quantum Devices

Master's Thesis

Proximitizing InAs 2DEG with NbTi through Epitaxial Aluminum

Author:

Asbjørn Cennet Cliff
Drachmann

Supervisors:

Charles M. Marcus
Fabrizio Nichele

October 14, 2016

Asbjørn Cennet Cliff Drachmann
March 22, 1991
skz927

DANSK RESUME

I denne afhandling præsenterer vi vores arbejde med at realisere og karakterisere transparent kobling mellem superlederen NbTi og en InAs todimensionel elektron gas (2DEG).

Som introduktion uddyber vi fordelene ved at realisere transparente hybrider af 2DEG og konventionelle højtemperatur superledere. Dernæst gennemgås grundlæggende teori om superledere, 2DEG og deres superledende "proximity-effekt".

En beskrivelse af vores materiale system og gennemgang af kredsløbsfremstilling gives sammen med information om den blandings-kryostat og det elektriske kredsløb som bruges til målinger. En detaljeret fabrikationsopskrift findes i opgavens appendiks.

Vi præsenterer målinger af to sub-mikrometer størrelse kredsløb fremstillet af den samme NbTi deponering: et superleder-kvante punkt kontakt-2DEG kredsløb og en superleder-2DEG-superleder Josephson diode. Begge kredsløb viser induceret superledning i 2DEGen fra NbTi med tæt på perfekt transmission, og deres resultater er sammenlignelige. Til sidst gives en konklusion på projektet samt en præsentation af ideer til optimering af disse systemmer.

ABSTRACT

In this thesis we present our work on realizing and characterizing transparent coupling between the superconductor NbTi and an InAs two dimensional electron gas (2DEG).

As an introduction we review the benefits of realizing transparent hybrids of 2DEGs and conventional high temperature superconductors, followed by fundamental theory on superconductors, 2DEGs and their superconducting proximity effect.

An explanation of our material system and a walk-through of the fabrication is given together with information on the dilution cryostat and electrical circuits used for measurements. A detailed fabrication recipe is given in the appendix of the thesis.

We will present measurements of two sub-micron sized devices made from the same NbTi deposition: a superconductor-quantum point contact-2DEG device and a superconductor-2DEG-superconductor Josephson junction. Both devices show induced superconductivity in the 2DEG from the NbTi with close to perfect transmission, and their results are comparable. Lastly conclusions are made, followed by ideas for optimization of these systems.

ACKNOWLEDGMENTS

First and foremost, I would like to thank Charles M. Marcus for making me part of QDev back in 2013. Since then, Charlie has given me interesting projects that were crucial for some sub-groups further research. This responsibility has coursed lots of hard work and has been a great learning experience! It is a huge privilege to have an internationally leading quantum electronics research group here in Copenhagen. I also want to thank Charlie for setting me in touch with Chris Palmström from University of California, Santa Barbara.

I would like to express my gratitude to Chris for inviting me to work in his group in the summer 2015. During that summer I worked with Borzoyeh Shojaei who has thought me a lot about MBE growth and processing of III/V 2DEGs. For this I am very grateful! Also, my thesis work would not have been possible without the materials grown by Bo later in 2015.

During my thesis work, I got indispensable daily guidance and advices from the 2DEG-team in QDev: Henri Suominen, Morten Kjærgaard and Fabrizio Nichele. Their knowledge and experience have helped me through many problems (both theoretical and experimental) without the need for time-consuming trial'n'error approach. For this I am truly grateful!

Shivendra Upadhyay has been a great help with supervision and council regarding nano-fabrication during the project. I'm very grateful for this support!

I would also like to thank the rest of the QDev family. People are always happy to help, have useful discussions and good times!

Lastly I would like to express my gratitude to the physics student community at the Niels Bohr Institute. During the last five years I've found a lot of great friends among the physics students and I have had many memorable moments! An extra thanks to Alexander, A9, Abdu, IV, Gorm, Marieke and Peter for proof-reading parts of this work.

CONTENTS

Dansk Resume	ii
Abstract	ii
Acknowledgments	iii
Table of Contents	vi
List of Figures	viii
List of Tables	ix
1 THE BENEFITS OF REALIZING SUPERCONDUCTOR-SEMICONDUCTOR HYBRIDS	1
2 FUNDAMENTAL CONCEPTS	5
2.1 Superconductivity	5
2.2 Super-Normal Interfaces	8
2.3 Super ₁ -Super ₂ Interfaces	10
2.4 InAs 2DEG	12
2.5 Super-2DEG Interfaces	14
3 FABRICATION AND EXPERIMENTAL SETUP	17
3.1 Material system of choice: InAs 2DEG with Epitaxial Al	17
3.2 Nano-Fabrication of Devices	18
3.2.1 Chip Preparation	19
3.2.2 NbTi(N) Deposition	22
3.2.3 Al- & Mesa Etch	26
3.2.4 Oxide Deposition by ALD	28
3.2.5 Gate Evaporation	28
3.3 Refrigeration	29
3.3.1 Preparing for Cooldown	30
3.3.2 Dry Dilution Refrigeration	32
3.3.3 High Temperature Control in Dilution Fridge	33
3.4 Electronic Setup	34
3.4.1 Checking Resistance of Bonded Lines	34
3.4.2 Current-Bias	34
3.4.3 Voltage-Bias	35
4 TUNNEL SPECTROSCOPY AT THE NBTI-AL/INAs INTERFACE	37
4.1 Tunnel Spectroscopy of Induced Gap	38
4.2 Quality of S-Sm Interface	40
4.3 Magnetic Field Dependence of Induced Gap	42
4.4 Temperature Dependence of Induced Gap	43

5	JOSEPHSON JUNCTION MEASUREMENTS	45
5.1	Temperature Dependence of S-Sm-S junction	46
5.1.1	Temperature Dependence of I_c	46
5.1.2	Temperature Dependence of Δ^*	48
5.2	Field Dependence of I_c	49
5.2.1	Out of Plane Field Dependence of I_c	49
5.2.2	In-Plane Field Dependence of I_c	50
6	CONCLUSION & OUTLOOK	53
6.1	Recap of Results	53
6.2	Suggestions for Further Work	53
6.2.1	Optimization of the InAs 2DEG growth	54
6.2.2	Removing Ti layer under NbTi	54
6.2.3	Using NbTiN-based superconducting stacks	54
6.2.4	In-situ deposition of NbTi(N)	55
A	ARTICLE	57
B	WORK ON AU-COVERED 2DEG	67
C	FABRICATION RECIPES	69
C.1	Alignment Marks	69
C.2	Ti/NbTi/NbTiN deposition	70
C.3	Mesa Etch	73
C.4	ALD	74
C.5	Inner Gates Evaporation	74
C.6	Outer Gates Evaporation	75
D	COMPARISON OF THREE SIMILAR NBTI DEPOSITIONS	77
E	ALIGNMENT WITH VECTOR MAGNET	79
F	REMOVING LINE RESISTANCE FROM CONDUCTANCE MAP	81
G	GATING OF REPORTED JOSEPHSON JUNCTION	83
H	FRAUNHOFER MEASUREMENTS ON EARLIER DEVICES	85
	Bibliography	87

LIST OF FIGURES

Figure 2.1	Superconducting gap & temperature dependence . .	6
Figure 2.2	Field dependence of type I & type II superconductors	8
Figure 2.3	Schematic of Andreev reflection	9
Figure 2.4	Probability of transmission, normal reflection and Andreev reflection	9
Figure 2.5	Schematic of proximity effect	10
Figure 2.6	Local density of states at S_1S_2 interface	11
Figure 2.7	Heterostructure of epi-Al/InAs 2DEG wafer	13
Figure 2.8	Hall bar, density & mobility measurement	14
Figure 2.9	Induced gap in superconductor-2DEG junction	15
Figure 3.1	Schematic of pair coupling along 2DEG/Al/superconductor stack	17
Figure 3.2	Overview of fabrication steps	18
Figure 3.3	Surface of epi-Al wafer	19
Figure 3.4	CAD-design template	20
Figure 3.5	S-Sm-S & S-QPC-Sm device designs	21
Figure 3.6	Overview of milling & NbTi(N) deposition	23
Figure 3.7	Superconducting stack used for reported devices . .	25
Figure 3.8	Sidewalls after sputtering liftoff	25
Figure 3.9	Overview of etch process	27
Figure 3.10	Images during etch process	27
Figure 3.11	Topgate crawling on mesa	29
Figure 3.12	Mounting chip into puck	31
Figure 3.13	Schematic of dilution refrigerator	32
Figure 3.14	Simple circuit for testing line resistance	34
Figure 3.15	Current-bias & voltage-bias circuits	36
Figure 4.1	SEM of S-QPC-Sm device	37
Figure 4.2	QPC pinch off curves	38
Figure 4.3	AC tunnelspectroscopy of gap	39
Figure 4.4	DC tunnelspectroscopy of gap & conductance map .	41
Figure 4.5	Tunnelspectroscopy at in- & out of plane fields	43
Figure 4.6	Tunnelspectroscopy at different temperatures	44
Figure 5.1	MAR illustration & SEM of S-Sm-S device	46
Figure 5.2	I_c vs temperature	48
Figure 5.3	Induced gap vs temperature	49
Figure 5.4	I_c vs out of plane field	50
Figure 5.5	I_c vs in plane field	51
Figure B.1	Heterostructure stack of InAs 2DEG covered by gold	67

Figure E.1	Alignment of vector magnet	79
Figure F.1	Measuring line resistance with voltage bias	81
Figure F.2	Correction of 2-terminal bias vs gate voltage conduc- tance map	82
Figure G.1	Gating of reported S-Sm-S device	83
Figure H.1	SEM of S-Sm-S devices used for measuring Fraun- hofer patterns	85
Figure H.2	Fraunhofer patterns	86
Figure H.3	Fraunhofer theory fit	87

LIST OF TABLES

Table 1	Physical properties of the InAs 2DEG in Bo509	14
Table 2	Comparing similar NbTi-based device from different depositions.	77

THE BENEFITS OF REALIZING SUPERCONDUCTOR-SEMICONDUCTOR HYBRIDS

If not familiar with superconductivity, the proximity effect, and/or 2DEGs, we suggest the reader begins by reading chapter 2, where these topics are briefly covered.

Since their invention in the mid 1900's, computers have been a main component in achieving mathematical results that would take years or decades for humans to calculate. The invention of the transistor was the launch pad for making computers as we know them today, where the computing power is governed by the amount of transistors. A transistor being opened or closed is called a bit with value of either 0 or 1. In the beginning transistors were several microns large, but the invention of nanofabrication with lithography has enabled us to make the transistors smaller, and today their size is on the order of tens of nanometers.

As transistors got smaller, computers have become faster and smaller because more transistors could fit on a chip. There is a catch though - making the transistors too small introduces quantum tunneling of the electrons, thus disabling the ability to keep a transistor closed without letting any current through. One way to decrease the probability of tunneling is increasing the resistance between the source and drain; unfortunately this introduces a new problem in the form of heating from passing currents through low conductivity materials. In short, we are reaching the lower limit of transistor sizes and without new technology, our computers can only get faster by increasing their sizes!

Already in the 80's people realized this problem, and they started formulating the theory for a new kind of computer based on quantum mechanics, which is the very thing that limits the evolution of classical computers. The fundamental idea is to find systems with coherent quantum states where quantum bits (qubits) can be defined. A qubit has probability of being both 0 and 1 (a so called super position), but will collapse into either 0 or 1 when measured, equivalent to performing a calculation. One example is the spin-qubits, where spin up and spin down is used as 0 and 1. The 0-1-superposition makes it possible for the quantum computer to perform

multiple calculations at the same time resulting in an exponentially increasing computing power equal to 2^n , where n is the number of qubits.

Solid state qubits have been made and coupled together, but their quantum information has a decoherence time that is too short for coupling multiple qubits. One way to handle this problem is to synchronize multiple qubits into one, more stable qubit [1]. Another approach is to find more stable systems for making qubits, and one of the ideas is using topological protected quantum states, e.g. Majorana fermions (MFs) [2, 3]. These MFs with non-Abelian statistics have been theoretically predicted to live in 1-dimensional large spin-orbit coupling semiconductors with transparent coupling to a superconductor and with a magnetic field applied along the 1-D channel. Signatures of MFs were first observed in InSb nanowires in 2012 [4] and have been observed in InSb or InAs nanowires multiple times since then [5–10].

Nanowires are great for analyzing the behavior of 1-D systems, but they lack in scalability which makes comprehensive circuits troublesome to fabricate. Two dimensional electron gases (2DEGs) on the other hand are excellent in scalability but one dimensional channels can be difficult to construct, and Majorana signatures have yet to be observed in 2DEGs. Recent theoretical proposals [11, 12] elaborate on how MF signatures can be observed without defining 1-D channels in the 2DEG.

Until recently, 2DEGs also had the problem that transparent superconductor-semiconductor interfaces have been hard to obtain [13–15]. A transparent 2DEG-superconductor interface was achieved by growing epitaxial Aluminum on an InGaAs/InAs 2DEG [16]. Despite the energy gap in Al, Δ_{Al} , being small, its use was dictated by its availability in conventional molecular beam epitaxy (MBE) systems and also by the ease of selective etch from the III/V semiconductors, i.e. removing Al without damaging the underlying III/V. The small Δ_{Al} comes with a critical temperature $T_{c,\text{Al}} = 1.2\text{K}$, making it expensive to apply these systems in industry.

Obtaining a transparent coupling between a 2DEG and a high temperature BCS superconductor would not only be beneficial for the research of realizing topological quantum computation, but would also enable superconducting qubits [17] and general superconducting electronics [18] at liquid ^4He temperature of 4.2 K, which would greatly reduce cooling-costs when implementing these technologies in the industry.

In this thesis, we report work on coupling a NbTi-based superconductor to an InAs 2DEG, using the epitaxial aluminum as "Andreev glue" between the two materials, ensuring a transparent transport from NbTi to InAs. We start by going through the necessary physical theory of superconductors and 2DEGs in chapter 2. Fabrication and measurement setups are elaborated in chapter 3. Two devices, made from the same deposition, are used to characterize the 2DEG/superconductor hybrid system: A superconductor-quantum point contact(QPC)-2DEG device and a superconductor-2DEG-superconductor Josephson junction. The data and analysis of the QPC device

is presented in [chapter 4](#) while [chapter 5](#) elaborates on results from the Josephson junction. Lastly, [chapter 6](#) summarizes the results and discusses possible improvements and further work. The work culminated in an article and the latest draft is attached in [Appendix A](#).

In this chapter we will go through the physics necessary to understand methods and results presented in this thesis. Firstly, [section 2.1](#) gives a crash course on the essential superconductor knowledge. It is followed up by the proximity effect of Super(conductor)-Normal(conductor) and Super₁-Super₂ interfaces, respectively in [section 2.2](#) and [section 2.3](#). A brief explanation of 2DEGs, specifically InAs, is given in [section 2.4](#), followed by an introduction on Super-2DEG interfaces in [section 2.5](#). Lastly we sum-up the two most essential concepts to take into account when building devices that exploit the superconducting proximity effect.

2.1 SUPERCONDUCTIVITY

Superconductivity has been known to mankind since Onnes back in 1911 measured zero resistance for the first time. He was the first person to liquefy Helium, and used it to measure different materials at these unexplored low temperatures. He found that the resistance of Mercury went from finite to zero when cooled below a *critical temperature*, T_c of 4.2K. This transition to a perfect conductance phase is one of superconductors key features, and T_c varies for different materials. Another key feature is the Meissner effect: Superconductors are perfect diamagnets, so they expel magnetic fields as long as the field is lower than the *critical field*, H_c , over which superconductivity is broken. H_c is a material-dependent property just like T_c . Since currents make self-fields, it is not surprising that superconductors also have a *critical current* I_c . If a current larger than I_c is passed through the superconductor it turns into a normal conductor.

It seems that superconductivity is lost when too much energy is put into the system. Why can that be, and why are superconductors dissipationless? It was not until the 50s that explanatory theories were published, especially two theories were revolutionary: GL-theory (Ginsburg & Landau) and BCS-theory (Bardeen, Cooper & Schrieffer). Superconductivity is a phase, a new state of matter (like gas, fluid and solid), that some materials can transition

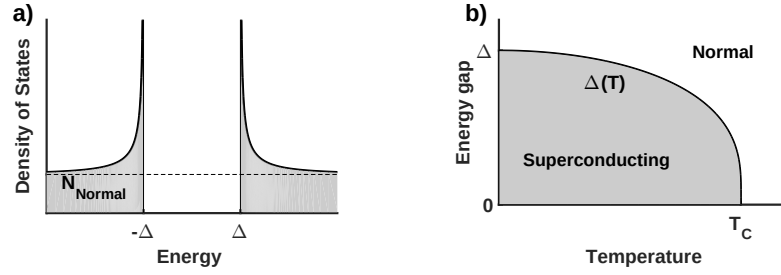


Figure 2.1.: Charateristics of the superconducting gap. **(a)** Shows the BCS density of states at $T = 0$, with $E_F = 0$ and with the dashed line being DOS in a normal metal. Calculated using equation from [19]. **(b)** Shows the temperature dependence of Δ , calculated by Equation 2.1.

into when cooled below T_c . At these low temperatures a weak electron-phonon-coupling is strong enough to bind electrons into pairs, where the two electrons have opposite momentum and spin: $(\mathbf{k} \uparrow, -\mathbf{k} \downarrow)$. These *Cooper pairs* (CP) have spin-0, and thereby acts as bosons. Since they are bosons, they can condense into the same quantum ground state, thus explaining the dissipationless motion.

The energy up to which it is favorable for the electrons to pair up is given by the *pair potential* aka. the energy gap Δ , which is on the order of $k_B T_c$, with k_B being the Boltzmann constant. The exact factor can be calculated by BCS theory, and varies for different superconductors [19]. From solid state physics, we know that the energetically most accessible electrons in a material lie at the Fermi Energy, E_F , so all electrons within $E_F \pm \Delta$ have low enough energy to condensate. This forms a gap in the electron density of states (DOS) as shown on Figure 2.1(a). If the electrons, by any means obtain an energy higher than Δ , the CP is broken. By increasing temperature from zero, the energy gap decreases until it collapses for $T > T_c$, see Figure 2.1(b), which depicts an approximation of the temperature dependence given by the following formula based on BCS theory¹:

$$\Delta^*(T) = \Delta^*(0) \cdot \tanh \left(1.74 \cdot \sqrt{\frac{T_c}{T}} - 1 \right), \quad (2.1)$$

The order parameter for this system is the superconducting wave-function $\psi = \sqrt{n_s} e^{-i\phi}$. The function only have two parameters; n_s is the density of superconducting carriers and ϕ is a quantum phase. Since all CPs condense into the same state, the order parameter dictates that they all have the same phase, even on macroscopic scale. The value of the phase is arbitrary and manifests when the material is cooled below T_c .

¹ The real solution to the temperature dependence of the BCS gap is bothersome to solve numerically. This approximation was found on stackexchange: <http://physics.stackexchange.com/questions/54200/superconducting-gap-temperature-dependence-how-to-calculate-this-integral> It should be valid up to 2% from a universal self-consistent solution.

Like any other transition, superconductors also have a *coherence length* ξ_0 which describes how far the phase-correlation can travel into a non-superconducting region before the correlation is lost. ξ_0 at $T = 0$ can be estimated from the uncertainty relation $\hbar \lesssim \Delta x \Delta p$ by assuming that the relevant electrons are within $\sim k_B T_c$ of E_F . Thus the momentum uncertainty can be written as $\Delta p = k_B T_c / v_F$, where v_F is the Fermi velocity. The position uncertainty is taken as the estimate of the coherence length, thus given by

$$\Delta x \gtrsim \frac{\hbar}{\Delta p} = \frac{\hbar v_F}{k_B T_c} \quad \rightarrow \quad \xi_0(T = 0) = \alpha \frac{\hbar v_F}{k_B T_c}, \quad (2.2)$$

with α being a real number close to unity. An important thing to notice is that ξ_0 is inversely proportional to $k_B T_c \sim \Delta$, telling us that superconductors with higher T_c have a lower ξ_0 . Another important length scale to mention is the *mean free path*, ℓ . This is a general material length scale describing how far a particle can travel before it scatters. If $\ell < \xi_0$, called the *dirty regime*, a new effective coherence length is needed since the phase correlation also can be lost by scattering. Different regimes will be discussed in [section 2.5](#)

A last length scale worth mentioning is the penetration depth, λ , describing how far a magnetic field penetrates a superconductor before it is expelled. It can be derived from the second London equation²

$$\mathbf{H} = -c \cdot \nabla \times \left(\frac{4\pi\lambda^2}{c^2} \mathbf{J}_S \right), \quad (2.3)$$

where $\mathbf{J}_S$ is the superconducting current (supercurrent) density. By use of Maxwells equation $\nabla \times \mathbf{H} = 4\pi\mathbf{J}/c$ together with [Equation 2.3](#), one obtains:

$$\nabla^2 \mathbf{H} = \frac{\mathbf{H}}{\lambda^2} \quad \rightarrow \quad H(x) = H_0 e^{-\frac{x}{\lambda}}, \quad (2.4)$$

with x pointing into the superconductor starting from the interface at $x = 0$, thus mathematically describing the Meissner effect. In physical terms, the penetration depth is a result of two opposing energies. It is energetically favorable for electrons with $E < \Delta(T, H)$ to stay in the CP condensate, but it also costs a lot of energy to keep out the magnetic field flux. To find an equilibrium, the superconductor sacrifices the outermost CPs in creating an interfacial layer with excited electronic states forming a domain wall, thus paying the energetic cost of excluding the magnetic field. These excited electrons move in a certain trajectory creating a self-field to cancel out the applied field. The interfacial layer has a thickness of $\sim (\xi - \lambda)$.

Unlike the coherence length, the penetration depth increases for superconductors with higher T_c , and for some materials λ is longer than ξ . In these materials, called type II superconductors, it can be energetically favorable to let small magnetic fluxes penetrate the whole superconductor, thereby releasing the magnetic pressure on the surface. This flux penetration changes

² The London brothers wrote down in 1935 two equations that described the electrodynamics of superconductors.

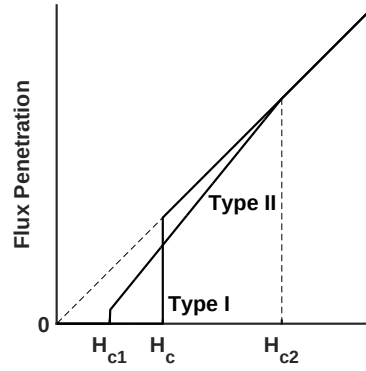


Figure 2.2.: Illustration of flux penetration as a function of applied field for Type I and Type II superconductors. Type I has a first order transition while Type II has a second order transition. Figure is adapted from [19].

the critical field dependence, as shown on Figure 2.2. Type I expels all flux until superconductivity breaks down at H_c . A type II superconductor has a continuous transition starting from H_{c1} , where only one *magnetic flux quantum*, $\Phi_0 = h/(2e)$, penetrates. Increasing the field further increases the amount of penetrating fluxes until reaching H_{c2} where the area of all the fluxes covers the whole superconductor and it goes normal.

Type I superconductors can also have magnetic flux penetration if their thickness, in the direction of applied field is shorter than the penetration length. Here their behavior is type II like. Another interesting feature of thin superconductors is that they have increased H_c , if the applied field is points along the thin plane or wire, due to only few magnetic field lines getting obscured by the superconductor.

2.2 SUPER-NORMAL INTERFACES

Superconductors (S) are by themselves interesting and fascinating, but combining them with other materials, eg. normal conductors (N), adds a lot of new physics and opportunities for applications. In this section we will describe the fundamental case: the transport across a Super-Normal (SN) interface. When a electron from N, with energy close to E_F hits the interface, it can either normal reflect back into N, or it can undergo *Andreev reflection* which is depicted on Figure 2.3. The incident electron (e) gets reflected as a hole (h) with equal but opposite momentum and spin. This effectively transfers two electrons into S in form of a CP. Likewise a hole can be Andreev reflected as a electron, thus effectively transferring two electrons from S into N. The electron-hole pair in the normal metal gets a phase-correlation from the Andreev reflection and the phase is kept within ξ , of the interface,

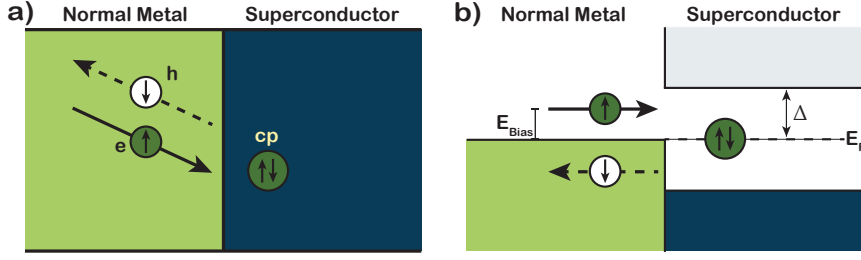


Figure 2.3.: **(a)** Sketch of Andreev reflection in real space: An electron incident on the SN-interface from the normal metal Andreev reflects as a hole with equal but opposite momentum and spin, thus transferring two electrons into the superconductor as a CP. **(b)** Energy diagram: An electron with $E_{\text{Bias}} < E_F + \Delta$ is retro reflected into a hole with $E = -E_{\text{Bias}}$ thus adding another CP to the condensate at E_F in the superconductor.

see Figure 2.5. A revolutionary paper in describing transmission through a SN interface was published by Blonder, Tinkham and Kalpwijk (BTK)[20]. Their model is to have a delta-function shaped potential barrier at the SN interface described by the dimensionless parameter Z , at zero temperature. They calculate the possibilities for Andreev reflection (A), normal reflection (B) and transmission with/without branch crossing (C/D). Here we will only look at a collective transmission $T = C + D$. Figure 2.4 shows plots of A, B and T as a function of energy at different values of Z . For low Z , A and T dominate while B has more influence as Z is increased. In conclusion, a low SN interface resistance gives more Andreev reflections. Another thing to notice is that no Transmission happens at $E < \Delta$ since no excitations live within Δ for a superconductor at $T = 0$.

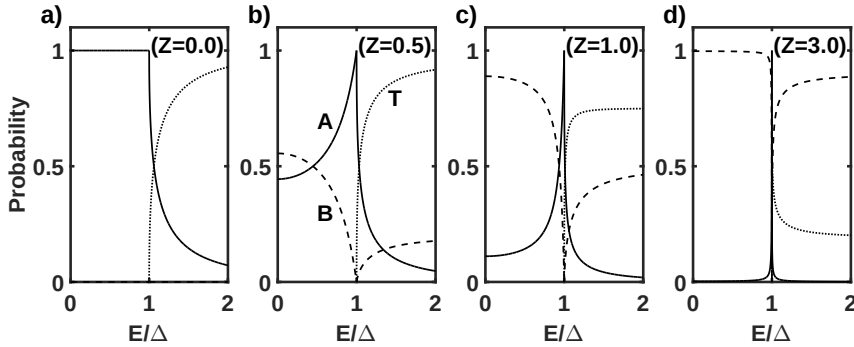


Figure 2.4.: Plots showing the probability of Andreev Reflection(A,—), normal reflection(B,- -) and transmission(T, ...) at a SN-interface as a function of energy for different Z -paramter. **(a)** $Z = 0.0$, a perfect interface means no B. **(b-c)** As Z increases B becomes more possible and fewer quasi-particles undergo A or T. **(d)** For high Z , B becomes the dominant process. Plots are calculated by equations from [20]

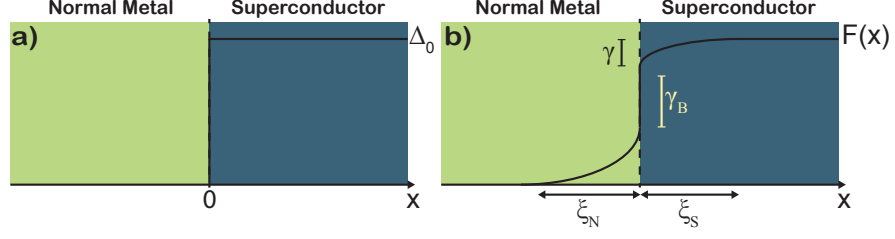


Figure 2.5.: Schematics showing the spatial dependence of the DOS for correlated particles, $F(x)$, with and without the proximity effect. **(a)** No proximity effect, $F(x) = \Delta_0$ in S and $F(x) = 0$ in N. **(b)** With proximity effect, $F(x)$ leaks from S into N on the order of the coherence lengths. The amount of leakage is controlled by γ and γ_B .

One of the key assumptions in the BTK model is to have a step-like order parameter potential $\Delta(x)$ at the SN interface, like on Figure 2.5(a). On the contrary, the DOS for correlated particles $F(x)$ spreads out close to the interface, if Andreev reflections happen. $F(x)$ leaks into the normal metal and decays on the order of the coherence length in N, ξ_N . This is called the *proximity effect*. The *inverse proximity effect* is the fact that $F(x)$ in S is reduced at the interface, but regain full value on the order of the coherence length in the superconductor ξ_S . Both effects are shown on Figure 2.5(b) which also introduces two parameters: the barrier strength

$$\gamma_B = \frac{2}{3} \frac{\ell_N}{\xi_N} \left\langle \frac{1-D}{D} \right\rangle, \quad (2.5)$$

and the pair-breaking parameter

$$\gamma = \frac{\rho_S \xi_S}{\rho_N \xi_N}. \quad (2.6)$$

Here D is normal-transmission coefficient from BTK, with $D^{-1} = 1 + Z^2$, $\langle \dots \rangle$ denotes angle averaging and $\rho_{\{S,N\}}$ are the specific normal-state resistances for the two materials. Both parameters are found by deriving boundary conditions for $F(E, x)$ and $G(E, x)$ which is the quasi particle DOS [21]. To increase the proximity effect (increase amount of $F(x)$ in N) one should try decreasing γ and γ_B . The pair-breaking parameter can only be changed by changing the material, but the barrier strength is greatly dependent on the interface between the two materials and have a huge impact on quality of the choice of fabrication methods, see chapter 3.

2.3 SUPER₁-SUPER₂ INTERFACES

This section will look into the transport between two different superconductors (S_1 and S_2), with $T_{c,1} > T_{c,2}$, in close proximity to each other. In the following we will assume a perfect interface ($Z = 0$). For quasi-particles with $E < \Delta_2 < \Delta_1$ CPs can be transferred across the interface. At $\Delta_2 < E < \Delta_1$ elec-

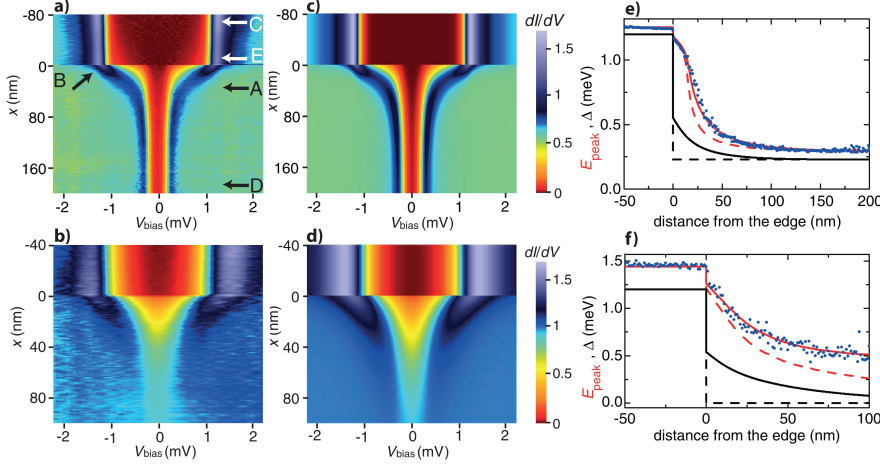


Figure 2.6.: Measurements and simulations of LDOS in a S_1S_2 interface. Graphs are copied from [22]. The topmost graphs are at 0.3K while the bottommost are at 2.05K. **(a-b)** STS measurements of dI/dV at the two temperatures. The junction interface is at $x = 0$, S_1 at $x < 0$ and S_2 at $x > 0$. In both cases a wider gap is seen in S_2 close to the interface. **(c-d)** Simulations of LDOS at the two temperatures, made from 1D Usadel equations. In both cases, the computed dI/dV resembles the features of the measured data very well. **(e-f)** Spatial evolution of the energy of the peak maximum $E_{\text{peak}}(x)$ and the order parameter Δ across the interface. Experimental data is compared to self-consistent (solid lines) and non-self-consistent (dashed lines) calculations. At both temperatures the data is nicely reproduced by the self-consistent calculations.

tron/holes from S_2 will Andreev reflect while for $\Delta_2 < \Delta_1 < E$ a combination of Andreev reflection and transmission will happen, like on Figure 2.4(a).

The first experimental data on the local density of states (LDOS) across a S_1S_2 interface was recently made by Cherkez et al [22]. They have an in situ grown 7 monolayer high Pb island (S_1) on a 1 monolayer Pb background (S_2) with $T_{c,1} \approx 6.2\text{K}$ and $T_{c,2} \approx 1.8\text{K}$. Using an in situ scanning tunneling spectroscopy (STS) they measure dI/dV across the interface which is proportional to the LDOS [23]. A selected part of their data is shown on Figure 2.6. Close to the interface a significant increase in width of the Δ_2 is visible both for T lower and higher than $T_{c,2}$. To simulate their data, they use 1D Usadel equations. For $T > T_{c,\{1,2\}}$ the materials are normal metals, with a huge electron density and therefore a low ℓ , coursing the system to be in the dirty regime for which Usadel equations are very efficient in describing transport for superconductors at arbitrary temperatures [22].

On Figure 2.6(e-f) the authors show self-consistent and non-self-consistent calculations of $\Delta(x)$. These calculations also give the energy of the peak maximum E_{peak} . By comparing E_{peak} to the STS data, it is clearly visible that for both temperatures the self-consistent calculations fit the data better. For $T < T_{c,2}$ the order parameter in S_2 is enhanced close to the interface and

for $T > T_{c,2}$ the order parameter is reintroduced in the otherwise normal conducting metal, again in the vicinity of the interface.

The interface parameters for a S_1S_2 junction, given in [24], are similar to those of a SN junction given by Equation 2.5 and Equation 2.6. The pair-breaking parameter is

$$\gamma = \frac{\rho_{S_1} \xi_{S_1}}{\rho_{S_2} \xi_{S_2}} \quad (2.7)$$

and the barrier strength

$$\gamma_{BN} = \frac{R_B}{\rho_{S_2} \xi_{S_2}}, \quad (2.8)$$

with R_B being the interface resistance times the interface surface area. As for the SN case, the proximity effect is most effective if both parameters are minimized. Again the interface resistance is the only parameter which is not material dependent, and can be minimized by optimizing fabrication.

2.4 INAS 2DEG

Superconductors are great in many aspects, but they are limited by having a high and uncontrollable electron density. Here, semiconductors, and especially 2 dimensional electron gasses (2DEGs), are the materials of choice. These are created by growing semiconductor heterostructures to create a quantum well (QW) in the growth direction which confines the carriers to move in the 2D plane perpendicular to the growth.

In the reported heterostructure an InAs/InGaAs QW is formed with an extra AlGaSb bottom barrier and epitaxially grown aluminum on top, see Figure 2.7. Self-consistent simulations on similar InAs/InGaAs QW shows that the wave function extends into the aluminum [16], thus enabling Andreev reflections. The epitaxially grown Al makes a pristine interface with the III/V, which we will look further into in section 2.5.

To describe the 2DEG, let us go through some terminology. The QW can be approximated by a finite square well with the dispersion relation

$$E_n(k_x, k_y) = \frac{\hbar^2 k^2}{2m^*} + E_n, \quad (2.9)$$

with n being the number of modes in the QW and m^* the effective electron mass which, in the case of an isotropic dispersion, is given by

$$\frac{1}{m^*} = \frac{1}{\hbar^2} \frac{d^2 E}{dk^2}. \quad (2.10)$$

Two dimensional systems have special property that the density of states is constant in energy:

$$D(E) = \frac{dN}{dE} = \frac{m^*}{\pi \hbar^2}. \quad (2.11)$$

Al	25nm
In _{0.8} Ga _{0.2} As	6nm
InAs	9nm
In _{0.8} Ga _{0.2} As	4nm
In _{0.8} Al _{0.2} As	2nm
Al _{0.9} Ga _{0.1} Sb	40nm
Al _{0.9} Ga _{0.1} As _{0.08} Sb _{0.92}	200nm
AlSb	5nm
GaSb	10nm
GaSb:Un(001)	Substrate

Figure 2.7.: Sketch of Epi-Al/InAs 2DEG heterostructure of the wafer: Bo509.
Grown by Borzoyeh Shojaei from Palmström Research Group.

Assuming $E_1 < E_F < E_2$ only one subband is occupied, and the density of states is

$$n = \int_{E_1}^{E_F} dE D(E) = \frac{m^*}{\pi \hbar^2} (E_F - E_1). \quad (2.12)$$

By plugging the Fermi wavelength, k_F , into Equation 2.9, we obtain $E_F = \frac{\hbar^2 k_F^2}{2m^*} + E_n$, which together with Equation 2.12 gives the relation

$$k_F = \sqrt{2\pi n}. \quad (2.13)$$

As explained below, n is easily measured so the relation between n and k_F enables determination of important physical quantities like the Fermi energy, Fermi velocity and Fermi wavelength:

$$E_F = \frac{\hbar^2 k_F^2}{2m^*}, \quad v_F = \frac{\hbar k_F}{m^*}, \quad \lambda_F = \frac{2\pi}{k_F}. \quad (2.14)$$

The mean free path is given by

$$\ell = v_F \tau_e = \frac{\hbar}{e} \mu \sqrt{2\pi n}, \quad (2.15)$$

where τ_e is the mean time between collisions (elastic scattering time) given by $\tau_e = \mu m^*/e$, and μ is the mobility of the electron, which like n is measured from Hall bar measurements, see Figure 2.8.

Mobility and density can either be determined by the crossing of the resistivities, see Figure 2.8(b), or by these relations [25]:

$$n = \frac{1}{e \frac{d\rho_{xy}(B=0)}{dB}}, \quad \mu = \frac{1}{e n \rho_{xx}(B=0)}. \quad (2.16)$$

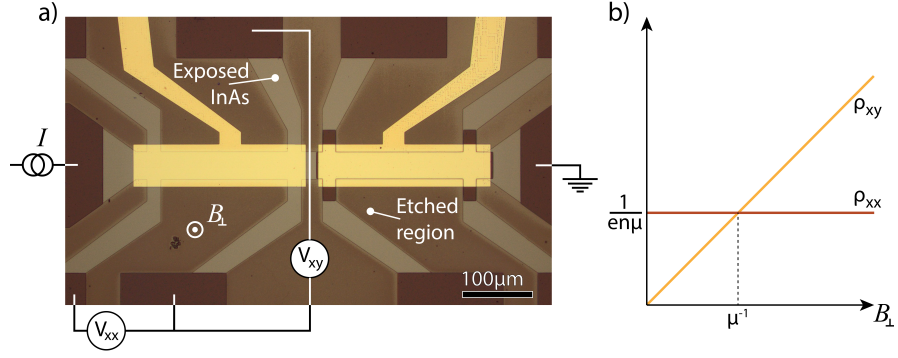


Figure 2.8.: **(a)** Optical image of the measured Hall bar also showing the setup to measure V_{xx} and V_{xy} . **(b)** Sketch of $\rho_{xx} = (V_{xx}/I) \cdot (W/L)$ and $\rho_{xy} = V_{xy}/I$ as a function of $B_{\perp}$. Their relations to n and μ are also displayed. On this Hall bar the L/W -ratio was 5.

Quick measurements were made to get an estimate of the physical properties of the 2DEG. Those properties are tabulated in Table 1:

$n(\text{cm}^{-2})$	$\mu(\text{cm}^2/\text{Vs})$	$k_F(\text{nm}^{-1})$	$\lambda_F(\text{nm})$	$\ell(\text{nm})$	$v_F(\text{m/s})$
$1 \cdot 10^{12}$	10.000	0.25	25	164	$1.11 \cdot 10^6$

Table 1.: Physical properties of the InAs 2DEG in Bo509

To obtain the Fermi velocity, the effective mass of bulk InAs $m^* = 0.026m_e$ [26] was used.

A last, but very important quantity is the (phase) coherence length which was mentioned multiple times in the last few sections. Depending on the geometry of a device, it might be either in the ballistic or diffusive regime, so a coherence length for both cases should be determined. As explained in section 3.3, measurements are done at ~ 30 mK for which the only dephasing process is electron-electron collisions. Electrons with different energy ΔE will after a time τ obtain a phase difference $\phi = \tau \Delta E / \hbar$. For simplicity, let us define the electrons as uncorrelated when ϕ is of the order unity and use that Fermi-Dirac statistics state that $\Delta E \sim k_B T$. This results in a dephasing time of $\tau_\phi = \hbar / (k_B T)$. The mean free path for ballistic and diffusive system are $l = \tau v_F$ and $l = \sqrt{D\tau}$ respectively, where D is the diffusion constant, which for a 2D system is given by $D = v_F \ell / 2$. Inserting the τ_ϕ in the two mean free paths, results in:

$$\xi_{\text{bal}} = \frac{v_F \hbar}{k_B T}, \quad \xi_{\text{diff}} = \sqrt{\frac{v_F \ell \hbar}{2 k_B T}} \quad (2.17)$$

2.5 SUPER-2DEG INTERFACES

The proximity effect between superconductor and semiconductor is similar to that for super/normal junctions, but with changes in the BTK Z -parameter describing the interface transport. Since the electron density in a semicon-

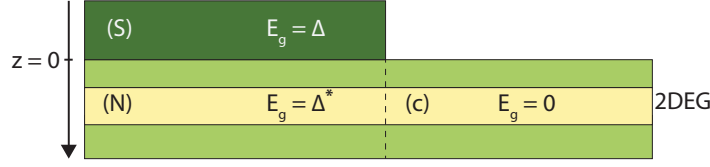


Figure 2.9.: Schematic showing the superconducting gap across a wafer like Figure 2.7. The superconductor (S), with a gap of Δ , is stripped from parts of the wafer, leaving behind exposed semiconductor (c). Only the S-capped 2DEG (N) has an induced superconducting gap Δ^* .

ductor can be smaller, the Fermi velocity can also be smaller, leading to a difference in Fermi energy of the two materials, which adds to the energy barrier between the two materials. This Fermi velocity mismatch $r = v_{F,N}/v_{S,N}$ is used in defining a new effective Z-parameter [21]:

$$Z_{eff} = \sqrt{Z^2 + \frac{(1-r)^2}{4r}}. \quad (2.18)$$

A typical metal has a Fermi velocity of $\sim 10^6$ m/s [27], which is comparable to that of our InAs 2DEG, see Table 1, so r does not play a big role for Z_{eff} in our material system.

Another problem with normal-semi or super-semi interfaces is the Schottky barrier, which forms a high electrical resistance at the interface. This is not the case for InAs though, since its Fermi level is pinned in the conduction band, thus causing an accumulation layer at the surface [28].

When a 2DEG is covered and in low electrical contact with a superconductor, as for Figure 2.7, with the 2DEG wave function extending into the superconductor, an induced superconducting gap $\Delta^* < \Delta$ is introduced in the 2DEG. This is due to quasi particles having a finite average lifetime in the 2DEG [29]. This part of the 2DEG is specified as "N". The size of Δ^* approaches Δ for $\gamma_B \rightarrow 0$. If parts of the 2DEG is not covered with superconductor we specify it "c", see Figure 2.9. The uncovered 2DEG does not have an induced gap, but phase-correlated quasi particles from N penetrate into c. Thus, the effective superconducting gap one measures in a superconductor/2DEG junctions is not Δ but instead Δ^* .

To build devices that exploit the superconducting proximity effect, many things have to be taken into account of which some are essential for functionality. In this last part we will recap the two most essential points:

First and foremost is a low interface resistance between the "proximitiser" (superconductor) and the conductor to be proximitised. Andreev reflections are the source of the proximity effect and the possibility for Andreev reflections is inversely proportional to the interface resistance. Interface transparency is paramount!

The other essential part is taking length scales into account. The phase-coherent quasi particle coupling from an Andreev reflection only lasts within a finite length: the effective coherence length of the material which the quasi particles are traveling in. When designing devices, one should make sure that, if necessary, the length scales of the device is on the order of the coherence length or smaller. If that is not the case, superconducting information will be lost.

FABRICATION AND EXPERIMENTAL SETUP

It has taken many days and long nights to execute the work presented in this chapter, which is devoted to the experimental specifications of the project. We'll start with explaining our material system of choice: InAs 2DEG with *in situ* deposited epitaxial aluminum on top. Next, the most time-consuming section: Nanofabrication. Afterwards follows an elaboration on our cooling technique, used to perform low temperature measurements together with a description of the electrical circuits, used for various measurements.

3.1 MATERIAL SYSTEM OF CHOICE: INAS 2DEG WITH EPITAXIAL AL

As mentioned previously, the goal of the thesis is to induce a wide and hard superconducting gap into a 2DEG. The reason we choose a 2DEG, instead of e.g. nanowires, is due to the ease of scalability, once a recipe is working. As concluded in the previous chapter, two things are essential for the functionality of devices based on superconducting proximity effect: Low interface resistances, and lengths shorter than the effective coherence length.

There are many methods to make the contact between semiconductor and superconductor, but like many other facets of fabrication, there are profitable ways and inefficient ways to do it. As explained in [section 2.5](#), the interface between the materials is crucial for the possibility of Andreev reflections. Chang et al. were the first to show that a hard gap is obtained

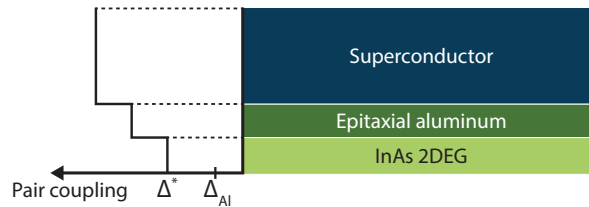


Figure 3.1.: Illustration showing how the superconductor pair coupling falls when going down into aluminum and becomes the induced gap Δ^* in the InAs 2DEG. Having a large gapped superconductor and transparent interfaces results in $\Delta^* > \Delta_{Al}$.

in a semiconductor, InAs, by depositing the superconductor, Al, in-situ in the MBE growing chamber [30]. Our methods of choice are based on the same idea of growing an epitaxial metal on the 2DEG *in situ* [16], but then in addition adding a higher T_C superconductor afterwards, which will result in a larger induced gap, see Figure 3.1.

Two different material systems were tested. Au-capped InAs and Al-capped InAs. The material with Au-capping was promising, since Au does not oxidize, which means that no rough surface cleaning would be necessary before deposition of the high- T_C superconductor. Unfortunately, the etching of the Au did not go well, presumably due to Au diffusing into the upper semiconducting layers, which made the Au-etch also attack the semiconductor. Our work with the Au is elaborated in Appendix B.

3.2 NANO-FABRICATION OF DEVICES

Our work on the Al-capped material is presented here in this section. I'll go through all the steps in the same chronological order of performance, as shown on Figure 3.2. The five subsections in this section are devoted to the five sub-figures (a-e). The subsections will explain the methods, while the specific recipes can be found in Appendix C.

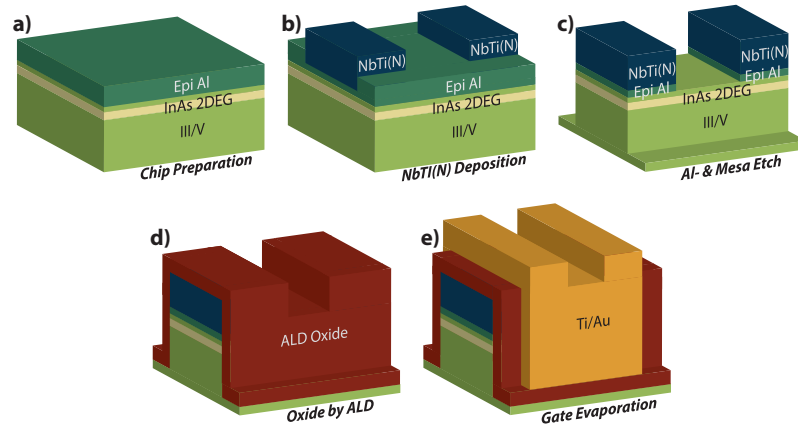


Figure 3.2.: Overview of fabrication steps on Al-capped wafers. The aspect ratio is not realistic, but the sketch shows the removal or addition of material for each step. All structures are defined by electron-beam lithography. (a) MBE grown wafer is cleaved into smaller chips, and each chip gets lithography-defined Ti/Au alignment marks. Figure 2.7 gives a thorough description of the wafer specifying all layers as well as their thicknesses. (b) The Al has a native oxide, which in lithographically defined areas is argon-milled away before deposition of a Ti/NbTi/NbTiN stack. Figure 3.6 gives an overview of the cumbersome fabrication steps. (c) To define mesas in the wafer, chemical wet etch is used. The three-step etch is elaborated on Figure 3.9. (d) For oxide/dielectric both Al_2O_3 and HfO_2 have been used, usually 50nm. (e) Evaporated Ti/Au is used for gates. The amount of evaporated material is always chosen, 50-100nm thicker than the mesa etch depth.

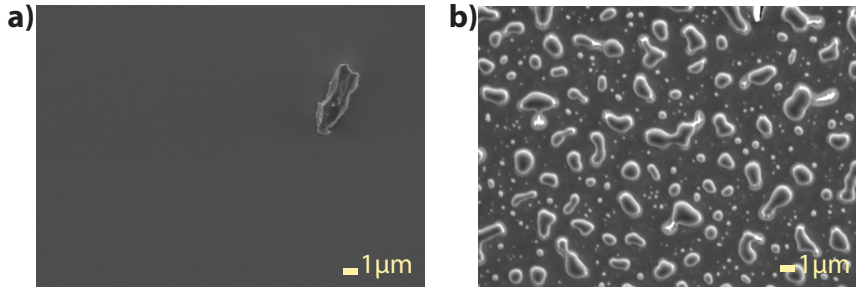


Figure 3.3.: **(a)** SEM of a good part of the wafer. The particle is used to show that the image is in focus. **(b)** SEM of a bad part of the wafer, in this case showing non-nucleated Aluminum.

3.2.1 Chip Preparation

From Wafer to Chip

The employed substrate was grown by Borzoyeh Shojaei from the Palmström group at University of California, Santa Barbara. The InAs 2DEG heterostructure is capped by 25 nm epitaxial Al, see Figure 2.7. The thickness of 25 nm is crucial for device fabrication, this is elaborated in subsection 3.2.2. The wafer is rather fragile and should always be handled with carbon tweezers. A big wafer-piece was received by mail. At first, its size was measured and the surface was inspected by optical microscope and scanning electron microscope (SEM), to identify good and bad regions of the wafer. In a good region, no surface features can be seen with the SEM, see Figure 3.3(a). A region can be bad either due to scratches, impurities, or due to Al not nucleating properly on the surface, giving rise to bubbles visible by SEM, see Figure 3.3(b).

After the characterization, resist is spun on the wafer and when not being used, the wafer is stored in nitrogen cabinets. This is done to prevent degradation of the material. Since the wafer is precious and limited, it is cut and cleaved into smaller pieces. The cuts were made with a manual scriber¹. A chip area of $2.5 \times 5 \text{ mm}^2$ was found to be a good size, compensating between being small and still big enough to work with.

Alignment Marks

The first lithography step is to define alignment marks for further lithography, see Figure 3.4(a-c). All lithography is done by electron-beam, to obtain precision down to 20 nm. First, the protecting resist is stripped and a new layer is spun. Because of its small size, the chip should spin slowly when depositing the resist. The corners of the chip are used to align the alignment mark design to the chip. Due to edge-beads after resist spinning, the bottom- and top-most marks can't be used for thick resist stacks. All subsequent lithography steps use 4-mark registration, making it necessary to have many

¹ A diamond tip mounted on a machine with high precision of movement and rotation in the plane of the wafer surface.

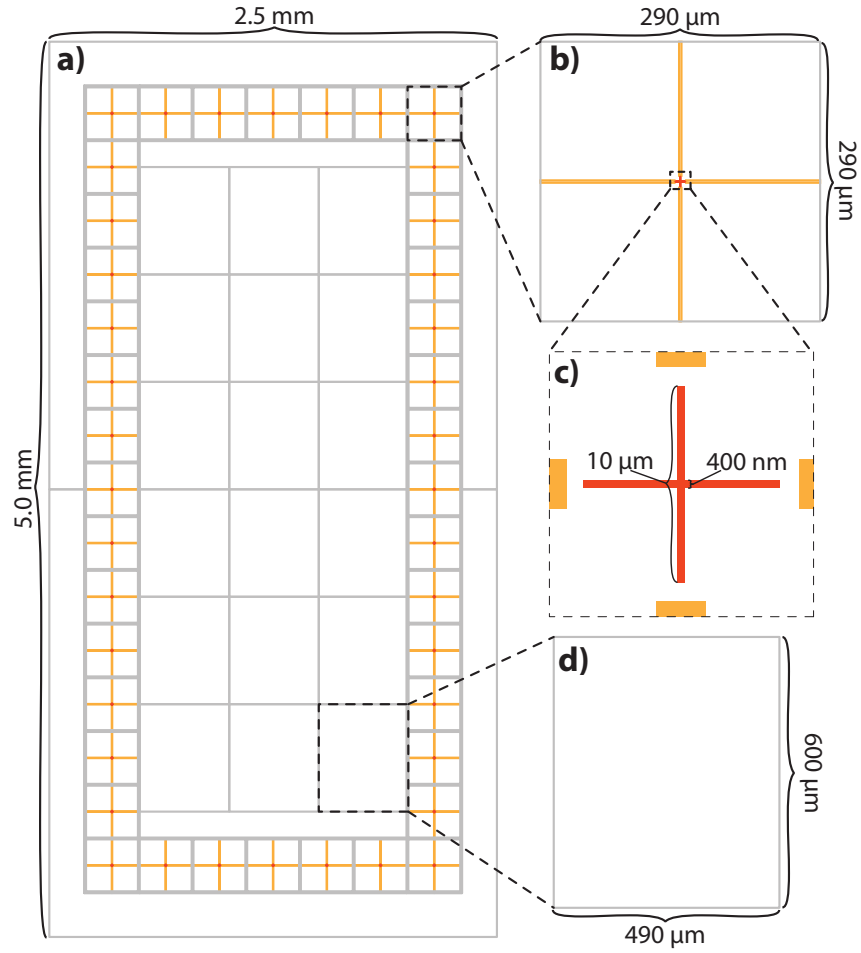


Figure 3.4.: **(a)** Overview of the design template of the $2.5 \times 5 \text{ mm}^2$ chips. **(b)** Zoom in on one of the alignment crosses. The big cross is used to pinpoint the inner alignment. **(c)** The inner cross is the actual alignment mark, used in lithography. **(d)** Shows size of the 18 device squares available on one chip.

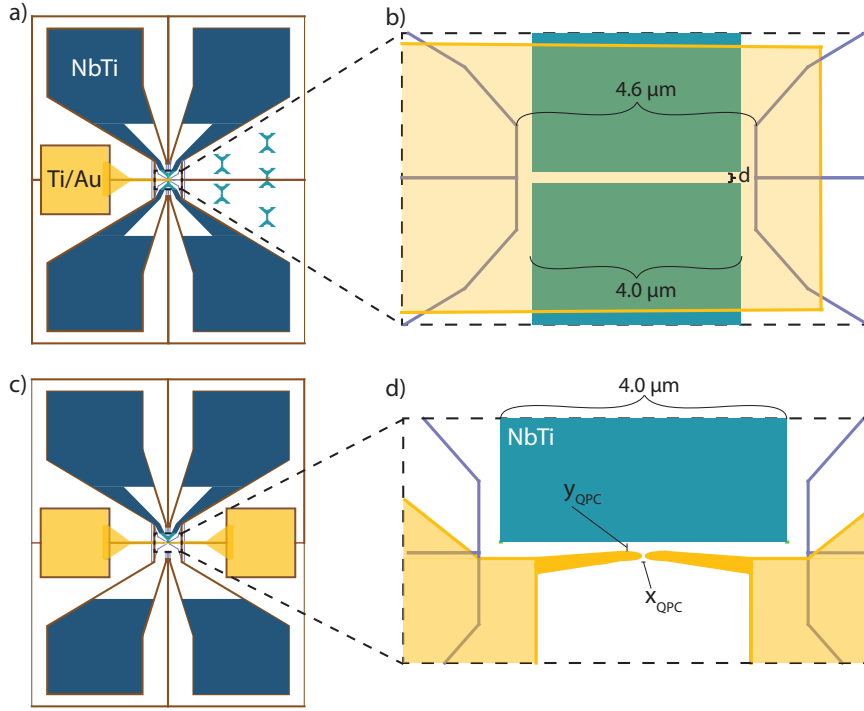


Figure 3.5.: **Designs for reported devices.** Dark- and light blue are outer and inner features for NbTi, respectively. All yellow structures are for Ti/Au deposition. These are made transparent to see features below. Brown and purple lines mark the boundaries for outer and inner mesa features respectively. **(a)** S-Sm-S device, four leads and one gate together with five tests for calibrations, located to the right. **(b)** Zoom in of S-Sm-S showing distances in the design files, including spacing between the superconductors, d . **(c)** S-QPC-Sm device, four leads and two gates. **(d)** Zoom in of S-QPC-Sm, defining the finger-to-finger-distance x_{QPC} and the QPC to superconductor distance y_{QPC} .

alignment marks. For some devices, alignment marks had to be utilized twice.

Designing Devices

Simple geometries, with up to 6 bonding pads, can fit in one of the 18 device squares highlighted on Figure 3.4(d). This could be a S-Sm-S or a S-Quantum Point Contact-Sm (S-QPC-Sm, elaborated in chapter 4) as shown in Figure 3.5(a-b) and (c-d). Larger devices like hall bars take up more squares, due to more than 6 bonding pads, see Figure 2.8.

When choosing which devices to fill in the 18 squares, it is recommended to include a few similar devices of each type, since many things can go wrong during fabrication, making some of the devices useless. Since we had to test a new deposition technique, we usually separated the 18 squares into 2-3 parts, each of these parts would have identical designs, but would be done by different depositions to increase the chance of having at least one success.

When needing to define small features, a low electron current is used, but using a low current to write big features can take multiple days. Instead, all designs were separated in fine inner features with low current and outer features with high current, making the whole writing much faster, but still precise where it is needed. For a lithography step, the alignment was done with the low current, followed by exposure of the inner features. Subsequently, the beam current was increased and the beam was calibrated, with waiting time before and after calibration. Lastly, the outer features were exposed.

For the reported devices the inner mesa and inner NbTi widths were $4.6\text{ }\mu\text{m}$ and $4.0\text{ }\mu\text{m}$ respectively, as shown on Figure 3.5(b,d). They are separated since the NbTi will spread due to it being sputter-deposited on a undercut resist, and the mesa etch will run, making the two values approach each other.

Figure 3.5(b) defines the spacing d between the deposited superconductors, while Figure 3.5(d) defines the QPC finger-to-finger-distance x_{QPC} and the QPC to superconductor distance y_{QPC} . d , x_{QPC} and y_{QPC} are variables worth changing within the same deposition.

The five inner NbTi structures in the center-right region of Figure 3.5 are tests, identical to the inner structure of the actual device, also with spacing d . After the NbTi deposition, the tests are analyzed with SEM to measure the actual spacing between the superconductors d' and the actual width of the contact. Thus, the length of the undercut d_{uc} can be determined by $d_{\text{uc}} = (d - d')/2$. d_{uc} is used to choose a proper value for y_{QPC} .

When bonding ², you push rather far into the substrate (depending on the settings). By bonding far into the substrate, one risks ending up in a conductive regime, thus creating leaks. Since the mesa etch at least removes a couple 100 nm, bonding in a etched regime might be fatal for devices. To prevent these kind of leaks, squares of mesa are placed under each top gate bonding pad.

3.2.2 NbTi(N) Deposition

The deposition of NbTi is the most important part of the fabrication and is also the one causing most problems. The steps are shown on Figure 3.6. I'll go through the steps, mentioning pitfalls along the way.

Choice of Resist Stack

Besides making the device pattern, the resist for this process needs two other qualities: undercut for sputtering liftoff of narrow features and a hard shell which can take large amounts of milling. A combination of MMA and CSAR is chosen, see Figure 3.6(b).

² Making electrical contact to devices, see section 3.3

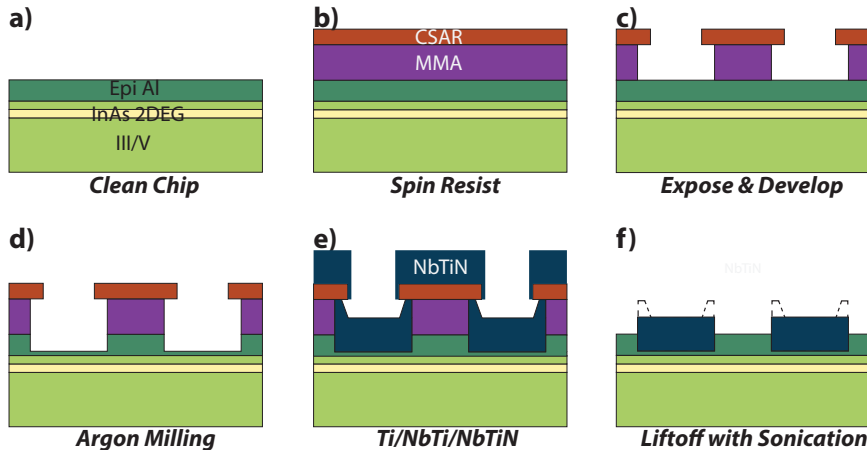


Figure 3.6.: **Overview of fabrication steps for NbTi(N) deposition.**

(a) Clean chip after the alignment mark deposition. (b) Spin a layer of MMA followed by CSAR. (c) Expose and develop design. The MMA/CSAR stack creates an undercut, which is useful when sputtering close spaced features. (d) Remove native aluminum oxide with Kaufman argon milling. Usually some of the aluminum is removed as well. (e) Deposit superconducting stack which should proximitize the Al. (f) Liftoff with sonication usually removes the sidewalls (marked by dashed lines) which are present due to sputtering.

Compared to the usual PMMA, MMA has shorter molecule chains and is therefore easier dissolved by e-beam and developer. When used under regular resist it therefore creates an undercut, see Figure 3.6(c), which is needed when sputtering narrowly spaced structures. In contrast to thermal evaporation, sputtered material moves diffusively, causing the material to crawl up the resist, see Figure 3.6(e). Without the undercut, a short would happen which is extremely hard to liftoff without damaging the rest of the chip.

CSAR is a physically resistant resist which can be milled for a long time without being trashed or hard baked (hard baked resist is *very* hard to strip). Using PMMA instead of CSAR would cause the milling to destroy the undercut. A thick layer of CSAR (CSAR13) was used, since it takes a lot of milling to remove native oxide of epitaxial aluminum.

Kaufman Argon Milling

To obtain proximity effect between the deposited superconductor (NbTi(N)) and the epitaxial aluminum, a low interface resistance is necessary, thus increasing the amount of Andreev reflections, as explained in section 2.3. The low resistance is obtained by removing the native oxide of the epitaxial aluminum, before deposition of the NbTi(N). The only *in situ* process available was Kaufman argon milling which bombards the substrate with Ar, thus removing material. The machine is known to be fluctuating and causing a lot of trouble. On top of it being fluctuating, the milling rate for Al is tens of times faster than the rate for aluminum oxide, making it difficult to stop

the milling before burning through the aluminum and into the III/V. This is why an aluminum thickness of 25 nm was chosen, see [Figure 2.7](#). Due to the low milling rate of aluminum oxide, a beam voltage of 600 V was chosen, for which the milling usually took $\sim 3:20 - 3:30$ min. Milling was done with a rotating sample plate, angled 15° away from perpendicular (in respect to the path of argon) to decrease milling time, and to be sure that the material in the resist undercut also got milled. For all settings, see [Appendix C](#).

The Kaufman has two kinds of fluctuations: a difference in rate between consecutive millings, and a long time drift in milling rate, most likely due to the argon source changing over time. Through many tests, it was found that a stable rate for consecutive uses could be obtained by heating up the machine: Before loading in any sample, the Kaufman was set to 600V and fired on an empty sample plate for ~ 10 min. Also after loading the sample, but before each use, the Kaufman was turned on for 2 min with a shutter protecting the sample.

Regarding the long term drift, a calibration before each use was necessary. This could be done with the InAs/Al substrate pieces, but the amount of material is limited and height differences are bothersome to measure. Instead a wafer with thick SiO_2 was used. The wafer was cut and cleaved into small pieces of $5 \times 5 \text{ mm}^2$. The thickness of the SiO_2 is easily measured by an reflectometer (aRTie from Filmetrics). The thickness is found by taking the mean of several scans. Etch depth is then the height difference before and after milling. Before SiO_2 can be used for calibrations, a conversion was needed. It was obtained by milling SiO_2 and MBE substrates simultaneously, then measuring the height differences of both materials after the process. Scrap MBE pieces (leftovers from cleaving) were used for these tests. To find the height difference of the MBE substrate, part of it was covered by aluminum foil before loading. It is important that the foil covers the substrate tightly, thus making sure that the covered part is not milled. After unloading, the height difference between the covered and unprotected parts were measured with an optical profilometer. It was found that $\sim 24.5 \text{ nm}$ SiO_2 is similar to milling through the aluminum oxide plus roughly halfway through the 25 nm Al.

With these calibrations and tests, I could obtain reproducible results in stopping the milling in the aluminum part of the MBE stack, see [Figure 3.6\(d\)](#). These results are presented in [Appendix D](#). The precise procedure is presented in [Appendix C](#).

Deposition: Evaporation & Sputtering

The superconducting stack used in fabricating the reported devices was a Ti/NbTi/NbTiN ($2/\sim 60/\sim 5 \text{ nm}$) stack, see [Figure 3.7](#). Ti is used as a sticking layer. Whether Ti is necessary or whether it decreases proximity effect (due to the inverse proximity effect from its very small Δ) is not known, since all devices without Ti were fabricated before the final milling recipe was made. Despite having a lower T_C , a thick NbTi layer was used instead

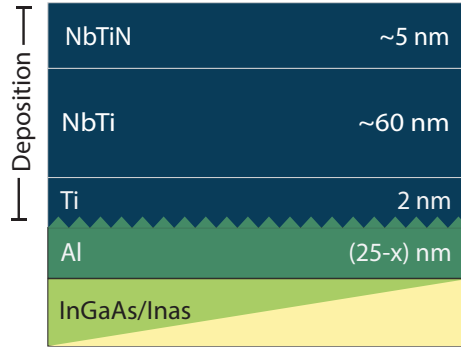


Figure 3.7.: Illustration showing the superconducting stack used for making the devices reported in [chapter 4](#) and [chapter 5](#). The ragged Al is due to milling. We don't know the exact amount of milled Al, but x should be within 5-20 nm. Due to earlier calibrations, we have a rough idea of the NbTi(N) thickness, but no easy means of measuring the exact number.

of a thick NbTiN layer since the former have produced more reproducible low contact resistances. The thin NbTiN layer is used to prevent the NbTi from oxidizing.

Ti was evaporated at an angle of 15° and under rotation to get it in the resist-defined undercut. NbTi(N) was sputtered with no tilt to reduce the thickness of the sidewalls which naturally form during sputtering, see [Figure 3.6\(e\)](#). The specific settings for the depositions are found in [Appendix C](#). If one is using a machine to deposit Nb, NbTi, NbN or NbTiN, for the first time, these articles [[10](#), [31–35](#)] are useful to read for choosing proper flow rates, pressures and thicknesses.

Liftoff with Sonication

Sidewalls from the sputtering can be troublesome for further fabrication. For narrow S-Sm-S devices, they might bend over and short the two super-

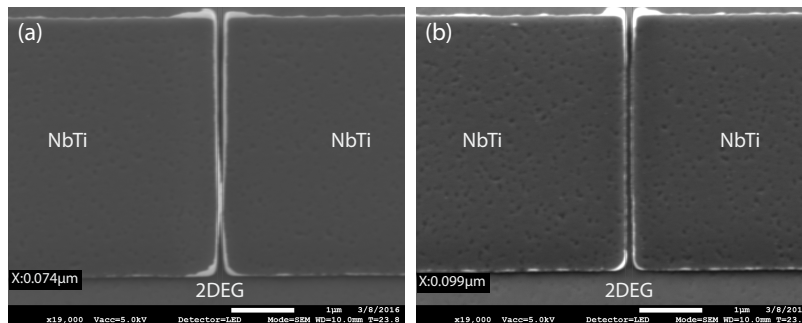


Figure 3.8.: Tilted SEM of narrow S-Sm-S test devices which were made simultaneously. Distances in the bottom left corners are measured spacing between the superconductors. **(a)** Sidewalls have collapsed and shorted the two superconductors **(b)** Most of the sidewalls were removed during lift-off.

conductors. Luckily a short is easy to observe with SEM, see [Figure 3.8](#). Though not tested, we believe that sidewalls make weak links after atomic layer deposition (ALD), which is used to electrically separate the substrate from top gates, used to deplete the 2DEG. This would explain the many shorts being observed between substrate and top gates on various devices.

One way to eliminate many of the sidewalls is sonication. After Ti/NbTi/NbTiN deposition, the chip was put in a beaker with Dioxolane and sonicated, then left in Dioxolane for more than one hour. Before taking the chip out, it is sonicated again. This procedure removed most of the side walls - sometimes more effectively than others. An exact recipe is found in [Appendix C](#).

The devices which produced the results reported in [chapter 4](#) and [chapter 5](#) were made with the superconducting stack displayed on [Figure 3.7](#). When deciding on the height of NbTi, two things should be taken into account: A thick layer might be hard to liftoff and sidewalls are harder to mill away. On the other hand, sputtered thin layers are strained, and this strain reduces the critical temperature of the deposited material [36]. A height of ~ 60 nm NbTi was chosen to compromise between the two.

3.2.3 *Al- & Mesa Etch*

In this step, isolated conducting regions, called mesas, are defined by etching past the 2DEG into the insulating part of the III/V heterostructure. In doing this, a lot of processes are made in quick succession, see [Figure 3.9](#). Performing these steps quickly limits the amount of oxidation between each step. During initial attempts however, it is recommended to inspect the chip under an optical microscope to make sure that the recipe is working as anticipated, see [Figure 3.10](#). It is also recommended to make all preparations before starting the first step and to have a partner during preparation and execution. For exact recipe details, inspect [Appendix C](#).

To begin with, the chip is cleaned, resist is spun, exposed and developed see [Figure 3.9\(a-c\)](#). The design is made so mesas are protected, see [Figure 3.10\(b\)](#). Again, the exposure is separated in inner and outer parts.

The aluminum is etched in 50°C hot aluminum etch type D (from Transene) followed by a 50°C hot MQ water rinse and a cold MQ water rinse. The etch rate heavily depends on the temperature of the etchant, so having a temperature of $50 \pm 1.5^\circ\text{C}$ is crucial for obtaining consistent results. It has been observed that without the hot water rinse, a lot of precipitate is found on the substrate after the etch. When working with aluminum etch type D, it is important to use CP-graded carbon tweezers, since others might dissolve, contaminating the solution. The etch time is dependent on the thickness of the aluminum, but usually 5-12 seconds. As for milling, the oxide etches slowly compared to pure aluminum, which makes the etch run a lot, if exposed to the etchant for too long.

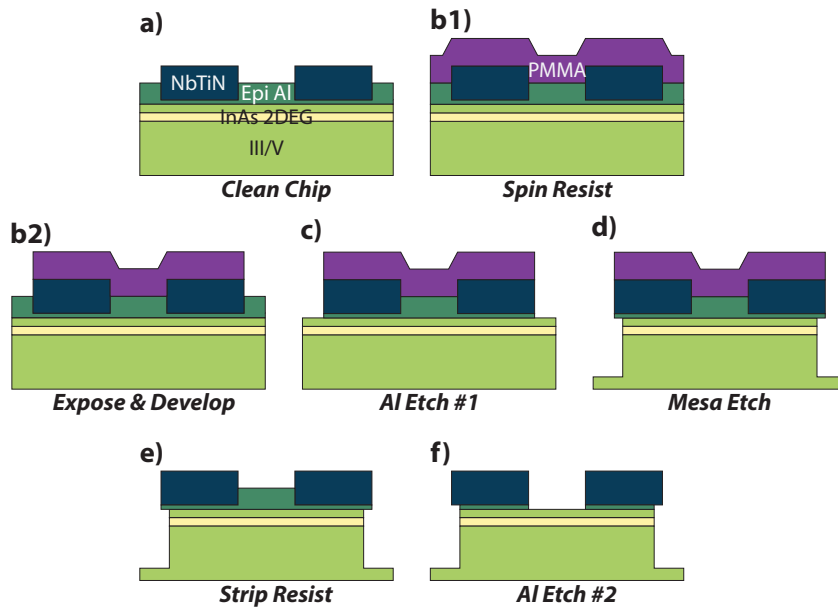


Figure 3.9.: **Overview of fabrication steps for mesa and Al etch.**

(a) Clean chip after NbTi(N) deposition. (b1) Spin regular PMMA. (b2) Expose and develop resist to protect the mesa region. (c) Etch aluminum in the etching region, to enable mesa etch. (d) Mesa etch crawls a bit under the superconductor. (e) Strip resist. (f) Etch aluminum in the mesa regions with NbTi(N) to enable gating of the 2DEG.

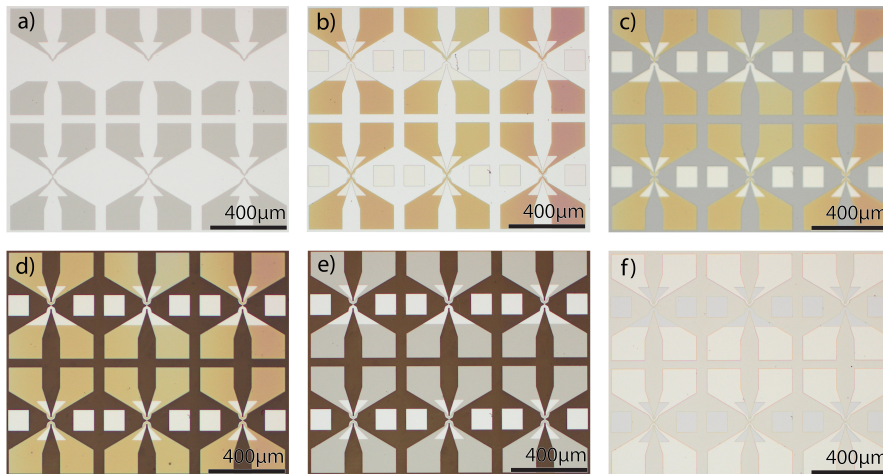


Figure 3.10.: **Optical microscopy after mesa and Al etch fabrication steps**

(a) Clean after NbTi(N) deposition. (b) Developed resist. (c) First aluminum etch exposing the III/V. (d) Mesa etch. (e) Resist is stripped. (f) Second aluminum etch.

Al is etched separately since the mesa etch solution used for etching III/V ($\text{H}_2\text{O} : \text{C}_6\text{H}_8\text{O}_7 : \text{H}_3\text{PO}_4 : \text{H}_2\text{O}_2$) does not attack aluminum, see Figure 3.9(d). The mesa etch time can vary depending on the substrate materials (antimonies are known to oxidize and etch fast) and on the desired etch depth. One should aim for getting down to an insulating regime in the heterostructure with no mesa-to-mesa leakage. However, going too far makes it hard to make successful top gates. The mesa etch also runs horizontally, see Figure 3.9(e).

After taking the chip out of the mesa etch solution, it is washed in two different MQ water baths to quench the reaction. Next, the resist is stripped, followed by another aluminum etch, with the same procedure as the first, see Figure 3.9(f-g). This last aluminum etch is used to remove all aluminum not covered by the Ti/NbTi/NbTiN stack, hence enabling gating of the 2DEG through topgates.

3.2.4 Oxide Deposition by ALD

Before depositing Ti/Au for the topgates, a dielectric is needed to ensure a capacitive coupling between 2DEG and topgates. For InAs 2DEGs with epitaxial Al, both Al_2O_3 and HfO_2 have shown good and bad results. Both materials are deposited with atomic layer deposition (ALD), which is a process that nucleates one atomic layer at a time on all surfaces of the chip. It was discovered that for both materials, slow growth at low temperature gives the highest success-rate.

Any weak links, breaking the capacitive coupling, introduce unintended leakage currents, rendering the gates useless. Weak links can happen due to bad ALD growth or e.g. sidewalls (from sputtering) breaking after ALD. The latter is not proven, but empirical observations suggest it.

In addition to acting as a dielectric, ALD also shields the underlying materials from further corrosion or other chemical damage. After ALD, the mesa etch depth is measured with a profilometer. The depth is necessary to know before depositing top gates.

3.2.5 Gate Evaporation

The gate evaporation is done in two or three lithography steps.

1. A thin layer for fine inner features, like QPC-fingers, see Figure 3.5(d)
2. A thick layer to connect bonding pads to inner structures
3. In case the first thick layer was not enough to crawl up the mesas, another thick layer is added to ensure contact.

When making QPCs, the limit of e-beam lithography is being used to obtain 20nm precision in placement and definition of the finger gates. For 2DEGs close to the surface, $x_{\text{QPC}} \sim 100 \text{ nm}$ has been found successful, while y_{QPC}

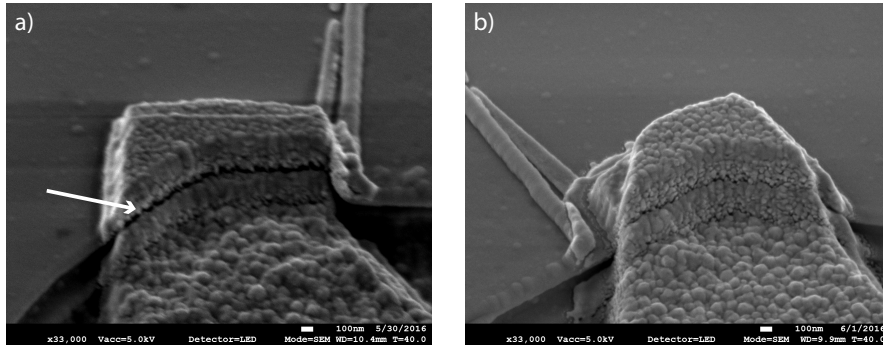


Figure 3.11.: **SEM after top gate evaporation**
 (a) Disconnected topgate. The black line, marked by the white arrow, is where the gate is disconnected. (b) Successfully connected top gate, without black lines as on (a).

should be as small as possible to probe the real Δ^* under the superconductor. A thin PMMA resist is used for lithography. A 100 pA e-beam current is used and under 50 nm of Ti/Au is thermally evaporated followed by liftoff. No tilt was used during evaporation.

For the outer parts, an e-beam current of 20 nA was used together with a thicker resist for easier liftoff. For very thick contacts, an undercut resist PMMA on MMA is recommended. Remember to take the undercut into account in the lithography design. The amount of evaporated material depends on the mesa etch depth. If an insufficient amount of gold is deposited, the physical and electrical contact between the bonding pad and the inner features will be broken at the mesa edge walls. This can be observed with SEM, see Figure 3.11(a). A rule of thumb is to evaporate, without tilt, a stack as thick as the mesa etch depth, followed by 50nm at a short angle. It is recommended to verify with the SEM, and it should look like Figure 3.11(b). If necessary, deposit a third layer.

When done with fabrication, it is recommended to take quick SEM of all devices to check whether they look good. Whether SEM can damage the devices or not, is not known, but we haven't observed signs of damage yet.

All of the methods mentioned in this section were used to fabricate the two devices reported in chapter 4 and chapter 5. The two devices were made from the same deposition. Two other depositions, using identical recipes and designs, were made and measured on the same chip. A comparison of the three depositions is given in Appendix D. In short, all three depositions improved the superconducting properties of the proximitized InAs 2DEG, though not equally.

3.3 REFRIGERATION

All quantum phenomena described in theory is, unless otherwise stated, for systems at absolute zero temperature, $T = 0$. This limit is unphysical

and unobtainable in a laboratory, but due to technological advances over the recent decades, it is now possible to get rather close to $T = 0$ by the use of sophisticated methods. The reason that low temperatures are necessary, is that even small thermal fluctuations can wash out measurable quantum signatures. One example is the determination of Δ of a superconductor. As shown by [Figure 2.1\(b\)](#), the size of Δ decreases for higher temperatures.

There are two important properties that a cooling method should have. Most crucial is the lowest temperature obtainable. Another, is the ability to controllably increase the temperature, to make temperature dependent measurements e.g. to measure T_c of a superconductor.

This section will provide need-to-know knowledge of the dry dilution refrigerator, used to produce results presented in this thesis. In a wet fridge, the sample is immersed in the cooling liquid. In a dry fridge, the cooling liquid is contained in pipes and tubes which are thermally coupled to the sample. The dilution refrigerator has a low minimum temperature of a few millikelvin, but it is troublesome (though not impossible) to increase T much higher than 2 K. A ^4He wet fridge can't get below 4.2 K, but it is rather easy to make temperature sweeps way beyond 20 K, where conventional materials lose their superconductivity.

Before we cool down though, we need to have electrical contact to the devices.

3.3.1 *Preparing for Cooldown*

There are many ways to make electrical contact between devices and a fridge. We choose to use an aluminum threaded wire bonder. Before bonding, the chip is stuck to a daughterboard by the use of resist. With a wooden toothpick, a small resist droplet is placed on the daughterboard and with a tweezer, the device chip is placed on the droplet. The daughterboard with resist and chip is then placed on a 115 °C heating plate for 5 min to harden the resist.

If magnetic measurements are needed, one should carefully place the chip to be parallel with the daughterboard, see [Figure 3.12\(a\)](#), which will make it easier to align the vector magnet to the devices on the chip, see [Appendix E](#). The orientation, x vs y (as shown on [Figure 3.12\(a\)](#)), should be chosen according to magnetic field directions which are elaborated below.

Before beginning the bonding, it is recommended to print out a pin-out sheet from the QDev wiki ³, put in your design schematic on it and make a plan for the bonding. The plan should both include what devices to bond and where to bond them - try to reduce the amount of ninja bonds⁴.

The wire bonder pushes the Al wire through the substrate, thus making contact with the 2DEG. This process is rather rough to the substrate, local to the bond, but it has a very high precision (when performed by an experienced

³ See https://wiki.nbi.ku.dk/qdevwiki/Sample_Holders

⁴ Ninja bonds: multiple bonds going under and above each other.

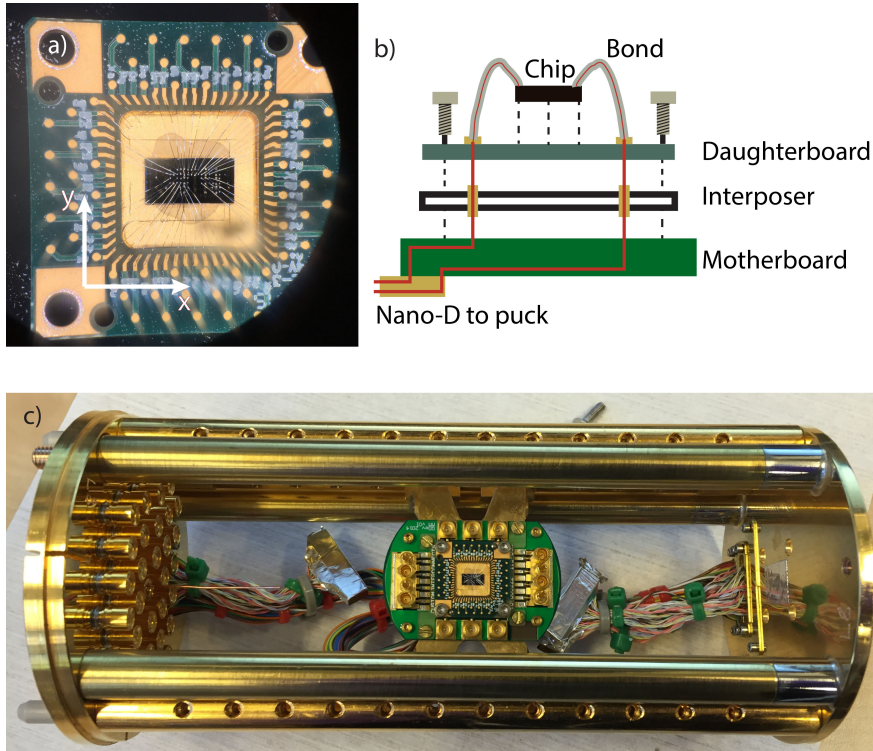


Figure 3.12.: **Mounting chip to puck**

(a) Chip mounted and bonded to daughterboard. Picture is taken through microscope glass. (b) Schematic showing the components needed to mount a chip to a puck. The red lines show how current can run from the chip through bonds to daughterboard and through fuz buttons in the interposer down to the motherboard connected to a Nano-D going to the puck. (c) Picture of an open puck with mounted boards and chip.

user) thus making it favorable. The other end of the wire is bonded to the daughterboard. After bonding to the chip, inspect it with a microscope, see Figure 3.12(a), to check whether the bonds are where they should be.

The daughterboard can now be mounted on a motherboard with an interposer with fuz buttons, see Figure 3.12(b). Thermal and electrical contact is ensured by tightening four screws. The motherboard can be placed in a puck, either along or perpendicular to the puck's long axis, see Figure 3.12(c). The puck can then be attached to a fridge. Our dilution refrigerators have vector-magnets, usually with 1 Tesla in two directions and 6 Tesla in the last. The direction of the strong field is parallel to the long axis of the puck, so for all reported measurements the motherboard was oriented as shown on Figure 3.12(c), since small out of plane fields quickly quench superconductivity.

Before loading and cooling of the device, the connection of all bonds are tested at room temperature, as explained in subsection 3.4.1. If a lot of lines have bad electrical contact, then these lines are re-bonded and tested again. That process is continued until a satisfactory small amount of lines have bad electrical contact.

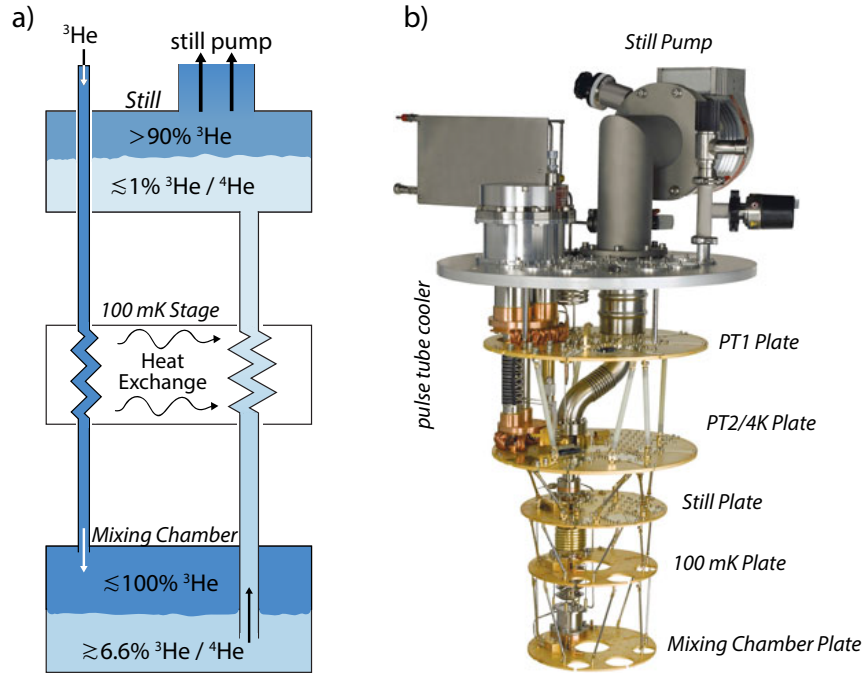


Figure 3.13.: (a) Simplified schematic showing the most essential dilution cryostat parts in getting to sub-Kelvin temperatures. (b) Picture of the inner parts of a Triton cryofree dilution refrigerator, similar to the one used in doing experiments⁵.

3.3.2 Dry Dilution Refrigeration

The $^3\text{He}/^4\text{He}$ dilution refrigerator is what enables measurements of condensed matter at millikelvin temperatures. There are great books, like Pobell[37], that give a detailed explanation; both of the physics and the engineering. This subsection will give a brief overview of some of the most important details.

To cool a system down, one can pump a liquid in that system. The hottest particles of the system, those in vapor phase, are removed thus cooling the system. This leads to a cooling power proportional to the vapor pressure. Why use a $^3\text{He}/^4\text{He}$ dilution? To begin with, the two isotopes are the only liquids that do not become solid under their own vapor pressure, even at $T = 0$ K. The two isotopes are also the only with finite vapor pressure around 1 K, but not in the millikelvin regime, making regular evaporation insufficient to reach the millikelvin regime.

For a $^3\text{He}/^4\text{He}$ dilution, the cooling is obtained by pumping a ^3He rich phase into a ^4He rich phase in the mixing chamber, see Figure 3.13(a). The latter phase has a higher enthalpy, causing the process to cool the system. The separation of the two phases happens at $T < 0.87$ K due to the quantum nature of the two isotopes, [37]. Even at $T = 0$ K the ^4He

⁵ <https://www.oxford-instruments.com>

rich phase has a finite solubility, thus enabling cooling. To keep the process going, ^3He is continuously extracted from the ^4He rich phase by pumping on the still, keeping the dilution from obtaining equilibrium. The puck is mounted in thermal contact to the mixing chamber plate, thus cooling the sample. Due to practical reasons, a few millikelvin is the lowest accessible temperature. This usually results in an effective electron temperature of ~ 100 mK. Thermal fluctuations ($\sim k_B T$) at these temperatures are too small to hide the quantum phenomena we want to measure. Sourced electrons are cooled before reaching the sample by thermally coupling wires to the different temperature stages/plates, see Figure 3.13(b). The thermal contact is enhanced through heat sinks, RC-filters ($0.1 - 4.1\text{k}\Omega$ & 2.7nF) and RF-filters (π -filters). The filters block high frequency electrical signals from reaching the sample. All the lines going down to the sample are controlled by a break out box in front of the fridge.

3.3.3 High Temperature Control in Dilution Fridge

When doing measurement sweeps at different temperatures, it is of course important that the temperature is somewhat constant during each sweep. Doing the measurements with a dilution refrigerator makes it troublesome to obtain stable high temperatures due to the many different phase transitions of the ^3He , ^4He , and their mixture, causing a lot of temperature jumps. The way to work around this was to monitor the temperature during the sweeps and then add cooling/heating power if needed. A lakeshore unit reads out the temperatures in the fridge and controls the heaters located inside the vacuum chamber. The heaters can be used to increase the temperature of the helium mixture and thereby the sample. The LakeShore unit has a PID loop to stabilize temperature up to 2.2 K. For $T > 2.2\text{K}$ we are forced to do manual temperature control.

When going for high temperatures, it is a good idea to collect some of the mixture in the mixture tank. This is done to prevent excessively high pressures in the pipe lines. The higher you wish to go in temperature, the more mixture should be collected. The mixing chamber is heated by turning up the power on the heaters, which can be done manually on the LakeShore display. If the mixing chamber is getting too hot, the forepump can be turned on, which quickly lowers the temperature, making it unfavorable to use for precise control. It should be noted that the pressure valve located after the forepump must not exceed 1 bar, and the pressure increases fast when using the forepump at "high" temperatures.

Optimally, a pressure and temperature should be found, at which the heat-gradient is not too large. When such a setting is found, only very small changes in heating power are needed to keep the temperature stable at the wanted value. An efficient way to keep track of the temperature is to couple the LakeShore to a DMM with a BNC cable. Then the temperature can be read out as a voltage on the DMM, which can be monitored and

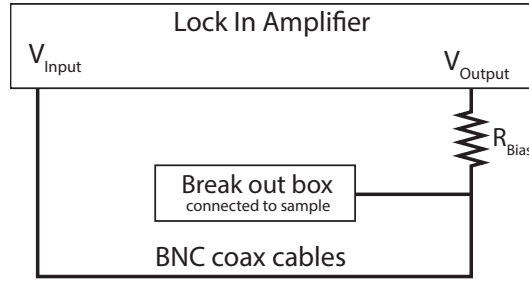


Figure 3.14.: Circuit used to check resistance of all bonded lines, one at a time.

stored in Igor (The program we used to control and do measurements). Such temperature measurements are displayed on Figure 5.2(b). The continuous DMM output can also be used to trace a value as a function of temperature, see Figure 5.2(d) where resistance at zero current bias was traced.

3.4 ELECTRONIC SETUP

In this last section, I'll go through the three different measurement circuits used for acquiring data.

3.4.1 Checking Resistance of Bonded Lines

Before cooling down, the resistance of all bonded lines are measured one by one, to see whether some of them should be re-bonded. Figure 3.14 shows a circuit schematic. A Nano-D to Fischer converter connects the puck to a breakout box. On the breakout box, all channels are grounded with exception to the one connected to the tested device line. The voltage through the line to ground is measured while sourcing a controlled current (1 – 10 nA), thus extracting the resistance. After cool-down, prior to other measurements, the lines are checked again, since some might have frozen out. Mesa-to-mesa leakage should also be checked to prevent unnecessary confusion when measuring.

3.4.2 Current-Bias

The resonances analyzed in the S-Sm-S junctions, see chapter 5, are all of size $\sim 0 - 100 \Omega$. With these low resistances, current bias is the preferred measurement technique. See circuit on Figure 3.15(a). A resolution of $I_{AC} = 5 \text{ nA}$ was obtained by sourcing 2.5 V from the Lockin with $500 \text{ M}\Omega$ in series. The bias current (sourced with a DAC) resolution was set well below $I_C \approx 8 \mu\text{A}$ by a bias resistance of $100 \text{ k}\Omega$. The drain contact was grounded to minimize noise. A voltage preamp with $\times 100$ amplification was used to enable, precise readout of both AC and DC by lockin and DMM respectively.

A Keithley was used to source the gate voltage since it simultaneously can measure if any current leaks through the oxide.

3.4.3 Voltage-Bias

When measuring with the QPC in the tunnel regime, see [chapter 4](#), resistances are way too high for current bias, so voltage bias is used instead. The circuit used for measuring S-QPC-Sm is shown on [Figure 3.15\(b\)](#). A voltage divider enables sourcing of voltages in the sub- μV range, sufficient to resolve the features around the gap $\Delta > 200 \mu\text{eV}$. A excitation voltage of 5 or 10 μeV was used for all experiments. The current is amplified by 10^7 or 10^8 with an Ithaco preamplifier and measured with lockin and DMM. The voltage drop is measured alike current bias. The differential conductance $G = dI/dV$, is found by dividing measured AC current with AC voltage.

In the deep tunnel-regime, current starts leaking to ground through the voltage preamplifier. To prevent this, the voltage preamp is unhooked and a 2-terminal measurement of current is used instead. Here the conductance is found by numerical differentiation of the measured $I_{\text{DC}}(V_{\text{sd}})$. As for the current bias setup, a Keithley is used for sourcing gates, to enable measurements of possible leakage currents. For all measurements, the two QPC fingers were sourced symmetrically.

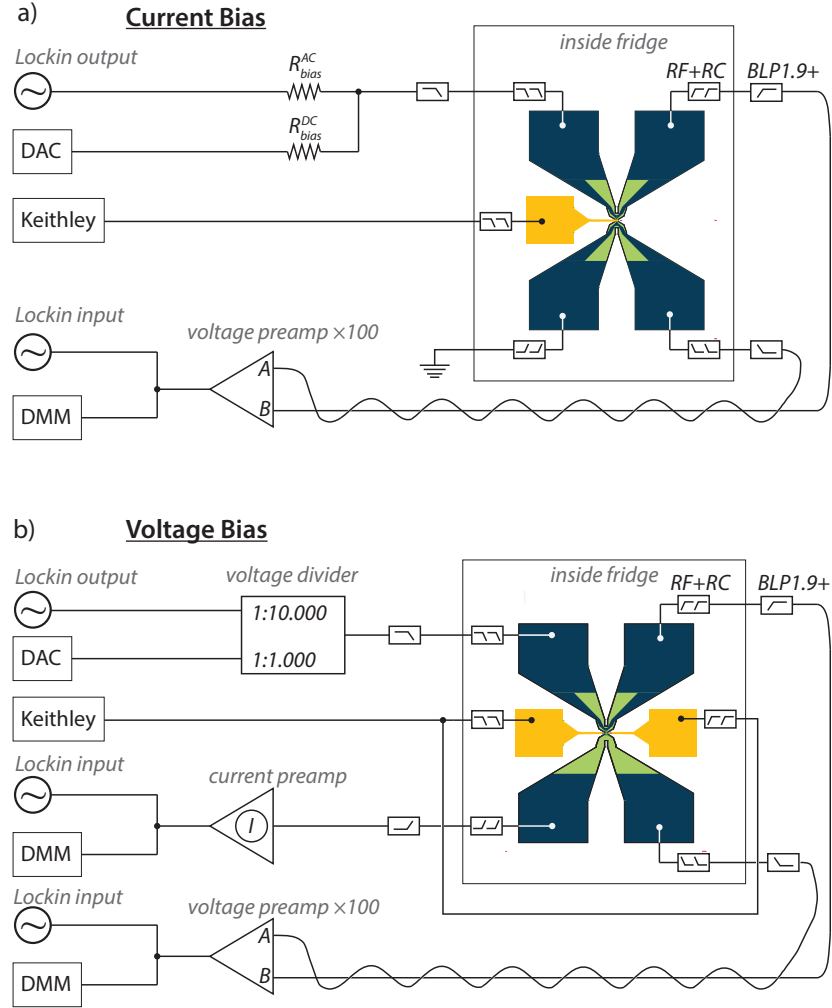


Figure 3.15.: **(a)** Current bias 4-terminal circuit used to measure the low resistances of S-Sm-S devices. The RF and RC filters are those mounted to the fridge, mentioned in the text. BLP1.9+ is a 1.9 MHz low pass filter from Mini-Circuits. A Keithley was used to source gate voltage while simultaneously tracking leakage current. **(b)** Voltage bias 4-terminal circuit used to measure the high resistances in the tunnel regime of S-QPC-Sm devices. When in the deep tunnel regime, a 2-terminal DC setup, with the voltage preamp unhooked, was used to lessen noise. For all measurements, the gate voltage was applied symmetrically on the two QPC fingers.

TUNNEL SPECTROSCOPY AT THE NBTI-AL/INAs INTERFACE

Tunnel spectroscopy enables us to measure the local density of states (LDOS) of quasi particles in a system. It is possible to do since the LDOS is proportional to the differential conductance in the tunneling regime which can be measured [23]. One way to probe the LDOS of a superconductor is through a scanning tunneling microscope (STM) [22]. When working with 2DEGs, a quantum point contact (QPC) can also be used [38]. A quantum point contact is a 2DEG with tightly spaced top gates, the QPC fingers, see Figure 3.5(d) or Figure 4.1. Driving a certain negative gate voltage through the fingers depletes the 2DEG under them. Increasing the negative voltage further squeezes the channel in between the fingers allowing fewer and fewer modes of electrons in the constriction until reaching the tunnel regime with transmission of $\mathcal{T} < 1$. For more details on QPCs inspect the pioneering work [39, 40].

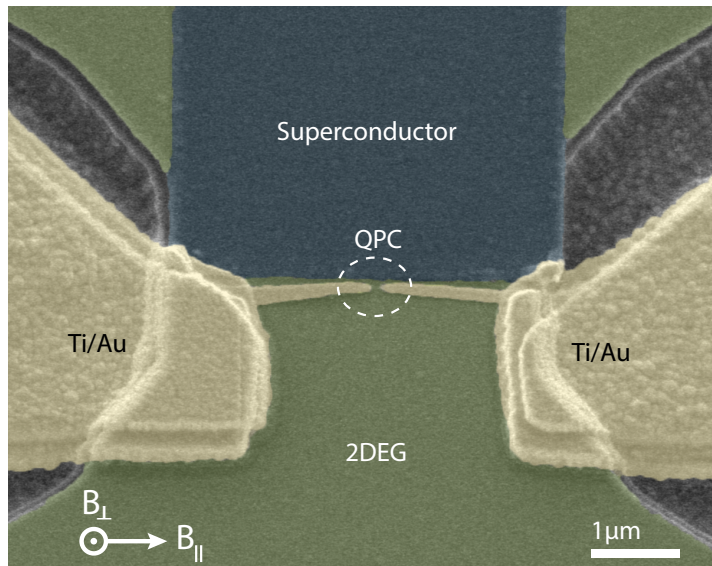


Figure 4.1.: SEM of S-QPC-Sm device. The superconductor stack is shown on Figure 3.7. The QPC is <100 nm from the Super-Semi interface. Magnetic field directions are defined in the bottom left corner.

This chapter will present results measured with a Superconductor-QPC-Semiconductor (S-QPC-Sm) device, with Sm being an InAs 2DEG, see Figure 2.7, and S being NbTi on epitaxial Al, see Figure 3.7. A scanning electron microscope (SEM) image of the specific device is shown on Figure 4.1. The QPC is placed very close to the S-Sm interface ($y_{\text{QPC}} < 100$ nm, see Figure 3.5(d)), making it suitable for probing quasi particles interacting with the S-Sm interface. The circuit used for these measurements is shown on Figure 3.15(b).

4.1 TUNNEL SPECTROSCOPY OF INDUCED GAP

After verifying a low resistive electrical contact in all connected lines (explained in subsection 3.4.1), the second-first thing to measure is whether the QPC gates leak, which would cause unintended currents, I_{leak} , to run from the gates into the 2DEG. That check is done by measuring I,V (both AC and DC) and the leakage current, I_{leak} , at zero bias, while sourcing a negative V_{gate} with the Keithley. The AC and DC currents, $I_{\text{AC,DC}}$ indicates when the QPC is in the tunneling regime in other words, when the $I_{\text{AC,DC}}$ is pinched off by the QPC: $I_{\text{AC,DC}} \sim 0$. A more strict definition of the tunneling regime is given by the differential conductance, $dI/dV = I_{\text{AC}}/V_{\text{AC}} \ll 2e^2/h$.

We measured a leakage current of $I_{\text{leak}} < 1$ nA in the tunneling regime, which is small enough to assume it does not affect conductance measurements. If $I_{\text{AC,DC}}$ is not significantly affected by the gate voltage at > 10 V, it might be due to the gate-contact not crawling properly up the mesa, see Figure 3.11. As seen below, we could pinch off the 2DEG on this device. There was no leakage at base temperature of the dilution refrigerator.

Figure 4.2 shows two sweeps of differential conductance dI/dV as a function of V_{gate} , obtained by $dI/dV = I_{\text{AC}}/V_{\text{AC}}$, showing a pinch off at

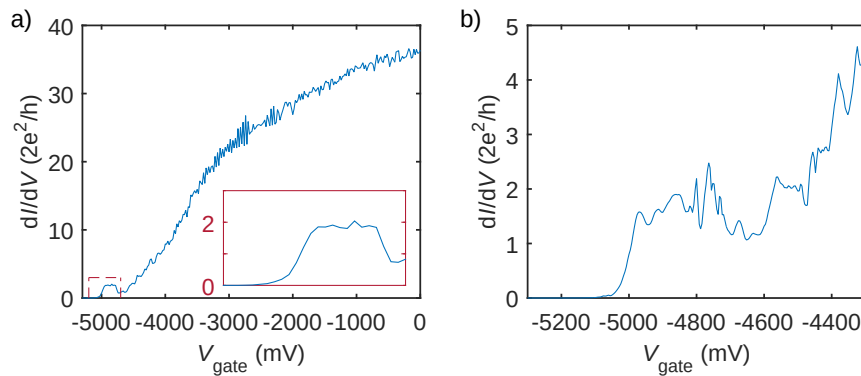


Figure 4.2.: Differential conductance dI/dV as a function of negative gate voltage V_{gate} **(a)** First trace taken on this device. It is not representative of the general data. The inset is a zoom-in on the plateau before pinch off. **(b)** A more representative trace, showing the general trend at low conductance

~ -5100 mV. Figure 4.2(a) displays the first gate sweep on this device showing a promising conductance step at $\sim 4e^2/h$ (see zoom in the inset) as predicted by Beenakker [41]. This will also be elaborated in section 4.2. All subsequent sweeps from the device did not have as clean plateaus at $\sim 4e^2/h$, but they still show a tendency of having the first plateau at $\sim 4e^2/h$ compared to $\sim 2e^2/h$. A good representation of these other sweeps is shown on Figure 4.2(b).

After verifying a successful current pinch off, we usually make a quick characterization of the induced gap, which is done by measuring dI/dV as a function of source-drain(bias) voltage V_{sd} . The actual important voltage drop is that across the device, V_{Dev} , which can be measured directly by a 4-terminal measurement. This is smaller than the applied V_{sd} , since some voltage will drop across the filters of the lines going from the voltage output to the device, see Figure 3.15(b).

When measuring differential conductance, two things should be taken into account when choosing a point in gate voltage-space for the measurement. When going further into the tunneling regime the dI/dV measurement resembles LDOS better [20]. On the other hand, the conductance signal gets weaker and weaker as we deplete the 2DEG. As a compromise, a gate voltage at which the normal conductance is $\sim 0.1 \cdot 2e^2/h$ is usually chosen. To get into the normal conducting regime, simply bias the system with $V_{sd} \gg \Delta^*/e$. Here Δ^* is the induced gap in the InAs 2DEG from the NbTi/Al stack on it, see section 2.5.

One such trace is shown on Figure 4.3(a), taken at $V_{gate} = -5194$ mV. The induced gap, Δ^* , is extracted as half the peak-to-peak distance, where the peaks are taken as the value of V_{Dev} corresponding to the highest value of dI/dV . The same definition of the superconducting gap Δ is used for the theoretical BCS DOS, see Figure 2.1(a). We extract $\Delta^* = 0.43$ meV which is a

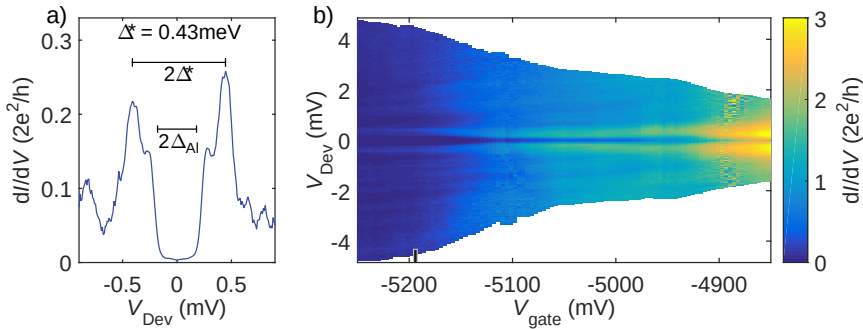


Figure 4.3.: **(a)** Differential conductance, dI/dV , as a function of the voltage drop across the device, V_{Dev} . The trace is taken at a gate voltage for which the normal conductance is $\sim 0.1 \cdot 2e^2/h$. The size of the induced gap, Δ^* is taken as half the peak-to-peak distance and is compared to gap of bulk aluminum $\Delta_{Al} = 180 \mu\text{eV}$. **(b)** 2D map of dI/dV as a function of V_{Dev} and gate voltage V_{gate} . The gate voltage at which (a) is extracted $V_{gate} = -5194$ mV is displayed. Measured in a 4-terminal configuration.

factor ~ 2.3 larger than measured in a similar material system where Al was the only superconductor [38]. Their observed value was close to that of bulk Aluminum, Δ_{Al} , shown as length scale in Figure 4.3(a) for comparison. The fact that the observed superconducting gap is larger than what was observed in aluminum shows us that the NbTi has proximitized Al and thus InAs. Compared to a BSC DOS, the conductance peaks on Figure 4.3(a) are rather broad and have shoulders/sub-gap peaks.

As mentioned above, electrostatic gates can be leaky or broken (with no electrical contact to the bonding pad). A third unfortunate property of electrostatic gates is switches. Charges jumping to and from an impurity or defect can change/switch the conductance at a given V_{gate} . Both small and large switches can happen, with only the latter being troublesome. Optimally the mean time between large switches, t_{switch} , should be longer than the time it takes to do a measurement, which for 2D maps might be several hours. Switches can for example happen due to: Poor MBE growth, poorly grown ALD, and/or impurities at one of the interfaces in the III/V - ALD - Ti/Au stack. On the reported device t_{switch} was on the order of several hours making it possible to obtain 2D sweeps with only small switches.

Figure 4.3(b) shows a measurement of the dI/dV vs V_{Dev} for V_{gate} ranging from -4950 mV to -5250 mV. The source drain voltage was swept from -5 to 5 mV. As the gate voltage is increased (negatively), the resistance of the QPC constriction increases causing a larger percentage of the voltage to drop across the device.

The data shows that a gap around zero voltage is present from the 1-channel conductance regime and all the way into the tunneling regime. There are two rather noisy regimes at $V_{\text{gate}} \sim -4900$ mV and -5100 mV, and otherwise only small switches around ~ -4950 mV.

4.2 QUALITY OF S-SM INTERFACE

As mentioned in the prior section, the LDOS in Figure 4.3(a) does not have steep and narrow conductance peaks like a BCS density of states as Figure 2.1(a). This soft-looking gap could make people question the S-Sm interface transparency. To extract information about the S-Sm interface, we compare our data with Beenakkers article [41]. He analyzes a S-N interface with *perfect* Andreev reflection and finds that the conductance of a single channel/constriction close to the interface (on the N-side) is given by

$$G_{\text{NS}} = 2G_0 \frac{\mathcal{T}^2}{(2 - \mathcal{T})^2}, \quad (4.1)$$

where $G_0 = 2e^2/h$ and $\mathcal{T}$ is the transmission through the constriction. In the case of the superconductor being in the normal conducting phase, the conductance is the known [39, 40]:

$$G_{\text{NN}} = G_0 \mathcal{T}. \quad (4.2)$$

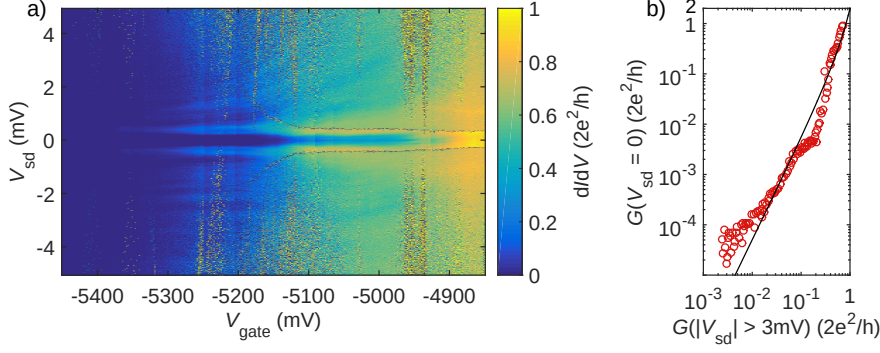


Figure 4.4.: **(a)** Differential conductance, dI/dV , measurement as a function of source drain voltage V_{sd} and gate voltage V_{gate} obtained by numerical differentiation of I_{DC} measured 2-terminal. **(b)** Conductance close to zero bias $G(V_{sd} = 0)$ vs conductance at high bias $G(|V_{sd}| > 3\text{mV})$, compared to theory for a *perfect* S-N interface, Equation 4.3. The data, which is extracted from (a) for each V_{gate} value, is slightly binned.

Chang et al. [30] introduced the idea of combining Equation 4.1 and Equation 4.2 writing G_{NS} as a function of G_{NN} :

$$G_{NS} = 2G_0 \frac{G_{NN}^2}{(2G_0 - G_{NN})^2}. \quad (4.3)$$

This expression is a theoretical prediction of the correlation between G_{NS} and G_{NN} with the same $\mathcal{T}$. The first plateau of a constriction's conductance (going from tunneling regime towards $V_g = 0$) occurs when one electron mode can pass through it: $\mathcal{T} = 1 \rightarrow G_{NN} = G_0$. For a one mode constriction connecting N and S, Equation 4.1 or Equation 4.3 then gives $G_{NS} = 2G_0 = 4e^2/h$, which was observed in Figure 4.2(a). This enhanced conductance is due to quasi particles Andreev reflecting at the interface. For a S-QPC-Sm device, $\mathcal{T}$ is the transmission through the QPC controlled by V_{gate} . G_{NS} is the conductance around zero bias and G_{NN} is the conductance at bias $V_{Dev} \gg \Delta^*/e$. Thus a 2D map like Figure 4.3(b) enables us to compare data with a theory for a perfect transparent S-Sm interface, even without fitting parameters, as done in [10, 30, 38]. Fitting parameters are not needed since the measured correlation between G_{NS} and G_{NN} are simply plotted together with Equation 4.3. As mentioned, the theory is based on a single-channel assumption and applies to $\mathcal{T} \leq 1$. Data should cover as many $\mathcal{T}$ (gate voltages) in this regime as possible to show a good agreement with theory.

As explained in subsection 3.4.3, the resistance of the QPC constriction in the deep tunneling regime is on the order of input impedance of the voltage preamplifier (Figure 3.15). This makes 4-terminal measurements insufficient for acquiring low $\mathcal{T}$ (high negative V_{gate}) data. Instead the voltage preamplifier can be unhooked and only current is measured. The current measuring lockin can also be unhooked to speed up data acquisition. As mentioned in section 4.1, the bias voltage is not equal to the voltage drop

across the QPC, due to some of the voltage dropping across the lines. How V_{Dev} is extracted in a 2-terminal setup, is elaborated [Appendix F](#) together with application on the 2D sweep.

With the 2-terminal setup a bias-gate sweep is done again, now going further into the tunneling regime, while only measuring I_{DC} . The bias sweep at each gate voltage step is numerically differentiated to obtain a conductance map, shown on [Figure 4.4\(a\)](#). Even though the data is obtained during a different cooldown, it is comparable to the AC measurement, [Figure 4.3\(b\)](#). A lot of noise at high bias is visible on [Figure 4.4\(a\)](#) similar to but more dense than the noise observed from the AC measurement. The extra noise could be an artifact due to the numerical differentiation¹.

With [Figure 4.4\(a\)](#) at hand, we can compare our data with Beenakker's theory, [Equation 4.3](#). The conductance in the gapped region, G_{SN} was taken as the mean conductance of the 42 points closest to $V_{\text{sd}} = 0$ ², and G_{NN} was taken as the mean of all $|V_{\text{sd}}| > 3$ mV. The result is displayed on [Figure 4.4\(b\)](#), showing a good agreement with the theory up to 4 orders of magnitude in G_{NS} , indicating that the S-Sm interface has close to perfect transmission.

4.3 MAGNETIC FIELD DEPENDENCE OF INDUCED GAP

For many practical applications it is important to know the field dependence of the induced superconductivity. One example is getting into the topological regime for a S-Sm devices. This regime is obtained for fields where $g_{\text{Sm}}\mu_{\text{B}}B > \Delta^*$ with the native superconductor (in this case the proximitized Al) retaining its gap [\[38\]](#). Here g_{Sm} is the g-factor in the Sm.

The QPC can also be used to probe field dependence. One simply finds an appropriate V_{gate} with $G_{\text{NN}} \sim 0.1G_0$, and do bias sweeps at different fields in a 2D sweep. This of course assumes that the device is aligned with the axes of the vector magnet in the dilution refrigerator. That is rarely the case, but since it is a vector magnet an alignment can be done, see [Appendix E](#). If an alignment is not done, an applied field $B_{\parallel}$, might have significant components in all axes of a device, making the data hard to interpret. [Figure 4.1](#) defines the axes used for measurements on [Figure 4.5](#).

[Figure 4.5\(a\)](#) shows a bias and in-plane field, $B_{\parallel}$, 2D conductance map. Sub-figure (b) shows line cuts at fields marked on (a) with corresponding colors on (b). As $B_{\parallel}$ is increased, the zero bias conductance increases and conductance peaks collapse. The map shows an induced critical field $B_{\parallel,c}^* \sim 750$ mT that is a factor 2.5 larger than observed in InAs/Al systems [\[38\]](#), similar to the factor 2.3 improvement of the induced gap width. This, together with the fact that $B_{\parallel,c}^* = 0$ when $\Delta^* = 0$, indicates a linear correlation between $B_{\parallel,c}^*$ and Δ^* . This is consistent with the explanation that it is the Zeeman splitting

¹ The Gradient function from Matlab was used, see <http://se.mathworks.com/help/matlab/ref/gradient.html> for information.

² Since the sub-gap conductance is low, even small fluctuations can affect the measured values significantly. Averaging over points close to $V_{\text{sd}} = 0$ was used to cancel out fluctuations.

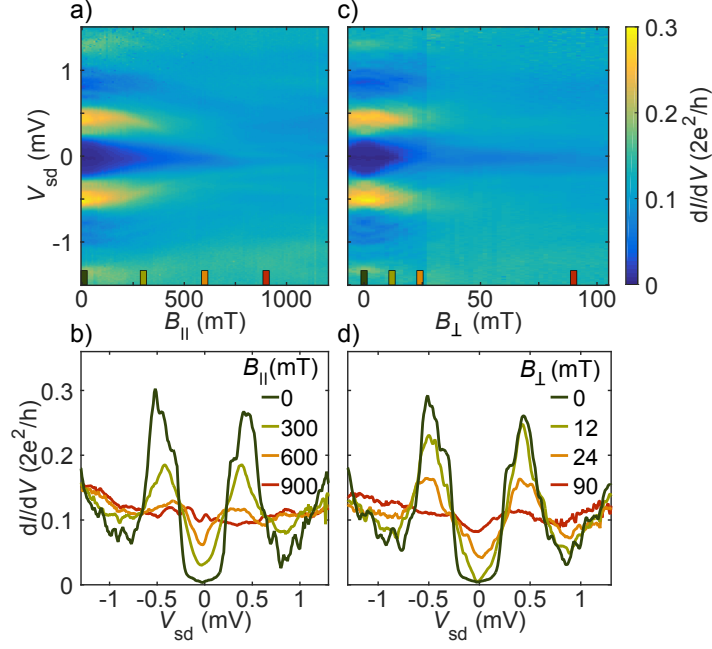


Figure 4.5.: **(a)** Differential conductance dI/dV as a function of source-drain voltage V_{sd} and parallel field $B_{||}$. Four colored lines show the $B_{||}$ values of the line cuts in **(b)**. **(c)** dI/dV as a function of V_{sd} and out of plane field $B_{\perp}$. Four colored lines show the $B_{\perp}$ values of the line cuts in **(d)**.

in InAs that quenches Δ^* [38]. Assuming $\Delta^* = E_{\text{Zeeman}} = g\mu_B B_{||,c}^*$, enables us to extract a g -factor, $g_{\text{Sm}} \sim 10$, which is comparable to that of bulk InAs.

Figure 4.5(c) shows a 2D conductance map with bias and out-of-plane field, $B_{\perp}$, while (d) shows line cuts at fields marked on (c) with corresponding colors on (d). For this field direction the superconductivity seems to be quenched at $B_{\perp,c}^* \sim 100$ mT. $B_{\perp,c}^*$ was expected to be smaller since $B_{||,c}^* \sim 1/d$ for thin superconductors of thickness d [19] and for this sample d was $\sim 70 - 90$ nm.

By tracing the conductance peaks in the out of plane sweeps another conclusion is found. The peaks don't collide but rather decrease in height as the zero bias resistance increases. This suggests that by increasing the out of plane field quasi-particles are added to the superconducting region. This could be due to fluxes penetrating the superconducting stack which is of type II. The generated vortices suppress the density of Cooper pairs but adds quasi particle states.

4.4 TEMPERATURE DEPENDENCE OF INDUCED GAP

A larger induced gap Δ^* comes with a higher induced critical temperature T_c^* , see Equation 2.1. Having superconductivity at higher temperatures ³ makes it less troublesome to implement in industry, since less sophisticated

³ Here we refer to conventional high temperature superconductors within the BCS regime, and not the exotic high temperature superconductors based on complex oxides [19].

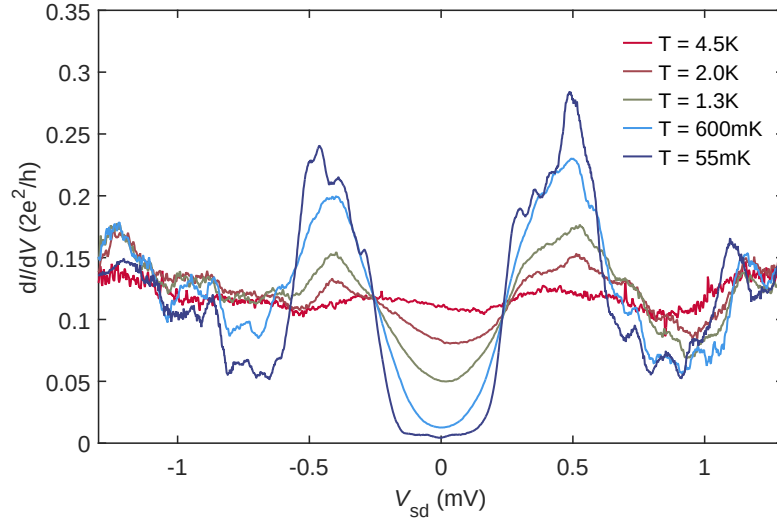


Figure 4.6.: Differential conductance dI/dV as a function of source-drain voltage V_{sd} , taken at different temperatures.

and less expensive cooling methods are needed to cool devices into the superconducting regime. A landmark would be to achieve induced superconductivity in a semiconductor above 4.2 K, the temperature of liquid helium at 1 bar.

One way to track the temperature dependence of the induced superconductivity is to monitor the LDOS at increased temperature, see Figure 4.6, where selected traces are shown. At first glance it looks like superconductivity is gone at 4.5 K, since the conductance is close to constant for varying V_{sd} . Tracing the conductance peaks as temperature is increased indicates another explanation. Their positions do not change much when comparing 2 K with base temperature; indicating that the gap has not been reduced significantly. The zero bias conductance increases without the conductance peaks collapsing is interpreted as the QPC no longer acts as a tunnel barrier at higher temperatures. It was also observed that the V_{gate} started leaking current into the system as temperature was increased. No accurate conclusions on the temperature dependence of the induced superconductivity can be made from these data.

Josephson junctions are two superconductive leads connected by a "weak link"; a non-superconducting material. If the weak link is conducting and smaller than its own effective coherence length, a supercurrent (current with no electrical resistance) will run between the two superconductors, carrying $2e$ charge¹ [42]. A supercurrent is only present if the interface resistances, between superconductors and weak link, are low enough for Andreev reflections to happen (see section 2.2). In this case, phase-correlated quasi particles Andreev reflect between the superconductors, thus transferring a supercurrent, shown in Figure 5.1(a). At certain biases these multiple Andreev reflections (MAR) create resonances. The number of Andreev reflections, n_{MAR} , a particle undergoes at a given resonance is given by the correlation [43, 44]:

$$eV = \frac{2\Delta}{n_{\text{MAR}}}, \quad (5.1)$$

where V is the DC voltage measured across the junction on the n 'th resonance. MAR resonances cause a peak/dip landscape to form when measuring differential resistance or differential conductance. Whether the resonances happen at peaks or dips, depends on the interface transparency between superconductor and weak link [45]. For high(low) transparency the MAR resonances happen at peaks(dips) in differential resistance and dips(peaks) in differential conductance. By tracing the voltages at which the different order of MAR resonance are located, one can extract the gap of the local superconductor with Equation 5.1.

In this chapter a S-Sm-S junction, lithographically similar to Figure 5.1(b), is studied. The SEM image was taken before mesa etch, ALD, and top gate deposition. As in chapter 4, the Sm is an InAs 2DEG, see Figure 2.7, and S is a layer of NbTi on epitaxial Al, see Figure 3.7. Unfortunately the top gate of the reported device began leaking at -1.5 V, which was not enough

¹ In the case of an insulating weak link a supercurrent also run, but only if the weak link is thin enough for Cooper pairs to tunnel through it.

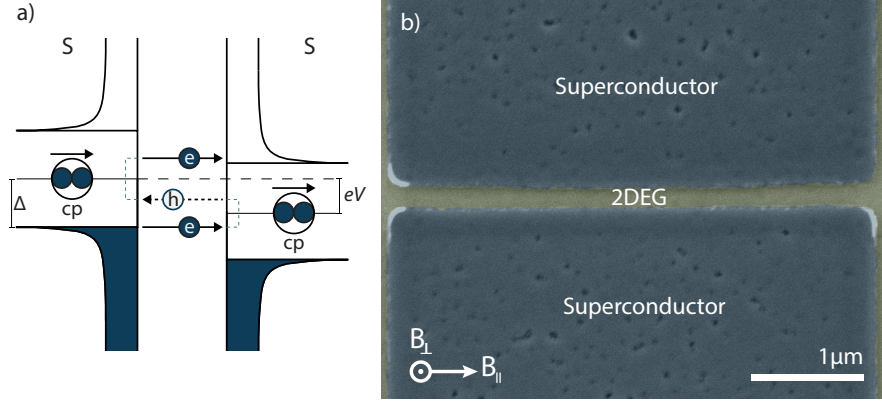


Figure 5.1.: **(a)** Schematic showing how multiple Andreev reflections (MAR), in this case two reflections, can transfer Cooper pairs (cp) from one superconductor (S), through a conducting "weak link" into another S, thus making a supercurrent flowing through the weak link. A bias results in a eV shift of the superconducting DOS, thus enabling different orders of MAR. **(b)** SEM of S-Sm-S device, graphically similar to the device which was used to obtain the results reported in this chapter. The image is taken before etch, ALD, and gate deposition. For the reported device, the distance between the superconducting leads was 180 nm. Magnetic field directions are defined in the bottom left corner.

to pinch off the 2DEG. It was enough though to make visible changes in measurements, which is reported in [Appendix G](#). In this chapter, the gate voltage was kept at zero to maximize the critical current in all measurements.

The distance between the superconducting banks is 180 nm, which means that the junction is in the quasi-ballistic regime, since the distance is on the order of the mean-free path of the InAs 2DEG $\ell = 164$ nm (see [Table 1](#)).

The S-Sm-S device was made from the same deposition as the S-QPC-Sm device reported in [chapter 4](#), so similar results should be obtained. A current bias setup, see [Figure 3.15\(a\)](#), was used to monitor the critical current, I_c , and MAR features as a function of bias, temperature, and magnetic field. The gap that gives rise to the MAR is the induced gap Δ^* , see [section 2.5](#).

5.1 TEMPERATURE DEPENDENCE OF S-SM-S JUNCTION

5.1.1 Temperature Dependence of I_c

One of many promising uses for superconductor-semiconductor hybrids is the realization of superconducting transistors: devices with a supercurrent that can be turned on or off without changing bias. One way to construct such a device is to build the known MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor), but with the semiconductor being a proximitized weak link between two superconductors, like on [Figure 5.1\(b\)](#). Having a superconducting transistor working at 4.2 K or higher is a landmark since it would be cheaper to apply in the industry, as elaborated in [chapter 1](#).

In this section we present data on the temperature dependence of I_c and MAR features. All data is obtained by measuring DC and AC voltage in current-bias sweeps at different temperatures. Figure 5.2(a) shows measured AC voltage divided by the AC current (5 nA), thus giving differential resistance. Starting with the base temperature sweep, a critical current of 7.5 μA is extracted. The superconducting leads have a width of $\sim 4.3 \mu\text{m}$ resulting in a critical current density of 1.74 $\mu\text{A}/\mu\text{m}$. At high bias, a normal resistance R_N of 53 Ω is extracted giving $I_c R_N = 0.40 \text{ meV}$. Both the critical current density and the $I_c R_N$ product are larger than earlier observed on S-Sm-S junctions based on epitaxial Aluminum [45].

The 2nd to 5th MAR resonances are highlighted for the base temperature sweep. These show up as peaks in resistance. The plotted sweeps at other temperatures are selected to show the evolution of the MAR features as a function of temperature. Figure 5.2(b) shows that the temperature during all bias sweeps with $T \geq 2 \text{ K}$, was kept rather stable. The MAR features evolve as a function of temperature, because the induced superconducting gap decreases which decreases the energy of the MAR resonances as well, see Equation 2.1 and Equation 5.1. At intermediate temperatures higher order MAR become visible, see Figure 5.2(a). As long as a supercurrent is present, the measured voltage is zero. So $eV(I_c)$ (e being the electron charge) defines the lowest energy at which MAR features are resolved. Figure 5.2(c) shows DC voltage as a function of for all temperature sweeps, including those of source-drain current Figure 5.2(a). From the DC measurement it is clear that $eV(I_c)$ falls as a function of temperature, enabling lower energy features to be resolved in Figure 5.2(a).

Another noticeable feature of Figure 5.2(c) is found by extracting lines from the normal region of the low temperature sweeps. These lines cross the V_{DC} at a finite I_{sd} value, which is unusual, compared to Ohmic I-V curves. This non-zero value, called excess current [20], is present because there are more Andreev reflections than normal reflections. The current gain from Andreev reflections is larger than the current loss due to normal reflections. This observation also suggests that the S-Sm interface is highly transparent.

The critical current as a function of temperature is extracted and displayed on Figure 5.2(d) together with the evolution of the zero-bias resistance as a function of temperature. The latter was obtained by sitting at zero-bias and measuring AC voltage and temperature while slowly increasing temperature. As expected, the zero-bias resistance starts increasing at the temperature for which $I_c = 0$. For our device this temperature is 3.7 K, which is close to the 4.2 K of liquid ^4He .

For temperatures above $T = 3.7 \text{ K}$, the zero bias resistance rises slowly, instead of having a sharp superconducting transition. The rising curve has two shoulders before reaching a sharp transition at $\sim 7.7 \text{ K}$, which we interpret as the critical temperature of the superconducting leads. This would also explain the big resistance difference between the two top curves

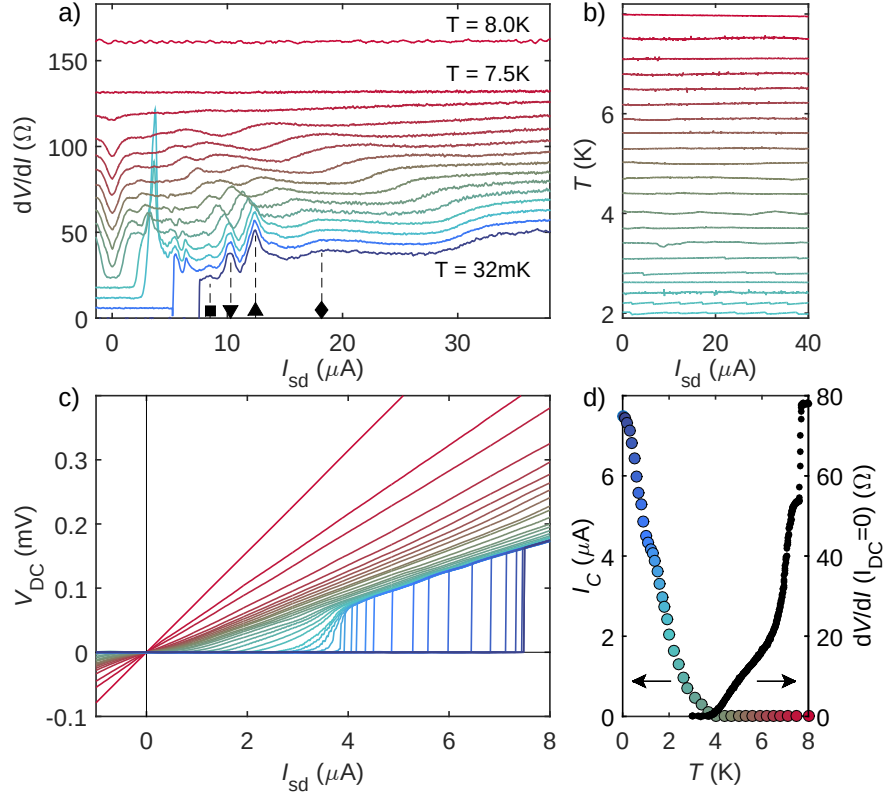


Figure 5.2.: **(a)** Differential resistance, dV/dI , as a function of source-drain current, I_{sd} , for selected temperatures ranging from 32 mK to 8.0 K. Traces are successively offset by 6 Ω . Peaks in resistance corresponding to different order of MAR resonances are highlighted by symbols: $\blacklozenge$: 2nd, $\blacktriangle$: 3rd, $\blacktriangledown$: 4th, and $\blacksquare$: 5th. **(b)** Temperature of mixing chamber during current-bias measurements. **(c)** Measured DC voltage as a function of source-drain current for all temperature sweeps. **(d)** Critical current (left axis) and zero bias resistance (right axis) as a function of temperature. I_C is extracted from (a) and the zero bias resistance was measured while slowly increasing the temperature, here binned in steps of 0.01 K.

in Figure 5.2(a). One explanation for the slow increase of the zero bias resistance could be thermally activated phase slips [46].

5.1.2 Temperature Dependence of Δ^*

In section 4.4 a QPC was used to study the induced gap as a function of temperature. Unfortunately thermal fluctuations hindered tunnel spectroscopy at higher temperatures. In this section an analysis of MAR as a function of temperature is used to obtain what the QPC couldn't. The analysis is done for the base temperature sweep on Figure 5.3(a), where the MAR features are plotted as differential conductance vs. measured DC voltage. This enables direct read of the MAR feature energies, eV. The MAR resonances is at dips in conductance, which is expected for high transparency junctions. That the

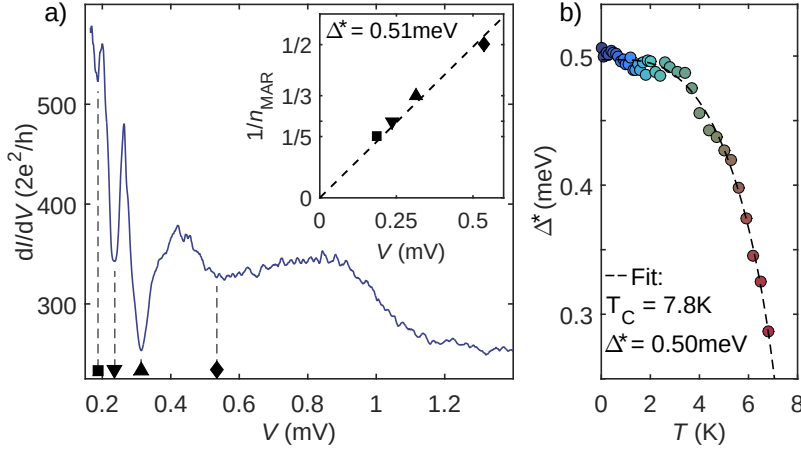


Figure 5.3.: **(a)** Differential conductance vs voltage at base temperature showing dips/peaks arising from MAR. The 2nd to 5th order MAR are highlighted as in Figure 5.2(a). Inset shows how Δ^* is extracted from $1/n_{\text{MAR}} = eV/2\Delta^*$. **(b)** Temperature dependence of the induced gap, Δ^* , extracted as shown in the inset of (a), is fitted by Equation 2.1 with T_c and Δ^* as parameters. Colors can be used to compare with data on Figure 5.2.

dips really are the resonances are verified in the inset figure where the extracted energies are matched well by a fit, which is a rewrite of Equation 5.1: $1/n_{\text{MAR}} = eV/2\Delta^*$. The extracted induced gap is $\Delta^* = 0.51 \text{ meV}$, similar to the base temperature gap observed in the QPC, $\Delta_{\text{QPC}}^* = 0.43 \text{ meV}$.

The induced gap was extracted from all temperature sweeps (besides the hottest where MAR features were hard to identify) and the results are plotted on Figure 5.3(b). The data is fitted by Equation 2.1 with two fitting parameters: The induced gap at zero temperature, $\Delta^*(0)$, and the critical temperature, T_c . The fit follows the data well and gives $\Delta^*(0) = 0.50 \text{ meV}$ and $T_c = 7.8 \text{ K}$. The first is close to the two other extracted values for the induced gap (extracted at base temperature) 0.51 meV and 0.43 meV . The latter is close to the critical temperature of the superconducting leads observed in Figure 5.2(d), which was 7.7 K .

5.2 FIELD DEPENDENCE OF I_c

In this section, we study how the critical current reacts when magnetic fields are applied on the S-Sm-S junction. Two orientations are reported, in-plane field perpendicular to the current direction $B_{\parallel}$ and $B_{\perp}$, which is perpendicular to the 2DEG, see Figure 5.1(b). We start studying the latter.

5.2.1 Out of Plane Field Dependence of I_c

Applying an out of plane field on a SNS (or S-Sm-S) junction is known to produce Fraunhofer interference patterns, [47]. The perpendicular field

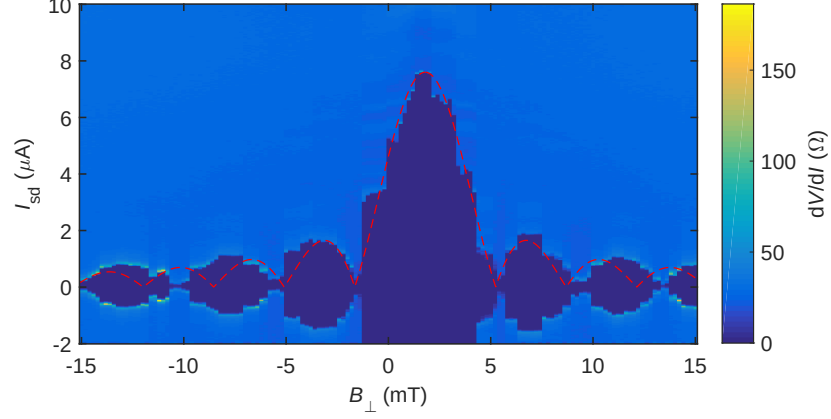


Figure 5.4.: Measurement of differential resistance dV/dI as a function of current bias I_{sd} at small perpendicular magnetic fields, $B_{\perp}$. The red dashed curve is calculated from Equation 5.2, by inserting $I_c(0) = 7.5 \mu\text{A}$, $L = 150 \text{ nm}$ and $W = 4.3 \mu\text{m}$.

penetrating the normal conducting material winds the superconducting phase along the junction, making the current density oscillate [48], creating an node anti-node trend for the supercurrent described by

$$I_c(B_{\perp}) = I_c(0) \left| \frac{\sin(\pi B_{\perp} LW / \Phi_0)}{\pi B_{\perp} LW / \Phi_0} \right|, \quad (5.2)$$

with L being the separation between superconductors, W the width of the superconductors, and $\Phi_0 = h/2e$ the flux quantum. The theory (red dashed line) is compared with the measurements on Figure 5.4 where differential resistance is measured as a function of current bias and perpendicular field. Besides the measurement being noisy/jumpy, there is a slight difference between data and theory when comparing the node spacing. The node spacing of the data is larger, which suggests that the effective area is smaller than $L \cdot W$ of the junction. No SEM of the device was taken in between mesa etch and top gate deposition, but it might be that the mesa etch was miss-aligned and the effective width is smaller than $4.3 \mu\text{m}$.

Fraunhofer measurements were also made on earlier devices. These were much cleaner, but had too low node-spacing, probably due to flux focusing. A test device with reduced flux-adding area showed significant improvements. These results are presented in Appendix H.

5.2.2 In-Plane Field Dependence of I_c

Before starting in-plane magnetic field sweeps, it is important to align the vector magnet according to the axes of the device. Otherwise an applied in-plane field could have an out of plane component, and even small $B_{\perp}$ components make huge oscillations in the critical current, see Figure 5.4. The alignment procedure is elaborated in Appendix E.

After alignment, differential resistance can be measured as a function of current bias and in-plane magnetic field, see Figure 5.5 (a). Sub-figure (b) shows line cuts of the 2D map, at marked $B_{||}$ values. The field suppresses the supercurrent, which dies out around 500 mT. At lower fields the scan is noisy, probably due to flux jumps. The asymmetry in source drain current is due to heating effects arising from the scans being taken from negative to positive current.

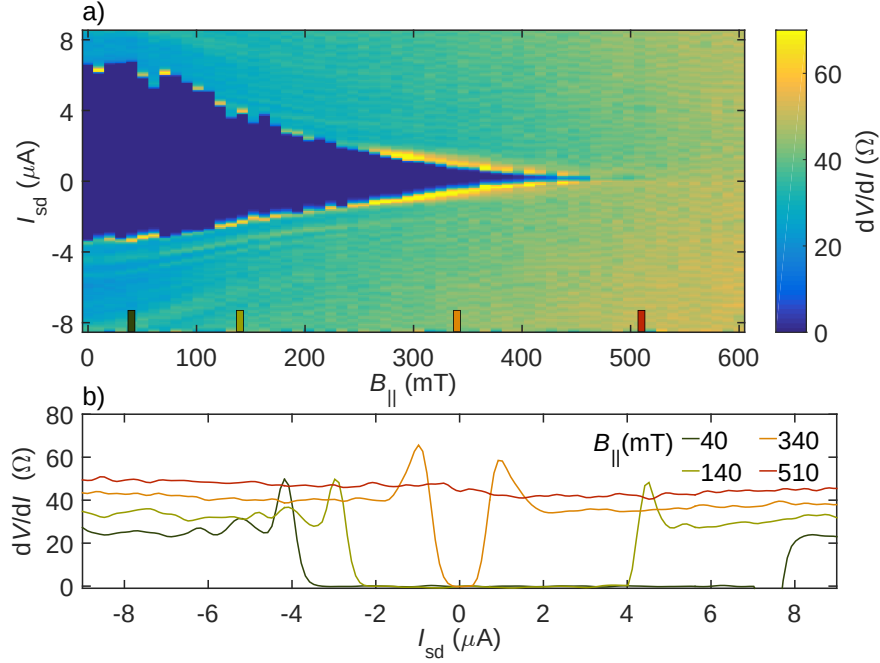


Figure 5.5.: **(a)** Differential resistance dV/dI as a function of current bias I_{sd} and in-plane field, perpendicular to the current direction, $B_{||}$. **(b)** dV/dI vs I_{sd} line cuts extracted from (a) at different $B_{||}$.

Especially in the negative current regime, peaks in resistance are visible due to MAR resonances. Only few resonances are visible and only for a limited range in $B_{||}$. If a scan with higher resolution and higher currents were taken, more MAR features could have been traced. That would have enabled the extraction of the superconducting gap as a function of in-plane field, which could have been compared with the data from Figure 4.5(a,b).

CONCLUSION & OUTLOOK

6.1 RECAP OF RESULTS

In conclusion, this work demonstrates a method for fabricating a superconductor/InAs 2DEG heterostructure with very high interface transparency and controllable induced gap. The base substrate is a MBE grown InAs 2DEG with epitaxially grown Al. The ex-situ deposition of a large gapped superconductor, to proximitize InAs through Al makes this method compatible with conventional growth and processing laboratories.

Prior to the superconductor deposition, argon ion milling is used to remove aluminum oxide to ensure low interface resistance between the superconductors. The milling machine fluctuated a lot, but careful calibrations enabled successive successful depositions.

A NbTi-based superconductor deposition was used to fabricate S-Sm-S and S-QPC-Sm junctions. Both devices demonstrated a high transparency super/semi interface and an enhanced induced superconductive gap Δ^* .

The QPC measure $\Delta^* = 0.43$ meV and was also used to measure an induced critical in-plane field $B_{c||}^* \approx 750$ mT, interpreted as due to Zeeman splitting in the 2DEG. Measuring the critical out of plane field and critical temperature was also attempted, but the measurement procedure lead to introduction of sub gap quasi particles instead of gap-closing, disabling an extraction of the critical values.

The Josephson junction with 180 nm spacing between the superconducting leads showed a critical current density of $1.74 \mu\text{A}/\mu\text{m}$, a $I_c R_N$ product of 0.40 meV and an extracted induced gap $\Delta^* = 0.50$ meV. The zero resistance state lasts up to 3.7 K, while the induced gap lasted until the superconductor stack entered the normal phase at ~ 7.7 K.

6.2 SUGGESTIONS FOR FURTHER WORK

The reported results pave the way for future super/semi conductor electronics above liquid ^4He temperature and topological states of matter. One interesting application is to make superconducting devices with different

superconductors, enabling the presence of trivial and topological regimes at the same time.

A lot of work could be done to improve the superconducting proximity effect into the InAs 2DEG and to optimize the properties of the 2DEG itself. Some of these optimizations are discussed below.

6.2.1 *Optimization of the InAs 2DEG growth*

Compared to buried 2DEGs, our mobility of $10.000 \text{ cm}^2/\text{Vs}$ is *very* low. The mobility could be increased by growing heterostructures that isolate the electron wave function from scattering sources. A huge source of scattering is the exposed InGaAs surface after stripping of Al. Starting with the Bo509 heterostructure, [Figure 2.7](#), the electron wave function could be moved away from the surface by decreasing transmission across the top InGaAs barrier. That is achieved either by increasing the thickness of the InGaAs or by using another material with a higher energy barrier, like AlGaSb. Complete isolation of the electrons from the surface would on the other hand lead to poor coupling to the epitaxial aluminum, impairing the superconducting proximity effect. Another possible pitfall is that a higher mobility comes with a lower Fermi-velocity which might significantly increase Z_{eff} through Fermi velocity miss-match. The optimal configuration could be estimated by a self-consistent Poisson solver [28] or it could be found by dedicated cranking by the growth chamber and in the cleanroom for a couple of months.

The location of the electron wave function can also be controlled by top- or bottom-gates. This nob-control of electron density in the growth-direction has many promising applications and might be crucial for realizing some physical systems.

6.2.2 *Removing Ti layer under NbTi*

The NbTi-based superconducting stacks used in this work had 2 nm Ti, which was intended to serve as a sticking layer under the NbTi. Whether the Ti is necessary to obtain low contact resistance is not tested yet since earlier depositions without Ti had imprecise milling. If Ti does not affect the interface resistance it should not be used since its low superconducting gap can cause a decrease of the induced gap in Al and InAs through the inverse proximity effect.

6.2.3 *Using NbTiN-based supercondcuting stacks*

An obvious way to increase the induced superconducting properties in the 2DEG is to couple it to a superconductor with a wider energy gap. Researchers at Delft have had great success using a NbTiN-based stack with a 5 nm narrow NbTi layer to proximitize InSb nanowires [10]. The NbTi layer

is necessary since a flow of nitrogen before deposition would form resistive nitrides on the surface. Once the optimal pressure and flow rates for NbTiN deposition is found, a similar stack should have a critical temperature twice the size of our NbTi-based stack, which was 7.7 K.

6.2.4 *In-situ deposition of NbTi(N)*

Another approach to the deposition of NbTi or NbTiN would be to do it in a chamber connected in-situ to the MBE system. A direct coupling (without Al) could be obtained, but this would introduce problems with selective etching when exposing III/V for gating. Pure niobium can be etched by reactive ion etching (RIE) [49], but literature on etching NbTi(N) was not found. In case no selective etch can be found, the benefits from a direct coupling cannot be exploited. Instead an aluminum spacer (like the 25nm used in this work) could be placed in between III/V and NbTi(N). Then the etch should just stop in the aluminum, and the chemical Transene D etch could ensure limited damage of the III/V. The minimal spacer thickness thus ensures consistent success should be chosen.

Another benefit from removing the NbTi(N) rather than depositing, is that sidewalls can be avoided. Depending on the etch though, sub-100 nm structures might be hard to define.



ARTICLE

On the following pages, the most recent draft of our article is presented.

Proximity Effect Transfer from NbTi into a Semiconductor Heterostructure via Epitaxial Aluminum

A. C. C. Drachmann,¹ H. J. Suominen,¹ M. Kjaergaard,¹
B. Shojaei,² C. J. Palmstrøm,^{2,3} C. M. Marcus,¹ and F. Nichele¹

¹*Center for Quantum Devices and Station Q Copenhagen, Niels Bohr Institute
University of Copenhagen, Universitetsparken 5, 2100 Copenhagen, Denmark*

²*Materials Department, University of California, Santa Barbara, CA 93106, USA*

³*Department of Electrical and Computer Engineering,
University of California, Santa Barbara, CA 93106, USA*

(Dated: November 23, 2016)

We demonstrate the transfer of the superconducting properties of NbTi—a large-gap high-critical-field superconductor—into an InAs heterostructure via a thin intermediate layer of epitaxial Al. Two device geometries, a Josephson junction and a gate-defined quantum point contact, are used to characterize interface transparency and the two-step proximity effect. In the Josephson junction, multiple Andreev reflection reveal near-unity transparency, with an induced gap $\Delta^* = 0.50$ meV and a critical temperature of 7.8 K. Tunneling spectroscopy yields a hard induced gap in the InAs adjacent to the superconductor of $\Delta^* = 0.43$ meV with substructure characteristic of both Al and NbTi.

Intimate coupling between semiconductors (Sm) and superconductors (S) gives rise to novel applications of superconducting electronics [1], as well as superconducting qubits [2] and new topological states of matter [3, 4]. A critical building block for S/Sm hybrids system is a transparent interface, ensuring high probability of Andreev reflection [5, 6]. However, obtaining a transparent S/Sm interface has been a technological challenge for decades [7–9]. Recent work has largely resolved the interface problem by realizing epitaxial growth of Al on InAs via molecular beam epitaxy (MBE), both for nanowires [10, 11] and, more recently, for two-dimensional electron gases (2DEGs) [12], which are better suited for realizing complex, branched devices [3]. Focusing on InAs 2DEGs with epitaxial Al, high interface transparency and a hard induced superconductive gap $\Delta^* = 0.18$ meV have been measured both by tunneling spectroscopy via a S-quantum point contact (QPC)-Sm junction [13] and by analysis of multiple Andreev reflection (MAR) in a S-Sm-S junction [14].

Despite its modest superconducting gap, critical temperature and critical magnetic field, Al has been the material of choice for Sm-S epitaxy to date because it is present in conventional III-V MBE systems and is compatible with standard fabrication recipes. *In situ* deposition (without breaking vacuum) or direct epitaxial growth of larger gap superconductors has proven challenging and requires dedicated growth systems. As an alternative, we demonstrate in this work the transfer of large-gap properties of NbTi via the proximity effect through a thin epitaxial Al layer into an InAs 2DEG.

Starting from an InAs heterostructure with epitaxial Al, we pattern *ex situ* a NbTi-based superconductive layer using standard lithographic techniques. The NbTi layer enhances the Al gap by the proximity effect [15, 16], which in turn results in an enhanced induced gap in the

InAs 2DEG. As the processing only involves the top-most Al surface, the high transparency of the epitaxial InAs/Al interface is not affected. As discussed below, the induced gap in the InAs 2DEG is found to be more than twice as large as both the induced gap using Al alone [13, 14] and the gap of the Al itself. The method can be extended to other choices of top-layer superconductor [15].

We investigate two device geometries, an S-Sm-S Josephson junction and a S-QPC-Sm junction. The S-Sm-S device shows pronounced MAR features, indicating high transparency, and we extract an induced gap, $\Delta^* = 0.50$ meV and a critical temperature, $T_c = 7.7$ K, with the zero resistance state across the junction persisting up to 3.7 K. Tunnel spectroscopy in the S-QPC-Sm device yields an induced gap of 0.43 meV and a hardness of the induced gap (measured by a sub-gap conductance suppression in the tunnel regime) comparable to the theoretical limit for S/Sm junctions [17]. Tunnel spectroscopy in a magnetic field reveals a gap closing at a critical in-plane field value of $B_{||,c} \sim 750$ mT, a value 2.5 times larger than in similar systems without NbTi [13].

The InAs heterostructure, grown on an undoped GaSb wafer along the [001] crystallographic direction, is shown in Fig. 1(a). The active region is similar to previous studies [12], but with a nominal 25 nm epitaxial Al layer, instead of the 10 nm Al layer used previously. Thicker Al allowed this layer to be thinned during fabrication without risking etching down to the interface, as discussed below. Transport measurements in a Hall bar with the Al removed were used to extract a mobility of $10,000$ cm²/Vs at a density of 1×10^{12} cm⁻².

Critical fabrication steps are outlined in Fig. 1b, with full details given in the Supplemental Material [18]. First, areas for NbTi deposition are patterned using electron-beam lithography. Inside the deposition chamber, the

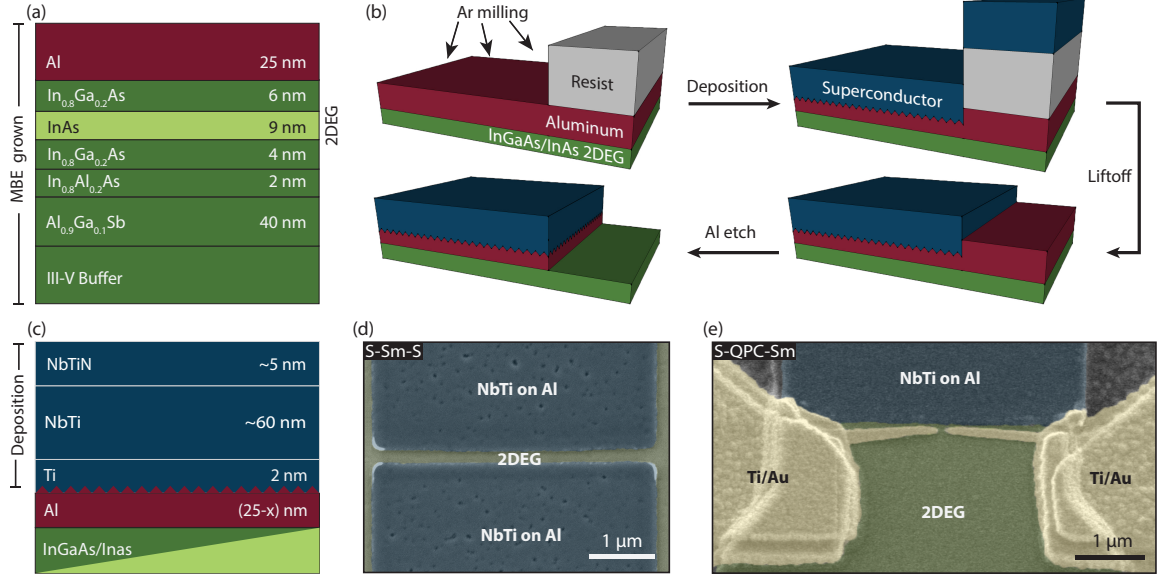


FIG. 1. (a) MBE-grown InAs/Al hybrid heterostructure. (b) Illustration of superconductor deposition and patterning. The native Al oxide is removed in the lithographically defined areas by Ar ion milling, leaving behind a ragged top surface of Al. The NbTi superconductor stack is then deposited without breaking vacuum. After liftoff, the NbTi stack serves as an aligned etch mask for an Al wet etch. (c) The NbTi stack includes a Ti layer to promote adhesion and a NbTiN capping to prevent oxidation. (d) False-color electron micrograph of an S-Sm-S device after the Al etch similar to the sample measured. (e) False-color electron micrograph of the finished S-QPC-Sm device.

native oxide on Al is removed using Kaufman Ar milling, followed immediately by evaporating Ti and sputtering NbTi/NbTiN without breaking vacuum, as shown in Fig. 1(c). The Ti bottom layer promotes adhesion and the NbTiN top layer prevents subsequent oxidation. Following liftoff, the patterned NbTi forms a self-aligned mask for a selective Al etch. Fabrication steps not shown in Fig. 1(b) include mesa etching, deposition of 50 nm of HfO_2 by atomic layer deposition, and evaporation of Ti/Au top gates.

Figure 1(d) shows an S-Sm-S device similar to the one measured. The measured device had a separation between the superconducting banks of 150 nm and a width of $4.3 \mu\text{m}$ [19]. Figure 1(e) shows the measured S-QPC-Sm device. All measurements were carried out using standard AC lock-in techniques in a dilution refrigerator with base temperature of 35 mK. The S-Sm-S device was measured with a 5 nA current bias; the S-QPC-Sm device was measured with a 10 μeV voltage bias.

The induced gap under the superconducting leads [6, 20] and the interface transparency [21] can be extracted from MAR measurements in the S-Sm-S junction. As discussed in Ref. [14], a characteristic feature of InAs/epitaxial Al Josephson junction is that sub-gap MAR features appear as peaks in resistance rather than in conductance, a consequence of the high S/Sm interface transparency. Differential resistance dV/dI as a function of DC bias I_{DC} at various temperatures is shown in Fig. 2(a). At base temperature, the critical current, $I_C =$

$7.5 \mu\text{A}$, with normal-state resistance $R_N = 53 \Omega$ reached at $I_{\text{DC}} = 45 \mu\text{A}$. The $I_C R_N$ product was 0.40 meV and critical current density was $1.74 \mu\text{A}/\mu\text{m}$, both considerably larger than that measured S-Sm-S junctions with epitaxial Al alone [14].

As seen in Fig. 2(b) the junction remains in the zero-resistance state up to 3.7 K, above which resistance increases up to a plateau at 53Ω , which we interpret as the normal-state resistance of the junction. The sharp transition at 7.7 K is associated with the critical temperature of the NbTi contacts. The differential resistance displays pronounced MAR features, appearing as sharp peaks in resistance [or dips in conductance, see Fig. 2(c)].

From the MAR relation $eV = 2\Delta^*/n_{\text{MAR}}$, a linear fit of the inverse MAR index $1/n_{\text{MAR}}$ as a function of the voltage bias V , [Fig. 2(c) inset] yields a base temperature induced gap $\Delta^* = 0.51 \text{ meV}$. Repeating the procedure over a range of temperatures yields $\Delta^*(T)$, shown in Fig. 2(d) along with a fit to the BCS form [22],

$$\Delta^*(T) = \Delta^*(0) \cdot \tanh \left(1.74 \cdot \sqrt{\frac{T_c}{T}} - 1 \right), \quad (1)$$

giving $\Delta^*(0) = 0.50 \text{ meV}$ and $T_c = 7.8 \text{ K}$ as fit parameters. Experimental data and the BCS fit are in good agreement.

A requirement for the use of S/Sm devices for certain applications, including topological quantum computing, is the absence of sub-gap states, reflected in a small sub-gap conductance. Using the approach of Ref. [10, 13],

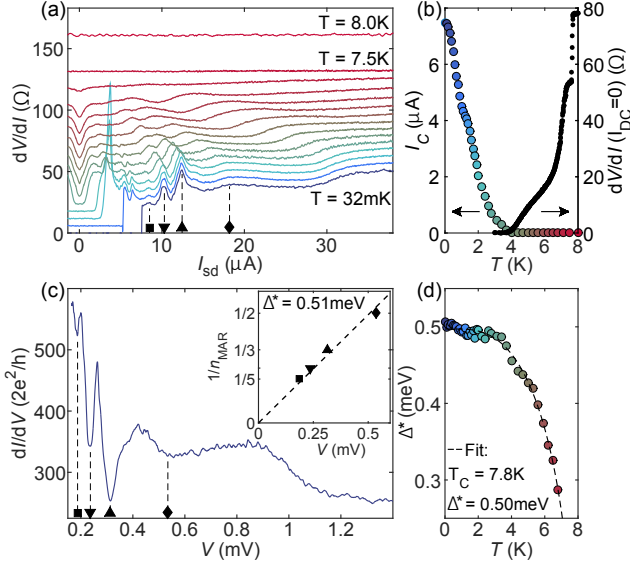


FIG. 2. Characterization of a S-Sm-S device similar to that shown in Fig. 1(d). (a) Differential resistance as a function of temperature, showing harmonic structures due to MAR resonances. Traces are successively offset by 6 Ω . Peaks in resistance corresponding to different order of MAR resonances are highlighted by symbols: ◆: 2nd, ▲: 3rd, ▼: 4th and ■: 5th. (b) Critical current (left axis) and zero bias resistance (right axis) as a function of temperature. I_c is extracted from (a) and the zero bias resistance was measured while increasing temperature, here binned in steps of 0.01 K. (c) Differential conductance vs voltage at base temperature showing dips/peaks arising from MAR. 2nd to 5th order MAR are highlighted as in (a). Inset shows how the induced gap, Δ^* , is extracted from linear fit to the MAR formula $eV = 2\Delta^*/n_{\text{MAR}}$. (d) Temperature dependence Δ^* extracted as shown in the inset of (c), is fitted by Eq. 1 with T_c and Δ^* as parameters. Colors are used to enable comparison of data between sub-figures.

we measured electron tunneling near the S/Sm interface using a gate-defined QPC fabricated on top of an ALD oxide. A false colored SEM of the device is shown on Fig. 1(e).

Figure 3(a) shows the differential conductance dI/dV as a function of source-drain bias V_{SD} where the gates are energized to set the QPC in the tunneling regime. In this case, the differential conductance maps the local density of states, allowing the induced gap Δ^* at the position of the QPC to be directly measured. Defining $2\Delta^*$ as the peak to peak separation gives $\Delta^* = 0.43$ meV, as shown in Fig. 3(a), similar to the value measured via MAR. In addition to the large energy gap—a factor ~ 2.3 larger than the Al-only case [13])—the hardness of the gap at zero energy is not affected by the additional fabrication. To demonstrate this, we measure similar curves as Fig. 3(a) for different values of out-of-gap conductance, which result in varying in-gap conductance, and produce the parametric plot of Fig. 3b (markers). These data are

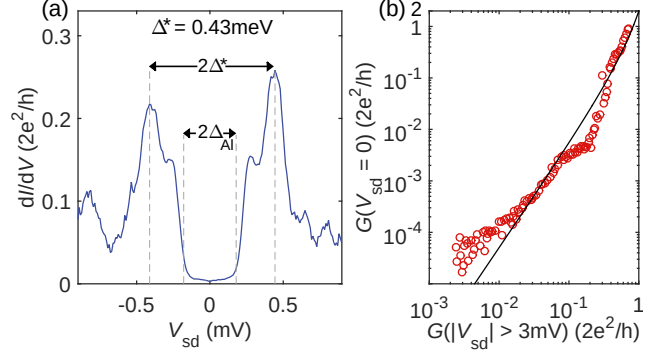


FIG. 3. Characterization of the S-QPC-Sm device shown in Fig. 1(e). (a) Differential conductance dI/dV as a function of the voltage drop across the QPC V_{sd} . Data is measured with the S-QPC-Sm device in the tunneling regime. An induced gap, Δ^* , is extracted as half the peak-to-peak distance. For comparison the gap of bulk Al $\Delta_{\text{Al}} = 0.18$ meV is also displayed. (b) Zero-bias conductance, $G(V_{\text{sd}} = 0)$ versus an averaged of conductance at high finite bias $G(|V_{\text{sd}}| > 3.0$ mV). Values are extracted from a bias-gate-2D map of conductance, shown in the appendix and are slightly binned. Black curve is a theoretical prediction for perfectly transparent junctions, eq. 2, with no free parameters.

compared to theory of a single mode S/Sm interface [17],

$$G_{\text{ns}} = 2G_0 \frac{G_{\text{nn}}^2}{(2G_0 - G_{\text{nn}})^2}, \quad (2)$$

with no fit parameters.

Here G_{ns} is the conductance in the superconducting regime, G_{nn} is the normal state conductance (measured at high source drain bias) and $G_0 = 2e^2/h$ is the conductance quantum. The agreement is remarkable up to four order of magnitude, demonstrating our devices operate in the theoretical limit of low in-gap conductance. The complete data set is presented in the Supplemental Material [18].

In order to drive the system in the topological regime, a necessary condition is that the Zeeman splitting in InAs, $g_{\text{Sm}}\mu_B B$, exceeds Δ^* while the parent superconductor remains gapped. Previous measurements on InAs/Al heterostructures showed a gap closing at in-plane fields $B_{\parallel} \sim 300$ mT, compatible with $g_{\text{Sm}} \sim 10$, a reasonable value for InAs [13]. Similar measurements presented in Fig. 4(a,b) indicate a gap closing for in-plane magnetic fields of $B_{\parallel,c} \sim 750$ mT, consistent with an induced gap 2.3 times larger than experiments with epitaxial Al. We note that gap closing is not linked to the quenching of superconductivity in the parent superconductor as NbTi can sustain much larger fields than those used here. A different situation is observed when the field is applied out-of-plane, as shown in Fig. 4(c,d). In this case the most prominent effect is not a gap closing (the $\pm\Delta^*$ peaks do not approach zero), but rather a gap softening above 100 mT that makes the gap indistinguishable

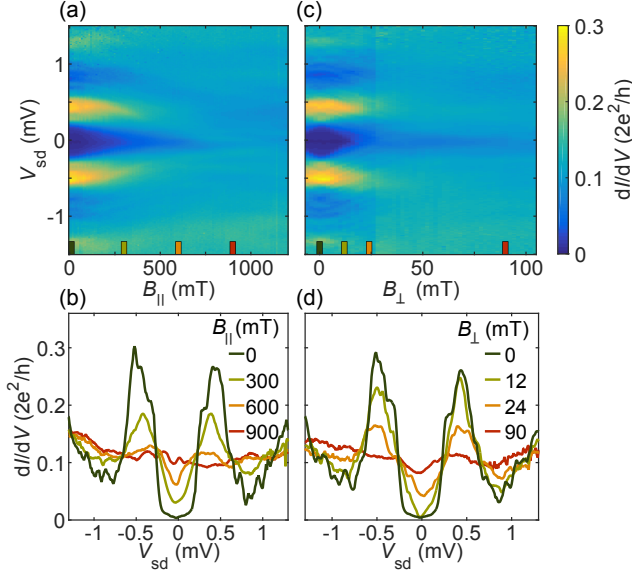


FIG. 4. Magnetic field dependence of the S-QPC-Sm device of Fig. 1(e). (a) Differential conductance dI/dV as a function of source-drain voltage V_{sd} and parallel field $B_{||}$, perpendicular to the current. Four colored lines show the $B_{||}$ values of the line cuts in (b). (c) dI/dV as a function of V_{sd} and out-of-plane field $B_{\perp}$. Four colored lines show the $B_{\perp}$ values of the line cuts in (d)

from the background. We interpret the softening as due to dephasing of Andreev pairs in the presence of vortices penetrating the S/Sm stack in a large out-of-plane fields [22].

The possibility to locally control the induced gap (and critical field) in the Sm by combining regions with only epitaxial Al or with NbTi/Al stacks allows the realization of complex devices required for future studies of topological states of matter [23]. For example, NbTi could be used to realize superconductive leads that persist in the trivial regime while one dimensional devices, proximatized by epitaxial Al only, undergo the topological transition.

In summary, we have demonstrated a method for obtaining a S/Sm heterostructure with high interface transparency and a large, controllable induced gap. The processing is based on MBE grown InAs/Al heterostructures and *ex-situ* deposition of a large-gap superconductor. The technique does not compromise the epitaxial interface and so should be compatible with a variety of materials and processing technologies. Our results suggest a path toward semiconductor-superconductor electronics, both conventional and topological, operating in the temperature range of liquid helium or pulse tube coolers.

We thank S. Upadhyay for useful discussions on fabrication. Research supported by Microsoft Station Q, the Danish National Research Foundation, the Villum Foun-

dation, and the European Commission through a Marie Curie Fellowship.

-
- [1] H. Weinstock and R. W. Raslton, *The New Superconducting Electronics* (Kluwer Academic Publishers, 1993) p. 457.
 - [2] J. Clarke and F. K. Wilhelm, *Phys. World* **17**, 29 (2004).
 - [3] J. Alicea, Y. Oreg, G. Refael, F. von Oppen, and M. P. a. Fisher, *Nat. Phys.* **7**, 412 (2011).
 - [4] M. Leijnse and K. Flensberg, *Phys. Rev. Lett.* **107**, 1 (2011).
 - [5] G. E. Blonder, M. Tinkham, and T. M. Klapwijk, *Phys. Rev. B* **25**, 4515 (1982).
 - [6] M. Octavio, M. Tinkham, G. E. Blonder, and T. M. Klapwijk, *Phys. Rev. B* **27**, 6739 (1983).
 - [7] M. Amado, A. Fornieri, F. Carillo, G. Biasiol, L. Sorba, V. Pellegrini, and F. Giazotto, *Phys. Rev. B* **87**, 1 (2013).
 - [8] Z. Wan, A. Kazakov, M. J. Manfra, L. N. Pfeiffer, K. W. West, and L. P. Rokhinson, *Nat. Commun.* **6**, 7426 (2015).
 - [9] H. Takayanagi and T. Akazaki, *Phys. Rev. B* **52**, 8633 (1995).
 - [10] W. Chang, S. M. Albrecht, T. S. Jespersen, F. Kuemmeth, P. Krogstrup, J. Nygård, and C. M. Marcus, *Nat. Nanotechnol.* **10**, 232 (2015).
 - [11] P. Krogstrup, N. L. B. Ziino, W. Chang, S. M. Albrecht, M. H. Madsen, E. Johnson, J. Nygård, C. M. Marcus, and T. S. Jespersen, *Nat. Mater.* **14**, 400 (2015).
 - [12] J. Shabani, M. Kjaergaard, H. J. Suominen, Y. Kim, F. Nichele, K. Pakrouski, T. Stankevic, R. M. Lutchyn, P. Krogstrup, R. Feidenhans'l, S. Kraemer, C. Nayak, M. Troyer, C. M. Marcus, and C. J. Palmstrøm, *Phys. Rev. B* **93** (2016).
 - [13] M. Kjaergaard, F. Nichele, H. J. Suominen, M. P. Nowak, M. Wimmer, A. R. Akhmerov, J. A. Folk, K. Flensberg, J. Shabani, C. J. Palmstrøm, and C. M. Marcus, *Nat. Commun.* **7**, 12841 (2016).
 - [14] M. Kjaergaard, H. J. Suominen, M. P. Nowak, A. R. Akhmerov, J. Shabani, C. J. Palmstrøm, F. Nichele, and C. M. Marcus, *ArXiv e-prints* (2016), arXiv:1607.04164 [cond-mat.mes-hall].
 - [15] G. Brammertz, a. Golubov, a. Peacock, P. Verhoeve, D. Goldie, and R. Venn, *Physica C* **350**, 227 (2001).
 - [16] V. Cherkez, J. C. Cuevas, C. Brun, T. Cren, G. Ménard, F. Debontridder, V. S. Stolyarov, and D. Roditchev, *Phys. Rev. X* **4**, 1 (2014).
 - [17] C. W. J. Beenakker, *Phys. Rev. B* **46**, 841 (1992).
 - [18] See Supplemental Material at [URL] for material and methods and presentation of additional measurements.
 - [19] Image is taken before etching, ALD and gate deposition.
 - [20] K. Flensberg, J. B. Hansen, and M. Octavio, *Phys. Rev. B* **38**, 8707 (1988).
 - [21] A. Chrestin, T. Matsuyama, and U. Merkt, *Phys. Rev. B* **55**, 8457 (1997).
 - [22] M. Tinkham, *Introduction to Superconductivity*, 2nd ed. (McGraw-Hill Book Co., New York, 1996) p. 454.
 - [23] D. Aasen, M. Hell, R. V. Mishmash, A. Higginbotham, J. Danon, M. Leijnse, T. S. Jespersen, J. A. Folk, C. M. Marcus, K. Flensberg, and J. Alicea, *Phys. Rev. X* **6**, 031016 (2016).

Supplemental Material for: Proximity Effect Transfer from NbTi into a Semiconductor Heterostructure via Epitaxial Aluminum

A. C. C. Drachmann,¹ H. J. Suominen,¹ M. Kjaergaard,¹
B. Shojaei,² C. J. Palmstrøm,^{2,3} C. M. Marcus,¹ and F. Nichele¹

¹*Center for Quantum Devices and Station Q Copenhagen, Niels Bohr Institute
University of Copenhagen, Universitetsparken 5, 2100 Copenhagen, Denmark*

²*Materials Department, University of California, Santa Barbara, CA 93106, USA*

³*Department of Electrical and Computer Engineering,
University of California, Santa Barbara, CA 93106, USA*

(Dated: November 23, 2016)

This supplemental Material Section describes the experimental procedures used to fabricate the devices presented in the main text and presents additional electrical measurements

FABRICATION TECHNIQUES

Here we present detailed information on the fabrication of the reported devices. All patterning was done by e-beam lithography and unless otherwise stated, standard PMMA resist was used. To reduce exposure time, all designs were divided into inner structures with small beam current and outer structures with larger beam current.

To enable alignment of consecutive exposures, alignment marks are made from a Ti/Au (5/100nm) deposition. The marks are placed near the edge, all around the $2.5 \times 5 \text{ mm}^2$ chip.

Argon Milling and NbTi deposition

Starting from the blank chip with alignment markers, we spin coat an MMA/CZAR resist bilayer. The choice of this resist stack is particularly important for a successful Ar etching and deposition step. In particular, the bottom MMA layer provides a sizable undercut to facilitate the lift-off of closely spaced contacts while the CZAR layer can sustain prolonged Ar milling times.

Argon Milling is used to remove the native oxide that forms on the epitaxial Al upon exposure to air, allowing the NbTi to directly contact the metallic Al. For this step we used a Kaufman ion source installed in the superconductor deposition chamber. The etching was performed with a beam voltage of 600 V, an acceleration voltage of 120 V, an Ar-flow of 30 sccm at 1 mTorr pressure and with a rotating sample plate. The desired etching depth in the epitaxial Al is between 10 and 20 nm.

The etching rate of Kaufman source can fluctuate over long periods of time, requiring a fine tuning of the etching time prior to each run. In order to reduce the consumption of epitaxial material, two distinct etching rate calibrations was performed on Si chips with thermally grown SiO_2 layer. We found that etching 24.5 nm of SiO_2 resulted in an optimal etch depth in the epitaxial Al layer. The etching depth was measured with an optical profilometer for epitaxial Al and a spectral reflectometer for

SiO_2 . For every etching session, the Kaufman filament was heated by a 10 minutes milling of an empty sample plate. The sample was subsequently loaded in the deposition chamber and two more minutes of milling were performed on a closed sample shutter before allowing the Ar ions to reach the sample. The samples presented in the Main Text were etched 3 min and 31 sec.

Immediately after Ar etching the superconductive Ti/NbTi/NbTiN stack is deposited in the same chamber. First 2 nm of Ti are e-beam evaporated to ensure good contact between NbTi and Al. Second, 60 nm of NbTi are deposited from a $\text{Nb}_{2/3}\text{Ti}_{1/3}$ sputter target with a beam power of 200 W in a 4 mTorr pressure with an Argon flow rate of 50 sccm, resulting in a deposition rate of 10 nm min^{-1} . When the desired NbTi deposition is terminated, the sample shutter is closed. Third, a N_2 flow of 6 sccm is let into the chamber and the shutter is opened again after 30 sec to deposit 5 nm of NbTiN. The sample is kept rotating during the entire deposition to ensure uniformity.

After deposition, the resist bilayer is lifted-off by immersion of the sample in dioxolane. Sputtering deposition on a undercut resist results in prominent sidewalls, high and narrow structures that can cause several problems during the remaining fabrication steps. Most sidewalls were removed by sonication during liftoff of the sputtered material.

The epitaxial Al wafers do not require specifically designed bonding pads, as low resistance ($< 500 \Omega$) contacts can generally be obtained by directly bonding on the epitaxial Al. In the present case, however, the epitaxial Al covering the surface (and not protected by NbTi) will be removed in a subsequent step. For this reason it is important to deposit NbTi also on the bonding pads of the mesa structure.

Mesa Etching and Al etching

A new resist-pattern is defined for mesa etching on standard PMMA. After chemical development with

MIBK:IPA 1:3, the chip is plasma ashed for 60 sec to remove possible resist leftovers. The etching is performed in two steps. First the epitaxial Al, that covers the entire surface of the wafer, must be removed. Second, the III/V semiconductor is etched to isolate different devices on the same chip. The epitaxial Al is removed by a 12 sec etching in 50 °C Transene Aluminum Etchant type D. The process is terminated first with 30 s stirring in 50 °C DI water and then 30 s stirring in room temperature DI water.

After blow drying the chip with nitrogen, the III-V is immediately etched by a prepared room temperature $\text{H}_2\text{O}:\text{C}_6\text{H}_8\text{O}_7:\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2$ (220:55:3:3) solution for 330 s, resulting in an etching dept of about 600 nm. The etching is stopped with stirring in room temperature DI water. The resist is lifted off with dioxolane, followed by washes in acetone and isopropanol. At this point the NbTi forms a self aligned mask that can be used for etching the epitaxial Al covering the mesas, so no further electron beam lithography step is needed. The Al etching step previously described is then repeated, but with no resist mask.

Atomic Layer Deposition of HfO_2 and gate deposition

Immediately after removing the unwanted epitaxial Al, the chip is transferred in an atomic layer deposition chamber for the growth of 50 nm HfO_2 as a gate insulator. To minimize the exposure of the uncovered III-V material to oxygen, a constant flow of 20 sccm of N_2 is maintained in the chamber at any stage, also during pumping down. HfO_2 is deposited by 500 cycles of Tetrakis(dimethylamido)hafnium pulse and 60 sec waiting time and water pulse and 60 sec waiting time pre-heated at 90 °C.

Top gate deposition is done in two steps, one for the fine features and the other for larger elements such as bonding pads. In Fig. 1(e) of the Main Text it is possible to distinguish the two depositions from their different metal height and surface roughness. The fine features are defined in a single PMMA layer by evaporation of 5 nm Ti/30 nm Au and lift-off. The larger features are defined in a MMA/PMMA bilayer and require the evaporation of 50 nm Ti/700 nm Au. In both cases the chips are plasma ashed for 60 s after development to remove eventual resist leftovers.

S-SM-S IN-PLANE FIELD DEPENDENCE

An in-plane field, perpendicular to the current direction, is applied on the S-Sm-S junction while measuring critical current I_C , see Fig. SS.1. The vector-magnet was aligned before the measurement. Still I_C is fluctuating

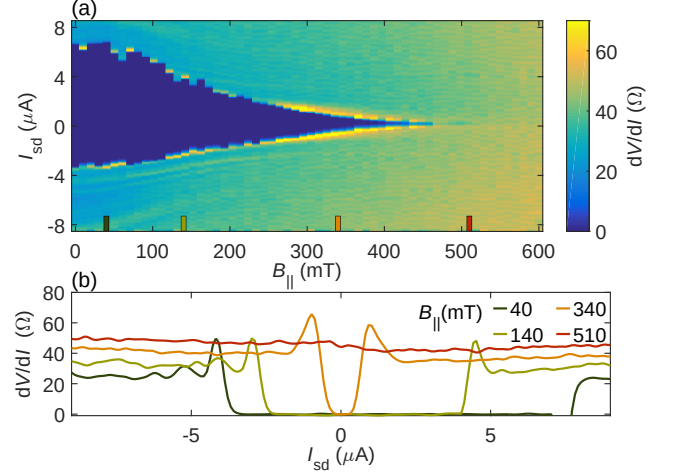


FIG. S.1. In-plane field dependence of the S-Sm-S. (a) Differential resistance dV/dI as a function of source-drain current I_{sd} and in-plane field $B_{||}$, applied perpendicular to the current flow. Colored squares show $B_{||}$ -values at which line cuts in (b) are taken. These line cuts are not offset.

at low fields, indicating flux jumps. These stabilizes at higher fields until the super-current dies out at ~ 500 mT. The sweeps are taken going from negative to positive, causing heating effects in the negative current region giving rise to the visible asymmetry of I_C .

QPC CONDUCTANCE

Beenakker predicted in 1992 [1] that an Andreev-enhanced QPC, like the one reported in this work, should have $4e^2/h$ steps in conductance after pinch-off. This was observed in an InAs 2DEG with epitaxial Aluminum S-QPC-Sm junction [2]. Despite the reported S-QPC-Sm does not show clear step features, presumably for the lower electron mobility of the wafer used in this work, the first plateau fluctuates around $4e^2/h$ rather than $2e^2/h$, see figure. SS.2.

Conductance in the tunneling regime

The parametric plot presented in Fig. 3(b) of the Main Text shows the QPC zero bias conductance as a function of the QPC high-bias conductance (which coincides with the normal state conductance up to experimental errors). The parametric plot was obtained from the measurement presented in Fig. S.3, showing the QPC conductance as a function of bias V_{sd} and gate voltage V_G close to pinch-off.

To accurately measure the sample conductance in the very low transmission regime, we used DC techniques

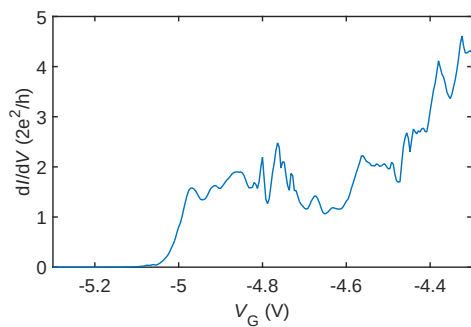


FIG. S.2. Differential conductance dI/dV as a function of gate voltage V_G , at zero bias, close to the pinch-off of the QPC.

only in a two-terminal configuration. A line resistance $R_{\text{Line}} = 11.8\text{k}\Omega$ was determined in a four-terminal measurement at $V_G = -4.85\text{ V}$. Figure Fig. S.3 is obtained by numerical differentiation of the measured DC current as a function of V_{SD} . The voltage dropping on the QPC was calculated as $V_{\text{eff}} = V_{\text{sd}} - I_{\text{DC}} R_{\text{Line}}$. The noise visible in Fig. SS.3 is presumably due to a combination of the differentiation method and intrinsic noise of the device, also noticed in AC measurements.

-
- [1] C. W. J. Beenakker, Phys. Rev. B **46**, 841 (1992).
 - [2] M. Kjaergaard, F. Nichele, H. J. Suominen, M. P. Nowak, M. Wimmer, A. R. Akhmerov, J. A. Folk, K. Flensberg, J. Shabani, C. J. Palmstrøm, and C. M. Marcus, Nat. Commun. **7**, 12841 (2016).

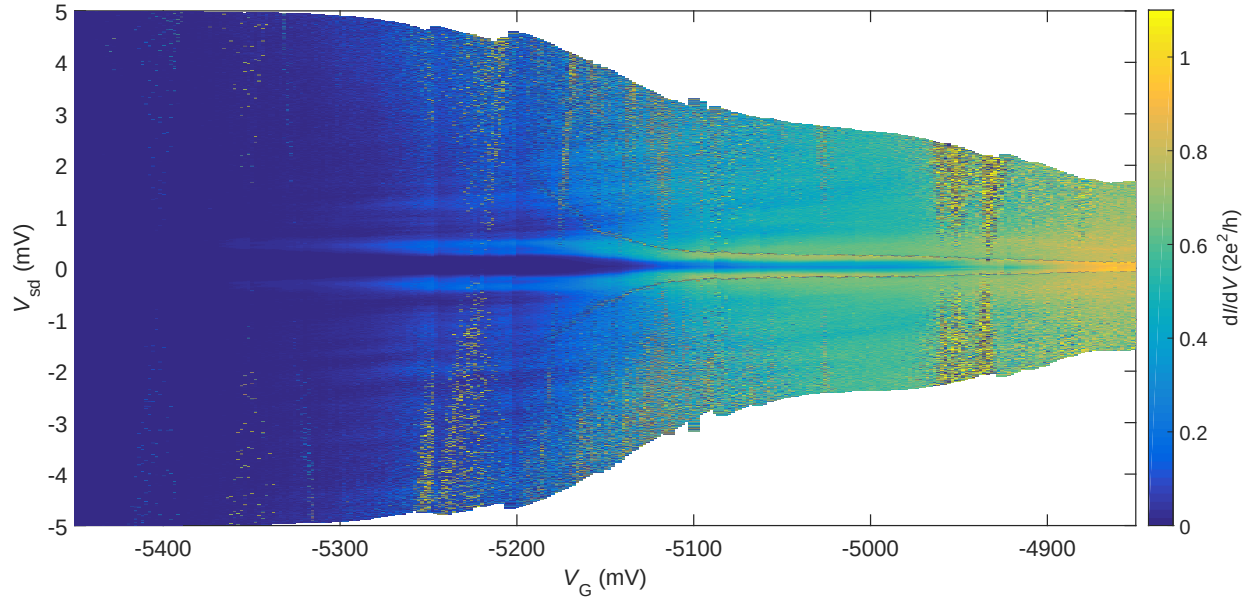


FIG. S.3. Numerically differentiated current dI/dV vs source-drain voltage V_{sd} for gate voltages V_G close to pinch-off with the QPC.

WORK ON AU-COVERED 2DEG

Au	5 nm
$\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$	15 nm
InAs	7 nm
$\text{Al}_{0.9}\text{Ga}_{0.1}\text{Sb}$	40 nm
Sb-based Substrate	

Figure B.1.: Illustration showing heterostructure of JSLo14: A InAs 2DEG covered by Au. Grown by Joon Sue Lee from Palmström Research Group

Besides working with InAs 2DEG covered with epitaxial aluminum, work was also done on InAs 2DEG covered with epitaxial gold. The idea of using Au instead of Al was to remove the need of milling before superconductor deposition, since the gold does not oxidize. The stack is displayed on [Figure B.1.](#)

To force electronic transport through the 2DEG and to enable gating, the Au had to be selectively stripped from the III/V. This was tried with potassium cyanide, KCN. This is a toxic substances that by any means must not come in chemical contact with any acid, since this forms the deadly hydrogen cyanide gas. Many precautions were taken during used.

Unfortunately, the etch was not selective and attacked the topmost III/V, leaving pits. We suspect that the Au diffused into the III/V, thus enabling KCN to attack these parts as well. Similar research on Au-covered InAs nanowires showed small superconducting gaps similar to alloys of Au and In, which also indicates a diffusion of Au into the III/V.

FABRICATION RECIPES

This part of the appendix has all the recipes used for making the working devices. They are written in short form so they can be cut out and brought into lab.

All lithography was done with the Elionix, and the files were formatted with use of Beamer.

All fab steps start with a clean and since the procedure is identical for the different fab steps I'll start by writing it down here:

Clean:

- Put chip in Dioxolane for 2 min
- Spray Acetone on the chip
- Spray Iso-Propanol (IPA) on the chip
- Blow dry with N₂ gun

C.1 ALIGNMENT MARKS

Clean

Resist:

- EL6, 4000rpm, 45 sec
- Bake 3 mins @ 185°C
- A4, 4000rpm, 45 sec
- Bake 3 mins @ 185°C

Elionix:

Current	Write Field	#Dots	Dwell Time
500 pA	300 µm	60.000	0.4 µs/dot

Development:

- 60 sec MIBK:IPA (1:2 dilution)
- 20 sec IPA
- Blow dry

Evaporation:

Sample rotation and no angle

- 10 nm Ti
- 100 nm Au

Liftoff:

- >1 hour in Dioxolane
- Acetone squirt
- IPA squirt
- Blow dry

C.2 TI/NBTI/NBTIN DEPOSTION**Clean****Resist:**

- EL6, 4000rpm, 45 sec
- Bake 3 mins @ 185°C
- Csar13, 4000rpm, 45 sec
- Bake 3 mins @ 185°C

Elionix:*Small Features*

Current	Write Field	#Dots	Dwell Time
500 pA	300 μm	60.000	0.17 $\mu\text{s}/\text{dot}$

Big Features

Current	Write Field	#Dots	Dwell Time
20 nA	600 μm	20.000	0.153 $\mu\text{s}/\text{dot}$

Development:

- 60 sec O-Xylene
- 60 sec MIBK:IPA (1:2 dilution)
- 20 sec IPA
- Blow dry

Milling on AJAz:

Before loading anything into AJA, do a 10 min milling on the empty sample plate to heat up the Kaufman -> Seems to make the milling rate more stable in subsequent uses. Do this with the same settings as are used for the actual milling:

Beam Voltage	600
Beam mAmps	12
Acc Voltage	120
Acc mAmps	4
Emission mAmps	13
Neutralizer mAmps	11

- Tilt: 15° away from Kaufman source
- Rotation: Nub at 70 rpm
- Ar Flow rate: 30 sccm
- Pressure: 1 mTorr

Earlier tests show that removing 24.5nm SiO₂ is equivalent to removing the native oxide of the epitaxial aluminum plus some of the Al, see [subsection 3.2.2](#). By finding the milling rate (R) for SiO₂ in nm/min, I can find the time (T) which I should mill the devices, to just remove the Al₂O₃: $T = 24.5\text{nm}/R$. To measure the milling rate two milling tests were made on SiO₂ chips:

- Measure height of two SiO₂ chips. An aRTie reflectometer from Filmetrics were used.
- Mill chip#1: 2 min heat up with shutter closed, 3 min with shutter open
- Measure height of chip#1, calculate the height difference and thereby the rate R₁.
- Mill chip#2: 2 min heat up with shutter closed, $T_2 = 24.5\text{nm}/R_1$ min with shutter open.
- Measure height of chip#2, calculate the height difference and thereby the rate R₂.

If $R_1 \sim R_2$ then the milling rate R can be assumed to be the mean of the two.

Load the real sample:

- Tilt: 15° away from Kaufman source
- Rotation: Nub at 70 rpm
- Ar Flow rate: 30 sccm
- Pressure: 1 mTorr
- Heat up: Turn on plasma with shutter closed for 1 min
- Mill: Open shutter and mill for $T = 24.5\text{nm/R min}$

Ti Evaporation at AJA 2:

- Tilt: 15°
- Rotation: Nub at 70 rpm
- Evaporate 2 nm

NbTi/NbTiN Sputtering at AJA 2:

- Tilt: 15°
- Rotation: Nub at 70 rpm
- Ar Flow rate: 50 sccm
- Pressure: 4 mTorr
- Ramp power to 200 W
- Open shutter, sputter NbTi for 6 min
- Close shutter
- N₂ Flow rate: 6 sccm
- Wait 30 sec
- Open shutter, sputter NbTiN for 30 sec
- Close shutter and ramp down

Liftoff:

- Sonicate in Dioxolane beaker for 1 min @ 80kHz, 100% power
- >1 hour in Dioxolane
- Sonicate in Dioxolane beaker for 1 min @ 80kHz, 100% power
- Acetone squirt
- IPA squirt
- Blow dry

C.3 MESA ETCH

Clean**Resist:**

- A4, 4000rpm, 45 sec
- Bake 3 mins @ 185°C

Elionix:*Small Features*

Current	Write Field	#Dots	Dwell Time
500 pA	300 μm	60.000	0.4 $\mu\text{S/dot}$

Big Features

Current	Write Field	#Dots	Dwell Time
20 nA	600 μm	20.000	0.36 $\mu\text{S/dot}$

Development:

- 60 sec MIBK:IPA (1:2 dilution)
- 20 sec IPA
- Blow dry
- 60 s in new Plasma Oven

Aluminum Etch:

Heat five beakers, three with Aluminum etchant D and two with MQ-water to $50 \pm 1.5^\circ\text{C}$. One of the three aluminum beakers is used to check temperature with a thermometer, and shouldn't be used for etching.

- 12 sec Al etch
- 20 sec hot MQ
- 40 sec room temp MQ
- Blow dry carefully

Mesa Etch:

H_2O : Citric Acid : H_3PO_4 : H_2O_2
 220 55 3 3

Add water, add citric acid, add H_3PO_4 and add H_2O_2 as the last step, approx 1 min before etching. H_2O_2 is stored in a fridge, and is taken out before each use. Magnet stirrer is used during mixing and etching. Prepare two beakers with MQ before etch:

- 330 s etch
- 20 s MQ beaker 1

- 20 s MQ beaker 2
- Blow dry thoroughly

Resist Strip:

- 60 sec Dioxolane
- Acetone Squirt
- IPA squirt
- Blow dry

Aluminum Etch:

Use same beakers as before

- 12 sec Al etch
- 20 sec hot MQ
- 40 sec room temp MQ
- Blowdry carefully

C.4 ALD

500 cycles of HfO_2 were used to deposit 50nm.

C.5 INNER GATES EVAPORATION**Clean****Resist:**

- A6, 4000rpm, 45 sec
- Bake 3 mins @ 185°C

Elionix:*Small Features*

Current	Write Field	#Dots	Dwell Time
100 pA	150 μm	60.000	0.38 $\mu\text{S}/\text{dot}$

Big Features

Current	Write Field	#Dots	Dwell Time
20 nA	600 μm	20.000	0.275 $\mu\text{S}/\text{dot}$

Development:

- 60 sec MIBK:IPA (1:2 dilution)

- 20 sec IPA
- Blow dry

Evaporation:

Sample rotation

- 5 nm Ti
- 40 nm Au

Liftoff:

- >1 hour in Dioxolane
- Acetone squirt
- IPA squirt
- Blow dry

C.6 OUTER GATES EVAPORATION

The amount of evaporated Au depends on the mesa etch depth D_{mesa} . If D_{mesa} is more than 400 nm, then do the deposition in two steps, to ensure successful liftoff.

Clean**Resist:**

- EL9, 4000rpm, 45 sec
- Bake 3 mins @ 185°C
- EL6, 4000rpm, 45 sec
- Bake 3 mins @ 185°C
- A4, 4000rpm, 45 sec
- Bake 3 mins @ 185°C

Elionix:

Current	Write Field	#Dots	Dwell Time
20 nA	600 μm	20.000	0.36 $\mu\text{S/dot}$

Development:

- 60 sec MIBK:IPA (1:2 dilution)
- 20 sec IPA
- Blow dry

- Ash: 4 min in new plasma oven

Evaporation:

Sample rotation during all steps

- 10 nm Ti no tilt
- D_{mesa} Au no tilt
- 50 nm Au at 10° tilt

Liftoff:

- >1 hour in Dioxolane
- Acetone squirt
- IPA squirt
- Blow dry

COMPARISON OF THREE SIMILAR NBTI DEPOSITIONS

The devices reported in [chapter 4](#) and [chapter 5](#) were made from one of three exposures on the chip: Bo509.7. Devices of the three exposures all showed enhanced superconducting properties compared to earlier results with aluminum as the only superconductor. Each deposition had two S-Sm-S junctions and four S-QPC-Sm junctions, so 18 devices in total. Of those, only eight device could be bonded up, due to limitations on the amount of lines on the daughter board. Measurement of the induced gap in the bonded device is summarized in [Table 2](#):

	QPC 1	QPC 2	S-Sm-S
Deposition 1	Leaky gates	Leaky gates	$\Delta^* \sim 580 \mu\text{eV}$
Deposition 2	$\Delta^* \sim 300 \mu\text{eV}$	Not bonded	Not measured
Deposition 3	$\Delta^* \sim 430 \mu\text{eV}$	Noisy, but $\Delta^* \sim 450 \mu\text{eV}$	$\Delta^* \sim 500 \mu\text{eV}$

Table 2.: Comparison of induced gap in NbTi-based devices from three different depositions. From the S-QPC-Sm devices, the induced gaps Δ^* are extracted by tunnel spectroscopy, while the MAR resonances in the S-Sm-S's are used to extract Δ^* .

These results show a fluctuation in induced gap, but a consistent improvement compared to values of aluminum-based device [38, 45]. This indicates that the milling calibrations elaborated in [subsection 3.2.2](#) do provide somewhat consistent results.

ALIGNMENT WITH VECTOR MAGNET

When preparing a device chip for loading, it is advised to always have the field directions of the vector magnet in mind. Our Triton dilution free cryostats have a vector magnet. It can produce magnetic fields in three orthogonal directions, with the strongest field pointing in the longitudinal direction of the fridge. Combining the three directions enables fields pointing in all possible directions of a 3D sphere.

When designing devices for high-field ($B > 1\text{T}$), one should keep in mind that all devices have the high-field-axis pointing in the same direction. In a puck, the motherboard can be oriented along or perpendicular to the high-field-axis, see [Figure 3.12](#). In the case of wanting the high field in plane of the device chip, the chips orientation should be chosen carefully when sticking it on a daughter board. For in-plane sweeps even small angles matters since small perpendicular fields alters the superconducting properties, see [Figure 4.5](#) and [Figure 5.4](#), especially for Josephson junctions.

Almost always, the chips are at least a bit miss-aligned to the vector magnets axes. In this work, the miss-alignment between $B_{\perp}$ and $B_{\parallel}$ was taken into account, see [Figure E.1](#), which also defines the magnetic field directions B_y and B_z .

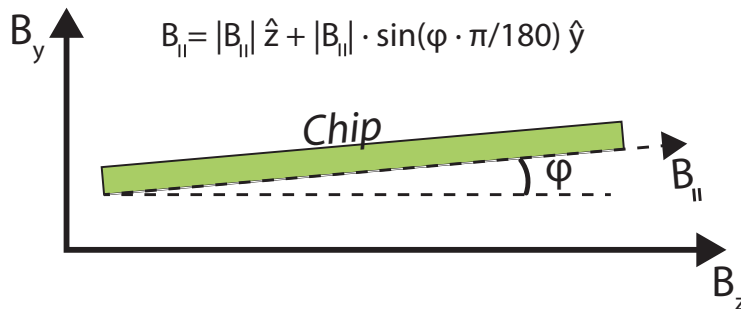


Figure E.1.: Illustration of a chip miss-aligned according to the vector magnet axes (y,z). The miss-alignment angle ϕ , found by [Equation E.1](#), is used to apply aligned in plane field $B_{\parallel}$.

To determine the miss-alignment angle, ϕ , B_y vs bias sweeps are done at different constant in-plane $B_{z,\text{const}}$, with the purpose of finding the field

$B_{y,\max}$ at which a superconducting state persists furthest out in bias. This can both be done with a S-Sm-S looking at the critical current or with a S-QPC-Sm looking at the gap closing. The critical current in S-Sm-S is easier to use since no gates are involved and since the transition from supercurrent to finite resistance is easy to see, and the maximum I_c is easily determined. Once $B_{y,\max}$ is found for some $B_{z,\text{const}}$ (the more the merrier), ϕ can be determined by fitting with the tangent relation

$$\phi = \tan^{-1} \left(\frac{B_{y,\max}}{B_{z,\text{const}}} \right). \quad (\text{E.1})$$

Once ϕ is determined a field direction parallel to the chip ($B_{||}$) can be obtained by sweeping both $B_z = |B_{||}|$ and $B_y = |B_{||}| \cdot \sin(\phi)$. A multiplication of $\cos(\phi)$ is not used on B_y since ϕ usually is small making $\cos(\phi) \approx 1$. This method was used to obtain all in-plane field sweeps presented in this thesis.

REMOVING LINE RESISTANCE FROM CONDUCTANCE MAP

As mentioned in [section 4.2](#), the setup, illustrated on [Figure 3.15\(b\)](#), used to measure the bias-gate 2D map (shown in [figure Figure 4.4\(a\)](#)), was two-terminal, so the actual voltage drop across the device is not known from that measurement alone. Before the 2D sweep, a 4-terminal voltage bias sweep was done at $V_{\text{gate}} = -4850$ mV, which was the same V_{gate} from which the 2D map was started. The voltage drop across the lines is determined by the difference between the applied V_{sd} and the voltage drop across the device V_{Dev} which is measured 4-terminal. Plotting this voltage difference as a function of the measure current I_{DC} enables determination of the line resistance, see [Figure F.1](#).

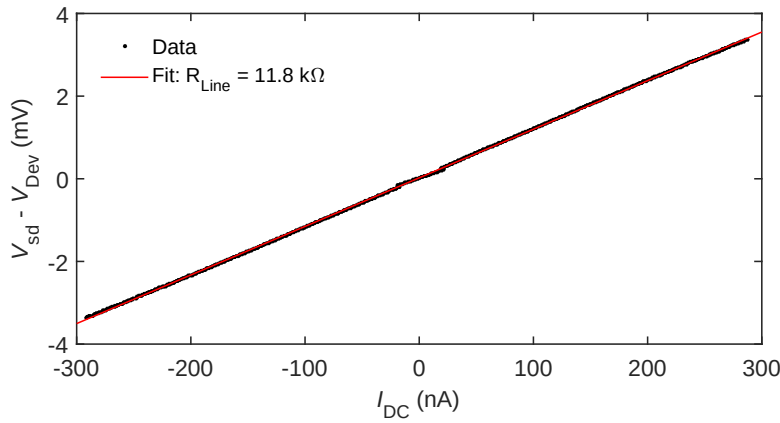


Figure F.1.: Difference between applied voltage V_{sd} and voltage drop across the device V_{Dev} as a function of measured DC current I_{DC} . Data is from a 4-terminal measurement on the S-QPC-Sm device, see [Figure 4.1](#). Fitting a straight line extracts the line resistance.

With the line resistance at hand, corrections to 2-terminal measurements, see [Figure 4.4\(a\)](#), can be done for any gate-voltage. The voltage bias axis at each V_{Gate} is squeezed towards zero with this equation $V_{\text{Dev}} = V_{\text{sd}} - R_{\text{Line}} \cdot I_{\text{DC}}$. The result is shown on [Figure F.2](#).

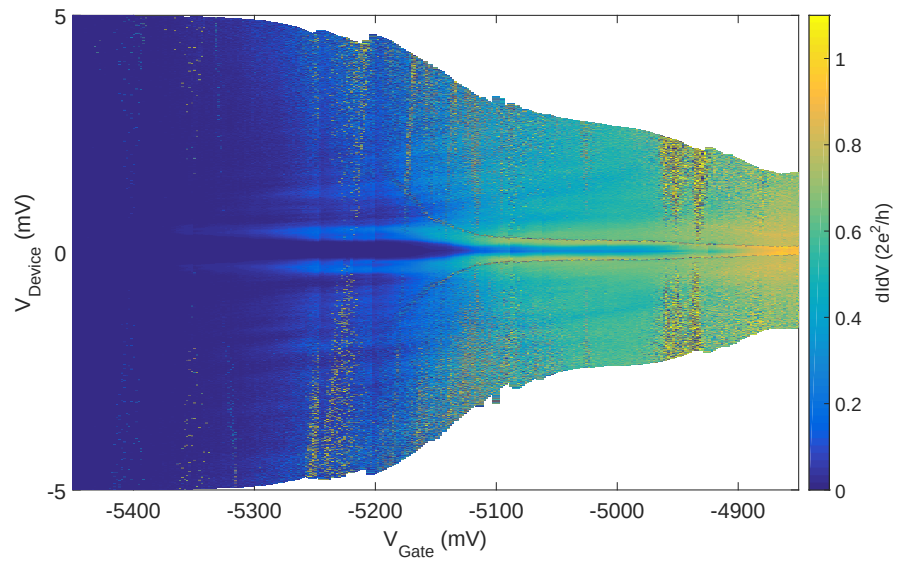


Figure F.2.: Differential conductance, dI/dV , measurement as a function of V_{sd} and gate voltage V_{gate} obtained by numerical differentiation of I_{DC} . Compared to Figure 4.4(a), the voltage drop across the line resistance is subtracted.

GATING OF REPORTED JOSEPHSON JUNCTION

The S-Sm-S device reported in [chapter 5](#) was fabricated with a top gate, but unfortunately it was leaky before it could pinch off the 2DEG. [Figure G.1\(a\)](#) shows that the gate becomes leaky around $V_{\text{Gate}} = 1.5$ V.

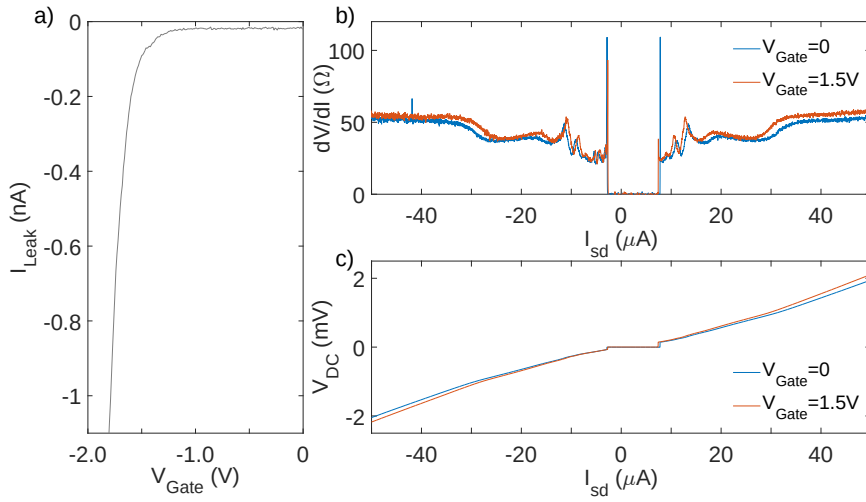


Figure G.1.: **(a)** Leakage current through the ALD as a function of gate voltage V_{Gate} **(b)** Differential resistance dV/dI vs current bias I_{sd} at $V_{\text{Gate}} = 0$ and 1.5 V. **(c)** DC voltage V_{DC} vs current bias I_{sd} at $V_{\text{Gate}} = 0$ and 1.5 V.

Even though not being able to pinch of the 2DEG, we are still able to show that the top gate affects the electrons. [Figure G.1\(b\)](#) shows differential resistance vs source-drain current for $V_{\text{Gate}} = 0$ and 1.5 V. As expected [\[45\]](#), a more negative V_{Gate} drags the MAR resonances towards zero bias, while the amplitude of the measured V_{DC} increases, see [Figure G.1\(c\)](#).

FRAUNHOFER MEASUREMENTS ON EARLIER DEVICES

Here we present Fraunhofer measurements on two earlier device, see [Figure H.1](#).

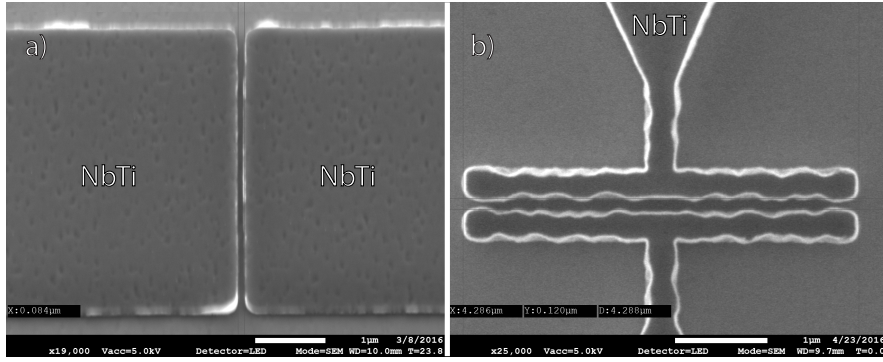


Figure H.1.: SEM of S-Sm-S. Taken after Ti/NbTi/NbTiN deposition
(a) Regular S-Sm-S device with a spacing of ~ 80 nm. **(b)** S-Sm-S device with thin bars and a spacing of ~ 120 nm. The wavy features are side walls from the sputtering deposition.

[Figure H.1\(a\)](#) was from the first deposition with successful milling having an induced gap of $\Delta^* = 310 \mu\text{eV}$, extracted from MAR. Among other measurements Fraunhofer patterns were measured by applying perpendicular magnetic fields $B_{\perp}$, see [Figure H.2\(a\)](#). These features look very clean when compared with [Figure 5.4](#). Another distinct difference is the closely spaced nodes in [Figure H.2\(a\)](#). The mean node spacing $B_{\perp, \text{node}}$ was extracted to be 0.27 mT. With [Equation 5.2](#) and the width W and separation L of the superconducting banks ($4.3 \mu\text{m}$ and 80 nm respectively), a theoretical estimate of the node spacing can be found:

$$\pi = \frac{\pi B_{\perp, \text{node}} L W}{\Phi_0} \rightarrow B_{\perp, \text{node}} = \frac{\Phi_0}{L W}, \quad (\text{H.1})$$

with the flux quantum $\Phi_0 = h/2e$. The estimated node spacing is 6.02 mT, a factor 22 higher than observed. This difference originates presumably from flux focusing: Most flux lines approaching the superconductors are not penetrating but bending around, thus increasing the effective magnetic

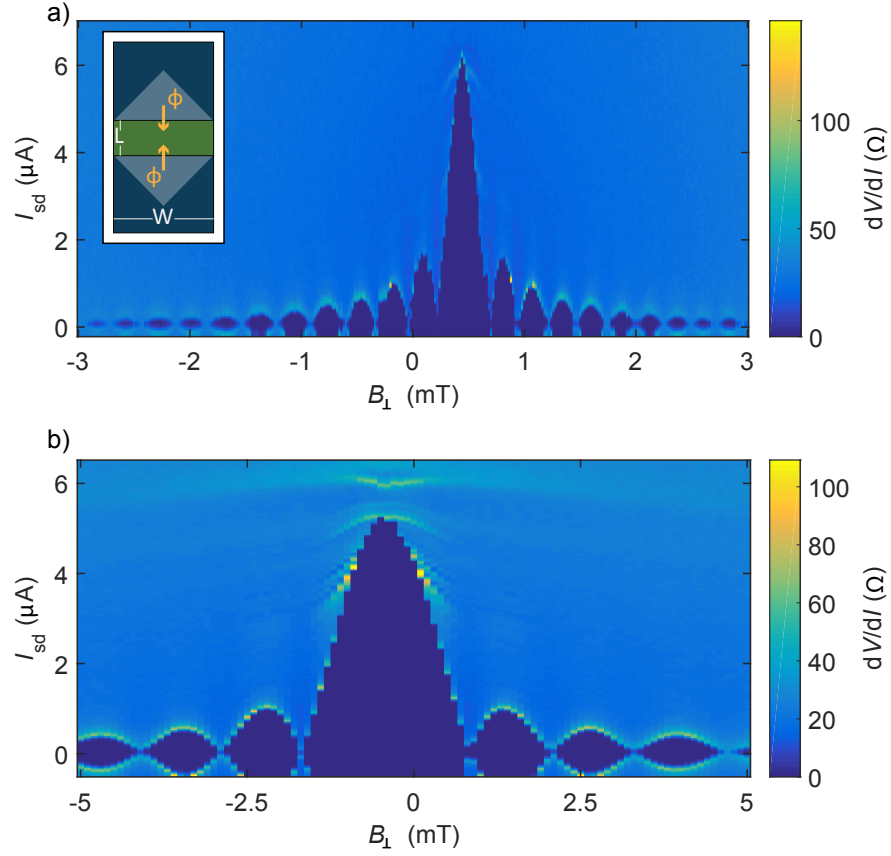


Figure H.2.: **(a)** Differential resistance dV/dI as a function of perpendicular field $B_{\perp}$ and current bias I_{sd} , showing Fraunhofer patterns with tight node spacing. Measured from Figure H.1(a). Inset defines L and W , and the shaded area adds to flux-focussing in the constriction. **(b)** Differential resistance dV/dI as a function of $B_{\perp}$ and I_{sd} , showing Fraunhofer patterns with widely spaced nodes. Measured from Figure H.1(b).

field penetrating the normal region. The part of the superconductors that forces flux lines into the normal region are marked (shaded) in the inset of Figure H.2(a). The shortest distance around the superconductor, when starting in the shaded region, is through the Josephson junction constriction. The flux-adding area from each superconducting bank is $\sim W^2/4$.

To verify this hypothesis, a test-device was made along with other new devices, see Figure H.1(b). The idea behind this geometry was to reduce the flux-adding area to achieve Fraunhofer patterns closer to the theoretical predictions. The device was made before the reported milling calibrations, and had a bad milling, leading to an induced gap of $150 \mu eV$, extracted from MAR. The extracted node spacing is 1.31 mT . With $L = 120 \text{ nm}$ and $W = 4.2 \mu m$ the theoretical estimate is 4.1 mT , which is only a factor 3.1 difference which is a factor 7 improvement compared to the regular S-Sm-S geometry.

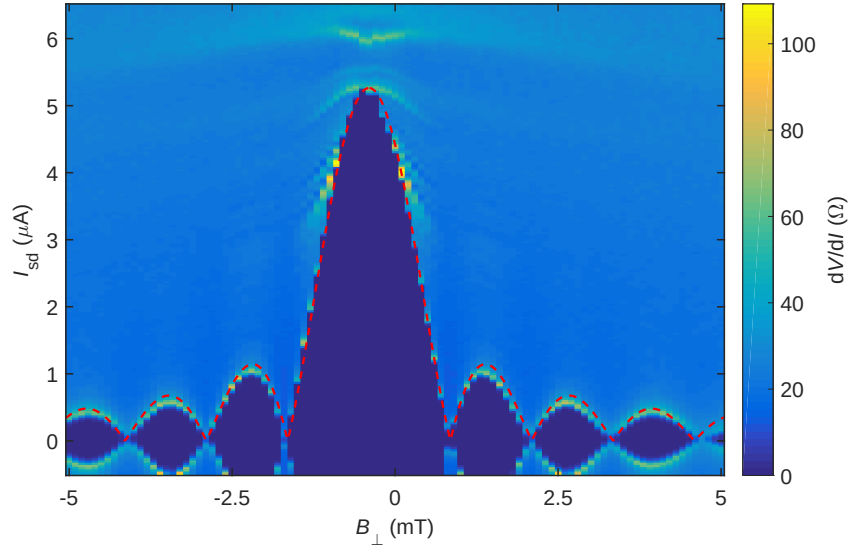


Figure H.3.: Data from Figure H.2(b) fitted with Equation 5.2 having $I_c(0)$ and the area $A = L \cdot W$ as free parameters. The fit is displayed as a red dashed curve.

The shape of the Fraunhofer pattern in Figure H.2(b) look a lot like the theory curve. To test the resemblance, $I_c(B_{\perp})$ was extracted from the dataset and fitted with Equation 5.2, taking $I_c(0)$ and the area $A = L \cdot W$ as free parameters, to optimize the match. The result is shown in Figure H.3.

BIBLIOGRAPHY

- [1] J. Kelly, R. Barends, A. G. Fowler, A. Megrant, E. Jeffrey, T. C. White, D. Sank, J. Y. Mutus, B. Campbell, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, I.-C. Hoi, C. Neill, P. J. J. O'Malley, C. Quintana, P. Roushan, A. Vainsencher, J. Wenner, A. N. Cleland, and J. M. Martinis, "State preservation by repetitive error detection in a superconducting quantum circuit," *Nature*, vol. 519, no. 7541, pp. 66–69, 2015. (Cited on page 2.)
- [2] J. Alicea, Y. Oreg, G. Refael, F. von Oppen, and M. P. a. Fisher, "Non-Abelian statistics and topological quantum information processing in 1D wire networks," *Nature Physics*, vol. 7, no. 5, pp. 412–417, 2011. (Cited on page 2.)
- [3] M. Leijnse and K. Flensberg, "Quantum information transfer between topological and spin qubit systems," *Physical Review Letters*, vol. 107, no. 21, pp. 1–5, 2011. (Cited on page 2.)
- [4] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. a. M. Bakkers, and L. P. Kouwenhoven, "Signatures of Majorana Fermions in," *Science*, vol. 336, no. 6084, p. 1003, 2012. (Cited on page 2.)
- [5] L. P. Rokhinson, X. Liu, and J. K. Furdyna, "The fractional a.c. Josephson effect in a semiconductor–superconductor nanowire as a signature of Majorana particles," *Nature Physics*, vol. 8, no. 11, pp. 795–799, 2012. (Cited on page 2.)
- [6] A. Das, Y. Ronen, Y. Most, Y. Oreg, M. Heiblum, and H. Shtrikman, "Zero-bias peaks and splitting in an Al-InAs nanowire topological superconductor as a signature of Majorana fermions," *Nature Physics*, vol. 8, no. 12, pp. 887–895, 2012.
- [7] M. T. Deng, C. L. Yu, G. Y. Huang, M. Larsson, and H. Q. Xu, "Anomalous Zero-Bias Conductance Peak in a Nb-InSb Nanowire-Nb Hybrid Device," 2012.

- [8] H. O. H. Churchill, V. Fatemi, K. Grove-Rasmussen, M. T. Deng, P. Caroff, H. Q. Xu, and C. M. Marcus, "Superconductor-nanowire devices from tunneling to the multichannel regime: Zero-bias oscillations and magnetoconductance crossover," *Physical Review B - Condensed Matter and Materials Physics*, vol. 87, no. 24, pp. 1–6, 2013.
- [9] S. M. Albrecht, A. P. Higginbotham, M. Madsen, F. Kuemmeth, T. S. Jespersen, J. Nyg, P. Krogstrup, and C. M. Marcus, "Exponential Protection of Zero Modes in Majorana Islands," *Nature*, vol. 531, no. 7593, pp. 206–209, 2016.
- [10] H. Zhang, Ö. Gül, S. Conesa-Boj, K. Zuo, V. Mourik, F. K. de Vries, J. van Veen, D. J. van Woerkom, M. P. Nowak, M. Wimmer, D. Car, S. Plissard, E. P. A. M. Bakkers, M. Quintero-Pérez, S. Goswami, K. Watanabe, T. Taniguchi, and L. P. Kouwenhoven, "Ballistic Majorana nanowire devices," pp. 1–21, 2016. (Cited on pages 2, 25, 41, and 54.)
- [11] M. Hell, M. Leijnse, and K. Flensberg, "Two-dimensional platform for networks of Majorana bound states," no. i, 2016. (Cited on page 2.)
- [12] F. Pientka, A. Keselman, E. Berg, A. Yacoby, A. Stern, and B. I. Halperin, "Topological Superconductivity in a Planar Josephson Junction," pp. 1–16, 2016. (Cited on page 2.)
- [13] M. Amado, A. Fornieri, F. Carillo, G. Biasiol, L. Sorba, V. Pellegrini, and F. Giazotto, "Electrostatic tailoring of magnetic interference in quantum point contact ballistic Josephson junctions," *Physical Review B - Condensed Matter and Materials Physics*, vol. 87, no. 13, pp. 1–5, 2013. (Cited on page 2.)
- [14] Z. Wan, A. Kazakov, M. J. Manfra, L. N. Pfeiffer, K. W. West, and L. P. Rokhinson, "Induced superconductivity in high-mobility two-dimensional electron gas in gallium arsenide heterostructures," *Nature communications*, vol. 6, no. May, p. 7426, 2015.
- [15] H. Takayanagi and T. Akazaki, "Andreev reflection at the superconductor-two-dimensional-electron-gas interface by a quantum point contact," *Physical Review B*, vol. 52, no. 12, pp. 8633–8636, 1995. (Cited on page 2.)
- [16] J. Shabani, M. Kjaergaard, H. J. Suominen, Y. Kim, F. Nichele, K. Pakrouski, T. Stankevic, R. M. Lutchyn, P. Krogstrup, R. Feidenhans'l, S. Kraemer, C. Nayak, M. Troyer, C. M. Marcus, and C. J. Palmstrøm, "Two-dimensional epitaxial superconductor-semiconductor heterostructures: A platform for topological superconducting networks," *Physical Review B - Condensed Matter and Materials Physics*, vol. 93, no. 15, 2016. (Cited on pages 2, 12, and 18.)
- [17] J. Clarke and F. K. Wilhelm, "Superconducting quantum bits," *Physics World*, vol. 17, no. 12, pp. 29–33, 2004. (Cited on page 2.)

- [18] H. Weinstock and R. W. Raslton, *The New Superconducting Electronics*. Kluwer Academic Publishers, 1993. (Cited on page 2.)
- [19] M. Tinkham, *Introduction to Superconductivity*. New York: McGraw-Hill Book Co., second ed., 1996. (Cited on pages 6, 8, and 43.)
- [20] G. E. Blonder, M. Tinkham, and T. M. Klapwijk, "Transition from metallic to tunneling regimes in superconducting microconstrictions: Excess current, charge imbalance, and supercurrent conversion," *Physical Review B*, vol. 25, pp. 4515–4532, apr 1982. (Cited on pages 9, 39, and 47.)
- [21] T. Schäpers, "Superconductor/Semiconductor Junctions," *Springer*, 2001. (Cited on pages 10 and 15.)
- [22] V. Cherkez, J. C. Cuevas, C. Brun, T. Cren, G. Ménard, F. Debontridder, V. S. Stolyarov, and D. Roditchev, "Proximity effect between two superconductors spatially resolved by scanning tunneling spectroscopy," *Physical Review X*, vol. 4, no. 1, pp. 1–13, 2014. (Cited on pages 11 and 37.)
- [23] H. Bruus and K. Flensberg, *Many-Body Quantum Theory in Condensed Matter Physics: An Introduction*. Oxford University Press, USA, 2004. (Cited on pages 11 and 37.)
- [24] A. A. Golubov, E. P. Houwman, J. G. Gijsbertsen, V. M. Krasnov, J. Flokstra, H. Rogalla, and M. Y. Kupriyanov, "Proximity effect in superconductor-insulator-superconductor Josephson tunnel junctions: Theory and experiment," *Physical Review B*, vol. 51, no. 2, pp. 1073–1089, 1995. (Cited on page 12.)
- [25] T. Ihn, "Semiconductor Nanostructures," 2010, p. 569, 2010. (Cited on page 13.)
- [26] Kittel, *Introduction to Solid State Physics*. 2010. (Cited on page 14.)
- [27] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*, vol. 2 of *Holt-Saunders International Editions: Science : Physics*. Brooks Cole, 1976. (Cited on page 15.)
- [28] J. Davies, *The Physics of Low-Dimensional Semiconductors*, vol. Cambridge. 1998. (Cited on pages 15 and 54.)
- [29] a. Chrestin, T. Matsuyama, and U. Merkt, "Evidence for a proximity-induced energy gap in Nb/InAs/Nb junctions," *Physical Review B*, vol. 55, no. 13, pp. 8457–8465, 1997. (Cited on page 15.)
- [30] W. Chang, S. M. Albrecht, T. S. Jespersen, F. Kuemmeth, P. Krogstrup, J. Nygård, and C. M. Marcus, "Hard gap in epitaxial semiconductor-superconductor nanowires," *Nature nanotechnology*, vol. 10, no. 3, pp. 232–6, 2015. (Cited on pages 18 and 41.)

- [31] L. Yu, R. K. Singh, H. Liu, S. Y. Wu, R. Hu, D. Durand, J. Bulman, J. M. Rowell, and N. Newman, "Fabrication of niobium titanium nitride thin films with high superconducting transition temperatures and short penetration lengths," *IEEE Transactions on Applied Superconductivity*, vol. 15, no. 1, pp. 44–47, 2005. (Cited on page 25.)
- [32] K. Makise, H. Terai, M. Takeda, Y. Uzawa, and Z. Wang, "Characterization of NbTiN thin films deposited on various substrates," *IEEE Transactions on Applied Superconductivity*, vol. 21, no. 3 PART 1, pp. 139–142, 2011.
- [33] C. Benvenuti, P. Chiggiato, L. Parrini, and R. Russo, "Production of niobium-titanium nitride coatings by reactive diffusion for superconducting cavity applications," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 124, no. 1, pp. 106–111, 1997.
- [34] N. N. Iosad, B. D. Jackson, F. Ferro, J. R. Gao, S. N. Polyakov, P. N. Dmitriev, and T. M. Klapwijk, "Source optimization for magnetron sputter-deposition of NbTiN tuning elements for SIS THz detectors," *Superconductor Science and Technology*, vol. 12, no. 11, pp. 736–740, 1999.
- [35] Lei Yu, N. Newman, and J. Rowell, "Measurement of the coherence length of sputtered Nb/sub 0.62/Ti/sub 0.38/N thin films," *IEEE Transactions on Applied Superconductivity*, vol. 12, no. 2, pp. 1795–1798, 2002. (Cited on page 25.)
- [36] T. Shiino, S. Shiba, N. Sakai, T. Yamakura, L. Jiang, Y. Uzawa, H. Maezawa, and S. Yamamoto, "Improvement of the critical temperature of superconducting NbTiN and NbN thin films using the AlN buffer layer," *Superconductor Science and Technology*, vol. 23, no. 4, p. 045004, 2010. (Cited on page 26.)
- [37] F. Pobell, *Matter and methods at low temperatures*. Springer, 2007. (Cited on page 32.)
- [38] M. Kjaergaard, F. Nichele, H. J. Suominen, M. P. Nowak, M. Wimmer, A. R. Akhmerov, J. A. Folk, K. Flensberg, J. Shabani, C. J. Palmstrøm, and C. M. Marcus, "Quantized conductance doubling and hard gap in a two-dimensional semiconductor-superconductor heterostructure," vol. 1, 2016. (Cited on pages 37, 40, 41, 42, 43, and 77.)
- [39] B. J. Van Wees, H. Van Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. Van Der Marel, and C. T. Foxon, "Quantized conductance of point contacts in a two-dimensional electron gas," *Physical Review Letters*, vol. 60, no. 9, pp. 848–850, 1988. (Cited on pages 37 and 40.)
- [40] H. van Houten and C. Beenakker, "Quantum Point Contacts," *Phys. Today*, vol. 49, no. July, p. 7, 1996. (Cited on pages 37 and 40.)

- [41] C. W. J. Beenakker, "Quantum transport in semiconductor-superconductor microjunctions," *Physical Review B*, vol. 46, no. 19, pp. 841–844, 1992. (Cited on pages 39 and 40.)
- [42] B. Josephson, "Possible new effects in superconductive tunnelling," *Physics Letters*, vol. 1, no. 7, pp. 251–253, 1962. (Cited on page 45.)
- [43] M. Octavio, M. Tinkham, G. E. Blonder, and T. M. Klapwijk, "Subharmonic energy-gap structure in superconducting constrictions," *Physical Review B*, vol. 27, no. 11, pp. 6739–6746, 1983. (Cited on page 45.)
- [44] K. Flensberg, J. B. Hansen, and M. Octavio, "Subharmonic energy-gap structure in superconducting weak links," *Physical Review B*, vol. 38, no. 13, pp. 8707–8711, 1988. (Cited on page 45.)
- [45] M. Kjaergaard, H. J. Suominen, M. P. Nowak, A. R. Akhmerov, J. Shabani, C. J. Palmstrøm, F. Nichele, and C. M. Marcus, "Transparent Semiconductor-Superconductor Interface and Induced Gap in an Epitaxial Heterostructure Josephson Junction," pp. 1–8, 2016. (Cited on pages 45, 47, 77, and 83.)
- [46] T. Hoss, C. Strunk, T. Nussbaumer, R. Huber, U. Staufer, and C. Schönenberger, "Multiple Andreev reflection and giant excess noise in diffusive superconductor/normal-metal/superconductor junctions," *Physical Review B*, vol. 62, no. 6, p. 4079, 2000. (Cited on page 48.)
- [47] K. Inoue and T. Kawakami, "Magnetic field dependencies of critical currents in InAs-coupled Josephson junctions," *Journal of Applied Physics*, vol. 65, no. 4, pp. 1631–1636, 1989. (Cited on page 49.)
- [48] A. Barone and G. Paterno, "Physics and Applications of the Josephson Effect," 1982. (Cited on page 50.)
- [49] S. K. H. Lam and D. L. Tilbrook, "Development of a niobium nanosuperconducting quantum interference device for the detection of small spin populations," *Applied Physics Letters*, vol. 82, no. 7, pp. 1078–1080, 2003. (Cited on page 55.)