



Pulsed gate experiments in two-dimensional semiconductor quantum dot arrays

Master Thesis

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Abstract

Spin qubits hosted in industry-fabricated silicon quantum dot devices have good prospects of tackling the scalability challenge that comes with realizing a large-scale, fault-tolerant quantum information processor. High-fidelity single- and two-qubit gates as well as long coherence times have been successfully demonstrated using spin qubits hosted in silicon QD devices [1][2]. A challenge in the operation of spin qubits hosted by (industry-fabricated) Si QD-devices is the complex valley-orbital structure that is unknown a priori and highly dependent on the atomic details of the confining interface [3], thereby strongly deviating from device to device.

Here, we perform pulsed gate experiments in a foundry-fabricated silicon-on-insulator device. We report the observation of enhanced relaxation rates at distinguishable values of the double dot detuning, which are attributed to level crossings in the double dot two-electron spectrum. The measurements are based on time-resolved measurements using gate-based dispersive RF sensing while applying a self-compensating detuning-axis pulse cycle.

In addition, by exploiting the two-dimensionality of a 2x2 Si QD array, we demonstrate an alternative RF charge sensing method by using a DQD as an RF charge sensor.

Furthermore, we tune and explore a singlet-triplet qubit in a GaAs/AlGaAs heterostructure device by operating exchange oscillations of a singlet-triplet qubit hosted by a GaAs double quantum dot.

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Introduction

The field concerned with information processing based on quantum bits, has experienced extremely rapid development, ever since the notion of quantum computation was raised by Pail Benioff in 1980 [4]. The first decade thereafter was primarily in light of developing quantum algorithms that are predicted to result in a significant speedup in computation times, leading to well-known quantum algorithms like Deutsch–Jozsa algorithm [5], Shor’s algorithm [6] and Grover’s algorithm [7]. This was followed by an increasing effort being directed towards the experimental realization of a well-defined quantum-mechanical two-level system whose basis states can be initialized, readout, and manipulated. The field concerned with the experimental realization of qubits, quantum hardware, has been a key agent in the astounding progress made in quantum computing over the last two decades, enabling the emergence of promising experimental realizations of well-defined qubits based on a diverse range of platforms and underlying physical principles.

Several experimental qubit realizations are promising candidates for quantum computation, demonstrating high coherence and high-fidelity single- and two-qubit operations.

While promising results have been obtained on the few-qubit level, scaling up to more qubits is one of the remaining challenges. The number of physical qubits necessary for fault-tolerant computation of the most promising quantum algorithms has been estimated to lie around $10^6 - 10^8$ physical qubits [8][9][10]. Consequently, the physical system needed for a single qubit as well as the readout and control schemes requires to be scalable in order to realize a large, fault-tolerant quantum processor that has the ability to compute relevant algorithms with minimal error (requiring the implementation of error correction codes).

Spin-based qubit encodings in semiconductor quantum dot devices comprise an attractive experimental qubit platform for working towards a fault-tolerant quantum processor. The inherent small size of the physical implementation of a single-qubit in electrostatically-defined quantum dot platforms compared to other experimental qubit implementations like superconducting qubits, in combination with long coherence times compared to single- and two-qubit gate operation times as well as high single-qubit ($F_{1Q}=99.96\%$ [11]) and two-qubit gate fidelities ($F_{2Q}=98\%$ [11]) makes semiconductor spin qubits one of the leading candidates for the realization of a scalable quantum information processor ¹.

In addition, the possibility of harnessing the existing semiconductor industry for the large-scale fabrication of semiconductor spin qubit devices will have the potential advantage of providing a high yield, throughput, and uniformity [2] in the fabrication of devices containing hundreds or thousand qubits. This significantly enhances the prospects of facing the scalability challenge.

This, together with the high coherence of spin qubits in Si², has motivated the spin qubit community to shift focus to silicon gate-defined QD devices. Spin qubits in industry-fabricated silicon QD devices have been demonstrated to reach coherence times close to coherence times reported in silicon QD devices fabricated in academic labs [2].

While using spin qubits in QD systems for quantum computation purposes has received a lot of attention, the applications of gate-defined QD systems are more diverse than fault-tolerant quantum computation.

Semiconductor QD arrays could play an essential role in the exploration of quantum simulation. The aim of quantum simulation is to emulate a complex quantum problem by measuring the evolution of a quantum state in an engineered system that acts according to the Hamiltonian that is to be simulated.

GaAs quantum dot devices have a relative in its simplicity of fabrication [12] and have played a crucial role in the early development of spin qubits in electrostatically-defined quantum dot devices [13]. However, limited coherence times of spin qubits hosted in GaAs as a result of the interaction of the spin qubit's state with the nuclear spin bath present in GaAs, make the experimental platform less attractive for the realization of the scalable spin-qubit-based quantum information processor. Methods to counteract dephasing of the spin qubit's state have been successfully harnessed

¹It is too simplistic to say that the physical qubit realization needs to be scalable [9], since the readout and control scheme, as well as the interconnectivity between instruments required to operate and readout the qubit's state, require to be scalable. A growing effort has been directed to making the control and readout scheme more scalable by for example moving to voltage control to the chip level (at cryogenic temperatures) [9] and more compact readout schemes. In combination with the demonstration of successful operation at higher temperatures, the prospects for scalability are increasing.

²A primary source of decoherence in materials like GaAs is the interaction of the qubit's state with the nuclear spin states of isotopes in the material. The lower concentration of half-integer spin nuclear isotopes in natural silicon has a beneficial effect on the coherence time of the spin qubits hosted in Si, which is even further enhanced by hosting the qubits in isotopically-enriched 28-Si.

and have shown the ability to extend coherence times by several orders of magnitude [12]. Compared to silicon quantum dot spin qubits, coherence times of spin qubits in GaAs quantum dots are limited and therefore less suitable as a material platform for a quantum information processor, especially when also considering the advantages that come with the integration of Si devices in the existing semiconductor industry. Nonetheless, the relative simplicity in fabrication and the extensive knowledge of GaAs QD systems allows for the fabrication of complex QD architecture allowing to engineer two-dimensional QD arrays and complex gate electrode layouts that provide precise control of the physical parameters in the system. These aspects make the material an excellent platform for, among other applications, quantum simulation or testing machine-learning automation schemes.

1.1 Thesis structure

The focus of this work is the exploration of two-dimensional semiconductor quantum dot arrays in a GaAs/AlGaAs heterostructure and a foundry-fabricated silicon-on-insulator device by exploiting state-of-the-art pulsed gate techniques.

Chapter 2 provides a short introduction to semiconductor quantum dot systems, focusing on providing a basic understanding of electrostatics and electron transport in QD systems. In addition, spin-based qubit encodings and their initialization, readout, and manipulation schemes in quantum dot system are introduced with a clear focus on a $S - T_0$ -qubit.

The experimental apparatus and relevant methods for a fundamental understanding of the results presented in Chapter 4-6 are presented in Chapter 3. The nanostructures of the two devices under study: a fully-depleted silicon-on-insulator 2x2 QD device and a GaAs/AlGaAs heterostructure device are introduced in Sec. 3.1 and 3.4 respectively. A short introduction of the employed charge readout methods based on RF reflectometry is introduced in 3.2, while details of the readout in the two setups are presented in Sec. 3.3 and Sec. 3.5. Electrostatic control of the QD potential landscapes are discussed in Sec. 3.1.2 and 3.4.1. The employed methods and calibration for applying high-frequency electrical control sequences to the gate electrodes are introduced in Sec. 3.6.

In Chapter 4, a $S - T_0$ qubit is realized in a DQD within a GaAs/AlGaAs heterostructure QD device, focusing on the operation of coherent exchange oscillations.

In Chapter 5, pulsed gate experiments are performed on a DQD in a fully-depleted silicon-on-insulator quadruple QD device, exploring the complex level structure present in SOI devices by performing pulsed gate spectroscopy.

In Chapter 6, a new RF gate-based readout method is presented, exploiting a DQD as an RF charge sensor in a two-dimensional Si QD array.

Chapter 7 provides a summary and outlook based on the results of the experiments presented in Chapters 4-6.

Introduction to spin qubits in gate-defined quantum dot systems

2.1 Introduction to quantum dots

Quantum dots are (quasi)-zero-dimensional nanostructures that can trap charge carriers in an artificially-created confinement potential.

A charge carrier trapped in a QD will occupy a discrete electronic level. The electronic level structure in a QD is dominated by two effects: the electrostatic Coulomb interaction between electrons and the non-interacting discrete single-particle energies in the QD as a result of the three-dimensional confinement potential [14]. The Coulomb interaction between electrons results in a charging energy E_C that has to be overcome when an additional electron is added to the QD, whereas the discrete level spacing results in an additional energy contribution (ΔE) that is required to populate the next single-particle level when an electron is added when the lower electronic shells are filled. The addition energy E_{add} is expressed as the sum of both dominant energy contributions: $E_{\text{add}} = E_C + \Delta E_i$.

In practice, the three-dimensional confinement required for the formation of quantum dots can be realized by a variety of experimental platforms, generally using a combination of smart engineered nanostructures that provide spatial confinement in one, two, or three dimensions and electrostatic confinement to ensure confinement in the remaining (if any) direction(s). Experimental platforms used for quantum dot devices include carbon nanotubes, self-assembled nanocrystals, and electrostatically-defined semiconductor QDs.

In this work, we explore electrostatically-defined semiconductor QD systems. Fig. 2.2 shows commonly-used QD systems that use an electrostatically-defined confinement potential to define the QDs in the system.

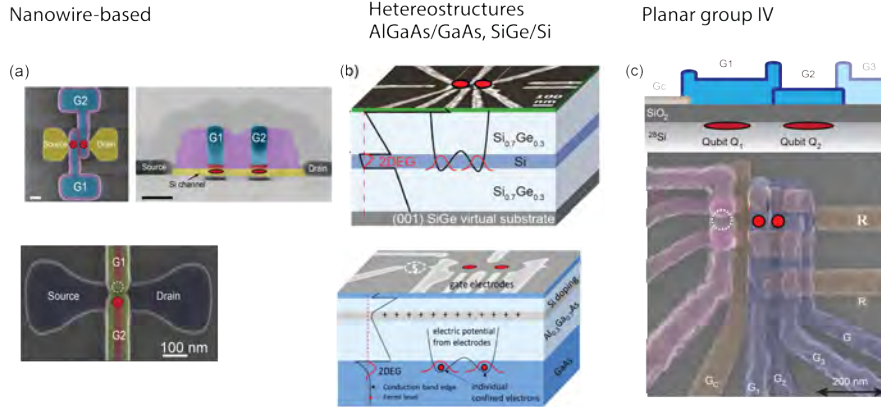


Figure 2.1: **Common-used nanostructures for electrostatically-defined quantum dot devices:** Quantum dots are schematically indicated in red, charge sensor dots indicated in white (dashed). From left to right: Nanowire-based QD devices - quantum dots are formed by electrostatic confinement in a nanowire channel. The channel provides two-dimensional confinement, while the electrostatic potential as a result of the voltages exerted on the lithographically-patterned gate electrodes (G1,G2) defines the confinement potential in the remaining direction. (a) Common-used accumulation-mode SOI nanowire-based geometries include pumping geometries (top) [1], split-gate geometries (bottom) [15] and side gate geometries. (b) Semiconductor heterostructures. A SiGe/Si heterostructure (top) [16], QD's are formed in the 2DEG by using lithographically-patterned gate electrodes that define the QD potential. AlGaAs/GaAs heterostructure (bottom) [17] (c) Planar group-IV gate-defined quantum dot devices. Confinement is provided is by electrostatic gating [18]

2.2 Charge transport in quantum dot systems

2.2.1 The constant interaction model

A simple, but effective description of the quantized charge states in a quantum dot system is based on considering the quantum dot as a conducting island that can be described with a constant capacitance C (independent of the number of electrons residing on the QD itself). The electrostatics of the resulting capacitive circuit describing the QD system gives a purely classical model, but is remarkably successful in providing an understanding of basic charge properties in QD systems [14].

The constant interaction model (CIM) is based on two assumptions [14]: First, the Coulomb interaction can be parameterized with a constant capacitance, and second the single-particle energies are assumed to be independent of the Coulomb interaction and other interactions in the system.

We consider a single QD that is tunnel-coupled to a source and drain reservoir, allowing for the exchange of electrons between the QD and the left(drain) and right(source) reservoirs. The quantum dot is modeled as a conducting island with a capacitance C

that can be charged/discharged by exchanging electrons with left and right electron reservoirs (Fig. 2.2). In this picture, the total capacitance on the quantum dot is given by the sum of the capacitances connected to the dot: $C = C_S + C_D + C_G$, where $C_S(C_D)$ is the capacitance between the QD and the source(drain) reservoir and C_G is the capacitance between the QD and the gate.

The total electrostatic energy stored by the single-dot system in the CI approximation is given by

$$U(N, V_G, V_S, V_D) = \frac{1}{2C}[-|e|(N - N_0) + C_S V_S + C_D V_D + C_G V_G]^2, \quad (2.1)$$

where V_G, V_D, V_S are the voltages on the gate and drain and source contacts respectively. $Q_0 = |e|N_0$ is the offset or background charge, with N_0 the number of electrons residing on the dot when $V_G = V_S = V_D = 0$

The electrochemical potential of the QD, given an occupation of N electrons, is given by

$$\mu(N) = U(N) - U(N - 1) = \frac{|e^2|}{C}(N - N_0 - \frac{1}{2}) - \frac{|e|}{C}(C_S V_S + C_D V_D + C_G V_G). \quad (2.2)$$

Self-evidently, adding the N th electron to a QD occupied by $N - 1$ electrons will then cost an energy¹

$$\mu(N) - \mu(N - 1) = \frac{|e^2|}{C} = E_C. \quad (2.3)$$

A change in voltage V_G on the capacitively-coupled gate electrode, will result in a shift of the electrochemical potential level of the dot μ_N . Consequently, this changes the relative electrochemical potential levels of the QD with respect to the source (μ_S) and drain (μ_D) reservoirs. This is at the core of control of the fixed number of electrons residing on the dot when operating the system in the Coulomb blockade regime, via exchange of charges with the source and drain electron reservoirs and can be used to load/unload electrons on the QD.

¹Here the discrete single-particle energies in the QD are not taken into account, which results in an additional contribution of ΔE_i whenever all lower-lying electronic shells are filled

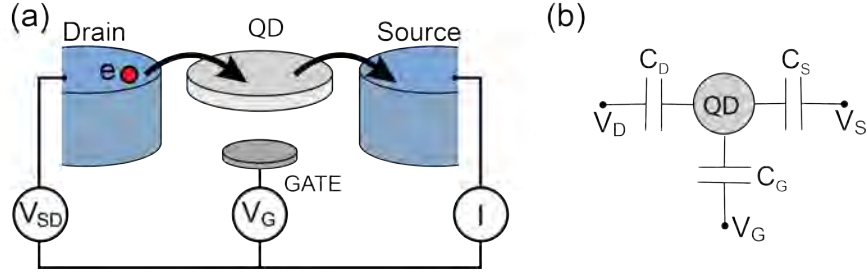


Figure 2.2: **Capacitive model of a single-quantum dot connected to source and drain reservoirs** (a) The quantum dot is modelled as a conducting island that is capacitively coupled to a gate and tunnel coupled to a electron reservoir on either side of the dot. The island can be charged/discharged by exchanging electrons with the reservoirs. (b) Purely capacitive model, where the quantum dot is modelled with a total capacitance C and is capacitively coupled to source ($C = C_S$), drain ($C = C_D$) and gate ($C = C_G$)

2.3 A double quantum dot

By adding a QD to the system with a mutual capacitive coupling C_m between the two dots, a double quantum dot system is formed, where we consider the left(right) QD to be tunnel coupled to the drain(source) electron reservoir. In the CI approximation, the total electrostatic energy stored in the double quantum dot (DQD) system is expressed as [19]

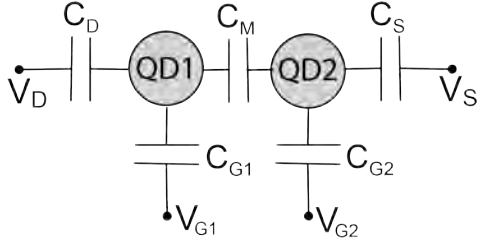


Figure 2.3: **Capacitive circuit of a double quantum dot system** - QD₁ and QD₂ have a mutual capacitive coupling C_m . Each of the dots is capacitively coupled to a gate electrode. QD₁ is tunnel coupled to the drain contact and QD₂ to a source contact, here solely modelled with a capacitance, but often a resistive element is added.

$$U(N_1, N_2, V_1, V_2, V_L, V_R) = \frac{1}{2}N_1^2 E_{C1} + \frac{1}{2}N_2^2 E_{C2} + N_1 N_2 E_{Cm} + f(V_1, V_2) \quad (2.4)$$

$$, \text{ with } f(V_1, V_2) = \frac{1}{-|e|} (C_{g1} V_1 (N_1 E_{C1} (N_1 E_{Cm}) (C_{g2} V_2 (N_1 E_{Cm} (N_2 E_{C2}) + \frac{1}{e^2} \frac{1}{2} C_{g1}^2 V_{g1}^2 E_{C1} +$$

$\frac{1}{2}C_{g2}^2V_{g2}^2E_{C2} + C_{g1}^2V_{g1}C_{g2}^2V_{g2}E_{Cm}$, the charging energy of QD₁ $E_{C1} = e^2 \frac{C_2}{C_1C_2 - C_m^2}$, the charging energy of QD₂ $E_{C2} = e^2 \frac{C_1}{C_1C_2 - C_m^2}$ and the mutual charging energy $E_{Cm} = e^2 \frac{C_m}{C_1C_2 - C_m^2}$.

Upon changing the voltages V_1, V_2 on the capacitively coupled gate electrodes, charge is induced on the dots or charge is exchanged between the two dots due to the mutual capacitive coupling. The charge ground states can be determined by finding the lowest energy state for a given set of voltages V_1, V_2 . As a function of the voltages on the gates, the charge ground states reveal a charge stability diagram that reveals a characteristic honeycomb pattern in the case of $C_m > 0$.

2.3.1 Characteristics of a DQD system

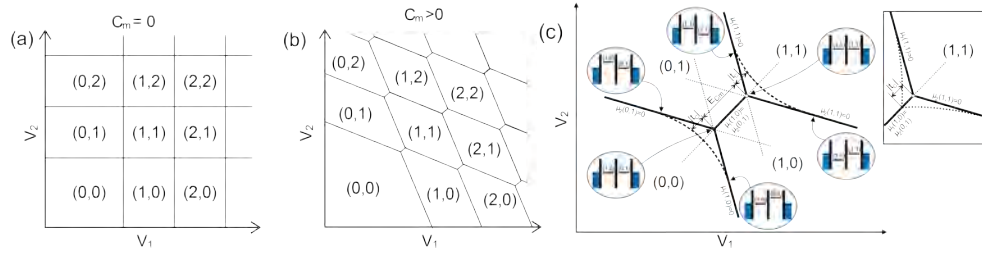


Figure 2.4: **(a)** Charge ground states of a DQD system as a function of the voltages on V_1 and V_2 (a charge stability map) in the absence of a mutual capacitance. Figure adapted from [19]. **(b)** Charge stability map in the presence of a mutual capacitance C_m . **(c)** Transport through a DQD in the absence of a source-drain bias V_{SD} . In the presence of a tunnel coupling t_c , the charge states hybridize, resulting in a curvature of the charge ground states that is proportional to t_c . Figure adapted from [14]

In the absence of a source-drain bias, transport through the DQD is only possible when the QD levels of the left/right dot align with the drain/source reservoir. In voltage gate space, this occurs at the so-called triple points, indicated in Fig. ???. When a source-drain bias is applied, single-electron transport in the DQD the triple points in triangular regions, known as bias triangles within which single-electron transport through the DQD occurs.

2.3.2 Constant Interaction Model of a system with N nodes

The CI model can be extended to larger dot systems by describing the electrostatics of a capacitive circuit consisting of N nodes. The capacitances between each node to each other node in the system as well as the capacitances between each node to ground make up the $N(N+1)/2$ capacitances in the resulting capacitive circuit. The total electrostatic energy stored on the $N(N+1)/2$ capacitances in the system can be expressed in a convenient matrix formulation [19]:

$$U = \frac{1}{2} \vec{V} \hat{\mathbf{C}} \cdot \vec{V} \quad (2.5)$$

, where \mathbf{C} is the capacitance matrix, where the diagonal elements are given by the total capacitance on node i : $c_{ii} = \sum_{j=0,j \neq i} c_{ij}$ and off-diagonal elements are given by $C_{ij} = C_{ji} = -c_{ij}$.

In a QD system, the nodes in the capacitive circuit represent a QD or a voltage source. Since the voltages on the voltage sources are known, it is convenient as a block matrices consisting of submatrices that describe the capacitances between voltage nodes and capacitors between the capacitors and between voltage nodes ($\hat{\mathbf{C}}_{\text{cv}}$, $\hat{\mathbf{C}}_{\text{cc}}$ and $\hat{\mathbf{C}}_{\text{vv}}$).

$$\begin{pmatrix} \vec{Q}_c \\ \vec{Q}_v \end{pmatrix} = \begin{pmatrix} \hat{\mathbf{C}}_{\text{cc}} & \hat{\mathbf{C}}_{\text{cv}} \\ \hat{\mathbf{C}}_{\text{vc}} & \hat{\mathbf{C}}_{\text{vv}} \end{pmatrix} \begin{pmatrix} \vec{V}_c \\ \vec{V}_v \end{pmatrix}, \quad (2.6)$$

where $\vec{Q}_c(\vec{V}_c)$ represents the charges(voltages) on the capacitors and $Q_v(V_v)$ the charges(voltages) on the voltage nodes.

2.4 Spin-based qubit encodings in QD systems

There exist several spin-based qubit encodings in gate-defined quantum dot systems, including (but not limited to) a Loss-Divenchenzo (single-spin) qubit, a singlet-triplet qubit hosted in a DQD, an exchange-only qubit and a charge-spin hybrid qubit [12]. Any physical qubit realization needs to meet key criteria to be considered suitable for quantum information purposes [20], which include initialization in a fiducial state, long coherence times (typically longer than computation times), the ability to perform high-fidelity single-qubit and two-qubit operations (which requires an interaction between the qubits resulting in an entanglement of the qubit's states) and a qubit-specific, high-fidelity readout capability,

2.4.1 A two-level QM system as a quantum information processing entity

A well-defined two-level quantum-mechanical system can be used to encode a qubit. The computational basis is then spanned by the eigenstates of the system and is encoded in $|0\rangle$ and $|1\rangle$.

Any quantum mechanical state of the system can then be expressed as a linear combination of the basis states $|0\rangle$ and $|1\rangle$ as $\psi = \alpha_1 |0\rangle + \alpha_2 |1\rangle$. The normalization of quantum states requires that $|\alpha_1|^2 + |\alpha_2|^2 = 1$. The qubit's state can be expressed as: $\psi = \cos \frac{\theta}{2} |0\rangle + \exp(i\phi) \sin \frac{\theta}{2} |1\rangle$. The qubit's (pure) states can therefore be represented as a unit vector in a two-dimensional complex space, commonly geometrically represented as a complex vector in a unit sphere, known as the Bloch sphere.

Figure 2.5: Geometrical representation of a qubit's state in a Bloch sphere

2.4.2 The Loss-Divichenzo qubit

The electron spin state of a single excess electron confined in a quantum dot can be used as a qubit encoding by encoding the electron's spin state in the computational basis $|0\rangle = |\uparrow\rangle, |1\rangle = |\downarrow\rangle$. In the presence of a static magnetic field B_z , the energy levels of $|\uparrow\rangle$ and $|\downarrow\rangle$ are split by the Zeeman energy $E_z = g\mu_B B_z$, where g is the electron g -factor and μ_B is the Bohr magneton.

This difference in energy for the $|\downarrow\rangle$ and $|\uparrow\rangle$ states at finite magnetic field allows for readout of the spin state by spin-to-charge conversion. This is achieved by energy-selective readout or tunnel-rate-selective readout. In energy-selective readout, commonly referred to Elzermann readout, the electrochemical potential of the electron reservoir is precisely tuned in between the energy-split spin-up and spin-down levels $\mu_\downarrow < \mu_D < \mu_\uparrow$. This then allows an electron in the spin-up state to tunnel from the dot to the reservoir, while a spin-down electron will be blocked. The spin state is inferred from the presence/absence of the charge tunneling event.

Initialization of a spin-down state² can be easily achieved in a similar way, where now tunneling from the reservoir to the spin-down state is energetically allowed, while the spin-up state is energetically inaccessible. Alternatively, an electron in a random state (either spin-up or spin-down) can be loaded and is initialized by interleaving the qubit's state for a time longer than the spin relaxation time to the ground state ($t_{\text{wait}} > T_1$).

The spin state can be controlled and manipulated by applying a local oscillatory in-plane magnetic field ($B = B_1 \cos(\omega_0 t)$). The field couples to the electron spin by the Zeeman effect, which allows for fast coherent control over the spin state. This can then be used to induce single-qubit rotations of the spin's state. For the realization of two-qubit operations, the respective spin states of the two qubits have to be entangled. This entanglement is often realized by exploiting the Heisenberg exchange interaction in the system. The interaction can either be direct or indirect (via for example the interaction with another spin state or via a spin bath (bus)).

2.4.3 Singlet-triplet qubit

The two-electron spin state of two electrons hosted in a DQD can be used to encode a qubit in the $S_z = 0$ subspace. The $|S\rangle$ - $|T_0\rangle$ -states and $|\downarrow\uparrow\rangle$ $|\uparrow\downarrow\rangle$ -states span a computational basis and are used to encode the qubit's state.

A singlet-triplet qubit is encoded in the $|S\rangle, |T_0\rangle$ -basis. The energy splitting between the two states is set by the exchange interaction strength J .

Initialization of the S – T₀ qubit is achieved by energy relaxation to the system's ground state by interleaving the qubit for a wait time longer than the energy relaxation T_1 .

Readout of the two-electron spin state of the system relies on Pauli spin blockade.

²For positive(negative) values of the g -factor, the $|\downarrow\rangle$ ($|\uparrow\rangle$)-state is the lower energy state

By projecting the (1,1) state onto the (0,2) or (2,0) state, the presence(absence) of a tunneling event implies the state being in a triplet state (singlet state), since the triplet states will be blocked due to Pauli spin blockade³. Readout is performed by projection onto (2,0)/(0,2) state by diabatically traversing the inter-dot transition.

The system's Hamiltonian in the qubit's basis $\{|S\rangle, |T_0\rangle\}$ is given by

$$\hat{\mathcal{H}} = \frac{J(\epsilon)}{2}\hat{\sigma}_z + \frac{\Delta B_{||}}{2}\hat{\sigma}_x, \quad (2.7)$$

where J is the exchange energy splitting between the $|S\rangle$ - and $|T_0\rangle$ -state, $\Delta B_{||}$ is a magnetic field gradient between the two dots and $\hat{\sigma}_x$ and $\hat{\sigma}_z$ are the Pauli spin matrices.

The unitary time evolution of the qubit's state $\phi(t)$ under the influence of the Hamiltonian given by Eq. 2.7 is given by

$$|\phi(t)\rangle = e^{-\frac{i\hat{\mathcal{H}}t}{\hbar}}\phi(0) = \hat{U}(t)\phi(0) \quad (2.8)$$

, where \hbar is the reduced Planck constant. $\hat{U}(t) \equiv e^{-\frac{i\hat{\mathcal{H}}t}{\hbar}}$ is an unitary time evolution operator. The evolution of the qubit's state under the influence of Eq. 2.7 translates into the precession of the qubit's state around a quantization axis defined by J and $\Delta B_{||}$.

If J dominates, the qubit will rotate around the quantization axis defined by the J , indicated in green in Figure 2.6 in the Bloch sphere.

The exchange interaction strength can be altered in-situ owing to its dependence on the double-dot detuning ϵ as $J = J(\epsilon)$. Experimentally, the exchange interaction can be altered by changing the voltages along a virtual detuning voltage parameter, that directly relates to the double detuning by its lever arm.

Rotation of the $S - T_0$ qubit is addressed experimentally by fast voltage control that alters the voltages along a detuning axis. The experimental implementation is discussed in more detail in Chapter 4, in which a $S - T_0$ qubit in a GaAs DQD is presented.

³Essential to note here, is that we here only consider the two-lower lying energy levels and that any excited state level spacing (higher-lying orbital-, valley-, or valley-orbit states) is greater than the Zeeman splitting, $\Delta E_i > E_z$.

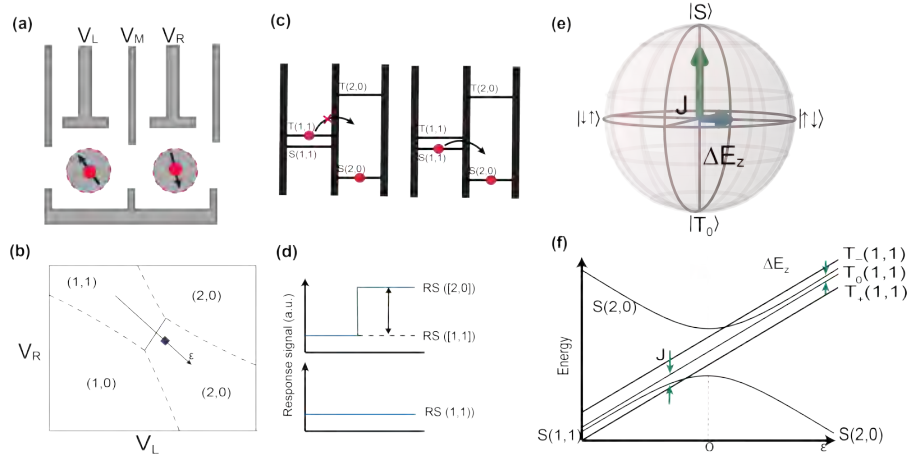


Figure 2.6: **Singlet-triplet qubit** (a) A singlet-triplet qubit is encoded in the spin state of two electrons hosted in a DQD system (b)-(c) Readout of a singlet-triplet qubit is achieved through projection of the $(1,1)$ spin state onto the $(2,0)$ spin state and relies on Pauli spin blockade of the polarized $T(1,1)$ state. (e) Bloch sphere representation of a $S - T_0$ qubit, illustrating the two quantization axes defined by J and ΔE_z respectively. (d) Schematic illustration of the two-electron spin spectrum of a DQD near the $(1,1)$ - $(2,0)$ transition.

Experimental methods

A standard experimental setup for the operation of semiconductor spin qubit devices has three key requirements. First, the device needs to be cooled to cryogenic temperatures, typically operating at temperatures below $T < 100\text{mK}$ ¹ in a dilution refrigerator.

Second, electrical control of the potential defining the QD system is required, thereby enabling control of physical parameters characterizing the QD system (e.g. μ_i, t_i). High-precision voltage control is generally provided by room-temperature equipment that is interconnected to the device's gate electrodes via low- and high-frequency lines in the cryostat. Focusing on the manipulation of a singlet-triplet qubit, high-frequency voltage pulses allow for manipulation of the qubit's state by rapid electrical control sequences [22]. The experimental setup and methods for low- and high-frequency voltage control are introduced in Sec. 3.1.2 and 3.4.1.

Lastly, readout of the charge and (electron) spin states is required. Here, we employ RF readout techniques for the experiments presented in Chapters 4-6. A general introduction to RF charge readout methods in quantum dot devices is presented in Sec. 3.5, focusing on gate-based dispersive readout methods and RF-SQD based readout.

In this work, experiments are performed on two devices: a foundry-fabricated fully-depleted SOI device (Sec. 3.1) and a GaAs/AlGaAs device (Sec. 3.4).

We employ a gate-based RF readout technique for readout of the four QD charge states in the FDSOI quadruple dot device and an RF-SET ohmic-based reflectometry technique. A general introduction to RF reflectometry is discussed in Sec. 3.2. The

¹Higher temperature ($T > 1\text{K}$) operation of spin qubits in silicon devices have been successfully demonstrated by several groups [10][21].

specifics of the readout setup and methods in the FDSOI device and GaAs device are discussed in Sec. 3.3 and Sec. 3.5 respectively.

3.1 A fully-depleted silicon-on-insulator 2x2 quantum dot array

3.1.1 Device nanostructure

The device under study is a foundry-fabricated fully-depleted silicon-on-insulator (FDSOI) device with a double split-gate geometry. The device is fabricated by LETI in Grenoble, using a top-down fabrication process on a 300mm silicon-on-insulator wafer [23][24]. Details on the fabrication process can be found in [24].

A scanning electron micrograph (SEM) image of a device similar to the one studied (Fig. 3.1) illustrates its nanostructure, consisting of a 7nm undoped silicon channel with n^+ -doped regions acting as source and drain electron reservoirs (dark grey). Two pairs of split-gates ($L_G=32\text{nm}$) partially overlap the channel and are used to induce four quantum dots in a 2x2 arrangement. The gate material stack consists of 50nm poly-Si and a 5-nm-thick TiN layer. The gates are separated from the Si channel by a thin insulating SiO_2 layer. SiN spacers are added to separate the gates as well as the gates and the doped source and drain region from each other [23]. Additionally, a metal line is situated 300nm above the nanowire channel (not illustrated), acting as an overall top gate.

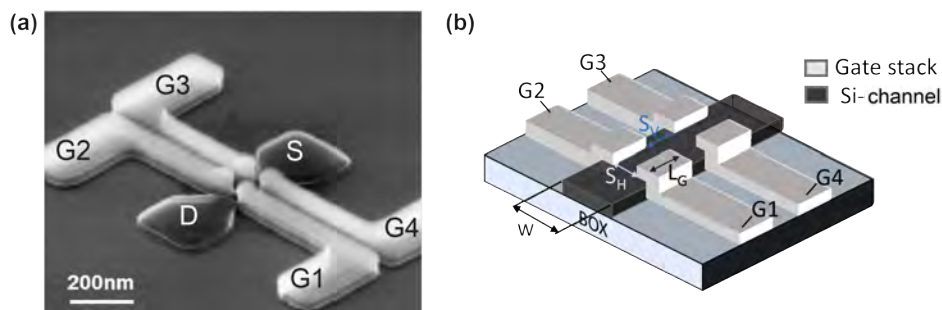


Figure 3.1: **Fully-depleted SOI QD device architecture** - (a) SEM image of a silicon split-gate device [23] similar to the device under study, (b) Simplified schematic illustration of the device layout with dimensions $W=70\text{nm}$, $L=32\text{nm}$, $S_H = 32\text{nm}$, $S_V = 32\text{nm}$.

3.1.2 Electrostatic control in a silicon 2x2 array

By changing the voltages exerted on the gates $G_1 - G_4$, electrons can be accumulated underneath each of the gates $G_1 - G_4$. Four quantum dots can be formed, constituting a quadruple dot system in a 2x2 arrangement when all QDs are activated.

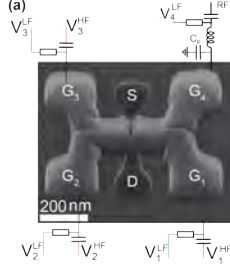


Figure 3.2: **Simplified schematic of electrostatic control of the Si quadruple dot system** - A tilted SEM of a device similar to the one under study, shows the Si channel with embedded source (S) and drain (D) reservoir. The gates G1-G3 are connected via on-chip bias tees to low-frequency and high-frequency lines, while G4 is wire bonded to an inductor L and connected via a bias tee to a low-frequency line and the coaxial transmission line used in RF readout. Details on filtering and attenuation on the low- and high-frequency are omitted here and can be found in Appendix A.

The electrochemical potential of the individual dots, μ_i , is altered and controlled with the voltages V_i exerted on the gates. In addition, the cross-capacitive coupling between the gate-dot (given by the off-diagonal elements of the dot-gate capacitive matrix: $C_{ij}^{cv} = C_{ji}^{cv} = -c_{ij}^{cv}$, $i \neq j$) induces a change in the electrochemical potential of the dots upon changing the voltages on the other gates. Similarly, the cross-capacitance between the dots (given by the off-diagonal elements of the capacitive matrix C_{cc}) results in a change in electrochemical potential upon changes in the number of electrons (N_j) in the other dots.

The dot-gate capacitances have been measured and reported in previous work on the device, yielding the following dot-gate capacitance matrix (elements expressed in attofarads) [25]:

$$\hat{C}^{cv} = \begin{pmatrix} 2.14 & 0.33 & 0.25 & 0.73 \\ 0.3 & 1.69 & 0.22 & 0.17 \\ 0.32 & 0.6 & 1.41 & 0.26 \\ 0.79 & 0.34 & 0.47 & 2.00 \end{pmatrix} \quad (3.1)$$

The metal line situated 300nm above the nanowire channel adds control of the overall tunnel couplings between the dots in the array ($t_{||}$ between parallel dots and t_{\perp} between opposing dots) [23].

While overall control of the tunnel couplings in the array is achieved in this manner, it is fair to note that the absence of barrier gate electrodes makes the precise tuning of the individual tunnel couplings between each pair of dots unattainable.

Additionally, the tunnel coupling is altered by the number of electrons in the respective dots.

Source and drain contacts are connected to low-frequency voltage control lines and can be used to apply a source-drain bias for the purpose of DC transport measurements. The presented experiments rely on RF reflectometry readout techniques and source and drain contacts are grounded in the experiments.

3.2 Introduction to RF reflectometry readout techniques

RF reflectometry has been harnessed as a high-sensitive, fast charge detection readout technique across several qubit platforms [13]. The concept of RF readout techniques relies on inferring the charge state from the RF signal reflected from an LC circuit loaded with a variable impedance that depends on the QD state. This is achieved by embedding a high-sensitive charge sensor (e.g. a QPC, SET) in the LC resonator circuit or by directly embedding the gate of a QD. The latter method, referred to as gate-based dispersive readout, has two main advantages. First, it yields an increased measurement accuracy [13] and second it drops the requirement of a separate in-proximity-placed charge detector, thereby simplifying the overall QD device architecture. We employ a gate-based dispersive readout method for the experiments performed on the 2x2 silicon device. The basic concepts of RF reflectometry techniques are introduced below, while the specifics of gate-based dispersive readout methods employed for charge readout of the silicon quadruple dot system are discussed in Sec. 3.4.

The amplitude and phase of the reflected signal will strongly depend on the variable complex impedance of the QD. The QD acts in this case as a variable impedance for the resonator. Upon encountering a change in impedance, the RF signal will be reflected with a (complex) reflection coefficient of

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \quad (3.2)$$

, where $Z_0 = 50$ is the impedance of the coaxial transmission line. Z is the QD-state dependent complex impedance of the resonance circuit. For perfect matching $Z = Z_0$, the reflected coefficient is at its minimum. If Z differs significantly from Z_0 , the method becomes insensitive to the loaded QD impedance. The sensitivity of the readout method is maximized if Z is near Z_0 such that a small change in QD impedance results in a large change in RF reflected signal.

Embedding the gate of a quantum dot in a resonant LC circuit in RF-based readout techniques allows for probing the parametric capacitance of the QD system.

For a single QD, the capacitance as seen by the gate has two contributions: a (fixed) geometrical capacitance C_{geom} and a variable tunneling capacitance C_t . The tunneling capacitance results from the single-electron tunneling between the QD and the

lead and is expressed as [26]:

$$C_t = -|e|\alpha \frac{\partial P_1}{\partial V_g} \quad (3.3)$$

, where α is the lever arm, $|e|$ the electron charge, and P_1 the probability of having an excess charge on the QD.

The tunneling capacitance can be probed by applying an RF tone with a frequency f_{drive} on the gate, the AC signal on the gate will result in a modulation of the difference in electrochemical potential levels of the dot and lead, given by the detuning ϵ : $\epsilon = \epsilon_0 + \delta\epsilon \sin(2\pi f_{\text{drive}}t)$. For $f_{\text{drive}} \ll \Gamma$, this then drives the resonant tunneling of an electron between the QD and the lead. This induces a change in the tunneling capacitance C_t , which results in a shift of the resonance frequency of the LC resonator. The change in resonance frequency can be detected by using standard homodyne detection techniques, which rely on intermixing the incoming RF (reference) signal with the reflected signal to detect changes in phase and amplitude of the reflected RF signal.

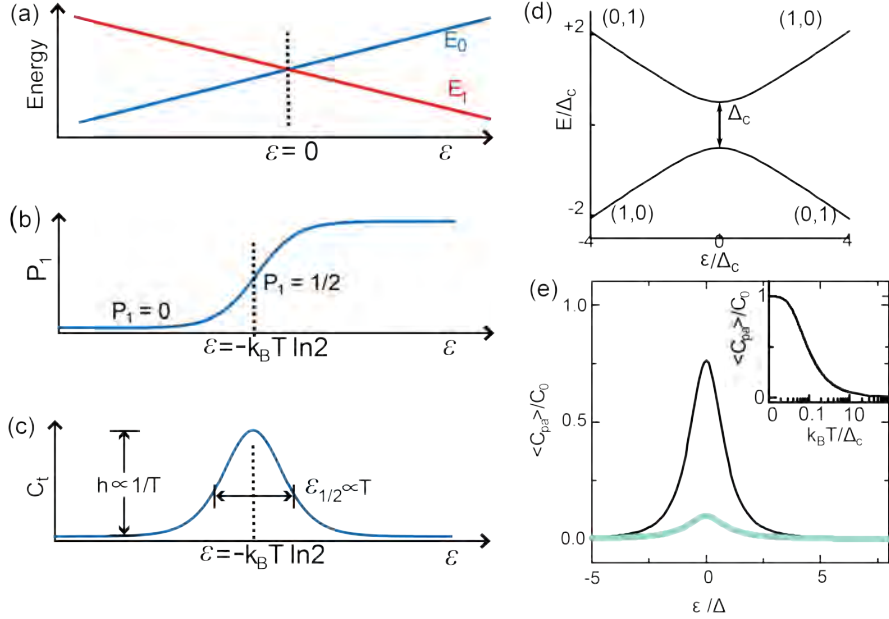


Figure 3.3: **Principles of gate-based dispersive readout by probing the state-dependent tunneling and quantum capacitance in a single-dot lead and double dot system:** Figures adapted from [27]((a)-(c)) [26]((d)-(e))

A tunnel-coupled DQD system occupied by a single electron charge forms a two-level system with eigenenergies $E_{\pm} = \pm\sqrt{\epsilon^2 + 2t^2}$.

The capacitance as seen by the gate [26] has two contributions: a geometrical capacitance and a quantum capacitance C_q . The quantum capacitance is a function of the band structure and polarizability of the DQD charge state [28]:

$$C_q = -(\alpha e)^2 \frac{d^2 E}{d\epsilon^2} \quad (3.4)$$

, where α is the lever arm, e the electron charge, and $\frac{d^2 E}{d\epsilon^2}$ the second derivative of the density of states.

A change in C_q results in a shift in the resonance frequency f_c . This shift can be detected using homodyne detection techniques [28].

3.3 Gate-based dispersive RF readout methods and setup quadruple dot silicon device

Gate-based RF readout is achieved by embedding the gate of one of the four dots (G_4) in an LC circuit. This is achieved by wire-bonding the gate to a surface-mount inductor ($L=820\text{nH}$). The inductor together with the downstream capacitance to ground then forms the LC circuit (Fig. 3.4). The resonance frequency can be extracted by measuring the transmission (S_{21}) between two ports of a Vector Network Analyzer (Fig. 3.4(c)) of which port 1 is connected to the RF input at the cryostat (Rx) which via an attenuated coaxial line reaches the device (Fig. 3.4) and port 2 is connected to the RF signal output signal at the cryostat (Tx). The measured transmission S_{21} then gives a measure of the reflection coefficient Γ , which is at its minimum if matching condition is achieved, $|\Gamma| = \Gamma_{\min}$ ($\Gamma_{\min} = 0$ if perfect matching is achieved).

The extracted resonance frequency f_0 is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{\text{tot}}}} \approx 191.2\text{MHz} \quad (3.5)$$

, yielding a total capacitance to ground of $C_{\text{tot}} = 0.84\text{pF}$.

The experiments are operated at a drive frequency near the resonance frequency. Thereby, the RF readout is operated near matching condition, where reflection is minimum. Here, the reflected signal is highly sensitive to any changes in the QD impedance loaded on the LC circuit.

Changes of the reflected RF carrier signal are measured by using standard homodyne detection techniques by intermixing the incoming RF (reference) signal with the reflected signal to detect changes in phase and amplitude in the reflected signal, yielding a demodulated DC voltage V_H . A schematic of the homodyne detection circuit is illustrated in Fig. 3.4.

The charge state of the other dots ($\text{QD}_1, \text{QD}_2, \text{QD}_3$) can be inferred from the sensor dot's state. This is achieved by exploiting the capacitive shift that the sensor dot

peak undergoes whenever an electron is loaded on of the other dots in the array. As long as the shift is larger than the Full Width Half Maximum of the sensor dot signal, the shift can be detected and used to infer charging events on the other dots. The number of electrons in each of the QDs in the system is determined by emptying the dots up to the last electron.

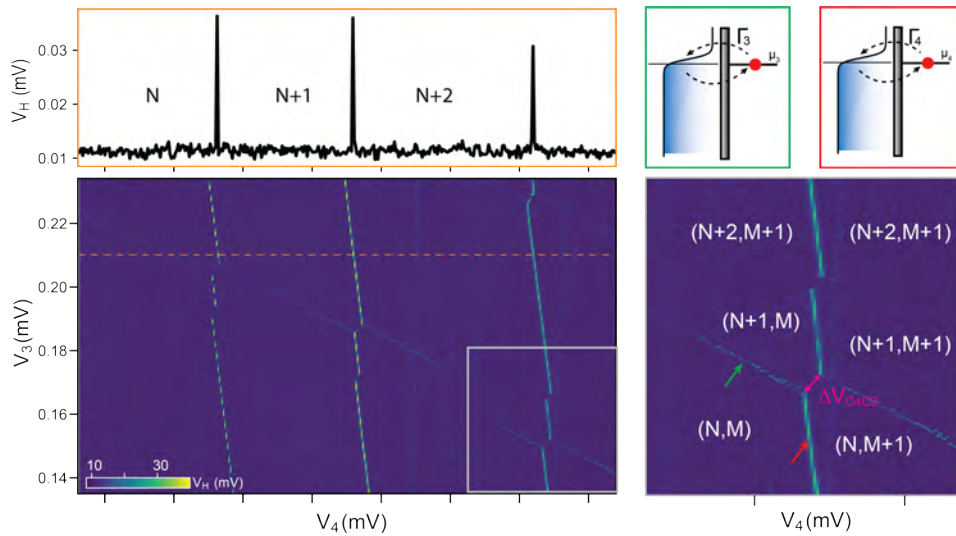


Figure 3.5: **Principles of RF charge sensing in the quadruple dot system** The Coulomb peaks of QD₄ (see line trace) are used as the sensing signal. A capacitive shift of the sensor dot peak $\Delta V_{C_3C_4}$ is the result of the loading(unloading) of an electron on the other dots in the array. If $\Gamma_i \gg f_{\text{drive}}$ the dispersive signal as a result of the resonant between QD_i and the leads gives a measurable dispersive RF response signal (indicated by the green arrow) for the QD₃ charging line.

We note that the dispersive readout technique requires high tunnel rates Γ between the sensor quantum dot (QD₄) and the lead. Experimentally, this is realized by occupying the sensor dot with multiple electrons (in this device, typically 5-8 electrons)

3.4 A two-dimensional GaAs four DQD array

Device architecture

A GaAs/AlGaAs heterostructure is used to trap electrons in a 2DEG (depth 59nm) [29]. Quantum dots are depleted in the 2DEG using the plunger gates of the DQD (indicated in red) and a SQD (indicated in white). The details on electrostatic control of the DQD and SQD potential well by using the gate electrodes are discussed in Sec. 3.4.1.

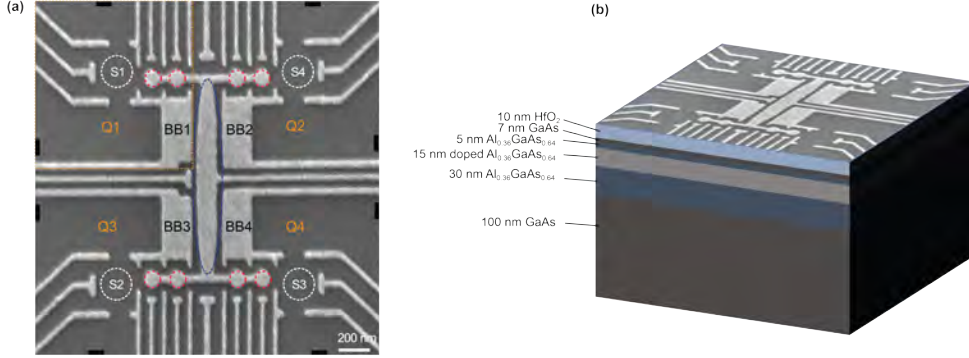


Figure 3.6: **GaAs device structure** (a) SEM of a GaAs device similar to the device studied, four double dots can be formed, one in each of the quadrants Q1-Q4. For readout purposes a nearby sensor dot is formed in proximity of the double dot (S1-S4). The large accumulation dot (white-dashed) can be used to couple the non-neighboring DQDs. **fedele**. (b) Schematic of the GaAs/AlGaAs heterostructure.

Apart from the larger accumulation dot (indicated by the white dashed lines in Fig. 3.6) and its gates, the gate layout of the device is top-down and left-right symmetric. Each of the four quadrants (Q1-Q4) contains nine gate electrodes and two ohmic contacts of which one is connected to a surface-mount inductor used to employ an SQD ohmic-based RF readout method. The other ohmics can be used as either source or drain contacts in transport measurements between any pair of ohmics in the device. The backbone gate electrodes (labeled BB in Fig. 3.6) can isolate the four quadrants by pinching off the 2DEG.

3.4.1 Electrostatic control in a two-dimensional GaAs array

Here we discuss the electrostatic control of the DQD and SQD potentials using the gate electrodes in one quadrant of the device. In each of the quadrants, a larger quantum dot and a double quantum dot can be formed. The larger quantum dot is used as a charge sensor and is electrostatically confined by its barrier gate electrodes (V_{RB}^{SQD} and V_{LB}^{SQD}). Electrons are loaded on the SQD by shifting the electrochemical potential ladder of the dot μ_{SQD} with respect to the lead by sweeping the voltage on the plunger gate V_{PL}^{SQD} .

A DQD can be induced in the proximity of the SQD using the plunger gates V_L and V_R . The electrostatic potential landscape of the DQD can be altered and controlled by the outer barrier gates (V_{LB}^{DQD} and V_{RB}^{DQD}), the plunger gates for the left (V_{LP}^{DQD}) and right QDs (V_{RP}^{DQD}) and a middle barrier gate (V_M) (Fig. 3.7). The middle barrier gate (V_M) allows for tuning of the tunnel coupling between electrons residing on the individual dots. This additional control knob is useful in the realization of a singlet-triplet qubit hosted by the DQD. The DQD potential well is defined and controlled by two outer barrier gates (V_{LB}^{DQD}) and V_{RB}^{DQD} , which enables control of the tunnel

coupling to the electron reservoir. If the middle barrier is sufficiently low, a single quantum dot is formed, while for a sufficiently high middle barrier, the two dots are well-separated and have a vanishing tunnel coupling. The DQD electron occupation is controlled by the plunger gates of the individual dots.

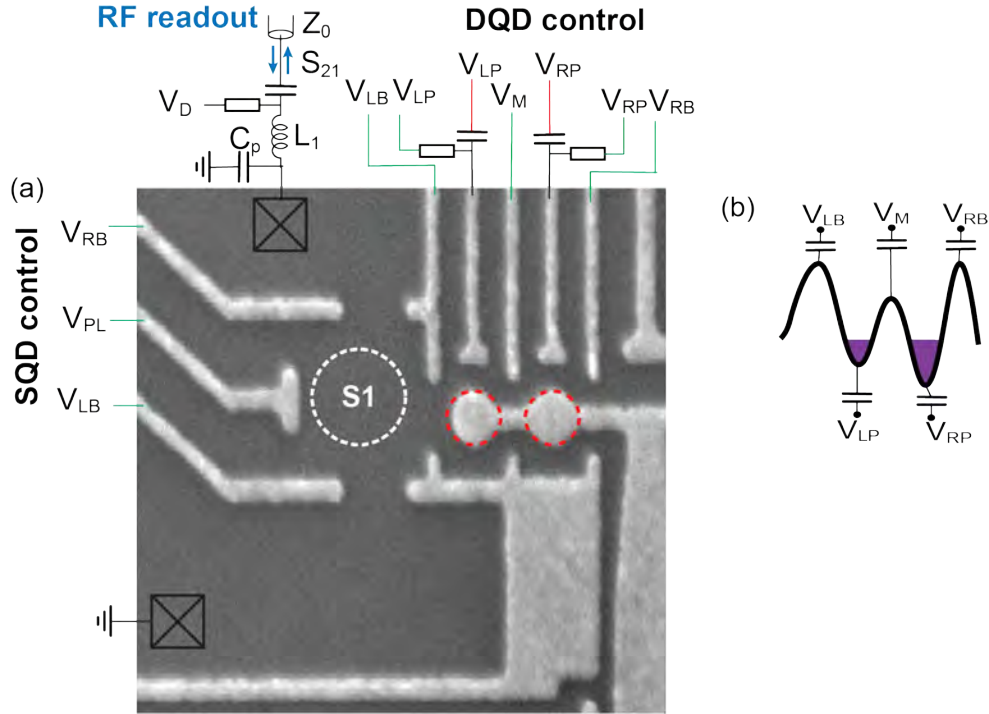


Figure 3.7: **Control and readout in one of the quadrants in the GaAs device:** (a) The gate electrodes that define and control the DQD constitute two outer barrier gates (V_{LB}^{DQD} and V_{RB}^{DQD}), a plunger gate for the left (V_{LP}^{DQD}) and right QD (V_{RP}^{DQD}) and a middle barrier gate (V_M). For charge sensing purposes a nearby sensor dot is formed and controlled with left and right barrier gates (V_{LB}^{S1} , V_{RB}^{S1}) and a plunger gate (V_{PL}^{S1}). The top left ohmic gate is connected to a tank circuit consisting of a surface-mount inductor (L_1) and a parasitic capacitance to ground (C_p). A coupling capacitor C_c and a resistor R_D form a bias tee that additionally allows for applying a DC voltage on the ohmic contact (which can be used in transport measurement). Another ohmic contact can act as a source/drain reservoir and allows for transport measurements between any pair of ohmics in the device. A voltage can be applied to act as a source-drain bias. The ohmic is grounded in RF reflectometry measurements.

3.5 Charge sensing using SQD ohmic-based RF reflectometry

Here, charge sensing with RF frequency reflectometry is achieved by monitoring the sensor dot impedance, which acts as a variable load on the LC circuit. In each quadrant of the device, one of the ohmics is connected to an inductor, which together with the parasitic capacitance to ground forms the LC circuit (Fig. 3.7b). Since $L_1 \neq L_2 \neq L_3 \neq L_4$, the resonance frequencies differ for the individual LC circuit resonators, which allows for simultaneous, frequency-multiplexed RF readout of the four DQD states. The DQD state is inferred from changes in the sensor dot state which is monitored by the RF reflectometry due to capacitive coupling to the SQD. From capacitive shifts in the sensor dot Coulomb peaks, charging events on the double quantum dot can be inferred. The occupations numbers in the DQD are determined from emptying the dot up to the last electron. Thereby inferring the first electron loading on QD₁ and QD₂ and counting the number of charging events from there.

The resonance frequencies are extracted by acquiring the reflection coefficient of the ohmic embedded in the tank circuit while pinching off the 2DEG of the corresponding quadrant with the backbone gates (Fig. 3.8). From S_{21} traces acquired with a VNA, we extract $f_0^1 \approx 130.4\text{MHz}$, $f_0^2 \approx 274.1\text{MHz}$, $f_0^3 \approx 156.8\text{MHz}$, $f_0^4 \approx 182.5\text{MHz}$.

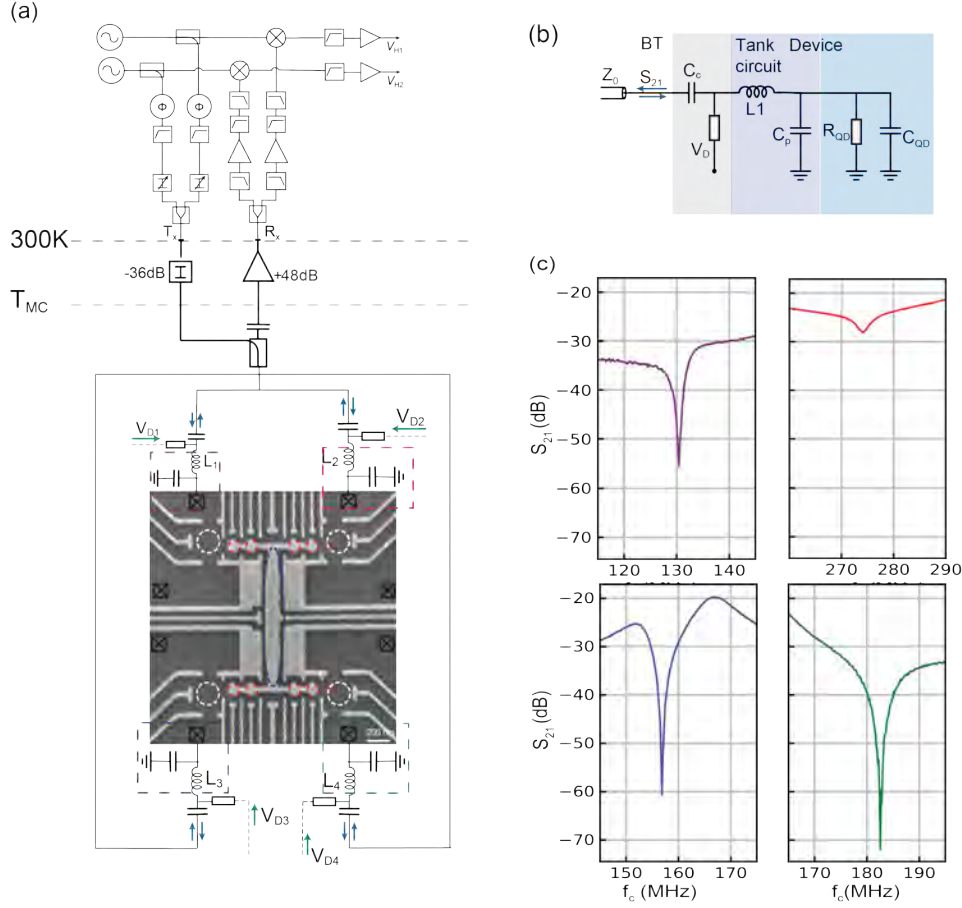


Figure 3.8: Averaged S_{21} -traces taken with a Vector Network Analyzer while pinching off the 2DEG in Q1 (purple), Q2(red),Q3 (blue) and Q4(green).

3.6 Calibration of high-frequency voltage pulses

Rapid electric control is at the core of readout and manipulation methods of $S - T_0$ qubits hosted in a DQD as well as for pulsed gate spectroscopy experiments. In the experimental apparatus, high-frequency voltage signals are generated by an arbitrary waveform generator (AWG) and are interconnected to the gate electrodes at the device through attenuated coaxial lines in the cryostat, reaching a bias tee that enables combining the low- and high-frequency voltage signals before reaching the gate electrode. This inter-connectivity has three experimentally relevant effects on the waveform arriving at the sample of the high-frequency voltage signal output by the AWG. Careful calibration is needed to ensure that the control sequence arriving at the sample corresponds to the designed control sequence.

First, the attenuation along the coaxial lines in the cryostat result in a reduction of the pulse amplitude by a factor $V_{\text{out}}/V_{\text{in}} = 10^{\text{loss}/20}$. To compensate for the attenuation, the signal output by the AWG is multiplied by the calibrated voltage division factor $V_{\text{out}}/V_{\text{in}}$. The voltage division factor is calibrated by measuring the peak splitting between two copies of a peak that appear when a continuous square wave pulse sequence with a 50/50 duty cycle and amplitude $V_{\text{pp}}^{\text{AWG}}$ is applied to the device.

When a high-frequency voltage signal passes the bias tee, the signal will be high-pass filtered, the high-pass filtering of the capacitor in the bias tee will result in a systematic distortion of the waveform arriving at the sample. We can correct for this systematic distortion by uploading a waveform that after high-pass filtering results in the desired waveform. This is done by applying a high-pass correction to the waveforms uploaded to the AWG and requires careful calibration of the applied correction.

In addition, a high-frequency voltage pulse cycle with non-zero time average passing through a bias tee, rejecting all low-frequency components of the signal. This then results in a DC offset of the high-frequency control voltage signal applied on the gate electrodes of the sample. To overcome this problem, a correction pulse, that brings the time-average of the pulse cycle to zero, can be embedded in the pulse cycle. A drawback of this technique is the (often) lengthy correction pulses as well as the need to adapt the uploaded correction pulse when pulse parameters (e.g. duration, the amplitude of the individual pulses in the cycle) is varied throughout the sequence. In the experiments presented in Chapter 5, we instead employ an alternative pulsing method that inherently has a zero time average, thereby overcoming this experimental complication.

A self-compensating pulse method

A self-compensating pulsing method employed in Chapter 5, is designing a pulse cycle for which $V^{\text{AWG}}(t + T/2) = V^{\text{AWG}}(-t + T/2)$, and consequently $\overline{V^{\text{AWG}}(t)} = 0$. Introducing this self-balanced pulsing technique drops the requirement of adding an additional correction pulse to the sequence and has the advantage of being inherently compensated. As a consequence, pulse parameters in the sequence can be varied without the need of adjusting the compensation. The basic and key concept is to design a pulse cycle in which the pulse voltage control cycle (purposed for the experiment to be performed) is traversed, the reversed path (in voltage space) is then added to the cycle to bring the center of gravity of the pulse cycle to zero.

By embedding two measurement points, the reversed path is re-purposed and can for example serve as a control, comparison, or verification measurement. This two-measurement self-compensating pulsing scheme could especially be of interest for pulsed gate spectroscopy or PSB experiments.

Fig. 3.9 shows two pulse cycle designs in the self-compensated pulsing scheme with a single (Fig. 3.9a) and two measurement points (3.9b) embedded in the pulse cycle. Fig. 3.9a shows a control cycle used for PSB measurements, constituting a typical

triangular pulse cycle used in PSB detection experiments (annotated in green). The reversed path (annotated in red) balances the pulse cycle, ensuring the center of gravity of the pulse cycle is found at zero.

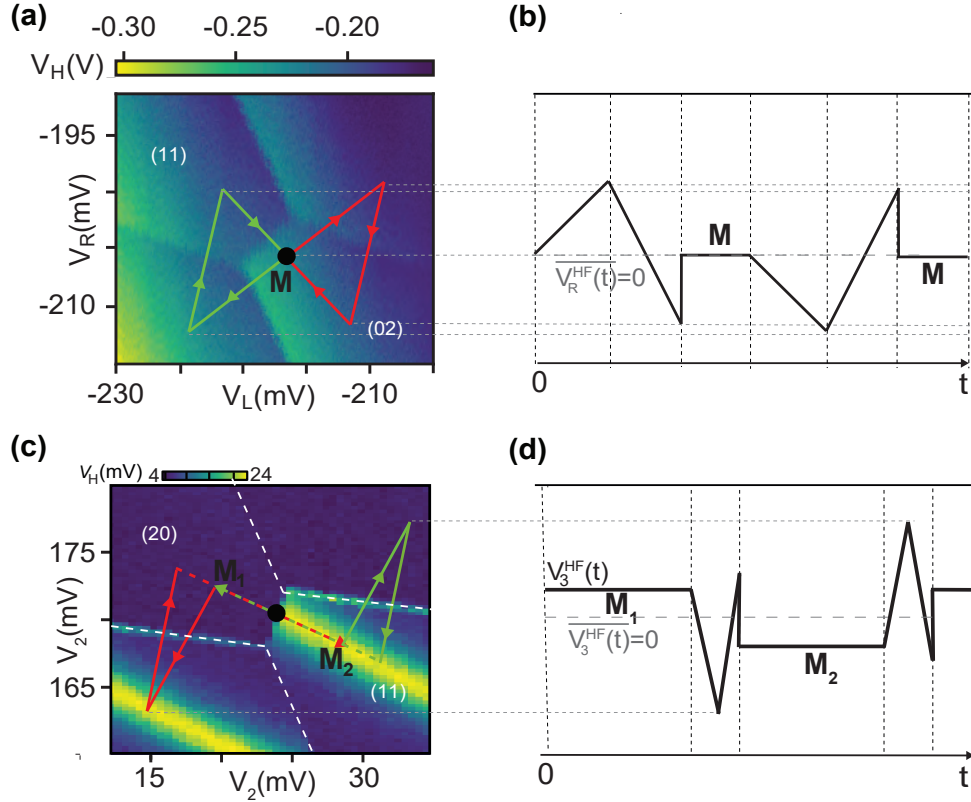


Figure 3.9: **A self-compensating pulse sequence scheme** (a) A single balanced pulse cycle containing one measurement that coincides with the center of gravity of the pulse cycle (black). A typical triangular pulse cycle used in PSB detection experiments is annotated on the charge stability map (green) of a DQD formed in the top-left quadrant of the GaAs device near the (1,1)-(2,0) transition. The reversed path (red) balances the pulse cycle and ensures that the center of gravity of the cycle is found at zero. (b) The voltage control pulse cycle applied on the high-frequency line of the right gate of the DQD. The time-average of the AWG output signal of a single pulse cycle is zero. (c) Balanced pulse cycle with two measurement points of interest M_1 and M_2 positioned in the (1,1) and (0,2) charge stability respectively. (d) Control voltage output signal of a single pulse cycle applied on the high-frequency line of one of the gates of the DQD.

Coherent operation of a singlet-triplet qubit in a GaAs double quantum dot

In the following, the coherent operation of a singlet-triplet qubit hosted by the top-left DQD of the two-dimensional GaAs QD array (see Section 3.6) is presented. We operate exchange-driven oscillations by applying a rapid electrical control sequence on the high-frequency lines of the plunger gates of the DQD. A sensible design of the control sequence requires knowledge of the S-T₊ anti-crossing in the two electron spin state spectrum from $|S\rangle$ into $|T_+\rangle$, to minimize leakage outside the qubit's subspace ($S = 0$).

To this end, S-T₊-leakage spectroscopy is performed (Sec. 4.1) to extract the location (in double-dot detuning ϵ) of the S-T₊ anti-crossing at a given magnetic field B_z . The point in the detuning of the S-T₊ anti-crossing moves with magnetic field as the split-off polarized triplet states will move in energy. A magnetic field sweep reveals a funnel-shaped pattern of the observed S-T₊-leakage from which the tunnel coupling t_c , the exchange interaction strength J (as a function of the double-dot detuning ϵ) and the parallel and perpendicular offset fields can be extracted.

Exchange-driven oscillations are operated by employing a fast electrical control sequence (Sec. 4.2). The rotations are a result of the spin-exchange interaction and yield oscillations at a frequency of $\Omega = J/\hbar$. Since J depends on the double-dot detuning ϵ , the frequency can be modulated by changing the exchange operation point in detuning ($\epsilon = \epsilon_E$), which is achieved by altering the exchange pulse amplitude in the electrical control sequence. We extract the Rabi frequency $f = \Omega/2\pi$, exchange interaction strength J , and the T_2^* -times from the measured exchange oscillations for different operating points ϵ_E .

4.1 S–T₊ leakage spectroscopy

The experiment is operated in the vicinity of the (1-1)-(2,0) inter-dot transition (Fig. 4.1) of the DQD in the top-left quadrant (Q1) of the GaAs device, where (n,m) is the number of electrons residing on the left and right dot respectively. Charge transitions are induced by traversing the (1,1)-(2,0) charge state degeneracy line by changing the voltages on the plunger gates of the DQD along a detuning axis - ϵ (V) (Fig. 4.1). This virtual voltage parameter is a linear combination of the voltages on the two plunger gates of the double dot and can be directly related to the double dot (energy) detuning by the lever arm α .

For $\epsilon < 0$, the DQD charge state where one electron resides on either dot (1,1) becomes energetically favorable, whereas for $\epsilon > 0$, the (2,0) state, where two electrons reside on the left dot is the energetically preferred state. Consequently, transitions from (1,1) to (2,0) can be induced by changing ϵ from negative to positive values. This is an essential tool in the readout of the two-electron spin state, which is achieved by spin-to-charge conversion through projecting the two-electron (1,1) spin state onto (2,0).

The two-electron spins form a singlet $S(2,0)$ when residing on the same dot (Fig 4.1(c)). When the two electrons are separated on the individual dots, the two-electron-spin state is a singlet ($S(1,1)$, $S=0$) or one of the triplet states ($T_+(1,1)$, $T_0(1,1)$, $T_-(1,1)$, $S = 1$). In the presence of a magnetic field, the triplet states are split by the Zeeman energy, given by $E_z = g^* \mu_B B$, where g^* is the electron g-factor ($g^* = -0.44$ in GaAs) and μ_B is the Bohr magneton. The singlet and unpolarized triplet state T_0 are split by the exchange interaction strength J . For large negative detuning, the spin exchange interaction approaches zero and consequently the spins become independent, i.e. the two-electron spin states are given by $|\downarrow\downarrow\rangle, |\downarrow\uparrow\rangle, |\uparrow\downarrow\rangle, |\uparrow\uparrow\rangle$.

At the S – T⁺ avoided crossing, $\epsilon = \epsilon_{ST_+}$, mixing of the two states results in a high probability of the state transitioning into the T₊-state. Thereby leaking into a state outside the qubit ($S = 0$) subspace. This S-T₊ leakage can be detected by applying a fast control sequence as discussed in the following.

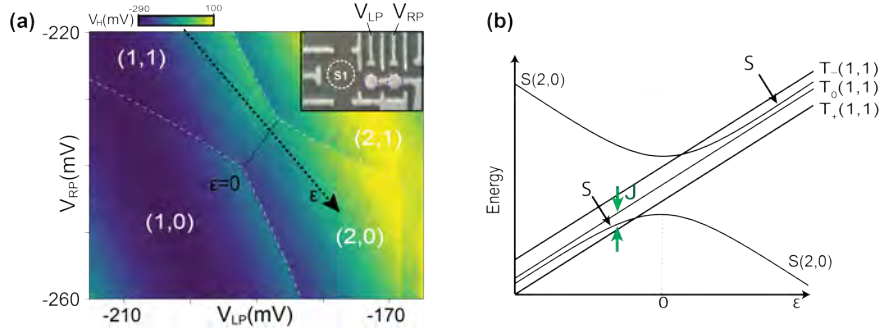


Figure 4.1: **Two-electron spin state spectrum in a DQD near the (1,1)-(2,0) transition as function of the detuning ϵ** - (a) Charge stability map in the vicinity of the (1-1)-(2,0) transition of the DQD under study. The defined detuning voltage parameter is annotated. The offset is defined such that $\epsilon=0$ is at the charge degeneracy line. (b) Schematic of two-electron spin state energy spectrum near the (1,1)-(2,0) transition as a function of the detuning ϵ .

A single train of voltage pulses that makes up the high-frequency pulse sequence for S- T_+ leakage spectroscopy is annotated on the DQD charge stability map (Fig. 4.2) and consists of four control steps. First, a S(2,0) is prepared on the left dot by (i) unloading and (ii) reloading an electron. This is achieved by applying slow adiabatic ramps ($t_L = t_U = 10\mu s$) across the charging line that adds(removes) an electron on the left dot. After preparation, the two electrons are separated on the individual dots by applying a diabatic pulse across the inter-dot transition along the detuning axis to $\epsilon = \epsilon_S = \epsilon_M - A_S$, where ϵ_S is the point in detuning of the separation point, ϵ_M is the location of the measurement point and A_S is the separation pulse amplitude in the sequence.

At the separation point ($\epsilon = \epsilon_S$), a wait time of $t_s=20ns$ is implemented. The amplitude of the separation pulse (and thereby ϵ_S), is varied in each consecutive waveform in the sequence from $A_S=1-50$ mV. For $\epsilon_S = \epsilon_{ST_+}$, an increased probability of leakage into the T_+ -state is expected. Since the $T_+(1,1)$ state is blocked due to Pauli blockade when projecting the state onto (2,0), the T_+ leakage probability can be indirectly inferred from the measured charge signal at $\epsilon = \epsilon_M > 0$. This then allows for extracting the point in detuning where the S and T_+ cross in the two-electron spin state level spectrum, since the leakage probability is expected to be highest at $\epsilon = \epsilon_{ST_+}$ as a result of maximum admixing of the states at the crossing point.

Projective measurement of the DQD charge state at M is achieved by applying a diabatic pulse from the separation point to $\epsilon = \epsilon_M$ across the (1,1)-(2,0) transition. In practice, this requires a measurable difference in the sensed reflected RF signal between the (1,1) and (2,0) DQD charge states at $\epsilon = \epsilon_M$. Projection of the DQD

charge state onto $(2,0)$ when the system resides in $T^+(1,1)$ will then result in sensing the RF signal corresponding to $V_M^H(1,1)$ charge state at the measurement point M.

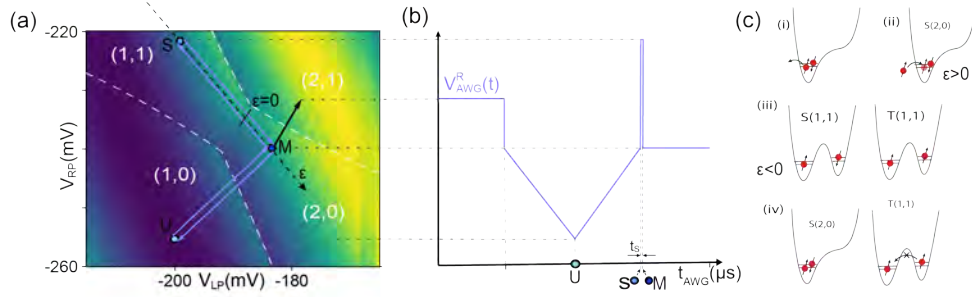


Figure 4.2: **High-frequency voltage control pulses for S – T₊-leakage spectroscopy:** The control pulse cycle of a single waveform consists out an adiabatic ramp to U followed by a ramp back to M to initialize S(2,0). The separation pulse separates the two electrons on the individual dots by pulsing from M to S. After a wait time of $t_s=20\text{ns}$, projective readout is achieved by pulsing from S to M. At M, a wait time of $10\mu\text{s}$ is implemented. (a) Annotated pulses of a single waveform. The points S and M are located on the defined detuning voltage parameter ϵ . (b) Schematic of the pulses contained in a single waveform applied on the plunger gate of the right dot.

Fig. 4.3 shows the measured integrated ($t_{\text{int}}=8\mu\text{s}$) homodyne voltage signal at M, measured by a fast digitizing card (Alazar 9360) while applying the above-described control sequence on the high-frequency lines of the plunger gates of the DQD. We observe S – T₊ leakage as a peak in the (averaged) detected homodyne voltage at the measurement point, which allows for extraction of ϵ_{ST_+} .

By sweeping the magnetic field, the split-off T_+ -state and thereby ϵ_{ST_+} are expected to move (Fig. 4.3) with magnetic field. A magnetic field sweep while acquiring the integrated homodyne voltage signal at M, shows a funnel-shaped pattern of the detected leakage signal.

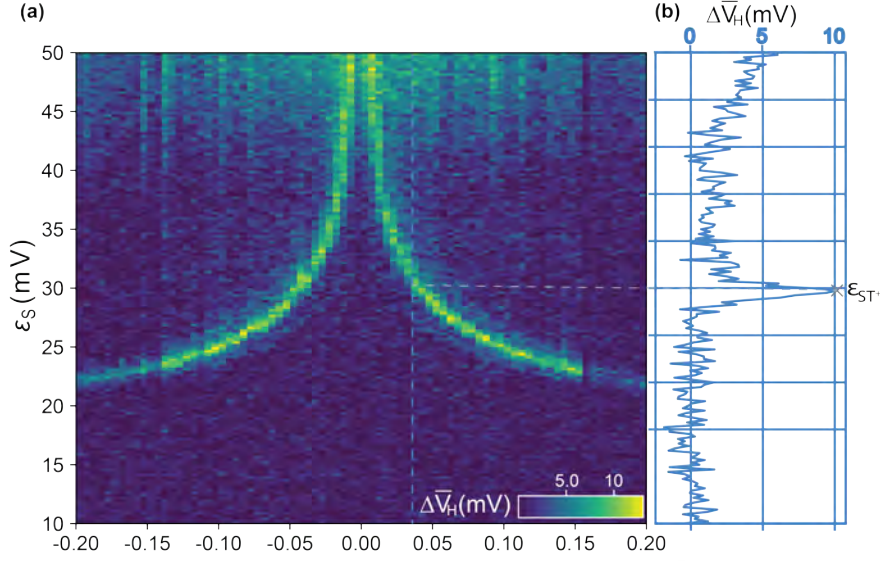


Figure 4.3: S – T+ leakage spectroscopy with varying magnetic field - (a) Spin funnel acquisition, the averaged integrated ($t_{\text{int}} = 8\mu\text{s}$ homodyne voltage measured at M gives an indirect measure of the T^+ leakage probability, a high (1,1) state probability results in a higher averaged detected homodyne voltage. (b) Line trace of (a) at $B_z = 0.03T$.

4.2 Coherent exchange oscillations of a singlet-triplet qubit

Coherent exchange oscillations can be driven by a high-frequency voltage control pulse cycle applied on the fast lines of the plunger gates of the DQD. To design a sensible electrical control pulse cycle, it is useful to know ϵ_{ST+} . This information can be extracted from a S-T₊ leakage spectroscopy acquisition at the magnetic field at which the exchange oscillations are operated ($B_z=100\text{mT}$ in the following).

The control pulse cycle (Fig. 4.4) starts with the preparation of a singlet S(2,0) by unloading and reloading an electron on the left dot. After which the two-electron-spin state is initialized in the $|\downarrow\uparrow\rangle-|\uparrow\downarrow\rangle$ basis **fedele**. This is executed in two steps: first a rapid adiabatic passage of the S – T₊ crossing is achieved by applying a ramp that is faster than the typical timescale where mixing between the two states due to the hyperfine interaction with the nuclear spin bath occurs ($\sim \hbar\mu_B g B_N$)[22]. This is followed by a slow, adiabatic ramp to large negative detuning $\epsilon = \epsilon_I \ll 0$, where the electron spin states become decoupled and the two-electron-spin state is a mixture of $|\downarrow\uparrow\rangle, |\uparrow\downarrow\rangle$. An exchange pulse is applied to bring the detuning to the operation point ϵ_E , where a varying wait time of τ is implemented. During this time the spin state

evolves for a period τ . If the Hamiltonian is dominated by the exchange interaction, this will result in a rotation of the spin state around the rotation axis that is defined J . After first pulsing back to ϵ_I , the reversed sequence is applied to arrive back at the measurement point M, where readout of the charge state at M gives an indirect measure of the two-electron spin state.

The frequency of the measured Rabi oscillations is determined by the exchange interaction strength as $\Omega = J/\hbar$. Since $J(\epsilon)$ depends on the double dot detuning ϵ , control of the Rabi frequency is achieved by changing the amplitude of the exchange pulse and thereby the exchange operation point ($\epsilon = \epsilon_E$) along the detuning axis (Fig. 4.4). We drive exchange oscillations at three different operating points ϵ_E by changing the exchange pulse amplitude to $A_E=(25,30,35)\text{mV}$ and thereby the exchange operation point with respect to the inter-dot transition to $\epsilon_E=(-22.7,-27.7,-32.7)\text{mV}$ respectively. The averaged homodyne voltage at the measurement point ($t_{\text{int}} = 8\mu\text{s}$) gives an indirect measure of the spin state and shows exchange-driven oscillations (Fig. 4.4). The Rabi frequencies at different operation points are extracted by fitting an exponentially damped cosine, yielding $f = (104.2 \pm 0.4)\text{MHz}$, $f = 64.2 \pm 1.3\text{MHz}$, $f = (41.1\text{MHz} \pm 4.6)\text{MHz}$ and an exchange interaction strength of $J = (0.43 \pm 0.002)\mu\text{eV}$, $J = (0.27 \pm 0.005)\mu\text{eV}$, $J = (0.17 \pm 0.019)\mu\text{eV}$ for $\epsilon_E=(-22.7,-27.7,-32.7)\text{mV}$ respectively. The extracted T_2^* -times at different operation points are given by $T_2^* = (52.9 \pm 3.2)\text{ns}$, $T_2^* = (54.0 \pm 4.0)\text{ns}$, $T_2^* = (41.1 \pm 4.6)\text{ns}$.

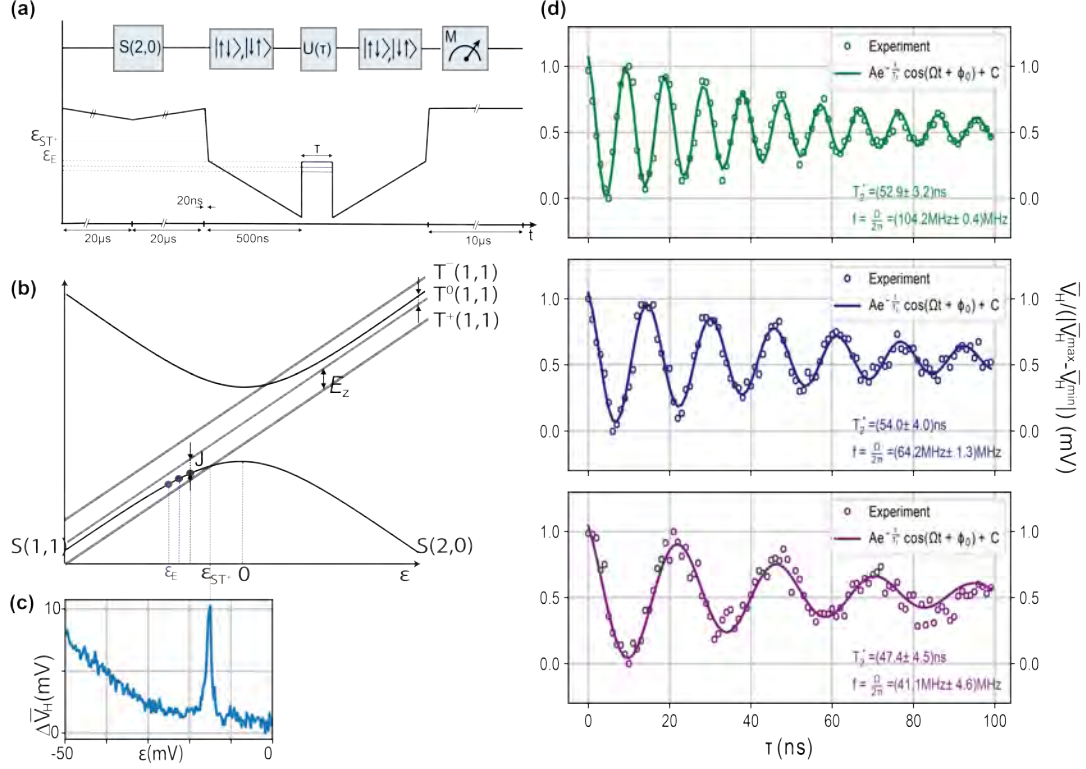


Figure 4.4: **Coherent exchange-driven oscillations:** (a) Illustration of the applied control sequence. The duration of the exchange pulse τ is varied in each consecutive waveform in the sequence. (b) Schematic of the energy spectrum of the two-electron spin states. The splitting between S and T_0 is given by the exchange interaction strength $J(\epsilon)$, which depends on the detuning ϵ . (c) S – T_+ leakage spectroscopy measurement at $B_z=100\text{mT}$ from which $\epsilon_{\text{ST}+}$ is extracted. (d) Driven exchange oscillations for different exchange operation points $\epsilon_E=-22.7\text{mV}$ (green), -27.7mV (blue), -32.7mV (purple).

4.3 Summary and discussion

We operate a singlet-triplet qubit hosted in a GaAs/AlGaAs heterostructure QD device. The exchange interaction strength J , and consequently the Rabi frequency of the exchange oscillations, is modulated by changing the operated exchange point. We extract T_2^* -times from the exponential decay of the recorded exchange oscillations at different operating points, yielding the values presented in Table 4.1.

ϵ_E (mV)	T_2^* (ns)	J (μ eV)
-22.7	(52.9 ± 3.2) ns	0.43 ± 0.002
-27.7	(54.0 ± 4.0) ns	(0.27 ± 0.005)
-32.7	(41.1 ± 4.6) ns	(0.17 ± 0.019)

Table 4.1: Extracted T_2^* and J -parameters at different operating points for a singlet-triplet qubit hosted in a GaAs/AlGaAs device

The future goal of this experiment is the optimization of $|S\rangle$ - $|T_0\rangle$ readout fidelities using machine learning. We here tune-up a singlet-triplet qubit that is used for testing of optimization of $|S\rangle$ - $|T_0\rangle$ readout fidelities.

Pulsed-gate experiments using a double quantum dot in a two-dimensional silicon quantum dot array

The valley degree of freedom in Si devices significantly complicates the realization of spin qubits, since it fundamentally can limit initialization, manipulation and measurement fidelities of spin qubits hosted in Si devices [30]. The high-dependency of the orbital-valley level structure on atomic-scale details of the confining interface that differs from device to device [30][3], has motivated the development of experimental probing techniques to extract information of the valley-orbital levels. Common experimental methods employed to extract the valley splitting include transport measurements via excited valley- or orbital level states, Shubnikov-de-Haas measurements, photon-assisted tunneling techniques and pulsed gate spectroscopy. Pulsed gate spectroscopy has been exploited to extract the valley splitting in a variety of devices, including nanowire-based silicon-on-insulator devices. Reported valley splittings in similar devices to the one under study range from 0.2-0.7 meV [15][31].

In the following, we perform a pulsed gate experiment in a DQD (formed by QD₂-QD₃) in the silicon 2x2 QD array using a self-balanced pulsing scheme. By performing time-resolved measurements while pulsing diabatically across a detuning axis that traverses the (1,1)-(0,2) inter-dot transition, non-monotonic behavior of the charge decay is observed. Distinctive biasing points in the detuning for which enhanced relaxation is observed, are identified and could be attributed to avoided level crossings in the (1,1)-(0,2) two-electron spin spectrum.

5.1 A self-balanced two-measurement pulse cycle

The pulsed gate experiment is performed by applying a high-frequency self-balanced voltage control cycle on the gates (V_2^{HF} and V_3^{HF}) of the DQD under study (QD₂ – QD₃) while simultaneously stepping the DC voltages (i.e. $V_2^{\text{LF}}, V_3^{\text{LF}}$) along a detuning axis $\epsilon(V)$. This defined virtual voltage parameter is given by:

$$\epsilon = \begin{pmatrix} 0.88 \\ -0.47 \end{pmatrix}^T \begin{pmatrix} V_2 \\ V_3 \end{pmatrix} + \epsilon_0 \quad (5.1)$$

, where ϵ_0 is defined such that the detuning axis crosses the (1,1)-(0,2) charge degeneracy line at $\epsilon = 0$.

The pulse sequence is built from a continuously repeated pulse cycle that has a total duration of 160 μs . We design a self-compensating pulse cycle, with two measurement points M_1 and M_2 , where M_1 is positioned in the (0,2) charge stability region and M_2 in the (1,1) charge stability region. Charge relaxation to the charge ground state is measured by applying a diabatic pulse from P_1 to M_1 and from P_2 to M_2 across the defined detuning axis (Fig. 5.1).

A single pulse cycle consists of six pulses, starting out with exchange of an electron of QD₃ with the leads via an adiabatic¹ ramp ($t_{\text{load}} = t_{\text{unload}} = 10\mu\text{s}$) across the QD₃ charging line from M_2 to R_1 and from R_1 to P_1 .

This is followed by a diabatic² pulse ($V_{\text{pp}}=13\text{mV}$) from P_1 to M_1 across the (1-1)-(0,2) inter-dot transition. A wait time of $t_{\text{wait}} = 60\mu\text{s}$ at the measurement point is implemented. The second part of the cycle follows the reversed path by first unloading and reloading an electron through an adiabatic ($t_{\text{ramp}} = 10\mu\text{s}$) ramp from M_1 to R_2 and R_2 to C_2 . This is followed by a diabatic pulse ($V_{\text{pp}} = 13\text{mV}$) along the defined detuning axis ϵ across the inter-dot transition to M_1 .

The purpose of the ramps between $P_1 - R_1$ and $P_2 - R_2$ is two-fold: it allows for the exchange of an electron with the leads before pulsing across the detuning axis and it serves as a reference point. The latter uses (in this case) three diagnostic features observed in the measurements: the two sharp, dispersive signal resulting from the resonant tunneling of an electron between QD₃ and the leads, and second the sensor dot peak signal at R_2 allows a check of the careful calibration of the pulses (e.g. R_2 can act as a check of how the waveforms are arriving at the gate electrodes).

By stepping the virtual detuning parameter, the position of the M_1 and M_2 measurement points are changed during the acquisition. Here, the stepped detuning axis

¹Since QD₃ charging line is sensed as a dispersive signal, we expect the tunnel rates of the exchange of an electron of QD₃ is expected to be $\Gamma > f_{\text{drive}}$, where $f_{\text{drive}} = 191.1\text{MHz}$. This is done by moving slow enough ($t_{\text{pulse}} > 1/\Gamma$) across the charging line in a $10\mu\text{s}$ ramp to point B_1 and back to C_1 in a $10\mu\text{s}$ ramp.

²We note that the diabaticity of the detuning pulse is an essential aspect for the interpretation of the data. Here, we assume that the detuning pulse induces a diabatic transition, which is based on performing increasingly fast ramps across the inter-dot transition to observe when tunnel times are faster than the ramps.

allows for changing the detuning biasing point and potentially probing the detuning-dependent DQD (1,1)-(0,2) spectrum.

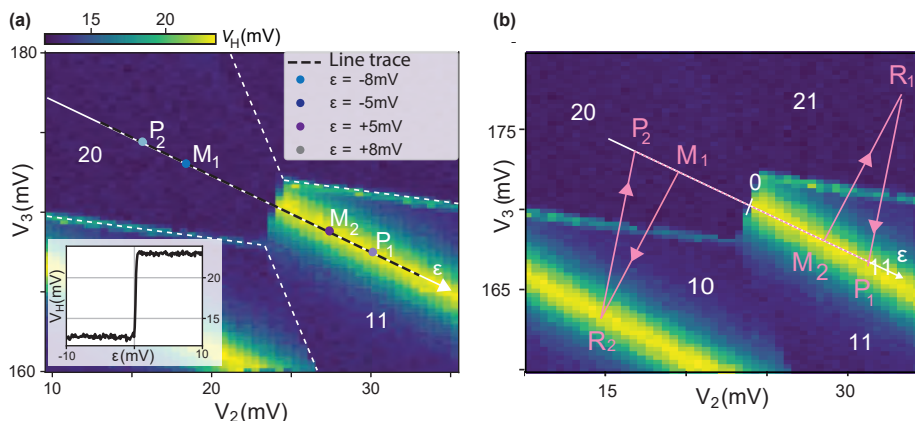


Figure 5.1: **Pulse cycle design** (a) Relevant DC points for the applied pulse cycle along the detuning ϵ (mV). The sensor dot signal is tuned at one of the measurement points M_2 such that there is a difference in contrast at (1-1) and (0-2). Points C_i and M_i are positioned along the defined detuning axis ϵ . The initial detuning DC offset is defined such that the charge it intersects with the charge degeneracy line at $\epsilon=0$. The measurement points M_1 and M_2 are positioned at $\epsilon=+5$ mV and $\epsilon=-5$ mV respectively. Points C_1 and C_2 are located at $\epsilon=+8$ mV and $\epsilon=-8$ mV, such that $V_{pp}=13$ mV for C_i - M_i square pulses. (b) Schematic of the output voltages on the low-frequency (top) and high-frequency (bottom) lines. A wait time of $60\mu\text{s}$ is implemented at each measurement point M_i .

A time-resolved measurement of the homodyne voltage acquired throughout the duration of one pulse cycle ($t=160\mu\text{s}$), reveals a non-monotonic charge relaxation pattern with points in detuning for which enhanced relaxation is observed. For each step along the detuning axis, the waveform is repeated 500 times, over which is averaged.

We observe enhanced relaxation when the measurement point M_1 and M_2 are biased at the inter-dot transition, where the (1,1) and (0,2) charge states are maximally hybridized. In practice, the actual detuning value at which the measurement is at the inter-dot transition depends on the definition of the $\epsilon = 0$ point. If the set $\epsilon = 0$ point slightly differs from where the detuning axis crosses the inter-dot transition, then the values for which M_1 and M_2 are found at the inter-dot transition are shifted by $|5 - \epsilon_I|$. Since by extracting the point in detuning where the homodyne signal changes from V_H^{sensor} to $V_H^{\text{background}}$, we can identify the value for which the inter-dot transition is traversed and introduce the corrected detuning voltage parameter as $\epsilon_{\text{shifted}} = \epsilon - (|5 - \epsilon_I|)$.

The other biasing point, labeled as $\epsilon_1^{M_1/M_2}$ of enhanced relaxation is observed when the exchange with the dot-leads becomes energetically favorable, resulting in a fast

transition to the energetically favorable charge configuration. This occurs when M_1 and M_2 are biased further into the (1,1)/(0,2) charge stability region.

We define the detuning probing window as $\Delta\epsilon_{\text{window}} = \epsilon_1^{M_1/M_2} - \epsilon_I$. Within this window, we observe non-monotonic charge relaxation at M_1 and M_2 . We investigate this behavior in more detail for different applied magnetic fields B_z (Sec. 5.1.1).

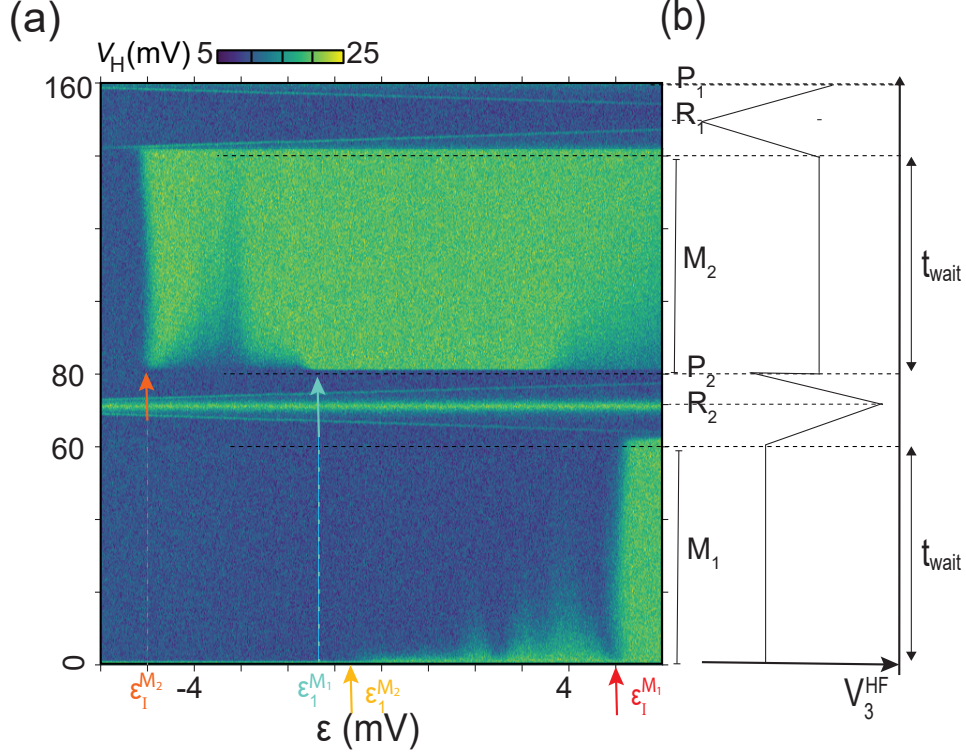


Figure 5.2: **Time-resolved measurement of a SC pulsed gate experiment at $B_z = 0.1\text{T}$** (a) Averaged traces of the homodyne voltage measured with a high-speed digitizing card (Alazar ATS9360) at a sample rate 100Msamples/s acquired throughout the full period ($t = 160\mu\text{s}$) of one pulse cycle. For every value of the detuning voltage parameter, the voltages on the low-frequency lines V_2^{LF} and V_3^{LF} are set according to $V_2 = 0.88 * \epsilon + V_2^{\epsilon_0}$ and $V_3 = 0.88 * \epsilon + V_3^{\epsilon_0}$. For every value in detuning, 500 traces are acquired, over which is averaged i.e. every column in (a) represents the average of 500 repetitions of the same acquisition.

5.1.1 Time-resolved measurements at different fields

We investigate the charge relaxation within the probed detuning window in more detail at different magnetic fields. Figure 5.3 shows the averaged traces resulting from

time-resolved measurement while pulsing the gates and stepping the DC voltages along a detuning axis as introduced in the previous section. While the traces are acquired throughout the full duration of one cycle ($t=160 \mu s$), here only the results during the M_1 and M_2 stage are shown. The resulting averaged traces are plotted against the shifted detuning, defined as $\epsilon_{\text{shifted}} = \epsilon - (|5 - \epsilon_I|)$. For each magnetic field, the detuning offset ϵ_0 is re-calibrated by taking a line trace along the defined detuning (see Fig. 5.1). For comparison purposes, the averaged traces in Fig. 5.3 are plotted against the shifted ϵ parameter to account for the difference in ϵ_0 and ϵ_I . For each magnetic field, $\epsilon_1^{M_1/M_2}$ is indicated. The measured charge decay features within the detuning probing window are investigated in more detail by extracting the decay times from fitting a single exponential decay function through the line traces during both measurement stages, resulting in Fig. 5.4. For $|\epsilon| > |\epsilon_1|$, the charge relaxation becomes too fast to fit a single exponential function, resulting in a large relative error of the found optimized fitting parameter.

For $|\epsilon| < |\epsilon_I|$ the M_1/M_2 measurement points have crossed the inter-dot transition. Fitting of an exponential decay function then results in an unphysical interpretation of the extracted time constant. Therefore, solely the extracted charge decay time constants for values of $|\epsilon_1| < |\epsilon| < |\epsilon_I|$ are shown ³.

³The time constants are extracted for a larger range of detuning values for the purpose of more precise extraction of ϵ_I and ϵ_1

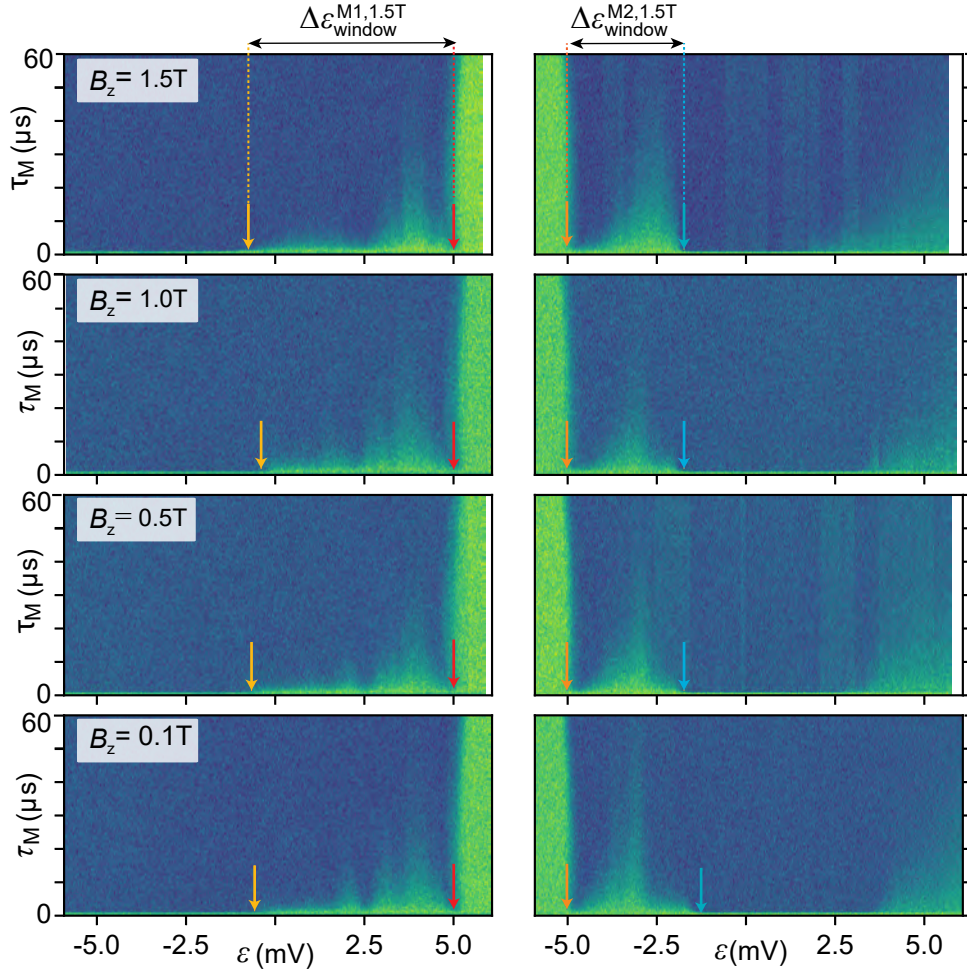


Figure 5.3: **Time-resolved charge decay measurements at M_1 and M_2 at different magnetic fields** (a) Averaged traces of the homodyne voltage signal acquired throughout the first measurement stage with a wait time ($t_{\text{wait}} = 60\mu\text{s}$) at M_1 . Distinctive charge decay features are observed. Fast relaxation indicated by the blue arrows is attributed to a fast transition from charge ground states due to exchange with the leads rather than inter-dot tunneling. At the inter-dot transition, fast relaxation is observed. The data is shifted such that M_1 and M_2 are exactly at the charge degeneracy line $\epsilon = 0$ for $\epsilon = +5\text{mV}$, $\epsilon = -5\text{mV}$ respectively (b) Time-resolved measurement during the M_2 stage in the sequence. Data is plotted on an inverted color scale for comparison purposes.)

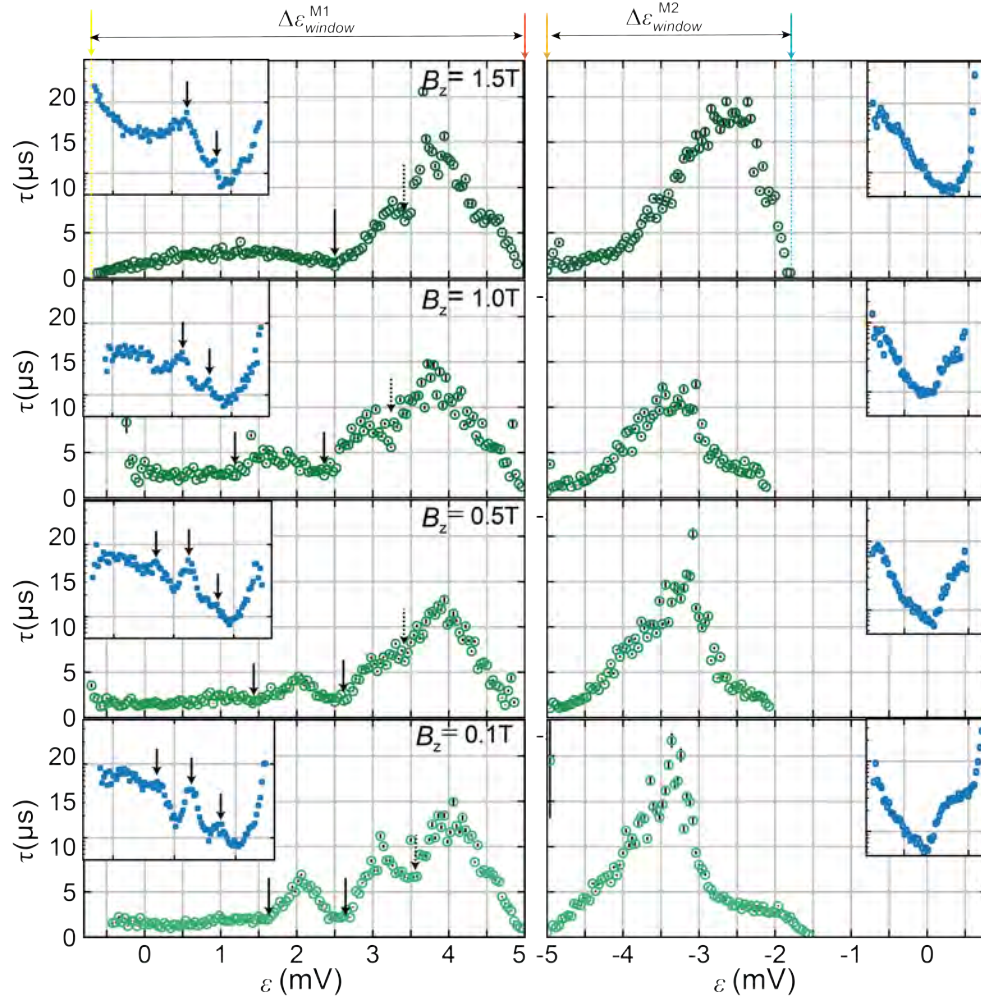


Figure 5.4: **Extracted charge decay times from averaged time-resolved measurements during wait times M_1 and M_2** ($t_{\text{wait}}^{M_1} = t_{\text{wait}}^{M_2} = 60\mu s$) Characteristic charge decay time scales extracted from an exponential fit from the averaged of a $40\mu s$ window of the measurement stages (M_1) and (M_2). **(a)** Extracted time constants during M_1 stage at different fields. The plotted error bars indicate the square root of the covariance of the optimized fitting parameter and are generally too small to distinguish. The inset shows the charge decay rate $\Gamma = 1/\tau$, plotted on a logarithmic scale. Detuning values within the probed window $\epsilon_{\text{window}}^{M_1}$ for which a clear enhanced charge decay rate is observed are indicated by the black arrows. **(b)** Extracted time constants during the M_2 -stage at different fields.

5.2 Summary and discussion

We report the observation of enhanced relaxation at distinctive values of the DQD detuning, reflecting the complex orbital-valley level structure in foundry-fabricated SOI devices. While pulsed gate spectroscopy has been extensively used to extract the valley splitting by probing the (0,1)-(1,0) spectrum, here we show the potential of probing the (1,1)-(0,2)/(2,0) two-electron spin state levels. We note that the crowding of states in the spectrum as well as the lack of knowledge of the tunnel coupling prevents us from extracted the exact level structure (1,1)-(0,2).

We note that the extraction of ϵ_I to shift the data presented in Fig. 5.3 gives a source of systematic error in the location of the observed relaxation features along the detuning axis, making it challenging to record the shifting of the observed relaxation hot spots in detuning.

5.3 Reproducibility

We report on the reproducibility of specific charge decay features observed at a given field in the Appendix (see B).

An RF-DQD charge sensor in a two-dimensional QD array

Charge sensing techniques based on RF reflectometry have been harnessed as a successful readout method in gate-defined quantum dot systems. In gate-based dispersive RF readout, the QD system is probed with an RF tone applied on an existing gate electrode, thereby dropping the requirement of implementing an additional charge detector in the device [32]. This eases the requirements imposed on the QD device architecture and enhances the scalability of the readout scheme. In conventional gate-based dispersive sensing techniques, the QD of which the gate electrode is embedded in the LC circuit acts as a sensing dot and can be used to sense nearby QDs that are capacitively coupled to the sensor dot by detecting the capacitive shift that the sensor dot Coulomb peak undergoes upon changes in charge occupations in the other dots¹.

Here, we explore RF charge sensing with a DQD in a two-dimensional QD array. The proposed readout technique has several (potential) key advantages compared to conventional gate-based dispersive readout using a single QD as a charge sensor.

First, the proposed readout technique does not directly involve a tunneling process with the leads as in charge sensing by measuring the response signal of a single electron tunneling between the sensor dot and the lead. And second, utilization of a DQD as an RF charge sensor is expected to further enhance the scalability of gate-based RF readout in two-dimensional QD arrays since the capacitive shift that the DQD inter-dot signal undergoes of a far-away QD is from a simple electrostatic consideration to be larger than the shift that the sensor QD peak undergoes.

¹This requires the capacitive shift to be larger than the FWHM of the sensor peak in order to be distinguishable

The concept of a DQD RF-charge sensor is demonstrated in a two-dimensional QD array in a FDSOI split-gate device. We focus on a two-by-two array, but the technique could be especially advantageous in larger two-dimensional arrays. The charge state of a DQD using the opposing two dots in the array as a DQD RF charge sensor by monitoring the RF response signal as a result of the single-electron tunneling between the dots of the tunnel-coupled sensing DQD. Thereby purposing the DQD as an RF charge sensor to sense the charge state of the two opposing dots in the array.

A double quantum dot is formed by loading electrons on QD₁ and QD₄ (of which the gate electrode G4 is embedded in the LC circuit).

Six to seven electrons are loaded QD₄ and one to two electrons on its neighboring dot (QD₁) to form the sensing DQD in the array. The RF carrier frequency is $f_c = 190.9\text{MHz}$ and the estimated RF power incident on the inductor is $P_{RF} = -105\text{dBm}$. Fig. 6.1a shows a charge stability map in the vicinity of the inter-dot transition (7,2)-(6,1) of the sensing DQD. The dispersive RF response signal at the charge degeneracy line resulting from the fast ($\Gamma > f_{\text{drive}}$) single-electron inter-dot tunneling between the two dots is used as the sensing signal.

The sensed dispersive signal at the charge degeneracy line of the sensing DQD can then be exploited to sense the charge state of the opposing QDs in the array.

This is achieved by precise tuning of the quadruple dot system such that the polarization line of the sensing DQD coincides with the (2,0) charge state in the four-dimensional voltage parameter space. Fig. 6.1(b) shows the measured charge stability map in the vicinity of the (1,1)-(2,0) transition of QD₂, QD₃. The dispersive inter-dot signal of the sensing DQD (QD₁ – QD₄) creates a contrast between the (2,0) and (1,1) charge states of the opposing DQD (QD₂ – QD₃).

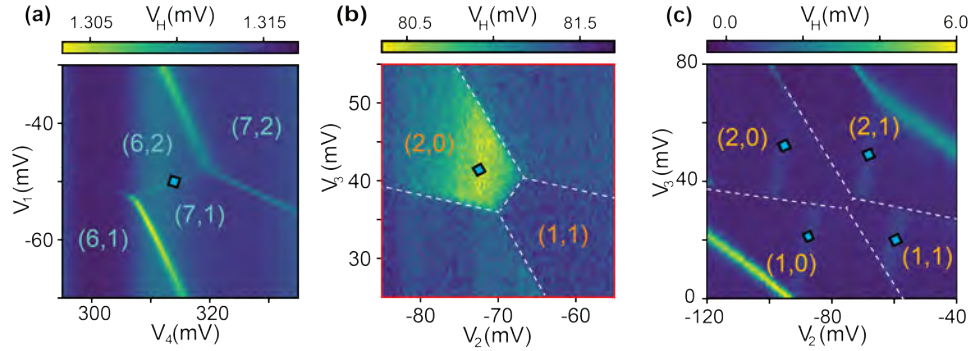


Figure 6.1: **RF charge sensing with a DQD-** (a) - Charge stability map showing the charge states of the DQD acting as a charge sensor in the two-dimensional array. The charge degeneracy line (7,2)-(6,1) of the DQD is measured as a dispersive RF response signal (indicated by the diamond) and is exploited to sense the charge occupations of the opposing quantum dots. (b) Charge stability map of the opposing DQD in the array (QD₂ – QD₃). The dispersive inter-dot signal of the sensing DQD (QD₄ – QD₁) is used to create a contrast between the (2,0) and (1,1) charge states. (c) Charge stability map of the opposing DQD (QD₂.QD₃) when the inter-dot signal of the sensing DQD is not tuned at the inter-dot transition.

6.1 Summary

In this chapter, RF charge sensing with a DQD in a two-dimensional Si array is demonstrating, serving as a proof-of-concept experiment.

Summary and outlook

This work has focused on performing pulsed gate experiments on a DQD within a two-dimensional QD array in a GaAs/AlGaAs heterostructure device and a silicon-on-insulator nanowire device.

We operate exchange-driven oscillations of a singlet-triplet qubit hosted in a GaAs/AlGaAs heterostructure device. We modulate the Rabi frequency of the exchange oscillations by changing the operation point ϵ_E along the detuning axis. The future goal is to use this $|S\rangle - |T_0\rangle$ test qubit to test machine learning algorithms. In specific, the aim is towards the optimization of $|S\rangle - |T_0\rangle$ -readout fidelity.

We perform pulsed gate experiments in a foundry-fabricated SOI device employing a self-compensating pulse sequence scheme that implements fast pulsing across a detuning axis from (0,2) to (1,1) and (1,1) to (0,2). While not originally purposed for pulsed gate spectroscopy, we observe enhanced charge decay rates at distinctive values in double-dot detuning, which may be related to enhanced relaxation near energy level crossings in the (1,1)-(0,2) level spectrum. Within the probed detuning window, enhanced relaxation is observed and identified at distinctive values of the double dot detuning. While pulsed gate spectroscopy has been extensively used to extract the valley splitting by probing the (0,1)-(1,0) spectrum, here we show the potential of probing the (1,1)-(0,2)/(2,0) two-electron spin state levels, which could be valuable information for the realization and operation of a singlet-triplet qubit in Si devices. We note that because of the crowding of states in the spectrum as well as the lack of knowledge of the tunnel coupling prevents us from extracted the exact level structure (1,1)-(0,2).

Future work on performing pulsed gate spectroscopy to extract the two-electron spectrum in SOI LETI devices should involve a systematic approach by first extracting

relevant parameters for simulating the two-electron spectrum (t_C, Δ_V) by employing a set of experimental techniques, where first the valley splitting is extracted by probing the (0,1)-(1,0) spectrum by for example the detuning axis pulsed spectroscopy technique recently proposed and demonstrated by HRL [30]. Once these parameters are known, the two-electron spectrum can be probed by a detuning pulse cycle similar to the one presented in this work. By recording the magnetic field dependence of the observed relaxation hot spots by sweeping the field over a larger range, information on the spectrum can be extracted. In addition, the presented pulse sequences can be further advanced by introducing a variable wait time at P_1 and P_2 and varying the pulse amplitude to measure when excited states become energetically (in)accessible.

In Chapter 6, we have demonstrated RF sensing with a DQD in a two-dimensional array. This alternative charge sensing technique is expected to have several advantages compared to gate-based dispersive charge sensing based on a single sensor-QD. Further exploration of using a RF-DQD charge sensor could focus on the demonstration of charge sensing in larger two-dimensional arrays as well as benchmark the readout sensitivity compared to conventional gate-based dispersive charge sensing techniques.



Experimental setup and instrumentation

The device is cooled down to cryogenic temperatures in a Oxford Triton 200/400 dilution refrigerator, reaching a MC temperature of $T_{MC} \approx 64\text{mK}$.

High- and low-frequency voltage control signals are provided by an Arbitrary Waveform Generator (AWG) and a high-precision voltage generator that operate at RT. The output of the RT voltage control instruments. The output the AWG that supplies high-frequency voltage signals is connected to the device chip via attenuated coaxial lines that can be connected that connect to the PCB hosting the device via mini-coax links. The low-frequency voltage signals output by the QDac are transferred inside the cryostat via DC looms equipped with a series of pi filters and low pass filters. The low- and high-frequency signals are combined by a bias tee on the motherboard. which then passes through an on-chip bias tees that connect to the gates of the device.

The RF signal is generated by a RF source typically operating at a carrier frequency of $f_{\text{drive}} = 191\text{MHz}$ in the experiments presented. The signal passes through a DC block before reaching a directional coupler that is connected to the reference port of a RF mixer and the RF input branch that reaches the RF input (Tx) port of the cryostat after a phase shifter, a high- and low-pass filter and a programmable attenuator. The Tx port connects to a coaxial line that is attenuated at different stages (total attenuation of -36dB), connect through the coupling port of a cryogenic directional coupler and then connects via a miniCoax tot the PCB, where it passes a bias tee consisting of a coupling capacitor and a resistor then through a surface-mount inductor to the gate of the sensor dot. The reflected RF signal then passes first through the inductor, capacitor via the mainline of the directional coupler to DC block. The reflected is then amplified amplified by a cryogenic amplifier at the 4K stage. The coaxial line connects via the output at the Rx port to a DC block and a

Reproducibility of measured enhanced charge decay rates

We test for the reproducibility of the detailed non-monotonic behavior of the charge transition time by repeating the same acquisition at a magnetic field $B_z=1.5T$. In a similar as discussed in Chapter5, we extract the characteristic decay time constant by fitting a single exponential decay function through the $30\mu_s$ of the M_1 stage, resulting in Figure B.1.

In addition, we compare the perform the same acquisition at opposite field $B_z = 0.1T$ and $B_z = -0.1T$. The extracted exponential decay time constants are given in Figure B.2.

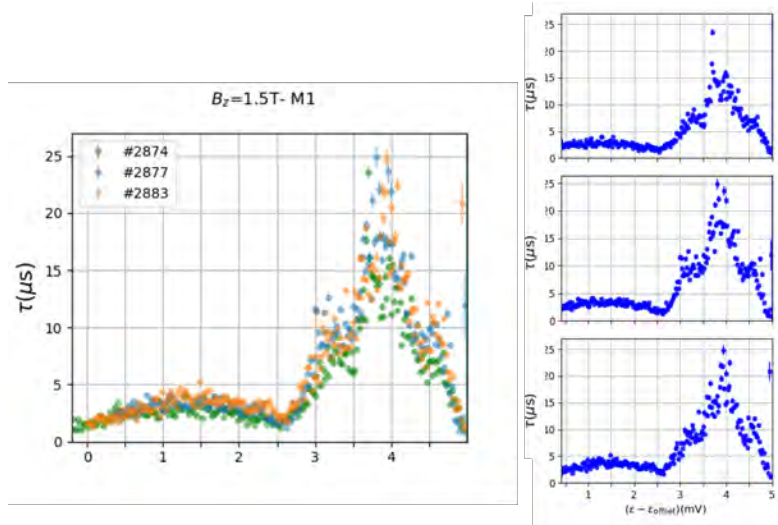


Figure B.1: **Extracted charge decay times at $B_z = 1.5\text{T}$.** A self-compensating pulse cycle as introduced in 5. Characteristic decay times during the M1 stage are extracted by fitting a single exponential decay function through the detuning line traces of the acquired time-resolved measurement.

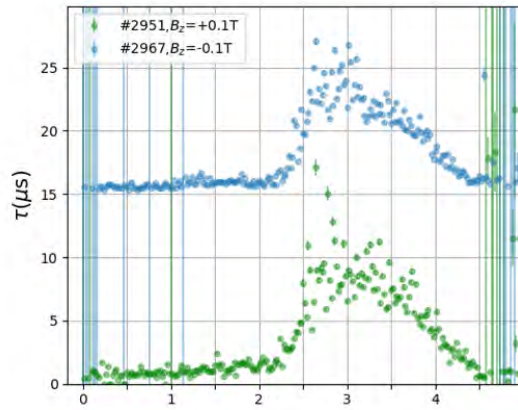


Figure B.2: **Extracted charge decay times at $B_z = 0.1\text{T}$ and $B_z = -0.1\text{T}$.** A self-compensating pulse cycle as introduced in 5. Characteristic decay times during the M1 stage are extracted by fitting a single exponential decay function through the detuning line traces of the acquired time-resolved measurement.

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