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Soft-mask fabrication of gallium arsenide nanomembranes for integrated quantum photonics

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Abstract

We report on the fabrication of quantum photonic integrated circuits based on suspended GaAs membranes. The fabrication process consists of a single lithographic step followed by inductively coupled-plasma dry etching through an electron-beam-resist mask and wet etching of a sacrificial layer. This method does not require depositing, etching, and stripping a hard mask, greatly reducing fabrication time and costs, while at the same time yielding devices of excellent structural quality. We discuss in detail the procedures for cleaning the resist residues caused by the plasma etching and present a statistical analysis of the etched feature size after each fabrication step.

Keywords: nanofabrication, plasma etching, photonic crystals, III–V semiconductors, quantum photonics, integrated optical circuits

(Some figures may appear in colour only in the online journal)

1. Introduction

Quantum photonic integrated technology deals with the generation, manipulation and detection of quantum light, typically in the form of single photons, within a semiconductor chip [1–7]. It constitutes an active field of research aiming at solving scalability issues of free-space quantum-optics experiments by means of optical fields confined in dielectric waveguides and resonant nanostructures such as photonic crystals (PhC). In particular, the efficient and coherent generation of single photons within direct-bandgap semiconductors constitutes a major step forward in realizing a photonic platform for quantum computation. To this end, InAs quantum dots (QDs) in GaAs, embedded in PhC [1, 5], have proven to be an excellent light-matter interface for near-unity efficiency single-photon generation [8, 9], nonlinear interactions [10, 11], and cavity quantum electrodynamics [12]. To achieve the high efficiencies needed for generating and routing photons, photonic integrated circuits have to be fabricated with highly precise micro- and nano-fabrication techniques. These techniques involve the direct writing of nanostructures using electron-beam lithography into a resist mask and the subsequent transfer to the substrate via anisotropic dry etching. The optical quality of the devices depends crucially on this last step, which is usually carried out using reactive-ion etching (RIE).

In RIE processes, the choice of the mask material is of utmost importance in order to etch features deeply into the substrate while keeping a high structural quality. In particular, the mask largely determines the selectivity of the process, i.e., the ratio between the etch rates of the mask and the semiconductor. For silicon photonic circuits the electron-beam resist is deposited directly on the substrate and used as a mask for dry etching, yielding good selectivity [13]. For III/V semiconductor etching, and in particular for PhC fabrication, it is more common to use intermediate layers, so-called hard masks, such as Si_3N_4, SiO_2, or metals, to improve the selectivity of small features [14–16]. There are situations, however, where introducing an additional mask layer is not desirable, especially when oxides or metals have been already deposited on the sample for other purposes, e.g., for the fabrication of superconducting single photon detectors [17]. In this letter we present a soft-mask process where a circuit is etched directly into a GaAs membrane through the patterned

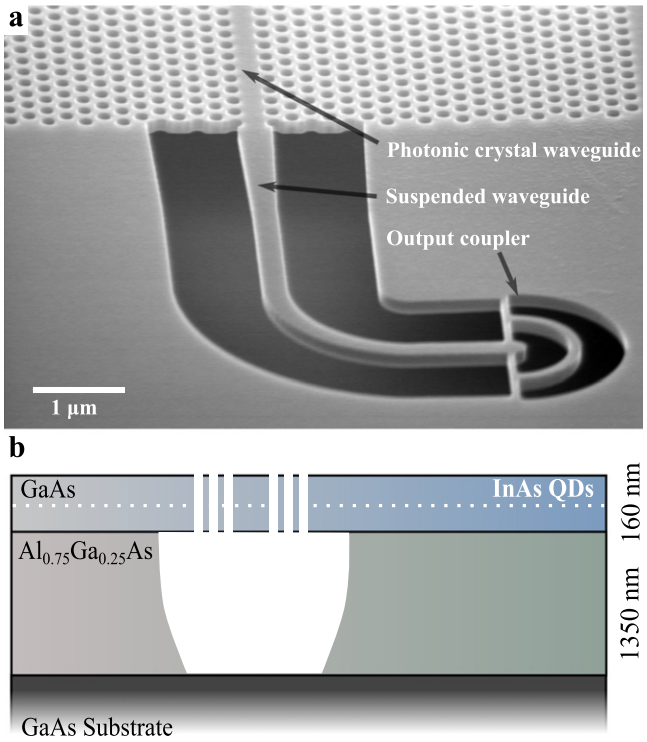

Figure 1. Integrated quantum photonic circuits in GaAs membranes. (a) Scanning electron micrograph of a PhC waveguide coupled to a suspended waveguide, fabricated in a GaAs nanomembrane. (b) Layout of the sample, showing schematically how the membranes have been patterned by dry etching and selective wet etching.

electron-beam resist. Unlike hard-mask processes, this method involves fewer fabrication steps, reduces the need for expensive deposition equipment and operates at lower temperatures.

We have developed a fabrication recipe that allows realizing circuits as shown in figure 1(a), composed of PhC waveguides, suspended waveguides and other passive components such as power splitters and out-couplers. Suspended PhC waveguides are ideal to achieve a high coupling efficiency between the emitter and the optical mode [9]. In this way, the GaAs layer forms a high-refractive-index membrane symmetrically surrounded by vacuum, providing a strong field confinement and suppressing the coupling between the QD and the lossy substrate modes [5]. Moreover, there is a significant mode mismatch between light propagating in PhCs and in GaAs ridge waveguides. Therefore the entire circuitry is fabricated on suspended membranes. In previous works [18, 19], the possibility to etch PhC on suspended slabs using soft masks has been discussed, but a detailed description of the etching process, including methods to properly clean the nanostructures from etching residues, is missing. This is particularly important because structural disorder in the form of surface roughness, polymer flakes, or other compounds deposited on the surface have detrimental effects on photonic circuitry. For example, structural disorder leads to unwanted sample-to-sample fluctuations in the resonance spectrum of nanoresonators [20] and has a dramatic effect on photonic-crystal waveguides in which disorder induces Anderson localization of light [21]. Here we provide a detailed discussion on how to minimize all possible sources of disorder and scattering to improve the overall circuit efficiency.

2. Experimental procedure

2.1. Sample preparation

The samples are grown by molecular-beam epitaxy on a (001) GaAs substrate with the material stack shown in figure 1(b). It consists of a 160 nm thick GaAs membrane with a layer of self-assembled InAs QDs located in the center. The membrane is grown atop a 1350 nm sacrificial layer ($Al_xGa_{1-x}As$, $x = 0.75$). Since the QD emission is centered around 940 nm at 10 K, the sacrificial layer thickness is designed so that light exiting from the couplers, see figure 1(a), is emitted preferentially towards the top, while keeping a sufficient distance from the substrate to avoid breaking the symmetry of the optical confinement in the membrane. The aluminum fraction in the sacrificial layer is chosen so that it can be easily removed by hydrofluoric or hydrochloric acid. We have found incomplete etching when $x < 0.7$ and excessive, uncontrollable undercut rates with $x > 0.8$. The sample is initially cleaned from dust and organic residues using, in sequence, acetone and isopropyl alcohol (IPA) and subsequently dehydrated at 185 °C for 5 min. The electron-beam resist ZEP520A is deposited by spin coating at 2000 rotations per minute and baked at 185 °C for 5 min on a hot plate to produce a mask thickness of 500–540 nm (measured by a spectral film-thickness analyzer). ZEP520A is chosen since it combines high resolution with good resistance to dry etching. The resist is patterned using a 100 kV electron-beam lithography tool (Elionix ELS-7000G) and developed in n-amylacetate for 1 min at 22 °C and rinsed in IPA for 10 s. PhC holes are exposed at a uniform dose of 300 μC cm^{-2} whereas the remaining features are exposed at a lower dose of 230 μC cm^{-2}.

2.2. Dry etching

To etch the patterns vertically through the membrane, a RIE tool (Plasmalab 100) from Oxford Instruments, equipped with an inductively coupled-plasma (ICP) source, is used. The system allows monitoring the remaining resist thickness in real-time using laser interferometry. We have observed that when the resist thickness in the homogeneous (un-exposed) part of the mask is reduced to less than 200 nm, the etched features tend to enlarge and erode around the sidewalls. This effect stems from the fact that, in the proximity of the exposed patterns, the resist etches faster, leaving the GaAs surface exposed to the plasma. Using the reflectance signal from the resist, it is possible to stop the process before this phenomenon occurs. Moreover, to avoid excessive heating and resist re-flow (occurring at around 140 °C) due to the reactive plasma, it is important to establish a good thermal contact between the sample and the electrode. For this purpose, the sample is glued to a Si carrier wafer using thermally

conducting and removable adhesives (fluorinated lubricants or wax) and the electrode temperature is lowered to 0 °C. Helium flow is introduced to attain a good thermal contact between the carrier wafer and the electrode table throughout the entire process. A plasma chemistry based on BCl_3, Cl_2 and Ar is used [18]. Chlorine is the main etching agent while the boron tetrachloride is used for side-wall passivation and argon for dilution [22, 23]. Additionally, Ar can enhance the physical etching (sputtering) and reduce the sidewall roughness [24]. The 65 mm diameter ICP coil power is set to 300 W since higher values lead to lower selectivity. The electrode RF power is adjusted so that the voltage between the RIE plate and the chamber walls is approximately around 300 V and that the plasma is stable. For most of the experiments, an RF power of 47 W is used. The chamber pressure is initially set to a strike pressure of 25 mTorr and then rapidly lowered to the desired value once the plasma has ignited. We have found that an optimum etching profile is obtained when the $BCl_3/Cl_2/Ar$ flow ratio is set to 3/4/25 sccm, respectively and the chamber pressure is 4.7 mTorr.

2.3. Sacrificial-layer undercut

After plasma etching, the residual resist layer is removed by soaking the sample for 10 min in n-methylpyrrolidone (NMP) at 60 °C. Once cooled, NMP is removed by washing it in IPA. Two acids have been tested for the selective removal of the $Al_{0.75}Ga_{0.25}As$ sacrificial layer, namely a 10% solution of hydrofluoric acid (HF 40% mixed 1:3 with water by volume) and a cold (<5 °C) hydrocloric acid solution (HCl 37% mixed 4:1 with H_2O) [25]. The HF etch rate is relatively high (approximately 65 nm s^{-1} lateral etch rate) whereas HCl provides a much lower rate (~3 nm s^{-1} depending on the solution temperature and Al content). To properly clean the sample from residues left by wet and dry etching, a 60 s hydrogen peroxide dip followed by deoxidation in a 20% potassium hydroxide solution (25 g of KOH dissolved in 100 ml water) is used. Suspended GaAs structures consisting of thin membranes usually show low mechanical stiffness, which can lead to a collapse onto the substrate due to capillary forces and subsequent inter-solid adhesion [26]. To avoid such stiction failures, attention is paid throughout the entire wet etching procedure to keep the surface covered by a liquid droplet until the end of the process. Then the sample is dried either by immersion in IPA followed by evaporation or by a supercritical point dryer in carbon dioxide.

3. Results and discussion

3.1. Dry etching

The samples are patterned with PhC waveguides (hole-to-hole distance 245 nm) coupled to suspended waveguides to simultaneously inspect the quality of different aspect-ratio features (defined as the average feature size over mask thickness). Plasma etching of small aspect-ratio features usually causes what is known as RIE depth lag, i.e. a correlation between the feature size and its etch depth. This implies that the optimum etching parameters depend on the feature size. Insufficient etch depth leads to incomplete penetration through the membrane and prevents the subsequent undercut of the membrane. The ICP-RIE process is optimized starting from values in the literature [18, 23]. The parameter space has been narrowed down by optimizing the $BCl_3/Cl_2/Ar$ ratio first and then by studying the effect of the chamber pressure and Ar flow only. Two processes have been optimized, one dedicated to vertical etching of PhC, and one for deeper etching of large features. In figure 2 these two recipes are compared in terms of etch depth and quality. Higher pressures (6 mTorr) lead to significantly higher selectivity, but more curved sidewall profiles. This is visible in particular when examining the cross-sectional profiles of PhC holes by scanning electron microscopy (SEM) as shown in figures 2(a)–(d). To achieve a better verticality the pressure is reduced to 4.7 mTorr while the Ar flow is increased to control the sidewall roughness and the selectivity. As the pressure is reduced, physical etching dominates over chemical etching, resulting in lower selectivity. With these settings the resist etch rate is on average around 280 nm min^{-1} while the total etching time is between 45 and 55 s depending on the initial resist thickness. The smallest holes that can be etched deeper than 160 nm (the membrane thickness) have a radius

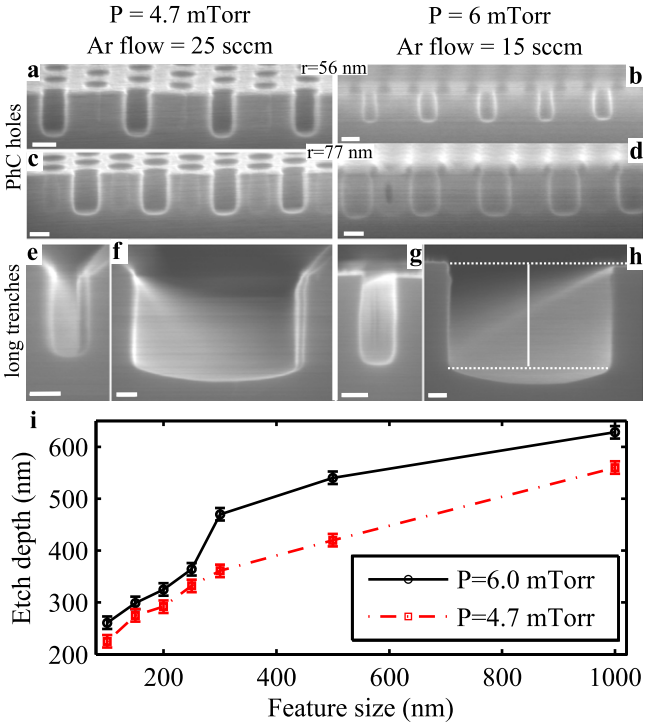

Figure 2. Optimization of dry-etching parameters. (a)–(h) Scanning electron micrographs of dry-etched GaAs membranes with different patterns. The process with low (high) pressure and high (low) Ar flow is shown to the left (right). (a)–(d) PhC holes with different radii and (e)–(h) cross-section of long trenches with different widths (100 nm and 1 μm). (i) Etching depth as a function of the trench size for two etching conditions. The depth is a function of the feature size are extracted as indicated in (h) by solid and dashed lines, respectively. All scale bars are 100 nm.

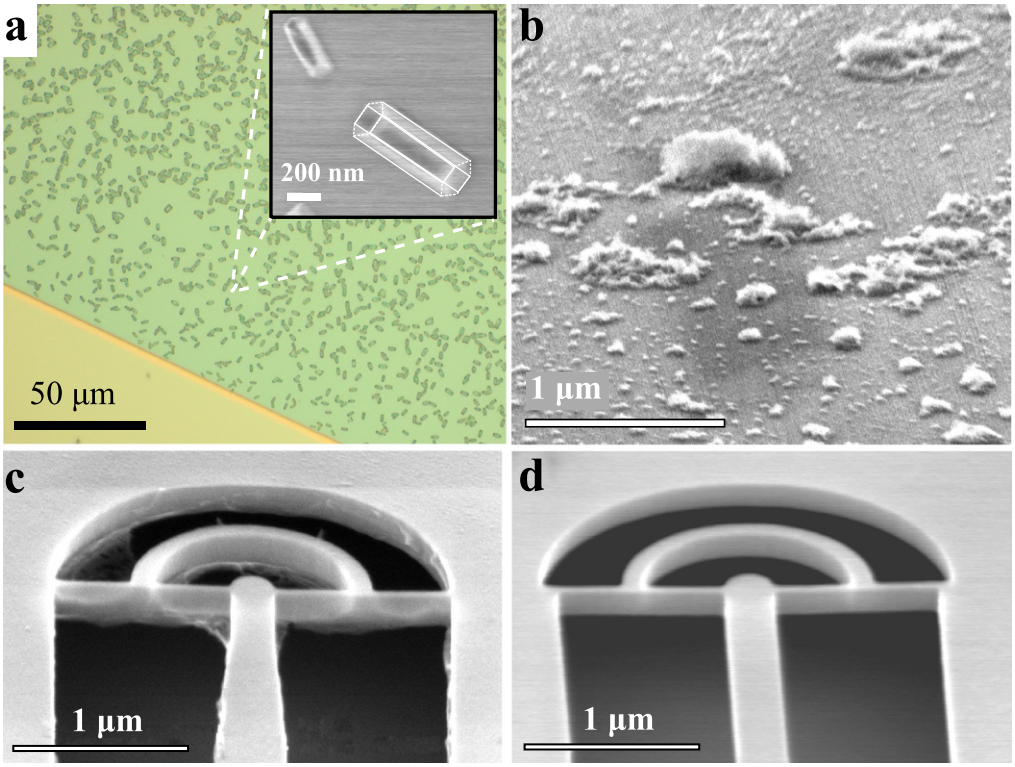

Figure 3. Removal of residues from etching leaving nanostructures of high structural quality. (a) Optical microscope image of AlF_3 crystals. Inset: SEM micrograph of the crystals where the crystalline structure has been outlined with solid white lines. SEM micrographs of (b) Al $(OH)_3$ residues on GaAs, and (c) debris of a thin, probably carbon-rich, film left by dry etching sticking to an output coupler. (d) Same as (c), after the treatment with H_2O_2 and KOH as described in the text.

of 56 nm and a corresponding etch rate of approximately 190 nm min^{-1}, resulting in a selectivity (GaAs etch to mask) of ∼2:3. For larger features such as the trenches shown in figures 2(f) and (h), the selectivity grows beyond 2:1. Figure 2(i) summarizes the etch depth as a function of the width of long trenches whose cross-sections are shown in figures 2(e)–(h) for the two recipes. As expected, the 6 mTorr recipe produces deeper features and it is thus more suitable for samples containing large non-periodic features where a deeper etching is needed. For PhC etching, however, the low-pressure recipe yields better results in terms of sidewall smoothness and verticality.

3.2. Wet etching

To reduce losses due to scattering in waveguides, it is crucial to properly clean the devices after wet etching. Several residues are observed on the fabricated structures after their release, especially when HF is used to remove Al(Ga)As. Most of the byproducts of Al(Ga)As and HF are gaseous or soluble in water [27] but we have noticed that solid compounds such as aluminum trifluoride (AlF_3), aluminum hydroxide ($Al(OH)_3$), and other amorphous residues caused by dry etching may be deposited at the bottom of the substrate and around the etched features. AlF_3 is identified by its crystalline structure as shown in figure 3(a) and it can be easily dissolved by a 10 min rinse in water. $Al(OH)_3$ residues, see figure 3(b), are sometimes observed as a product of HF vapors and can be removed by a dip in 20% potassium hydroxide. Figure 3(c) shows an amorphous residue that sticks to the edges of the released GaAs structures and which is always observed at the end of the wet etch process. Such fragments of what appears to be a thin organic layer cannot be removed by further HF etching. Moreover, it is also observed after HCl etching, indicating that it is more likely a product of dry etching. To investigate the origin of this compound and, more importantly, ways of removing it, different cleaning steps before and after the HF undercut are performed. Using basic or acidic de-oxidizing solutions (such as dilute phosphoric acid, dilute hydrocloric acid, potassium hydroxide or ammonium hydroxide) does not help in removing the substance. Instead, a single digital etching cycle [28], which consists of 60 s immersion in concentrated hydrogen peroxide (H_2O_2 30%) followed by a 60 s water rinse and 120 s etching in 20% potassium hydroxide, can remove the residues completely, leaving a smooth surface as shown in figures 3(d) and 4(a). The use of a soft mask in very hot plasmas typically leads to resist damage and the formation of carbon-rich films, which are hard to strip afterward. These residues may redeposit inside the etched features during the dry etching or later on, during the resist stripping in NMP. We speculate that this is the case for the residue in figure 3(c). This hypothesis is supported by the fact that applying an oxygen plasma seems to be beneficial, although not sufficient, to removing the debris of this carbon film. Additionally, we have noticed that using concentrated H_2O_2 alone, followed by a water rinse,

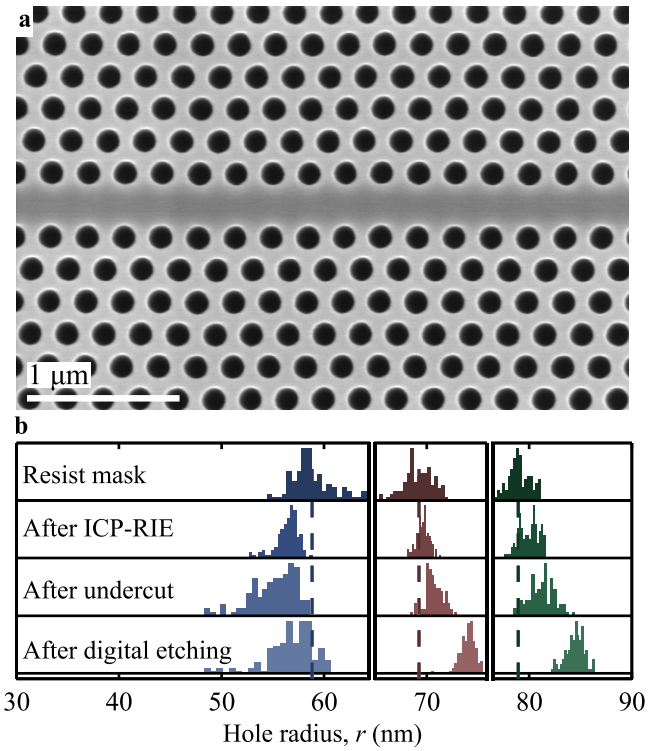

Figure 4. Reproducibility and accuracy of PhC patterning. (a) SEM micrograph of a PhC waveguide (PhC lattice parameter 245 nm and radius $r = 70$ nm). (b) Statistics of the hole radius distribution before and after each etching step. The vertical dashed lines indicate the average radius value in the mask. The original mask design values are 61 nm (blue), 70 nm (red), and 77 nm (green).

removes the residue completely, suggesting that the carbon-rich film is oxidized by peroxide and turned into volatile compounds such as CO_2. Clearly, the use of peroxide has the side-effect of oxidizing GaAs and thus necessitates a final de-oxidation step. Among the various de-oxidizing agents available, KOH has the additional advantage of performing a thorough cleaning of other residues such as $Al(OH)_3$.

3.3. Effects of the process steps on the hole size

The most delicate aspect in fabricating PhC waveguides is the accuracy in the hole positioning and radius, which is mainly achieved using state-of-the-art electron-beam-lithography tools. In particular, the accuracy in reproducing a given hole radius allows positioning the photonic band edge to the correct wavelength relative to the QD emission. To this end, the effects on the hole size due to processing are analyzed. Figure 4(b) summarizes the results of a statistical analysis of SEM micrographs of PhCs with different radii after each step. All images have been acquired with the same settings and equalized to uniform brightness and contrast. An enlargement of 2–3 nm is observed after the digital etching. This is in the range expected from the literature [28] and can easily be compensated by proper mask design. We note additionally that the dry-etching process does not visibly enlarge the hole radius. This indicates that the process is very accurate in transferring a pattern from a soft mask into GaAs. From figure 4(b) we also notice that when the holes in the mask are smaller than 60 nm, they tend to have a larger distribution, which partly obscures the enlargement from step to step. This higher radius spread is probably due to incomplete opening in the resist mask and has to be corrected by adjusting the exposure dose in the electron-beam lithography.

4. Summary and conclusions

We have developed a nano-fabrication process for quantum photonic integrated circuits involving suspended and PhC waveguides without the deposition and etching of a hard mask. Particular attention has been devoted to achieving vertical holes in the ICP-RIE process and to clean all residues from dry and wet etching. A good accuracy in reproducing PhC patterns has been observed and it is confirmed by a statistical analysis of the hole-radii distribution. The process described here could be extended to fabricate more complex devices involving electrical gates or on-chip superconducting detectors. In fact, the low-temperature process strongly minimizes the chances of damaging metallic contacts or sputtered films. Additionally, HCl or HF can be used almost interchangeably depending on the required material selectivity, so that dielectrics such as Si_3N_4, SiO_2 or flowable oxides could be used as well, e.g., to protect sensitive parts of the chip during dry or wet etching. Finally we should like to mention that our fabrication process is relevant for a range of applications of GaAs nanomembranes, e.g., quantum opto-mechanics [29, 30].

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