BACHELOR PROJECT

Fabrication and Electrical Characterization of Semiconductor Nanowire Devices

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1 Abstract

1.1 English

In this report several InAs-core nanowire based devices meant for electrical characterization of nanowires are successfully created through Electron Beam Lithography fabrication utilizing state of the art equipment. The fabrication process is documented and described. The nanowires are electrically characterized at three different temperatures: 299 Kelvin, 50 Kelvin and 25 Kelvin. Through 4-probe measurements the intrinsic resitivity of the nanowires are measured to in the order of $10^{-4}\Omega/m$. A global Silicon/Silicon-Oxide back gate is used to perform field effect mobility measurements. The mobilities found are lower than expected. Reasons for these low mobilities are discussed and from the experiences made in this report, proposals for design improvements for future investigations are given.

By measuring aluminum etched InAs-core and InAs/GaSb-core nanowires in comparison with control nanowires that have not seen aluminum, this report will try to document the effect aluminum etching have on the mobility of the nanowires. However this report could not document a clear effect of the aluminum etching.

1.2 Dansk

I denne rapport bliver adskillige InAs-kerne nanowire-baseret devices, designet til elektrisk karakterisering af nanowires, fremstillet ved hjælp af Electron-Beam-Lithography-fabrikation under brug af det nyeste tekniske udstyr. Fabrikationsprocessen bliver dokumenteret og beskrevet. Nanowirene bliver elektrisk karakteriseret ved tre forskellige temperaturer: 299 Kelvin, 50 Kelvin og 25 Kelvin. Ved hjælp af 4-probemålinger bestemmes den intrinsiske resistivitet af nanowirene til at være af størrelsesordenen $10^{-4}\Omega/m$. En global Silicium/Siliciumoxid back gate bliver brugt til at udføre field-effect-mobilitetsmålinger. De fundne mobiliteter er lavere end forventet. Grunde til disse lave mobiliteter bliver diskuteret, og ud fra erfaringerne gjort i denne rapport foreslås designforbedringer til fremtidige undersøgelser.

Ved at sammenligne målinger af aluminiumsætsede InAs-kerne og InAS/GaSb-kerne nanowire med kontrolnanowires, som ikke har være i kontakt med aluminium, vil denne rapport prøve at dokumentere hvilken effekt aluminiumsætsningen har på nanowirenes mobilitet. Dog kunne denne rapport ikke dokumentere en klar effekt af aluminiumsætsningen.

Contents

2   Introduction

The fast growth in electronics have given rise for demands of smaller and smaller electronic devices. Here semiconductor nanowires show promising signs of becoming the key to the design of next generation electronic devices[1], given their unique possibility of controlling their physical properties such as dimension, composition and doping during growth[10].

In order to utilize the nanowires fully it is needed to know their electrical properties precisely. Through electron beam lithography it is possible to create electron circuits of the scale of the nanowires and thereby creating devices for characterizing the nanowires. The goal of this bachelor project is to successfully create such nanowire devices and perform an electrical characterization of the nanowires.

Two types of measurements will be performed: a field effect mobility measurement to determine the mobility of the nanowires, and a 4-probe measurement to determine the intrinsic resistance which makes it possible to extract the resistivity of the nanowire. These two properties of the nanowire will be utilized to calculate the electron density.

In the resent years great efforts in making a topological quantum computer have been made. Here nanowire-based superconducting qubits have showed very promising results[2] of becoming a scalable solid state solution for building a quantum computer.

These nanowire-based qubits require small superconducting aluminum "islands" on the surface of the nanowire. The "islands" are made by etching away chosen parts of the aluminum shell of the nanowires. At Center for Quantum Devices (Qdev) the etchant Aluminum Etchant type D is used for etching.

It has been shown that this etching process creates tiny cracks and other lattice defects in the semiconductor crystal of the nanowire, and therefore it is suspected that the etching process will have an effect on the electrical properties of the nanowire. This report will try to document this effect by measuring the resistivity and mobility of two type of nanowires exposed to the etchant: Qdev343 InAs/Aluminum half shell and Qdev297 InAs/GaSb/Aluminum half shell and compare the result with measurement of two nanowires of the same semiconductor core, but which have never had an aluminum shell: Qdev1 InAs and Qdev287 InAsGaSb. These nanowires will act as control. In this way it is the hope that possible differences in the mobility and resistivity coming from the etchant can be proven. To the best of this author's knowledge, the effects of the aluminum etching on the electrical properties of nanowires have not previously been documented.

All of the four nanowires will be placed on the same chip and go through the same fabrication process except for the aluminum etching, to ensure that the nanowires receive as similar treatment as possible.

The measurements will be done at three different temperatures: 299K, 50K and 23-25K.

The outline of the thesis is as follow: The first section present general theory of semiconductors, mobility and resistivity. The second section describes the fabrication process of making these devices. The third section contains an introduction to the measuring methods used in this report and a subsection with some complication that emerged during the measurement. The fourth section presents and discuss the results. The fifth section is the conclusion of the report. The report ends with a section with suggestions of improvement of the design and ideas for further investigations.

2.1   Acknowledgements

3 Theory

The nanowires (hereafter written as NW) used in this report are made out of semiconductor crystal. Semiconductors have electric properties that makes them unique from conductors and insulators, this becomes apparent if we look at band structures of semiconductors (figure 1). For an intrinsic semiconductor the Fermi level lies in the middle of the bandgap between the valence and conducting band[3]. The Fermi level comes from the Fermi-Dirac distribution:

$$f(E) = \frac{1}{e^{(E-\mu)/(k_B T)} + 1} \tag{3.1}$$

Where μ is the Fermi level, k_B is the Boltzmann constant, T the temperature and E is the energy.

The Fermi-Dirac distribution is a probability distribution which gives the probability of an electron occupying an energy state. The Fermi level marks the energy where there is a 50% chance of a state being occupied.

For temperatures approaching zero Kelvin the Fermi-Dirac distribution is an sharp division where states at energies higher than the Fermi level have zero percent chance of being occupied. This makes the semiconductor an insulator at 0K (see figure 1a))[4].

At high temperatures for which $E - \mu \gg k_B T$, the Fermi-Dirac function approximates into: $f(E) \cong e^{-(E-\mu)/k_B T}$. This increases the "tail" of the Fermi-Dirac distribution, so that states in the conducting band starts getting filled making the semiconductor electrically conducting (see figure 1b)). The width of the Fermi-Dirac "tail" is around $\sim k_B T$. Unlike metals, the conductance of semiconductors will generally increase as temperature increases.
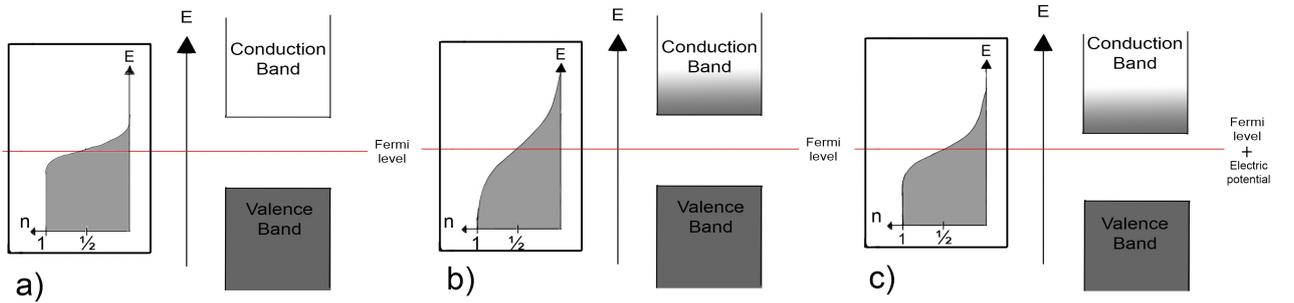

Figure 1: A schematic illustration of the band diagram and Fermi-Dirac distribution of a semiconductor in three cases. The insert on the left shows the Fermi-Dirac distribution with energy along the y-axis and probability along the x-axis. The fermi level (red line) intercepts the graph at 0.5. On the right the band diagram is shown. The fermi level lies in the band gap. The color indicate if the band is filled. Case a) is the low temperature case. Here the valence band is full and the conduction band is empty. The semiconductor is non-conducting. Case b) is at a higher temperature than a). The "tail" of the Fermi-Dirac distribution has increased such that the conduction band is getting partially filled. In this case the semiconductor is electrically conducting. In c) an electric potential has been added to the original fermi level. The accumulated fermi level has moved closer to the conduction band, such that the semiconductor is electrically conducting.

What makes semiconductors especially useful in electronics is that their Fermi level and therefore their conductance can be modulated. The modulation is either done by doping the material or by gating the material, as will be done in this report.

Gating is when one effects the semiconductor with an external electric field by applying a voltage to a "gate", which is an electrode placed close the semiconductor, here in this report: a silicon back gate. The external electric field causes either the valence or conducting band to move closer to the Fermi level, and therefore either decreasing or increasing the conductance of the semiconductor (see figure 1c)). In this report I am able to completely deplete the NWs at low temperatures.

Gating is utilized in Field Effect Transistors (FETs) such as JFETs, MOSFETs and many other types of FETs. When using nanowires the devices are called nanowire field effect transistors (NWFET).

3.1 Mobility

In the Drude model a conducting material have a "sea" of electrons moving freely around. If there is no applied electric field the electrons will move around at random. This means that the total current is zero, since all the random contributions will cancel each other out. When an external electrical field E is applied the electrons will feel a force acting upon them:

$$\vec{F} = m\frac{d\vec{v}}{dt} = -e\vec{E} \tag{3.2}$$

This is the Lorentz force with no magnetic field. Here m is the mass of the electron, -e is the elementary charge of the electron and v is the velocity. Solving for the momentum one finds that: $m\vec{v}(t) = -e\vec{E}t$. Due to different scattering mechanisms, such as impurity scattering, phonon scattering and other types of scattering, the electrons will lose momentum. After a certain time τ, called the momentum relaxation time, the electrons will be in a steady state resulting in them moving at a constant drift velocity v_d:

$$\vec{v_d} = -\frac{e\vec{E}}{m}\tau \tag{3.3}$$

The mobility μ is defined as the ratio of the drift velocity and the magnitude of the electric field:

$$\mu = \frac{|v_d|}{|E|} = \frac{e}{m}\tau \tag{3.4}$$

It can be seen that the mobility is directly proportional to the momentum relaxation time, which again is dependent of the different scattering mechanisms in the material.

There are many different types of scattering in a material and they all contribute to a total momentum relaxation time, as by Matthiessen's rule:

$$\frac{1}{\tau} = \frac{1}{\tau_{impurities}} + \frac{1}{\tau_{phonons}} + \frac{1}{\tau_{coulomb}} + \frac{1}{\tau_{lattice\ defects}}... \tag{3.5}$$

To increase the mobility one can try to decrease one or more types of scattering, meaning increasing the momentum relaxation time belonging to that type of scattering. Phonon scattering, for example, is temperature dependent, so decreasing the temperature will increase the $\tau_{phonons}$.

As mentioned in the introduction, part of this report's goal is to determine the effect the aluminum etching has on the mobility. Aluminum etching is needed to create those superconducting Al-"island" needed for quantum computing, but there has also been concerns that the strong etchant will create tiny cracks in the semiconductor material. This will likely increase the scattering due to lattice imperfections and therefore decrease the mobility of the NW.

Through field effect measurement of the mobility this report will try to investigate whether this effect can be measured.

3.2 Resistivity and the Electron Density

Returning to the case of applying an electric field to a conducting material the end result will be a current running through the material. When the electron density is n and the charge of an electron is q=-e, the current density J is given by:

$$\vec{J} = -ne\vec{v_d} = \frac{ne^2\tau}{m}\vec{E} = \sigma\vec{E} \tag{3.6}$$

Here we have defined the electrical conductivity as $\sigma = \frac{ne^2\tau}{m}$. The resistivity ρ is defined as:

$$\rho \equiv \sigma^{-1} = \frac{m}{ne^2\tau} \tag{3.7}$$

Inserting equation 3.4 into the expression I find that the electron density is given by:

$$n = \frac{1}{\rho \mu e} \tag{3.8}$$

In this report I will measure the resistivity ρ of the NWs through 4-probe measurements and measure the mobility μ through field effect measurement, and then finally insert the results into equation 3.8 to find the electron density of the NWs. The experiment will be repeated at three different temperatures: 299K, 50K and 25K. The hypothesis is that the effects of the Aluminum etching become more prominent at lower temperatures, because of the reduced phonon scattering, which is often dominant at room temperatures.
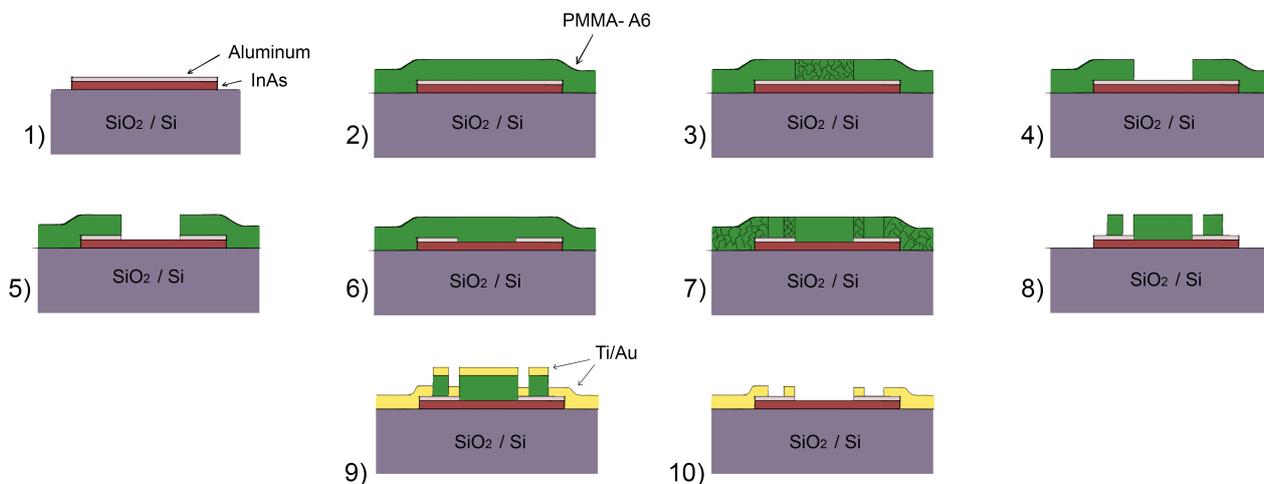
4   Device Fabrication

Figure 2: The figure shows the multiple steps in the fabrication process. In the figure a NW with aluminum half shell is shown; for NW without aluminum half shell step 3)-6) is unrequired. The proportions and scale are not accurate. 1) With the MicroManipulater the NW is placed on the silicon chip with 500nm thick SiO$_2$ layer. 2) A layer of Pmma-A6 resist is spun onto the chip. 3) In the Raith e-line the windows are exposed. 4) The chip is developed with PMMA-A6 developer MIBK (1:3). The chip is then cleansed in IPA and MQ-water and then ashed for 60 seconds. 5) The exposed aluminum is etched away with Aluminum Etchant Type D. 6) All of the old resist is removed with 60°C hot NMP and new PMMA-A6 resist is applied. 7) Contacts are exposed in the e-line. If the design has a side gate, that gate will be expose here as well. 8) Development is done as described in step 4). 9) The chip is loaded into the AJA-system, exposed to RF-miling and is then metalized with 5nm Ti and 200nm Au. The contacts are depicted as lying on top of the NW, in reality they go around the NW. 10) Finally the lift off is done in 60°C hot NMP and the chip is then cleansed in acetone, IPA and MQ-water.

The devices in this report is fabricated using electron beam lithography (EBL), a highly advanced technic that is widely used when it comes to creating nano scale circuits. The great advantage of EBL is the very high resolution of electron exposures and can make extremely fine patterns. The resolution also depends on the type of resist. In this report polymethyl methacrilate (PMMA) is used which is one of the highest resolution resist available[6]. In this report details of ∼50nm in thickness was made.

The fabrication process is complicated and involve many steps. A simple error in one of these steps will follow along the whole process and in worst case ruin the entire device. The first two and a half months of this project was therefore dedicated to learn the fabrication process and how use and handle the machines and chemicals needed for fabrication. It took two failed attempts before successful devices were made. The fabrication takes place in a clean room, since it is very important that the environment is clean and close to dust free.

In this section the fabrication process will briefly be described in seven parts. Figure 2 shows the basics of the fabrication process.

The nanowires used in this report are:

- Qdev1 InAs

- Qdev343 InAs/Al (Al half shell(2 facets))

- Qdev287 InAs/GaSb (GASb full shell)

- Qdev297 InAs/GaSb/Al (GaSb full shell, Al half shell(2 facets))

Placing the NW
The Micro Manipulator with 0.1 μm needles is used to transfer the nanowires from their growth wafer and place them on the chip. Uniquely designed reference marks on the chip makes sure that the optical images of the wires can be matched with the design in DesignCad Pro.

After the placing of the NW, polymethyl methacrilate (PMMA)-A6 resist is spun onto the chip at 4000rpm for 45 seconds, this will give a 300nm thick layer of resist. Hereafter the chip is hard baked at 185°C for 2 minutes. An optical microscope is then used to take images of the nanowires.

Drawing and Exposing the Windows
In DesignCad Pro the optical images are matched with the base design of the chip, using the reference marks as guidance as previously mentioned. The first part of the design process is drawing the windows in a separate layer for those NWs with aluminum half-shells. The windows will be holes in the resist. This ensures that only the part of the NWs that lies inside the windows will be exposed to the Aluminum Etchant. The width of the windows are 1 μm for short nanowires and 2 μm for some of the longest NWs.

In chip is hereafter transferred into the Raith e-line. Under low pressure ($1.13 \cdot 10^{-6}$ mbar) the chip is exposed by an electron beam at 20kV. The higher the acceleration voltage, the finer patterns can be made. The electrons will chemically change the exposed resist.

Pmma-developing.
The chip is developed in the PMMA developer Methyl Isobutyl Ketone (MIBK) diluted 1:3 in isopropanol (IPA) for 1 minute. The developer will remove only the exposed parts of the resist. Then the chip is cleaned in isopropanol (IPA) for 30 seconds and then MQ-water for 30 seconds.

The chip is then loaded into the Asher that will expose the chip to an Oxygen-plasma for 60 seconds. The resist is an organic material meaning that it will react with the highly reactive Oxygen-plasma forming H_2O, CO_2, ect. The Asher will, for an expose time of 60 seconds, remove about 11 nm of resist. These three steps is done to make sure that all of the exposed resist is removed, before the NW is exposed to the Aluminum etchant.

Aluminum Etching.
The chip is then lowered into 47°C warm Aluminum Etchant type D (Al Etch) for 10 seconds. The Al Etch is a very strong acid and both the temperature and the expose time are crucial for the success of the etching. The 10 second exposure time was chosen because other experimentalista at Qdev have had success with this exposure time. The temperature is important since the etching rate of the acid varies with temperature. The Al Etch has it highest etching rate, 200 Å/sec at 50°C and will start to break down at higher temperatures[5]. After the etching the chip is then cleansed in 47°C warm MQ-water and then MQ-water at room temperature. Experiences of other groups show that, for the etching to be successfull, it is important that the chip is firstly cleansed in MQ-water that has the same temperature as the Al Etch.

After the etching process all of the resist is removed by lowering the chip into N-Methyl-2-Pyrrolidone (NMP) at 60°C for 50 minutes. The chip is then cleansed in Acetone, which also is a resist remover, IPA and then MQ water.
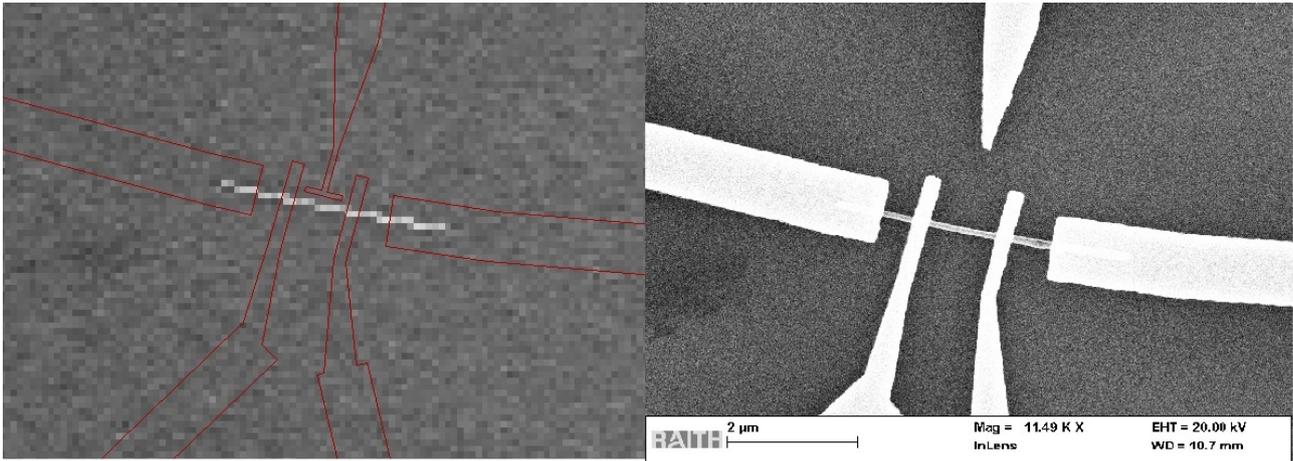
Figure 3: Comparison of the design of the contacts and side gate in DesignCadPro and the end result. The device pictured is Qdev297 01 an InAs/GaSb/Al-etched nanowire.

Drawing and exposing the contacts

When all resist is removed the chip is once again loaded into the e-line, to utilize the SEM to take pictures of the NWs to see if they should have moved during the previous processes. The SEM also provides much sharper images than the optical microscope, so that the contacts can be placed more precisely. The SEM pictures are quickly taken with the image software to minimize the deposited Carbon from the SEM.

In DesignCad Pro the SEM images are matched with the chip design using the reference marks. The four contacts are drawn on a separate layer. Some devices are also designed with a side gate sitting between the two inner contacts. The side gate will be made of the same metal as the contacts, but unlike the contacts it will not touch the NW, but sit very closely next to it. The side gates are made very thin in order to fit between the inner contacts and therefore they are very fragile and are easily removed during the "lift off"-process. Unfortunayely no side gates survived the fabrication, most likely because of the sonication during the lift off process. The side gates could have provided an alternative way of gating the devices since they are local compared to the global back gate.

In figure 3 to the right a SEM photo of InAs/GaSb/Al-etched device Qdev297 01 can be seen. To the left is the design drawn in DesignCadPro. As it can be seen the T-formed side gate is missing from the end result.

After designing the contacts, Pmma-A6 resist is once again spun onto the chip. The process is the same as described earlier. The chip is loaded into the Raith e-line where the contacts and side gates are exposed. The chip is then developed in MIBK (1:3), cleansed in IPA and MQ, and ashed for 60 seconds in the same manner as described earlier.

RF-Milling & Metallization.

The RF-milling and metallization is done inside an AJA-system, which is essentially a big vacuum chamber that allows me to do these two steps at very low pressure: $3 \cdot 10^{-8}$mTor. During the ashing of the NWs and just by carrying the chip around in the cleanroom, the NWs will inevitably have been exposed to oxygen, which reacts with the aluminum forming Al_2O_3 or just sits inertly on the semiconductor parts of the NW. This prohibits a good ohmic contact and needs to be removed. This is done by RF-milling, a milder form of Ion milling, which removes the oxygen sitting on the semiconductor parts of the NW, but not the Al_2O_3.

RF-milling works by exposing the chip to an Ar-plasma, which is ignited at 25 Watts and then slowly raised to 49 Watts by 1 Watt per second. The Ar-gas is kept at a constant pressure, 6 mTor. Too low a pressure and there will not be enough argon, too high and Ar-Ar collisions start to hinder the process. The chip is exposed for 10 minutes.

After the RF-milling the metallization can start. An electron beam is used to slowly heat up the desired metal which then starts to evaporate. Once the desired evaporation rate is reached and is

steady, the substrate shutter is opened and the chip is exposed to the evaporated metal. When the desired height of metal has settled on the chip, the substrate shutter is closed, and the electron beam is slowly turned off and the metal cools down for 2 minutes, before moving to the next metal. For the contacts and gates I first evaporate 5 nm of titanium and then 200 nm of gold. The titanium is needed to make a good ohmic contact to the NW.

In figure 2 9) the contacts are depicted as lying on top of the NW. In reality the contacts go around the NW, so this means that there also is direct contact between the semiconductor and the metal contacts.

The Lift Off.
The final step is the lift off. The chip is lowered in NMP at 60°C for 50 minutes. This dissolves all the resist and the titanium and gold that previously was lying on the resist will be floating on top of the NMP. To remove all of the gold from the finer details of the design, the chip is hold tight with a tweezer while rinsed with acetone. It is important that the chip always is kept submerged in liquid. If the gold dries in air it will be impossible to remove. If there is doubt whether all of the gold has been removed, the chip can be examined through an optical microscope, though the chip must be kept submerged in acetone all the time. The chip is then moved to the sonicator and sonicated the lowest power (30%) at the highest frequency 80Hz to remove the rest of the gold. Since the NW is kept in place by the contacts there is little chance they will fall off the chip. However small features of gold can fall off and this is probably what happened to the side gates.

After the lift off the chip is cleansed in IPA and MQ and then ashed for 60 seconds.

5 Method of Measuring

All the electrical measurements takes place in the probestation. The probestation has a center chamber where the chip is put. The air can be pumped out of the chamber by the pump attached to the probestation. When the chip is unloaded the chamber is flooded with nitrogen before opened. Liquid helium is used to cool down the probestation when the low temperature measurements are made.

The probestation has six probes with small needles. These needles can either be grounded or connected to a current/voltage source, in this report a Keithley 2400, or multimeter, a Hewlett Packard DMM. Each contact of my devices are connected to a contact pad. By turning the knobs of the side of the probestation, the needles make contact with the contact pads and this is how the device is connected to the Keithley and HP DMM.

Pumping out the probestation takes about 1.5 to 2 hours and cooling down the probestation take another 1.5 hour. Moving the needles around using the knobs are also a slow process. Therefore the three measurements at the different temperatures 299K, 50K and 23-25K were made on separate days. The pumping time varies for each measurement. Unfortunately the pressure of the probestation was not noted.

5.1 Measuring the Field Effect Mobility

The mobility μ is measured by a field effect measurement. When doing such a measurement the result is referred to as the "field effect mobility" in this report denoted as μ_{FE}.

During the field effect measurements the system is set up as in figure 4. Using a Keithley 2400 Sourcemeter, a bias voltage V_{SD} is applied to the first inner contact (i.e. the source) while the other one is grounded (i.e. the drain). The current through the NW, I_{SD} is measured by the same Keithley. A second Keithley is used to apply a gate voltage V_g to the back gate of the probestation, in the figure 4 symbolized as the plate beneath the device. The Keithley produces a voltage with an accuracy of $5\mu V$ and measure the current I_{SD} with a resolution of 1pA[8]. Figure 5 shows a graph of the mobility measurements of device Qdev1 4a at room temperature, 299K.
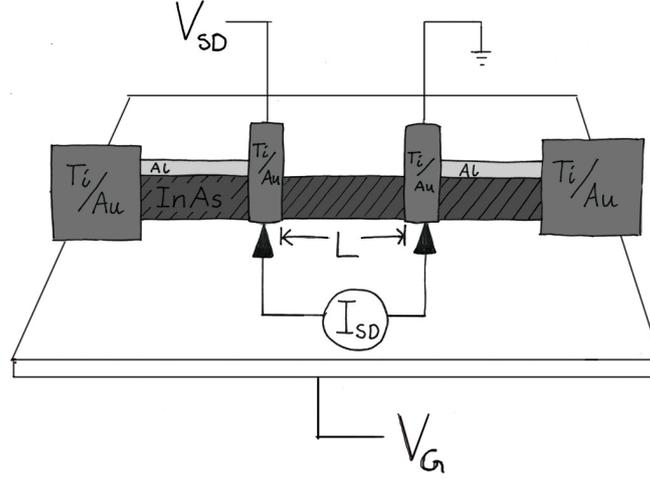
Figure 4: A schematic illustration of the field effect measurement setup. A bias voltage V_{SD} is applied to one of the inner contacts, while the other contact is grounded. A gate voltage V_G is applied to the global back gate an swept through an interval, for the 299K measurements in a ± 10V range. The current I_{SD} running through the contacts and its response to the changing gate voltage is measured with an amperemeter.

The transconductance g_m is defined as the slope of the graph:

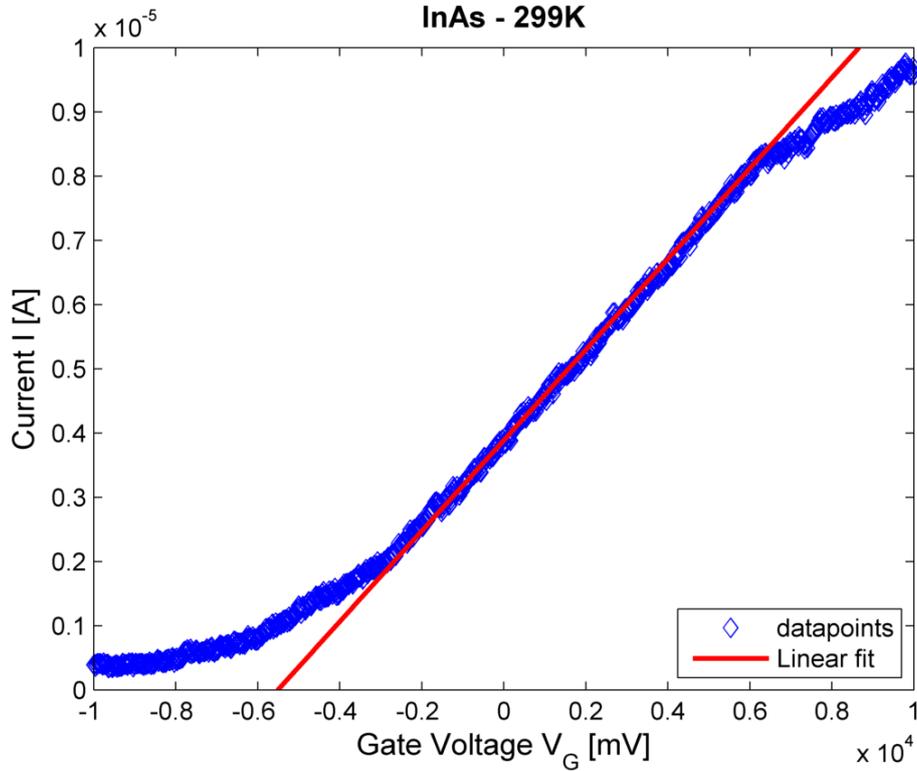$$g_m \equiv \frac{\partial I_{SD}}{\partial V_g} \qquad (5.1)$$

Figure 5: Mobilty measurement of Qdev 1 4a InAs NW at room temperature. The linear fit (red line) is made in the linear region.

From figure 5 it can be seen that there is a region where the current I_{SD} through the device shows a

linear dependence of V_g. This region is called the linear regime or the ohmic mode of the NWFET, since the devices show ohmic behaviour in this region.

To extract the transconductance g_m of the ohmic mode a linear fit (the red line) is made using Matlabs fitting tool. Its slope is the transconductance, which is proportional to the mobility μ_{FE}.

The value where the fit intercept the x-axis (in the figure around $\sim$-5.5V) is defined as the threshold voltage V_t of the NWFET. If the NWFET was in the ohmic mode there should be no current running through the device below the threshold voltage. However as it is seen from figure 5 there is in fact a current. This region is called the sub-threshold regime where $V_g < V_t$ and the current is called the sub-threshold current I_{subthr}[11]. At a sufficiently high gate voltage (in figure 5 above 6V) the linear dependence of the ohmic mode also breaks down.

Since there is no simple relation between the current I_{SD} and gate voltage V_g, outside the linear region, the field effect mobility is derived in this region. The deriving of μ_{FE} is done as follows: The current through the NW is given by:

$$I_{SD} = \int qnv_d dA \qquad (5.2)$$

Where q is the electron charge, n is the electron density, v_d is the drift velocity and the integral is over the cross-section of the NW dA. Inserting equation 3.4:

$$I_{SD} = \int qn\mu_{FE}|E_{bias}|dA = \int qn\mu_{FE}V_{SD}L^{-1}dA = \frac{Q_{tot}\mu_{FE}V_{SD}}{L^2} \qquad (5.3)$$

The second equality holds because: $|E_{bias}| = |-\nabla V_{bias}| = |-\frac{V_{SD}-0}{L}|$, where V_{SD} is the bias voltage applied to the source contact, the drain contact is grounded and L is the length between the two source drain contacts. Q_{tot} is the total free charge and in the linear ohmic region it is given by: $Q_{tot} = C(V_g - V_t)$ [10], where C is the capacitance of the back gate, V_g is the gate voltage and V_t is the threshold voltage as described earlier. Using this and introducing the transconductance g_m defined in eq. 5.1:

$$g_m \equiv \frac{\partial I_{SD}}{\partial V_g} = \frac{C\mu_{FE}V_{SD}}{L^2} \qquad (5.4)$$

Isolating the expression for the field effect mobility, I get:

$$\mu_{FE} = g_m \frac{L^2}{CV_{SD}} \qquad (5.5)$$

This equation 5.5 is used to find the mobility. L is the distance between the inner contacts, which is extracted from SEM pictures taken after the measurements. V_{SD} is set by the Keithley and C is the capacitance of the back gate. The transconductance g_m is extracted from the linear fit of in the linear region of field effect mobility graphs, like in figure 5.

The capacitance C is estimated by the commonly used formula[10][12][13]:

$$C = \frac{2\pi\epsilon L}{ln[(t_{ox} + r + \sqrt{(t_{ox+r})^2 - r^2})/r]} \approx \frac{2\pi\epsilon L}{ln(\frac{2t_{ox}}{r})} \qquad (5.6)$$

Where ϵ is the permittivity of the SiO_2 layer, t_{ox} is the thickness of the SiO_2 layer and r is the radius of the NW. The last approximation holds for $t_{ox} \gg r$; in this experiment t_{ox}= 500nm and the NW radii is around $\sim$50nm[1].

This formula for the capacitance actually comes from the model of a metallic cylinder on an infinite metal plate, and to use this formula several assumptions is required[12]: Firstly the electron density in the NW is assumed to be high ($\sim 10^{17}cm^{-3}$) in order to be treated as metallic. Secondly the distance L must be much longer than the thickness of the SiO_2 layer in order to neglect the fringing

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[1]Consult figure 12 in the appendix, to see the diameters of all the NWs

capacitance of the source and drain contacts. It is also assumed that there is no movable charges or defects in the SiO_2 layer or on the NW surface and that the cross section of the NW is circular. Lastly the model assumes that the NW is completely submerged in the SiO_2. However this model is also used for back gate measurement where the NW lies on top of the substrate[12][13]. Because of the lack of dielectric medium around the NW, this model can only give an upper limit for the capacitance.
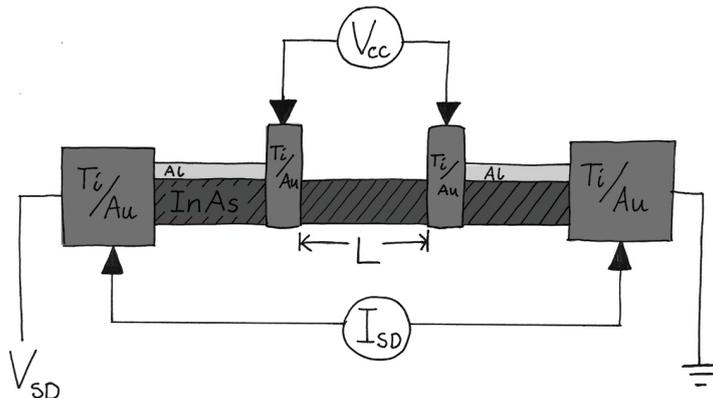
5.2 Measuring the resistivity

Figure 6: A schematic illustration of the 4-probe measurement setup. A bias current V_{SD} is applied to the source contact while the drain contact is grounded. An amperemeter (the Keithley) measures the current flowing through the NW. A voltmeter measures the voltage drop V_{cc} between the two inner contacts. The distant L between the inner contacts and the cross area of the NW (not pictured) is needed to find resistivity ρ.

The resistivity ρ of the NW is found by measuring the intrinsic resistance R of the NWs. This is done by setting up a 4-probe measurement. The system is shown in figure 6. The two outermost contacts are used as source and drain contacts while the two inner contacts are used as sensors.

With a Keithley 2400 Sourcemeter, a bias voltage V_{SD} is applied to one of the outer contacts (i.e. the source) and the other contact is grounded (i.e. the drain). The Keithley will produce a bias voltage with a accuracy of 5μV and measure the current I_{SD} running through the NW with a resolution of 1pA[8].

The two inner contacts is connected to a Hewlett-Packard 34401A Digital Multimeter (dmm), which measures the voltage drop between the two contacts V_{cc} with an accuracy of 0.003% of the measured value[9]. The dmm has a input resistance of 10GΩ[9], which is much higher than the resistance of the NWs[2], this insures that no current runs through the sensor contacts connected to the HP dmm.

If there was a current running through the contacts, the measurements could no longer give the intrinsic resistance of the device, since there would also be a voltage drop from NW to sensor contact and other voltage drops throughout the system. For this same reason a 2-probe system would not give me the intrinsic resistance of the NW, but the resistance of the system as a whole[7].

With the Keithley a voltage sweep of V_{SD} in the range of ± 5 mV is done[3]. The measurement produces two graphs like in figure 7. When the NWFET is operated in the ohmic mode there is linear dependence of I_{SD} and V_{cc} versus V_{SD}. Using the fitting tool in Matlab a linear fit is generated and the slopes a_I and a_V are extracted. Since the measurement have the same step size ΔV_{SD} these slopes can used to calculate the intrinsic resistance using Ohm's law:

$$R_{int} = \frac{a_V}{a_I} = \frac{V_{cc}/\Delta V_{SD}}{I_{SD}/\Delta V_{SD}} = \frac{V_{cc}}{I_{SD}} \tag{5.7}$$

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[2]In article [10] E.T. Yu, D. Wang, et al. measures the resistance of InAs NW (length 3μm) to be around ∼15-20kΩ

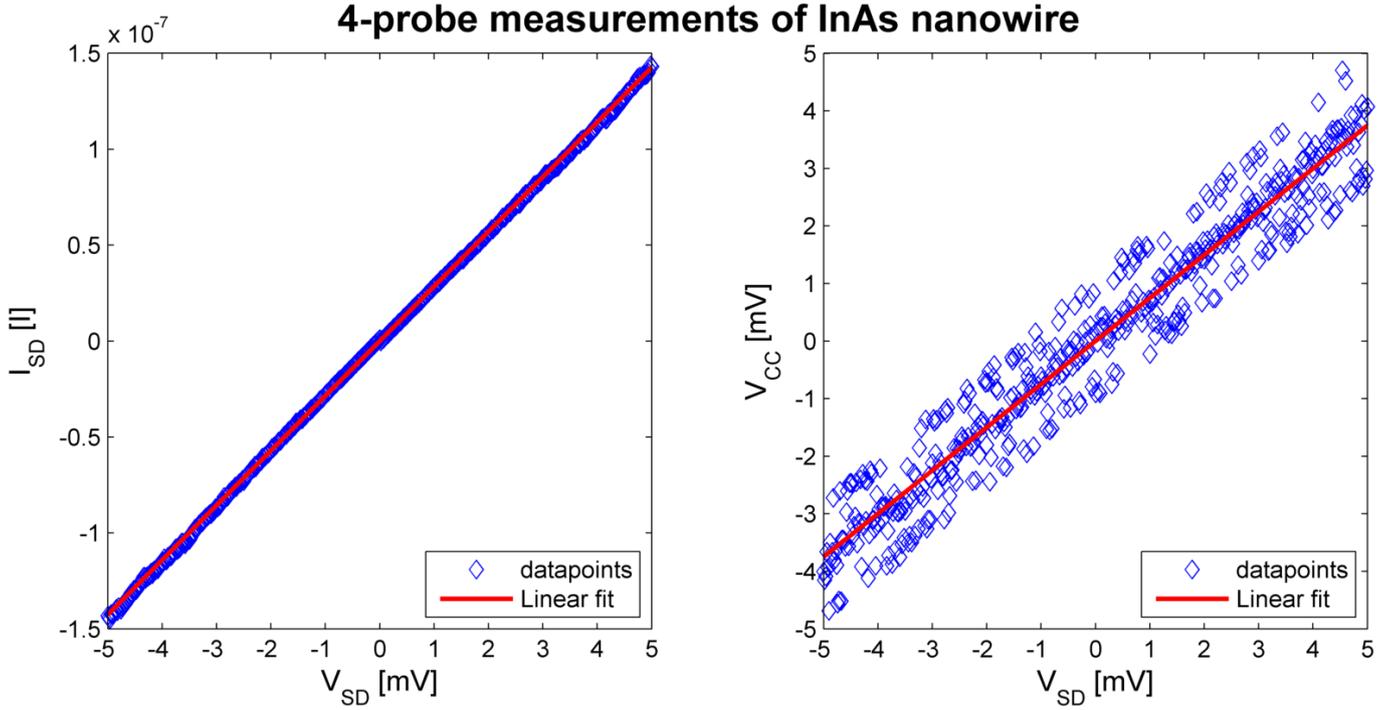[3]For the 50K measurement the voltage sweep is in the range of $\pm$1mV

Figure 7: The 4-probe measurement produces two graphs: The one on the left shows the current I_{SD} versus the bias voltage V_{SD}, the right graphs shows the voltage drop over the two inner contacts V_{CC} versus V_{SD}. The red line is a linear fit which's slope is used to calculate the resistance. In that way it is possible to average over many data points.

From the intrinsic resistance I find the resistivity ρ:

$$\rho = \frac{R_{int}A}{L} \tag{5.8}$$

Where L is the distance between the two inner contacts and A is the cross area of the NW. The cross section is approximated to be a circular and the cross area is found by the formula: $A = \pi r^2$, where r is the radius of the NW.

The length L between the two inner contacts and the radius is extracted from SEM pictures of the devices taken in the Faith e-line.

5.3   Complications During Measurements

During the second measurements (23-25K) certain complications came up. The original thought was the measurement should take place at around 4 Kelvin which is the temperature of the liquid helium used to cool down the probestation. However the probestation could never reach temperatures of 4 Kelvin. Further more the temperature was not stable but slowly rose during the measurements. When the pump was turned off (with the pump valve closed) the temperature would rise quickly. With the pump turned on the temperature would still rise but slower. The measurements were performed with the pump turned on and the temperature rose from 23.2K to 25.5K during measurements. This rise in temperature and the effect of the pump turned on or off suggest that there is a leak in the system, such that air seeping into the system raises the temperature. The pressure of the system would never reach the base pressure of the pump: $1.4 \cdot 10^{-6}$hPa.

The resistivity measurements would behave weirdly around 20 Kelvin; Devices that previously had worked fine suddenly stopped having good ohmic contact. This resulted in some devices suddenly have a much higher resistivity than earlier. This behaviour probably comes from nitrogen ice forming on the contacts and NW and thereby hindering the electric contact. This is caused by an insufficient pump out of the probestation.

The third measurement was carried out in order to try low temperature measurement again. As soon as the temperature dropped to around 20K the freezing out of electric contact would start. When

the probestation was heated up to 50K the electric contact would start working again. This support the hypothesis of ice forming at the contact at too low temperatures. In the end the measurements was carried out at 50K.

The SEM pictures taken to determine the dimensions of the NW were taken after the measurements at 299K and 23-25K, but before the 50K measurements. This might have an effect on the result since the SEM will deposit some carbon, which could change the capacitance and conductance of the NW.

Lastly, due to human errors, not all the devices survived all measurements. A common mistake would be confusing the source-drain voltage with the gate voltage, which results in a way to high bias voltage that ruins the NW. Therefore, in the first measurements at room temperature there are more working NW and fewer in the second and third measurements.

6 Results & Discussion
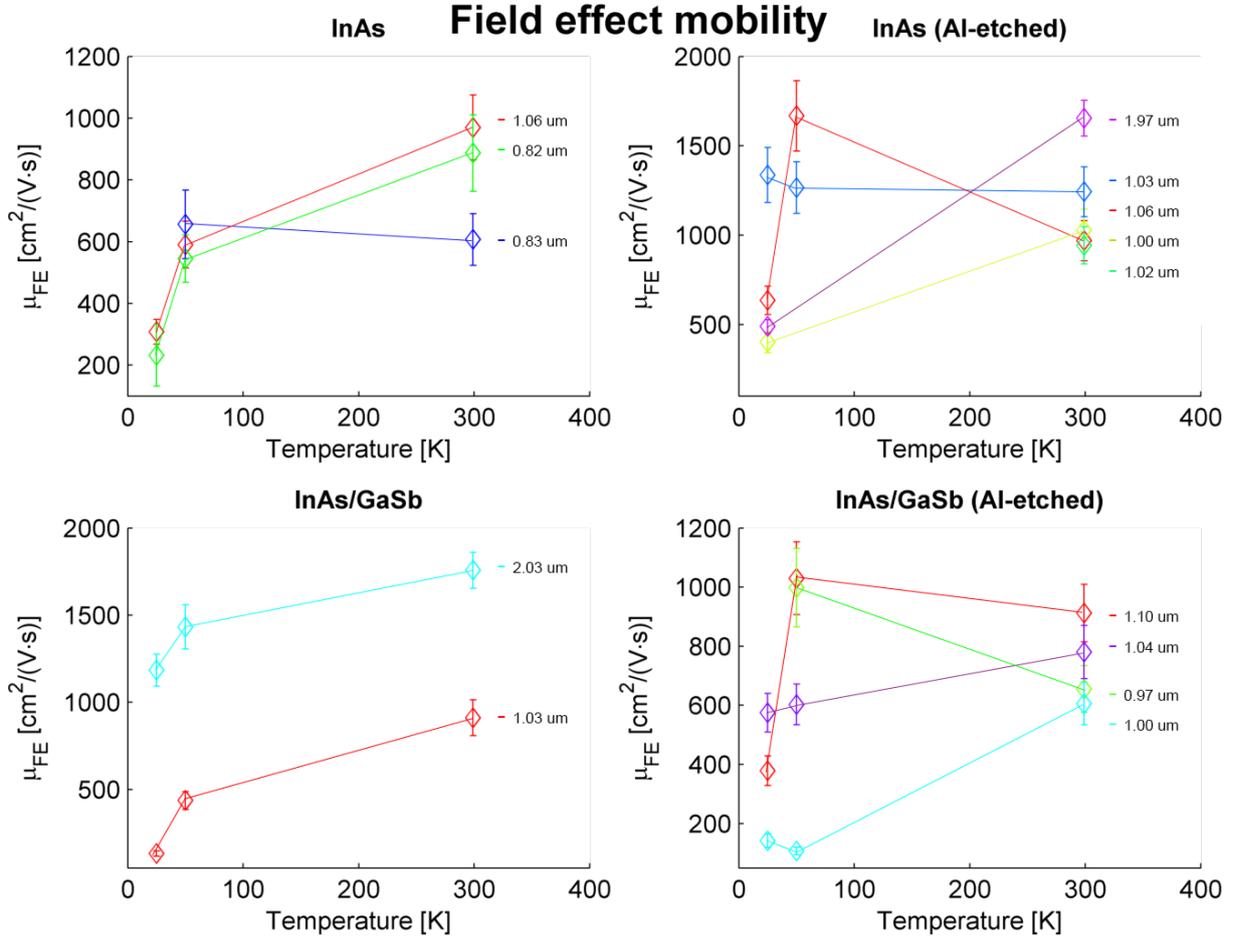
6.1 The Field Effect Mobility

Figure 8: The figure shows graphs of all the four different NW types. In the left column is the non-etched and in the right column is the aluminum etched. Compared to the etched NWs the non-etched NWs seems to have a more uniform response where the mobility decreases as the temperature decreases.

Figure 8 shows the field effect mobility μ_{FE} for the four different NW measured at the three different temperatures. The mobilities found in this report are far less than the expected values of InAs NW of this sort. Other reports have found the field effect mobility of InAs NW to be 2000 $cm^2/(V \cdot s)$ and higher [1][13].

In the lower left window showing the graphs for the Qdev287 NWs, it is interesting to see that device 09 (turquoise) is always significantly higher than device 03 (red). Device 09 also have a mobility closer to the expected value of $2000 cm^2/(V \cdot s)$ at room temperature, namely $1758\ cm^2/(V \cdot s)$. That is about twice the size of the mobility of device 03 ($911\ cm^2/(V \cdot s)$). Interestingly, device 09 also has twice the length L (2.0μm) between the inner contacts as compared to device 03 (1.0μm). This may suggest that the length L has an influence on the measurements, which theoretically should not be the case since μ_{FE} is independent of the length.

A reason for this possible length dependency of μ_{FE} is likely to come from the way the capacitance is estimated. In the expression used for calculating the capacitance it is assumed that the length between the contacts is much longer than the thickness of the dielectric medium, in order to neglect the shielding of electric field coming from the metallic contacts. Unfortunately, this is not the case: the thickness of the SiO_2 layer is 500nm and the typical distance L between the two inner contacts is $\sim 1\mu$m except for two NW (see figure 8). This is a major flaw in the design of the devices.

The shielding from the metallic contacts will lessen the effect of the field coming from the back gate. This means that the distance L in eq. 5.6 for the capacitance is effectively much less than the physical distance L between the contacts, making the real capacitance of the system much less than calculated. Therefore the actual field effect mobility can be assumed to be much higher than the results calculated by using the measured contact to contact distance.

If the probestation is insufficiently pumped out, as feared given the discussion in section 5.3, this will also lower on the measured mobility. If dielectric molecules like, H_2O, CO_2 or N_2 sits on the surface of the nanowire they will as well as the metal contacts shield the NW from electric fields. Since the eletron transport of NWs is mainly on the surface, because of surface band bending, this kind of shielding may have a high impact than expected.

6.2 The Resistivity

In figure 9 the resistivity results can be seen. The resistivity of the NWs is generally in the order of $10^{-4}\Omega$/m. Though at the 23-25K measurement two extremely high resitivies shows up in the measurements of the InAs/Al-etched NWs (Qdev343). One device exceeds $1100 \cdot 10^{-4}\Omega/m$[4]. It is highly doubtful that these values are the actual resistivities of the NWs; more likely they come from flawed measurements, like ice forming on the surface of the contact pads that hinder the ohmic contact to the device. Therefore these two values are not presented in figure 9.

6.3 The Electron Density

Because of the limited space in this report the graphs for the electron density were moved to the appendix (figure 13). Since the electron density is a product of the resistivity and mobility, the results will have the same case of some very high values at the 23-25K measurements. If we disregard these values by assuming that they are caused by errors in the measurements (e.g. ice forming) the general electron density of the NWs is in the order of 10^{17}cm^3.

6.4 Effect of the Aluminum Etching

One of the goals of this report was to investigate whether or not the aluminum etching has an impact on the mobility of the NWs. Figure 10 shows the average mobility of the NW types at the three temperatures; the left window shows InAs-core NWs (Qdev1 and Qdev343), the right window shows the InAs/GaSb-core NWs (Qdev287 and Qdev297). The errorbars have the length of $\pm$ one standard deviation of the average. The red color represent the aluminum etched NWs and the blue color represent the non-etched.

As it can be seen from the figure the great variance of the results makes it hard to conclude one specific tendency. From the left window it seems like the etching process have raised the mobility of the Qdev343 NW. Looking at the right window the same etching process seems to have lowered the
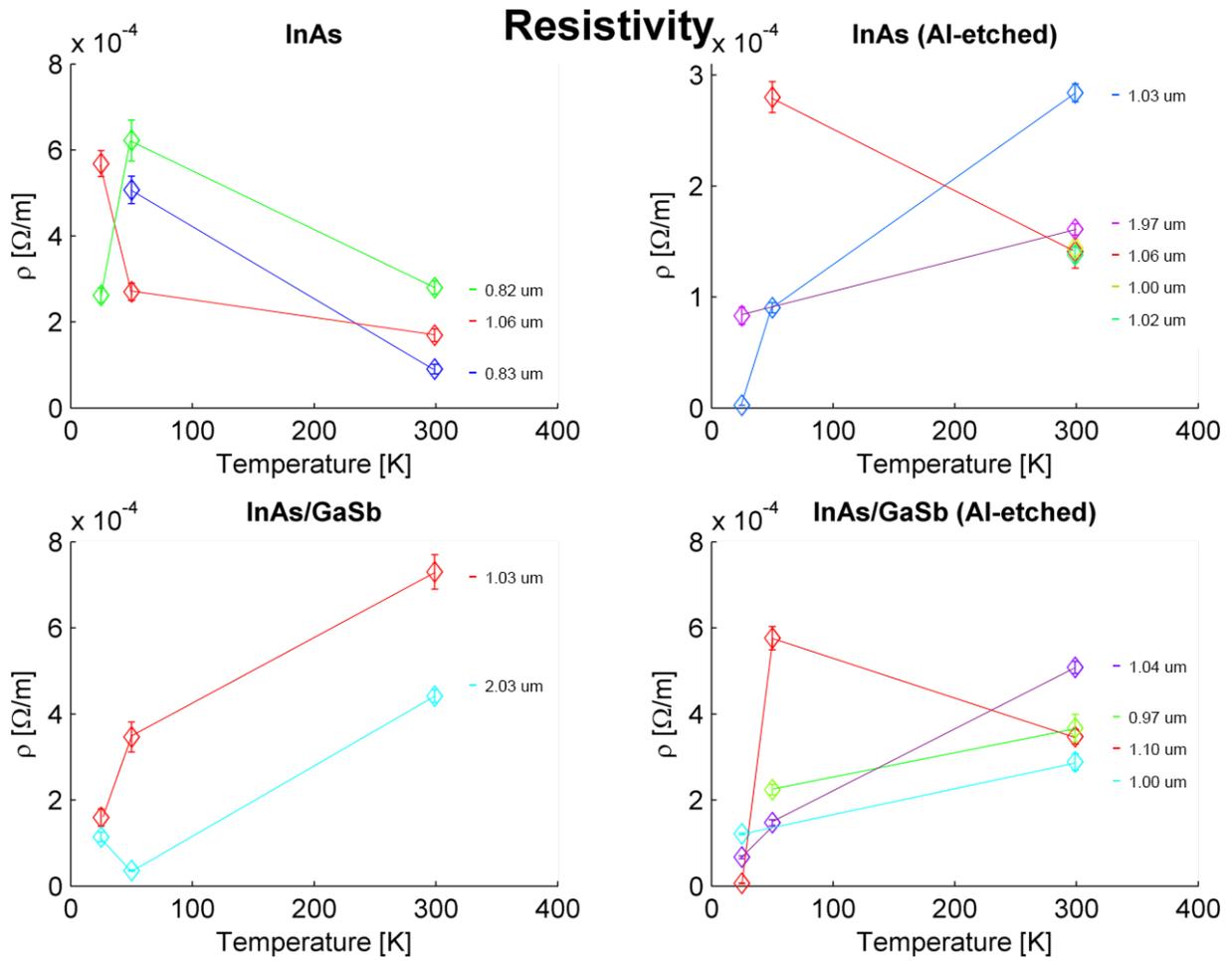
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[4]see appendix figure 14

Figure 9: The figure shows graphs of the resistivity of all the four different NW types. In the left column is the non-etched and in the right column is the aluminum etched. In the upper right window the data point belonging to device Qdev343 and Qdev343 09 at the 23-25K measurements has been omitted, since these were many orders of magnitude higher than the rest.

mobility, as one would expect, given the discussion in section 3.1 where the Al etch is suspected to create more scattering due to increased lattice defects.

7 Conclusions

The first goal of this report was to master and document the complicated fabrication process of nanowire devices. All the devices created in this report show the characteristic response of the field effect measurements and the linear dependence of V_{SD} and I_{SD} from the 4-probe measurements indicate that there is ohmic contact between NW and contacts. Therefore several working devices were successfully created, but due to design flaws and a possible insufficient pump out of the probestation the mobility of the NWs could not be measured accurately.

In their article *High Electron Mobility InAs Nanowire Field-Efffect Transistors*, E.T. Yu and D. Wang (et al.), also measure the field effect mobility of InAs NWs at room temperature[10]. They perform measurements on seven NW and obtain an average mobility of $3380cm^2/(V \cdot s)$ with a standard deviation of 51% of the average. In my report the average mobility of the non-etched InAs NW (Qdev1) was found to be $822cm^2/(V \cdot s)$ with a standard deviation of 23% of the average. At room temperature none of the average mobilities measured in this report have standard deviations exceeding 50% of the average (see appendix figure 14. The mobilities measured in this report are therefore not less consistance of that of E.T. Yu and D. Wang's.

At the low temperature 23-25K measurements problems with possible nitrogen ice forming on the contact pads and the nanowires may hinder the results of both the resistivity and the field effect
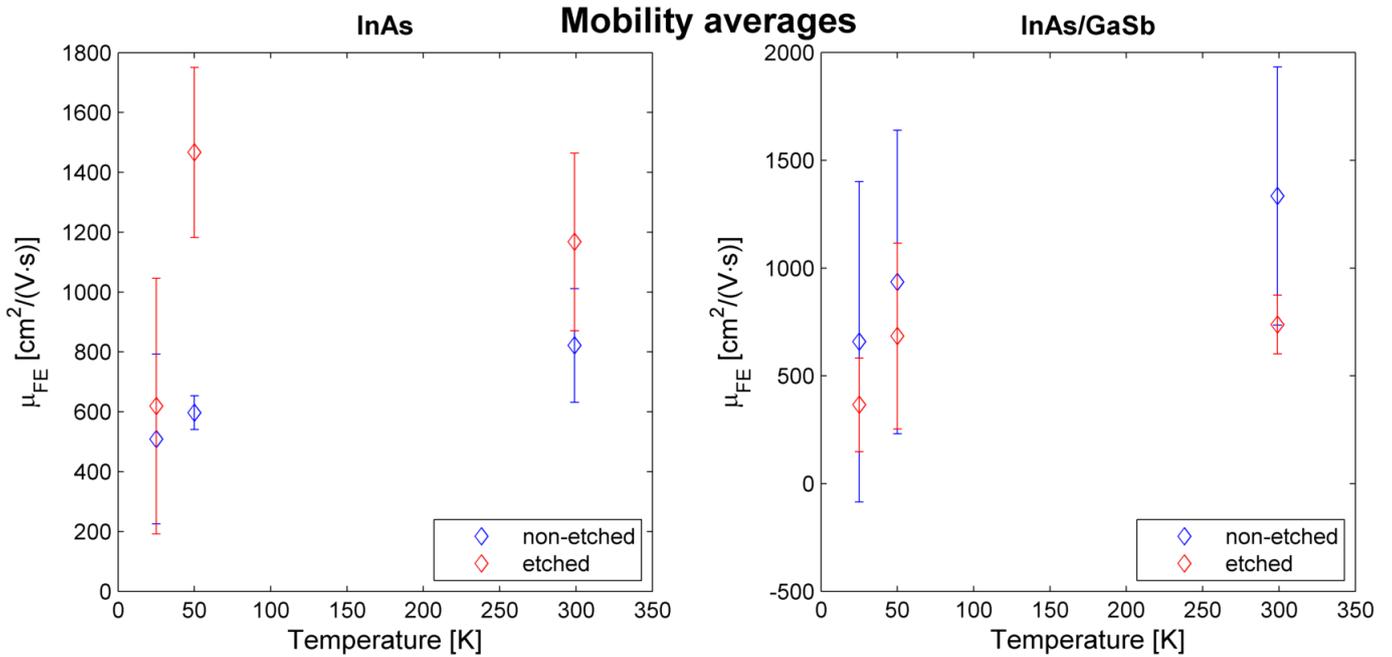
Figure 10: The two windows show average mobility of a NW type (diamond shape), with the error bars as ±one standard deviation. The blue color show the non-etched NW and the red color shows the aluminum etched NW.

mobility, as seen in figure 15 in the appendix were the 23-25K measurements have high standard deviations. This is most prominent in the resistivity measurements of the Qdev343 NWs (see tabel 14), were one NW have a resistivity exceeding $1100 \cdot 10^{-5} \Omega/m$. The problem with ice forming can be solved with a better pump out of the probestation.

An insufficient pump out of the probestation will also cause trouble at room temperature even though no ice is formed. Small dieletric molecules, like H_2O and N_2, may sit on the surface of the NW shielding the wire from the gate field. This lowers the field effect mobility measured.

Given the results of this report it is not possible to consistently determine the effect of the aluminum ecthing have on the electric properties of the NWs.

This was the first batch of devices made and given the complicated fabrication process it has been a successful first try that has giving result to further investigate. Now come the process of optimizing and improving the design and yield of the devices using the knowledge gained from the experiences of this report.

8   Improvements and Further Investigations

In order to get better measurements and more accurate results, improvements of the design needs to be made. For future experiments I have three suggestions for improvements of the design:

- **Aluminum Etch:** Etch all the aluminum away instead of only in between the two inner contacts. The aluminum is not used for anything during the experiments and it has an unwanted shielding effect of electric fields for the NW. Further more, it simplifies the fabrication process since the electron beam exposure of etching windows is no longer needed.

- **Longer Distance Between the Inner Contacts:** In order to use the model for the capacitance eq. 5.6, a sufficiently longer distance between the source and drain contacts, compared to the thickness of the SiO_2 layer, is needed.

- **Longer Pump Out Time:** Nitrogen ice is suspected to form on the device when the temperature is sufficiently low, at room temperature no ice is formed, but dielectric molecules may sit

on the surface of the NW contributing to the capacitance. In order to prohibit this, the system needs to be at a very low pressure. An advice would be to try and pump out the system for 24 hours before taking any measurements.

Another addition to the design of the device would be to add side gates to the devices and compare side gate with back gate field effect measurements. One could also perform Hall effect measurements and comparing the Hall mobility with the field effect mobilities as it is done by O. Hultin and K. Storm in their 2015 article *Comparing Hall Effect and Field Effect Measurements on the Same Single Nanowire*[14].
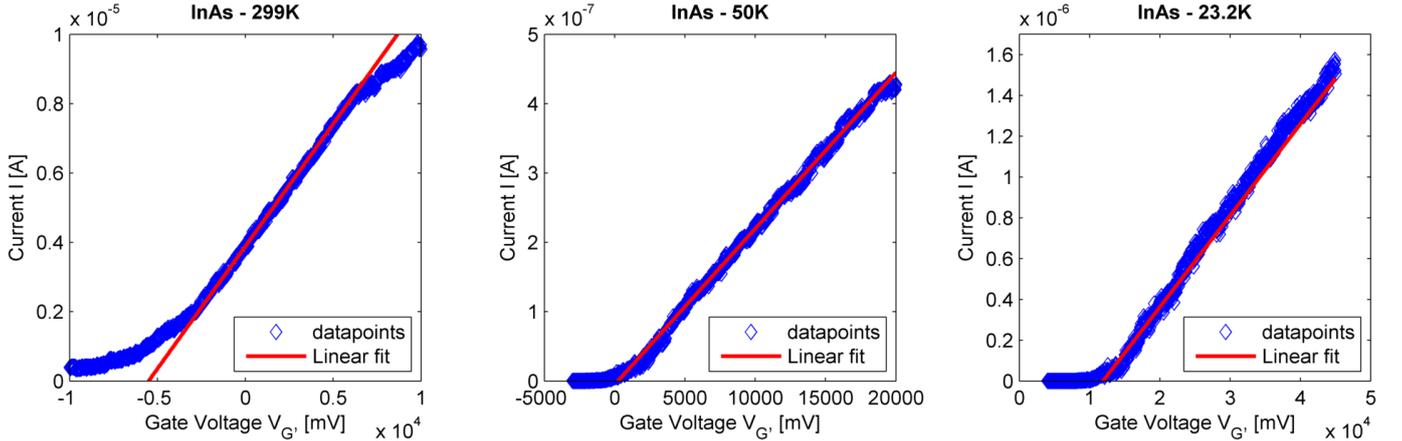

Figure 11: Field effect measurements of the same InAs nanowire done at the three different temperatures: 299K, 50K and 23.2K.

An interesting property of the NWs, not investigated in this report, is the activation energy. As it can be seen from figure 11 the threshold voltage increase as the temperature decreases. To extract the activation energy of the nanowire one could look at current I_{SD} at a certain gate voltage and see how it changes at different temperatures. Using Arrhenius equation one could make an Arrhenius plot with $\ln(I_{SD})$ plotted along the y-axis and $1/(k_B T)$ along the x-axis. The slope would be the activation energy E_A of the nanowire as seen by the formula:

$$ln(y) = ln(A) - E_A \frac{1}{k_B T} \tag{8.1}$$

Where A is an constant and k_B is Boltzmann's constant.

In this report different bias voltages were used for the three temperature measurements: at room temperature the bias voltage was 100mV, at 50K it was 5mV, and at 23-25K it was 20mV. This means that the change in current will more likely come from the change in bias voltage than from temperature change, which can be seen from looking at the y-axis scale in figure 11. Therefore the results of this report cannot be used to find the activation energy since the field effect mobility measurements at the different temperatures needs to be done at the same bias voltage.

Finding the activation energies from the field effect measurement is a smart way of utilizing the same graphs to find to properties of the NW.

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9   Appendix

Dimensions			
Wire type	**Device name**	**Length L [µm]**	**diameter [µm]**
Qdev1 InAs	4a	1.06 ± 0.05	0.13 ± 0.05
	8	0.82 ± 0.05	0.15 ± 0.05
	25	0.83 ± 0.05	0.11 ± 0.05
Qdev343 InAs/Al	7	1.00 ± 0.05	0.12 ± 0.05
	9	1.02 ± 0.05	0.09 ± 0.05
	10	1.06 ± 0.05	0.09 ± 0.05
	12	1.03 ± 0.05	0.09 ± 0.05
	15	1.97 ± 0.05	0.09 ± 0.05
Qdev 287 InAs/GaSb	3	1.03 ± 0.05	0.10 ± 0.05
	9	2.03 ± 0.05	0.10 ± 0.05
Qdev297 InAs/GaSb/Al	1	1.10 ± 0.05	0.10 ± 0.05
	3	0.97 ± 0.05	0.10 ± 0.05
	23	1.00 ± 0.05	0.10 ± 0.05
	27	1.04 ± 0.05	0.10 ± 0.05

Figure 12: Tabel of the physical dimensions of the devices.
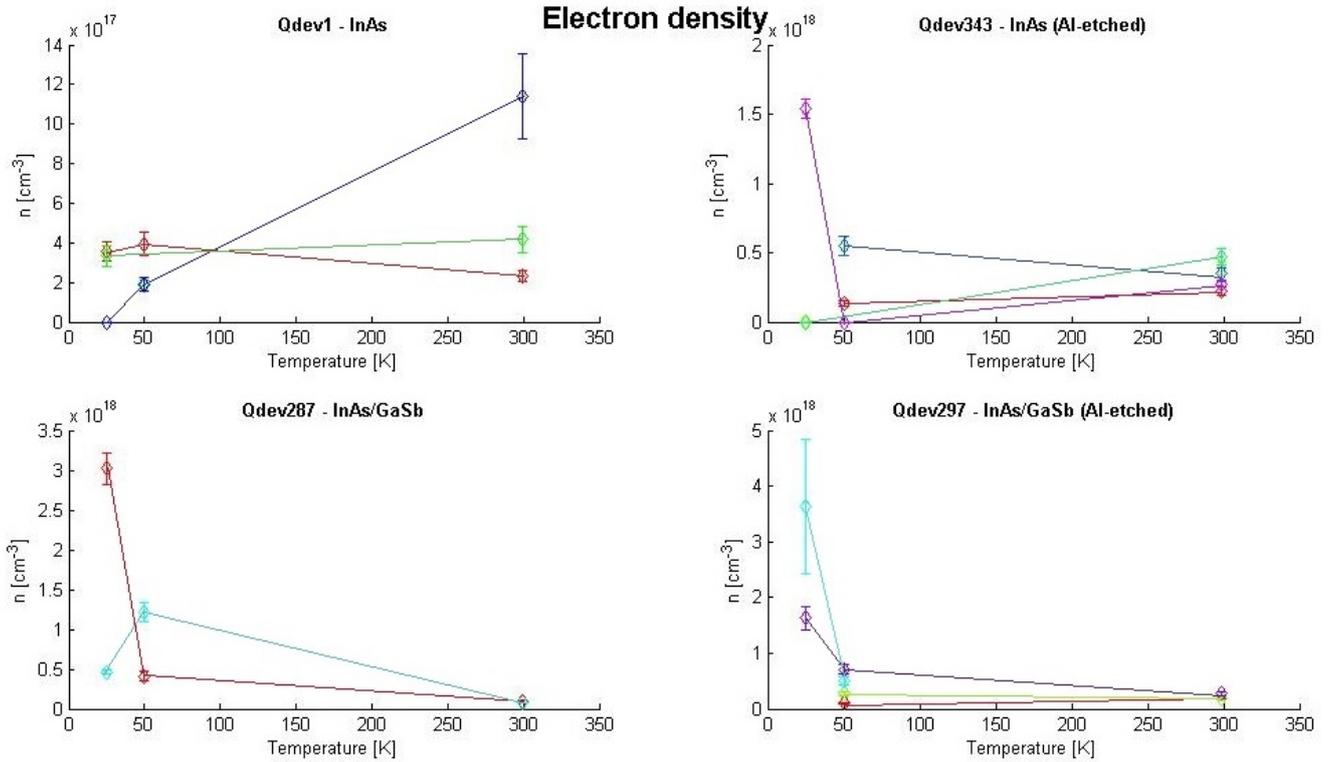
Figure 13: Graphs of the electron densities

299 K				
Wire type	**Device name**	**ρ *10^-5 [Ohm/m]**	**μ_FE [cm^2 / (V * s)]**	**n *10^17 [cm^-3]**
Qdev1 InAs	4a	16.9 ± 1.5	970 ± 105	2.30 ± 0.28
	8	28.0 ± 1.5	887 ± 124	4.16 ± 0.69
	25	9.04 ± 1.1	607 ± 84	11.4 ± 2.1
Qdev343 InAs/Al	7	14.1 ± 1.5	969 ± 113	2.27 ± 0.29
	9	14.4 ± 0.8	1028 ± 117	3.86 ± 0.49
	10	13.8 ± 0.7	943 ± 104	4.71 ± 0.57
	12	28.4 ± 0.8	1243 ± 140	3.48 ± 0.43
	15	16.1 ± 0.5	1654 ± 100	2.74 ± 0.19
Qdev 287 InAs/GaSb	3	73.0 ± 4.0	911 ± 103	0.939 ± 0.12
	9	44.1 ± 1.5	1758 ± 103	0.806 ± 0.05
Qdev297 InAs/GaSb/Al	1	34.7 ± 1.7	912 ± 97	1.97 ± 0.23
	3	36.7 ± 3.2	655 ± 79	1.88 ± 0.25
	23	28.8 ± 1.9	606 ± 72	2.81 ± 0.36
	27	50.8 ± 1.8	780 ± 90	2.78 ± 0.35
50 K				
Wire type	**Device name**	**ρ *10^-5 [Ohm/m]**	**μ_FE [cm^2 / (V * s)]**	**n *10^17 [cm^-3]**
Qdev1 InAs	4a	27.0 ± 2.0	590 ± 76	3.92 ± 0.59
	8	62.2 ± 4.8	545 ± 72	1.85 ± 0.30
	25	50.7 ± 3.2	656 ± 111	1.88 ± 0.34
Qdev343 InAs/Al	7	28.0 ± 1.4	1667 ± 197	1.34 ± 0.17
	12	9.02 ± 0.45	1266 ± 145	5.47 ± 0.68
Qdev 287 InAs/GaSb	3	34.6 ± 3.5	437 ± 51	4.13 ± 0.64
	9	3.59 ± 0.16	1433 ± 127	12.1 ± 1.21
Qdev297 InAs/GaSb/Al	1	57.6 ± 2.7	1030 ± 123	1.05 ± 0.14
	3	22.4 ± 1.2	998 ± 133	2.79 ± 0.40
	23	118 ± 7.0	107 ± 13	5.00 ± 0.71
	27	14.7 ± 0.7	603 ± 69	7.07 ± 0.89
23 - 25 K				
Wire type	**Device name**	**ρ *10^-5 [Ohm/m]**	**μ_FE [cm^2 / (V * s)]**	**n *10^17 [cm^-3]**
Qdev1 InAs	4a	56.8 ± 3.0	308 ± 24	3.57 ± 0.50
	8	26.2 ± 1.7	232 ± 29	3.36 ± 0.52
Qdev343 InAs/Al	1	5974 ± 418	232 ± 19	0.046 ± 0.005
	7	11265 ± 391	635 ± 37	0.0087 ± 0.0020
	9	6215 ± 366	401 ± 38	0.025 ± 0.003
	12	0.242 ± 0.024	1336 ± 53	193 ± 13.4
	15	8.30 ± 0.78	489 ± 26	15.4 ± 0.8
Qdev 287 InAs/GaSb	3	15.9 ± 2.0	132 ± 8	30.2 ± 2.0
	9	11.4 ± 1.1	1184 ± 92	4.62 ± 0.26
Qdev297 InAs/GaSb/Al	1	0.64 ± 0.1	379 ± 50	238 ± 59.2
	23	12.1 ± 0.4	142 ± 23	36.4 ± 12.1
	27	6.68 ± 0.30	575 ± 65	16.3 ± 2.11

Figure 14: Tabel showing all of the results of the measurements.

average ± standard deviation			
299 K			
NW type	ρ *10^-5 [Ohm/m]	μ_FE [cm^2 / (V * s)]	n *10^17 [cm^-3]
Qdev 1	18.0 ± 9.5	822 ± 190	5.94 ± 4.80
Qdev 343	17.4 ± 6.2	1167 ± 397	3.41 ± 0.95
Qdev 287	58.9 ± 20.4	1334 ± 599	0.873 ± 0.094
Qdev 297	37.7 ± 9.3	738 ± 137	2.36 ± 0.51
50 K			
NW type	ρ *10^-5 [Ohm/m]	μ_FE [cm^2 / (V * s)]	n *10^17 [cm^-3]
Qdev 1	46.6 ± 18.0	597 ± 56	2.55 ± 1.19
Qdev 343	18.5 ± 13.4	1466 ± 284	3.31 ± 2.86
Qdev 287	19.1 ± 21.9	935 ± 704	8.14 ± 5.67
Qdev297	31.6 ± 22.9	877 ± 238	3.64 ± 3.10
23 - 25 K			
NW type	ρ *10^-5 [Ohm/m]	μ_FE [cm^2 / (V * s)]	n *10^17 [cm^-3]
Qdev 1	41.5 ± 21.6	509 ± 283	3.46 ± 0.15
Qdev 343	4692 ± 4773	619 ± 427	41.7 ± 85.0
Qdev 287	13.5 ± 2.96	658 ± 743	17.4 ± 18.1
Qdev297	6.47 ± 5.68	366 ± 217	96.7 ± 122

Figure 15: Tabel showing the average of each NW type ± on standard deviation.