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Center for Quantum Devices

Bachelor Thesis

Fabrication of Devices with Superconducting Proximity Effect in InAs Nanowires

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Acknowledgments

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Lastly I want to thank Charles M. Marcus for helpful advices along the way and for having me in the group.

Abstract

In this thesis I present my work on fabricating a InAs-Al-Nb device with a hard superconducting gap with high critical field induced in the InAs nanowire through proximity effect. As an introduction I explain the motivation, that my work is part of the hunt for Majorana Fermions, followed by a short recap of superconductivity and the theory of proximity effect for SN and SS' interfaces.
Subsequently I describe the mesoscopic device and the fabrication processes needed for making it. I didn't finish a working device, but all the steps needed to do so is documented.

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Chapter 1

Motivation

If not familiar with superconductivity, proximity effect and/or the definition of a hard superconducting gap, I suggest the reader to start reading chapter 2, where these topics are explained.

Majorana Fermions (MF) were predicted by Ettore Majorana back in 1937, but are not yet confirmed by measurement, though Mourik et al have published measurements that might indicate MF [1]. These exotic particles have many fascinating abilities. One of them is their non-local nature, which makes them suited for controlled quantum information processing [2]. As the fabrication of mesoscopic electrical circuits has improved over the past decades, the hunt for MF has found its place in condensed matter physics since they are strong candidates for realizing quantum computers. M. Leijnse and K. Flensberg have reviewed how MF might be found in 1-Dimensional systems [2]: a semiconducting nanowire with strong spin-orbit coupling should be in contact with a superconductor which through proximity effect induces superconductivity in the semiconductor. This system should also have a large Zeemann splitting, induced by an outer magnetic field perpendicular on the spin-orbit field. If those criteria are fulfilled, then theory predicts that a pair of MFs would be present in a delocalized correlated state, which is protected from different types of decoherence. This state is protected because it is isolated in the middle of a superconducting gap, being the only state in the gap, see FIG 1.2(c).
Mourik et al have measured a zero bound peak (peak in the middle a superconducting gap) in a InSb-NbTiN-junction, but their system has a soft gap, with a subgap conduction suppression below 5, meaning other states are present inside the gap, see FIG 1.1(a). Even if it was MF they measured, these couldn't be used for quantum computation because their zero bound peaks are not isolated and hence not protected form coherence. The reason they have a soft gap is most likely because of a bad interface between InSb and NbTiN [3]
The nanowire group in QDev have successfully made a good interface between InAs and Al by growing the Al as an epitaxial shell on the InAs nanowires, see FIG1.1(b-d). Measurements on these wires have showed a very hard gap with a subgap conduction suppression of 50[4], meaning that no states are present inside the gap, see FIG 1.2(b). Unfortunately Al has a weak pair potential, so the gap is narrow compared to Mouriks measurement FIG 1.2(a) and cannot withstand superconductivity in a magnetic field sufficiently high to measure MF.
The junction documented in this thesis is a InAs-Al-Nb junction. The idea is to use Nb to proximitize Al, thereby increasing its critical field and still have the good contact to InAs. The goal is to measure a hard gap, like FIG. 1.2(c), with a higher critical field than earlier measured.

A short recap of superconductivity and the theory of proximity effect in NS and SS interfaces will be explained in the Theory chapter, while the challenges in fabricating and realizing such a system will be addressed throughout the Fabrication chapter. The Results chapter states how far in the process this project has got and Conclusion & Outlook sums up and explains what further work needs to be done.

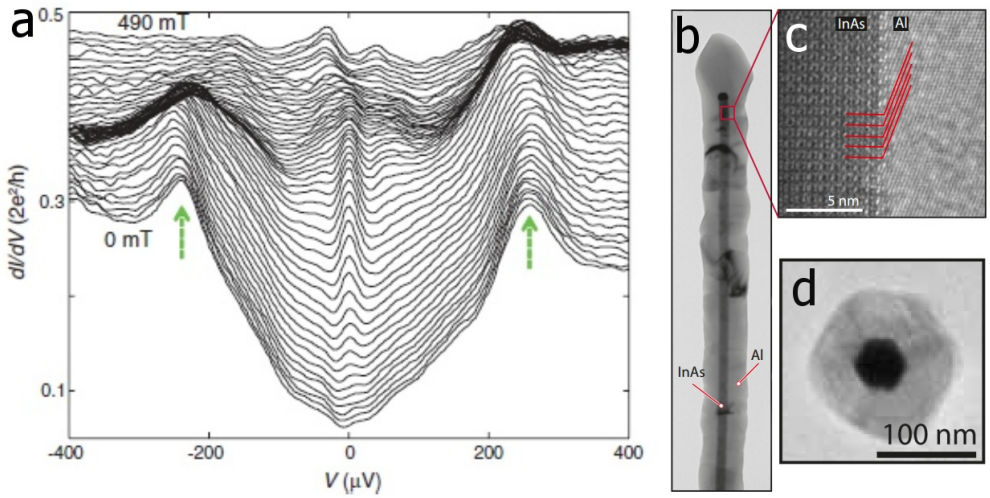

Figure 1.1: *(a)Graph of one of many tests Mourik et al present to verify that their measured zero bound peak is a Majorana[1]. They have a NbTiN contact and a normal contact on a InSb nanowire, and measures differential conductance at different parameters. This graph shows measurement voltage sweeps at 70mK with magnetic fields ranging from 0 to 490mT with an interval of 10 mT. All traces besides 0 mT are offset for clarity.* ***(b)*** *Image of InAs nanowire with Al shell.* ***(c)*** *Closeup image of the InAs Al interface.* ***(d)****Picture from the end of a wire shows its hexagonal structure. (b-d) is adapted from [5]*

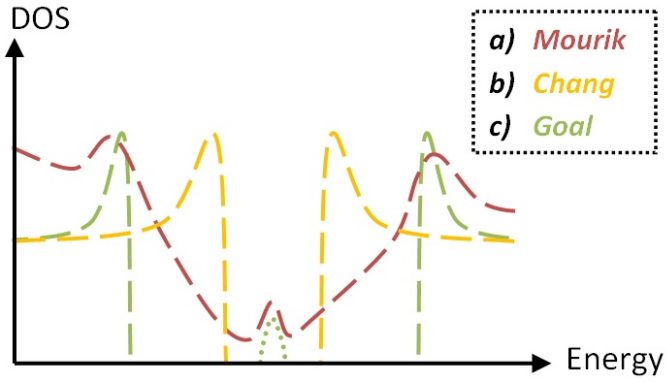

Figure 1.2: *Illustration showing three different DOS curves. Red is the soft gap with a zero bound peak that Mourik et al measured. Yellow is the narrow hard gap that W. Chang have measured. Green is the curve scientists endeavors to measure(A hard and wide gap), which might have a isolated zero bound peak.*

Chapter 2

Theory

2.1 Superconductivity

When cooled down below a (material dependent)critical temperature T_C, some materials become superconducting. At this temperature the crystal lattice of the material vibrates slow enough for electrons to bind in pair (cooper pairs) through interaction with the lattice. Together the electrons have spin 0 or 1 and thus have the abilities of a boson. All Cooper pairs condense down in the same energy level and have free motion here, which gives the characteristic zero resistance. The binding energy (Δ) of a cooper pair is the order parameter of the superconducting phase and is called the pair potential. Δ is, like T_C, different for different superconductors. Electrons with energies (E) higher than Δ can not bind in cooper pairs. By applying energy higher than Δ to electrons in the superconductor, all cooper pairs can be broken, and superconductivity is lost. This energy can eg be in form of heating, voltage or magnetic field.

2.2 Superconducting Proximity Effect

Proximity effect is a phenomenon that happens when superconductors (S) are in good electrical contact with other conducting materials. The superconductor shares certain properties with these materials, in the vicinity of the interface within a distance determined by a coherence length, explained below. This section will go through proximity effect of two different interfaces: SN-interface (N being a normal metal, with superconductor critical temperature much lower than the temperature (T) the measurements are done at; $T \gg T_{C,N}$) and SS'-interface with S and S' being two different superconductors with $T_{C,S} > T_{C,S'} > T$.

2.2.1 NS-Interface

The property that a superconductor shares with a adjacent normal metal is quasi particle phase correlation, enabling N to conduct supercurrents from the superconductor. The strength and the reach of this proximity effect will be explained in the fellowing section.

The strength of the proximity effect

The strength of proximity effect is a measure of how similar the superconducting properties of N is compared to those of S. Blonder et al (BTK) have proposed a theory for how interface resistance(Z),

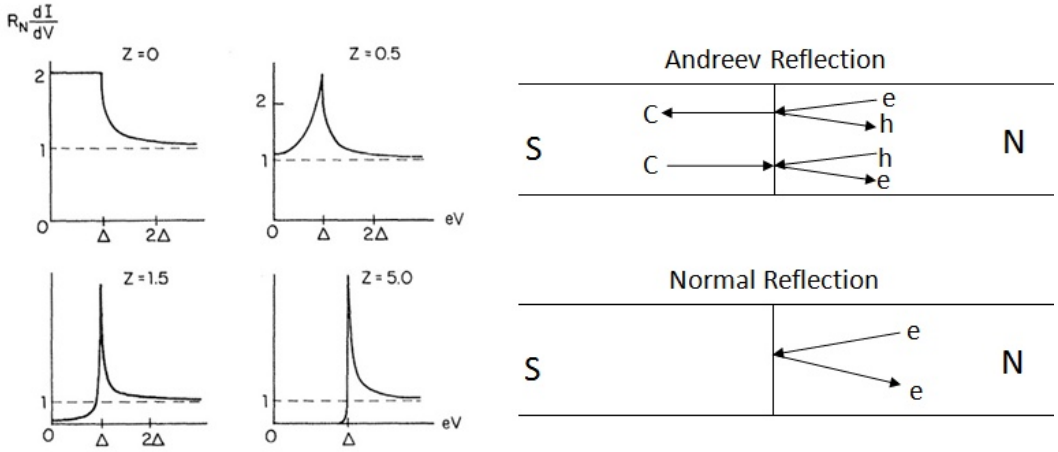

Figure 2.1: *Graphs to the left show theoretical calculated differential conductance curves of S, as a function of order parameter Δ. The energy axis shows energies above the fermi energy, $\epsilon_F = 0$. These plots are made for different Z: interface resistance between superconductor and normal contact. Adapted from [6]. Drawings to the right show the particle transport for Andreev and Normal reflections. e, h and C are electrons, holes and Cooper pairs respectively.*

between S and N contact, influences the proximity effect of this system[6], see FIG 2.1. The graphs are calculated dI/dV curves, called differential conductance curves. When in the tunneling regime (high interface resistance) dI/dV measurements are proportional to the electron density of states (DOS) of that device. These measurements enable one to check DOS of a device at different energies($E = eV$, with e the electron charge) with a voltage sweep. Interfaces with high Z ($\sim M\Omega$) have normal reflection at the NS surface: an electron from N gets reflected back as an electron at the interface. There is no transport over the interface for electrons with $E < \Delta$. Looking at the graph with Z=5.0, this is seen by a hard gap in the electron DOS, meaning that electron states with energies inside the superconducting region ($E \in [\epsilon_F - \Delta; \epsilon_F + \Delta]$) cannot penetrate S, instead these states pile up just outside the gap.

For lower Z, the probability of normal reflection falls while the probability for Andreev reflection rises. The probabilities for the two reflections sum up to 1. Andreev reflection is an incident electron (hole) from N being reflected as a phase correlated hole (electron), thus effectively transferring two electrons (holes), as a cooper pair into S (N). Looking at the Z=0 graph from FIG 2.1, it is seen that with a perfect interface, only Andreev reflections occurs which is why a current propertional to two electrons are measured. The phase correlation from an Andreev reflection is what makes N able to conduct super currents from S, and are hence necessary for proximity effect. For cases with both normal and Andreev reflections, Z=0.5 and Z=1.5, the number of measured electrons through S is between 0 and 2. DOS of a interface with both Normal and Andreev reflections shows a soft gab, like 1.2a. To distinguish between gaps of different shapes, a quantity called the hardness of a gap is defined as the ratio between the conductance of the states outside the gap and the conductance at the bottom of the gap. The ratio is called the subgap conductance suppression. The higher the ratio, the harder the gap.

To sum up, low interface resistance is favorable for proximity effect so most electrons Andreev reflect, while a high interface resistance is necessary to do DOS measurements.

The reach of the proximity effect

The phase correlation between electron and hole in N, from an Andreev reflection, is getting weaker when moving away from the interface because of collisions with other quasi particles. The reach of the proximity effect is the distance it takes the phase correlation to vanish, which is of the order of the coherence length ξ_N. In any bulk material it is equal to the Pippard coherence length of that material, ξ_0. It describes the length it takes the material, disturbed from outside, to obtain its original undisturbed order. The actual coherence length is given by

$$\frac{1}{\xi} = \frac{1}{\xi_0} + \frac{1}{l}, \tag{2.1}$$

where l is the mean free path of the material, which describes the length a quasi particle can travel without being scattered. The mean free path is dependent on the cleanness of the material. Clean N have long coherence lengths on the order of μm, but if the same material had many impurities(dirty material), the mean free path would be lower, and the coherence length would be lower as well. To have a metal with a strong electron-hole phase correlation through out the metal, the thickness of the metal (d_N) should be much smaller than the coherence length of that material.
The devices documented are made of grown InAs nanowire with epitaxial grown aluminum shells which both are considered clean, while niobium contacts are sputtered on the wire and is considered dirty. InAs is a semiconductor, so the bulk coherence length is expected to be even larger because of its low density of conduction electrons. The diameter of the InAs wires is below 100 nm so the part of the wire covered by superconductor should have a strong electron-hole phase correlation, when assuming a good interface with a high amount of Andreev reflections.

2.2.2 SS'-Interface

SS' is a superconductor-superconductor-bilayer, where $T_C^S > T_C^{S'} > T$. The superconductors affect each other through Andreev reflections as they would affect metals. The proximity effect from S increases $T_C^{S'}$, and the proximity effect from S' decreases T_C^S within a distance corresponding to the relative coherence lengths of S' and S. When proximity effect decreases T_C it is called inverse proximity effect. The S-gap is wider in energy-space than the S'-gap enabling quasi particles from S' to be reflceted by S thus providing the opportunity for Andreev reflections and proximity effect, see FIG 2.2 [7]. This is the first documented experiment showing spatial proximity effect in a SS' bilayer, published January 2014. The following section will explain following properties of SS' proximity effect: Energy Gap, strength, reach and quasi particle trapping.

Pair potential vs Energy Gap

As seen on FIG 2.2 Δ changes spatially throughout the bilayer because of the proximity effect. The energy gap E_g for a bulk superconductor is 2Δ, but for a SS'-bilayer it varies spatially around the interface. If the material thicknesses is of the order of the respective coherence lengths, then the gap can be considered constant [8] throughout the layer. Its magnitude is between that of the two superconductors and depend on the amount of proximity and inverse proximity.

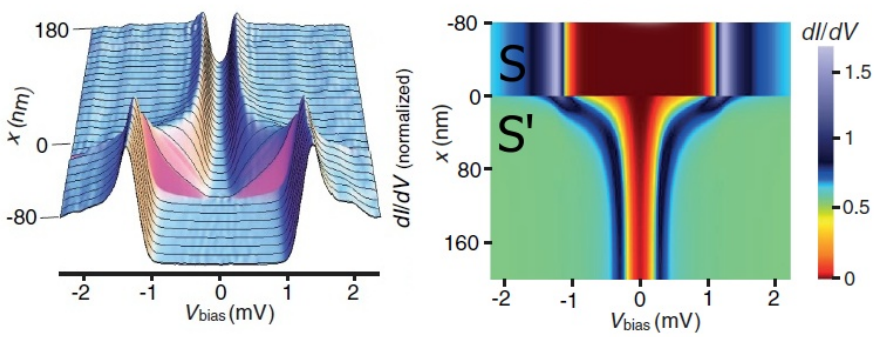

Figure 2.2: *Experimental 3D and theoretical 2D graphs showing the spacial dependence of the DOS at a SS' boundary in the bias voltage-distance-space. The whole device was fabricated in vacuum, making it possible to have low interface resistance. The measurements were made with Scanning Tunneling Spectroscopy. The interface is located at x=0, S is located in x<0 and S' in x>0. Inverse proximity effect were neglected and is therefor not visible in the 2D graph. Adapted from [7]*

The strength of the proximity effect

SS' proximity effect have many different uses. This project aims to use S (Nb) to induce a stronger pair potential in S' (Al) wanting it to be equal to that of S. To optimize the fabrication for such needs one should take following 3 parameters into account: the thickness of the materials d_S and $d_{S'}$, the proximity strength γ and the boundary transparency γ_{BN}. These are explained below.

Thickness of the materials, d. One way to increase the total T_C is make sure that the thickness of S is larger than the thickness of S', $d_S \gg d_{S'}$. The amount of surface reflections is reverse proportional to the thickness of the material, so by decreasing d'_S the quasi particles use less time in S', thus decreasing inverse proximity. Likewise a thick d_S will increase the proximity, because the quasi particles use more time in S.

Proximity strength γ. This factor is introduced by Golubov et al, in their paper from 1995 [9] where they propose a theory for SS' proximity effect for very thin S' layers, $d_{S'} \ll \xi_{S'}$. The factor is given by

$$\gamma = \frac{\rho_S \xi_S}{\rho_{S'} \xi_{S'}}, \tag{2.2}$$

where ρ are the respective normal-state resistivities. To get a grab of the physics in this equation it is helpful to use the following equation for the resistivities

$$\rho = \frac{m}{ne^2\tau}, \tag{2.3}$$

with m the electron mass, n is the DOS, e is the electron charge and τ is the mean time between quasi particle collisions. When plugging eq. 2.3 into eq. 2.2 one finds that γ is proportional to the ratio of DOS in the two superconductors

$$\gamma = \frac{\xi_S n_{S'} \tau_{S'}}{\xi_{S'} n_S \tau_S}. \tag{2.4}$$

The ratio of DOS tells whether the transport is from S to S' or reverse, since particles tend to flow toward places with lower densities. By including ξ and τ the equation takes diffusibility of the superconductors into account. During calculations Golubov introduces a new factor

$$\gamma_m = \gamma \frac{d_{S'}}{\xi_{S'}}. \tag{2.5}$$

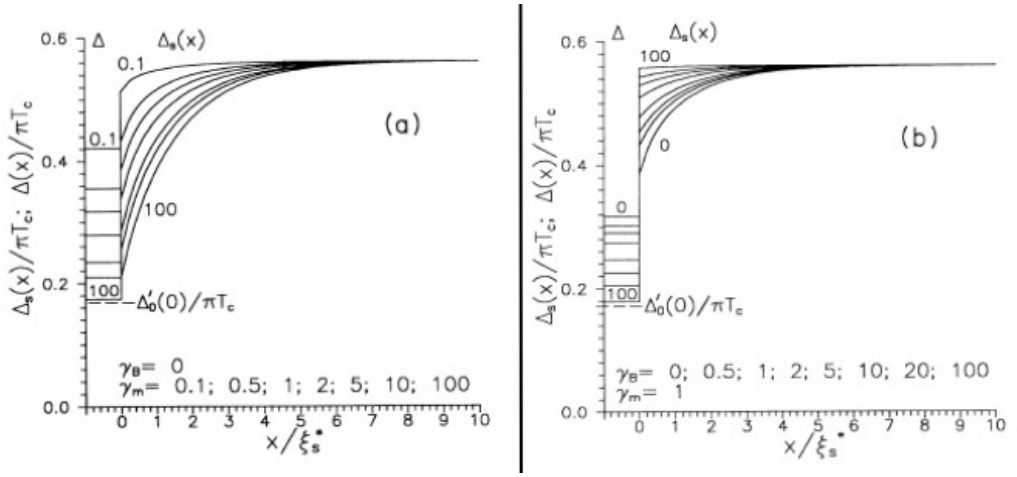

Figure 2.3: *Theoretical estimates made by Golubov et al [9]. Graphs showing spacial varying order parameter in a SS' interface for different γ_B and γ_m. The interface is located at x=0, the S' is located in negativ x region and S fills the positive x region.* ***(a)*** *Shows order paramter in the bilayer of variating Proximity strength γ_m. γ_B is set to 0 while γ_m ranges from 0.1 to 100.* ***(b)*** *Shows how different Boundary transparencies γ_B affect the order parameter in the bilayer. γ_m is set to 1 while γ_m ranges from 0 to 100.*

The order parameter Δ for a SS' bilayer is plotted for different γ_m on FIG 2.3(a). It is seen that Δ is constant in S', which is a good approximation for $d_{S'} \ll \xi_{S'}$. To get the strongest pair potential in S' the graph shows that a low γ_m is preferable. Looking at eq. 2.2 it makes sense since a low gamma is obtained $n_{S'} < n_S$, so most transport is from S to S'. Changing DOS or collision time or coherence length can only be done by changing materials, which was not an option for this project. Eq. 2.5 shows the direct proportionality between γ_m and $d_{S'}$, which is a quantity that can be changed during fabrication. To maximize the pair potential in S', that layer should be thin.
The Proximity strength for the devices documented can be estimated by using bulk values of Al and Nb. Even though it is not a good approximation, it gives an idea of where in γ_m-space the devices are. Bulk values used are from Appendix A, while the thickness of Al in the devices is 10-30 nm:

$$\gamma_m = \frac{\rho_S \xi_S}{\rho_{S'} \xi_{S'}} \frac{d_{S'}}{\xi_{S'}} = \frac{152\Omega nm}{28\Omega nm} \frac{38nm \cdot 30nm}{(1600nm)^2} = 2.4 \cdot 10^{-3} \tag{2.6}$$

This value is very small which would give a strong pair potential in Al, which is exactly what is wanted. Again, one should keep in mind that bulk values probably are a bad approximation.
Boundary Transparency γ_{BN}, is also introduced by Golubov et al [9] and calculated by

$$\gamma_{BN} = \frac{R_B}{\rho_{S'} \xi_{S'}}, \tag{2.7}$$

where R_B is the SS' boundary resistance times its surface area. Recall that for two surfaces with same electrical resistance but different surface area, the larger surface will have a smaller resistance. R_B takes that into account by multiplying by the surface area, thus making it an intrinsic property of that kind of surface interface. The boundary transparency is a factor that compares the resistance of the interface with the resistivity and quasi particle movability of S'. As for the proximity strength, another factor is introduced, by multiplying with same constant

$$\gamma_B = \gamma_{BN} \frac{d_{S'}}{\xi_{S'}}. \tag{2.8}$$

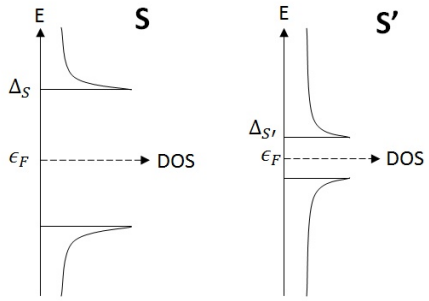

Figure 2.4: *Sketch showing the quasi particle DOS in superconductors with different order parameter Δ. S' with lowest Δ have quasi particle states with energies closer to the Fermi energy ϵ_F than S have.*

Its contribution to the spatial behavior of the order parameter is shown in FIG. 2.3(b). The highest order parameter in S' is obtained by minimizing γ_B. Looking at eq 2.7 and 2.8 this can be obtained experimentally by minimizing the thickness of S' or by having a surface with low resistance. Recalling that the proximity effect is present because of Andreev reflections and the probability for these is highest for low interface resistances, minimizing R_B makes perfectly sense. This value can not be calculated yet because no measurements have been done to measure the Al-Nb-interface resistance.

The reach of the proximity effect

As for the NS-interface, the reach in the SS' case depend on the coherence lengths and impurities of the materials. The Pippard coherence length for low T_C superconductors can be calculated by

$$\xi_0 = \frac{\hbar v_F}{\pi \Delta(0)}. \tag{2.9}$$

This equation shows that stronger superconductors have shorter coherence length, $\xi_S \ll \xi_{S'}$. In the experiments $d_S > \xi_S$ and $d_{S'} \ll \xi_{S'}$. These thickness dimensions give a spatial varying order parameter in S, while it is almost constant in S' as shown in FIG 2.3

Quasi Particle Trapping

Another effect of SS' interfaces is that quasi particles tend to be in the S' material [10]. As shown on FIG 2.4, the S' material have quasi particle states closer to the fermi energy than S has. Thus quasi particles created in the bilayer by microwaves or heat radiation will most likely end up in S', even though they were created in S. If too many quasi particles pile up in S', it would lead to poisoning of the proximitized gap in S'. Poisoning meaning that the gap gets thinner or more soft.

To sum up, low interface resistance is crucial to have a strong proximity effect, both for NS and SS' interfaces. To have a fully proximitized device, the material thicknesses should be on the order of their respective coherence lengths.

Chapter 3

Fabrication

From the theory we know that the length scales needed to have a global proximity effect are on the order of the coherence lengths of the materials used, see Appendix A, which is between nm and μm. This chapter explains how fabrication and measurements of these mesoscopic electrical circuits are done, the machines used and the complications of the process. First, let us look at how the devices should look like.

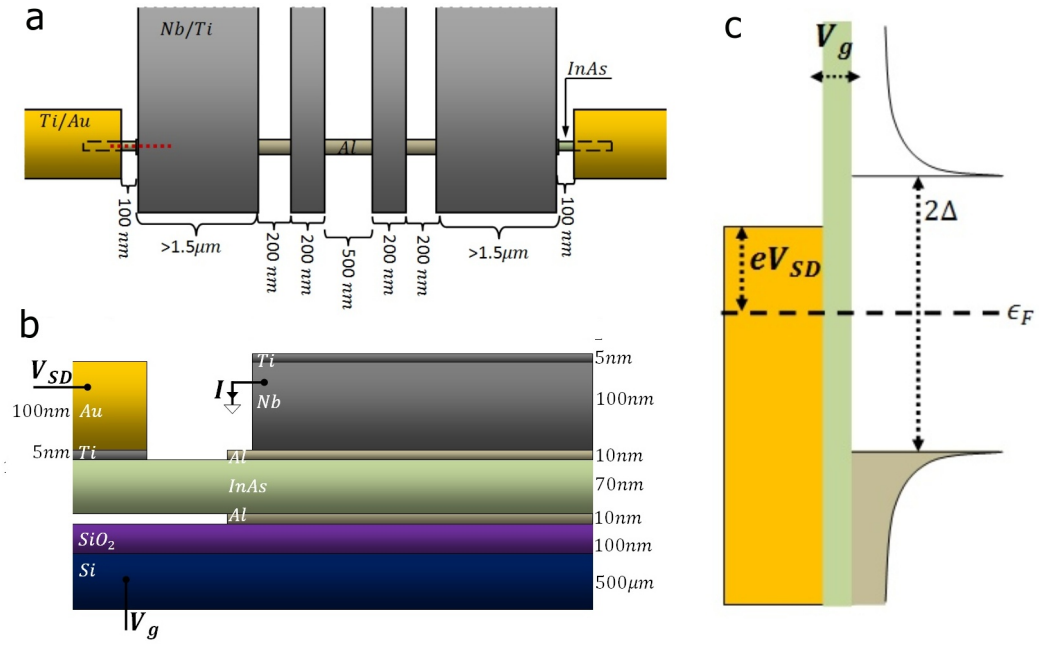

Figure 3.1: ***(a)****Drawing showing the dimensions of the devices as seen from above. An InAs nanowire with Al shell has its shell etched away in both ends. Two Ti/Au contacts are placed on the etched part of the wire,* $\sim 100nm$ *away from the shell edge. Four Nb/Ti contacts are attached to the Al shell with dimensions shown on the drawing. The red line shows the cut of the device shown on (b).* ***(b)*** *Shows the layer structure of the chip, wire and contacts. The foundation of the chip is* $500\mu m$ *P-doped Si topped with* $100nm$ SiO_2*. The wire has a core of* $\sim 70nm$ *InAs with a* $10 - 30nm$ *epitaxial grown aluminum shell. The 100nm thick gold contacts have a 5nm Ti bottom while the 100nm thick Niobium contacts have a 5nm Ti top layer. The chip is bonded so a gate voltage,* V_g*, can be driven across the* SiO_2*. A source-drain voltage,* V_{SD}*, goes from Au to Nb contact. The current is measured before going to ground.* ***(c)*** *Illustration of energy states.* V_{SD} *controls at which energy the measurement is done,* $V_{SD} = 0$ *corresponds to being at the Fermi energy,* ϵ_F*. The measured* dI/dV_{SD} *is proportional to the density of states between the two contacts.* V_g *is used to make a tunnel resistance between the two contacts.*

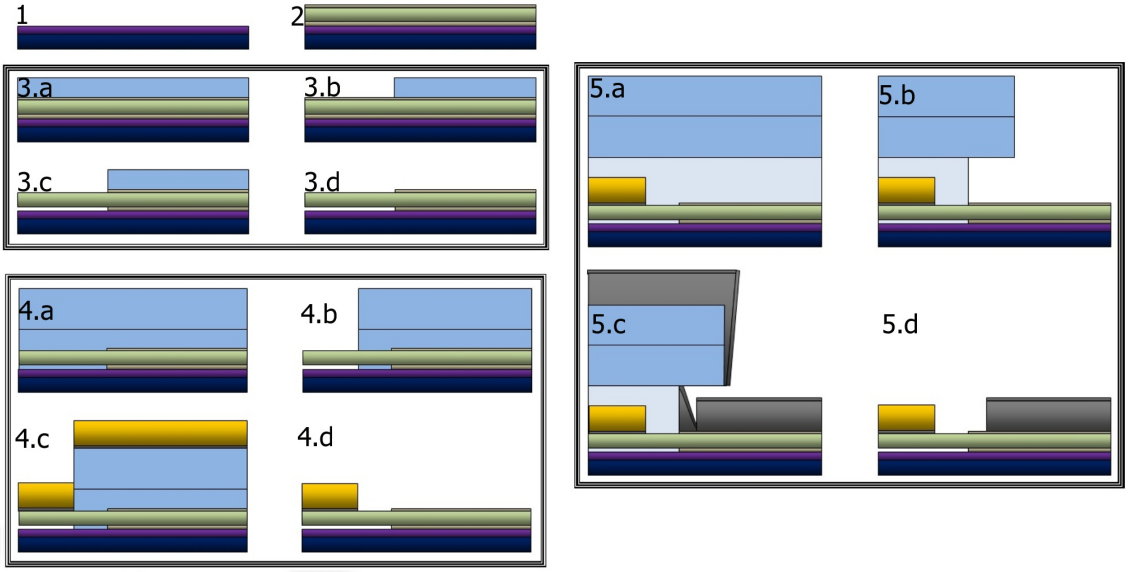

Figure 3.2: *Drawing showing all the fabrication steps from a clean chip (1) to a finished device (5.d). The three lithographic steps (3-5) are divided in four steps:* ***(a)*** *deposit on resist,* ***(b)*** *expose resist and develop on exposed regions,* ***(c)*** *etch or deposit material and* ***(d)*** *remove resist and excess material. The numbers represents the following steps:* ***(1)*** *Having a clean chip.* ***(2)*** *Deposition of wires.* ***(3)*** *Etching wire shells.* ***(4)*** *Deposit Au contacts.* ***(5)*** *Deposit Nb contacts. The reason for using different resists is explained in section 3.6.*

3.1 Device Designs

A sketch of the device dimensions are shown in FIG 3.1(a). The six contacts on the wire are connected to meanders on the chip which go to bonding pads, see FIG 3.3(b), so they can be connected to measurement apparatus. The goal is to do dI/dV measurements of quasi particles in the InAs at different temperatures, magnetic fields and gates voltages. This is why the aluminum shells are removed under the gold contacts, FIG 3.1(b). It is also important that the big Nb contacts does not touch the InAs core, because the desired measurements are the transport through the Al. At the same time, the distance between the Au and the outer Nb contacts should not be to large, since the induced proximity effect weakens over distance. The idea with the four Nb contacts is to be able to measure the interface resistance with 2 and 4 terminal measurements. With the interface resistance, an estimate of the boundary transparency, eq. 2.8 can be obtained.
A gate voltage (V_G) is driven between Si and the wire, see FIG 3.1(b). The SiO_2 is a dielectric, and the Si is highly p-doped, which makes the Si-SiO_2-wire layer a capacitor. By driving a voltage V_g across the capacitor a electric field is made. The only place this field can penetrate is between Au-contact and Al-shell. Applying a negative V_G electrons are removed from the middle of the exposed InAs, creating a tunnel barrier between the normal and the superconducting part, which is exactly what is needed to measure DOS with differential conductance.
The other voltage shown on FIG 3.1(b) is the source drain voltage(V_{SD}) controlling the current from Nb contact through the wire to the Au contact. The current is measured before going to ground. Being at $V_{SD} = 0$ means being at ϵ_F. By sweeping V_{SD} one can control the energy of the measured electrons.

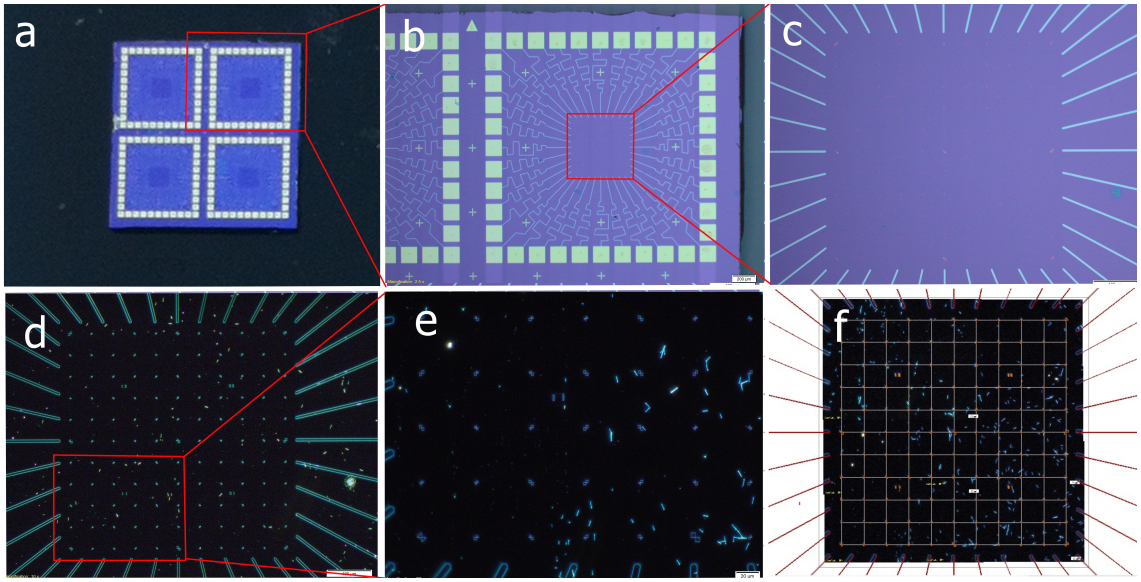

Figure 3.3: *Pictures of a device chip with wires.* ***(a)*** *Shows a picture of the whole chip which is* $5 \times 5mm$. ***(b)*** *Shows a zoom-in of one of the quadrants. Notice the arrow in the top to the left. This defines the direction of the chip. Each of the golden squares is a bonding pad, connected to the meanders going into the middle of the quadrant.* ***(c)*** *Zoom of the middle of a quadrant. The square is* $550 \times 550\mu m$. *No wires are visible.* ***(d)*** *Picture of same location as (c) but now with dark field. The systematic dots are alignment marks, while the things lighting up green are nanowires.* ***(e)*** *Shows a larger zoom of (d), where the nanowires are more visible.* ***(f)*** *Shows 6 pictures of the same zoom as (e) aligned in DesignCAD.*

FIG 3.2 gives a overview of the fabrication steps needed to end up with a device similar to FIG 3.1. There are 5 steps: (1) Have a clean chip. (2) Deposit wires. (3) Etch these wires. (4) Put on Ti/Au contacts. (5) Put on Nb/Ti contacts. FIG 3.2 will be used as a common tread, and will be referred back to through this chapter. Curly brackets are used to simplify the references e.g. {4.*c*} refers to FIG 3.2(4.c). The letters (a-d) are used so that {a} refers to process of putting resist on the chip, FIG 3.2(3.a, 4.a and 5.a).

3.2 Chips for Fabrication

The foundation of these devices are the chips{1}, see FIG 3.3, which were made by Willy Chang. They are made of 500 μm Si topped with 100 nm SiO_2. The chip area is 5×5 mm and it is divided in 4 quadrants, FIG3.3(a). Each quadrant has its own bonding pads and meanders FIG3.3(b). The meanders are curved so they all are equally long and thus have an equal resistance. They go from the bonding pads into the center of that quadrant FIG3.3(c). It is in these quadrant centers that fabrication takes place. Notice the arrow to the upper left on FIG3.3(b), which is used for orienting the chip. Notice also the eight crosses in each quadrant. Each of these have 4 alignment marks around them, used for alignment of the chip in a machine. For more information on the chip see the appendix of Willy's PhD thesis [4]

3.3 Wire Deposition & Identification

The InAs nanowires with epitaxial Al shells are the core of QDevs search for Majorana Fermions in 1D systems. These are special because they have a good interface between a semiconductor and

a superconductor with an experimental reachable T_C, see FIG1.1(c). Two different methods have been used for wire deposition from substrate, which they are grown on, to chip{2}: Mechanical deposition and wet deposition (Explained i Appendix B).
Mechanical deposition is done with a cleanroom wipe and a tweezer. A little triangle is cut of the wiper and picked up with the tweezer, so the sharpest corner points away from the tweezer. The tweezer is used to gently rub the wipe on the substrate with wires, so that wires are attached to the wipe. By rubbing the wiper on a chip, wires are deposited from the wipe to the chip. The placement of wires are more controlled with this process, but the amount of wires deposited can be hard to control. It is recommended to rub the wiper once each place where wires are needed and check the wire density with a microscope before rubbing again. It is easy to add more wires, but harder to remove them again.
The wires are located by a microscope with dark field, see FIG 3.3(d). Dark field pictures of higher resolution, as the one on FIG 3.3(e) are taken so they together cover quadrant centers chosen for fabrication. The alignment marks are used to align the pictures in a program called DesignCAD as shown on FIG 3.3(f). DesignCAD is used to communicate with and orientate the chip in fabrication machines. The wires used for further development is chosen from the aligned pictures. It is not uncommon that mistakes happen when fabricating mesoscopic circuits, so many wires are chosen. The wires chosen should be: long enough for all the contacts $> 5\mu m$, isolated from other wires and as close to the meanders as possible.

3.4 Material Deposition

The material deposition for contacts {4.c & 5.c} was made with a AJA International machine, see schematic FIG. 3.4. This machine was used for three different purposes: Evaporation, sputtering and milling. All these processes are done in the same chamber, with a high vacuum, so it is possible to do several operations on the same sample without exposing it to oxygen.
E-gun Evaporation is a method where materials are heated by electrons until they start evaporate. The materials are located in the bottom of the chamber as indicated by FIG 3.4. The

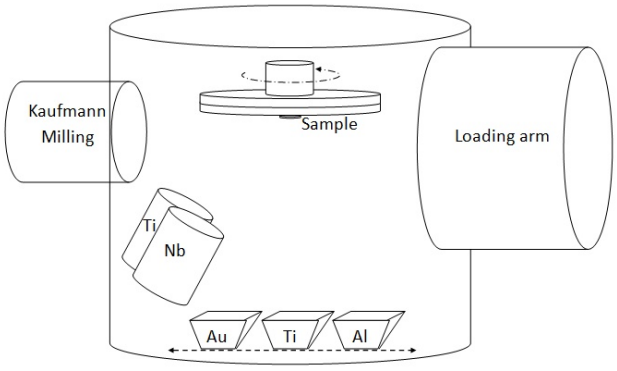

Figure 3.4: *Sketch of the AJA. A sample can be mounted on a sample plate and loaded in situ. The sample plate can be rotated around two axises. One is controlled by a motor and turns the sample in the plan of the sample plate, marked by a dashed arrow. The other rotation is controlled mechanically, and can make the chip face the Kaufmann Milling (KM), the crucibles or the loading arm. KM is an argon gun shooting Ar atoms at a sample turned to face it. The 3 beakers in the bottom are evaporation crucibles. These can be moved right below the sample facing down. The two cylinders to the left are sputtering targets, which contains the materials for sputtering.*

evaporated atoms are moving ballistically in the vacuum until they hit the sample. This method is preferable because the evaporated material can be considered clean and because the procedure is very controllable. A computer keeps count of how much material has been evaporated. Several materials are available, and can be switched between while the sample is in vacuum. The evaporated materials in this fabrication are Ti and Au.

Sputtering is used for those materials who have too high melting temperatures to be evaporated. Instead of heating the material with electrons, ignited argon plasma is fired onto the material. To avoid the plasma to smash into the sample, it is accelerated towards the substrate target by an electric field underneath it where the plasma mashes atoms free from the target. These atoms move directional diffusively towards the sample. The material is sputtered from an angle, so the sample is rotated during sputtering to even out the deposited layers. The diffusivity causes sputtered material to form clusters, which affect the property of the material. Unlike evaporation, the machine don't have a way to measure the amount of material deposited with sputtering, so a calibration is needed. This is done for Niobium, explained below.

Milling is a tool to remove unwanted materials or layers, eg oxide layers, from a sample. The Kaufmann ion-source fires Ar ions at the sample, tearing the outermost atoms off the sample. Dose intensity and length is chosen according to the unwanted material. Using too strong intensity or firing too long will destroy more of the materials than wanted. In this thesis, milling is used to remove AlO_x and $InAsO_x$. These are respectively milled for 3:00 min and 1:15 min, with a pressure of 0.8 mTorr and a flow of 15 sccm (Standart Cubic Centimeters pr. Minute)

3.5 Niobium

Compared to earlier Al-InAs experiments in QDev, this thesis focuses on introducing Nb to increase the overall proximity effect in such systems. Nb is chosen because it is the strongest non-alloy superconductor. A bulk Nb has a critical temperature of $T_C^{Nb} = 9.50K$ which is a lot higher than the one of Al $T_C^{Al} = 1.14K$, see appendix A. Nb has a very high melting temperature (2741 K) which makes it hard to evaporate. This is why it is sputtered. As mentioned in the previous section, one have to make a calibration to know the sputtering rate of a material. Such a calibration was made for Nb: A silicon wafer was cut in many small chips $\sim 5 \times 5mm$. These were mounted and sputtered in the AJA, one at a time, with tiny strips, $\sim 1mm$ wide, of aluminum foil tightened across them. The foil is used to protect parts of the chip from the sputtered Nb. If not put on tight, Nb atoms will diffuse underneath. Using the same settings each time, the chips were sputtered for different time intervals. After unmounting a chip, the foil was removed. The hight difference between the niobium layer and the places protected by the foil was measured with a Profilometer. Results are shown on FIG 3.5(a). A rate of $11.14nm/min$ was found with a linear fit forced through origo.
The diffusivity of sputtering causes the Nb to form nonuniform grains and the sputtered material is considered dirty. Besides reducing the mean free path, it reduces the critical temperature. Others have made experiments on the correlation between T_C and the size of the grains for sputtered Nb[11]. With this correlation our Nb, with a grain size of 10-20 nm, see FIG 3.5(b), has $T_C \sim 8K$.

3.6 Resist

After both evaporation and sputtering, not only the whole chip, but the whole sample plate is covered with the deposited material. This is unfortunate when wanting to do electrical measurements with nm thin contacts like the ones on FIG 3.1. To be able to fabricate such small circuits, a template/mask is needed to protect the chip from a deposited material, like the aluminum foil during sputtering rate calibration. These masks must be precise down to tenths of nm.
Amazingly, such masks are possible to make with resist. Resist is a general word for different

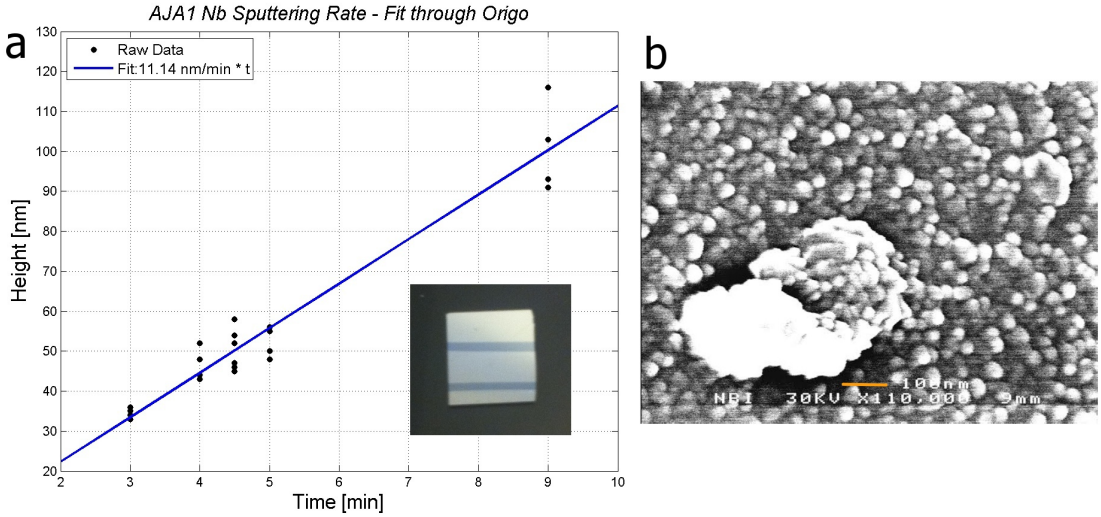

Figure 3.5: *(a)Measurements of thickness of sputtered Nb as a function of exposure time. Five different chips were sputtered on with the same settings but for different time intervals. Height of the sputtered Nb were measured with a Profiliometer. Each measurement point was done in different places on a chip. The linear fit is forced through origin showing a sputtering rate of 11.14 nm/min. In the bottom right corner is a picture of one of the chips used. The two lines are made by aluminum foil, protecting these parts of the chip during sputtering and peeled of after exposure. The height measurements are made across these lines.(b) Close up picture of sputtered Nb from AJA. The orange line is a length scale of 100 nm, indicating that the size of the Nb grains is between 10 and 20 nm. The SEM micrograph is taken by Mingtang Deng, with Raith Eline 100.*

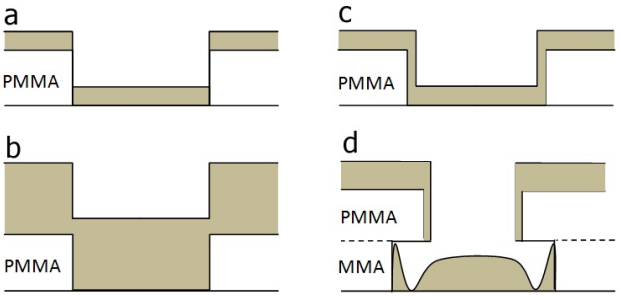

Figure 3.6: *Pictures showing evaporation and sputtering with different resists. **(a)** shows how a device with resist looks after evaporating substrate on it. After liftoff the unwanted substrate is removed as well. **(b)** Shows the problem of evaporating too much substrate, or having a too thin resist. The wanted and unwanted part is connected and liftoff probably won't go well. **(c)** shows sputtering on PMMA. The sputtered material moves diffusively and sticks everywhere, connecting wanted and unwanted material. Liftoff will not go well. **(d)** Double layered resists like these are called shadow masks. The bottom resist is MMA and the top PMMA, which results in a undercut after development. Shadow masks are used for sputtering.*

polymers used for such masks. They get porous when exposed to a electron beam, because the beam cuts the polymers in smaller pieces. When in contact with MIBK (Methyl isobutyl ketone) for 90 seconds, only the porous polymers dissolve. However acetone attacks all the polymers and desolves them after some hours.
To see how resist was put on the device {a}, see Appendix C. To use resists as masks, one needs a very precise electron beam to draw the template. This project used an Elionix ELS-700 which precisely can expose a sample with electron beams with a uncertainty of 20 nm. The template is designed in DesignCAD, which tells the Elionix where to expose on the device with resist. After the exposure the device is put in MIBK to develop the template drawn in the mask{b}. Depending on the dose during the exposure, there might be small pieces of resist left after development. To remove those, and to smoothen the resist, the device can be ashed. Ashing is a process where the device is exposed to a plasma: a combination of oxygen and nitrogen was used. The plasma ashes small fragments of the resist, which are pumped out by a vacuum pump.
There are different kind of resists, and depending on what you want to do with your device, different kinds are preferable, see FIG 3.6. When evaporating, a long polymer (PMMA) was used to make a precise template, see FIG 3.6a. If a thick layer was evaporated, two layers of the same resist was used to avoid FIG 3.6b. When sputtering something on the device a shadow mask like FIG 3.6d was used. It is a double layer resist, PMMA un top of MMA. MMA is a shorter polymer, so less electrons are need to break it down and it gets soluble further away from the electron beam, thus making the undercut. Sputtering on a resist only made of PMMA would resolve in FIG 3.6c. To remove the resist the sample is put in a acetone bath overnight. Next day the sample is sprayed with acetone from the side. This procedure is called liftoff{d}. All the metal only attached to the resist will be removed with it, which is why situations like FIG 3.6b and c want to be avoided.

3.7 Lithographic Steps

A lithographic step is the procedure of putting on resist{a}, expose the resist with Elionix and develop the exposure{b}, etch or expose the device{c} and finally doing liftoff{d}. My devices have 3 lithographic steps, which will be explained in this section: Etching{3}, evaporating Ti/Au contacts{4} and sputtering Nb/Ti contacts{5}.

3.7.1 Etching

When measuring the device it is important that the measured current goes through the semiconductor wire and not the superconducting shell, since it is the properties of InAs that decides whether the device is a candidate for MF or not. This is why the aluminum shell is etched away in the ends of the wire where the gold contacts touch the wire. see FIG 3.1. Etchings are done with aluminum etchant, a chemical which primarily etches Al. To delimit the area exposed to the etch, a mask is made of PMMA and designed in DesignCAD, where only small squares at the ends of the wires are exposed by Elionix. After development and ashing, the wires are etched. The problem with using chemicals for etch (called Wet-etch) is that the chemical can run under the resist, and thereby etch more of the shell than intended. To minimize this, the chip is only in etch for 10 seconds and is quickly transfered into Di-water to wash off the remaining chemical. As explained above, a lot of wires are etched, but only the best are picked for further fabrication. The good etchings are picked by taking Scanning electron microscope (SEM) images of all the etched wires.

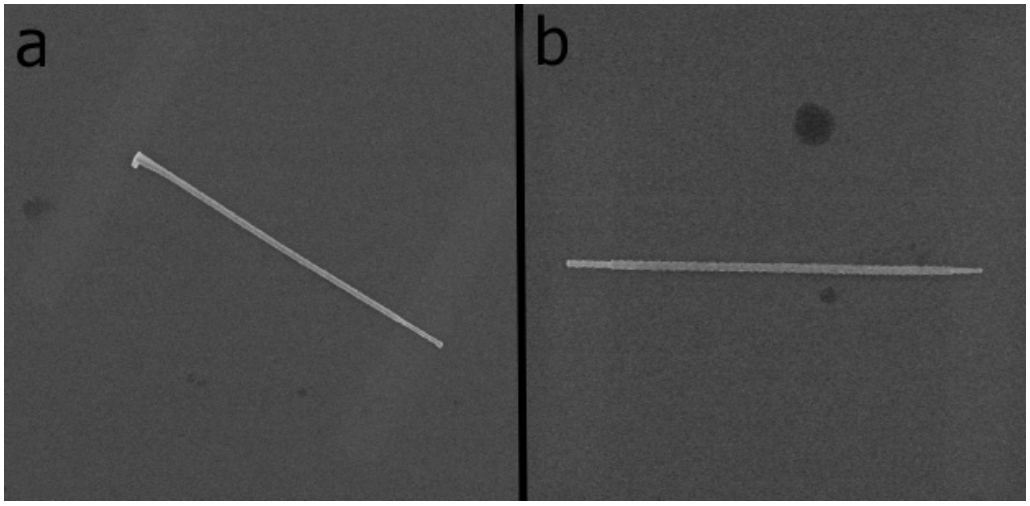

Figure 3.7: *Pictures of two wires $\sim 5\mu m$ after etch, taken with Eline.* ***(a)*** *Shows how a bad etching could look like. The etch windows are a little misaligned to the wire. The edge of the shell is not very sharp.* ***(b)*** *Shows a good etch. Both ends of the wires is etched and the edge of the shells are sharp.*

These pictures are taken with a Raith Eline 100, see FIG 3.7. The Eline is set to save the pictures together with another file which have the pictures location with only few nm uncertainty. This permits an exact placement of the high resolution pictures in DesignCAD for further design of the two next lithographic steps.

3.7.2 Gold Contacts

When the preferred wires are chosen, the mask for the gold contacts can be designed in DesignCAD. This time a double layer PMMA is used to avoid FIG 3.6(b). After the etch, the InAs is oxidized, since it is now exposed to air. This new oxide layer has to be removed before the gold contacts are evaporated on the chip. A oxide layer would result in a large resistance in the InAs-Ti/Au interface, which would influence electrical measurements. To remove the oxide, the InAs is milled. There is a big risk in milling the InAs wires, since their conduction electrons are located close to the surface. If the surface is destroyed by milling, it might ruin the conductive abilities of the wires. After the milling, 5 nm of Ti is evaporated followed by 100 nm of Au. The reason Ti is evaporated before Au is to wet the Au so it is distributed more evenly. Earlier experiments in the group have showed that if Au is evaporated without Ti, the Au tends to form small islands instead of an even layer. This gave bad electrical measurements[4].

3.7.3 Niobium Contacts

Theory tells us that the interface is extremely important for the proximity effect. This fact is very essential for our fabrication methods. The epitaxial contact between InAs and Al is good, see FIG 1.1(c), but the contact between Al and Nb is not necessary good. Unfortunately, Nb cannot be sputtered in the nanowire growth chamber, and the device has to taken out of vacuum. This causes the outer part of the Al shell to oxidize, which increases the resistance in a possible Al-Nb interface, thereby increasing the γ_B, which makes the proximity less effective, recall FIG 2.3. An undercut resist was used, made one layer of MMA and another of PMMA, as shown on FIG3.6(d). To remove the aluminum oxide layer the sample is milled before the Nb is deposited. After the

milling, 100 nm Nb is sputtered on the sample, and to protect the Nb from oxidizing, a thin ($\sim$ 5nm) layer of Ti is lastly sputtered on the Nb. The Ti is sputtered this time to make sure it covers the rough surface of sputtered Nb. Ti will introduce a tiny reverse proximity effect, but because its a thick Nb layer $d_{Nb} > \xi_{Nb}$, the reverse proximity effect shouldn't affect the bottom part facing the nanowire. A oxide layer on the other hand could possibly affect the entire Nb layer. Another favorable affect of the Ti shell is that it acts as a quasi particle trap. When measured on, quasi particle might be created from microwaves or heat excitations. These would diffuse to or stay in the Ti shell because $T_{C,Ti} \ll T_{C,Nb}$, see appendix A.

Chapter 4

Results

One thing is to write about or know how to fabricate a mesoscopic device as explained in Chapter 2, another is to actually fabricate a device that looks right. And ones you got a device that looks good, does not necessarily mean that it actually works as desired. A lot of mistakes can happen, some more fatal than others. Mistakes where you can only blame yourself and others which could not have been prevented. The recipes used is documented in Appendix D. Most of the steps {1-4} had been done before and were mostly fail-safe. An unexpected error happened when making the Nb contacts {5} on generation 1, see FIG 4.1(a). The gold contacts seems fine, while the Nb contacts are connected and are wider than expected. The area between the Nb contacts is brighter because resist is trapped under the Nb shorting the contacts. This happened because the milling of Aluminum oxide also removed a lot of the resist and made it uneven. The combination of an thinner uneven resist and sputtering of a thick layer results in this.
The solution to this problem is to use a new kind of resist: zep520. This resist has a very strong mechanical resistance, but is a little porous. Another change was an extra layer of PMMA. This extra layer makes it harder for the Nb to diffuse into the undercut, which decreases the changes of a bad liftoff. The final resist composition is shown on FIG 4.1(b). Before trying the new resist on a generation 2 chip, some tests were made to test the new resist. Different exposure doses were tried, and the most successful liftoff is shown on FIG 4.1(c).

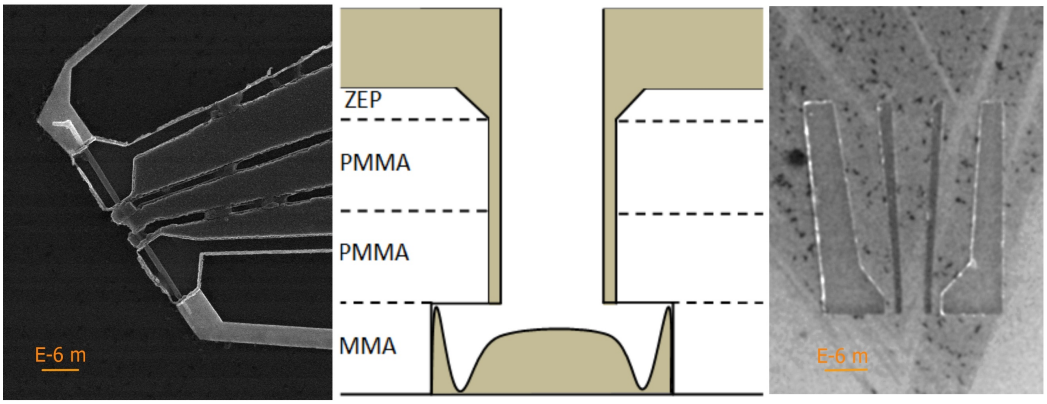

Figure 4.1: *Pictures of Nb contacts after liftoff.* ***(a)*** *Picture of a device on chip generation 1 after Nb liftoff. The two outer most contacts are gold contacts. The 4 Nb contacts in the middle should have been isolated but is connected with Nb. Resist used: MMA/PMMA.* ***(b)*** *Schematic of a new resist used for Nb contacts.* ***(c)*** *Picture of one of the tests of the new resist. Contacts are isolated as they should be. The image is blurred because of dirt and scratches on the chip.*

Chapter 5

Conclusion & Outlook

This thesis explain the theory behind and the fabrication of a InAs-Al-Nb device, designed to be able to induce a hard and wide superconducting gap in InAs nanowires. Earlier experiments have shown a hard but narrow gap in InAs-Al devices. The idea is to use Nb to induce a stronger pair potential in Al through superconducting proximity effect.
Theory of SS' proximity effect explains that two important factors are experimentally changeable without changing materials: The ratio of the thicknesses of Al and Nb and the interface resistance of the Al-Nb interface. To increase the pair potential in Al and thereby InAs, these should be as small as possible.
A device was not finished in time because of complications with sputtering Nb/Ti contacts after milling of AlO_x. An advanced resist was necessary to control the dimensions of the contacts. The new resist was tested and worked as planned. Recipes can be found in Appendix D.

Besides making a functional device and measure it, there are a lot of things to be done. The knowledge from the measurements can be used in the search for Majorana Fermions.
If a device shows a wide and hard superconducting gap, other device geometries, which enables Majorana Fermions to be measured, must be investigated. It is possible to make half-shell nanowires: InAs nanowires with Al only on half of the surface. Nb contacts can be placed controllable on the half of the nanowire with Al shell, so the device is gateable. Such a device might be a Majorana Fermion candidate.
If the devices does not show good results, error analysis must be made, to check where the fabrication went wrong. A candidate for fabrication problems is the milling of the wires. Both too little or too much milling would increase the interface resistance, which is paramount for superconducting proximity effect. Two and four terminal measurement can easily be done with a probestation to check the resistance of the different contacts. This would be a efficient way to check different milling doses if that would be necessary.
Another solution is to avoid milling by growing a gold shell on the aluminum shell in the nanowire growth chamber, to protect the Al from oxidation. The fabrication is not yet mastered, and the gold layer includes some etching problems, and a N layer in between the two superconductors, which might affect the superconducting proximity effect. So this solution has pros and cons.

Generally this topic has a lot of interesting uninvestigated subjects which, with the right facilities, are right for the taking. And who knows, maybe measured Majorana Fermions and Quantum Computations are on the other side of this research.

Appendix A

Element Characteristics

	Type	ξ_0	λ_L	v_F	$H_c(T=0)$	T_C	$\Delta(T=0)$	ρ
Al	1	1600 nm	16 nm	$2.02 \cdot 10^6 m/s$	$105 \cdot 10^{-4} T$	1.140K	$1.7 \cdot 10^{-4} eV$	$28\Omega \cdot nm$
Nb	2	38 nm	39 nm	$0.273 \cdot 10^6 m/s$	$1980 \cdot 10^{-4} T$	9.50K	$15.3 \cdot 10^{-4} eV$	$152\Omega \cdot nm$
Ti	1				$100 \cdot 10^{-4} T$	0.39K	$0.6 \cdot 10^{-4} eV$	$420\Omega \cdot nm$

Appendix B

Wet Deposition & Removing Nanowires from a Chip

To do wet deposition, the substrate with nanowires are put in a beaker with methanol. The beaker is placed in a sonicator with a water bath. When turned on, the sonicator sonicates the water with a frequency proportional to the current going through it. Water waves sonicates the beaker which sonicates the methanol and lastly the substrate. The shaking can cause the wires to be ripped off the substrate. These wires diffuses out in the methanol. With a pipette, controlled amounts of methanol can then be placed on a chip. By carefully drying the chip, wires are now distributed over the chip. It is recommended to do this in several small steps, because the wires are easy to deposit, but not easy to remove again, see below.

There are many ways to remove nanowires from a chip. Most of the efficient ways might also damages the chip. A method that removed most wires was sonication. The chip is put in a beaker with acetone which is sonicated. To remove almost all wires from a chip, sonicator was used in approximately 8 minutes. The wires where not dense on the chip before, and only a couple of wires where left in the fabrication squares (squares on fig. 3.3(d)). Unfortunately two bonding pads lost their gold layer in the process, but the rest of the chip was intact. The process can be done in small intervals of few minutes so the chip can be checked during the process.
Another reason for one to remove wires is that the density of wires in 1-3 of the fabrication squares is too large. If this is the case, start fabricating on the squares with suitable wire densities. During some of the fabrication processes, random wires are ripped of the chip eg. during liftoff. When done with the fabrication on the suitable squares, check the density of wires on the other squares. If its still to high, use a more rough method such as the first mentioned, but have in mind that functional circuits on the chip might be destroyed during these processes.

Appendix C

Spinning Resist

Being able to control the abilities of the resist used to make masks/templates on chips is very crucial. This thesis uses 3 different resists: MMA, PMMA and ZEP. MMA and PMMA are similar besides MMA being shorter polymer chains than PMMA. These are kept diluted in bottles. To be able to differentiate between PMMA and MMA they are labeled as Ax and ELx respectively, where x is an integer. This integer says how many percent of the dilution is resist. A4 is a 1:25 PMMA dilution and EL6 is a 1:16.7 MMA dilution. To have a resist with sharp features, the resist should not be viscous on the chip, so only resist is left behind. This means that a higher solution percentage gives a thicker layer of resist.

Two steps are used to remove the liquid of the dilution: baking and spinning. Baking is done by placing the chip on a hot plate at 185 °C. Spinning is done with a spinner, a machine that is able to spin the chip at thousands of rounds pr minute (rpm). The chip is stuck to the spinner with a tiny vacuum pump, so it does not fall off during spinning.

Here is the whole procedure. Firstly, the chip has to been clean. This is done by spraying acetone on the chip, then isopropanol (IPA) and drying the chip with a air gun. To further dry the chip, it is baked for 4 minutes, which should evaporate unwanted material or liquid. While waiting, chose the desired rotation speed and duration on the spinner. Quickly after baking, place the chip in the spinner and turn on vacuum. The chip is initially set to spin 500 rpm. While at this rotation speed, one drop of resist solution is placed on the chip with a pipette and the chosen spin program is started. The centrifugal force of the high rotation speed throws of a lot of the liquid during the spin. After the spin, the chip is bakes again to boil away the remaining liquid.

If more layers of resist is needed, this procedure can be repeated just after the second bake, but this time no cleaning is needed. Remember to keep a chip with resist away from acetone unless you want to remove the whole resist.

Appendix D

Recipes

This appendix has all the recipes used for making the device. They are written in short form so they can be cut out and brought into lab.

D.1 Resists

Resist for etchings

- Clean chip (Acetone, IPA & Air gun)
- Bake 4 min at 185 °C
- Spin A6 for 60s at 5000rpm - Bake 2 min at 185 °C

Resist for Ti/Au contacts

- Clean chip (Acetone, IPA & Air gun)
- Bake 4 min at 185 °C
- Spin A4 for 60s at 5000rpm - Bake 2 min at 185 °C
- Spin A4 for 60s at 5000rpm - Bake 2 min at 185 °C

Resist for Nb/Ti contacts

- Clean chip (Acetone, IPA & Air gun)
- Bake 4 min at 185 °C
- Spin EL6 for 60s at 5000rpm - Bake 3 min at 185 °C
- Spin A4 for 60s at 5000rpm - Bake 3 min at 185 °C
- Spin A4 for 60s at 5000rpm - Bake 3 min at 185 °C
- Spin ZEP1:3 for 60s at 5000rpm - Bake 3 min at 185 °C

D.2 Exposure of Resists

The exposures was done with a Elionix ELS-700, which is not walked through in this thesis, and the settings written here will not make sense unless the reader knows the machine.

Exposure of resist for etchings

- Dots: 240.000
- bc: 500pA
- wf: 600μm
- Area Dose: 1500 $\mu C/cm^2$

Exposure of resist for Ti/Au contacts

- Dots: 240.000 pixels
- bc: 500pA
- wf: 600μm
- Area Dose: 1500 $\mu C/cm^2$

Exposure of resist for Nb/Ti contacts

- Dots: 240.000 pixels
- bc: 500pA
- wf: 600μm
- Dose time: 15 $\mu s/dot$

D.3 Development

Development of PMMA and MMA exposure

Develop: 90 s in MIBK 1:3 IPA dilution
Quench reaction: 10 s in IPA

Development of Nb/Ti resist exposure

Develop ZEP: 20 s in O-xylene
Develop PMMA & MMA: 90 s in MIBK 1:3 IPA dilution
Quench reaction: 10 s in IPA

D.4 Etch

Prepare 5 beakers, 2 of them respectively with Aluminum Etchant D and DI water heated to 55 °C, 2 others are filled with room temperature DI water and the last is kept empty.

- Ash sample for 30 s
- Wash chip in hot DI water
- 10 s in hot Aluminum Etchant D
- 20 s in cold DI water
- 20 s in cold DI water
- Spray IPA on chip held over the empty beaker, and put it in the beaker (now filled) for 15 s
- Dry with air gun

D.5 Evaporate Ti/Au Contacts

An AJA was used for evaporation.

- **Milling**: 1:15 min, 0.8 mTorr, 15 sccm
- **Evap. Ti**: 5 nm with 30 mA
- **Evap. Au**: 100 nm with 154 mA

D.6 Sputter Nb/Ti Contacts

An AJA was used for sputtering.

- **Milling**: 3:00 min, 0.8 mTorr, 15 sccm
- **Sput. Nb**: 9:00 min, 4 mTorr, 30 sccm, 300 W
- **Sput. Ti**: 0:30 min, 4 mTorr, 30 sccm, 200 W

Bibliography

[1] V. Mourik et al, "Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices", Science vol. 336, pp. 1003-1007, (2012).

[2] M. Leijnse & K. Flensberg, "Introduction to topological superconductivity and Majorana fermions", Semicond. Sci. Technol. 27, 124003 (2012)

[3] S. Takei et al, "Soft superconducting gap in semiconductor Majorana nanowires", arXiv: 1211.1029 (2013)

[4] Willy Chang PhD Thesis, "Superconducting Proximity Effect in InAs Nanowires", (2014)

[5] N.L.B. Ziino et al, "Epitaxial aluminum contacts to InAs nanowires", arXiv:1309.4569 (2013)

[6] G. E. Blonder, M. Tinkham, & T. M. Klapwijk, "Transition from metallic to tunneling regimes in superconducting microconstrictions: Excess current, charge imbalance, and supercurrent conversion", Phys. Rev. B 25, 4515–4532 (1982)

[7] Cherkez, V.; Cuevas, J. C.; Brun, C.; et al, "Proximity effect between two superconductors spatially resolved by scanning tunneling spectroscopy", Phys. rev. X 4, 011033 (2014)

[8] Brammertz et al, "Generalized proximity effect model in superconducting bi- and trilayer films", J. Appl. Phys., vol. 90, no. 1, pp. 355–364, (2001).

[9] A.A. Golubov et al, "Proximity effect in superconductor-insulator-superconductor Josephson tunnel junctions: Theory and experiment", Phys. Rev. B 51.1073 (1995)

[10] A. Zehnder et al, "Proximity effect in Nb/Al-ALO$_x$-Al/Nb superconducting tunneling junction", Phys. Rev. B 59.8875 (1999)

[11] JIN YiRong et al, "Grain-size dependence of superconductivity in dc sputtered Nb films" Sci China Ser G | vol. 52 | no. 9 | 1289-1292 (2009)