Charge noise and stability of foundry-fabricated silicon spin-qubit devices

Bachelor Thesis

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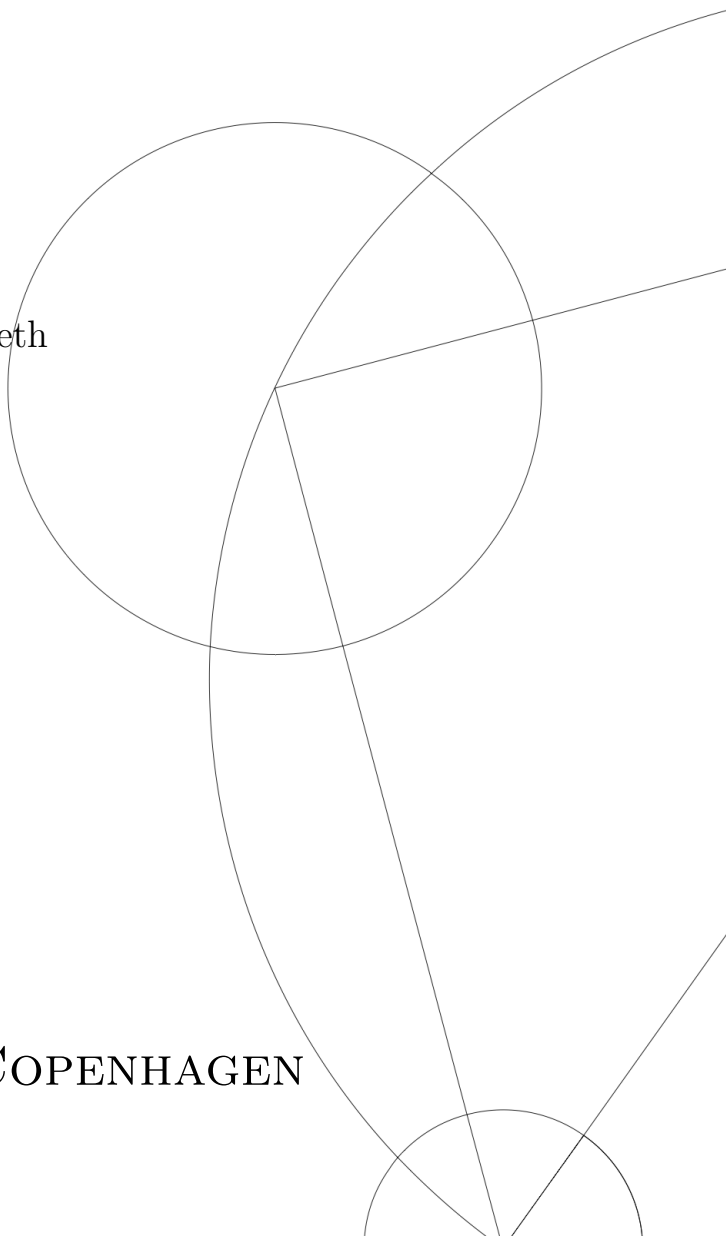

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Abstract

Foundry fabrication of gate-controlled silicon devices provides a tantalizing approach to massive spin-qubit production. Unlike classical transistors operating at room temperatures, such quantum devices cannot easily be simulated, and must be characterized experimentally at sub-kelvin temperatures. In this thesis, devices fabricated by two different foundry processes were compared in terms of their gate behavior and charge noise, namely planar SiMOS devices with multiple gate layers, and single-gate-layer Si/SiGe heterostructures. From DC and lock-in transport measurements performed at temperatures below 100 millikelvin, we obtained barrier pinch-off characteristics, Coulomb blockade diamonds, as well as current noise, which we convert into effective gate-voltage noise (charge noise). Overall, the stability observed in several devices were not as good as the best previous devices implemented in foundry-fabricated silicon-nanowire devices, although more statistics would be useful to compare different platforms. Specifically, the SiGe devices showed high amount of instability and large amount of charge noise. Some of the SiMOS devices showed very good stability and charge noise as low as $5.5 \frac{\mu eV}{\sqrt{HZ}}$, which is slightly above state-of-the-art non-foundry Si/SiGe devices. While the Si/SiGe platform requires more work to improve the stability of the devices, we were able to tune up double quantum dots in the SiMOS devices, making these devices good candidates to explore spin-dependent effects next, such as Elzerman-type readout and spin relaxation measurements.

Contents

1 Introduction

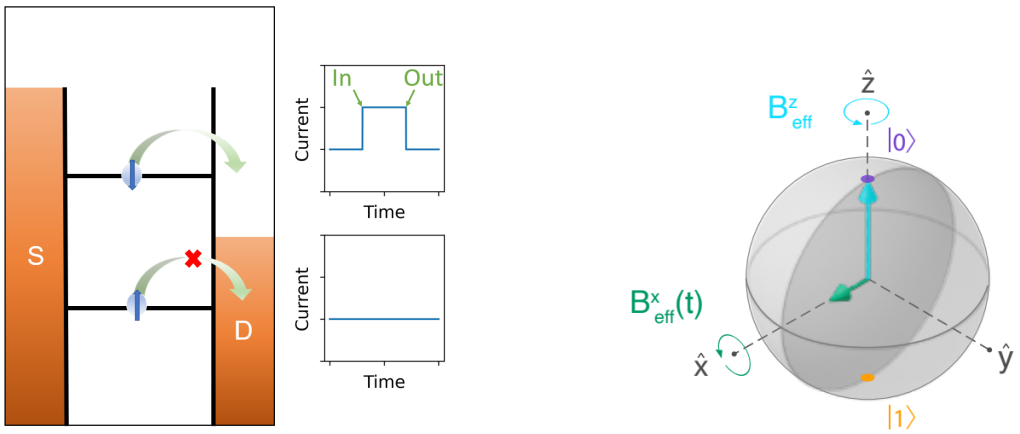
In recent years the complexity of scientific problems has been increasing rapidly, and current classical computers are not able to keep up with this increasing complexity in terms of computation power. There is therefore a need for something that would be able to compute such problems in a time much faster than currently possible. One potential candidate to help scientist tackle these complex systems and problems would be the field of quantum computing. In this field the goal is to be able to utilize quantum mechanical phenomena to reach a significant improvement in computational complexity, when compared to current classical computers [1].

To perform quantum computation certain requirements have to be fulfilled, and they are the following :
1) The system needs to be scalable and have well defined states that can be differentiated between.
2) The system needs to be able to initialize all the states to the same initial value, thus creating a baseline reference point.
3) The coherence time of the system needs to be larger than time to compute a unitary gate to avoid computational errors.
4) A universal gate set that can manipulate the states in the system, so that they can reach any allowed value, needs to exist.
5) The state at the end of the measurement needs to be obtainable.
These requirements are known as the DiVincenzo criteria [2].

2 Spin Qubits

A platform which meets all the requirements of the DiVincenzo criteria uses spin-based qubits defined in quantum dots. Spin qubits utilize the spin of electrons as their well defined differentiable states, since an electron's spin is either spin-up or spin-down. There are also multiple configurations of spin qubits, but the most simple one, in terms of the amount of quantum dots, would be the Loss-DiVincenzo configuration [3]. This configuration also fulfills all of the DiVincenzo criteria. It has well defined states when a static magnetic field is applied to it, as a result of the spin states being split because of the Zeeman effect. This allows for one state being the higher energy state and the other being the lower energy state. We can then use this difference in energy to initialize the spin qubits to a specific state. One way to achieve this is by connecting two reservoirs of electrons to a confined region where only discrete tunneling is allowed. One platform which allows us to do this is a quantum dot, and it will be explained further in section 3. This can be done by tuning the barriers that confine the quantum dot, in such a way that both spin states would be allowed to tunnel onto the dot, but only the higher energy state would be allowed to tunnel out of the dot.

But to know that the spin qubit is initialized to the state we want, then we need to be able to measure the electrons on the dot due to Coulomb blockade. To do this we need to have a method of charge detection near the spin qubit, e.g by measuring a current. The way we can do this is by either coupling the spin qubit to a quantum point contact or another quantum dot which is sensitive to the electrostatic changes [4]. By doing this it allows for measurement of the spin qubit system's state, since we can then distinguish between the high and low energy state. When measuring the current of the charge detector we would expect to see an abrupt change of current, or a "blip", if we



(a) (b)

Figure 1: Loss-DiVincenzo spin qubit (a) Diagram of the electrochemical potential, showing that the higher energy state is allowed to tunnel to the drain, while the lower is not. (b) Bloch sphere showing a time varying magnetic field $B^x_{eff}(t)$ rotates the state around the x axis, while a static magnetic field B^z_{eff} rotates it around the z axis [3]

load an electron of the higher energy state, since then we would allow for the electron to tunnel onto and off the quantum dot. The same logic can then be in contrast, we expect no "blip" when loading an electron of the lower energy state, since this electron would be stuck on the quantum dot due to Coulomb blockade. An illustration of this energy splitting and the theory of how the charge sensing works can be seen in Figure 1, and the platform which allows us to do this will be explained further in section 3.

To manipulate the spin states we need to use more than the static magnetic field which facilitates the Zeeman splitting of the spin qubit. One way to gain complete control of the spin state would be to have a smaller transverse AC magnetic field in addition the the previous static magnetic field. We can illustrate this using a Bloch sphere, which is a representation of pure states of a two-level quantum system. An illustration of this is shown in Figure 1. Each point on the sphere represents a unique quantum state $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ The illustration also shows what effect the different magnetic fields would have on the state. The static magnetic field rotates any state around the quantization axis (blue arrow), which does not do anything to the basis states $|0\rangle$ and $|1\rangle$. Whereas the AC magnetic field rotates states around an axis perpendicular to the quantization axis (green arrow) [3].

Such AC magnetic fields can be generated using a nearby ESR antenna, or by employing effective magnetic fields generated by spin-orbit coupling or micro magnetic structures.

3 Quantum dots

As mentioned previously the way we can isolate these spin qubits is by forming quantum dots, which is an object confined in all spatial dimension, thus allowing for localization of electrons to a well-defined small region in space and the possibility of single electron transport. A quantum dot can be seen as an artificial atom, since it has some of the same properties when it comes to electrons. But before we are able to investigate the properties of a quantum dot, we need to fabricate one. To create a quantum dot we need to confine it in all spatial dimensions. One way to achieve this is by the construction of a 2D electron

gas (known as a 2DEG), which is an interface between two different semiconductors with different bandgaps, where the two semiconductors are engineered in such a way that it is only in the interface that there are any mobile electrons at low temperature. It is then possible to further confine the 2DEG by designing a gate layout that allows for precise manipulation of the electrostatic potential in the 2DEG plane. To allow for quantized charge tunneling, more conditions need to be met. We can describe the quantum dot as a circuit, which is displayed in Figure 2. When we have a quantized amount of electrons on the quantum dot, then the charge on the dot is defined by Ne. Where N is an integer describing the amount of electron on the dot, and e is the elementary charge. If tunneling from the source to the drain is allowed, then the amount of charges on the dot would be related to the energy of the system, since the most optimal state of the circuit would be where the energy was minimized. This then means that if we want to add another electron to the quantum dot, then some energy is required, and this energy is the charging energy, which is given as

$$E_C = \frac{e^2}{C} \tag{1}$$

where C is the total capacitance of the system. This energy is generally very low, and therefore it is important that the system is cold to be able to observe these discrete states. The reason for this is because if the thermal energy of the system is equivalent or larger than the charging energy, then we would lose the ability to tunnel discrete charge states onto the quantum dot, because now the energy needed can be supplied by the thermal energy.

Another condition for quantized charge tunneling is the barriers being sufficiently opaque. This means that the barriers needs to be strong enough that they pinch of the transport between the source and the quantum dot, and from the quantum dot to the drain. The restriction for these barriers can be found when looking at the typical time to charge or discharge a quantum dot, which is just an RC circuit. This time is given as $\Delta t = R_t C$.

If we then apply both the energy and time we just found and look at them using Heisenberg's uncertainty relation we get the following: $E_c \Delta t = R_t C \frac{e^2}{C} = R_t e^2 > h$. This shows a restriction imposed on the resistance of the system. Taken into account the two criteria we just defined, we can get the following two equations

$$R_t >> \frac{h}{e^2} \tag{2}$$

$$\frac{e^2}{C} >> k_B T \tag{3}$$

Equation 2 says that the tunnel resistance needs to be much larger than the resistance quantum, which is $\frac{h}{e^2} = 25.813$ kΩ. Equation 3 say that the charging energy needs to be much larger than the thermal excitation, since if this isn't true then the electrons would be able to populate the quantum dot due to thermal fluctuations, and we therefore lose control of the quantization of charge. [5]

3.1 Coulomb blockade

A quantum dot formed in a 2DEG has some very interesting properties, which stem from the discrete charge states. As described previously the electrons tunnel on and off

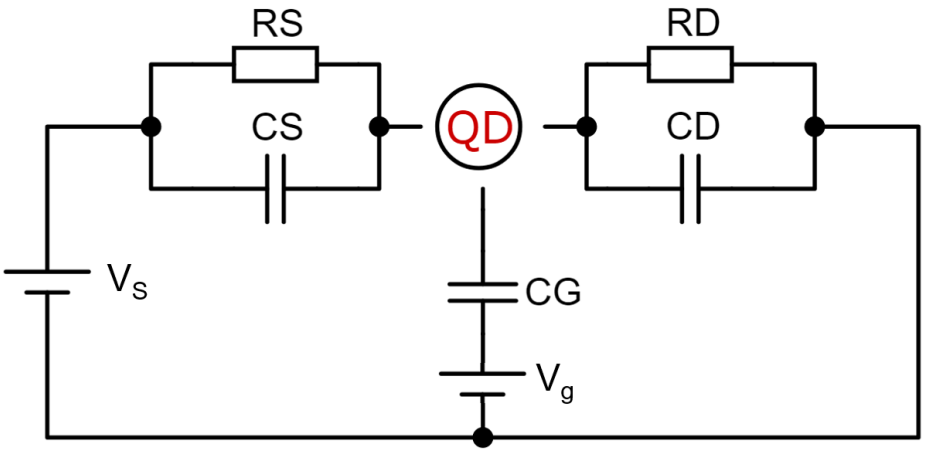


Figure 2: Circuit Diagram of a quantum dot, the tunnel junctions consist of a resistor and capacitor connected in parallel, and the gate is defined by a single capacitor.

the quantum dot using two tunnel junction, one connecting the dot to the source and one connecting the dot to the drain. The way to control the amount of electrons on the dot is using a gate electrode. By then increasing or decreasing the voltage on this gate electrode, it then allows for either population or depopulation of the quantum dot respectively. When the source and drain potential is at resonance, then there is only current flowing through the device when the source/drain potential aligns with energy of an electron state. This can also be seen from Figure 1a. The regions between states therefore have no current flow, and are what we describe as Coulomb blockade. If we apply a source/drain bias on the gate electrode, then we are able to observe so called Coulomb diamonds, which can be seen in Figure 6 and 11. These Coulomb diamonds allows for extraction of valuable information about a quantum dot. We can extract the charging energy by looking at the height of the diamonds, which is the source/drain space. If we then extract half the height, then this is equivalent to the charging energy, shown in equation 1. The same energy can also be found by looking at the width of the diamond, which is the gate voltage space. Here an extra variable is needed which we call the gate lever arm α. This is because the ratio or conversion between the source/drain bias and the gate voltage is given by the following equation

$$|V_{SD}| = \frac{|V_G|}{\alpha} \tag{4}$$

Since we are able to extract the charging energy, then we can also find the total capacitance of the system, and using the slopes of the diamonds we can convert this to the source, drain and gate capacitance. The reason we can do this is since the total capacitance of the system is given as $C = C_G + C_S + C_D$, where C is the total capacitance, C_G is the gate capacitance, C_S is the source capacitance and C_D is the drain capacitance. [4]

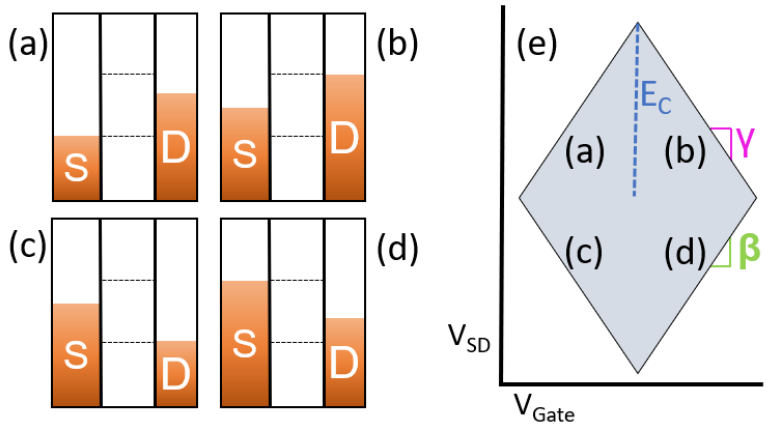


Figure 3: Source/Drain alignment at each slope in a Coulomb diamond. For actual data obtained in this regime, see Fig. 6

At the positive slopes (β), then the chemical potential of the source aligns with either the upper or lower of two different states, depending on if the positive slope is at positive or negative bias voltage, shown in Figure 3.a and 3.d. When following the positive slope, this can then be seen as a "sweep" of the the chemical potential of the drain. It goes from a lower state to an upper state for a positive bias voltage, and it goes from an upper to lower state for a negative bias voltage. The same concept also applied for the negative slopes (γ), but here it is just swapped, so the fixed chemical potential is the drain and the one being "swept" is the source,shown in Figure 3.b and 3.c. These slopes are useful for extracting the capacitance of the system, since they relate to them as follows

$$\beta = \frac{C_G}{C_G + C_D} \tag{5}$$

$$\gamma = \frac{C_G}{C_S} \tag{6}$$

β and γ can also be refereed to as the lever arms for the drain and source respectively. This also means that they relate to the total lever arm of the system as follows $\frac{1}{\alpha} = \frac{1}{\beta} + \frac{1}{\gamma}$ [6].

3.2 Scalability of $<$ 10 qubit devices

Industrial-scale production and research foundries, such as Interuniversity Microelectronics Center (IMEC) and Laboratoire d'électronique des technologies de l'information (CEA-Leti), have previously been instrumental in the evolution and improvement of fabrication methods for electronic circuits. One such example is their large contribution to the field of Complementary metal–oxide–semiconductor (CMOS) devices, used to construct integrated circuits, as well as their effort in developing photonic integrated circuits [7].

These foundries have recently begun using their expertise on the development and fabrication of integrated circuits, to fabricate qubit devices. If there is success in the field of foundry fabrication of qubit devices, this would be a substantial step towards the realization of large-scale quantum computers. It has already been shown that it is indeed possible to form quantum dots and have individual electron control [8], in nanowires developed using CMOS technology. The performance of these are not yet on par with

what can be achieved with fast-turnaround university-fabricated devices, but it shows that it is indeed a promising endeavor [9]. Using fully-depleted silicon-on-insulator processes, nanowires hosting quantum dots have also been produced and measured. These also show capabilities of charge sensing, by having one nanowire act as a sensor which detectes the charge state transition in another nanowire [10]. Similar devices have also shown low charge noise in the range of $1.1\frac{\mu\text{eV}}{\sqrt{\text{Hz}}}$ at 1 Hz, as well as the electron exchange in a 2x2 qubit array [11]. Other foundry fabricated spin qubit devices have also show the ability of spin readout as well as a long maximum relaxation time of 9 ± 3s [12]. Thus showing that devices fabricated this way could allow for low-error quantum computations.

4 Devices

In this project three different designs of devices were investigated and measured; two were devices based on a silicon–germanium (SiGe) heterostructure, while one was based on silicon metal–oxide–semiconductor (SiMOS). All the devices were fabricated in IMEC's 300 mm fab. It should also be stated that the SiGe devices were fabricated with a preliminary flow. Figure 4f shows the design of the heterostructure. If we look at the design from left to right, then we first have the gate layer, where the control gates has been fabricated onto. Then there is a 8nm gate oxide that separates the gates from a 1nm Si cap. The Si cap is then separated from the 8nm quantum well by a 20nm SiGe layer. The rest of the layer beyond the quantum well is another layer of SiGe. The Ohmic contacts are connected to both the Si cap and the quantum well.

4.1 Single gate layer SiGe devices

Two different designs of SiGe devices were investigated, and both had a single gate layer design. The overview of all the SiGe devices can be seen in the appendix Figure 16, and here we see the two different design, one labeled as 24_x_x (Vertical devices) and another set of devices labeled as 16_x (Diagonal devices). Both the diagonal and vertical devices were measured.

4.1.1 Vertical device

The design of the vertical device contains a SET, which is the left part of the device (black dot), and a double dot, which is the right part of the device (red dots). The SET and double dot is separated by a barrier which is labeled as the CM gate. In this project only the SET was investigated. The design of the SET has the following gates, accumulation gates (ASS and ADS), barrier gates (BTS and BDS), "control gates" (CTS and CDS) and the top gate (ST). The quantum dot which will be formed in this SET is meant to reside near the tip of the ST gate. The accumulation gate's role is to supply electron that can tunnel onto the quantum dot, and the barrier and control gates can be used to pinch off the quantum dot. The design is displayed in Figure 4b. Here we also see the desired location of the quantum dot of the SET, marked by a black dot, and the desired location of the double dots, marked by red dots.

4.1.2 Diagonal device

The design of the diagonal device contains a SET, which is the top left part of the device (black dot), and a double dot which is the bottom of the device (red dots). The SET and double dot is separated by the BSD and BT gates. The design follows the same as the vertical device, so accumulation gates, AS and AD gates, are used to supply electrons to the quantum dot. The barrier gates, BSR and BSL, are used to pinch off the quantum dot, and the dot is desired to be formed beneath the ST gate. The design is displayed in Figure 4a Here the desired location of the quantum dot of the SET, marked by a black dot, and the desired location of the double dots, marked by red dots. The orange dot is where we suspect the dot to actually be, based on data presented below.

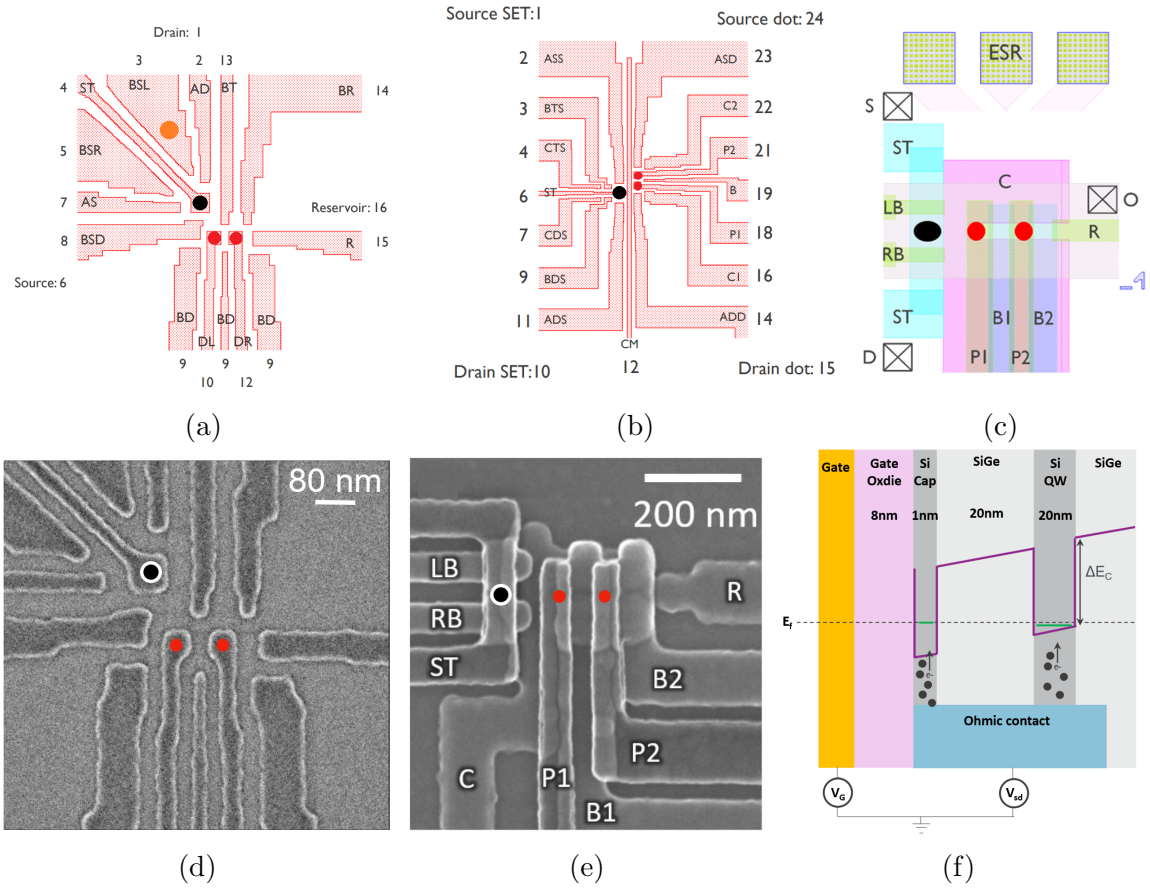


Figure 4: Device designs. The red dots in (a), (b), (c) and (d) are the desired positions of the double dots, and the black dot is the desired position of the SET quantum dot (a) Gate design of the Diagonal SiGe device. The orange dot is the inferred position of the SET quantum dot. (b) Gate design of the Vertical SiGe device (c) Gate design of the SiMOS device. (d) Scanning electron microscope (SEM) image of a similar diagonal SiGe device. (e) SEM image of a similar SiMOS device (f) An illustration of the SiGe heterostructure used for the devices. All illustrations shown in this figure were provided by IMEC.

4.2 Multi-gate layer SiMOS devices

The SiMOS device has an overall design similar to the SiGe devices. We still have one part of the device which is an SET while the other part is a double dot. The biggest difference

is the use of a multi gate layer, and also the different material of the heterostructure. An electron spin resonance (ESR) antenna is also placed in this device, and the purpose of this is to perform spin manipulation. A SEM image of the device with the ESR antenna is shown in appendix 9.3, and we can see how the ESR antenna is designed to create an oscillating magnetic field when an AC current is applied to it. The device has three different ohmics, which are all connected to highly n-doped regions. The source and drain ohmics allow transport through the SET, and ohmic "O" supplies electrons to the double dot. The SET consists of a top gate (ST) and two barrier gates (LB and RB). During operation of the SET a positive voltage is applied to all gates related to it. The double dot part of the device has 5 different gates used to operate it: An accumulation gate (R) connecting the dots to the reservoir of the ohmic "O". A barrier (B2), which separates the right dot from the reservoir and the other barrier (B1), which separates the two quantum dots. Two plunger gates (P1 and P2), which control the chemical potential of left and right quantum dot respectively. A back gate (C) is used in fine-tuning the device when tuning up the double dot. Figure 4e shows an SEM image of a typical device.

5 Experimental Techniques

5.1 Experimental Setup

For this project the devices were cooled to ≈ 30 mK using an Oxford instruments Triton dilution refrigerator. When tuning and operating the device a QDAC was used to apply voltage and the current was measured using an Ithaco 1211 current preamplifier and a Keysight 34465A digital multimeter. For troubleshooting of leaking gates a Keithley 2614B sourcemeter was used to both apply voltage and measure current. Differential conductance was measured with an Stanford Research Systems SR380 lock-in amplifier. BNC cables were used to connected the QDAC to the breakout box, for each gate a 1.9 MHz low pass filter was used between the QDAC and breakout box. A divider was used between the QDAC and the breakout box for the source of the devices, and an AC DC adder was connected between the QDAC and lock-in amplifier, to apply the sine wave from the lock-in and the bias voltage from the QDAC simultaneously. An illustration of the setup is shown in Figure 5.

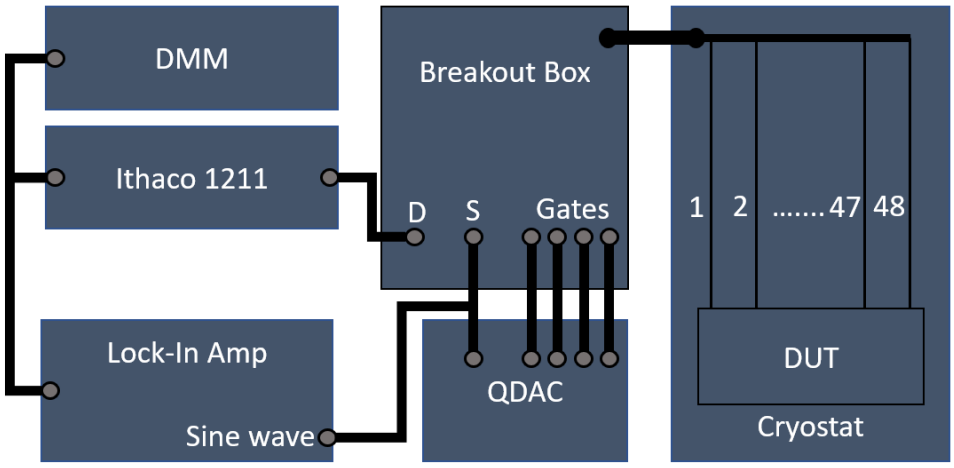


Figure 5: Measurement setup

5.2 Procedure for characterizing multiple similar SiGe SETs

The procedure for measuring the SiGe SETs were done the same way for all devices. The same process was also used to activate the SET of the SiMOS device.

For all devices the first step was to check for leakage current. This was done by applying no bias to the specific gate, while all other gates were grounded. The current of the same gate was then measured, and if it exceeded a the baseline current then it was investigated further for leakage. This was done by floating nearby gates, to try and find a combination that would result in the current going back to the baseline again. This would then inform which gates it was leaking to.

If no gates were leaking then to tune up the SET and two different tune up processes was performed. The first process consisted of applying a bias to the source, and then ramping all other gates with a positive voltage, until activation of the device was reached, evident as a rapid increase in conductance. Then the barriers were pinched off, by reducing their voltage, to try and reach Coulomb blockade.
For the second process a bias was also applied to the source, but here only the gate responsible for creating a path for the current was ramped to a positive voltage, until activation of the device was reached. For the vertical device the gates responsible for creating the current path were the accumulation gates and the ST gate, and it was assumed it was also the accumulation gates and ST gate of the diagonal device which would be responsible for creating the current path. Then a negative voltage was applied to the barriers to pinch of the device, in an attempt to reach Coulomb blockade. If potential Coulomb blockade was seen when pinching off the barriers individually, then a 2D map was created of a barrier/barrier plot, an example can be seen in Figure 7b and 12b. From these a position inside this Coulomb blockade region was chosen and then the plunger gate was swept alongside the bias voltage, in an attempt to measure Coulomb diamonds. The plunger gate was then lowered to try and reach the first electron regime. In this process well-defined Coulomb diamonds were chosen as candidates for measuring charge noise. Charge noise was measured at 4 different points at a Coulomb peak, the left flank, the peak maximum, the right flank and a position off the peak in Coulomb blockade. The stability of the device over time was also measured at these position, by acquiring time traces of an increased duration.

5.3 Method for determining charge noise and stability

The desired frequency bandwidth for the charge noise measurement were in the range of 10^{-1} Hz $-$ 10 Hz, since we were interested in the noise at 1 Hz. We can therefore define our upper and lower bound for our bandwidth as follows. The lower limit for the bandwidth is determined by the duration of the measurement, therefore since we want to measure a lower limit of 10^{-1} then we need to measure for at least $T = \frac{1}{10^{-1}} = 10$ s. To make sure we also get to see the data at 10^{-1} Hz then we measured for longer than the minimum time, where the time used were 100 s. The upper limit of the bandwidth is defined from the Nyquist theorem. Since we want to see the noise at 10 Hz then we again oversampled to make sure we can see the frequency. To do this we first calculated the maxiumum rise time needed of the Ithaco pre-amplifer, with the closest corresponding rise time being 1 ms (BW 160 Hz). This was then again oversampled by the multimeter using a sample rate of 1600 samples per second, thereby satisfying the Nyquist theorem. It states that the sampling frequency needs to be twice as fast as the signal you want to measure, so $f_s = 2f_0$, where f_s is the sampling frequency and f_0 is the desired frequency

to measure [13]. This set the upper limit of the bandwidth as $f_s = 2 \cdot 1600$ Hz $= 3200$ Hz, which is a time between each acquisition of 300 μs. The final bandwidth we therefore have with these settings are 10^{-2} Hz $-$ 160 Hz.

To measure the stability of the devices, longer time traces were acquired. Here a rise time of 10 ms was used on the Ithaco and a PLC of 1 was used on the DMM, which is equivalent to 20 ms integration time on the DMM. This results in a low noise measurement, since we are then only sensitive to noise below 8 Hz. This then allows for measurement over a long period of time, where we then can see if there are any charge jumps from the device, which is a measure of stability.

6 Characterization of SiGe devices

All measurement shown in the results for SiGe devices were taken from vertical devices, the device shown in figure 4b, except measurements from section 6.5. The devices measured were from the wafer AL902605 Die 2.

6.1 Device activation and barrier pinch off

The activation of the SiGe devices showed an increase in activation threshold over time. The measurement were acquired over a span of 2 weeks, and the voltage for activation ranged from 0.8 V to 1.6 V. As can be seen in Figure 7a, the first change of threshold voltage was substantially larger than subsequent threshold changes, section 8.2 covers the potential cause of this. Figure 7b shows that the combination of BDS and CDS pinches off the device at -200 mV while we see that BTS and CTS exceeds beyond -200 mV. In this range clear Coulomb blockade is visible, indicated by the diagonal lines.

6.2 Coulomb diamonds

The barrier and accumulation gate settings used to measure the analyzed Coulomb diamond was -20 mV on CDS and BDS, -210 mV for CTS and BTS, and 865 mV for the ASS and ADS gate. The exact diamond used to extract various information was the one between 855 mV and 862 mV in ST gate space, which is also shown in Figure 6. The center of the diamonds had an offset of around -0.45 mV. The tip of the diamond in positive bias voltage lies at 1.65 mV and the tip at negative bias voltage lies at 2.55 mV. Knowing that half the height of the diamond can be converted to the charging energy, we can utilize equation 1 to find the total capacitance of the quantum dot. The charging energy was extracted to be $E_C = 2.1$ meV and from this a total capacitance of $C = 76.3$ aF is obtained. The total lever arm can then be extracted using the width of the Coulomb diamond and equation 4. The width of the diamond was found to be 16 emV, using this and the charging energy gives a lever arm of $\alpha = 0.333$. Equation 4 also applies to the relation between the total capacitance and the

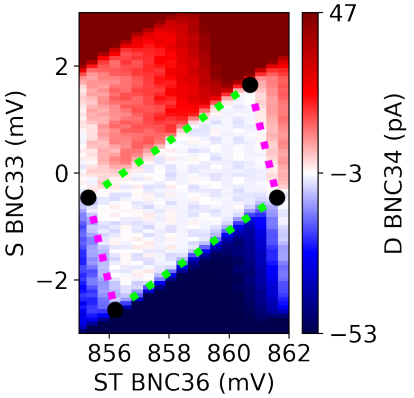


Figure 6: Close-up of the SiGe Coulomb diamond used to extract data. The lime green lines represent the slope β and the magenta lines represent the slope γ. Data acquired from device D21 10B (T2) 24_3_3.

gate capacitance, using the lever arm we therefore get
$C_G = 25.4$ aF. To find the slopes of the diamond, 4 different point were defined and the slope of connected point were calculated. This resulted in the drain lever arm to be $\beta = 0.389$ and the source lever arm to be $\gamma = 2.33$, this indicates that the dot is positioned closer to the source than the drain. A reason for this higher coupling to the source than drain, could be due to the barriers CTS and BTS being pinched off more than CDS and BDS. Utilizing these lever arms in equation 6 and 5, the final capacitance's can be extracted. The source capacitance was $C_S = 10.9$ aF and the drain capacitance was $C_D = 40.0$ aF.

On the left side of Figure 7c it shows the diamonds fading out, and there is no longer any states that the source and drain can be at resonance with, at 0V bias. This indicates that we are in the few electron regime at this point, and potentially at the first electron regime or simply too small tunnel rates.

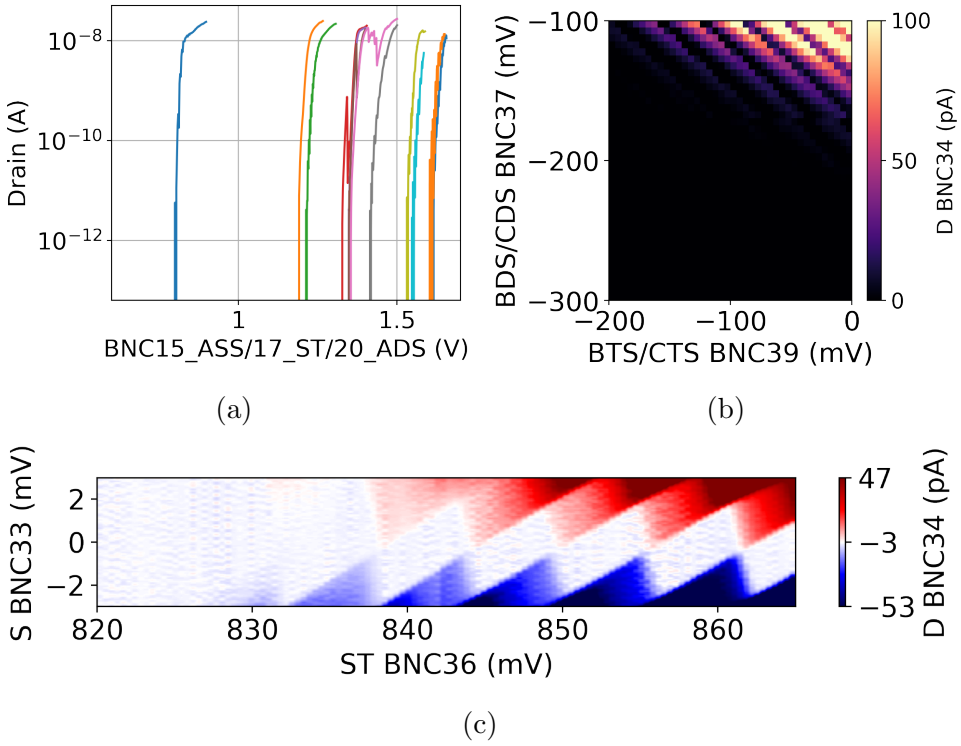


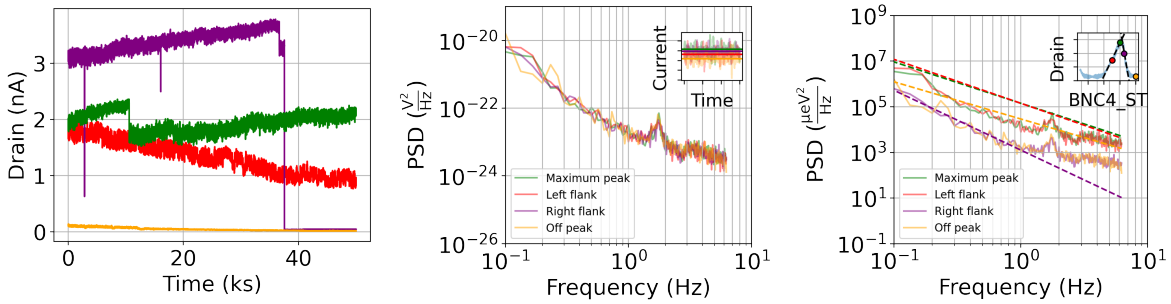
Figure 7: (a) Gate sweeps of the accumulation gates and the ST gate, this results in "activation" of the device allowing for current to flow through the SET. The lines show gate sweeps taken at different days over the span of two weeks, indicating an increase in activation threshold. Bias = 1 mV (b) Barrier sweep showing diagonal features indicating Coulomb blockade (c) Coulomb diamonds possibly reaching the few-electron regime. Data in Fig. (a) was acquired from D22 10A (T1) 24_2_3, data in Fig. (b) and (c) was acquired from D21 10B (T2) 24_3_3.

6.3 Charge noise and device stability

To calculate the power spectral density (PSD) used to quantify charge noise the following was done. The time traces were split into 10 equally large segments, then the fast Fourier transform (FFT) was taken for each segment, and then the product between the FFT and its complex conjugate was calculated. This value was then normalized using the frequency

bin. The final result is then found by averaging all the segments together, yielding an averaged PSD of a specific time trace. This PSD was then plotted in a double log scale plot. Figure 8c shows the PSD of a SiGe device. The settings used when measuring time traces for SiGe device was not the same as the ones mentioned in the methods section. Here an acquisition time of 80ms was used, resulting in an upper bound of 6.25 Hz.

The stability traces, shown in Figure 8a, shows 4 measurement at different point of a Coulomb peak. The initial measurement was set as follows, the red trace was the left flank of a peak, the green trace was the peak maximum, the purple was the right flank and the orange was off the Coulomb peak. As can be seen the currents measured for each does not correspond with the expected value they would have, with the expected current being green > red = purple > orange. The reason for this is due to a large charge jump, which resulted in the Coulomb peak being moved during the measurements.



(a) (b) (c)

Figure 8: (a) Time traces from different positions of a Coulomb peak, due to large charge jump the position of each trace is shifted (b) 100s time traces converted to a power spectral density in units of $\frac{V^2}{Hz}$. Inset: time traces (c) Power spectral density in $\frac{\mu eV^2}{Hz}$ with $\frac{A}{f^\beta}$ fit. Values of β in fits on graph (c) descending order of its legend: 1.81, 1.92, 3.15, 1.63. Data acquired from device D21 10B (T2) 24_3_3.

6.4 Localization of the quantum dot formed in the SET of vertical device

To establish that the dot was on the ST gate and between the two accumulation gates, a sweep of the two accumulation gates was performed, which is displayed in Figure 9b. Here we see two diagonal lines with the same slope, which shows that the coupling between the two accumulation gates is the same. This indicates that the quantum dot indeed has formed between the accumulation gates, and therefore is underneath the ST gate. Afterwards we also check if the barriers acts as a top gate, or if it is only the ST gate that acts as a top gate. The result from this is shown in Figure 9a. Here we again see these clear diagonal lines, indicating that the quantum dot is coupled to both the ST and the Barriers. This shows that only when the barriers and ST are at resonance with each other then current is allowed to flow. Therefore the barriers indeed do not work as an extra top gate.

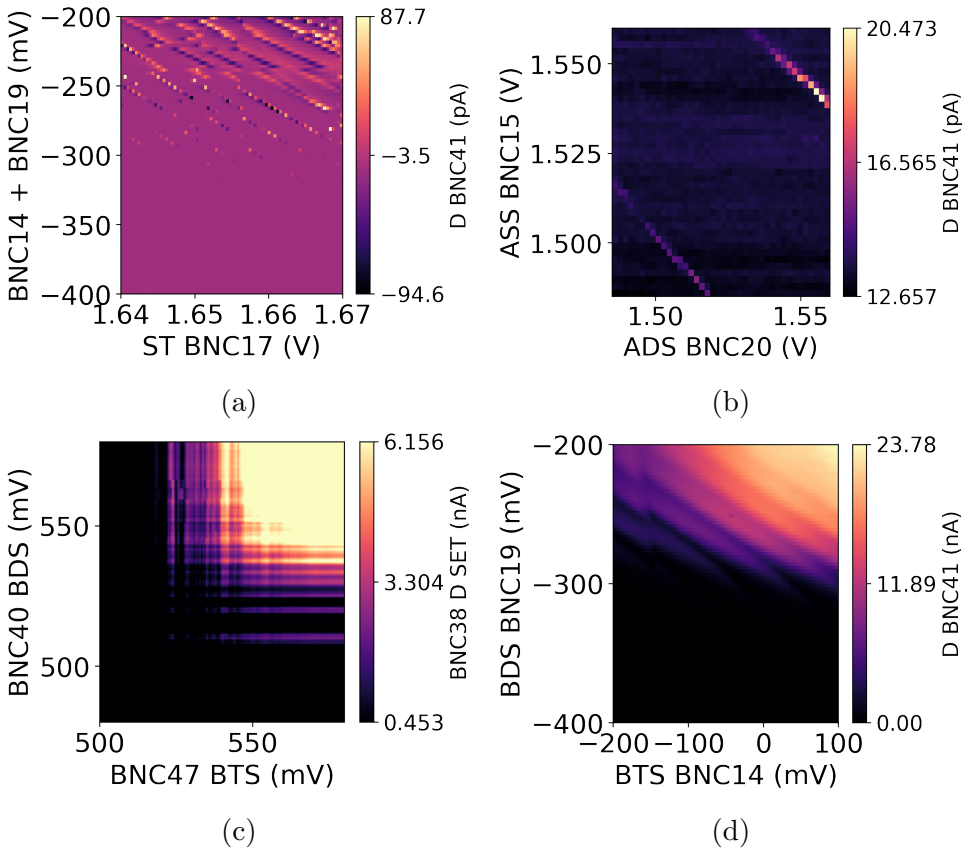


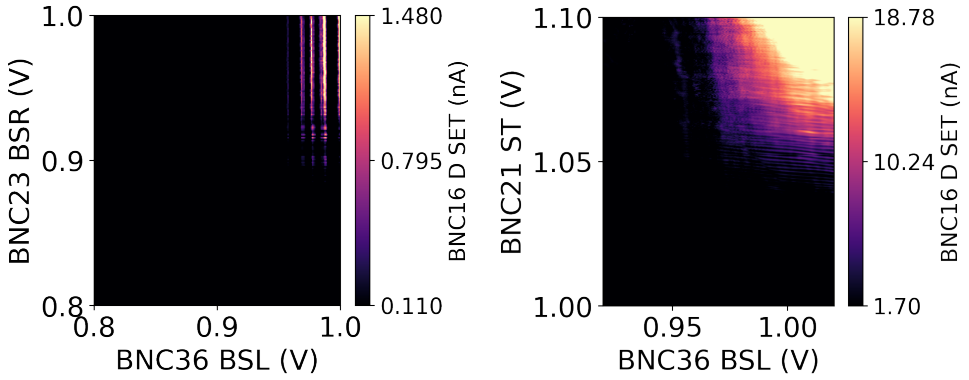
Figure 9: Gate sweeps to localize the quantum dot. (a) Sweeps over the ST gate and barriers. The voltage displayed for the barriers indicate the value for BNC14, while the voltage on BNC19 is larger by 0.3 V, so $V_{BNC19} = V_{BNC14} + 0.3$ V. (b) Sweeps over the accumulation gate to verify that the quantum dot is located between the barrier gates. (c) Barrier/barrier sweep of a vertical device with positive voltage on all gates. (d) Barrier/barrier sweep of a vertical device while only operating the accumulation gates and ST gate at a positive voltage. Data from Fig. (a), (b) and (d) was acquired from device D22 10A (T1) 24_2_3. Data from Fig. (c) was acquired from device D21 10B (T2) 24_4_2.

Figure 9c shows the results of a barrier plot while applying only positive voltages to the vertical devices gates. Here we see that BDS pinches off at around 510mV and BTS pinches of at 520mV. Both barriers seems to be strongly coupled to the dot, but there is no sign of Coulomb blockade. This indicates that the quantum dot hasn't formed beneath the ST gate. Comparing this to when a positive voltage is only applied to the accumulation gates and the ST gate, we get a barrier plot looking like 9d and 7b. This shows that by only applying a positive voltage to the accumulation gates and ST gate, then only a low or negative voltage is needed to observe Coulomb blockade.

6.5 Localization of the quantum dot formed in the SET of diagonal device

Figure 10b shows a sweep of the BSL gate and the ST gate of a diagonal device. During this measurement all gates of the SET were at a positive voltage. The horizontal lines, which only have a slight vertical slope, show strong coupling between the ST gate and

the quantum dot, while there is only a slight coupling between the quantum dot and the BSL gate. The two barriers of the device were also swept, which is displayed in Figure 10a. Here we see a strong coupling to BSL while there is almost no coupling to BSR. These two measurments together indicate that the dot is formed somewhere in the upper part of the device, since it can be controlled by BSL and the ST gate. The orange dot in Figure 4a illustrates the possible position of the dot.



(a) (b)

Figure 10: Measurements of a diagonal design device where a positive voltage is applied to all SET gates. (a) Barrier/barrier sweep showing a strong coupling to BSL. (b) Sweep of the barrier gate BSL and the ST gate. Date for Fig. (a) and (b) was acquired from device D20 10B (T3) 16_3.

7 Characterization of SiMOS devices

All measurement done on SiMOS was taken from a single device (QBB16_3_5). The measured device was from wafer AL00126614 D21 D21 D1SD5.

7.1 Device activation and barrier pinch off

The activation of the SiMOS device showed no increase in activation threshold over time. In Figure 12a two measurements are shown, the blue curve was the first activation of the device and the orange curve was measured two weeks after. For both measurements the first signs of an increase in current is at 550 mV, while if we look at the point at which the current reaches 100 pA the orange curve is at 605 mV gate voltage, while the blue curve is at 625 mV gate voltage. There is therefore no significant change in the activation threshold, indicating a stable device. The barriers of this device were also tested, and the results can be seen in Figure 12b. Here we can observe clear Coulomb oscillations in the range 300 mV to 500 mV for both gates, with the thresholds of RB being slightly higher than LB.

7.2 Coulomb diamonds

The methods used for extracting the lever arm and capacitances from the SiGe samples were also used on the SiMOS samples. The tuning of the device was a voltage of 400 mV on barriers RB and LB. The rest of the devices gate were at 0mV. Here the diamond used was the one between 700 mV and 720 mV in ST gate space, and Figure 11 shows a close-up of the Coulomb diamond. The bias offset was -0.07 mV, and from 0 mV bias to the positive tip was 0.53 mV and to the negative tip was -0.67 mV. This yields a charging energy of $E_C = 0.6$ meV. From this a total capacitance was calculated to be $C = 267$ aF. The width of the diamond was 16 meV, and using this value and the charging energy results in a lever arm of $\alpha = 0.0375$. This then yields a gate capacitance of $C_G = 10.1$ aF. Analyzing the slopes gives a drain lever arm of $\beta = 0.075$ and a source lever arm of $\gamma = 0.075$. This then allows for calculation of the final capacitance, where the drain capacitance was found to be $C_D = 123$ aF and the source capacitance was $C_S = 134$ aF.

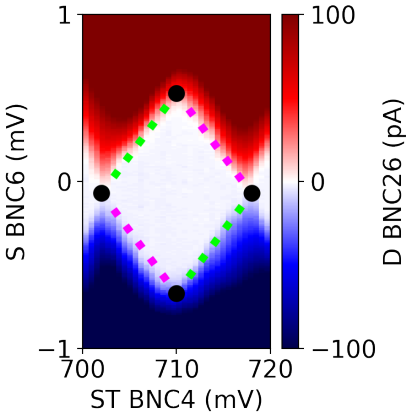
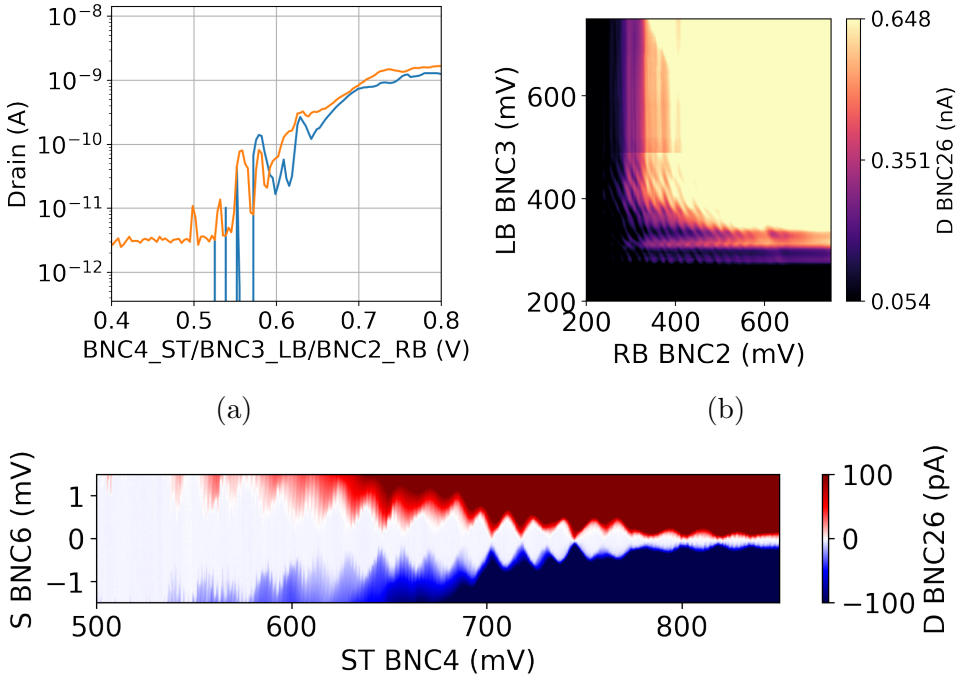


Figure 11: Close-up of the SiMOS Coulomb diamond used to extract data. The lime green line represent the slope β and the magenta line represent the slope γ. Data acquired from device QBB16_3_5.



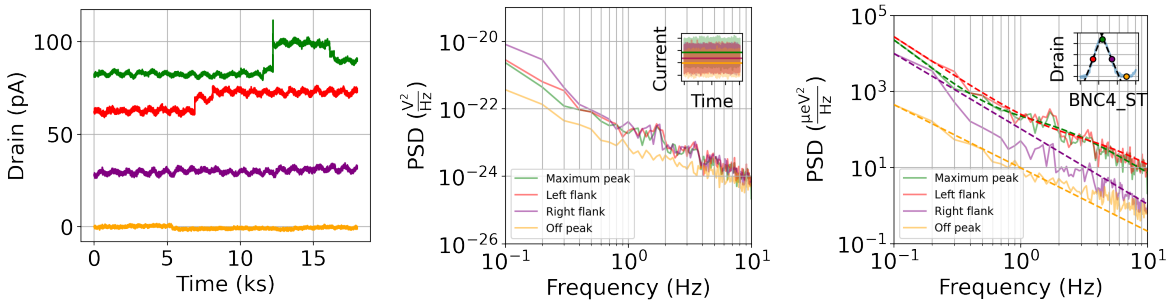
(a) (b)

(c)

Figure 12: (a) Activation of the SiMOS device in log scale. Bias = 0.3 mV. (b) Barrier sweeps of SiMOS showing clear Coulomb blockade at the region where the voltage on the barriers are approximately 400 mV. (c) Coulomb diamonds of a SiMOS device. Data acquired from device QBB16_3_5.

7.3 Charge noise and device stability

The process of converting time traces to power spectral densities, was the same for SiMOS as it was for SiGe. The only difference is the setting used, for SiMOS the optimal settings explained in the methods section was used. Figure 13c shows the PSD of SiMOS in the range from 0.1 Hz to 10 Hz. Stability traces of a Coulomb peak were also measured for SiMOS. This is shown in Figure 13a, here we see the largest jumps in current was approximately 20 pA, while being at the maximum of a Coulomb peak. A jump of 10-15 pA was also spotted when taking the time trace at the left flank of the device.



(a) (b) (c)

Figure 13: (a) Time traces of SiMOS devices taken on different position of a Coulomb peak. (b) 100 s time traces that has been sorted into 10 equally large windows averaged together, converted to a power spectral density in units of $\frac{V^2}{Hz}$. Inset of time traces used in top right corner (c) Power spectral density in $\frac{\mu eV^2}{Hz}$ with $\frac{A}{f^\beta}$ fit for the purple and orange trace, and a $\frac{A}{f^\beta} + \frac{B}{\frac{f^2}{f_c^2}+1}$. Values of β in descending order of the legend is : 2.53, 2.14, 1.98, 1.66 and the value of f_c for the green trace is 1.90 and for the red trace it is 4.73. Data acquired from device QBB16_3_5.

The plot showing the higher frequencies, Figure 14, shows the power spectral density based of 3 different points on a Coulomb peak, 1 point off the Coulomb peak, 1 measurement with a BNC cable which was connected to a channel on the breakout box, that wasn't connected to the device, and the last measurement is the results from connecting nothing to the ithaco. The peak at 50 Hz is from the power line. The peak at 72 Hz which only showed up for this device is a result of a lock-in amplifier which was connected to the source of the device, since the sine wave applied with the lock-in amplifier was 72 Hz. From all these peaks we also see their harmonics, which results in the 72 Hz lock-in noise polluting the signal with noise from instrumentation.

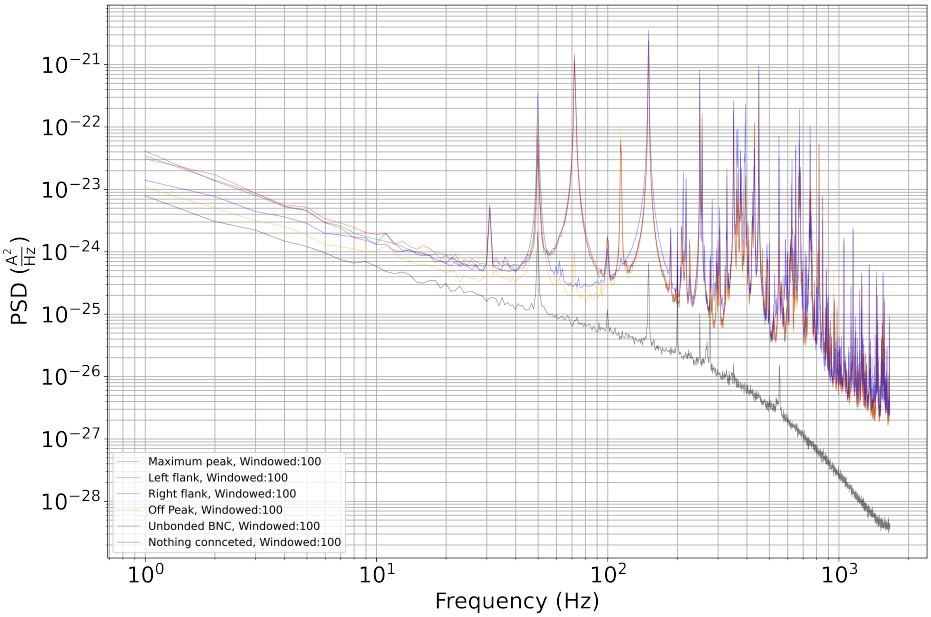


Figure 14: Higher frequency power spectral density using 100 windows averaged together, resulting in 1 s time traces. Data acquired from device QBB16_3_5.

7.4 Tuning up a double dot

A double quantum dot was also tuned up in the SiMOS device. For readout of the stability map shown in Figure 15, the SET was tuned to the flank of a Coulomb peak. This results in it being sensitive to changes in the double dot of the device, which allows for readout of the double dots, since we see no charge jumps, the transitions are remarkably regular and their visibility is good across a wide range of gate voltages. This gives flexibility when performing qubit operations. The process to tune up the double dot was to firstly tune the left dot, then the right. To tune up the left dot, the right dot was conducting to allow access to the right reservoir. When looking at the stability map, then the vertical lines indicate a change of the electron population of the left dot, while the horizontal lines indicate a change of electron population of the right dot. The diagonal transitions between the dots then represent transport of an electron from one dot to another.

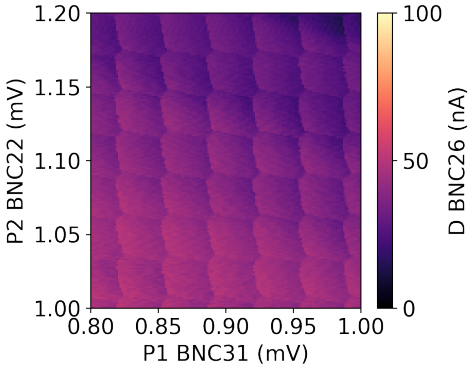


Figure 15: Plunger sweeps of the double dot in the SiMOS device. Data acquired from device QBB16_3_5.

8 Discussion

8.1 Quantum dot properties

The capacitances of the quantum dots can be used to estimate their size. When comparing the total capacitance's of these SiGe and SiMOS devices, then we can see a large difference

between the two. SiGe had a total capacitance of 76.3 aF while SiMOS had one of 267 aF. If we assume that the quantum dots are isolated disk, then we can approximate their size using the equation $r = \frac{C}{8\epsilon_r \epsilon_0}$, with ϵ_r being the dielectric constant with a value of $\epsilon_r = 11.7$, and ϵ_0 being the vacuum permittivity $\epsilon_0 = 8.85 \cdot 10^{-12} \frac{\mathrm{F}}{\mathrm{m}}$. This results in the radii of SiGe and SiMOS quantum dot measured in this thesis is respectively $r_{SiGe} = 92.1$ nm and $r_{SiMOS} = 322$ nm. The SiMOS quantum dot is therefore 3.5 times as large as the SiGe quantum dot. Comparing this to other literature we see that sizes for SiGe in the order of $r = 29$ nm is possible [14], and for SiMOS dots of the size $r = 38$ nm [15] and $r = 16$ nm [16]. We also see that the SiGe has a larger coupling to source than the drain, which can be seen from the lever arms. The Coulomb diamond of the SiMOS device shows that it is coupled equally to the drain and the source.

8.2 Hysteresis and stability of SiGe devices

As seen from Figure 7a and 8a, the SiGe devices were not very stable and they had frequent large charge jumps. Some of the charges might have been pulled up into the Si cap, which can be seen on Figure 4f. If this has happened then the charge would be screening the device from the gate, which would results in a higher gate voltage being needed to activate the device. This issue was seen in multiple of the SiGe devices and was a common issue when working with them. When parked on a Coulomb peak then it could also be seen that the current drifted substantially, as can be seen in Figure 8a. Comparing this to the SiMOS device, then it had no substantial change in its activation voltage over an entire cooldown, as can be seen from Figure 12a, and the device was stable as can be seen from only small charge jumps in Figure 13a. The SiMOS also showed no signs of drift, but there was an approximately 1 mHz oscillation when parked on a Coulomb peak. The reason for this oscillation is yet unknown.

8.3 Charge noise comparison

From the graph at Figure 8c we see that the noise at 1 Hz for the SiGe sample was in the range $120 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$ to $38.7 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$. For the SiMOS sample we can from Figure 13c see that the noise at 1Hz ranged from $8.37 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$ to $5.48 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$. If we compare these values with other literature, then it is clear that they are above average, in terms of the noise level. E. J. Conners measured the same value to $1 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$ at 1 Hz, in Si/SiGe quantum dots [17]. E. Chanrion measured a value ranging approximately between $0.89 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$ and $2 \frac{\mu\mathrm{eV}}{\sqrt{\mathrm{Hz}}}$, depending on if it was measured on the left or right flank of a Coulomb peak respectively. This was in a CMOS device. [18]. This indicates the noise measurement from our devices might have been from instrument or fridge noise. An example of this is also shown in appendix 9.2, which shows a comparison between measuring the noise with the pulse tube on and with it off. This results show around a factor of 10 difference when looking at the 1 Hz noise, which does indeed indicate that a large part of the noise measured in this thesis was due to instrumentation noise.

8.4 Gate Design

When comparing the barrier design, then if we start by looking at the performance of the diagonal device barriers, which can be seen in figure 10a and 10b. Here the two barriers could not be used to pinch off the dot from each side, since the position of the quantum

dot was not at the desired region, as compared to vertical SiGe devices, Figure 7b, and SiMOS devices, Figure 12b. Both of these design were able to reach Coulomb blockade, and each barrier could pinch off the device separately. The range in which the barriers of the SiGe device could pinch off was when applying a negative voltage, while the SiMOS where able to pinch off by just reducing a positive voltage.

8.5 Leakage of SiGe and SiMOS devices

The measurements performed in this thesis were done on multiple devices. There were therefore some devices which are not included in the thesis, since they had leakage from crucial gates. For the vertical SiGe devices a total of 11 devices were measured, with five showing leakage from crucial gates. In addition to the leaking gates, one device formed double dots instead of a single dot on-top of the ST gate, three could not pinch off the device using the barrier gates. For the diagonal SiGe devices a total of two devices were measured and none of them had leaking gates, but none of the were able to form a quantum dot at the desired location. For the SiMOS devices a total of two devices were measured, where one them had leakage from crucial gates. The percentage of vertical SiGe devices which functioned was 18%, of diagonal SiGe devices 0% and for SiMOS 50%. The diagonal SiGe devices and the SiMOS devices had a low sample size, making the result from these potentially very inaccurate.

8.6 Outlook

From the work done in this thesis, it can be seen that both of these device platforms, are not yet ideal in term of characteristics, when compared to previous foundry fabricated devices. For both devices it was observed that they had a larger charge noise at 1 Hz and larger sized quantum dots, when compared to other foundry fabricated devices. Comparing the SiGe and SiMOS devices investigated in this thesis, then it shows that the SiMOS device generally outperformed the SiGe devices in most areas. The SiMOS device had lower noise, and were more stable but had a somewhat larger quantum dot size. The SiGe devices also had more leakage and barriers which were not working as intended. From this we can therefore say that the SiGe devices are currently still unstable and need more work in term of device stability and gate layout for the diagonal SiGe devices. The SiMOS devices were stable and good potential candidates for future investigations.

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9 Appendix

9.1 SiGe device overview

Figure 16: Locations of several SiGe Devices and their bonding pads on chip A and chip B. ID of SiGe wafer: AL902605 Die 2. Image provided by IMEC.

9.2 Pulse Tube PSD

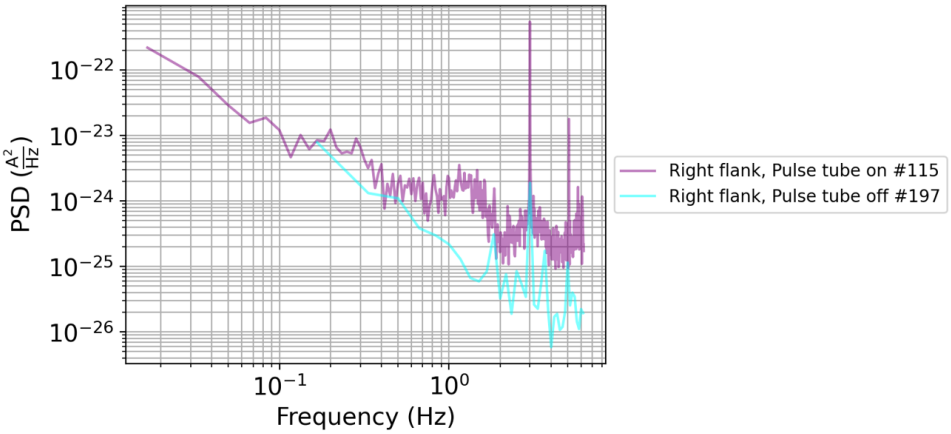

Figure 17: Noise spectra, as obtained in 7.3, but with pulse tube cooler temporarily turned off for #197

9.3 SiMOS ESR Antenna

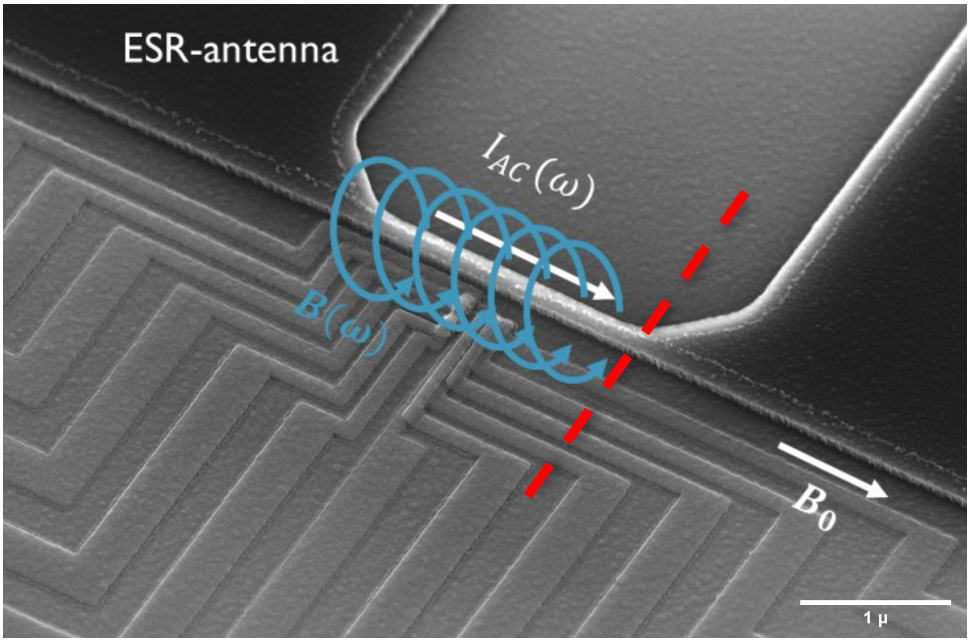

Figure 18: SiMOS SEM image, illustrating how an AC current through the ESR antenna creates an AC magnetic field B(ω) at the qubit location, perpendicular to the static applied field B_0. Image provided by IMEC.