FACULTY OF SCIENCE
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Bachelor's Thesis in Experimental Physics

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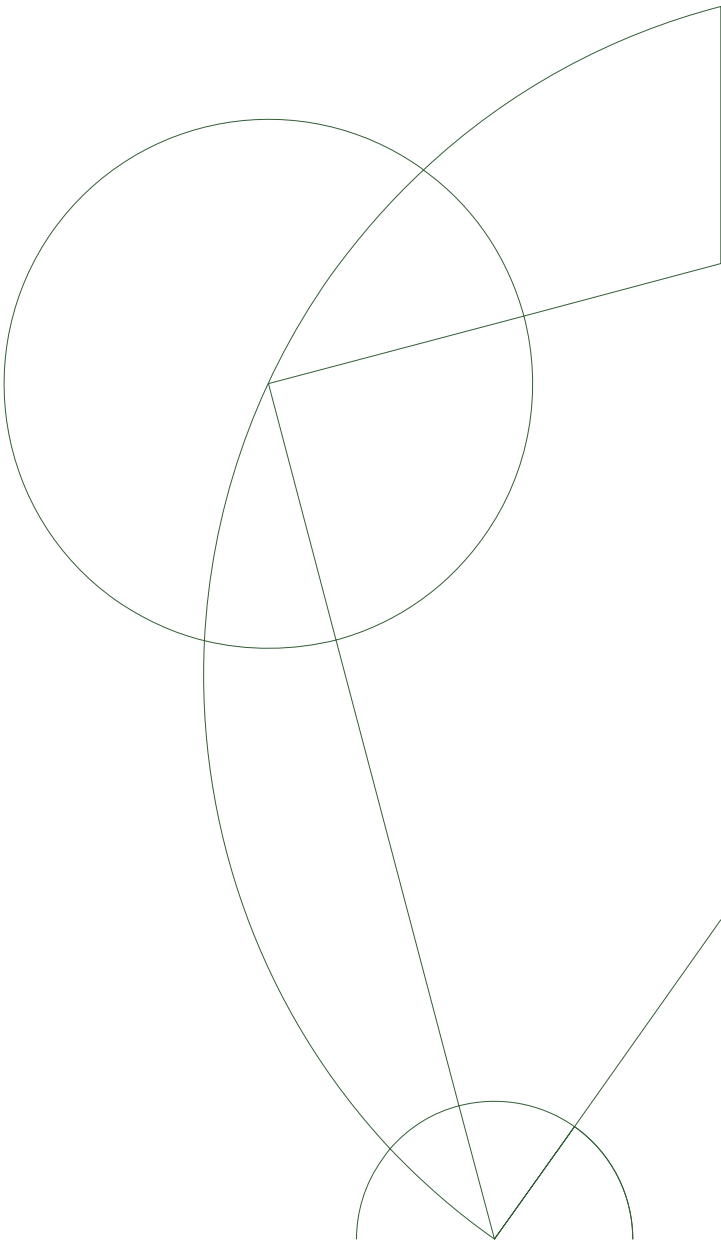
Modular Low-Temperature Load-Locked Sample System for Quantum Devices

Center for Quantum Devices



Supervisor: Ferdinand Kuemmeth

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Abstract

In this thesis I present the limitations and considerations involved in designing a new sample system for low temperature transport physics.
Currently, several systems are used and none of them take full advantage of recent modifications of the dilution refrigerators or new technology. The new system, its functions and features, as well as a comparison to the old systems are presented.
Interconnect solutions inside the puck, transmission lines for RF signals and impedance, as well as residual magnetism inside the puck are described.
It was not possible to have fabricated boards ready before the hand-in of the thesis and as such, future tests to be performed are only mentioned.

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1 Introduction

The purpose of this project was to create new and improved experimental hardware primarily for all teams at the Center for Quantum Devices (QDev) which currently use out-dated ceramic chip carriers with significant limitations. In collaboration with the researchers connected to the Majorana subgroup the new sample setup was discussed, limited and developed to their needs and wishes as best as technology and limitations, which I will get back to later, of the Oxford Instruments dilution fridge setup allows. The idea for the new sample system came from struggles with the existing setup for the spin-qubit group (the Mayo board, see figure 1a) and a technique called an *Interposer board* using Fuzz Buttons[1] used by one of QDev's collaborators, David Reilly [1]. The problem associated with the Mayo board is that the fully assembled boards are expensive, approximately $1000 due to DC and RF connectors. Also, when a sample device has been wire-bonded to the board, removing it again will over time damage the bonding pads by either tearing off the gold or leaving wire bonding material on the bonding pads (see figure 1b). Another problem with having this expensive board setup is that if you have a device which is almost perfectly wire-bonded, but you have other devices to test, then you have to un-bond the device from the board as you cannot just stock up on expensive boards.

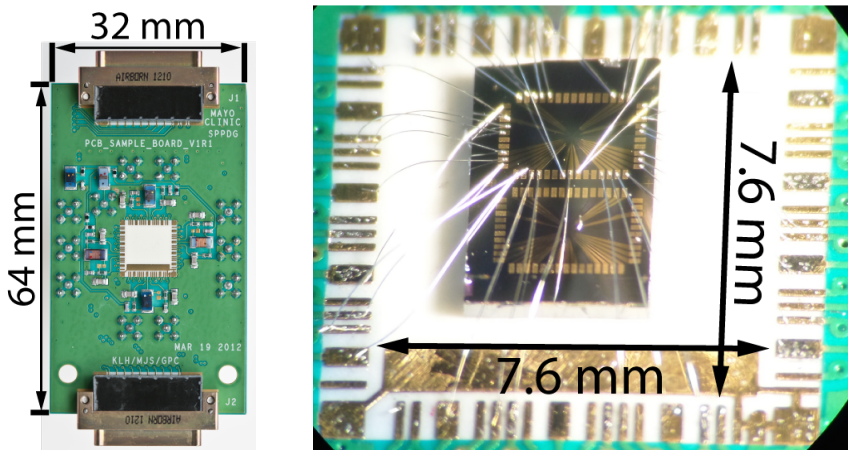
The following sections give a brief introduction to the existing hardware which is currently used in nanowire, 2DEG and spin qubit experiments. I will discuss how the technical limitations of the current sample holders motivates my sample and puck design.

1.1 Current sample holder and chip carrier

Today many subgroups in QDev uses ceramic chip carriers where the sample is glued onto and wire bonded to the gold contacts and then inserted into a spring-loaded socket (see figure 2a). The socket is equipped with copper contacts which connects the bond pads on the ceramic chip carrier with the sample holder and the rest of the setup. The beryllium-copper (BeCu) contacts on the socket are coated with a nickel sticking layer before being gold-plated, but due to nickels magnetic properties we etch away the gold and nickel, thus leaving us with completely non-magnetic BeCu contacts on the sample holder. The problem is now that BeCu oxidize over time which decreases the performance of the sample holders as well as reduce the thermal conductance of the contacts. The gold contacts on the ceramic chip were custom-made without a nickel sticking layer and as such do not suffer from magnetic or oxidization issues.

The ceramic chip carrier also supports up to 32 DC connected lines but the Oxford dilution fridges supports up to 48 DC connected lines, where 24 of the lines go through one set of filtering (also called a loom) and the other 24 go through another, sometimes different, type of filtering as well as 14 coax lines for high-frequency signals. Due to this

[1] Fuzz Buttons are small spring-like electrical connectors made out of wound-up wire. See http://www.custominterconnects.com/fuzzbuttons.html for further details.



(a) (b)

Figure 1: (a) Photo of the Mayo board used in spin-qubit experiments. The PC board itself measures 64 mm × 32 mm, and accomodates chips up to 7.6 mm × 7.6 mm with 48 DC lines, 10 fast gate lines, and one RF readout line (4 SMD coil resonators) [2]. (b) Photo of a wirebonded (the thin wires) GaAs spin qubit sample glued onto the Mayo board. Note the small gray dots all over the bonding pads, resulting form rebonding multiple samples on the same board. Image courtesy of Peter Dahl Nissen and Martin Kufahl, QDev 2014.

filtering of the DC lines the amount of available lines for users using the ceramic chips is reduced to a single loom.

Another thing which is bad with this setup is that you have to put the chip carrier in the opening of the sample holder and then press it together so the chip carrier falls into the hole and the copper contacts sticking out makes contact. This procedure may destroy some of the fragile wire bonds and thus reduces the number of gates you can use on your device

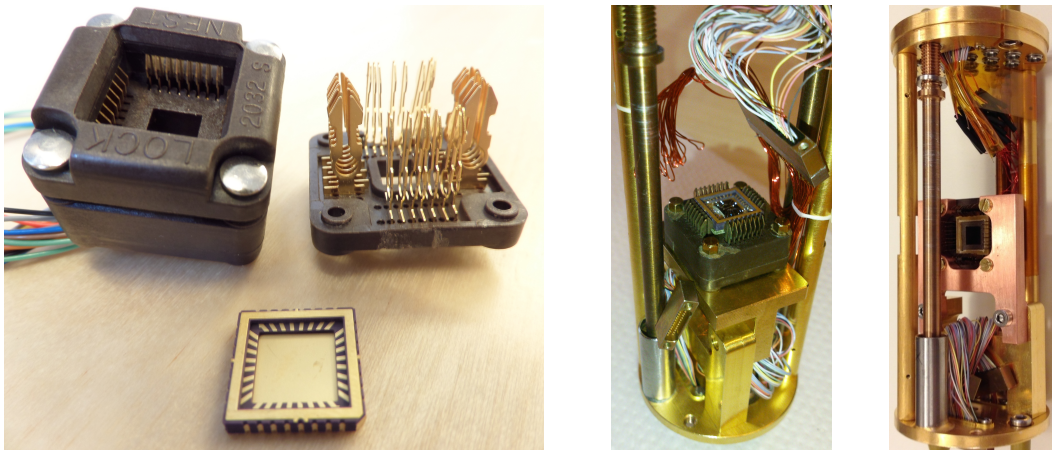
1.2 Technical limitations

The space inside the puck is the primary limiting factor when it comes to using current sample setups as well as developing new setups. The theoretical 'available' space inside the puck is a cylinder with a radius of 20.75 mm and a height of 100 mm.

Inside the puck two 51 pin nano-D connectors are fitted[2], one in each end of the puck. The top (the 'thick' plate in the top of figure 2c) is used to connect the puck with the dilution fridge and thus is mandatory for use. The bottom connector is used by some fridge users while the sample holder is sitting in the puck loading stick (PLS) which is used to load the puck into the fridge (see appendix I for photo). The PLS can then be connected to the breakout box[3] via fischer connectors which allows the user to

[2]See http://www.omnetics.com/products/bilobe-dualrow/ for more info.

[3]The breakout box is where all the cables for the gates are connected. See appendix H for a picture of the breakout box.



(a) **(b)** **(c)**

Figure 2: (a) Photo of the ceramic chip carrier and socket used in current nanowire experiments. Used sample holders have had the top part removed (see e.g. (b)) due to the four rivets being magnetic. (upper left), the spring-loaded mechanism which compresses when you push down on the sample holder to load in your sample (upper right) and the current ceramic chip carriers. Figures (b) and (c) show the current sample holder with a device loaded in two different magnetic field configurations where (b) shows the sample in the perpendicular mounting (image courtesy of Merlin von Soosten, QDev 2014), and (c) shows the sample in the parallel mounting (image courtesy of Willy Chang, QDev 2014).

either apply a bias voltage or ground all the gates while loading. The first method is primarily used by gallium arsenide (GaAs) substrate users because it turns insulating at subkelvin temperatures (i.e. the resistivity of GaAs is much greater than that of the device. Semi-insulating GaAs e.g. has a resistivity ranging from 10^7 - 10^9 Ω [3]). The other method is used by people who have very sensitive devices which might be damaged by uncontrolled electrostatic discharge.

After fitting the driving rods, which are used to screw the puck into the dilution fridge, as well as the new mounting/stabilizing rods, the space is reduced to about 42 mm × 27.4 mm (see figure 3). Since the Majorana subgroup is interested in both perpendicular and parallel mounting of their devices with respect to the strong magnet axis B_z, designing a long and thin board like the Mayo board was not an option (a typical vector magnet has a range of ±6 T in B_z and ±1 T in B_x and B_y).

Another limiting factor in the design process of the boards is the size of the components to be fitted. The surface-mounted device (SMD) 51 pin nano-D connector body is about[4] 22.86 mm × 4.2 mm, and we need to fit two of these on the board, as well as fourteen SMP connectors[5].

[4]See http://omnetics.com/products/bilobe/pdffiles/A28200-051.pdf for technical datasheet on the 51 pin nano-D connector (accessed 29/05/2014).

[5]See http://rosenberger.de/ok/images/documents/db/19S141-40ML5.pdf for technical datasheet on the Rosenberger SMP connector (accessed 14/05/2014).

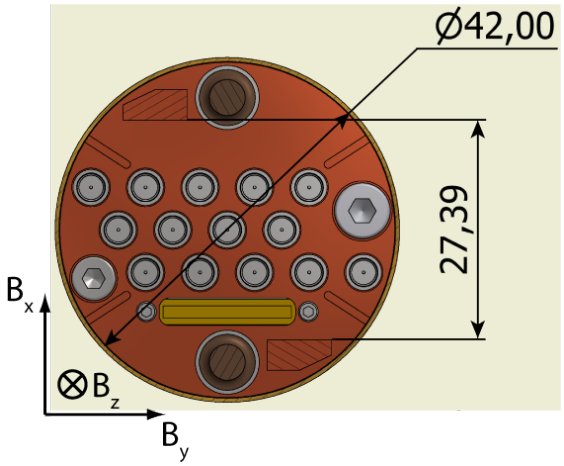


Figure 3: A cross sectional picture of the puck with the new mounting rods fitted. Dimensions are in mm and show the actual usable space inside the puck available for the setup. Magnetic field axis' with respect to the puck when it is load-locked inside the fridge are also shown.

2 Considerations for experimental low-temperature designs

In this section I will cover the considerations which went into this project from an experimental low-temperature physicist's point of view. I will discuss the heat transfer across two interfaces, primarily a solid/solid interface, which affects the choice of materials we use, and the use of twisted pairs.

2.1 Heat conduction across interface

When it comes to transfering heat inside a cryostat many different conduction interfaces are viable. At QDev all of our cooling power through our puck to our sample comes through metal/metal (solid/solid - S/S) pressured interfaces. When dealing with pressured solid/solid interfaces there are different ways to increase the heat flow depending on how much pressure is applied to the interface. For the pucks we rely on high-pressure (> 1 MPa) S/S interfaces so all the necessary components are gold-plated to achieve the highest thermal conduction through the interface and thus the lowest possible sample temperature. For less pressured interfaces either grease or a thin indium film in-between can be used to increase the heat flow [4].

For these pressure S/S interfaces it has been found experimentally that the heat conduction λ of the interface increases linearly with pressure which consequently means that the heat flow $\dot{q}$ through the interface becomes independent of the contact area since $\dot{q}_{\text{pressure s/s}} \propto \lambda A \, \mathrm{d}T/\mathrm{d}x \propto F \, \mathrm{d}T/\mathrm{d}x$ [4]. Due to this direct dependence on force, we fit helicoils[6] in the new mounting hardware in order to increase the heat flow to/from our sample device, by virtue of increasing the force that can be applied via the screws..

[6] A helicoil is a small coil which is inserted into the tapped hole to make the thread stronger and harder to tear. This is especially useful in soft materials like copper, where threads often tear quickly.

2.2 Materials

Different characteristics of the materials make for different uses of them. Besides the thermal conduction, the thermal contraction is the most important property for my puck sample system. The primary materials used in the puck at QDev are copper, bronze[7], and possibly brass (see table 1 for their thermal conduction and contraction coefficients). Different parts of the puck needed different characteristics, e.g. some parts need to contract more than others, while some need to heat conduct more than others etc.

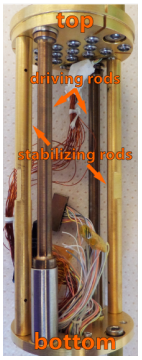


Figure 4: Photo of the inside of a puck with the current stabilizing rods and no sample. Cables are from an old experiment and will be changed when the new sample system arrives.

Some of the materials in table 1 did not have thermal contraction data available at 4 K, but there is a method for estimating the thermal contraction from 293 K to 4 K using

$$\left.\frac{\Delta L}{L}\right|_{4\text{ K}}^{293\text{ K}} (\%) = \alpha_{293\text{ K}} \cdot (185\text{ K} \pm 15\text{ K}) \cdot 100\ , \quad (1)$$

where $\alpha_{293\text{ K}}$ is the thermal contraction of the material at room temperature. I have not been able to find tabulated values for the thermal conductance of bronze at 4 K anywhere, but I believe the reason to use bronze is not because of its thermal conductance either, it is because of its great thermal contraction coefficients as well as because it is self-lubricating in vacuum.

The driving rods (see figure 4) are used to fasten the puck inside the fridge using the PLS. To achieve the best mating between the top of the puck and the mating piece inside the fridge the driving rods must contract more than the top piece to achieve a good heat flow and for this reason they are made of bronze. On the other hand, the top piece of the puck is the conducting pressured solid/solid interface with the fridge and thus gold-plating this piece provides the best heat flow from puck to fridge. Besides acting as stabilizing rods, the new mounting rods will also serve as the thermal connection between the fridge, the PCB-holder, and the sample and as such needs to be made from a material which has a good thermal conductance (see figure 14 for photo of puck fitted with the new hardware). Since this project is not the final, finished redesign of the puck the mounting rods and PCB-holders have been fabricated from electrolytic tough-pitched copper (Cu-ETP) since it has a good thermal conduction without being incredibly expensive. After fabrication, the parts are gold-plated to ensure a good heat flow from device to the fridge.

[7] When Morten L. Jensen (machineshop staff at NBI) examined the driving rods (see figure 4) he concluded they were made of a *standard bronze alloy*.

Material	$\lambda_{4.2\ \mathrm{K}}$ [W/(m · K)]	$\Delta L/L_{293-4\ \mathrm{K}}$ [%]
Cu-ETP (99.9%)	∼ 560	0.31 ± 0.03
OFHC-Cu (99.99%)	∼ 850	0.31 ± 0.03
High-purity Cu (99.999%)	∼ 11300	–
Brass (C36000)	∼ 4.5	0.21 ± 0.02
Bronze (Cu-5wt%Sn)	–	0.33
Bronze (Cu-10wt%Sn)	–	0.38
Bronze (Cu-13.5wt%Sn)	–	0.40

Table 1: The table includes the materials' thermal conductivity at 4.2 K as well as their thermal contraction from 293 K to 4 K.. Thermal conductivity coefficients for all copper types as well as thermal contraction coefficients for all bronze types and brass has been found in [4]. Thermal contraction data for Cu-ETP, OFHC-Cu, and brass can be found in [5, 6, 7] respectively. No data on thermal contraction was available for 5-nines copper.

2.2.1 Ortho-para conversion of H_2

High-conductivity copper is preferred when doing low-temperature experiments as removing the impurities from the copper increases its thermal conductivity dramatically. Removing the O_2 impurities is done by treating the copper with hydrogen, but this treatment comes not without a price because by doing this, small bubbles of molecular H_2 form inside the copper with a diameter of about 100 nm in concentrations of 10 to 100 ppm. Due to the spin of the proton in each hydrogen atom the total nuclear spin of H_2 is either $S = 0$ or $S = 1$. The spin-configuration with $S = 1$ is called *ortho*-H_2, and the spin-configuration with $S = 0$ is called *para*-H_2. In thermal equilibrium at room temperature the ratio of ortho-hydrogen to para-hydrogen is 3:1 due to the nuclear degeneracy, and because the para-state has a lower energy than the ortho-state by 170 K, a shift towards >99.9 % para-hydrogen will occur as temperature is lowered to base temperature around 10 mK. However, this conversion, which does not conserve the total nuclear spin, is very slow, about 1.8% *per hour* [8, 9], and compared to the cooldown time of the puck from room temperature to base which is about 6 hours, the heat from this nuclear spin conversion will be radiating inside the fridge for days.

These H_2 heat bubbles can be removed by annealing the copper [4], but this procedure might make the copper soft which may very well decrease our heat flow as the amount of force we can apply decreases, even though the thermal conductivity of the material increases.

2.3 Twisted pairs

Since all DC signals in the fridge setups at QDev are transmitted from the breakout box into the puck through a sequence of electrical filters and twisted pairs, a brief discussion of what the ideal use of a twisted pair is as well as how and why we often deviate from this ideal use is in order.

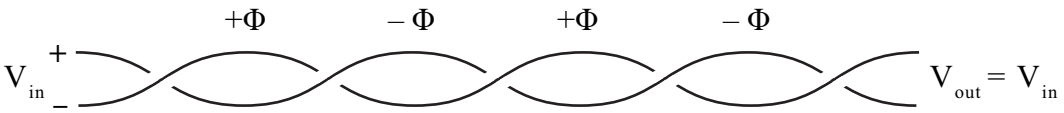
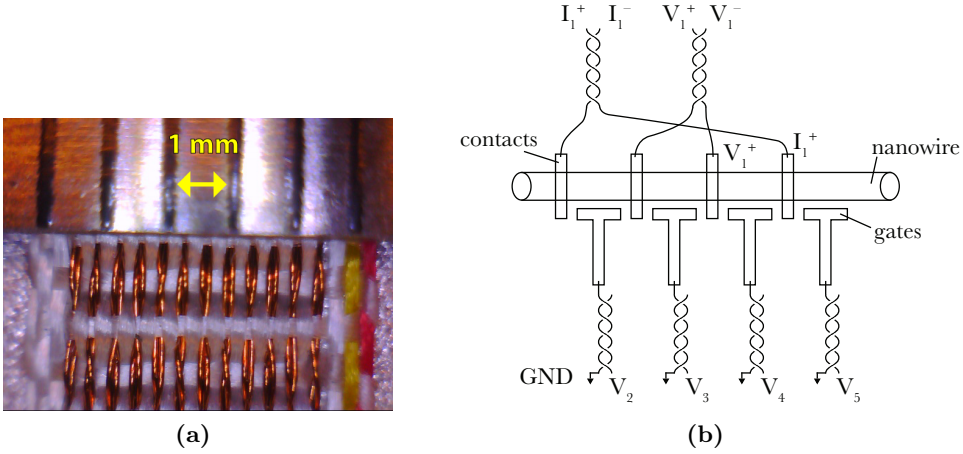


Figure 5: A sketch of the ideal use of a twisted pair. If you apply a magnetic field through the twisted pairs (i.e. perpendicular to the screen/paper) then, because of the braiding of the wires and the fact that each loop area is small, each loop will create an opposite flux opposite the previous loop and in total it will cancel out all together. The voltage difference between two twisted pairs is thus robust against magnetic noise.

A twisted pair is a type of wire which consists of two wires that are braided closely together. 12 of these pairs are then put together into a compact ribbon which is then used in an experimental setup (see figure 6a). The reason for this braiding is to eliminate magnetic induced noise generated in the wire-loops when exposed to a magnetic field. (see figure 5). An experiment which could realise this ideal use of the twisted pairs would e.g. be a four-point measurement of the resistance of a nanowire (see figure 6b). However, in normal experiments it is very hard to realise this ideal use of the twisted pairs as the devices often either has too many gates which needs to be operated (see e.g. figure 1a) or the twisted pair bond pads are also the two neighbouring pads on the chip carrier (see figure 11a for pin layout of the ceramic chips). What can be done instead is to use the twisted pairs as a "poor man's coax cable", i.e. the twisted partner is grounded and becomes the shield (see figure 6b). Grounding the twisted partner ensures that most of the electrical fields from the signal wire will terminate on the grounded partner thus preventing electrical signal coupling between twisted pairs and coupling to electrical noise in the environment. The twisted pairs are currently being used for measurements running at frequecies ranging from[8] DC and up to ~ 7 kHz even though they are useful up to ~ 1 MHz [10]. The reason is that the twisted pairs are filtered through two low-pass filters in series, typically with a 2 kΩ resistor and a 2.7 nF capacitor in QDev's fridges.

When choosing a frequency to perform AC/lock-in measurements a few key frequencies should be avoided. The electrical signal noise from the power supply, which in Europe is at 50 Hz, and also its higher harmonics, i.e. 100 Hz, 150 Hz etc., should be avoided. The noise from the turbo pump above the fridge should also be avoided, which operates at 820 Hz or 1000 Hz. Typical frequencies used in the lab are 8 Hz and 17 Hz, both used by the Fractional Quantum Hall Effect (FQHE) team, and 177 Hz which is used by the Majorana team.

[8] At ~ 7 kHz we have a -3 dB cutoff in gain through the RC filter. Cutoff frequency is calculated using a script made by the Fractional Quantum Hall Effect team [2].



(a) **(b)**

Figure 6: (a) Photo of Oxford Instruments loom with 12 twisted pairs. The ribbon is about 6 mm wide. (b) Two different ways of using twisted pairs on a hypothetical sample. Current bias I_1 is applied via a twisted pair, and the resulting voltage drop V_1 measured via another twisted pair, without suffering from magnetically induced noise. Gate voltages V_2, V_3, V_4, and V_5 are applied via four different twisted pairs. By grounding one wire of each twisted pair at the breakout box, it acts as a shield and reduces coupling of electric noise to gate voltages V_2, V_3, V_4, and V_5, thereby the twisted pairs function as a "poor-man's coax cable".

3 Modular high-density, high-frequency sample holder

In this section I will explain the purpose of the three printed circuit boards, the thoughts behind each design as well as the new sample holder and hardware for the current sample pucks. I will discuss interconnect solutions currently used as well as transmission line structures for RF signals, and what the future might hold. Lastly I will discuss the importance of the use of nonmagnetic materials.

3.1 Printed circuit boards

A printed circuit board (PCB) consists of 1 or more dielectric layers each with up to two copper layers, one on each side of the dielectric material. A dielectric with two layers of copper is referred to as a two-layer board. These two layers could be connected through the dielectric by a via (a plated, electrical conducting hole). Having more than two layers allows the user to create more complex boards and only increase the thickness of the board. As mentioned in the introduction the spin-qubit subgroup uses single board (with 10 layers) on which the chip area is damaged over time. This project is using the technology of interposer boards to split this into two different boards (see figure 7) where the interposer serves as a connector-free electrical connection between the two via fuzz buttons.

Parallel with the designing of these boards the FQHE subgroup (or 5/2 subgroup) has also been working on new boards for their team. Midway through this project it

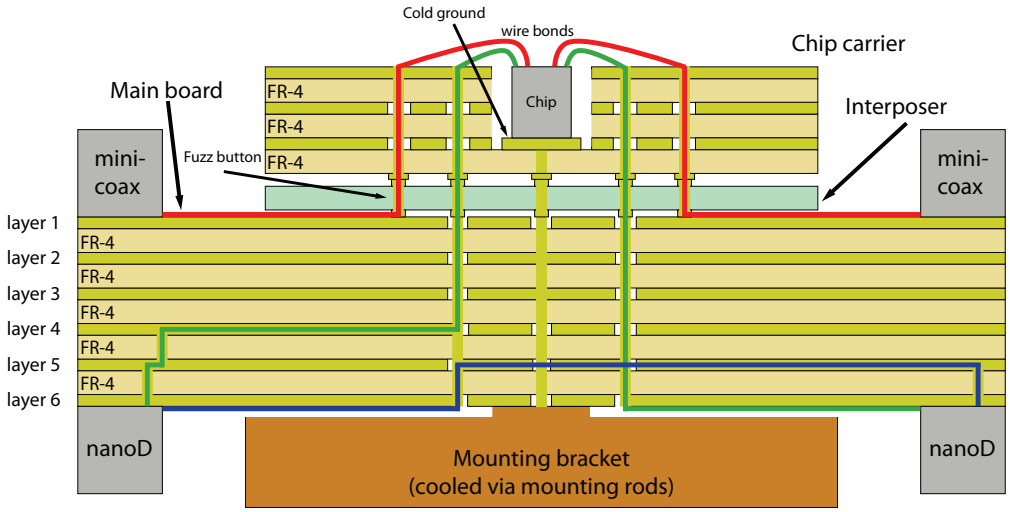
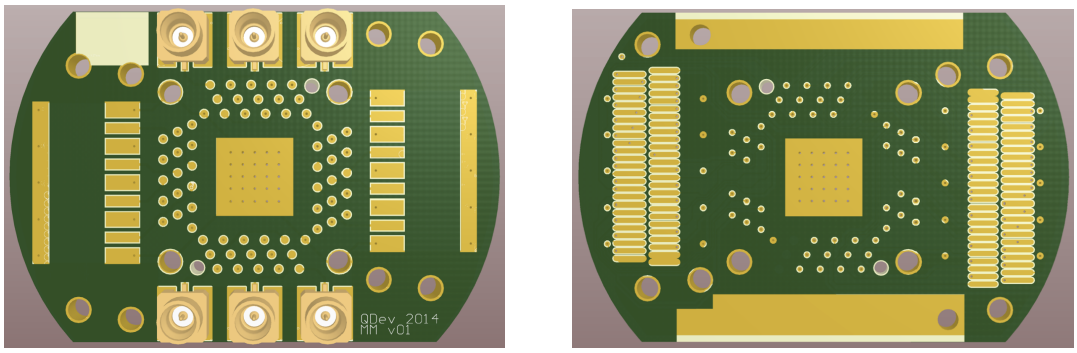


Figure 7: Cross-sectional sketch of the board stack not drawn to scale. In reference to figure 8 the cross-section is taken through the center from right to left and features the chip carrier with a cold ground (see figure 25 in appendix J). **Chip carrier:** Consists of four signal layers and three dielectric layers. Top layer is used to connect vias with bonding pads and the bottom layer is used to mate with the interposer. **Interposer:** Features the fuzz buttons which carries the signal from the main board to the chip carrier. **Main board:** The main board features all the connectors to the puck and consists of six signal layers and five dielectric layers. **Top layer (layer 1):** Six mini-SMP as well as two 4-channel mini-coax connectors are located as well as routed to the pads on the top layer (red). **Layer 2 and 3:** Both layers are connected to ground and acts as a shield between the DC and RF connections. **Layer 4, 5 and 6 (bottom layer):** Two 51 pin nano-D connectors are soldered to the bottom layer. These three layers are all used to connect the two nano-D connectors to each other (blue) as well as with the vias (green) connecting them with the chip carrier. For detailed layer drawings of main board and chip carrier see appendix **??** and **??**, respectively.

was decided to fuse the two PCB projects together in order to increase the compatibility of setups available at QDev. At first we wanted to make everything interchangeable between the two projects but in the end decided to make two different main boards as well as two different mounting brackets, but keeping the chip carriers and interposer universal.

All boards (except for the interposer which is fabricated from Ultem 1000) have been manufactured from standard FR-4 material as this is more durable to bending than e.g. Rogers 4350B (i.e. the flexural strength of FR-4 is higher than for RO4350B), which on the other hand is better for RF circuits. We went with FR-4 instead of RO4350B because it is the cheaper solution and the primary use of the boards is not going to be for RF measurements, but we want to offer people the possibility of doing it. The boards are also mounted to the mounting bracket using stainless steel M1.6 socket head cap screws.



(a) **(b)**

Figure 8: (a) and (b) shows the top- and bottom view, respectively, of the main board generated in Altium. The three connectors in top and bottom of (a) are the six mini-SMP connectors, and the plated areas to the right and left of the board replicate the footprint as seen in the technical datasheet for the mini-coax connector. In (b) the solderpads for the two nano-D connectors can be seen, as well as exposed copper for better thermal conduction between main board and mounting bracket. 64 round landing pads for fuzz buttons are visible, out of which 48 carry DC signals, 14 carry high-frequency signals, and the 25 vias in the center square carry cold ground.

3.1.1 Main board

The main board (see figure 8) is the board which carries all the connectors to the puck and all of the electrical connections in the setup. It consists of five dielectric layers and six signal layers where the top layer is used for RF connections and the three bottom layers are used for routing the two nano-D connectors with the Fuzz Button connections as well as each other.

One of the biggest difficulties in designing this board was actually to be able to fit two nano-D connectors, keep 14 RF connections and still be able to mount both perpendicular and parallel to the field. If you e.g. look at figure 8 then the two outermost holes on each side of the board is used to screw the nano-D connector onto the board.

3.1.2 Interposer

The main purpose of the interposer is the ability to make modular board structures for increased flexibility in the sample system. It is fitted with 64 Fuzz Buttons which carry the signal of the 48 DC lines and the 14 RF lines from the chip carrier to the main board. Two of the Fuzz Button connections on the main board are grounded, but have been kept due to the introduction of the chip carrier rotation scheme (see section 3.1.3). Another 25 Fuzz Buttons are fitted in the middle of the board to carry cooling power from the main board (which carries the cooling power from the underlying copper mounting bracket through the vias) to the chip carrier.

The interposer is also fitted with two alignment pins to allow for easy mounting of chip carrier and interposer to the main board.

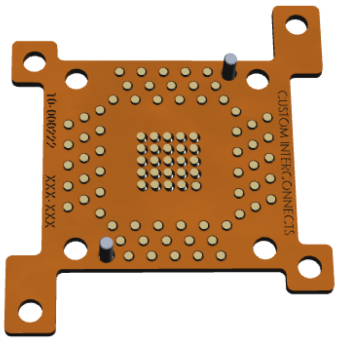


Figure 9: Model view of the interposer. The four outer holes are used to mount the interposer (oriented as shown) onto the main board, and the four inner holes are used to mount the chip carrier onto the main board and interposer stack. The two gray pins are the alignment pins used to ensure succesful mating of the stack. Photo is provided by Custom Interconnects.

3.1.3 Chip carrier

The chip carrier is practically just an inexpensive, removable chip area. There were several reasons behind this, where a few of them have already been mentioned, but another reason is the gained flexibility in the design of the chip carrier. One of the designs can be seen in figure 10 and the two other flavours currently designed can be seen in appendix J. Other designs of the chip carriers could include stuff like differently placed/sized/shaped bonding pads, bigger/smaller chip area, deeper/less deep cutout for the sample to sit in, more/less cooling power vias etc.

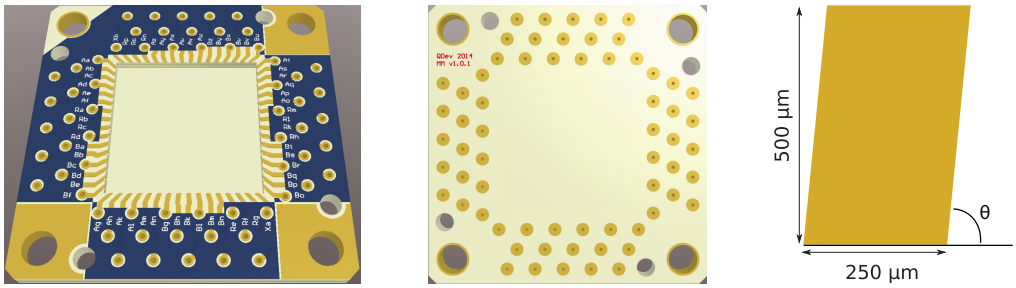
Bonding pads

The bonding pads have each been rotated $n\pi/32$ radians, where n counts the corresponding bonding pad from the center, i.e. the first is rotated $\pi/32$ radians, the next $\pi/16$ radians etc (see figure 10c). This ensures that the corner pads have been rotated $\pi/4$ radians, thus making the two corner pads parallel. This was done to make for a better wire-bonding 'environment'. Imagine you needed to wire-bond to the first eight bonding pads in the corner (i.e. four horizontal, four vertical). If the bonding pads were not rotated like this, residual wire-bond material might short two neighbouring bonding pads.

Each bonding pad is 250 μm wide at the base and 500 μm long, independent of their rotation. The space between each bonding pad is also 250 μm at the edge of the cutout. This further prevents shorting two pads together unintentionally.

Even/odd routing of bonding pads

As mentioned in sec. 2.3, being able to use the twisted pairs as "poor man's coax cables" and maintaining a high line count (cf. discussion of figure 6b) a redesign of the pin layout was needed. I have tried to address this issue with the new boards by splitting up the twisted pairs across the chip layout, and so instead of having the twisted wires



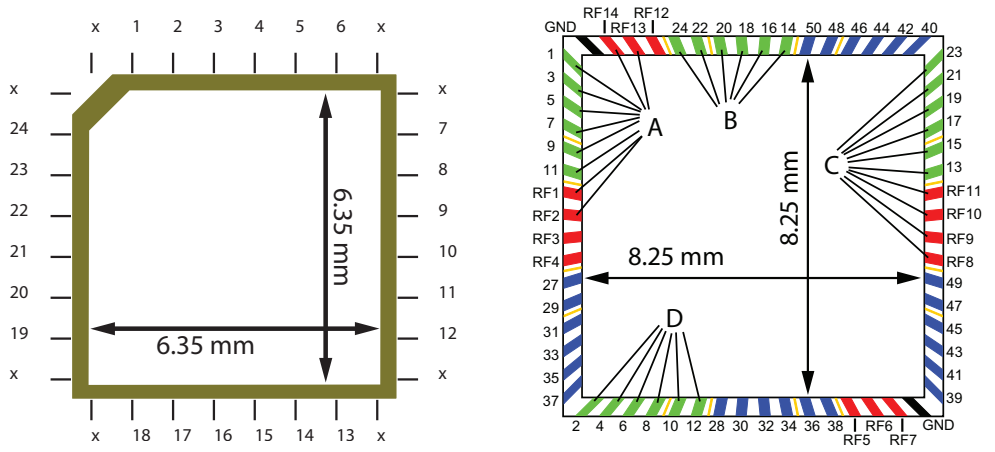
(a) (b) (c)

Figure 10: Model view of one of the three versions of the chip carrier genereated using Altium. (a) Shows the top view of the chip carrier **without** a plated region designed for RF measurements. The four big holes in the corners are used to mount the chip carrier with the interposer and main board, and the four smaller holes next to them are for the alignment pins in the interposer. The plated corners provide the users of the RF version with the ability to wire-bond to a cold ground as well as help cool the boards, instead of using the filtered grounds via the bonding pads, and the upper-left corner is used to show the user what is considered the 0-degree mounting (see section about the rotation scheme for elaboration). (b) Shows the bottom view of the chip carrier. 64 round landing pads are visible and solder mask (blue layer in (a)) has been removed to ensure better mating conditions for the fuzz buttons. (c) shows a close-up of a bonding pad indicating the angle of rotation mentioned in the section. As the bonding pad is located farther away from the corner of the cutout, the bigger the bending angle θ.

next to each other as on the old chips, the first 6 odd numbers (wires) are collected (i.e. line 1 to 11), then somewhere else around the chip area the first 6 even numbers (wires) are located (see figure 11b for complete pin layout of the new chip carrier). Another reason to spread out the twisted pairs was also of fear for crosstalk between two twisted wires when used on different gates (consider e.g. a device where line 1 and 2 (i.e. a twisted pair) were wire bonded to two different input gates on the same device to be used simultaneously).

PCB cutout

The PCB cutout has been made to make the wire bonding process easier. When wire-bonding you have to control the needle with two knobs, where the first knob moves the needle in the plane and the second knob moves it up or down perpendicular to the plane. By plane I mean the top surface of the sample. On the Mayo board, but not the ceramic chip carriers, wire-bonding requires you to wire-bond from the bonding pad and **up** to the pad on the device. This means you have to guess how thick your sample is and raise the needle accordingly. However, if the top surface of the sample sits below the bonding pads, you can just touch the bonding pad, locate the needle over the sample pad and then move it down. In the current version of the chip carriers, this cutout is 450 μm deep. The width of the chip area, i.e. the width of the cutout, is 8.25 mm $\times$ 8.25 mm, i.e. larger than both Mayo board and ceramic chip carriers. An increase beyond that would be difficult due to the many connectors which had to be fitted on the main board.



(a) (b)

Figure 11: (a) A figure of the pin layout of the ceramic chip carriers. Notice how twisted pairs (i.e. line 1-2, 3-4, ...) are located next to each other, complicating the efficient use of twisted pairs under certain circumstances. Image courtesy of Henri Souminen, QDev 2014. (b) Example of efficient use of twisted pairs while maintaining high line count. Shown here for four independent devices on a chip wire bonded to loom 1 (green) and a few fast gates (red). While device A is measured, other devices are grounded at the breakout box, thereby turning line 2 (4, 6, ...) into a grounded shield for line 1 (3, 5, ...), cf. figure 6b. Note that the two grounded bonding pads are grounded inside the fridge, i.e. are cold ground pads.

Another upper bound on the size of the area was the fuzz buttons and the sizes of the landing pads on both bottom of the chip carriers and the top of the main board. Had the space between the fuzz buttons been decreased, routing of the fast gates on the top layer of the main board would not be possible.

Ground, cold ground, and backgate

A wide variety of experiments are being conducted in QDev and as such we decided to design three different flavours of the chip carrier to make the new sample system useful for as many users as possible. Some people want to do RF measurements, some people want very cold electrons and some people want to use the backgate to tune their substrate. In this section I will explain what a cold ground is, how it differs from a normal ground and what a backgate is used for.

A *global* backgate is a plated electrical conducting area which you glue your sample onto. Now consider the device construction in figure 12a. A thick, highly (degenerately) doped silicon substrate with a thin silicon oxide layer is glued onto the copper backgate and a nanowire (NW) is deposited onto the SiO_2. The NW is then connected to source and drain, and the backgate is wire-bonded to a bonding pad. This highly doped silicon will act as a metal at low temperatures, thus applying a positive bias to the backgate will accumulate positive charges at the top of the silicon, underneath the insulating SiO_2. This accumulation of positive charges in the substrate will lead to accumulation

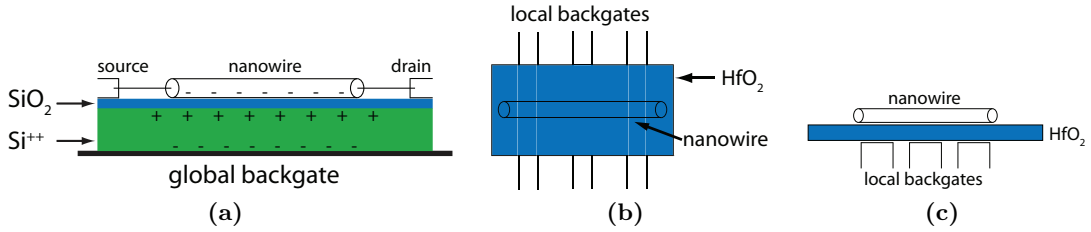


Figure 12: (a) Illustration of a device which benefits from a global backgate to make a field-effect transistor with the substrate and the nanowire. Source and drain simply means a connection to the lab equipment. (b) and (c) illustrates a device which incorporates the use of local finger backgates to locally tune the electron density in the nanowire. Instead of using the oxide layer on the substrate an insulating layer of hafnium-oxide has been deposited on top of the gates, and then the nanowire is put on top of this.

of negative charges at the bottom of the NW, and the more bias voltage that is applied to the backgate, the more charges accumulate and at some finite voltage electrons start flowing through the NW. Thus a global backgate can be used for example to create field-effect transistors.

Another version of the backgate is a *local* backgate which is seen in figure 12b and 12c. Here the gates are deposited on the substrate, then a layer of insulating material, in this case hafnium oxide, and then our nanowire. This allows the user to locally tune the electron density in the nanowire. A combination of local and global backgate can also be used, but depending on the density of local gates on the device, the global backgate might be screened from the NW and thus has no effect.

A cold ground is a ground wired directly to the puck/fridge setup and so both electron and phonon temperatures of the ground is the same as for the fridge. A normal ground on the other hand is a connection which is grounded outside the fridge on the breakout box and as such does not have the same electron and phonon properties as the cold ground. However, if the thermalization and filtering of the wires in the mixing chamber plate inside the fridge are good, then we can regard the normal ground as a cold ground. Both grounds are available on all three versions, but for the backgate and RF version you have to wirebond to either the grounded bonding pads or the exposed plated corners of the chip carrier.

Rotation scheme

As mentioned earlier, one of the things we want to move away from with this project is the need to un-bond a device chip if you want to try a new one, or if you want to test the same device with a different line configuration (fast vs. slow signal lines, loom 1 filtering vs. loom 2 filtering). As mentioned in the introduction, the puck offers 48 DC lines, with half going through one type of filtering and the other half through another. Doing an experiment and having your device chip in one type of filtering might not show significant data that you can use, but doing the same experiment through the other

filtering might give you the significant data you want to see. That is why a rotational scheme was build into the sample system.

When you load the chip carrier 180° in respect to the default orientation, bonding pads associated with loom 1 and 2 will interchange. This enables the user to test their sample through both filterings without having to re-bond the sample. We also wanted to be able to interchange loom 1 and the RF lines as well as loom 2 and the RF lines, but due to there being less RF lines than DC lines, a perfect mapping cannot be achieved. In the current design, if you rotate the chip carrier 90°, eight loom 1 and loom 2 lines are interchanged with RF lines, eight loom 1 lines are interchanged with loom 2 and vice versa, and eight of both loom 1 and loom 2 stay the same, but exit a new BNC cable # on the breakout box at the fridge station (see appendix **??** for table with how all lines change under all four rotations).

3.2 Interconnects inside puck

The 42 mm Oxford puck comes readily equipped with two 51 pin nano-D connectors (see appendix **??** for pin layout of nano-D connector) and 14 SMP connectors which allows for 48 DC signals and 14 RF frequency signals to be used on a single device. In this section I will go over which connectors we have ordered for both soldering to the boards and for connecting the boards with the puck itself.

3.2.1 DC connectors

The main board is fitted with two 51 pin nano-D SMD connectors which provide the sample with 48 DC signals and can be purchased through different vendors like Glenair, Omnetics, and Airborn. SMD connectors to be used for these boards come from Omnetics and have partnumber MNPO-51-VV-T-ETH, which is a male pin connector mounted vertically on the board with an unplated titanium shell and is equipped with end threaded holes. The cable connectors ordered for this project comes from Glenair and have partnumber 891-005-51GST-2B7-4TT which is a 4 inch, #32 wire gauge, unplated titanium shell back-to-back cable connector. The cable connectors interface with those provided by Oxford Instruments at the top and bottom of the puck.

3.2.2 RF connectors

Due to space issues on the main board the RF signals are transmitted through a mix of SMP, MSMP and mini-coax connectors. The SMP bullets are fitted to the puck itself, but due to the sheer size of these connectors the main board is fitted with MSMP and mini-coax connectors, with part # 18S141-40ML5 and 23C11E-40ML5, respectively. The first two types of connectors are available through vendors like Rosenberger, but the last is only available through Rosenberger. To make assembling and disassembling the semi-rigid SMP cables from the boards easy the MSMP SMD connectors are smooth bore connectors and flexible RTK-047 cables are used for connecting the mini-coax connector with the SMP bullets in the puck.

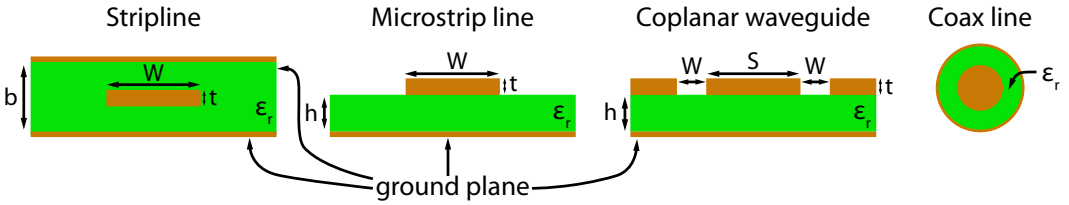


Figure 13: A sketch of four different line structures for RF signals. **Stripline** has very good signal characteristics, but because it is placed in between two dielectric materials it is not easily integrated into a component circuit. **Microstrip** line is fabricated on the top of the dielectric and as such is very easily integrated into a component circuit. **Coplanar waveguide** has, unlike both microstrip and stripline, its ground planes on the same side of the substrate as the signal trace which makes it the most easy connector to integrate in a component circuit. This also means that the CPW structure requires a lot more space than the two others.

Unlike for DC signals, having a good transmission line structure on the PCB for RF signals is very important. The geometry of the transmission line structure determines the impedance of the line and thus how much (or how little) of the signal is reflected, as well as the delay of the signal. In figure 13 four different line structure cross-sections are shown, and for this project we primarily considered the microstrip and the coplanar waveguide structures. Since the coplanar waveguide consists of both a trace width, two gaps and a ground plane it takes up more space than the microstrip structure. This ultimately lead us to choosing the microstrip structure for RF signal transmission on the PCB's. For design equations to determine the characteristic impedance and signal losses in microstrip line, see appendix F and G.

3.2.3 Flex printed circuit

The primary space consumption comes from the wish to support as many connections as the puck offers which also means we have to fit a lot of connectors on the board. At the beginning of the project our intention was to move away from the nano-D cable assemblies and individual SMP coax links, and replace them by compact, flexible circuit boards (FPC's). This would allow for better use of the available space on the boards instead of "wasting" it on connectors and thus making it possible to e.g spread out the landing pads to make room for CPW structures, bias-tees, tank-circuits or a bigger chip area on the chip carrier.

A two-layer FPC can be fabricated with a thickness of down to ~ 50 μm. With a bending radius of about ten times the FPC thickness this would be a whole new way of doing PCB setups in QDev. The FPC would simply exit on the side of the main board and bend up or down towards the puck connectors without wasting any space on the two outer layers. The appropriate connectors would be placed at the end of the FPC's and only require space near the top and bottom of the puck. I have designed a prototype flexboard with four coplanar waveguides of length 20 cm that would allow us to characterize flexboards in regards to low-temperature compatibility, 50 Ω matching, bandwidth, losses and crosstalk between neighbouring channels. For

details see appendix K. Due to the high cost of these prototype FPC's (starting from $4000 USD for 6 boards) and the need to redesign the mounting slot on the Oxford Instruments' sample puck we have not yet pursued FPC interconnects further.

3.3 Sample mounting

The stabilizing rods in the pucks provided by Oxford Instruments are round and cannot be used for mounting of sample holders nor was that the intention when they were designed. In order to increase the effective utilizing of available space inside the puck this project set out to come up with a new design which extended the use of the stabilizing rods to also be mountable. The current sample mount for the Mayo board (the gold bracket seen mounted to the bottom in figure 2b and 2c) which has been extended to support the Majorana team (the copper extension seen in figure 2c) is being mounted to the bottom of the puck which means all the cooling power has to go through multiple metal-metal interfaces to the bottom of the puck and up the mounting bracket before it cools the sample. Using the new mounting system seen in figure 14, we move away from mounting to the bottom of the puck and instead we mount to the stabilizing rods. This not only allows for a more efficient use of space, but the improved surface-to-surface conditions between the cold stabilizing rods and the sample mount may also allow for more cooling power to be transfered. All of the threaded holes in the mounting bracket and the parallel mount arm are fitted with stainless steel (SS) helicoils.

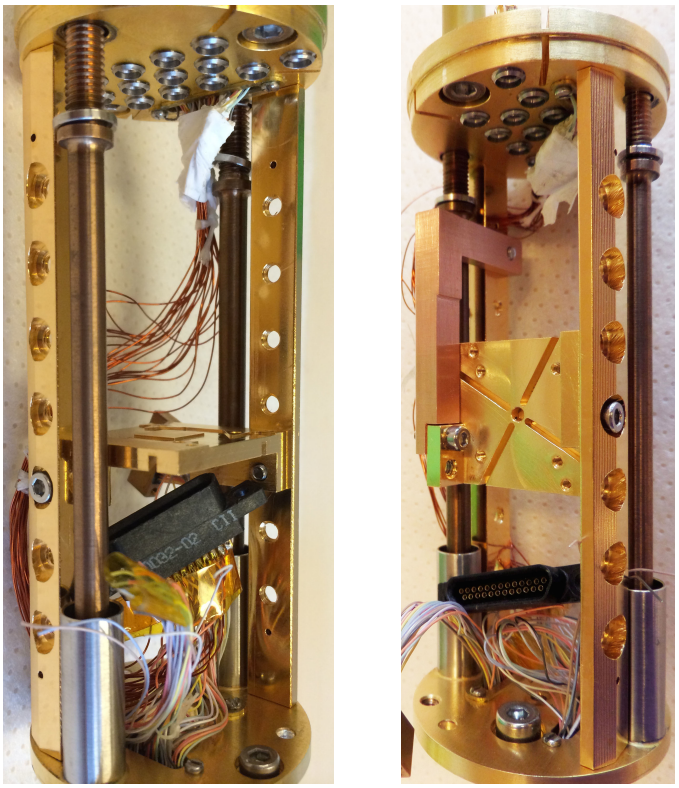
The main body of the bracket measures 27.4 mm × 23.8 mm × 3 mm. Since our mounting bracket is made of copper, sweeping a magnetic field will create eddy currents which leads to heating of the sample. To minimize this heating effect, 2.5 mm deep slits have been machined in the bottom side of the bracket (see figure 14b). To avoid the copper bracket from bending during manufacturing the slits are not connected, and instead a 2.5 mm deep hole has been drilled in the center. The indented valley on the top side of the bracket is made such that when the main board is mounted, throughhole vias do not short on the bracket.

The new stabilizing rods and the mounting bracket are shown in more detail in appendix L.

3.3.1 Residual magnetism

When designing equipment for low-temperature high-field measurements it is important to avoid magnetic materials as much as possible. At every step of the design process we have made sure to avoid magnetic materials where we had the choice, e.g. by skipping the nickel sticking layer under the PCB gold finish,but some of the components may be weakly magnetic such as stainless steel mounting screws and helicoils, and small amounts of nickel in RF connectors, fuzz buttons etc.

During weak antilocalization (WAL) measurements performed in QDev using the ceramic chip carriers and sockets, a typical magnetic offset has been observed in the B_z direction of the order 0.2 mT. We expect that these offsets originate from flux trapping in the superconducting coils of the vector magnet or unavoidable stray magnetic fields in



(a) **(b)**

Figure 14: (a) Photo of the new mounting rods and mounting bracket mounted in the perpendicular magnetic field orientation. (b) Photo of the new sample system mounted in the parallel magnetic field orientation using the parallel-mounting arm. micro-D cable assembly will be replaced by nano-D.

the cryostat/lab environment, and that they will be comparable using the new sample system. An important quantity to verify will be the electron temperature while sweeping the vector magnet through zero magnetic field, as such a measurement can be sensitive to residual magnetism (also see outlook).

4 Conclusion and outlook

A new, modular sample system has been developed which enables the users of the ceramic chip carriers to now use all 48 DC lines and all 14 high-frequency lines inside the fridge without being limited to only mounting their devices in one magnetic field direction. It also allows the user to create bigger chips as well as provide them with a much better wire-bonding environment. It enables the user to interchange the filtering on the gates by rotating and remounting the chip carrier on the interposer without the unnecessary step of having to re-bond the whole device chip. Splitting the boards into an expensive connector board, i.e. the main board, and a cheap and disposable chip carrier also provides the user with the ability to save old devices still wire-bonded to the chip carrier while testing new devices.

Besides providing a better mounting environment, the upgraded stabilizing rods also provides fridge users with the ability to mount things like thermometers or heaters to the spare threaded holes.

To my regret, the boards will not be finished before the hand-in of this project and as a consequence it has not been possible to test the boards inside a fridge and see how well they perform. Future tests of the boards I would like to conduct is first of all to see them fitted inside the puck with all the connectors connected and the radiation shield put on in both mounting positions. Next test would be to see if all 48 DC lines and 14 RF lines work as intended as well as to see how much attentuation we have on the RF signals as the frequency increases. Testing the magnitude of magnetic field offsets using the new boards in e.g. WAL experiments is also something which would be fun to look at. Equally important, as a basic acceptance test, will be to measure the electron temperature (for example using Coulomb blockade peaks of a quantum dot) at high field, low field, and while sweeping the magnetic field through zero.

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Appendices

Appendix A List of design file names

In this section a table with all the design file names of used components for the project as well as a download directory is provided to the reader.

Inventor files

Name	Design file name (.ipt)
Mounting bracket	QDPS 01.00.01a
Parallel B-field arm	QDPS 01.00.03
Stabilizing rod	QDPS 01.00.04

Altium Designer files

Name	Design file name (.PcbDoc)
Main board	QDPS 01.00.01a
Interposer	Designed externally. See appendix **??** for concept drawing with annotated dimensions.
Chip carrier, RF	QDPS 01.00.04
Chip carrier, backgate	
Chip carrier, cold ground	

Appendix B Chip carrier pin layout

In this appendix a zoom-in of the bonding pads and their labels is shown together with a sketch of the nano-D connector fitted to the puck and its pinout. The two tables converts the bonding pad labels on the board to nano-D pins when mounted in 0° (default) orientation. The column "BB #" is meant for fridge users whose breakout box numbers does not match the nano-D pinout. For all rotations see table 4.

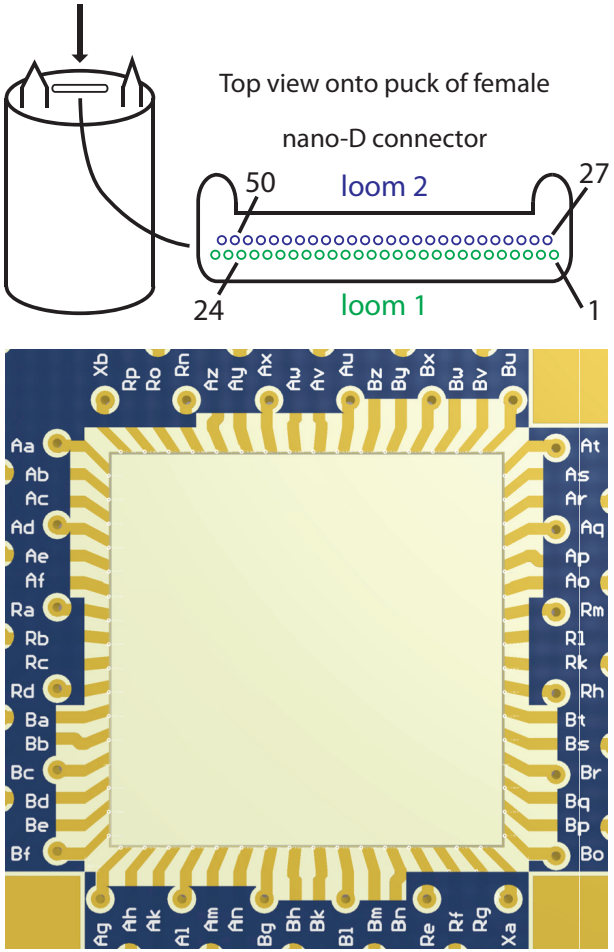


Figure 15: Figure showing sketch of the nano-D connector fitted to the top of the puck with pin numbers indicated. Also shows model top view of bonding pads and chip area with readable bonding pad labels.

Label	nano-D	BB #
Aa	1	
Ab	3	
Ac	5	
Ad	7	
Ae	9	
Af	11	
Ag	2	
Ah	4	
Ak	6	
Al	8	
Am	10	
An	12	
Ao	13	
Ap	15	
Aq	17	
Ar	19	
As	21	
At	23	
Au	14	
Av	16	
Aw	18	
Ax	20	
Ay	22	
Az	24	

Table 2: Table used to convert the bonding pad labels starting with A on the board to the pinout of the nano-D connector.

Label	nano-D	BB #
Ba	27	
Bb	29	
Bc	31	
Bd	33	
Be	35	
Bf	37	
Bg	28	
Bh	30	
Bk	32	
Bl	34	
Bm	36	
Bn	38	
Bo	39	
Bp	41	
Bq	43	
Br	45	
Bs	47	
Bt	49	
Bu	40	
Bv	42	
Bw	44	
Bx	46	
By	48	
Bz	50	

Table 3: Table used to convert the bonding pad labels starting with B on the board to the pinout of the nano-D connector.

Appendix C Chart of pin layout for all four rotations

The following two charts converts the labels for the bonding pads to the pin layout shown in figure 11b. The DC line numbers correspond to the respective number on the nano-D pinout on the top of the puck (shown below), and the RF numbers correspond to a given connector on the main board (see figure 17). Note that two pads are permanently grounded inside the fridge. The column "BNC #" is meant for fridge users whose breakout box numbers does not match the nano-D pinout. **NB:** All rotations are counterclockwise.

Label	BB #	0°	90°	180°	270°
Aa		1	2	39	40
Ab		3	4	41	42
Ac		5	6	43	44
Ad		7	8	45	46
Ae		9	10	47	48
Af		11	12	49	50
Ag		2	39	40	1
Ah		4	41	42	3
Ak		6	43	44	5
Al		8	45	46	7
Am		10	47	48	9
An		12	49	50	11
Ao		13	22	27	36
Ap		15	24	29	38
Aq		17	RF12	31	RF5
Ar		19	RF13	33	RF6
As		21	RF14	35	RF7
At		23	GND	37	GND
Au		14	RF1	28	RF8
Av		16	RF2	30	RF9
Aw		18	RF3	32	RF10
Ax		20	RF4	34	RF11
Ay		22	27	36	13
Az		24	29	38	15

Table 4: Conversion chart for all bonding pads starting with A.

Label	BB #	0°	90°	180°	270°
Ba		27	36	13	22
Bb		29	38	15	24
Bc		31	RF5	17	RF12
Bd		33	RF6	19	RF13
Be		35	RF7	21	RF14
Bf		37	GND	23	GND
Bg		28	RF8	14	RF1
Bh		30	RF9	16	RF2
Bk		32	RF10	18	RF3
Bl		34	RF11	20	RF4
Bm		36	13	22	27
Bn		38	15	24	29
Bo		39	40	1	2
Bp		41	42	3	4
Bq		43	44	5	6
Br		45	46	7	8
Bs		47	48	9	10
Bt		49	50	11	12
Bu		40	1	2	39
Bv		42	3	4	41
Bw		44	5	6	43
Bx		46	7	8	45
By		48	9	10	47
Bz		50	11	12	49

Table 5: Conversion chart for all bonding pads starting with B.

The following table shows how the RF lines and the two grounded bonding pads (in default mount) change when the chip carrier is rotated. To see which connector on the main board each RF bonding pad corresponds to see figure 17. For pinout of the SMP bullets in the puck, see QDev wiki [2].

Label	0°	90°	180°	270°
Ra	RF1	28	RF8	14
Rb	RF2	30	RF9	16
Rc	RF3	32	RF10	18
Rd	RF4	34	RF11	20
Re	RF5	17	RF12	31
Rf	RF6	19	RF13	33
Rg	RF7	21	RF14	35
Xa	GND	23	GND	37
Rh	RF8	14	RF1	28
Rk	RF9	16	RF2	30
Rl	RF10	18	RF3	32
Rm	RF11	20	RF4	34
Rn	RF12	31	RF5	17
Ro	RF13	33	RF6	19
Rp	RF14	35	RF7	21
Xb	GND	37	GND	23

Table 6: Conversion chart for all RF and both GND bonding pads.

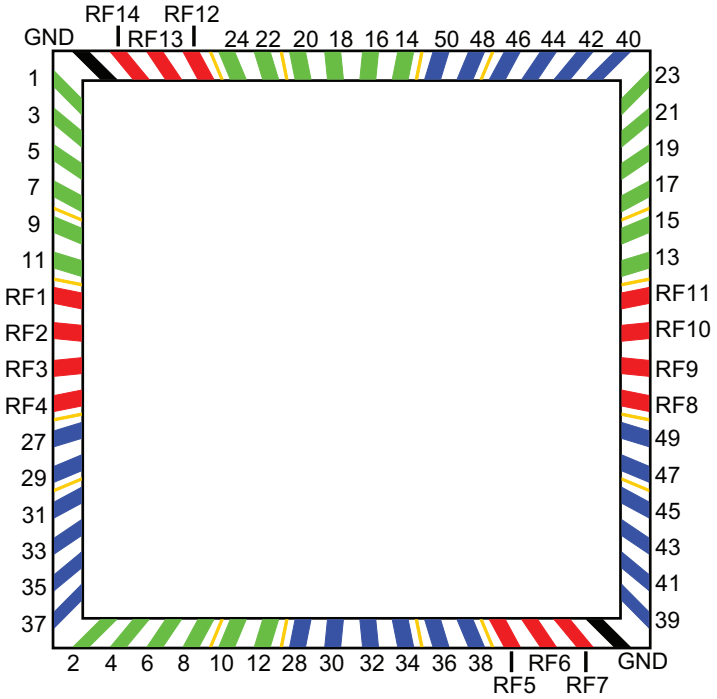


Figure 16: Figure showing the bonding pad layout of the chip carrier in default mount (0 degrees).

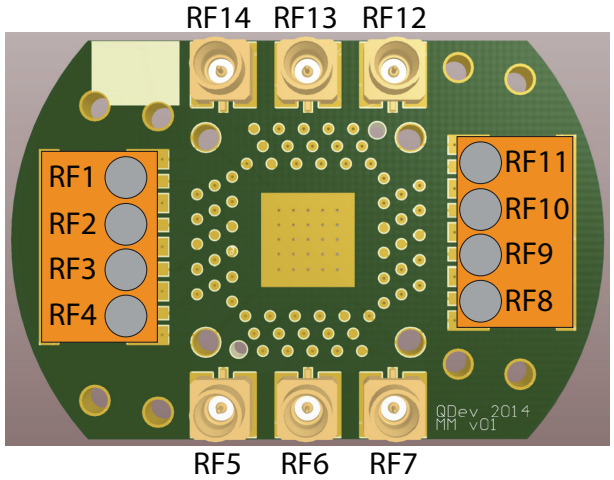


Figure 17: Model view of main board showing which RF connector corresponds to which bonding pad label on the chip carrier.

Appendix D Main board layer schematic

The following two pictures, each with three layer schematics, have been generated using Altium's "Smart PDF" function. Each picture shows the board outline (purple), the copper on the layer (different colour for each layer), and vias (gray).

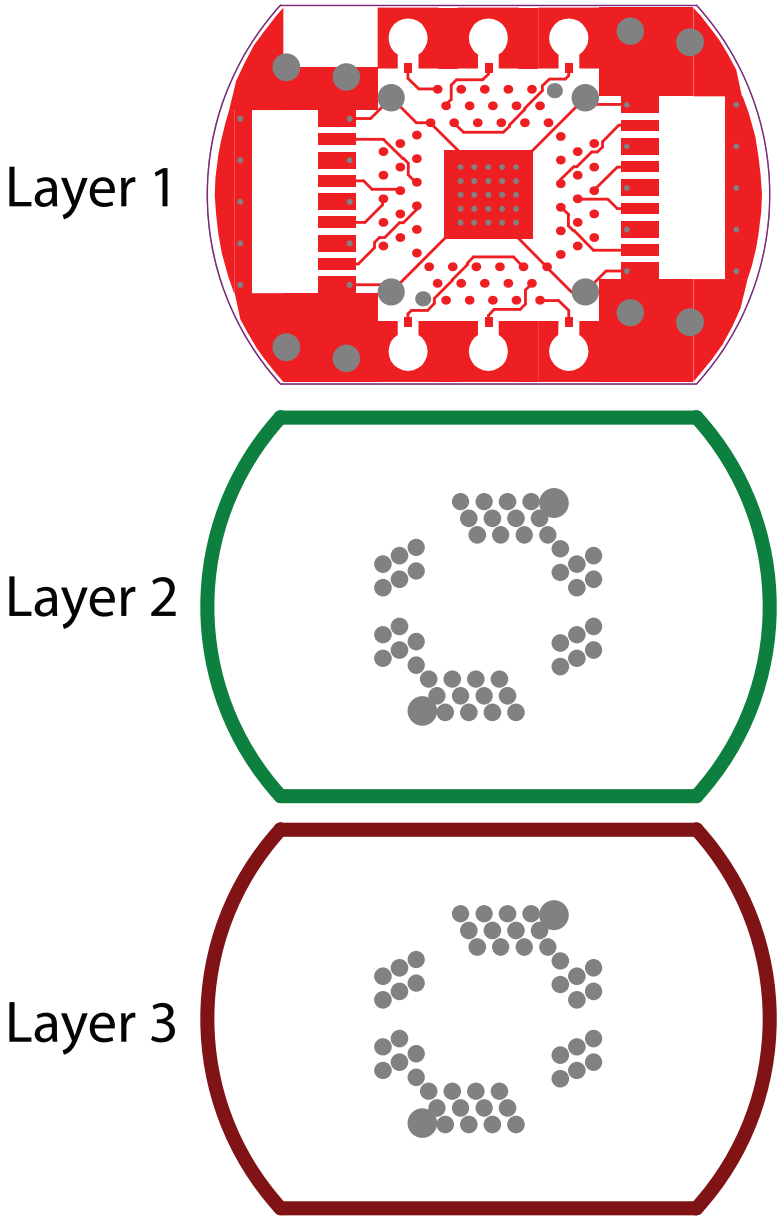


Figure 18: Layer schematic of layers 1-3 of main board. Note that layers 2 and 3 are negative, but layers 1, and 4-6 are positive in colours. This means that layers 2 and 3 don't show where copper is printed, only where copper is not printed.

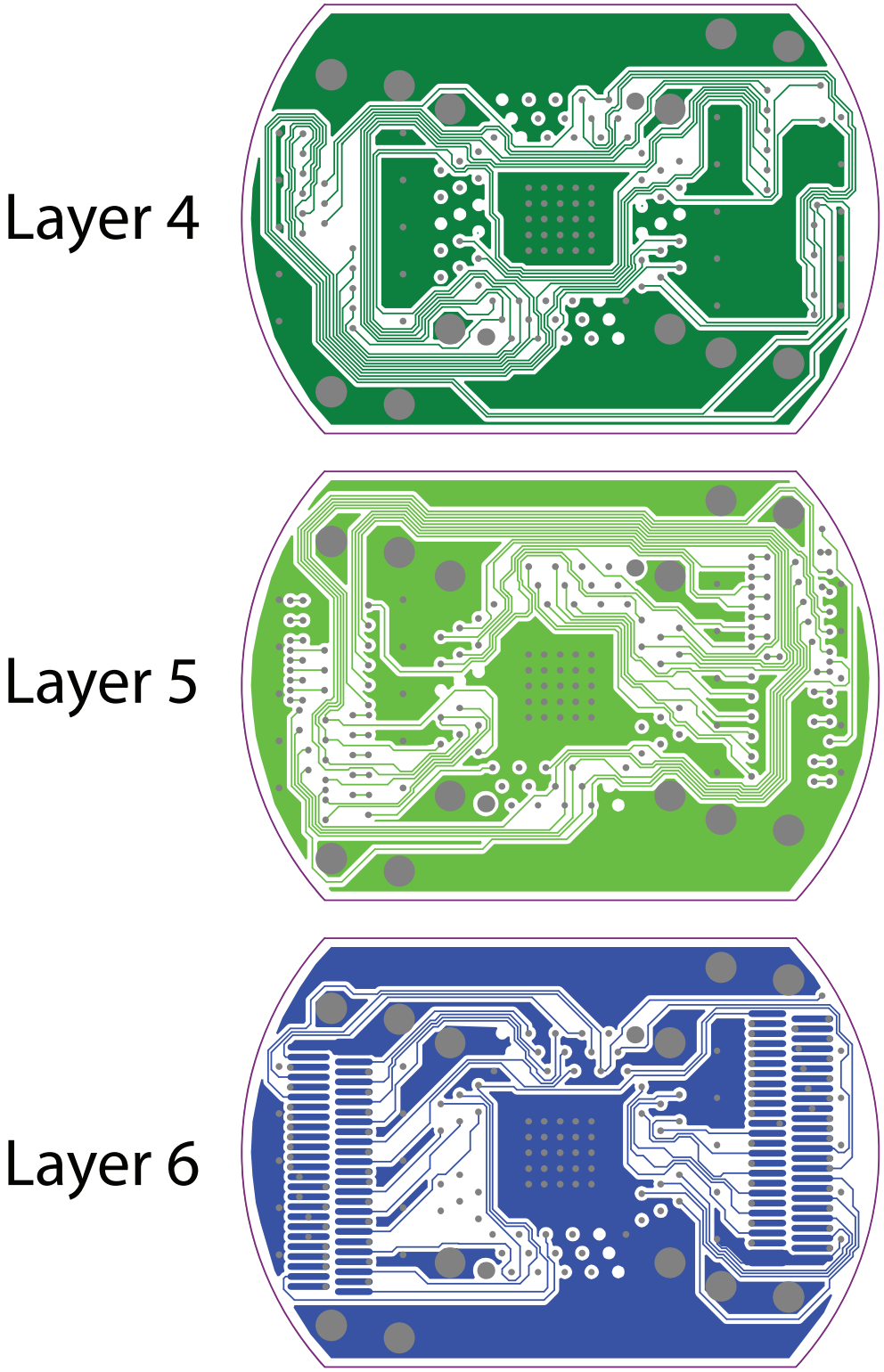


Figure 19: Layer schematic of layers 4-6 of main board.

Appendix E Chip carrier layer schematic

The following three pictures, each with four layer schematics, have been generated using Altium's "Smart PDF" function. Each picture shows the board outline (purple), the copper on the layer (different colour for each layer), and vias (gray). Also shown eight thin gray lines, but these were only used in Altium to define regions and have no physical meaning on the working boards.

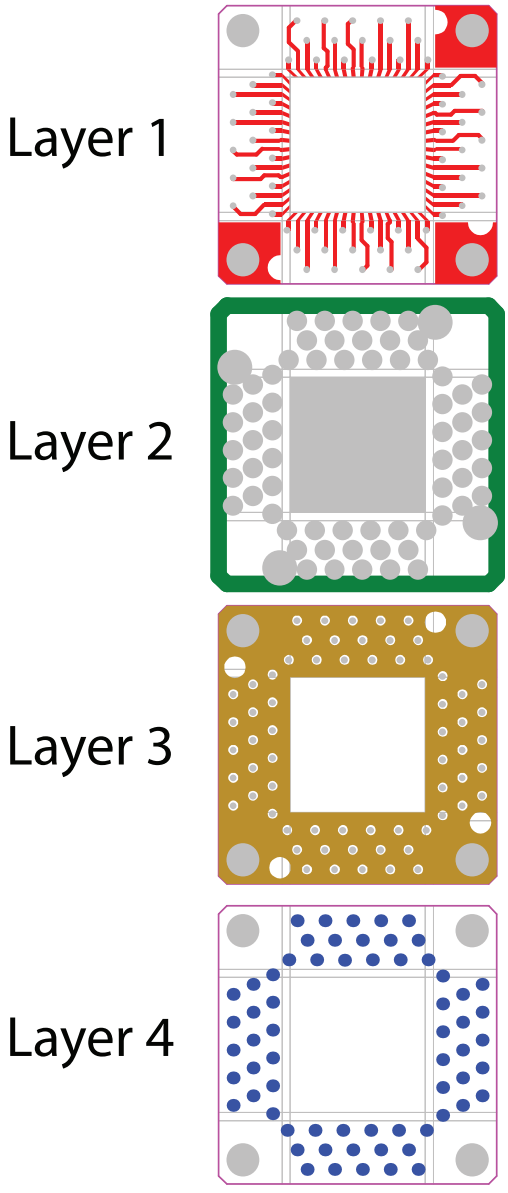


Figure 20

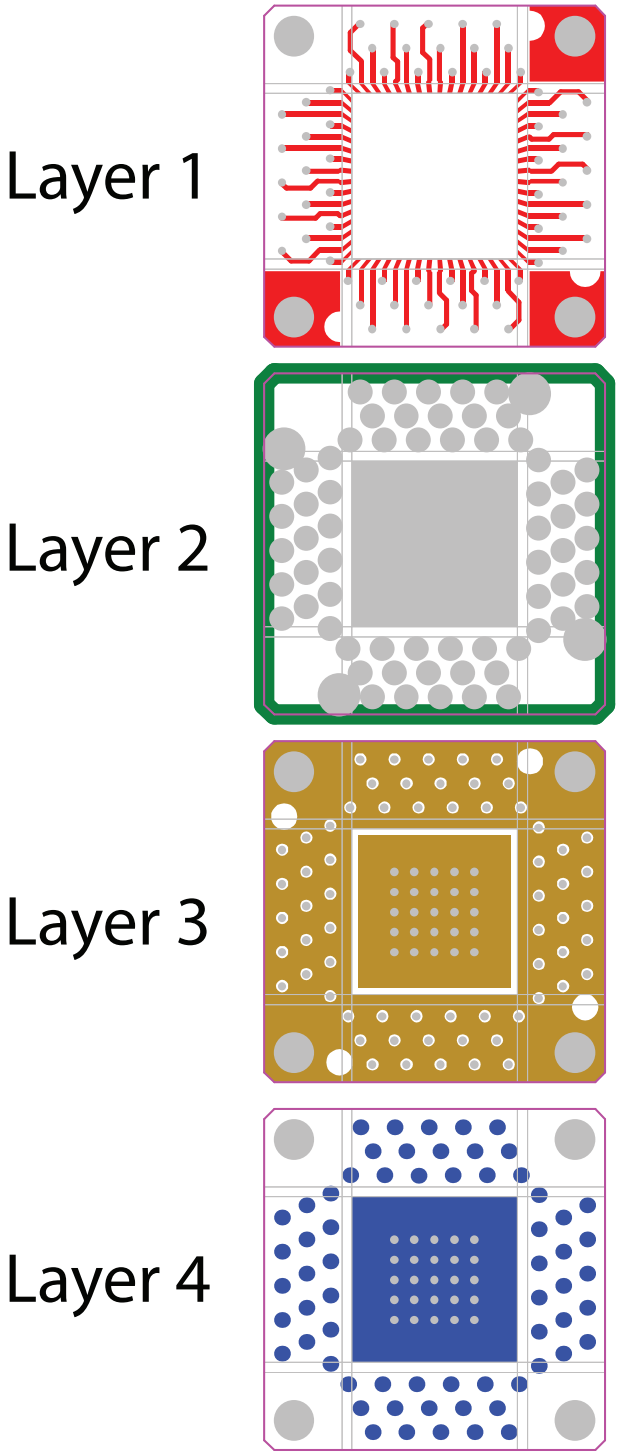


Figure 21

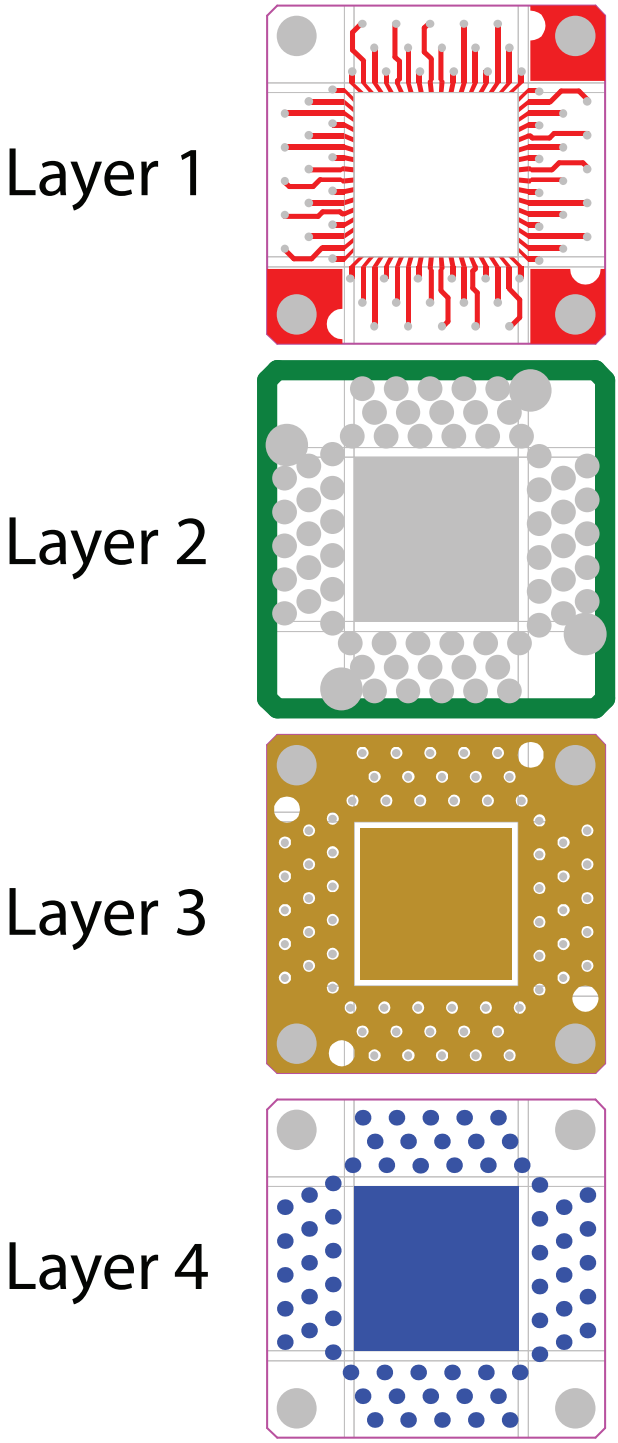


Figure 22

Appendix F Microstrip transmission line equations

When designing impedance matched transmission line structures a question that often went through my head is whether to take the finite thickness t of the conductor into account or not. It turns out, however, that this depends on the height h of your substrate. If $t/h \leq 0.005$ then we can assume the conductor thickness to be negligible and not worry about it affecting the calculated results significantly. This is not the case in the boards I've designed and so I've taken the conductor thickness into account.

The characteristic impedance of a microstrip line with effective strip thickness is given as [11]

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\epsilon_{re}}} \log\left(\dfrac{8h}{W_e} + \dfrac{W_e}{4h}\right) & (W/h \leq 1) \quad (2a) \\ \dfrac{376.7}{\sqrt{\epsilon_{re}}} \left[\dfrac{W_e}{h} + 1.393 + 0.667 \log\left(\dfrac{W_e}{h} + 1.444\right)\right]^{-1} & (W/h \geq 1) \quad , \quad (2b) \end{cases}$$

where the effective conductor width W_e is given as

$$\frac{W_e}{h} = \frac{W}{h} + \frac{\Delta W}{h} \ , \tag{3}$$

and the width correction ΔW is given as

$$\frac{\Delta W}{h} = \begin{cases} \dfrac{1.25}{\pi} \dfrac{t}{h} \left(1 + \log\left(\dfrac{4\pi W}{t}\right)\right) & (W/h \leq 1/2\pi) \quad (4a) \\ \dfrac{1.25}{\pi} \dfrac{t}{h} \left(1 + \log\left(\dfrac{2h}{t}\right)\right) & (W/h \geq 1/2\pi) \quad . \quad (4b) \end{cases}$$

The effective dielectric constant is given by

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F(W/h) - Q \ , \tag{5}$$

where

$$Q = \frac{\epsilon_r - 1}{4.6} \frac{t/h}{\sqrt{W/h}} \ , \tag{6}$$

and

$$F(W/h) = (1 + 10h/W)^{-1/2} \ . \tag{7}$$

When doing high-frequency measurements or using high-frequency circuits in general you'll encounter both losses from the conductor trace and the dielectric substrate. The conductor loss is given by

$$\alpha_c = \begin{cases} 1.38A \dfrac{R_s}{hZ_0} \dfrac{32 - (W_e/h)^2}{32 + (W_e/h)^2} & (W/h \leq 1) \quad (8a) \\ 6.1 \times 10^{-5} A \dfrac{R_s Z_0 \epsilon_{re}}{h} \left(\dfrac{W_e}{h} + \dfrac{0.667 W_e/h}{W_e/h + 1.444}\right) & (W/h \geq 1) \quad , \quad (8b) \end{cases}$$

(in dBm units) where

$$A = 1 + \frac{h}{W_e}\left(1 + \frac{1}{\pi}\log\left(\frac{2B}{t}\right)\right) \ , \tag{9}$$

and the sheet resistivity for the conductor is

$$R_s = \sqrt{\pi f \mu_0 \rho} \ , \tag{10}$$

where f is the frequency and ρ is the resistivity of the conductor. Lastly

$$B = \begin{cases} h & (W/h \geq 1/2\pi) \quad (11a) \\ 2\pi W & (W/h \leq 1/2\pi) \quad . \quad (11b) \end{cases}$$

The dielectric loss is given by

$$\alpha_d = 27.3 \frac{\epsilon_r}{\epsilon_r - 1} \frac{\epsilon_{re} - 1}{\sqrt{\epsilon_{re}}} \frac{\tan\delta}{\lambda_0} \ . \tag{12}$$

with $\tan\delta$ being the loss tangent of the dielectric and λ_0 the free-space wavelength.

Appendix G Characteristic impedance and losses script

Based on the equations seen in appendix F from [11] I wrote the following script in MATLAB to calculate the characteristic impedance of the microstrip traces on the chip carrier.

```
clear all; clc;
W = 0.25; % Width of copper trace
h = [3:10].*10^(-3).*25.4; % standard available thicknesses of FR-4
t = 0.036; % Copper thickness
eps_r = 4.6; % Dielectric constant for FR-4

% The following equations have been found in Gupta
F = (1+10.*h./W).^(-1/2);
Q = ((eps_r-1)/4.6).*((t./h)./sqrt(W./h));

% Effective dielectric constant
eps_re = (eps_r+1)/2 + ((eps_r-1)/2).*F - Q;

for i=1:size(h,2)
    if W/h(i) <= 1/(2*pi)
        deltaWH(i) = ((1.25)/pi)*(t./h(i))*(1+log(4*pi*W/t));
    elseif W/h(i) >= 1/(2*pi)
        deltaWH(i) = ((1.25)/pi)*(t./h(i))*(1+log(2.*h(i)./t));
    else
        disp('bah')
    end
end

% Effective strip width due to nonzero trace thickness
WeH = W./h + deltaWH;

% Characteristic impedance of trace
Z0 = (60./sqrt(eps_re)).*log( 8./WeH + 0.25.*WeH)

% LOSSES
for i=1:size(h,2)
    if W/h(i) <= 1/(2*pi)
        A(i) = 1 + (1+(1/pi)*log(4*pi*W/t))./WeH(i);
    elseif W/h(i) >= 1/(2*pi)
        A(i) = 1 + (1+(1/pi)*log(2*h(i)/t))./WeH(i);
    else
        disp('bah')
    end
end

mu0 = 4*pi*10^(-7); % Magnetic permeability
f = 10^(10); % Operation frequency
rho = 16.78 * 10^(-9); % Resistivity of copper
c= 3*10^8; % Speed of light

Rs = sqrt(pi*mu0*f*rho); % Surface resistivity
```

```
47
48 % Conductor loss
49 alpha_c = (1.38.*A.*Rs./(h.*Z0)).*( (32 - WeH.^2)./(32 + WeH.^2));
50
51 % Loss tangent of FR-4
52 tanD = 0.0037;
53
54 % Dielectric loss
55 alpha_d = 27.3.*(eps_r./(eps_r-1)) .*...
56           ( ( eps_re-1)./sqrt(eps_re)).*tanD/(c/f);
57
58 % Total loss
59 alpa_T = alpha_d+alpha_c;
```

This script is based on the same equations as the previous and is used to calculate the characteristic impedance of the microstrip traces on the main board.

```
1  clear all; clc;
2
3  % CALCULATIONS BASED ON EQUATIONS FROM
4  % "Computer aided design of microwave circuits" by GUPTA et. al.
5
6  format long
7  W = 0.20;
8  h = 0.5*0.254;
9  t = 0.036;
10 eps_r = 4.6;
11
12 F = (1+10*h/W)^(-1/2);
13 Q = ( (eps_r-1)/4.6 )*( (t/h)/sqrt(W/h) );
14 eps_re = (eps_r+1)/2 + ((eps_r-1)/2)*F - Q;
15
16 if W/h <= 1/(2*pi)
17     deltaWH = ((1.25)/pi)*(t/h)*(1+log(4*pi*W/t));
18     disp(1)
19 elseif W/h >= 1/(2*pi)
20     deltaWH = ((1.25)/pi)*(t/h)*(1+log(2*h/t));
21     disp(2)
22 else
23     disp('bah')
24 end
25
26 WeH = W/h + deltaWH;
27
28 if W/h <= 1
29     Z0 = (60/sqrt(eps_re))*log( 8/WeH + 0.25*WeH)
30 elseif W/h >= 1
31     Z0 = ( 376.7/sqrt(eps_re) ) * ( WeH + 1.393 + 0.667 * log( WeH +...
32           1.444) )^(-1)
33 else
34     disp('bah')
35 end
```

```
36
37 % LOSSES
38 if W/h <= 1/(2*pi)
39     A = 1 + (1+(1/pi)*log(4*pi*W/t))/WeH;
40     disp(1)
41 elseif W/h >= 1/(2*pi)
42     A = 1 + (1+(1/pi)*log(2*h/t))/WeH;
43     disp(2)
44 else
45     disp('bah')
46 end
47
48 mu0 = 4*pi*10^(-7);
49 f = 10^(10);
50 rho = 16.78 * 10^(-9);
51 c = 3*10^8;
52
53 Rs = sqrt(pi*mu0*f*rho);
54
55 alpha_c = (1.38*A*Rs/(h*Z0))*( (32 - WeH^2)/(32 + WeH^2));
56 tanD = 0.0037;
57 alpha_d = 27.3*(eps_r/(eps_r-1)) * ( ( eps_re-1)/sqrt(eps_re))*tanD/(c/f);
58
59 alpa_T = alpha_d+alpha_c
```

Appendix H QDev breakout box

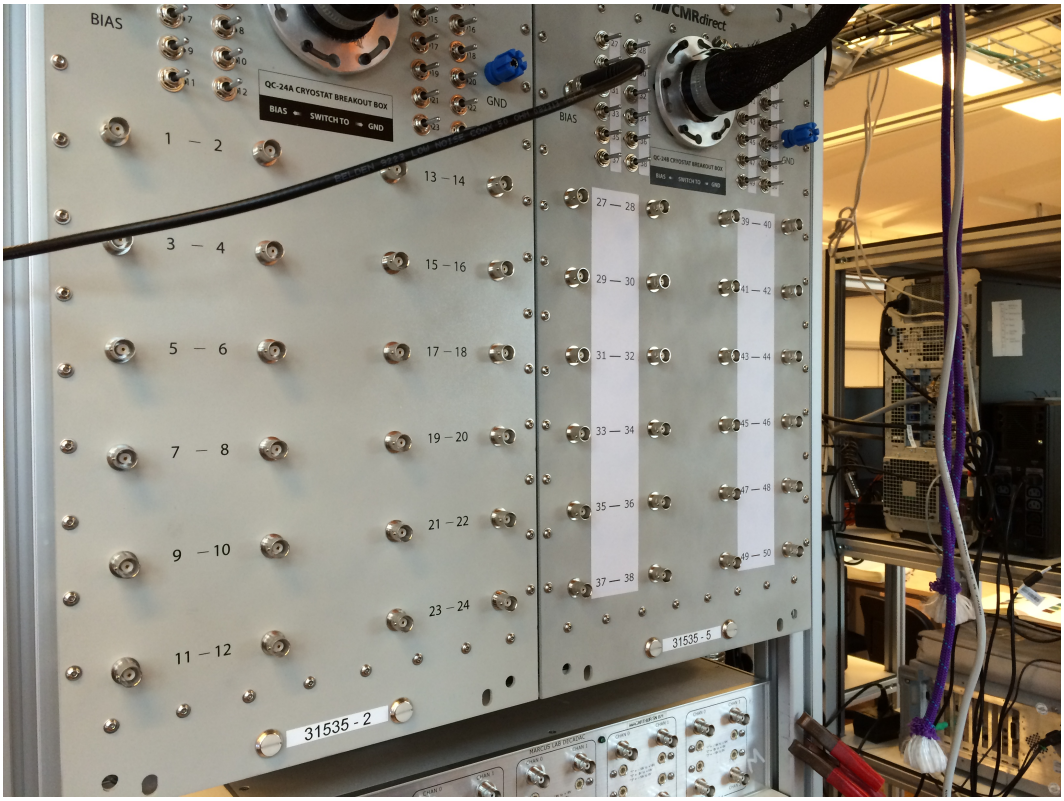


Figure 23: Photo of the breakout boxes which all fridge stations are equipped with. The numbers on the breakout box correspond to the nano-D pin number.

Appendix I QDev load-lock

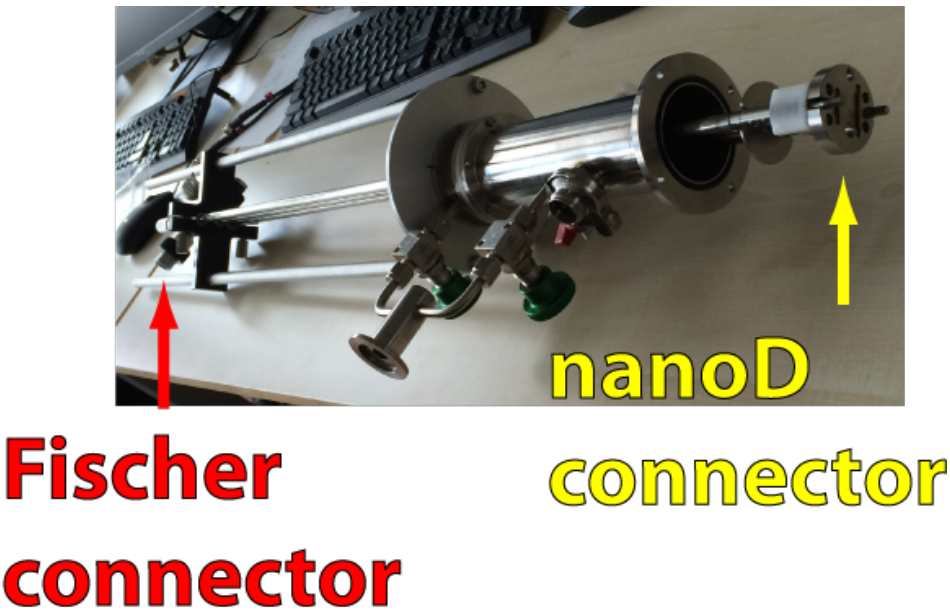
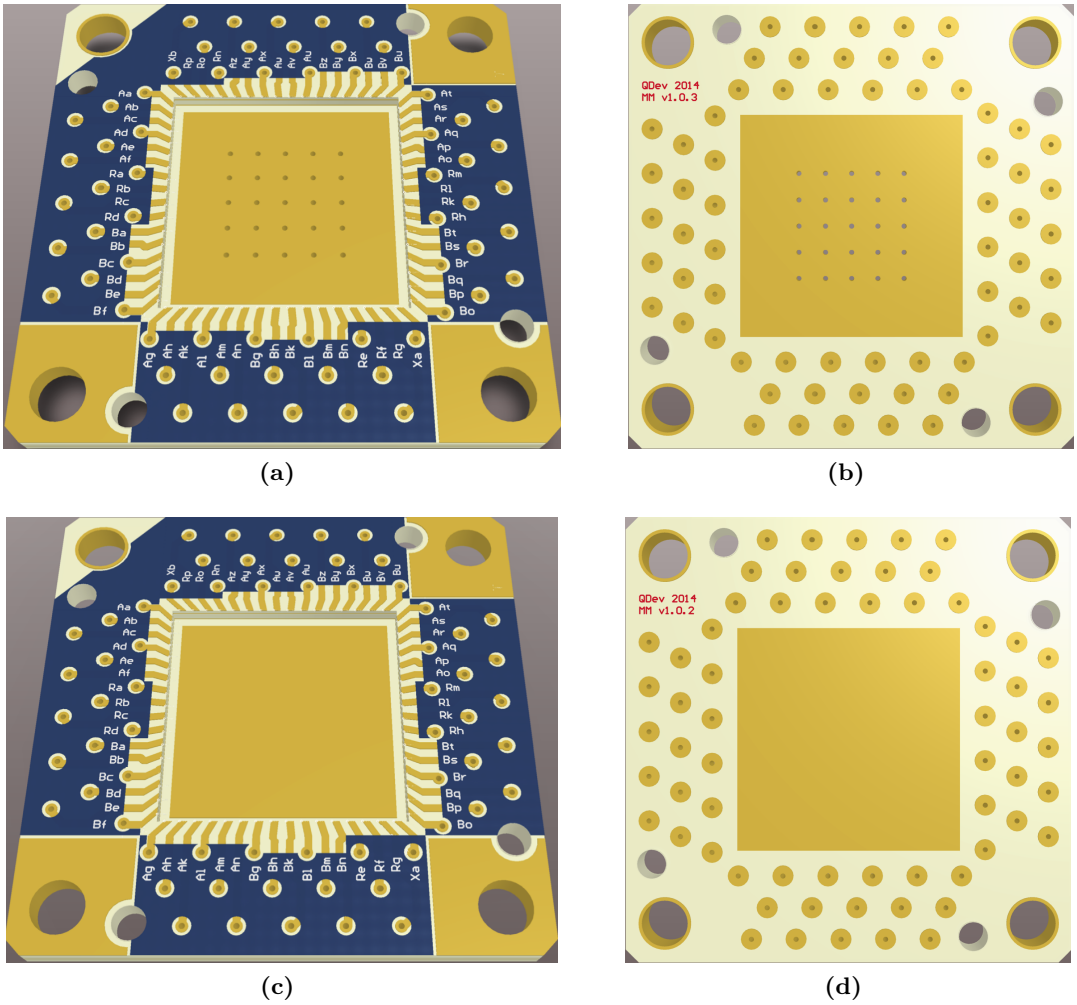


Figure 24: Photo of the load-lock used in QDev. The load-lock is used to mount the bottom nano-D connector with the mating piece on the load-lock. This enables us to load and unload the puck without the need to warm up the whole fridge.

Appendix J Chip carrier designs



(a) **(b)**

(c) **(d)**

Figure 25: Figure showing the two other chip carrier designs with (a) and (b) showing top- and bottom view, respectively, of the version with the plated cutout region acting as cold ground, and (c) and (d) showing top- and bottom view, respectively, of the version with the plated cutout region acting as a backgate.

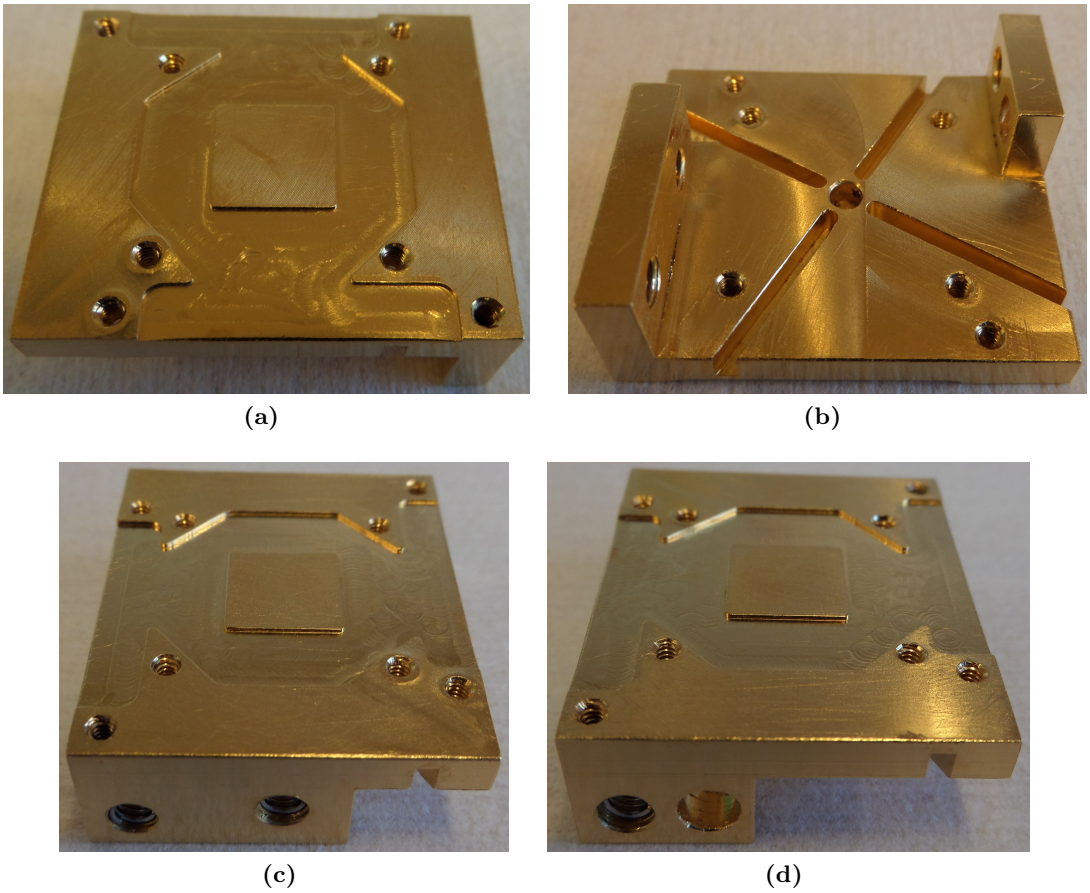
Appendix K Flexboard design

(a)

(b)

Figure 26: A 3D generated photo of the flexboard prototype which would allow us to characterize the use of flexboards for low-temperature measurements where (a) shows the top view and (b) shows a side view. The FPC is fitted with eight smooth bore SMP edge-mount connectors. The FPC is a four-layer rigid-flex $\sim$0.5 mm thick at the ends, and $\sim$0.2 mm thick along the thin strip.

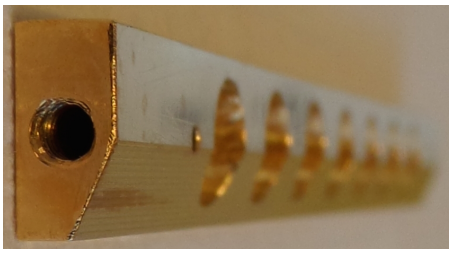
Appendix L New mounting bracket and stabilizing rods



(a) **(b)** **(c)** **(d)**

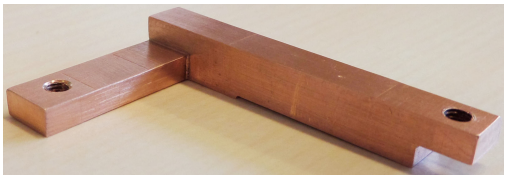
Figure 27: Photo of the new mounting bracket from (a) the front, (b) the bottom, and (c) and (d) both sides. The tapped holes in (c) and (d) are fitted with stainless steel M2.5 helicoils. The small drill holes on the top side of the mounting bracket are the M1.6 holes used to mount the boards onto the bracket.

(a)

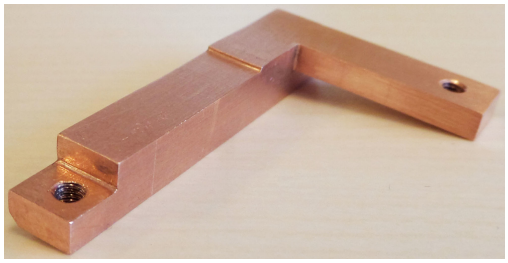


(b)

Figure 28: Photo of the new stabilizing rods with (a) and (b) shows them from the side and the end, respectively. The big holes in (a) are M3 holes used as M2.5 clearance holes for mounting of the mounting bracket. The small holes are made to make sure we don't have trapped air when putting the puck in a vacuum. (b) Shows the in both ends of the stabilizing rods used to mount them to the top and bottom piece of the puck.



(a)



(b)

Figure 29: Photo of the new parallel mounting arm for the new mounting bracket shown from (a) the top and (b) the bottom.