



Patterning of complex oxide interfaces based on $\text{SrTiO}_3/\text{LaAlO}_3$ heterostructures using photolithography

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Nanoscience

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Patterning of complex oxide interfaces based on SrTiO₃/LaAlO₃ heterostructures using photolithography

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The two-dimensional electron system (2DES) found in the SrTiO₃/LaAlO₃ interface displays interesting properties. In this study, the Heidelberg μ PG 501 LED writer has been used to pattern the interface. The limit of photolithography using this light source has a resolution of to $1\mu\text{m}$. The study also shows, the possible use of photoresist working as hard mask instead of LSM, making the fabrication process less complicated. Furthermore, the longitudinal resistance is accurately explained with the two band model taking multiple charge carriers into account. The measurements showed the temperature dependency of the permittivity which results in a decrease in the sheet resistance with a decreasing temperature in the $10\text{ K} < T < 100\text{ K}$ regime.

I. INTRODUCTION

The research of finding new materials to fabricate electronic devices is one of the major quests in modern physics. Since the discovery of the two-dimensional electron system (2DES) in the interface of two band insulating oxides, namely SrTiO₃ (STO) and LaAlO₃ (LAO) they have been the pivot of vast interest in material science [1]. STO/LSM interface displays fascinating properties such as superconductivity [2] and gate tunable superconductivity[3]. The presence of the conducting interface requires a LAO topfilm of 4 unit cells (uc), although it was showed that the interface becomes conductive at 3uc by inducing an electric field with the backgate [4]. Furthermore, it was discovered that the interface is not damaged by optical lithography[5], although a accurate patterning still remains a challenge. In this study, three samples have been fabricated. The first sample (S1) is a (001), and has photoresist as a hard mask insulating STO from LAO making it possible to pattern a design. Amorphous-LAO (a-LAO) was used in this study[6]. Photoresist is not capable of high temperatures, making a-LAO a suitable topfilm. The other samples (S2 and S3) have LSM as hard mask, but are (001) and (111) respectively. In the beginning of this study the focus was on using LSM, but when it was demonstrated using photoresist as hard mask, while still having a conductive interface, the focus changed. Using photoresist instead of LSM makes the fabrication process easier. Therefore, figure 3 shows 6 hall bars with corresponding AFM images for S2 rather than S1, which the low temperature measurements has been performed on.

II. FABRICATION

The fabrication process involves these following steps: *TiO*₂ termination, deposition of insulating mask, photolithography, wet etching and deposition of a-LAO. The process is sketched in figure 1. *TiO*₂ termination is performed because the interface is only achieved when the STO substrate is *TiO*₂ terminated [7]. In order to achieve terminated *TiO*₂, chemical treatment and furnace annealing is executed. The procedure is described in appendix A. The LSM is deposited using pulsed laser deposition (PLD) due to the easy and precise usage. The deposition is performed at room temperature (RT) at ultra high vacuum. After the hard mask is applied, a layer of $0.5\mu\text{m}$ thick photoresist (AZ1505) is spin coated on top, followed by UV exposure using Heidelberg μ PG 501 LED writer, which has a wavelength of 390nm. Although the wavelength is 390 nm, the expected resolution for the channels thickness and the spacing is $1\mu\text{m}$ which was estimated in earlier local observations. The next step is to develop (MF321) followed by etching using a LSM etchant. The etchant is a 2:2:35 solution of KI(3M):HCl(35%):H₂O, the same solution as used by F. Trier et al[8]. The residual resist is removed using NMP for 5 minutes at 80°C and plasma ashing for 2 minutes to ensure the sample is clean of organic matter. Atomic force microscopy (AFM) images is made to make sure the etchant has reached the STO substrate. Figure 2 shows the sample after the etching process. Panel (a) is the channels for the leak current measurement, where there is $2\mu\text{m}$ between the etched channels. Panel (b) shows the devices for measuring if the devices is conductive. (c) shows a AFM images of (a) to verify the distance between the channels, where the yellow area is the LSM, which is not etched. A hall bar (d) has been etched successfully as well. It is possible to observe terraces in the

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etched area. The last step in the fabrication is to deposit LAO with PLD, where 12nm is deposit, which should be enough to make the conducting interface[4]. Although figure 1 shows the method for patterning using LSM as hard mask, this could be performed using photoresist instead. If using photoresist instead of LSM one could skip step (b), (d) and (e). This means, after the TiO_2 termination, photoresist is spin coated on the substrate followed by exposure and development. From this step, it is possible to deposit a-LMO, in the same way as if LSM was used.

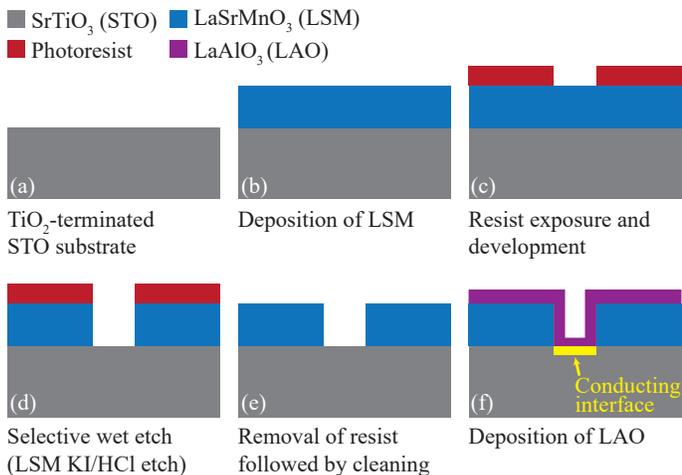


Figure 1. Schematic of the fabrication process. First the STO substrate has to be TiO_2 terminated (a). To make a pattern interface a LSM top film is deposit (b). Photoresist is applied followed by exposure and development and a wet etch is executed (c) and (d). The remaining resist is removed (e), and the LAO film is applied (f). Virtually the same process has been executed in order to fabricate the resist sample. If one use photoresist as insulating hard mask separating the STO substrate from the LAO topfilm, panel (b), (d) and (e) should be skipped.

The contact connecting the interface with the measurement equipment were prepared connecting Al wires attached to the bond pads of the sample to a daughter-board. This was done using an automatic ultrasonic Al-wire bonder making a linear four point probe method. The sample is attached with conductive silver paste. The room and low temperature measurement were measured using the setup as described in appendix D. The low temperature was achieved using an Oxford He cryostat equipped with a 6 T superconducting magnet making a perpendicular field through the sample.

III. RESULTS AND DISCUSSION

Transport measurements were executed both at room temperature as seen on figure 2 and low temperature as seen on figure 4.

Figure 2 (e) shows the room temperature measurements,

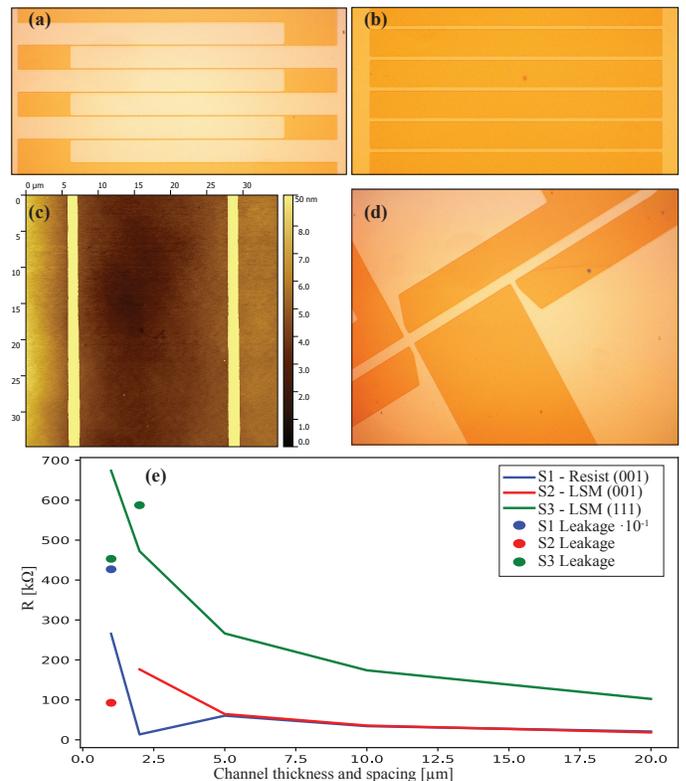


Figure 2. (a) shows an optical image of the device testing for leak current. The device imaged is with a $2 \mu m$ gap and (b) shows an optical images of the device testing to see of the deive is conducting with an channel of $2 \mu m$. Panel (c) shows an AFM images of (a), where the yellow lines are the barriers separating the channels. A hall bar with a channel thickness is seen on panel (d). The devices have been measured as shown on panel (e), where solid lines are for the device testing if it is conductive at a thickness of $10 \mu m$, and the dots is the device which showed leak current. The leakage measurement for S1 is a factor 10 larger than shown on the figure.

where the solid lines display the conducting devices and the dots are for the leak current devices. The x axis displays the increasing thickness, the y-axis displays the measured resistance. It shows the channels are conductive down to $1 \mu m$ except for S2, where it is conductive until $2 \mu m$. This is due to an error in the fabrication process as seen on figure 13 in appendix E. The results correlate great with the presumption, which sets the limit of photolithography with the Heidelberg μpg 501. Figure 2 (e) also shows the resistance is almost proportional with the inverse channel thickness $R \propto \frac{1}{W}$. Although it turns out, the resistivity is not constant, which is difficult to tell why. The leak current measurements showed the sample with photoresist as hard mask, had a more confined patterning with a much larger resistance at $1 \mu m$ gap between the wires than the samples with LSM indicating a weaker leak current is present. The (111) sample STO/LSM/a-LAO showed leak at $2 \mu m$. Also, the (111) sample showed a much larger resistance than the (001)

sample at 1 μm distance. This means, in order to make the most precise samples, photoresist might be a better hard mask than LSM. The measurements have been executed using a four-point probe method. The measured resistance is not an absolute value, hence the resistance changed with a couple of hundred ohm, by changing the source/drain cable with the probe cables.

It was believed, there was a local enhancement in the conductivity at certain domains on the sample[9] and the conductance would be enhanced in certain orientation which was showed by B. Kalisky et al. [10]. This gave rise to make 6 hall bars with orientation going from 0° to 150° with a 30° shift of the hall bars. This is seen on figure 3. The terraces on the sample have the same orientation, although there is a slightly change in the direction of the terraces, however the direction of the terraces is not believed to influence the conductivity, it is rather the orientation of the crystal lattice. The measurement however did not seem to show a clear sign of enhancement in the conductance, even though it is not the same sample which was measured on figure 4 that was shown on figure 3. The measurement is seen on tabel 15 in appendix E. . The channel which has been measured both at a room temperature and low temperature is $30\mu m$, which is larger than the domains, meaning no enhancement in the conductivity is expected. Although, HB5 in the low temperature measurements has a continual lower conductance than the other hall bars. If this is due to the domain effect or the change in orientation it is difficult to determine. As mentioned above, low temperature measurements has been performed. The measured hall bars have a channel thickness of $30\mu m$, as seen in appendix B. Figure 4 shows the measurements. The measurements have been performed on sample S1 (resist sample).

Figure 4 (a) shows the cooldown of the sample. The conductance increases until 10 K, from where it begins to go down with a decreasing temperature. In the temperature in the 10K to 100K regime the resistance is expected to decrease with T^2 [11]. However n-type STO is strongly dominated by contribution from electron-phonon scattering R_{el-ph} , where $R_{el-ph} \propto T^2$ were expected, but the sheet resistance depends on impurity scattering R_{imp} as well [12]. The impurity scattering comes from oxygen vacancies, where the vacancies can act as a charge trap. In order to explain the fully dependence of the sheet resistance the permittivity needs to be taken into account as well. The permittivity depends on the temperature, which is described using the Barrett formula [13]:

$$\epsilon(T) = C (T_1/2 \times \coth (T_1/2T) - T_0)^{-1} \quad (1)$$

Where C is the Curie constant, T_1 is the dividing point between the low temperature region, where the quantum effect becomes important[13] and T_0 is the critical temperature taken from the classical mean field theory. This means, when the temperature decrease the permittivity will increase due the hyperbolic function, and the expression is in the inverse of the permittivity. Using

Fermi's golden rule giving us $R_{imp} \propto N_i V^2$ and $V \propto \epsilon^{-1}$, where N_i is the number of charge traps and is dependent of the temperature. This means, if ϵ is large the potential will decrease resulting in smaller R_{imp} at lower temperatures[12]. Plotting equation 2 with the parameter from D. Fuchs et al. paper give a mathematical model as shown in appendix E, which fits the observation in this study. Due to lack of time, the data has not been fittet. The impurity scattering is dependent of the number of charge traps impurities as well. Following Matthisen's rule, where the net resistance is the sum of the contribution gives: $R_s = R_{imp} + R_{el-ph}$. Substituting the equations results in an equation explaining the sheet resistivity[12]:

$$R_s(T) = A \left[1 - \exp \left(-\frac{T_a}{T} \right) \right] \left[\frac{T_1}{2} \coth \left(\frac{T_1}{2T} \right) - T_0 \right]^2 + B \times T^2 \quad (2)$$

A accommodates C and N_0 , T_A and T_1 are fitting parameters, as well as B is a fitting parameter. Equation 2 shows a decreasing temperature as the number of charge traps increasing, as seen on the first term: $\left[1 - \exp \left(-\frac{T_a}{T} \right) \right]$. The second term is the effectivity of the charge traps. This term states R_s decrease until $T = T_1$ where R_s begins to increase again. However, this is not the only contribution to the sheet resistance. As equation 2 states, the last term scale with the squared temperature times a fitting factor. This term decrease with a decreasing temperature. At the 10 K to 0 K regime the resistance begins to increase. Other studies suggest this might be due to the Kondo effect. Brinkman et al. showed that polar discontinuity is the cause of the Kondo effect rather than oxygen vacancies [14]. Although it is difficult to determine if the Kondo effect is cause of the increase in resistance in this study. The decreasing conductance could also be caused by the impurity scattering taking over due to the low temperature. Looking on figure 14 in appendix E which shows the model as it would occur in D. Fuchs et al. In that model, the conductance begins to decrease at around 30 K. This is however with the fitting parameter in their study, which very likely would look different in this study. The last dip at the cooldown is due to a failure of the cryostat, which caused the temperature to rise and fall. Both conductivity of the device and the dip has changed after the backgate traces seen on figure 4 (d), where the backgate has been swept from 0V to -50V to 50V and back to 0V. The mobility and electron density is calculated using the slope of figure 4 (b) fitting from 1 T to 5T, which is before the applied electric field. The same has been done after the backgate sweeps (figure not shown). This shows the mobility and electron density has changed, which correlate with the change in conductance. The mobility and electron density before the backgate traces were both calculated: $\mu_{HB1,before} = 660.31 cm^2/Vs$ and $n_{s,HB1,before} = 2.07 \cdot 10^{13} cm^{-2}$ for hall bar 1 and hall bar 4 gives:

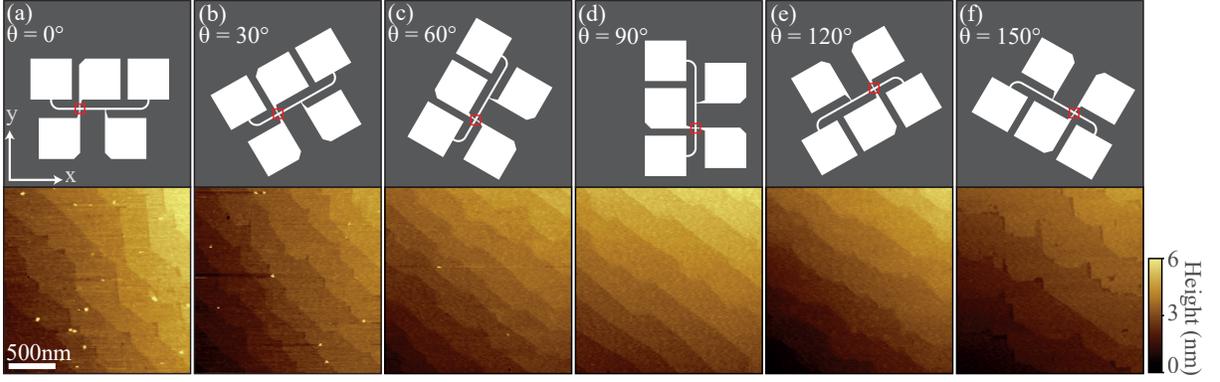


Figure 3. Schematic of six hall bars with a changing orientation (θ) with corresponding atomic force microscope (AFM) images matching the red squares. The channel of the hall bars have a width of $30\mu\text{m}$. The scale bar is 500nm . Going from (a) with an angle of 0° to (f) with an angle of 150° , the hall bars change with an interval of 30° for each step. The AFM images has been taken with the same angle for all the hall bars. All the AFM images shows approximate the same terraces structure with only a slight change in the direction, suggesting the directing of terraces is consistent throughout the whole sample.

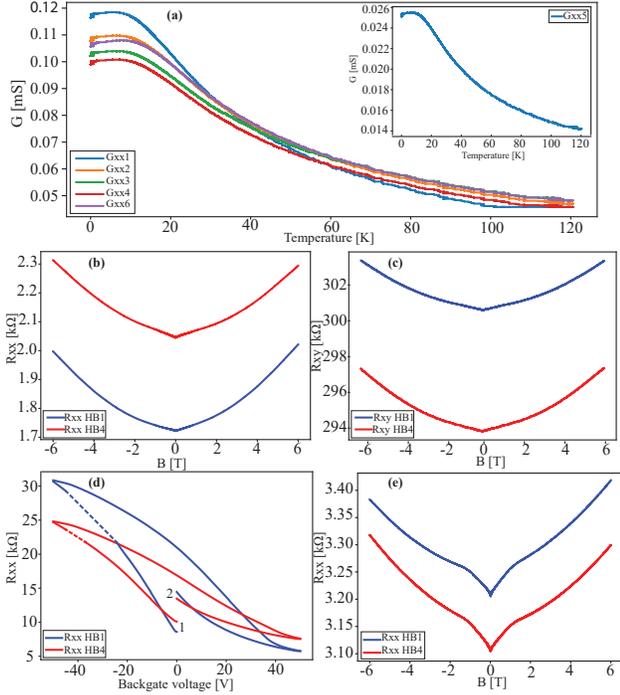


Figure 4. Low temperature measurements. (a) shows the change in conductance in range of $\sim 0\text{ K} < T < 120\text{ K}$, showing the conductance increase as the 2DEG is cooled down. (b) shows the longitudinal resistance as a function of the magnetic field, while (c) is the Hall resistance calculated from the slope of a linear fit of V_{xx} , from where the electron density is calculated and R_H is obtained. (d) shows backgate sweeps beginning in 1, from where it goes to 50V , back to -50V and back to 0V at the 2 mark. The dotted line is due to the equipment overloading, resulting in removing the data and drawing an artificial line, which serve as guidance. (e) is the longitudinal resistance after the gate traces in figure (d), showing a larger dip near $B = 0\text{ T}$.

$\mu_{HB4,before} = 456.27\text{cm}^2/\text{Vs}$ and $n_{s,HB4,before} = 2.12 \times 10^{13}\text{cm}^{-2}$. After the backgate traces the values changed to: $\mu_{HB1,after} = 309.87\text{cm}^2/\text{Vs}$ and $n_{s,HB1,after} = 2.4 \cdot 10^{13}\text{cm}^{-2}$ for hall bar 1 and $\mu_{HB4,after} = 221.04\text{cm}^2/\text{Vs}$ and $n_{s,HB4,after} = 3.50 \times 10^{13}\text{cm}^{-2}$. Using $\sigma = e\mu n_s$ this agrees with the change of hall bar 1 having a lower resistance than hall bar 4 in figure 4 (b) to hall bar 1 having a larger resistance in figure 4 (e). A larger dip in (e) after the gate sweeps is noticeable as well. Similar phenomenon has been seen by A. D. Caviglia et al. They show an applied electric field can change the spin coherence. They have a possible interpretation saying, there might be a presence of strong spin-orbit coupling which counteract the weak localization making weak antilocalization. The study did the measurements above the threshold of superconductivity to neglect the effect from the superconductive phase. Even though the measurements were executed at $\sim 20\text{mK}$ in our study, no sign if superconductivity were seen. If the dip in figure 4 (e) is due to an enhancement in the spin orbit coupling or something different is difficult to tell. Not only does figure 4 (b) show a dip near $B = 0\text{ T}$, but it also shows an aberrant longitudinal resistivity, rather than a constant resistivity in a changing external B-field. In order to explain the increasing resistivity at increase magnetic field, the two band model can be used to explain this behaviour [15]. At high magnetic field regime, the resistivity is given by:

$$\rho_{xx} = \frac{(n_1/\mu_1) + (n_2/\mu_2)}{e(n_1 + n_2)^2} \quad (3)$$

This fits the observation on figure 4 (b). For the low magnetic field regime, the resistivity is given by:

$$\rho_{xx} = \frac{1}{e(n_1\mu_1 + n_2\mu_2)} \quad (4)$$

This means, in order to explain the the longitudinal resistivity the two band model come in use. The model uses the contribution from both charge carriers, meaning if the charge density and the mobility changes for one of the charge carriers the slope of the resistivity changes. In conclusion, this means the dip near $B = 0$ T in figure 4, could be explained by a change in the carrier density due to change in the charge carrier, which leads change in the resistivity.

IV. CONCLUSIONS

In summary, this study shows evidence for making patterning down to $1 \mu\text{m}$ before the the device cease to conduct, and down to $2 \mu\text{m}$ before they begin to leak current. The varying orientation of the hall bar did not seem have any noticeable influence on the conductance in a $30 \mu\text{m}$ channel. Furthermore, the samples showed great dependence of the external magnetic field, which could be explained by the two band model, due to a change in the

charge carrier. An enhancement in spin-orbit coupling in the after sweeping an electric field to $\pm 50\text{V}$ might appear and show sign of what could be weak antilocalization, but the sweep of the electric field might also have made the mobility of the sample lower. Finally, using photoresist as hard mask instead of LSM, could make the further fabrication processes less complicated, and more confined. Further studies is needed to examine other kinds of resist e.g. e-beam resist to make structures in higher resolution.

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Appendix A: Substrate treatment

This procedure has developed by Dennis. V Christensen, Felix Trier and Yunzhong Chen

Chemical treatment

1. **Preheat water** in an ultrasonic bath to 70°C (7/8 filled)
2. **Immerse substrate in EtOH** and sonicate for 5 min. at RT followed by drying and defect/dirt inspection
3. **Repeat step 2 with acetone.**
4. **Immerse substrate in milli-Q water** (or de-ionized-water) and sonicate for 20 min. at 70°C followed by drying and defect/dirt inspection.
5. Prepare an 3 : 1 : 16 $\text{HCl}(37\%) : \text{HNO}_3(66\%) : \text{H}_2\text{O}(\text{milli} - \text{Q})$ acid solution (e.g. 9ml:3ml:48ml for a total of 60ml) by adding HCl slowly to HNO_3 (and not visa versa). Let it be for 5 min. **Immerse substrate in acid solution** and ultrasonicate for 20 min. at 70°C and transfer directly to water (step 6). Clean alumina oven boxes with the acid solution.
6. **Immerse substrate in milli-Q water** (or de-ionized water) and sonicate for 30 s. at RT followed by drying and defect/dirt inspection.

Annealing in tube furnace

1. **Place** tube in furnace with $\approx 13\text{cm}$ of each tube-end outside the furnace. Check the thermocouple with corresponding plug in rear end reaches 50 cm into the tube.
2. **Place** substrate in alumina boxes and insert the box close to thermocouple **in the center of the furnace.** Set the flowrate of oxygen through the tube to ≈ 10 (arbitrary units) with 5-10 bubbles per second in the bubble-bottle (with 500ml water).
3. **Bake substrate** by ramping $100^{\circ}\text{C}/\text{h}$ to 1000°C in tube furnace and hold for 1 h then ramp to 25°C at $100^{\circ}\text{C}/\text{h}$

Appendix B: Design in the patterning

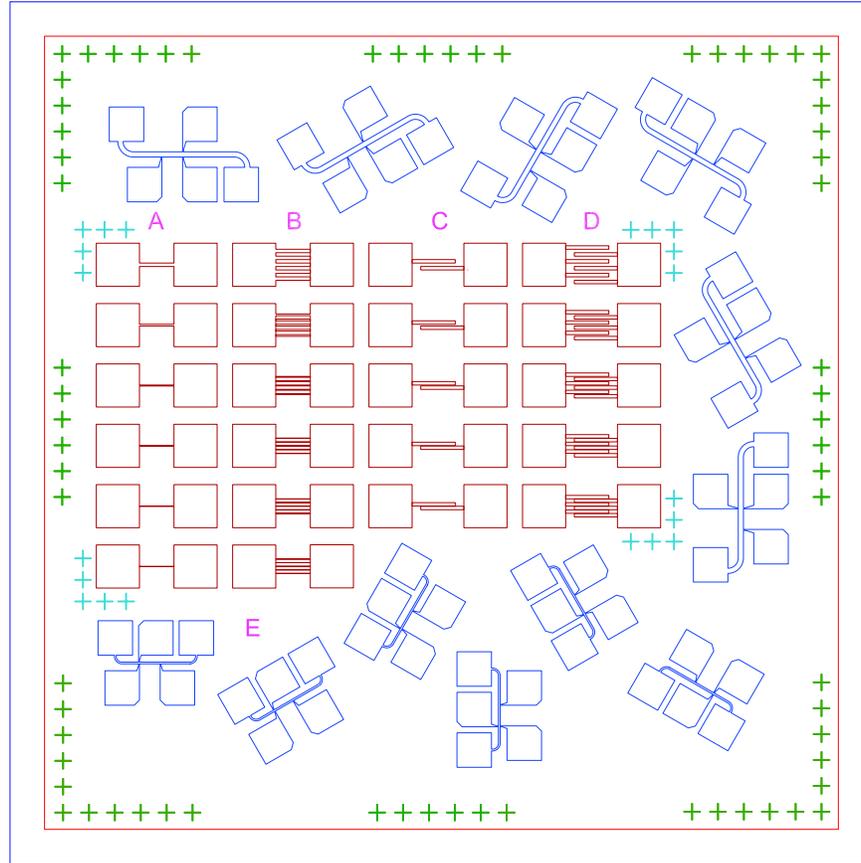


Figure 5. Schematic of the design used in this study. The design consist of 5 series: A, B, C, D and E, and a non indexed series with consist of 6 hall bars. A and B has an decreasing channel thickness going from $20\ \mu m$ to $0.5\ \mu m$. C and D has a spacing between the channels with an decreasing distance going from $20\ \mu m$ to $1\ \mu m$

- . The E series consist of 6 hall bars with a channel thickness of $10\ \mu m$ and a chaning orientation. The non indexed hall bar series is the same as E but with a channel of $30\ \mu m$.

Figure 5 shows the patterning design used in this study. The design consist of 5 series indexed A, B, C, D and E and a non indexed series, contains 6 Hall bars. The purpose of series A and B was to see how wide it was possible to make the channels before they ceased to conduct. Serie A has one channel, while serie B has five channels. The thickness degrease from $20\ \mu m$, $10\ \mu m$, $5\ \mu m$, $2\ \mu m$, $1\ \mu m$ and to $0.5\ \mu m$. It was expected for the Heidelberg $\mu PG\ 501$ with the etch to have a resolution down to $1\ \mu m$. Series C and D was to see how close it was possible to place patterns to each other before they began to show sign of leak current. To examine this, two channels with a thickness of $20\ \mu m$ were placed with a distance of $20\ \mu m$, $10\ \mu m$, $5\ \mu m$, $2\ \mu m$ and $1\ \mu m$ from each other. The E series consist of hall bars with a channel thickness of $10\ \mu m$ with variating orientation. The orientation shifts going form left to right with 0° , 30° , 60° , 90° , 120° and 150° . The non indexed hall bar series has a channel thickness of $30\ \mu m$ with a changing - going from left to right, of: HB1= 0° , HB2= 30° , HB3= 60° , HB4= 150° , HB5= 120° and HB6= 90° . The change in orientation is to see if there is a change in the conductance relative to the orientation on the chip.

Appendix C: Etch test

In this study, the same procedure is used as in F. Triet et al[8]. However the etching turned out to be an issue. This led to several etch tests on both LaMnO_3 LMO and LSM. The etchant which is used, is the same as in Trier's paper: A 2:2:35 $\text{KI}(3\text{M}) : \text{HCl}(35\%) : \text{H}_2\text{O}$ acid solution. Furthermore it was expected for LMO and LSM to have the same conditions when etching. The first samples have been deposited with LMO. It was believed LMO and LSM had the same circumstances in the etching procedure. Therefore two samples were etched for 30 and 60 seconds, respectively. This is seen on figure 6. The etch seems nice, however panel (c) and (d) shows another story, namely they didn't reach the STO substrate. This is due to it was expected for the LMO film to have a height of 45 nm and no terraces were observed.

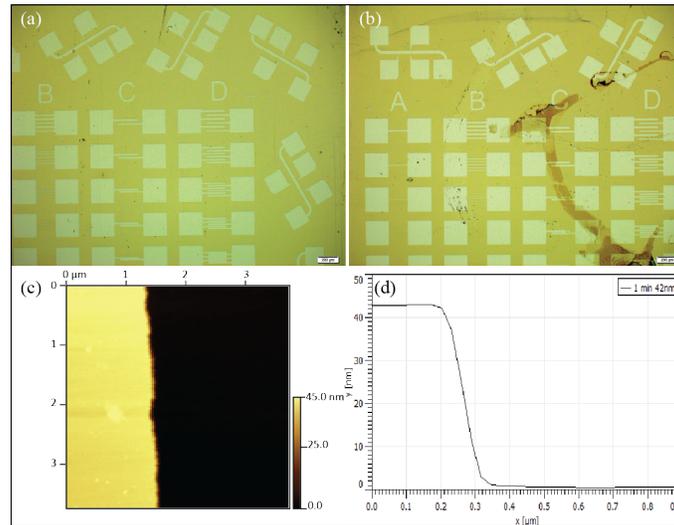


Figure 6. (a) shows an optical image after 30 seconds of etching, and (b) shows an optical image after 60 seconds of etching. The etch seems good at first, due to sharp edges, and only a little over-etched. However (c) and (d) indicate the etchant has not reached the STO substrate for the 60-second etch, meaning 30-second etch neither has.

Figure 6 shows on panel (a) and (b) that the etchant seemed good at first, however looking at (c) shows an AFM image of the etched sample, where the yellow color shows the LMO, and the black color shows the etched area. Seeing no terraces indicated the etchant has not reached the STO substrate, although (d) shows a height profile, showing the height from the etched area to the top of the non-etched LMO. It has a height of approximately 42 nm, which was expected for the top film to be. In order to make sure the etchant has etched through the LMO top-film terraces, this has been observed in the patterned area. This gave rise to making an etch test, testing for 2, 3, 4, and 5 minutes of etching. Figure 7 shows 4 vertical lines in which have etched for 2, 3, 4, and 5 minutes, going from left to right.

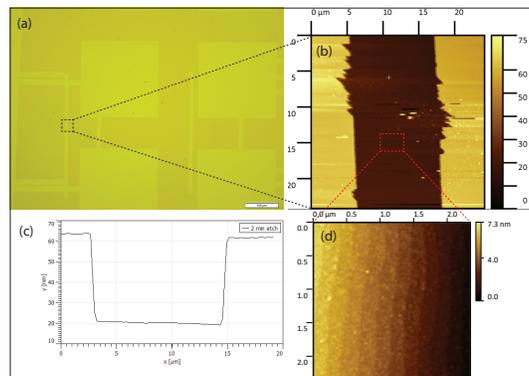


Figure 7. (a) shows an optical image after the different etching times. The four vertical lines going from left to right represent different etch times: 2 minutes, 3 minutes, 4 minutes and 5 minutes. (b), (c) and (d) show the 2-minute etch has reached the STO substrate due to terraces and a reasonable height profile corresponding to the expected height.

The etch lines were made by spinning resist on the sample, exposure and development followed by the different etching times. This were done four times in order to make the 4 lines. Figure 7 shows clear signs of a STO substrate. Panel (d) shows terraces after 2 minutes of eatching, meaning there was no reason to check if 3, 4 and 5 minutes had terraces as well. Panel (a) shows an optical images of the etch lines after the 4 etch lines were made. However, the channel seem a bit rough as seen in panel (b), but for this larger scale devices it didn't matter too much, even tough a sharper etch would be preferred. Panel (c) shows the height of the channel. At the time of the etch testing, it was belived that LMO and LSM had the same etching rates, which ment 2 minutes seemed to be the right time. However LMO and LSM is not the same. figure 8 shows how the etching look after 2 minutes. This leads to another etch test but on LSM this time. The etching times had to be below 2 minutes, which led to trying out 30s, 60s and 90s.

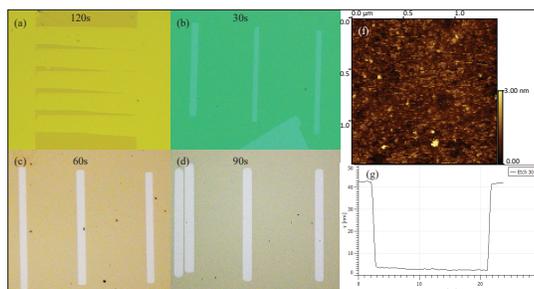


Figure 8. (a) is after 2 minutes etch. What seemed to work on LMO does not work on LSM. Therefore a 90 seconds, 60 seconds and 30 seconds etch test has been executed as seen on (b), (c) and (d). (e) and (f) shows an AFM images and a heigth profile form the top of the LMO film to the STO substrate respectively, indicating the etch should have reached the buttom, however the AFM images shows no terreces.

The lack of terraces indicates the STO substrate is covered by residue LSM, which still means it's not possible to deposit LAO to form the conducting interface. It was suggested to make a new etchant, which was carried out. The new etchant followed the same recipe as the previous one, the results are seen on figure 9.

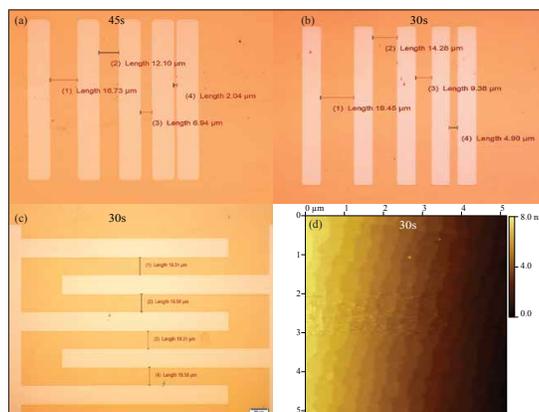


Figure 9. Optical images of an etch test. (a) is after development, where the lines have only expanded a little. (b) is after 1 minute etching, where the lines have expanded greatly, telling that 30 seconds appears to be the best etching time in the test.

While it has not over etched much. The etchant has reached the STO substrate after 30 second etch. This concludes, the right etching time for LSM is 30 second, while the right etching time for LMO is 2 minutes. The etching process for LSM is very time dependend. This means, if etched too long the patterning will expand, and the pattern will not be well defined. This not the case for LMO, which is not as time dependend as LSM. This makes it less complicated to control the etching process. However, this test does not tell if the different topfilm have an influence on the transport measurements. The test also concludes the etchant can behave somewhat randomly. Therefore the two etchants, which should have been identical was not. Despite this, study lead to a recipe for patterning process:

Preparing the etchant

- Prepare a **2:2:35 KI(3M):HCl(35%):H₂O** by pouring 37 ml milli-Q water (or de-ionized water) H₂O in a conical flask.

- Solute 0.996 g KI_s in the H_2O . Use a magnetic stirrer (remember to clean the magnet) to solute the KI completely.
- When the KI is soluted pour 2 ml 35% HCl in the solution.

Exposure and development

- Clean the substrate with acetone and IPA, preferably with a spray flask, then dry the substrate with N_2 gas. Make sure the substrate is clean by looking at it in the optical microscope. If not, clean with acetone and IPA again.
- Place the substrate on the spincoater and turn on the vacuum. Close the lid and pour AZ1505 photoresist on the substrate with a micropipette. Set the spin coater to 4000 rpm for 45 seconds with a 5 seconds ramp time.
- Bake the substrate for 2 minutes at $115^\circ C$.
- Look in the optical microscope to see if the resist is good.
- Place the substrate in the Heidelberg μpg 501. Note the direction of writing if necessary. Use pneumatic focus (due to transparent sample) to locate the center of the substrate.
- Pour MF321 developer liquid in a plastic cup, and milli-Q water (or de-ionized-water) H_2O in another. Immerse the substrate in MF321 for 1 minute followed by immersing directly in milli-Q water for 1 minute. Dry the substrate with N_2 gas.

Wet etching

- Pour the etchant in a glass beaker, have a bottle with IPA on the side ready to spray (place some wipes on the table to soak the IPA) and pour NMP in a plastic beaker (the plastic beaker should have a lid).
- Immerse the substrate in the etchant and stir it slowly around with the tweezers for 30 seconds. Remove the substrate from the acid and spray with IPA followed by immersing in NMP. Let it be for 5 - 10 minutes at $80^\circ C$. Immerse in acetone then IPA for 1 minute each. Dry the substrate with N_2 gas.
- Plasma ash the substrate for 2 minutes to remove residual organic matter.

Appendix D: Measurement equipment setup

For the measurements, the setup is as follows. Figure 10 show a schematic of the setup for room temperature measurements, while 11 shows the setup for low temperature measurements. Both the low temperature and room temperature measurements are not connected directly to the sample, but to a breakout box, which is connects to the sample.

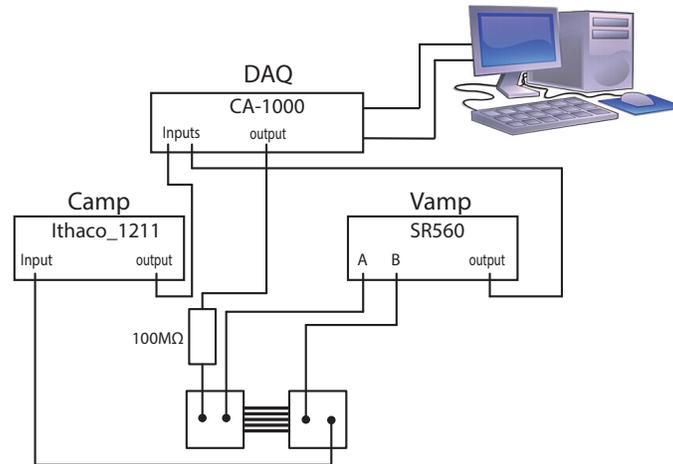


Figure 10. Schematic of room temperature measurement setup. Where the Vamp is a voltage amplifier, the DAQ (data acquisition) device, which is inside a computer. Is connected to a connector accessory, which is sketched as the DAQ in the schematic. The Camp is a current amplifier, and the sample is connected to a breakout box, which is connected to the sample.

The measurement setup for room temperature is shown as a schematic in figure 10. The purpose of the data acquisition (DAQ) is to sample the real world measured physical signal and convert them into a digital number. This is done by a analog - digital conveter (DAC) inside the DAQ. The DAQ is inside a computer, and is connected to a connector accessory (CA) of the model CA-1000 by National Instruments. The source of the sample is connected directly to the CA with a $100M\Omega$ resistance. The large resistance is to make the current constant throughout the sample. The drain is connected to a current amplifier of model Ithaco1211 by DL instruments, which is connected to the DAQ. As well as amplify the signal from the sample. To make measurable, the current amplifier converts the current into voltage. It is a 4 terminal measurement, meaning a voltage amplifier of model SR560 by Stanford Research is connected to the sample as well. The voltage amplifier is set to B-A, meaning the measured value is the voltage drop across the sample. From here is is possible to calculate the resistance. The voltage amplifier is connected to the DAQ aswell.

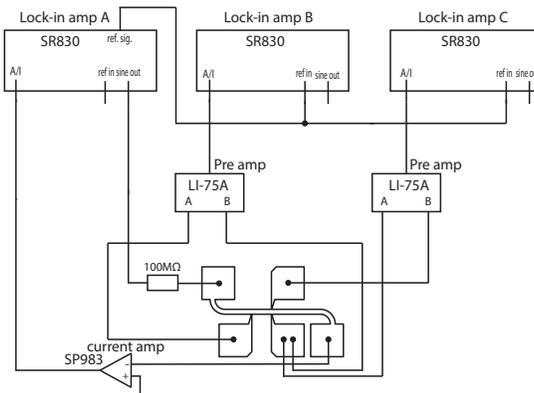


Figure 11. Schematic of low temperature setup.

Figure 11 shows the setup for the low temperature measurements. In order to measure the signal lock-in amplifiers are needed. Three lock-in amplifiers of the model SR838 by Stanford Research are used to measure 1 hall bar. One lock-in is needed for the source drain connection, one is needed for the longitudinal connection, and one is needed for

the transverse connection. The signal from the sample is very small, and can easily be buried in the noise. The carrier wave is chosen by making a frequency test, to find the signal with the lowest amount of noise, but before the signal begins to drop. The lock-in amplifiers are connected to each other to have the same reference frequency. Lock-in amp A is directly connected to the sample with a $100\text{ M}\Omega$ resistance as in the room temperature measurements. Again this is to keep a constant current through the sample. The drain is connected to a current amp of the model SP983 by University of Basel, which amplifies the signal. The signal then goes back in to lock-in A. The longitudinal voltage is measured using lock-in amp B. The amplifier is connected to a pre amp of the model LI-75A by NF corporation, which is connected to the sample as sketched in figure 11. Lock-in amp C is connected to a pre amp as well, but is used to measure the transverse voltage. The lock-in amplifiers are connected to a computer from which the data can be processed digitally.

Appendix E: Various figures

	Series	S1 - resist 001 (k Ω)	S2 - LSM 001 (k Ω)	S3 - LSM 111 (k Ω)
Channels	B1 - 20 μm	20780.88	18445.73	102399.01
	B2 - 10 μm	34244.04	35707.08	174006.91
	B3 - 5 μm	60454.21	64525.94	266355.92
	B4 - 2 μm	135457.22	176497.94	472410.97
	B5 - 1 μm	265407.35	BMT	673721.87
	B6 - 0.5 μm	BMT	BMT	BMT
Leakage	C1 - 20 μm	BMT	BMT	BMT
	C2 - 10 μm	BMT	BMT	BMT
	C3 - 5 μm	BMT	BMT	BMT
	C4 - 2 μm	BMT	BMT	587435.42
	C5 - 1 μm	4270479.61	92717.67	453151.1
	BMT =	Below measurement threshold		

Figure 12. Table of room temperature measurements, showing S1 and S3 are conductive down to $1\mu\text{m}$ and S2 is conductive down to $2\mu\text{m}$. The leak current measurements shows the leakage at $1\mu\text{m}$ for S1 and S2, while S3 begins to leak at $2\mu\text{m}$.

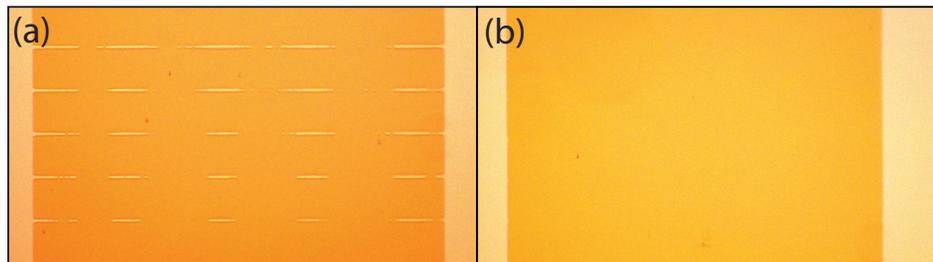


Figure 13. Optical images of sample 2 showing the B series. Panel (a) shows the device with a channel thickness of $1\mu\text{m}$. It shows a dotted behavior, which is properly caused by a failure in the fabrication process, compared to the other sample with a similar thickness which didn't show this behavior. Panel (b) shows the last device which should enclose a $0.5\mu\text{m}$ thick channel. The optical images didn't show sign of this channel.

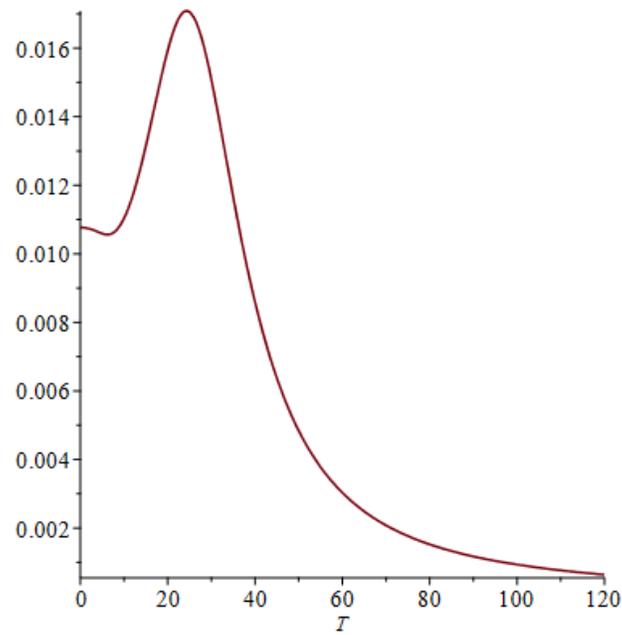


Figure 14. Mathematical model plotted with the parameter from D. Fuchs et al. paper. The model looks very similar with the cooldown data from this study.

Device	R (Ω)	Orientation (deg)
HB1	137722,01	0
HB2	136641,33	30
HB3	137972,67	60
HB4	108287,9	150
HB5	107946,24	120
HB6	108370,72	90

Figure 15. Room temperature measurements of the hall bars with a channel thickness of $30 \mu\text{m}$, showing no clear consistency in the resistance with respect to orientation.