University of Copenhagen

Niels Bohr Institute

Center for Quantum Devices

Fabrication of Nanowire-based Majorana Devices

Author:
Veronica S. Kirsebom
jtf385

Supervisor:
Prof. Charles M. Marcus
Doc. Deng Mingtang

June 10, 2015

1 Acknowledgments

When I became part of Center for Quantum Devices one year ago I had never heard about superconductors, quasi particles and density of states. In fact I did not even know that there was a distinction between the field of condense matter physics and the field of particle physics. If it had not been for Morten Kjærgaard I would probably still not know and even worse I would not have achieved all the experience, insight and confidence, I have today. I do not think you know how grateful I am that you gave me this opportunity! I also want to thank my "Qdev parent" Mingtang Deng, who has been teaching me all about fabrication and the basic physics behind the devices we are fabricating. Thank you Shivendra Upadhyay for teaching me how to use different machines and for always being so passionate and nice. Whenever fabrication failures occurred I found a lot of comfort in talking and laughing with Nina Rasmussen, Charlotte Bøttcher and Joachim Sestoft. Thank you for knowing exactly how frustrating fabrication can be. Also, thank you Nina for inputs, support and a lot of sugar during the last intense days of writing! Thank you Oli, you always know how to solve my problems! Also, thank you Jess Martin, Katrin Hjorth and Tina Bang-Christensen for always being extremely helpful and liable. I also want to thank my very good friend Naya Sophie Rye for creating a relaxed and quite space, where I can always be myself. And finally I want to thank Charles M. Marcus for including me as a researcher in the Majorana group. It has been extremely exciting to be part of this research and I have learned so much, which I could never had learned from normal university courses. Thank you everyone!

Abstract

In this thesis I present my work on fabricating nanowire-based Majorana devices. In particular focus has been on a device in which energy splitting of nearby Majorana zero modes could be observed. Unfortunately the fabrication of the devices did not turn out successful due to system and self-inflicted fabrication failures. However, devices presented in this thesis are still highly relevant in MF research and it is therefore worth making an effort into achieving these devices. Fabrication is discussed and a proposals of how to proceed is made.

Contents

2 Motivation

Majorana fermions (MFs) are studied intensively in the research field of quantum computation.[4] These particles are fermions, which are their own antiparticles. In condensed matter physics they are believed to exist as quasi-particle excitations obeying Non-Abelian exchange statistics, meaning that exchanging two MFs is an operation which in general does not commute.[8] Researchers believe that the Non-Abelian statistics of MFs can be used in the construction of a so-called topological qubit, which should in principle be protected against decoherence, traditionally a thing which has been hampering the realization of quantum computation. [4] [1] Several condense matter systems have been proposed as candidates for hosting MFs. One of these is a topological superconductor (TS), which can be engineered in a one dimensional (1D) semiconductor wire possessing strong spin-orbit coupling and a large g-factor. Conventional superconductivity is induced in the wire and a magnetic field is applied. In the TS-phase a zero energy MF bound state will be created and the detection of it is usually associated with a zero bias peak (ZBP) appearing in the center of a superconducting gap in tunneling experiments.[8] The first reported measurement of a ZBP in a hybrid superconductor-semiconductor nanowire device came from researchers at Delft University.[10] Shortly after more reports of ZBPs followed. The induced superconducting gap in these measurements were soft, meaning that the zero bias peak was not isolated inside the gap as it should to become relevant in quantum computations.[10] [2][8] Lately, researchers at Center for Quantum devices (Qdev) at University of Copenhagen have measured a hard induced superconducting gap in a InAs nanowire with a epitaxial Aluminum shell.[5] Another recent (and unpublished) measurement at (Qdev) shows a ZBP inside a hard induced superconducting gap, making it possible to proceed the research toward a topological qubit based on MFs.

The focus of this project has been to achieve a better understanding of the theory behind MF zero modes in a 1D system by designing and fabricating hybrid semiconductor/superconductor 1D nanowire devices in which MF zero energy modes can be detected. In particular the focus has been on devices in which the energy splitting of nearby MF energy zero modes could be observed. The ultimate goal is to achieve a working device and measure the energy splitting by using gates to control the position of MFs.

This report starts out with a short introduction to the theory of MFs in solid state physics. Hereafter my experimental work will be presented. Design of devices and fabrication procedures used will be explained. Finally, results and discussion will be provided ending the report with a conclusion and outlook.

3 Theory

In the following chapter I will give a short introduction to the theory of MFs in solid state physics. The hamiltonian for a 1D spinless p-wave superconductor will be presented together with a recipe for how to engineer such a system. A simple tunneling setup for detecting MFs zero energy modes will also be explained.

3.1 MFs in solid state physics

MFs are as the name suggests fermions, but also they are their own antiparticles. In solid state physics this can be expressed in terms of second quantization annihilation γ_i and creation $\gamma_i^\dagger$ operators as:

$$\gamma_i = \gamma_i^\dagger \tag{1}$$

Expressed in words, removing a MF in state i is equal to creating a MF in state i and vice versa.

In solid state physics the antiparticle of an electron is a hole and one could therefore imagine a MF being a quasi particle of equal superposition of electron and hole. A natural place to look for this kind of quasi particle is in a superconducting system where so-called Boguliubov quasi particle excitations

consisting of both electron and hole components occur. The annihilation operator of a Boguliubov quasi particle in a s-wave superconductor is:

$$b = uc_{\uparrow}^{\dagger} + vc_{\downarrow} \tag{2}$$

where $c_{\uparrow}^{\dagger}$ is the creation operator for a fermion of spin up and $c_{\downarrow}$ is the annihilation operator for a fermion of spin down. The characteristic of a s-wave superconductor is that the electrons in the cooper pairs have opposite spin direction. Obviously $b \neq b^{\dagger}$, so the Boguliubov quasi particle in a s-wave superconductor is not a MF. However if we change the expression into:

$$\gamma = uc_{\sigma}^{\dagger} + u^{*}c_{\sigma} \tag{3}$$

where σ is the spin projection, we get $\gamma = \gamma^{\dagger}$. The quasi particle now have equal electron and hole components and the fermion operators have same spin directions. The quasi particle satisfies being a fermion and its own antiparticle, and therefore it is a MF. The question now is if a solid state system supporting this quasi particle exists? One obvious candidate would be a superconductor in which pairing between electrons of same spin-direction happened, this is a so-called p-wave superconductor. Unfortunately such a superconducting phase has not yet been observed experimentally. However, it is believed that a so-called spinless p-wave superconductor in 1D, supporting spatially separated MFs, can be engineered.[8]

3.2 MFs in 1D

In this section the Hamiltonian describing a spinless p-wave superconducting phase will be presented and it will become clear why this system supports spatially separated MFs. We consider a 1D chain consisting of N fermion operators, between which the pairing mechanism is p-wave superconducting. The Hamiltonian describing this system was first introduced by Alexei Kitaev and it takes the form:

$$H = -\mu \sum_{i=1}^{N} c_i^{\dagger} c_i - \sum_{i=1}^{N-1} (tc_i^{\dagger} c_{i+1} + \Delta c_i c_{i+1} + tc_{i+1}^{\dagger} c_i + \Delta^{*} c_{i+1}^{\dagger} c_i^{\dagger}) \tag{4}$$

where μ is the chemical potential, c_i is the fermion annihilation operator at site i, Δ is the superconducting gap and t is the hopping constant. The two latter quantities are assumed to be the same for all sites. The hamiltonian only allows one spin direction of the electrons, and they are therefore effectively spinless. MFs operators are obtained by splitting a fermion into its real and imaginary part:

$$c_i = \frac{1}{2}(\gamma_{i,1} + i\gamma_{i,2}) \tag{5}$$

$$c_i^{\dagger} = \frac{1}{2}(\gamma_{i,1} - i\gamma_{i,2}) \tag{6}$$

That $\gamma_{i,1}$ and $\gamma_{i,2}$ are in fact MF operators can be realized by inverting equation 5 and 6.

$$\gamma_{i,1} = c_i + c_i^{\dagger} \tag{7}$$

$$\gamma_{i,2} = i(c_i^{\dagger} - c_i) \tag{8}$$

satisfying $\gamma^{\dagger} = \gamma$. Using the anti commutation relations for fermion operators, one can show that MFs also satisfy: $\{\gamma_i, \gamma_j\} = 2\delta_{i,j}$. Making it clear that MFs do not obey Pauli principle, since $\gamma_i^2 = 1$. Acting twice with a MF operator will get us back to the same state as we started with. On fig. 1[1] Kitave's 1D p-wave superconducting chain is illustrated. In the upper panel a fermion operator on each site i is split into two MF operators $\gamma_{i,1}$ and $\gamma_{i,2}$. [8]

[1]This figure is taken from the article: "Introduction to topological superconductivity and Majorana fermions" by Martin Leijnse and Karsten Flensberg

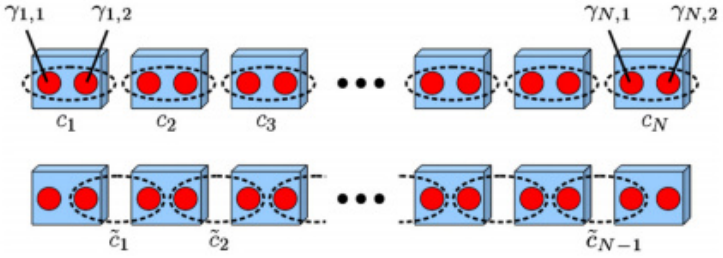


Figure 1: Model of Kitaev's 1D chain associated with a spinless p-wave superconductor. Upper panel: At each site i a fermion operator c_i is split into two MF operators $\gamma_{i,1}$ and $\gamma_{i,2}$. Lower panel: for $\mu = 0$ and $t = \Delta$ the Hamiltonian of a spinless p-wave superconductor has eigenstates on the form $\tilde{c}_i$, which combines MF operators on different sites and thereby leaving the two MF end-states unpaired. Combining these two isolated states gives a highly non-local zero energy fermion state $c_{\tilde{M}}$.

We want to express the hamiltonian in equation (4) in terms of MFs operators. The problem is simplified by setting $\Delta = t$ and $\mu = 0$. Inserting equation (5) and (6).

$$H = -it \sum_{i=1}^{N-1} \gamma_{i,2}\gamma_{i+1,1} \tag{9}$$

This is the diagonalized Hamiltonian, which can more easily be seen, if we represent it in terms of a new fermion operators defined as $\tilde{c}_i = \frac{1}{2}(\gamma_{i+1,1} + i\gamma_{i,2})$. The situation is illustrated in lower panel of fig.1. The new fermion operators consists of a MF from neighboring sites. The Hamilton becomes:

$$H = 2t \sum_{i=1}^{N-1} \tilde{c}_i^{\dagger}\tilde{c}_i \tag{10}$$

From equation (9) we see that the states $\gamma_{1,1}$ and $\gamma_{N,2}$, which are localized at the ends of the chain, are missing from the expression. We can describe this non-local state as:

$$c_{\tilde{M}} = \frac{1}{2}(\gamma_{N,2} + i\gamma_{1,1}) \tag{11}$$

Since $c_{\tilde{M}}$ is absent from the Hamiltonian, occupying this state costs zero energy. The ground state of the spinless p-wave superconductor given by equation (4) is therefore two fold degenerate, corresponding to having in total even or odd number of electrons in the superconductor. It can be shown that for $\mu \neq 0$ and $t \neq \Delta$ MFs remain at the ends of the chain as long as the chemical potential is within the superconducting gap. Furthermore MFs will also occur in the transition points between TS and non-TS regions. In reality MFs are not completely localized at the ends of a wire. Their wavefunctions will decay exponentially away from the edges, but as long as the wavefunctions do not overlap the MFs remain at zero energy.[8] It turns out that a degenerate ground state separated from excited states by a gap is a crucial ingredient for non-Abelian statistics. By slowly exchanging the position of MFs one can bring the system from one ground state to another. These two ground states serve as a topologically protected qubit states. The idea is to exploit their Non-Abelian statistics to make quantum processing. The simplest setup in which exchanging of MFs can take place is in a T-junction device made out of two wires perpendicular to each other. Here MFs can be exchanged without colliding, we call this exchange operations braiding. The investigation of the interaction between MFs, this is if the combine into an electron or hole, when they get close enough to each other, is referred to as the fusion rules of MFs.[1]

3.3 Realizing MFs in 1D

In the following a recipe of how to engineer a spinless p-wave superconductor will be presented and explained. The necessary ingredients are:

1. 1D wire
2. Strong spin-orbit interaction
3. Large g-factor and an external magnetic field
4. Induced superconductivity

The setup is illustrated in fig. 2*a*. A 1D wire is placed along the x-axis resulting in a momentum, $\mathbf{k}_x = \pm k_x \hat{\mathbf{x}}$. A s-wave superconductor is placed on the side of the wire. We choose the the electric field to be $\mathbf{E} = -E\hat{\mathbf{z}}$ resulting in a spin-orbit field $\mathbf{B_{SO}} = \pm B_{SO}\hat{\mathbf{y}}$, and the external field is chosen to be $\mathbf{B_z} = B_z\hat{\mathbf{x}}$.

1. In an idealized 1D wire, for which quantization along the wire can be ignored, there is one single subband, as illustrated in fig. 2*b*. We assume there is no spin-orbit interaction now. The dispersion relation for electrons in the wire is parabolic, that is $\epsilon(k_x) = \frac{\hbar^2 k_x^2}{2m*}$. The subband is spin-degenerate. However, in reality the wire will only be quasi 1D, because it has a finite diameter. The electrons can therefore have momentum transverse the wire direction leading to more spin degenerate subbands. As long as the diameter of the wire is small compared with the length of the wire, we can assume that the 1D subbands are well separated on the important energy scales, making it possible to achieve an isolated pair of MFs in the wire.

2. A strong spin-orbit interaction is introduced in the wire resulting in an effective spin-orbit field $\mathbf{B}_{SO} \propto \mathbf{k}_x \times \mathbf{E}$. The situation is illustrated in fig.2*c*. The electric field in an experimental setup, $\mathbf{E}$, is not known, but from the cross product we know that $\mathbf{B}_{SO}$ must be perpendicular to the wire. We choose $\mathbf{B_{SO}} = \pm B_{SO}\hat{\mathbf{y}}$, which is illustrated on fig.2*c* by orange arrows. The spins are illustrated with red and blue arrows. $\mathbf{B}_{SO}$ couples to the spins forcing them to be aligned parallel or anti parallel to $\mathbf{B}_{SO}$. This results in a energy change of $\epsilon_{SO} \propto -\mathbf{s} \cdot \mathbf{B_{SO}}$, where $\mathbf{s}$ is the spin. This will lift the spin-degeneracy except at $\mathbf{k}_x = 0$.

3. An external magnetic field $\mathbf{B_z} = B_z\hat{\mathbf{x}} \perp \mathbf{B_{SO}}$ is introduced, illustrated on fig.2*d*, as green arrows. The total magnetic field $\mathbf{B_{TOT}} = \mathbf{B_z} + \mathbf{B_{SO}}$, illustrated by black arrows, aligns the spins parallel or anti-parallel to it and thereby lowers and increases their energies respectively. The spin degeneracy at $\mathbf{k}_x = 0$ is lifted by $\mathbf{B_z}$ creating a Zeeman gap of $2E_z = g\mu_B B_z$, where g is the Lande g-factor and μ_B is the Bohr magnetron. Each of the two new subbands holds only one spin projection, which is indicated by the gray arrows, although the total spin direction is different for each momentum in the band. The region inside the gap where only one spin projection is present is called the spinless regime. A large g-factor is favored since a small B_z will induce a large Zeeman splitting.

4. Placing a s-wave superconductor in close contact with the wire results in induced superconductivity in the wire, illustrated on fig.2. This phenomena is called superconducting proximity effect. How well the superconductor proximitizes the wire depends on the cleanses of the interface between the two materials, their lattice constants and the coherence length of the superconductor. The induced superconductivity results in a induced gap opening of $2\Delta^*$ at the Fermi energy and the Zeeman gap is also modified. For $\Delta^* > 0$ and $E_z = 0$ we have a normal s-wave superconductor. As E_z is increased to $E_z = \sqrt{\Delta^{*2} + \mu^2}$ the gap at $\mathbf{k}_x = 0$ closes and the wire enters the TS-phase. As E_z continues to increase the gap reopens and remains in TS-phase. The requirement for being in the TS phase is therefore $E_z > \sqrt{\Delta^{*2} + \mu^2}$. Without spin-orbit interaction each the two subbands would be spin polarized and it would therefore not be possible to induce

s-wave superconductivity, in which electrons of opposite spin direction are paired. Spin-orbit is therefor crucial to induce superconductivity in the wire.[2] [9]

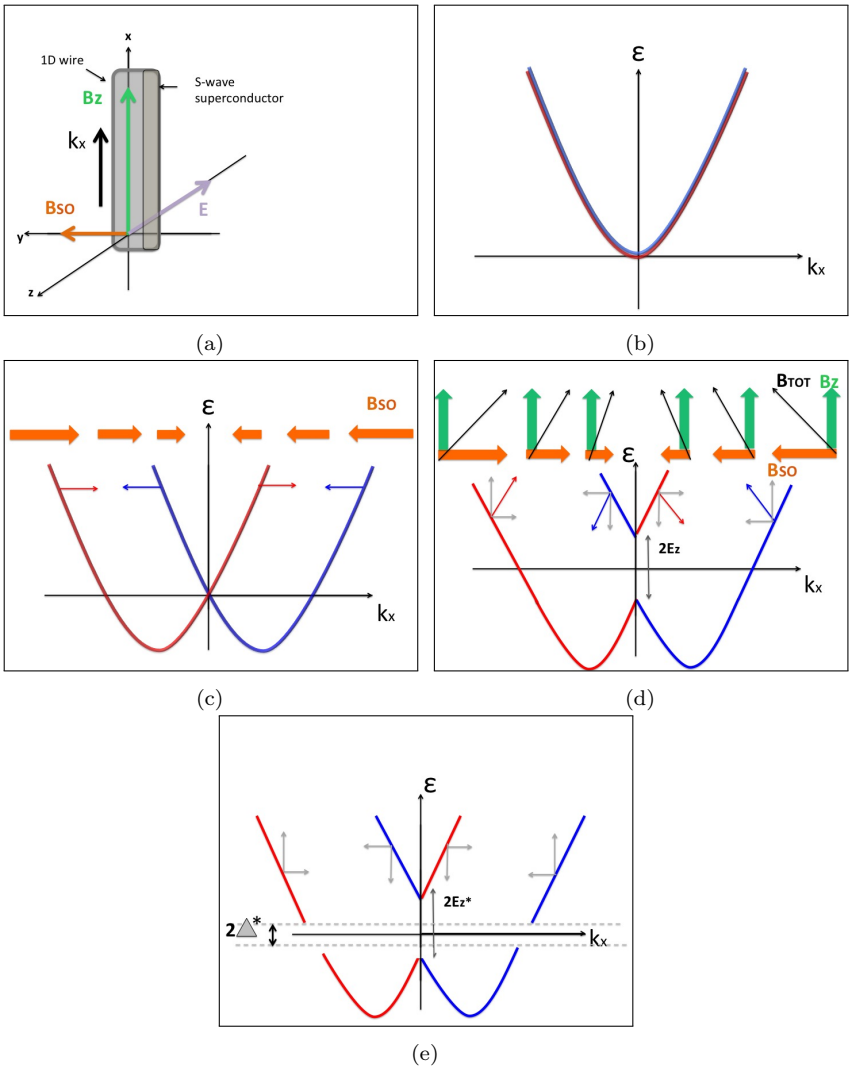


Figure 2: Engineering of a 1D spin-less p-wave superconductor (Topological superconductor). a) A 1D wire is placed along the x-axis. The momentum, $\mathbf{k}_x = \pm k_x \hat{\mathbf{x}}$. A s-wave superconductor is placed on the side of the wire. The electric field is $\mathbf{E} = -E\hat{\mathbf{z}}$, the spin-orbit field is $\mathbf{B_{SO}} = \pm B_{SO}\hat{\mathbf{y}}$ and the external field is $\mathbf{B_z} = B_z\hat{\mathbf{x}}$. b)Energyband, $E(k_x)$, for an 1D wire. There is one single spin-degenerate subband with the dispersion relation $E(k_x) = \frac{\hbar^2 k_x^2}{2m}$. c) A spin-orbit field $\mathbf{B}_{SO} \propto \mathbf{k}_x \times \mathbf{E}$ splits the subband. The orange arrows illustrates $\mathbf{B}_{SO}$, which depends on $\mathbf{k}_x$. Red and blue arrow are Spin projection. d) Green arrow is $\mathbf{B}_z$ and the black arrows are the total field $\mathbf{B}_{TOT} = \mathbf{B}_z + \mathbf{B}_{SO}$. The total field aligns the spins either parallel, which lower their energy or anti-parallel increasing their energy, resulting in two mixed spin-bands separated by a Zeeman gap of $2E_z$. The grey arrows show the x and y projections of the spins. e) S-wave superconductivity induced a gap of $2\Delta^*$ at the fermi energy. The gray arrows indicate the effective spin direction of the two bands. For $\Delta^* > 0$ and $E_z = 0$ electrons of different spin projection can combine leading to s-wave superconductivity. For $E_z \geq \sqrt{\Delta^{*2} + \mu^2}$ the wire is in the TS-phase.

3.4 Measuring MFs

A simple tunneling experiment can be performed in order to detect MF zero bound states. The setup is illustrated on fig.3.

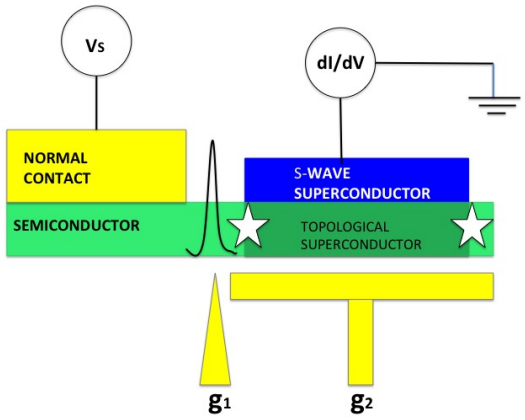


Figure 3: Tunneling experiment for the detection of MFs (white stars)

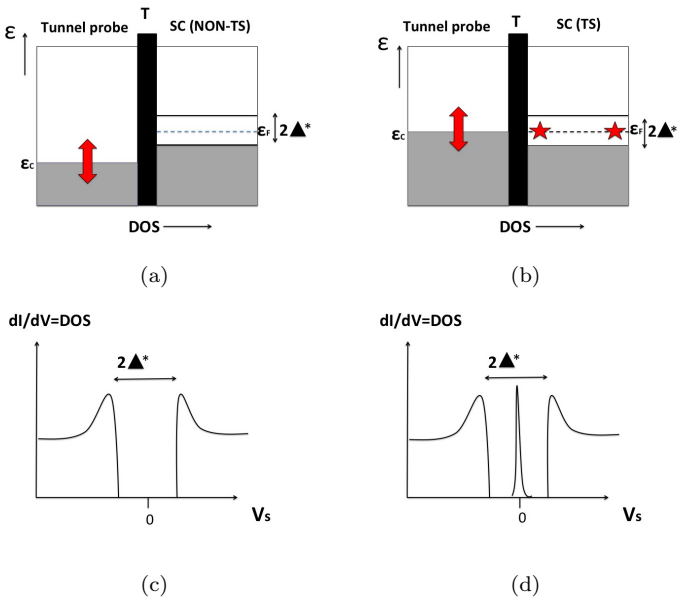


Figure 4: The DOS in the setup. a),b) DOS vs. energy for each side of the tunneling barrier (T). The tunneling probe to the left and the superconducting proximitized wire to the right. a) No MFs in the induced gap. b) MFs in the induced gap. c),d) Measurements of DOS for changing voltage of the tunneling probe. c) DOS for the proximitized wire, when there is no state inside the induced gap. d) DOS for the proximtized wire, when it supports MFs, resulting in a peak at zero bias (ZBP)

The semiconducting wire proximitized by a superconductor and exposed to a magnetic field constitutes the engineered spinless p-wave superconductor. The wire is contacted with a normal contact, to which a bias voltage, V_s, is applied. The superconductor is connected to a measurement channel and

then grounded. There are two gates, g_1 and g_2. By changing the voltage of g_2 the above segment can be brought in and out of the TS-phase. A tunnel barrier, T, which makes a clear distinction between the so-called tunneling probe and the proximitized wire, is created by applying a large negative voltage to g_1. The tunnel probe work as a conductor. It is the differential conductance, dI/dV, as function of V_s that we want to measure, since this will give us the electronic density of states (DOS) of the system ($dI/dV \propto$ DOS).

First we consider a case in which the wire is proximitized by the superconductor, but it is not in a TS-phase. Measuring dI/dV while continuously changing the V_s give us the DOS of the wire with an induced superconducting gap of $2\Delta^*$, as illustrated on fig. 4*c*. To understand why this is so, one can look at fig. 4*a*, which at the left hand side illustrates energy of the electrons in the tunneling probe as a function DOS. The energy of the conducting electrons is denoted ϵ_c, and this can be increased or decreased be varying V_s. On the right hand side we have a superconductor with a energy gap of $2\Delta^*$, in which no electronic states exist. In the middle of the gap is the fermi energy ϵ_F. If ϵ_c is below the gap, electrons from the superconductor can tunnel into the tunnel probe. If ϵ_c is inside the gap, no electrons can tunnel into the superconductor, and if ϵ_c is above the gap, electrons from the tunnel probe can tunnel into the superconductor. This picture is, however, not entirely accurate. Single electrons can tunnel into the gap by a process called Andreev reflection. Basically this is a mechanism in which an electron enters the superconductor and a hole is reflected, making it possible for the entering electron to combine with another electron into a cooper pair. The conductance associated with this process is so small compared with the conductance outside the gap, so fig.4*a* still holds. Assuming now that the TS-phase has been achieved resulting in MFs at each end of the TS-segment, illustrated as white stars on fig. 2*a*, the gap will no longer be empty, but contain a state in the center at the ϵ_F, corresponding to a pair of MFs, as illustrated on fig. 4*b* . Aligning ϵ_c with the MF state will lead to a resonant transmission process, meaning that an electron with zero energy will enter the superconductor occupying the MF-state and simultaneously a hole with the exact same energy will be reflected, resulting in a signal twice as large, with a conductance of $G = \frac{2e^2}{h}$ for a temperature of zero Kelvin. The DOS for this measurement is illustrated in fig. 4*d*. The state in the center of the induced superconducting gap is also referred to as a zero bias peak ZBP and this is the MF zero mode.

This is of course an idealized and simplified picture of how to achieve and measure MFs. The actual engineering of an spinless p-wave superconductor and the detection of MFs is much more complex, however this should give some intuition about MFs and the detection of them.[9]

4 Experimental Work

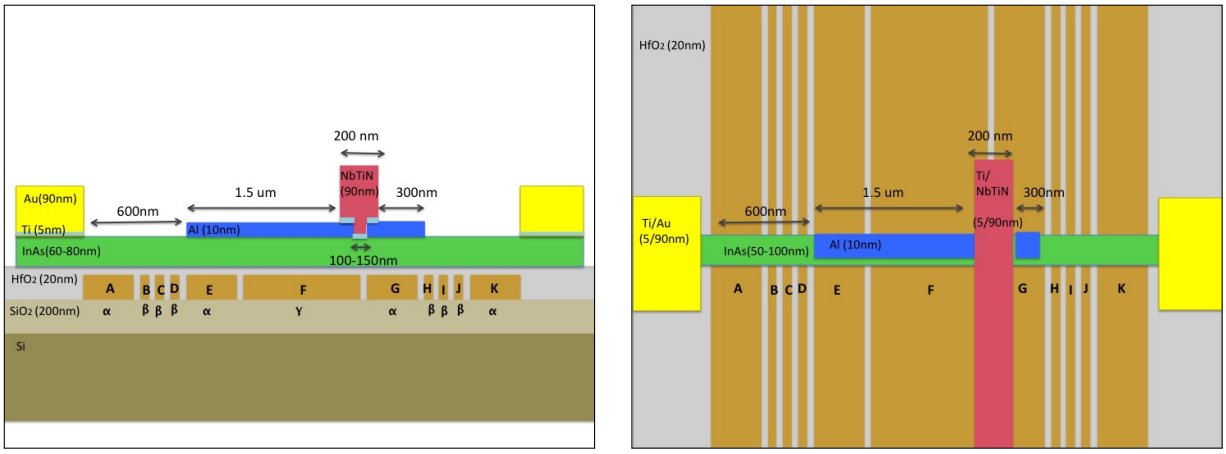
This experimental project consists of the development of two hybrid nanowire devices. The purpose of the first device (Dev1) is to investigate the interaction between two MFs across a junction similar to the one in the T-geometry and the interaction between two MFs on the same topological segment. The purpose of the second device (Dev2) is to investigate the possibility and advantage of using InAsSb/Al nano wires instead of InAs/Al. Device designs and fabrication procedures have gradually improved during the project, yielding multiple generations of devices. In this chapter designs and fabrication procedures associated with the latest fabricated generation of Dev1 and Dev2 are presented.

4.1 Dev1 Design

A schematic model of Dev1 is shown in fig. 5. This device consists of an InAs nanowire with an epitaxial grown Al-shell, which covers half of the wire [2] The thickness of the shell is less than 10 nm. The length of the nanowire is between 6-8 μm and the diameter is 60-80 nm. The wire is situated on top of bottom gates denoted with letters A-K. The Al-shell is etched away at both ends and at a short section above the boundary region between F and G. This section has a width of about 100-150

[2]Nanowires are grown by Qdev assistant professor Peter Krogstrup with molecular beam epitaxy (MBE)

nm, and we refer to it as the junction. The junction divides the wire into two segments. One part with an Al-shell of length 300 nm and another part with an Al-shell of length 1.5 μm. We refer to these as the short and long segment. Two normal contacts (Ti/Au) are placed at each end of the wire, leaving only the bare InAs nanowire above A-D and H-K. A superconducting contact (Ti/NbTiN) of width 200 nm is placed at the junction touching the Al-shell and the InAs nanowire. The thin layer of Ti serves as glue between the chip surface and Au and NbTiN respectively, since Ti is much more adhesive compared with the two other materials.



(a) (b)

Figure 5: Dev1: A InAs/Al nanowire is placed on top of bottom gates denoted A-K. The Al-shell is removed at both ends of the wire and contacted with (Ti:5 nm/Au:90 nm). A junction of width 100-150 nm splits up the Al-shell in a long and short segment of length 1.5 μm and 300 nm respectively.(Ti:5 nm/NbTiN:90 nm) of width 200 nm is placed at the junction. a) Cross section of Dev1. b) Dev1 seen from above.

The main purpose of Dev1 is to find out if the MFs at the junction will fuse and under which conditions they will do so. In connection with this we wish to investigate at which separation distance the wave function of two MFs at the same topological segment start to overlap.

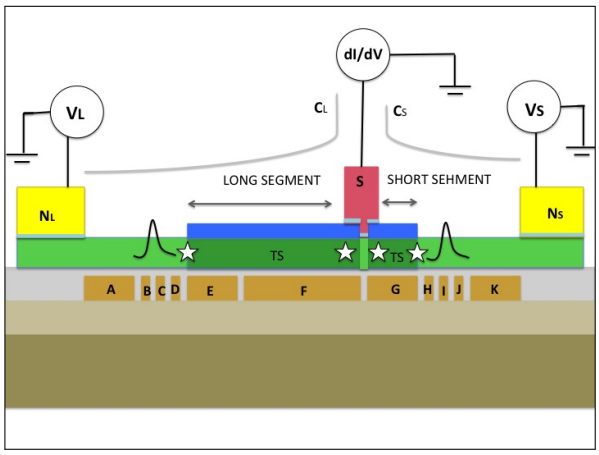
The TS-phase supporting MFs can be achieved in Dev1 by cooling it down below a temperature of 10-20 mK in a dilution refrigerator. At this temperature Al and NbTiN are superconducting. The superconducting proximity effect between Al and InAs is strong, leading to a hard induced superconducting gap in the InAs, [5] which has a strong spin-orbit interaction and g-factor. By applying a magnetic field and changing the gate voltages of E, F and G and thereby changing the chemical potential of the wire segment above, parts of the wire can be brought into and out of the TS-phase. The situation is illustrated on fig.(6a) where E and F have turned the long segment into the TS-phase and likewise has G turned the short segment into the TS-phase. The white stars illustrates MFs. A transition point cannot occur between E and F, because Al is a conductor and it will therefore equalize potential differences. This is why the Al-shell is not continuous between the long and short segment. We want to ensure that each segment independently can be turned into or out of the TS phase. An additional reason for having a junction is to achieve good ohmic contact to the wire.

The investigation is done through tunneling experiments. Dev1 has two channels for measurements, C_L and C_S, illustrated on fig.6a. A tunneling experiment at C_L and C_S is the measurement of the differential conductance, dI/dV, due to a voltage drop, V_L between N_L and S and V_S between N_S and S, respectively. The two tunnel barriers in front of the long and short segment are made by changing the gate voltages of B-D og H-J respectively. For instance applying a large negative voltage on C and a positive voltage on B and D creates a sharp barrier for electrons to tunnel through. By inversing the

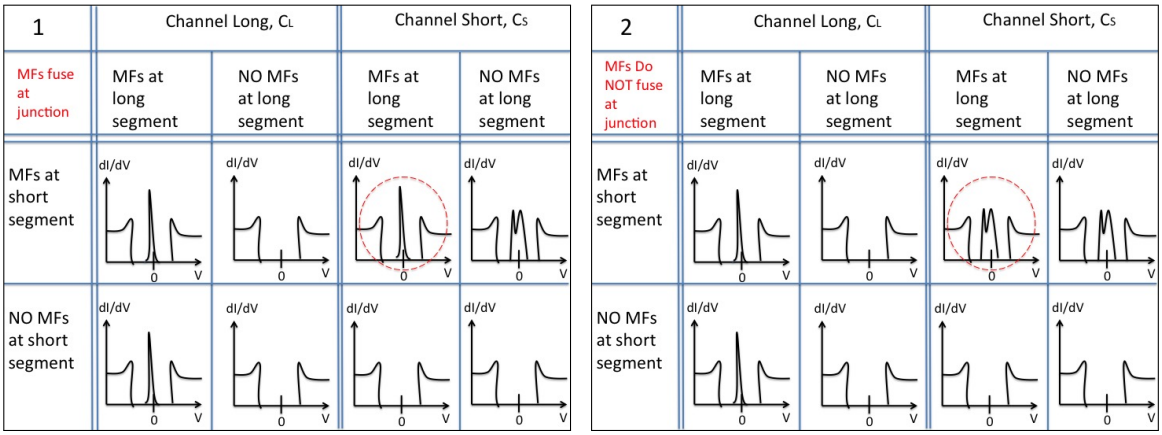
sign of the gate voltages we can create a quantum dot. The electron density in front of the two tunnel barriers is increased by applying a positive gate voltage to A and K. The idea is to measure dI/dV at C_L an C_S as function of V_L and V_S for the following four situations:

1. No MFs in long and in short segment
2. MFs in long, but not in short segment
3. No MFs in long, but MFs in short segment
4. MFs in long and short segment

The expected measurement for fusing and non-fusing MFs at the junction is shown in fig.6*b* and fig.6*c* respectively. The two schemes differ in the measurement of dI/dV at C_S when the long and short segment are both in the TS-phase, indicated with red circles. If the two MFs at the junction fuse, one peak at zero bias will appear inside the superconducting gap, but if the MFs do not fuse, the peak at zero bias will split into two states with finite energy. The relatively short distance between the two MFs at the short segment will make their wave functions overlap leading to a finite energy of the two MFs.



(a)

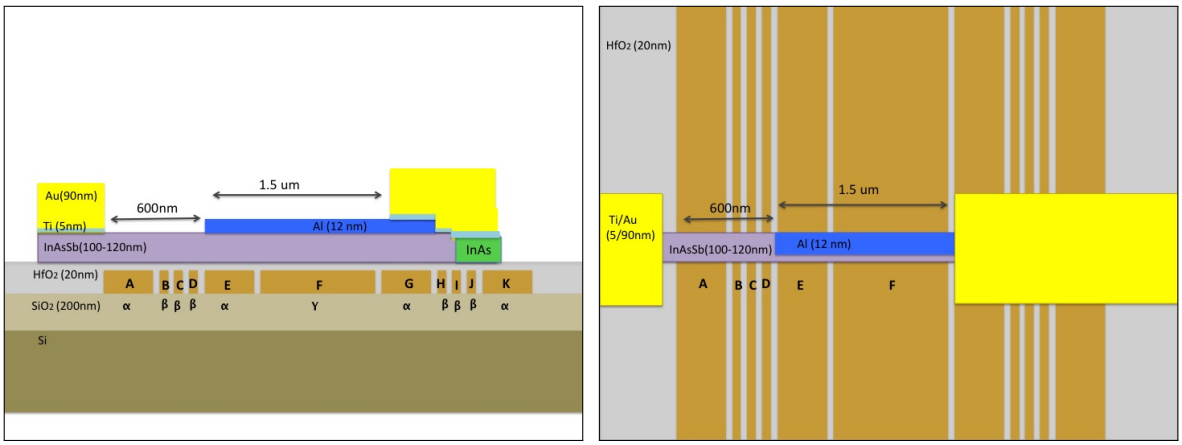


(b) (c)

Figure 6: Two-channel tunneling experiment on Dev1. a) dI/dV due to a voltage drop V_L and V_S between N_L and N_S respectively is measured at channel C_L and C_S. The long segment can be turned into the TS phase by E and F, while the short segment can be turned into the TS-phase by G, resulting in the creation of MFs illustrated as white stars. A sharp tunnel barrier is created by tuning on B, C and D and H, I and J and the electron density is increased by A and K. b) Outline for expected measurements of dI/dV at C_L and C_S as a function of the voltage of V_L og V_S for different combinations of having and not having MFs in the long and short segment. In this scheme the MFs at the junction fuse. c) Outline for same measurements as in b), but in this the MFs do not fuse at the junction

4.2 Dev2 Design

A schematic model of Dev2 is shown in fig. 7. Dev2 is a one-channel equivalent of Dev1 with an InAsSb wire. The thickness of the Al-shell is about 12 nm. The length of the nanowire is between 3.5 μm and the diameter is 100-120 nm. The first 700 nm of the wire consists of only InAs and this part will not be measured on, as illustrated on fig.7a. The Al-shell at the right end of the wire is removed to achieve good ohmic contact between the InAs and the normal contact (Ti/Au), which is placed on the Al-shell as well as the etched part. The Al-shell is also removed at the left end of the nanowire and a normal contact (Ti/Au) is placed so that only that section of the InAsSb wire above A-D is left exposed.



(a) (b)

Figure 7: Dev2: A InAsSb/Al nanowire is placed on top of several bottom gates denoted with letters A-K. At both ends of the wire Al is removed. At the right end of the wire a normal contact (Ti:5 nm/Au:90 nm) is placed on the Al-shell and the InAsSb. At the left end of the wire the normal contact (Ti:5 nm/Au:90 nm) is placed only on InAsSb. a) Cross section profile of Dev2. Notice that the right end of the wire consist of InAs. b) Dev2 seen from above.

The main purpose of Dev2 is to make basic characterizations of the InAsSb/Al nanowire in order to find out if it may be a better platform for MF research than the currently favored InAs/Al nanowire. The InAsSb/Al nanowire is expected to posses a higher spin-orbit coupling and larger g-factor than the InAs/Al nanowire.[11] If this is the case and the Al-shell induces a hard superconducting gap in the wire, InAsSb/Al will most likely replace InAs/Al in future devices.

An important measurement associated with Dev2 is to measure the hardness of the induced superconducting gap and eventually a ZBP inside this gap. This can be done through tunneling experiments where dI/dV, due to a voltage drop, V_S, between N_1 and N_2 is measured at channel C_1 as function of the voltage applied at gate A. the setup is illustrated on fig.8).

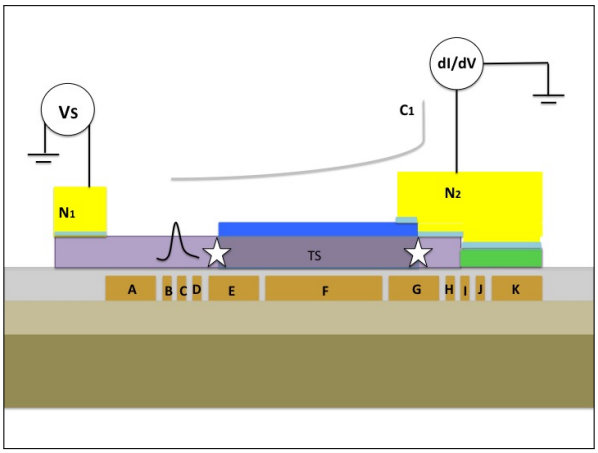


Figure 8: One-channel tunneling experiment on Dev2. At channel C_1 dI/dV due to a voltage drop V_S between N_1 and N_2 is measured. The wire segment situated above E and F is turned into the TS-phase, resulting in the creation of MFs illustrated as white stars. A sharp tunnel barrier is created by tuning on B, C and D and the electron density in front of the tunnel barrier is increased by applying a positive voltage to A.

4.3 Fabrication

The fabrication of Dev1 and Dev2 consists of several so-called lithographic steps: the first step is wire deposition and location, the second step is etching the Al-shell, the third (and also the last step for Dev1) is making Au-contacts and the fourth step (and final step for Dev2) is making NbTiN-contacts. Each lithographic step is a five or six step procedure:

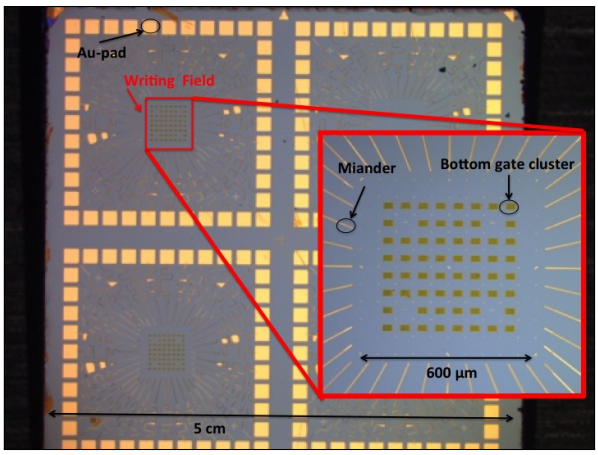
1. Spinning resist on a chip
2. Expose a pattern with Electron Beam Lithography (EBL)
3. Develop the pattern
4. Use pattern for either wire deposition, etching or metal deposition
5. Removing all resist in Lift-off
6. If necessary taking scanning electron microscope (SEM) images of the sample

Dev1 and Dev2 are fabricated in two separate quarters of the same chip and at the same time.

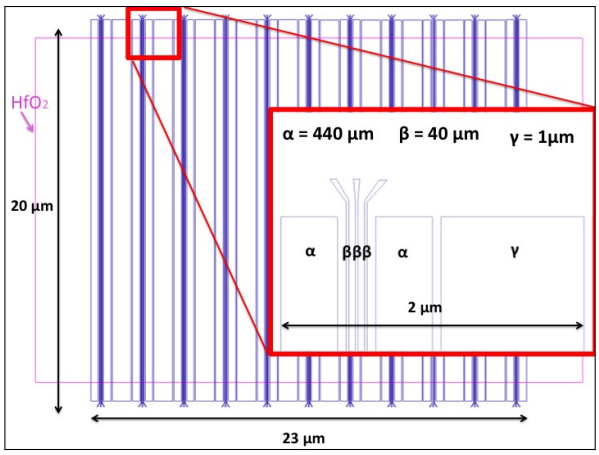
In the following chapter information about chip and bottom gates are provided and the fabrication procedures associated with the four lithographic steps are explained.

4.3.1 Chip and Bottom Gates

The chip serves as the platform for our devices. It is where we deposit the nanowires and electrically contact them via Au meanders and pads. The chip is made out of Si, but with a top layer of 200 nm SiO_2. The chip area is 0.5 cm x 0.5 cm and is divided into four squares, as illustrated on fig.9*a*. Each square has a central area of 600 μm x 600 μm, which is surrounded by 40 Au-meanders. It is in this center area, also called the writing field, that the nanowires are deposited and connected to the meanders.



(a) Chip and writing field



(b) Bottom gate cluster and repeating pattern

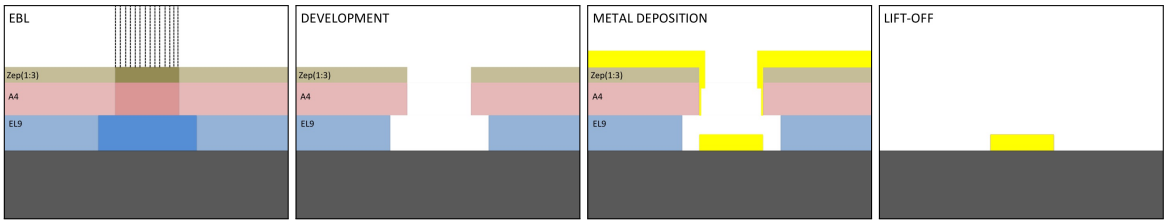
The first steps toward Dev1 and Dev2 is fabrication of bottom gates, which is done by bachelor student at Qdev Magnus Jørch Ravn. A writing field contains of 60 clusters of bottom gates, as shown in fig.9*a*. In fig.9*b* the design of a bottom gate cluster is shown. There exist three different sizes of bottom gates, namely: α=440 nm,β=40 nm and γ= 1 μm and they are organized in a repeated pattern of: $(\alpha, \beta, \beta, \beta, \alpha, \gamma)$. The separation distance between neighboring bottom gates is about 40 nm. The bottom gates are made out of (Ti:5 nm/Au:20 nm). A 20 nm thick layer of HfO_2 is deposited on top of the bottom gates by the method of Atomic layer deposition (ALD). The layer of HfO_2 covers the

entire bottom gate cluster except at the top and bottom, where they are electrically connected to the meanders and Au-pads.

The procedure of fabricating bottom gate chips is still relatively new in Qdev lab, so no devices with bottom gates have yet been measured in a dilution refrigerator. SEM-images show that the bottom gates are often shorted near the writing field edge. The bottom gate clusters in the center of the writing field have a yield of 9/10. Usually, the shortened bottom gates can be identified on SEM-images. The ohmic resistance between neighboring bottom gates has been measured at room temperature. About 8 x 4 neighboring bottom gates, which all looked fine on SEM-images, were measured, and out of these two were shortened.

4.3.2 Resist

Resist used in fabrication of Dev1 and Dev2 is electron sensitive. Exposing the resist to a focused electron beam changes its solubility, which enables the removal of exposed areas by applying a so called development solvent. A smooth layer of resist is achieved by spinning the chip at high rotation speed. If the nanowires are not fixed by contacts they might change position during spinning. After spinning this is checked in an optical microscope and usually the wires have not moved. However, small movements can be hard to detect in an optical microscope. In fabrication of Dev1 and Dev2 three different kind of resist are used: A4 or A6, El9 and Zep(1:3) [3]. Multiple layers of resist are used when depositing metal. The first layer is El9, the middle layer is A4 and the final layer is ZEP(1:3). The combination of A4 and El9 creates an undercut, as illustrated on fig.10. The undercut is created because EL9 is more sensitive toward EBL than A4. The undercut is about 50 nm, with the EBL settings used in this project. The purpose of undercut is to prevent the overall metal on the surface of the resist to connect with the contacts and electrodes and thereby damaging them when removing all resist in lift-off. The final layer is a protection layer against Ar-milling.



(a) EBL (b) Development (c) Metal deposition (d) Lift-Off

Figure 10: Undercut

4.3.3 Electron Beam Lithography (EBL)

Electron beam lithography is the procedure of drawing a pattern in resist by exposing it to a focused electron beam. In the fabrication of Dev1 and Dev2 the chosen settings in EBL enables one to draw very small features of a few nanometers. There will always be an alignment error. Depending on the purpose of the pattern different values of alignment errors are accepted. For instance the accepted error associated with wire windows is much greater than the one associated with contacts. In the latter case an error of more than 50 nm is not accepted, and it should be possible to achieve an error smaller than 30 nm.

[3]PMMA950k A4 or A6, MMA/AMM El9 [6] and ZEP520:A (1:3) [7].

4.3.4 Development

Development is the procedure of removing resist, which has been exposed in EBL. The chip is immersed into a solution, which resolves the exposed resist, leaving a pattern in the resist. This is always followed up by exposing the chip to oxygen asher. This procedure removes about 20 nm of the overall resist, making sure no residual resist is left inside the developed pattern.

4.3.5 Scanning Electron microscopy (SEM)

SEM is the procedure of taking high resolution images of a sample by scanning it with a focused electron beam. Interaction between beam-electrons and atoms in the sample produces signals, which can be detected and transformed into an image. The chip is always exposed to oxygen asher before loading into the SEM. The purpose is to remove any residual resist or dirt, which will charge up inside the SEM and disturb the image. In fabrication of Dev1 and Dev2 SEM-images are taken for two purposes. The first purpose is to locate nanowires, which can be used for devices. The size of the images is 50 μm x 50 μm containing one bottom gate cluster and one alignment mark. The images show which bottom gates that are definitely shortened and they can then be de-selected for devices. Furthermore one can identify that part of the InAsSb/Al nanowire, which consist of only InAs. The second purpose is to locate where the Al-shell has been etched. These images have a size of 8 μm x 8 μm and must be high resolution since the Al-shell is only about 10 nm thick.

Taking SEM-images of a device, which are supposed to be measured later on, is a balance between obtaining information about the device and damaging it. The interaction between beam-electrons and the atoms in the device may change the crystal structure and charge up the sample and thereby damage it. However, carbon seems to be a greater problem. Although there should be vacuum inside the SEM-machine, exposing a device, when taking images, will eventually result in formation of carbon at the exposed region and this may end up destroying the device. The degree of damage depends on the energy of the electrons and the exposure time. To minimize the damage the exposure time is made as short as possible by setting up automatic imaging. The energy of the electrons are also low.

4.3.6 Lift-off

Lift-off is the procedure of removing all resist from the chip, by immersing it into a solution. When the wires are not fixed on the surface of the chip by contacts the chip must be immersed into the solution with great care. However, wires have been observed to change position during Lift-off.

4.3.7 Wire Deposition and Location

To ensure that the nanowires are deposited correctly relative to the bottom gates, so-called wire windows are made in the resist. The size of a wire window is 1 μm x 40 μm and it is placed transverse to the bottom gates. A clean room wiper is cut into triangles of about 1 cm x 2 cm and picked up with a tweezer. The sharp tip of the wipe is gently rubbed against the growth substrate, making wires stick to the tip. The tip is gently rubbed along the direction of the wire windows on the chip, making the wires fall into the windows. The resist can easily get damaged. The procedure is repeated, while frequently checking the progress in a microscope. When sufficient number of wires have fallen into the wire windows, all resist is removed and thereby also the wires on top of the resist. If enough wires seem to have a good placement SEM-images are taken.

The SEM-images are transfered to a computer program called DesignCAD23, which contain a model of the chip. The alignment marks on the SEM-images are aligned with the corresponding alignment marks in the model. In this way we get to know the location of the wires inside the writing field and with high accuracy we can then decide where to place etching windows, contacts and electrodes. The high resolution SEM-images for detecting the Al-shell do not contain alignment marks, but the Al-shell can in general be located rather precisely by comparing the nanowires in the two SEM-images.

4.3.8 Al-Etching

In fabrication of Dev1 and Dev2 the Al-shell has to be removed at the two ends of the wire. See fig.5 and fig.7. From earlier experiments we know that the Al-shell can be etched up till 150 nm underneath the resist. Therefore the etching windows are placed 100 nm from the point where the Al-shell is supposed to be removed. In fabrication of Dev1 the Al-shell also has to be removed to create a junction in the Al-shell. The width of this etching window is 50 nm. To make it easier for the etching solution to go inside the relatively narrow window it is shaped like an hourglass. The etchant is Aluminum Etchant type D. A cup of Al etchant is placed in the hot bath. When the temperature of the solution is 55 ± 3 degree Celsius the chip is fixed by a tweezer and immersed into warm Milli-Q water. The purpose of this is to avoid the creation of air bubbles on the chip, which might prevent the etching from happening. When the chip is wet, it is immersed into Al etchant for 9 s and then directly immersed into the hot milli-Q water to remove the Al etchant. To ensure all Al etchant is removed the chip is also immersed into two other cups with milli-Q water.

4.3.9 Deposition of Metal

InAs/Al and InAsSb/Al interact with air making the surface insulating, therefore one have to find a way to remove the oxidized layer before the wire can be electrically contacted. There exist different possibilities, which all have pro and cons. In fabrication of Dev1 and Dev2 Ar-milling has been chosen as the preferred method for removing the oxidized layer of InAs and InAsSb. We do not try to remove the oxidized layer of Al with Ar-milling, because the time needed to do this is about four times longer than the time needed for removing the oxidized layer of InAs. Trying to remove the oxidized layer of Al would damage the crystal structure of InAs.

Ar-milling and metal deposition are performed in the same machine in high vacuum. In this way it is ensured that no new oxide will be created on the surface of the wire between milling and metal deposition. Ar-milling is the procedure of bombarding a material with Ar-atoms, causing some of the atoms of the material to leave it. In the ideal case the accelerated Ar-atoms will not go into the material, but only transfer some of their kinetic energy to atoms at the surface and then bounce off again. In reality the Ar-atoms might go deeper into the material depending on their energy and the properties of the material. This may course a change in the crystal structure of the bombarded material, which is of course not desirable. The milling time used in fabrication of Dev1 and Dev2 were based on experiences from other researchers at Qdev. For this specific milling time ,they had achieved good ohmic contact to InAs/Al nanowires.

To make up for an inevitable small angle with respect to horizontal the sample holder is set to rotate while metal is deposit either by electron beam evaporation or by sputtering. In electron beam evaporation a focused electron beam heats up a metal causing it to evaporate. In fabrication of Dev1 and Dev2 electron beam evaporation is always used for deposition of Ti and Au. In the process of sputtering, a substrate containing Nb and Ti is bombarded with Ar-ions and N-ions. Due to energy transfer between the incoming Ar-ions and atoms of the substrate, some of the Nb and Ti atoms will be ejected and combine with N leading to deposition of NbTiN on the chip.

5 Results and Discussion

During the past four months I have been working on four generations of devices. The first two generations of Dev1 were without bottom gates. Instead the gates were deposited on the chip surface and placed as close to the wire as possible without touching it. Both generations were unsuccessful. Many gates and contacts were shortened and milling seemed to have damaged the wires, as seen in fig.11*a* and fig.11*b*. In both cases system failures occurred in connection with metal deposition, but it was also concluded that the wires had been over milled. To avoid shortening and to achieve more effective gates bottom gates were introduced. The next two generations of Dev1 and Dev2 were

fabricated with bottom gates. Unfortunately these two generations were also unsuccessful. SEM-images show the result of Dev1 and Dev2 on fig.11*c* and fig.11*d*. Again system failures occurred in connection with metal deposition. In the last attempt to fabricate Dev1 and Dev2 on bottom gates the wire deposition was not successful. Reasons for this was bad wires and many shorted bottom gates.

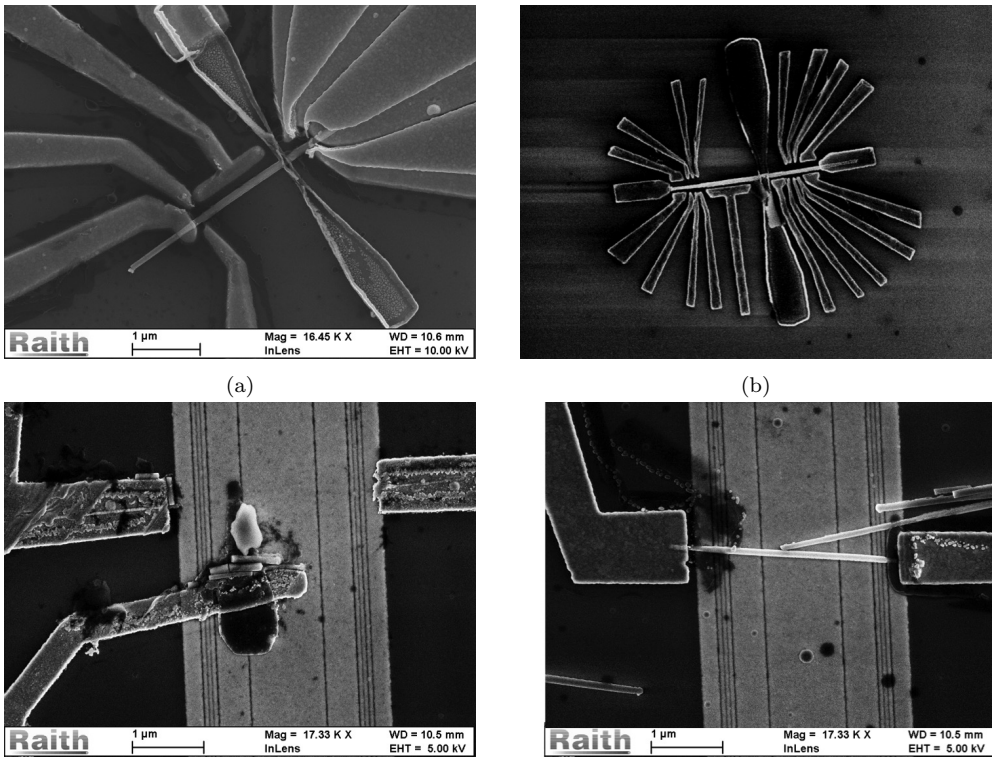


Figure 11: Different generations of Dev1 and Dev2. a), b) Dev1 without bottom gates, in both images the gates are shorted. c) Dev1 with bottom gates. The wire is gone and the contacts seem rough and damaged. d) Dev2 with bottom gates. The wire is almost gone at the contacts

Although there has been many problems in the fabrication of Dev1 and Dev2, the designs are still relevant for MF research and furthermore it is important to find out if the bottom gates work and if they should replace the method used so far. In the following I will elaborate on the main difficulties associated with the fabrication of Dev1 and Dev2, alternative fabrication procedures and finally I will propose how to proceed.

One challenge arising from the bottom gates is wire deposition. The wires must be placed on top of all the relevant bottom gates to become part of a device. The wire windows are helping to place wires transverse to the bottom gates. However, the shorter the wires are relative to the bottom gate pattern required and the more shortened bottom gates there are, the less is the probability of achieving wires relevant for devices. An easy way to achieve a more successful deposition is to use longer wires. One should aim for wires of more than 8 μm, which are possible to grow. The yield for the bottom gates must of course also be improved.

Another method for depositing wires could also be considered. This involves picking up individual nano wires from a growth substrate with a tungsten tip, while looking in a microscope. The tungsten tip can be moved and lowered down to a chip surface where the wire will be deposit. The setup is very similar to a setup developed at Aachen University [3]. Researchers at Aachen University can control the position with a lateral accuracy below 1 μ and an angular accuracy of 9 degrees. They

have obtained an average time of 5-10 min for picking up one wire and depositing it. Although their method is not exactly the same as the one used in Qdev Lab, it seems like the procedure can become more efficient with training and it seem worth investing time into this project. One should be aware that the Al-shell might fall of in this process, but this can also happen in the currently used method.

The introduction of bottom gates has lead to an unexpected challenge, namely detecting the Al-shell. Using the SEM-settings which before the introduction of bottom gate chips made it possible to detect the Al-shell no longer works when the wires are placed on top of bottom gates. This may be caused by the Au bottom gates reflecting a larger amount of electrons and thereby making it more difficult to detect a small signal coming from the Al-shell. It is crucial for fabricating these devices that it is known where the Al-shell has been etched. In order to solve this problem one could make a test sample containing wires on top of bottom gates and on the normal SiO_2 chip surface. The latter is to control that the wires have actually been etched. One should try different beam voltages, different angles and different lenses. Hopefully one will be able to find settings which will make it possible to find the shell.

Another important issue is how to create good contact to the wire. Researchers have achieved good ohmic contact, when they have been milling InAs. However, from the fabricators viewpoint Ar-milling is troublesome. The milling rate changes over time and currently there is no standardized measure for achieving good ohmic contact. Initial steps have been taken. The idea is to perform milling on InAs and SiO_2, and find out how much removed SiO_2 corresponds to good contact with InAs. This is of course achievable, but it takes time because one has to perform many tests. However, it would be very helpful to have and probably it would reduce fabrication failures. One could also consider other methods for the removal of oxide on the wire, since Ar-milling to a greater or lesser extent damages the crystal structure of the wire. An alternative method is passivation, which would not damage the crystal structure of InAs. By immersing the sample into Ammonium sulfide, oxygen is replaced with sulfide and the surface thereby does not oxidize. The problem associated with this is that the solution also etch the Al-shell. If a passivation solution without this disadvantage exist is not known at the moment.

Several system failures turned out to be fatal in fabrication of Dev1 and Dev2. These have all occurred in connection with metal deposition. The first one was overheating of the sample holder damaging the resist and thereby resulting in shorted gates and contacts. In the second one the shutters stopped working resulting in too much metal being evaporated onto the chip leading to shortening. In the third one the neutralizer associated with Ar-milling broke resulting in charged Ar-ions bombarding the sample, this lead to general damage of contacts and wires. Of course all cannot be blamed to system errors, but the overall damage made it difficult to asses what else had gone wrong. In order to reduce the probability of destroying the device one should try to minimize the number of times using metal deposition for one device, but of course without compromising the physical relevance of the device.

Leaving the discussion of fabrication procedures I will now mention some recent experimental insight, which have impact on the design of Dev1 and Dev2. A recent measurement preformed by Post doc. Mingtang Deng on a device using same InAs/Al wire as Dev1 implies that the wave function of two MFs separated with a distance of 1 um will overlap significantly. This discovery obviously have consequences for Dev1, since the long segment cannot be considered long anymore. We would now expect that a measurement at C_L when the long segment supported a pair of MFs would lead to a splitting of the ZBP.Another even more recent measurement performed by Post doc. Mingtang Deng showed a hard induced superconducting gap in a InAsSb/Al nanowire . This observation is a very important. If it turns out to be reproducible in more InAsSb/Al nanowires, these wires will most likly replace the currently favored InAs/Al nanowire in Qdev lab. This mean that the InAsSb/Al nanowire should also be used in Dev1. It will then be interesting to see if and how much the MFs wavefunctions will overlap in the new material.

If one were to proceed this work it is crucial that a solution to the problem concerning detection of the Al-shell in SEM is found. The new direction of using bottom gates definitely seems promising. It is important to achieve working devices with bottom gates, so it can be clarified through measurements

in the dilution refrigerator if they are working as intended. Regardless of which wire deposition method that is chosen long wires would must likely make wire deposition easier. Nanowires of about 8 μm or longer would work well. In connection with this one might invest some time getting familiar with the new wire deposition method, which could lead to a more efficient and controllable placing of the wires. Due to the new insights concerning InAsSb/Al nanowires, these wires are probably the ones we want to use for future devices. System and self-inflicted fabrication failures will always occur, however, minimizing the number of lithographic steps, especially the once including metal deposition, will improve the possibility of success. To achieve good and working devices it is important that each fabrication procedure is relatively reliable. An effort should be put into finding a process which will give good ohmic contact to the wire and which is reliable.

6 Conclusion and Outlook

The focus of this project has been on designing and fabricating hybrid semiconductor/superconductor 1D nanowire devices in which MF zero modes can be detected. In particular the focus has been on devices in which the energy splitting of nearby MF zero modes could be observed. The ultimate goal was to get a working device and measure the energy splitting by using gates to control the position of MFs. Unfortunately the fabrication of these devices did not turn out successful due to system and self-inflicted fabrication failures. However, the device designs presented in this report are still highly relevant in MF research. It is therefore worth making an effort into achieving these devices. In order to do so the fabrication process must be improved. The implementation of bottom gates is promising and they should for now maintain part of the setups. It is crucial to find out how to detect the Al-shell of the wires, when they are situated on top of bottom gates. Furthermore it is important to find a reliable procedure to obtain good ohmic contact to the wires. The new InAsSb/Al nanowires look promising and due to recent measurement of a hard induced gap, these should replace InAs/Al nanowires in future devices. To improve wire deposition on the bottom gates a new method involving picking up individual nanowires should be used. Regardless of the wire deposition method longer wires are needed, also in order to make more advanced designs for devices. The field of MF research is now moving away from the detection of MF zero bound states into more complicated experiments trying to test fusion rules and exchange statistics of MFs. These experiments demand more advanced devices making the fabrication more challenging. Here there seem to be a big potential in sharing and cooperating with other research groups. One could imagining having a online sharing database, where researchers could upload their fabrication improvements and recipes. However, this online sharing should be organized and regulated by someone in order to make it useful.

References

[1] Jason Alicea, Yuval Oreg, Gil Refael, Felix von Oppen and Matthew P.A. Fisher, *Non-Abelian statistics and topological quantum information processing in 1D wire networks Nature Physics*, Vol.13, February 2011.

[2] Anindya Das, Yuval Ronen, Yonatan Most,Yuval Oreg, Moty Heiblum and Hadas Shtrikman, *Zero-bias peaks and splitting in an Al-InAs nanowire topological superconductor as a signature of Majorana fermions*, emphNature physics, Vol.8, pp.887-895, 2012

[3] Kilian Flöhr, Marcus Liebmann, Kamil Sladek and H. Yusuf Günel, *Manipulating InAs nanowires with submicrometer precision*, emphReview Of Scientific Instruments, Vol. 82, 113705, 2011.

[4] Jay D. Sau, David J. Clarke, and Summanta Tewari, *Controlling non-Abelian statistics of Majorana fermions in semiconductor nanowires*, emphPhysical Review, Vol. 84, 2011.

[5] W.Chang, S.M.Albrecht, T.S.Jespersen, F. Kuemmeth, P. Krogstrup, J. Nygård and C.M.Marcus *Hard gap in epitaxial semiconductor–superconductor nanowires Nature Nanotechnlogy*, Vol.10, March 2015

[6] MicroChem Innovative Chemical Solutions for MEMS and microelectronics, *http://www.microchem.com/pdf/PMMA_Data_Sheet.pdf*, Visited: 03. June 2015

[7] NanoFab, A Micro Machining and Nanofabrication Facility, *http://www.nanofab.ualberta.ca/wp-content/uploads/downloads/2011/02/ZEP_Spin_Curves1.pdf*, Visited: 03. June 2015

[8] Martin Leijnse and Karsten Flensberg, *Introduction to topological superconductivity and Majorana fermions Semicond. Sci. Technol.*, Vol.27, March 2012.

[9] Sergey Frolov, *Quantum Transport, Lecture 20: Majorana Fermions*, University of Pittsburgh, Spring 2013.

[10] V.Mourik,K.Zuo,S.M.Frolov,S.R.Plissard,E.P.A.M.Bakkers,L.P.Kouwenhoven, *Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices,Science*, Vol. 336, pp.1003-1007, May 2012

[11] Su-Huai Wei and Alex Zunger, *InAsSb/InAs: A type-I or a type-II band alignment*, *PHYSICAL REVIEW B*, Vol. 52, 15 October 1995.