University of Copenhagen

Bachelor Thesis

Fabrication and characterization of superconducting coplanar waveguide resonator on silicon and silicon germanium heterostructures

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"The thing that differentiates scientists is purely an artistic ability to discern what is a good idea, what is a beautiful idea, what is worth spending time on, and most importantly, what is a problem that is sufficiently interesting, yet sufficiently difficult, that it hasn't yet been solved, but the time for solving it has come now"

Professor Savas Dimopoulos, Stanford University

UNIVERSITY OF COPENHAGEN

Abstract

Center for Quantum Devices
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Fabrication and characterization of superconducting coplanar waveguide resonator on silicon and silicon germanium heterostructures

by Victoria SOSNOVTSEVA

This thesis describes the theoretical framework, fabrication and measurements of a superconducting NbTiN resonator on silicon and silicon-germanium heterostructures. The idea is to create a circuit quantum electrodynamic architecture with spin qubits in semiconducting quantum dots coupled to a coplanar waveguide resonator, where the high quality allows the system to be in the strong coupling regime; this provides a scalable solution towards long-range entanglement of spin qubits. The thesis suggests a fabrication recipe developed for a liftoff process for making half wavelength 20 nm NbTiN resonators. Identical resonators were deposited on three different materials: silicon, silicon germanium with an etched quantum well and an implanted silicon germanium with a quantum well intact. On the implanted material the design also included accumulation gates and ohmics in order to test the accumulation of the 2DEG and its effect on the resonator. Resonators were tested in a Oxford Instruments Triton TM 200 cryogenic free dilution refrigerator at base temperature; the characterization consisted of S21 transmission measurements with input powers ranging from -40 dBm to -10 dBm, and parallel and perpendicular magnetic field sweeps in order to confirm the location of the resonance peak. Data were analyzed in order to fit a Lorentzian to the resonance peak and extract the quality factor. The quality factor for resonators on silicon and implanted Si/SiGe heterostructures was of the order 10^3, while the resonator on Si/SiGe with an etched away quantum well showed no resonance. The dependence of the quality factor and resonance frequency on magnetic field were also studied: the quality factor deteriorates with magnetic field while the resonance frequency decreases. Improvements to the fabrication recipe and design are discussed, which can lead to higher quality factors in the future.

Acknowledgements

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Chapter 1

Theoretical background

1.1 Introduction

Quantum computing is exciting because it has the potential to efficiently simulate processes that occur in nature. Feynman envisioned a use for quantum computers 35 years ago to solve problems that classical computers cannot solve. Now perhaps we are reaching a stage where this is becoming reality. Recently IBM's 50 qubit cloud quantum computer was used to solve n-atom electronic-structure problems. This cannot be done by classical computers since the task of finding exact solutions to such problems scales exponentially with the size of the system [1]. However, the idea that quantum computing is worth the investment relies on two key assumptions: quantum computing is powerful and scalable.

Power of quantum computing is based on quantum algorithms. One of the most celebrated algorithms is Shor's algorithm for factorization. The ability of a classical computer to factor a number with n digits grows exponentially; it is harder the longer the number is. RSA cryptography takes advantage of this in order to encrypt information. However, for a quantum computer the difficulty grows as a polynomial of n degree, which is a considerable improvement [2].

The scalability of a quantum system depends on its hardware that is made up of qubits, which is a two level system. These qubits need to fulfill Di Vinzcenso criteria in order to be useful [3]:

- Storage: A system with scalable qubits
- Isolation: Protection of qubits from decoherence
- Readout: The ability to measure a system reliably
- Gates: The ability to control qubits over long distances
- Precision: The ability to perform quantum gates quickly and precisely

Spin qubits are one of the possibilities for the building block of a large scale quantum computer, along with superconducting qubits, ion trap qubits, majorana qubits and many others. The thesis will focus on the fabrication and characterization of a resonator that is needed for the scalability of a spin qubit based quantum computer [4].

1.1.1 Spin as a qubit

There are many different types of qubits, both natural and artifical. The main focus of tghis thesis is the spin qubit. The spin qubit is most basically defined by the electron spin either pointing up or down, however can also be defined in other states such as a singlet/triplet state. Spin is the intrinsic angular momentum carried by particles.One uses Bloch sphere for a geometrical representation of qubit states. On the Bloch sphere one can set a coordinate system such that the z-axis is associated with spin up. Thus the spin up state is $|0\rangle$, the negative z-direction is $|1\rangle$ and the x-axis is the state $\frac{1}{\sqrt{2}}|\uparrow\rangle + \frac{1}{\sqrt{2}}|\downarrow\rangle$. In order to measure if a spin qubit is in state $|\uparrow\rangle$ or $|\downarrow\rangle$ one defines an operator with eigenvalues $|\uparrow\rangle$and $|\downarrow\rangle$. The operator is called the Pauli spin matrix:

$$\sigma_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} , \tag{1.1}$$

which has eigenvectors $|0\rangle$ and $|1\rangle$ with eigenvalues 1 and -1 respectively. Since spin has a magnitude of $\hbar/2$, this will be scaled. To measure spin in a different direction one uses an operator with different eigenvectors, for example, the operator for the x-direction will be:

$$\sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \tag{1.2}$$

with eigenvectors $|+\rangle = \frac{1}{\sqrt{2}}|0\rangle + \frac{1}{\sqrt{2}}|1\rangle$ and $|-\rangle = \frac{1}{\sqrt{2}}|0\rangle - \frac{1}{\sqrt{2}}|1\rangle$ [5].

1.2 Circuit quantum electrodynamics

Circuit quantum electrodynamics helps to understand the interaction between light and matter. In order to describe coherent behavior between a bosonic system (harmonic oscillator) and a fermionic two level system one uses the Jaynes Cummings Hamiltonian [6]:

$$H = \hbar\omega_r(a^\dagger a + 1/2) + \frac{\hbar\omega_{01}}{2}\sigma^z + \hbar g(a^\dagger\sigma^- + a\sigma^+) . \tag{1.3}$$

The first term describes the energy in the electromagnetic field inside the cavity with each photon having the energy $\hbar\omega$. The second term represents the two level system, in this case an atom, with spin half, and the third term describes how the atom absorbs or emits a photon at the rate g.

However, in such a system there are also incoherences such as the leakage of photons from the cavity, which can be used to define the the Q factor as:

$$Q = \omega_r/\kappa , \tag{1.4}$$

where κ is the photon leakage rate from the cavity. Other forms of incoherence may arise due the atom itself decaying at a rate γ and the finite lifetime of the atom $T_{transit}$. When the cavity is in resonance with the atom the two can freely exchange energy and the competition between coherence and incoherence becomes important. If no decay is present then the system will oscillate forever between absorption and emission of a photon by the atom. These oscillations are called vacuum Rabi oscillations. If these oscillations happen before the atom or photon is lost, the system is in the strong coupling limit which fulfills the condition:

$$g > \kappa, \gamma, T_{transit} . \tag{1.5}$$

This regime is also significant due to the change of eigenstates. When the cavity and atom have an interaction term in their hamiltonian the ground and excited states of the atom, $|g\rangle$ and $|e\rangle$ are no longer the eigenstates. The new eigenstates that can diagonalize the interaction term in the Hamiltonian are:

$$|\Phi\pm\rangle = (|g\rangle|n\rangle \pm |e\rangle|n-1\rangle)/\sqrt{2} . \tag{1.6}$$

These eigenstates are split by the energy $2g\sqrt{n}$ which is important for identifying a system in the strong coupling regime.

In order to study this phenomenon in a controlled environment, cavity QED has given rise to the field of circuit QED where the photon is stored in a one dimensional resonator and the two level system is an "artifical atom". The first artificial atom was the cooper pair box [8] followed by

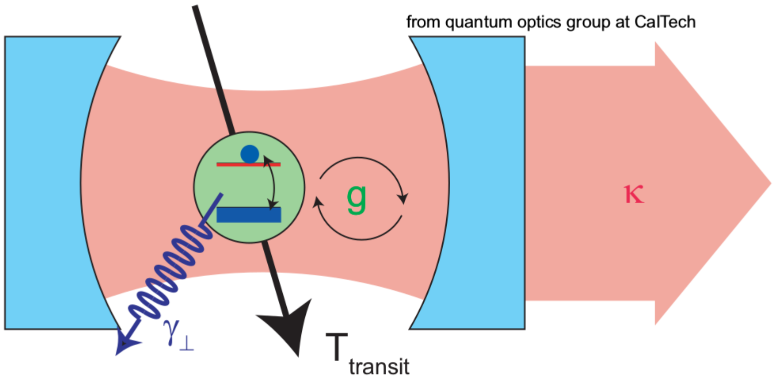

FIGURE 1.1: Schematic illustration of cavity QED showing the rate of coupling g, the rate at which photons escape the cavity κ, and the rate of decoherence of the atom γ. Reproduced from [7].

others such as transmon qubits and gatemon qubits. However, in this experiment one deals with spin qubits. This is of particupar interest in the scientific community: Is it possible to combine spin qubits with cQED in order to create a new hybrid system for quantum computing which could provide a platform for quantum readout and transportation of quantum information [7].

1.2.1 Why silicon?

Spin qubits rely on the spin of an electron which can be up or down for its two well defined states; two dimensional electron gas found in semiconducting heterostructures is a natural medium for creating quantum dots contatining spin qubits.- An interface between two interfaces with different band structures is needed to create a 2DEG, such as between Si and $Si_{1-x}Ge_x$.In order to control quantum dots one needs to have confinement in one or more directions using electrostatic gates [9].

We used Si/SiGe heterostructures for DQD experiments since they have high electron mobility; room temperature mobility of 40,000 $\mathrm{cm}^2/\mathrm{Vs}$ and low temperature mobilities of 800,000 $\mathrm{cm}^2/\mathrm{Vs}$ have been measured. This can be further improved by using positively biased accumulation gates instead of doping the structure. These gates are placed on top of the surface and insulated from it using an oxide such as Al_2O_3. This method eliminates impurities inside the substrate that cause scattering and bring mobilities up as high as 1.6×10^6 $\mathrm{cm}^2/\mathrm{Vs}$ [10].

The first material of choice for making a 2DEG was gallium arsenide, however nuclear spins in III/V heterostructures limit spin relaxation and coherence times. Another option was to use isotopically purified silicon, which has zero nuclear spin which reduces the dephasing of electron spins[11]. Quantum devices based on silicon can be scaled up to larger systems of qubits using the already in place industrial standard for production of semiconductors.

Arrays of quantum dots in silicon have already been demonstrated. For example, an array of 9 quantum dots fabricated on a Si/SiGe heterostructure by Jason Petta's group (Princeton University, US). This was a proof of concept to show the scalability of linear semiconducting qubit arrays, thus, fulfilling the first Di Vincezo criteria of storage. These quantum dots showed coherence times of 28 ms and high charge readout sensitivity. (CITE) The next criteria to be fulfilled is performing gate operations. Jason Petta's group demonstrated a controlled CNOT gate using two Si spins [12]. Vandersypen group (Delft University of Technology, The Netherlands) demonstrated a computational algorithm in Si [13]. However, a problem arises when fulfilling the criteria for control of qubits over a large distance. Semiconducting quantum dots are small (the previouly mentioned linear array of dots fit into an area of 1.5 μm) but they do not interact unless their wave functions overlap. This means they only interact with nearest neighbors. In order to solve this problem we need to create a hybrid architecture that combines circuit quantum dynamics and semiconducting quantum dots [14].

In this setup the optical cavity is replaced by a transmission line resonator and the atom with superconducting or semi conducting quantum dots. This system creates a mechanism by which Si qubits become entangled with a photon and exchange quantum information. Since the length of the resonator extends over mm, and the circulating photon cam share quantum information between numerous array of Si qubits. Since silicon has long been used in the industry, engineers can leverage fabrication experience developed since the development of the first classical computers and potentially scale up the device to contain thousands of qubits.

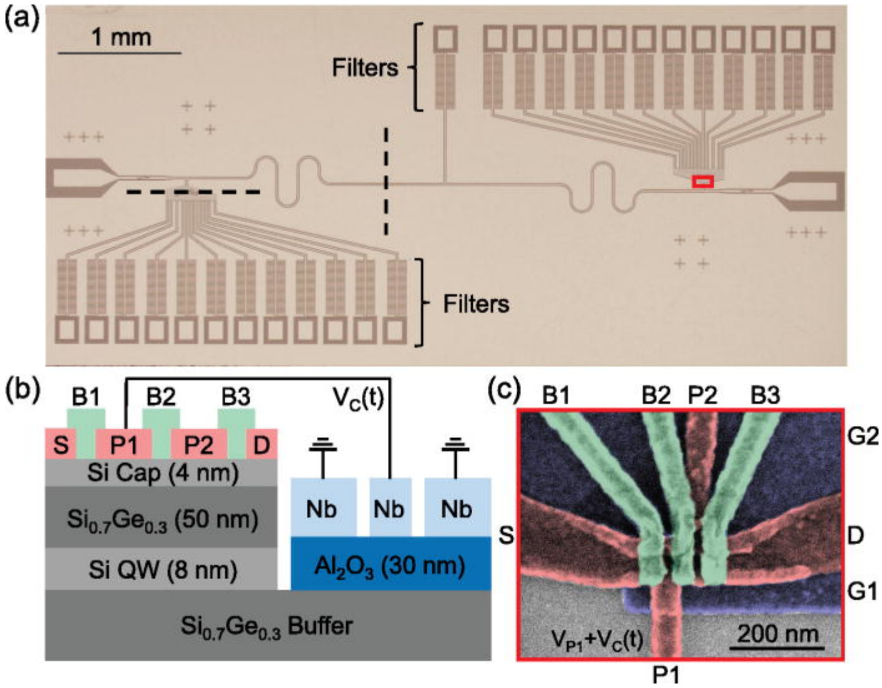

FIGURE 1.2: Jason Petta's hybrid cQED device. (a) An optical image shows a $\lambda/2$ Nb resonator has DQDs placed at its voltage anti-nodes with LC filters reducing leakage of cavity photons. (b) Cross sectional cut of the substrate: the quantum well is etched away underneath the resonator, and left intact under the overlapping Al gates that define the DQD. (c) False-color scanning electron microscope image of DQD. Reproduced from [15].

The coupling of a superconducting resonator to double quantum dots (DQDs) has been demonstrated by Jason Petta's group (Princeton University, US), where the arrangement of DQDs and the superconducting resonator can be seen in Fig. 1.2. In their silicon hybrid cQED device they placed a DQD at each voltage antinode of the cavity, with LC filters at every DC connection in order to reduce leakage of caivity photons. The Si quamtum well under their resonator was etched away. Their resonator had a cavity center frequency of 7.67 GHz and a Q of 5400, though without the LC filters the Q was 1000 and lower. The DQDs were made through an overlapping gate architecture with two plunger gates and a source and drain accumulation gates. The estimated coupling between their cavity and qubit (g_c) is $23 \times 2\pi$ MHz, which compares favorably with those in other semiconductor systems [16].

1.2.2 Coplanar waveguide resonator

Coplanar waveguide resonators (CPWs) are advantagious to use with cQED due to their easily controlled impedance and high quality factors. CPWs are made up of a central conducting strip with two ground planes on either side which are seperated by a length s. The ground planes need to be much larger than s in order to be approximated as infinite. Coplanar waveguide properties are good for creating open circuited transmission line resonators because their properties are dependant on geometry of the structure (especialy on the seperation between the center conductor and ground planes (s) and the thickness of the superconductor (t)). In this thesis we fabricated an open circuited transmission line resonator that behaves as a parallel LCR circuit when the length is multiples of $\lambda/2$. For more information on modeling a transmission line as an LCR circuit refer to Appendix A.

To measure the resonator it needs to be coupled to the outside environment using capacitors and measured using a vector network analyzer which measures its scattering matrix as:

$$[V^-] = [S][V^-] \, , \tag{1.7}$$

which can be rewritten as:

$$S_{ij} = \frac{V_i^-}{V_j^+} \, . \tag{1.8}$$

For example, S_{21} is found by driving port one with a voltage and measuring the amount of voltage at port 2 with respect to port 1 [17].

In order to evaluate the transmission of the resonator and to deduce its intrinsic Q factor we can use the ABCD matrices which we can write out the following way based on the circuit model of the resonator [18]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{i\omega C_{in}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos(\beta l) & iZ_r \sin(\beta l) \\ \frac{i}{Z_r}\sin(\beta l) & \cos(\beta l) \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{i\omega C_{out}} \\ 0 & 1 \end{bmatrix} \, . \tag{1.9}$$

The resulting matrix can then be normalized for the external impedance and converted to the transmission amplitude:

$$S21 = \frac{2}{A + B/R_L + CR_L + D} \, . \tag{1.10}$$

An analytic expression for the external Q factor can be extracted from S21 with relation to C_{in} and C_{out} [18]:

$$Q_{ext} = \frac{\pi}{2} \frac{1}{\omega_0^2 Z_r^2 (C_{in} + C_{out})^2} \, . \tag{1.11}$$

The external Q factor is the ration between energy stored in the resonator and the energy lost to the coupled circuit [19].

In this thesis the resonances were fitted to Lorentzian and the Q was found as:

$$Q_L = \frac{f}{\Delta f} \, , \tag{1.12}$$

where f is the resonance frequency and Δf is the full width half maximum of the fitted Lorentzian peak.

The resonator also has an intrinsic quality factor which can be related to the external Q factor in the following way:

$$\frac{1}{Q_L} = \frac{1}{Q_{int}} + \frac{1}{Q_{ext}} \, . \tag{1.13}$$

where the loaded Q factor is a parallel combination of the internal and external Q factors. The external Q factor will be further lowered by microwave losses such as resistive and dielectric losses and radiative losses as discussed in Appendix A.

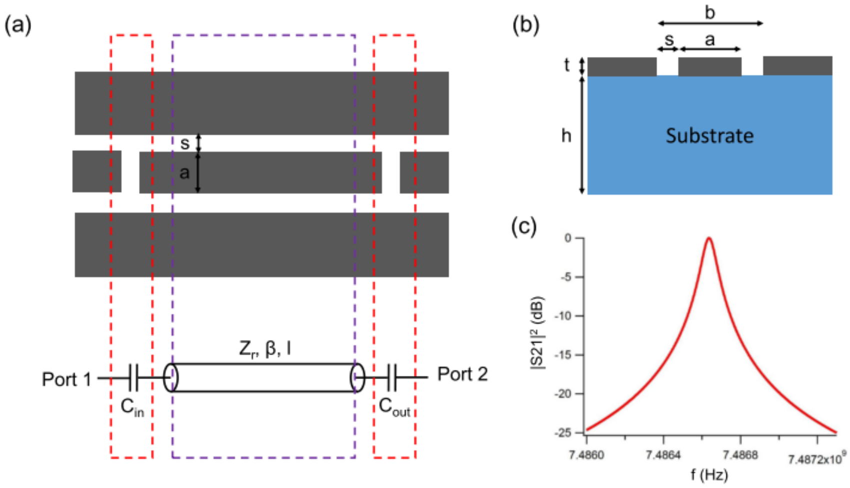

FIGURE 1.3: Schematic illustration of CPW resonator. (a) Circuit schematic with the corresponding physical parts of the CPW. (b) Cut through substrate with resonator on top and its parameters. (c) Example of S21 transmission for a $\lambda/2$ resonator. Reproduced from [18].

The internal quality factor is related to the geometry of a $\lambda/2$ resonator (Fig. 1.3) as defined as below:

$$Q = \frac{n\pi}{2\alpha l}\,, \tag{1.14}$$

where n is the nth mode of frequency, α is the attentuation constant of the transmission line and l is the length of the resonator defined as $2\lambda = l$.

The resonator's fundamental frequency is given by:

$$f_0 = \frac{c}{\sqrt{\epsilon_{eff}}}\frac{1}{2l}\,, \tag{1.15}$$

where ϵ_{eff} is the effective permittivity of the transmission line which depends on the wavegiode geometry and permittivity of the substrate. We can describe the specific CPW capacitance and inductance as dependant on parameters s and a:

$$L_l = \frac{\mu_0}{4}\frac{K(k_0')}{K(k_0)}\,, \tag{1.16}$$

$$C_l = 4\epsilon_0\epsilon_{eff}\frac{K(k_0')}{K(k_0)}\,, \tag{1.17}$$

where κ is the complete elliptic integral of the first kind with the arguments:

$$k_0 = \frac{a}{a+2s}\,, \tag{1.18}$$

$$k_0' = \sqrt{1-k_0^2}\,. \tag{1.19}$$

Thus the inductance and capacitance of the resonator are dependent on the geometry of the CPW and the resonant frequency dependent on the length and thickness of the superconductor used [18, 20, 21].

For information on how the resonator couples to DQDs, please, see Appendix A.

Chapter 2

Design, fabrication, and measurements

2.1 Design

A higher impedance cavity leads to a higher charge coupling rate (g_c) between the cavity and the spin qubit which is given by $g_c = \sqrt{Z_l}$ [22]. To increase coupling we made a high impedance cavity, which can be done by making geometrical changes to the CPW design.

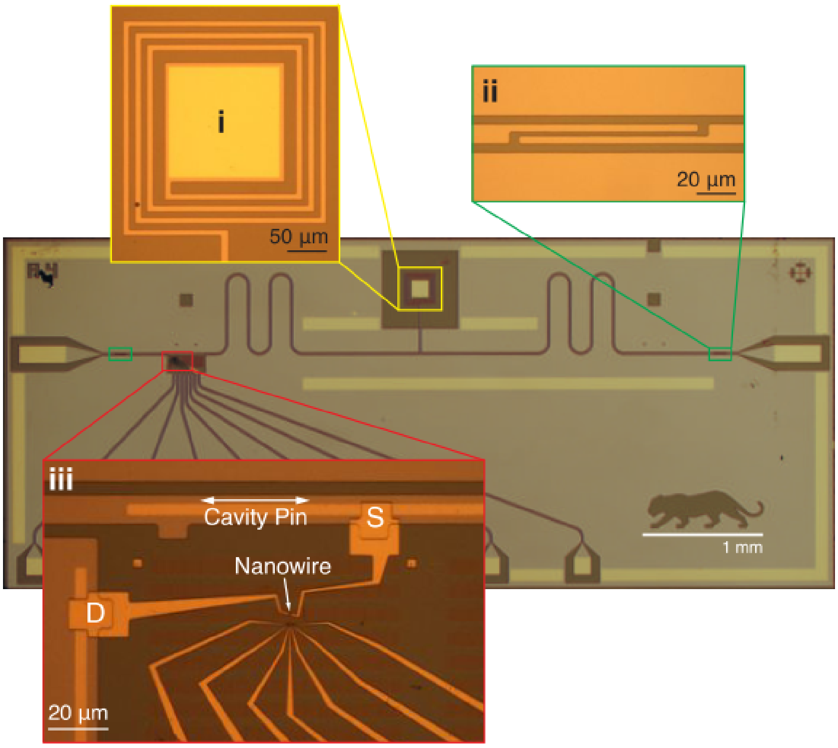

FIGURE 2.1: Optical image of a hybrid DQD/superconducting resonator device made by Jason Petta's group (Princeton, US) with zoomed views of the spiral inductor at cavity node (i), capacitors (ii) and nanowire quantum dot (iii). Reproduced from [23].

Fig. 2.1 shows the original design described in the publication on coupling a DQD to a resonator [23]. We made a number of geometrical changes based on the relationship between the impedance and the geometry of the resonator. This is summarized in the following equations:

$$Z_l = \sqrt{L_l/C_l}\ , \tag{2.1}$$

$$L_l = \frac{\mu\lambda_L^2}{at} g(a,s,t)\ . \tag{2.2}$$

This shows that the cavity impedance is directly proportional to the kinetic inductance of the waveguide, which is inversely proportional to the thickness of the superconductor and width of the center strip. Kinetic inductance is associated with the mass of current carriers, and in superconductors it dominates over resistance [24].

In our design we used a higher kinetic inductance material NbTiN rather than Nb, and reduced its thickness from 100 nm to 20 nm from Jason Petta's design, as well as varying the center strip width. Specific details of the different designs can be found in Appendix B. This design also has the benefit of reducing the effect of applied magnetic field on the type-2 superconductor: introducting hole pinning sites to the superconductor and reducing the width of the center strip has the effect of Abrikosov vortices in the superconductor. More theory on this is covered in Appendix A. Fig. 2.2 illustrates the design used in this thesis.

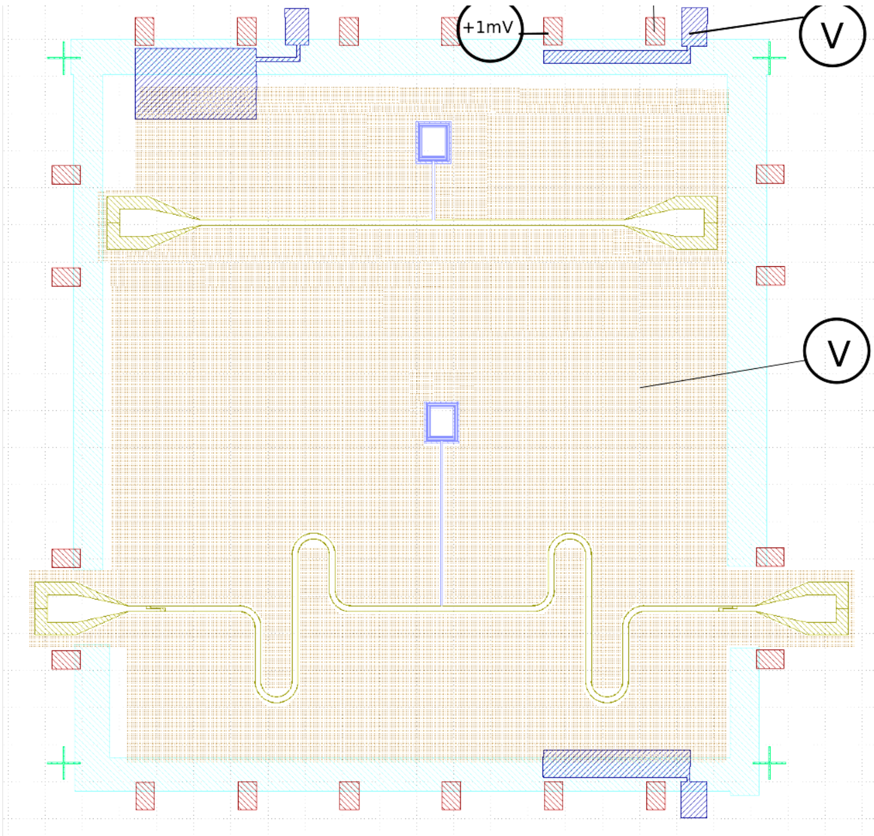

FIGURE 2.2: DXF image of our resonator design with feedline, accumulation gates and ohmics which was fabricated on top of the heterostructureseen shown in Fig. 2.3.

Our design also is different in two ways from the Jason Petta group's original design:

- In our final design we left the silicon quantum well intact rather than etching it away. The implanted heterostructure that we deposited the resonator on can be seen in Fig. 2.3. In this design accumulation gates and ohmics are deposited on the same layer as the resonator which allows for a quantum well to be accumulated underneath the resonator. This is done by applying a voltage on the accumulation gates: one can measure if the 2DEG is accumulated by measuring the current from the source to drain ohmic which is connected to the 2DEG through the implantation regions;

- We used an in-house liftoff process instead of a more conventional etching process used by other groups [25]. This discussed further in the next section.

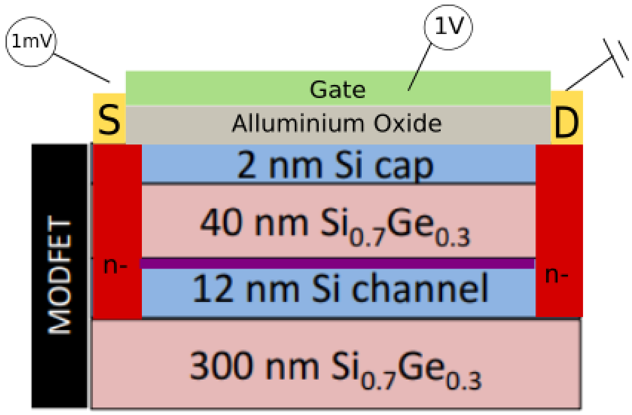

FIGURE 2.3: MODFET illustration. The purple layer shows the 2DEG formation at the interface between Si and Si/SiGe. The red area is the implantation region. On top of the heterostructure there are source and drain ohmics with a top gate on a layer of alumimium oxide.

2.2 Fabrication

2.2.1 Optical lithography

The first step is to create a chip with a resonator WAS to expose the pattern. This is done by using the Heidelberg *mPG* 501 optical lithography machine. The photo lithography process works by using light to transfer a pattern applying a photo mask to a light sensitive chemical on the chip called a "photo resist". For the 2D pattern we used the AZ1505 resist and a LOR3B resist spun at 4000 rpm for 45 s and baked at 115°C for 2 min and 185°C for 4 min, respectively. It is important that the photo resist is homogeneous: for small chips resist can accumulate on the edges of the chip causing problems in development (Appendix C, Fig. C.2). If it is possible, keep chips, going into the Heidelberg photolithography machine, of a minimum size of 10 $\times$ 10 mm: the smaller the chip, the less accurate the writing of the pattern. If using smaller chips using optical focus and not turning on freeze-focus helps increase writing accuracy. For information on how to expose the design in the Heidelberg photolithography machine refer to Appendix C.

After exposing the design the chip was developed in MF321 for 35 s for an exposure time of 22 ms and -2 defocus. A dose test should be done to comfirm the optimal exposure and development time for a specific substrate. After this it is important to ash the chip for 4 min in order to remove excess photo resist otherwise liftoff of metal will not work and result in a failed attempt as shown in Fig. C.1 [26]. An optical image of an exposed resonator design can be seen in Fig. 2.4.

2.2.2 Implantation

For the fabrication of implanted Si/SiGe material the substrate needed to be implanted with phosphorous ions that become electron donors in the substrate allowing a 2DEG to form on the interface between Si and Si/SiGe. The implantation was done using highly energetic ion beams and the energy needed to make the ions reach down to the silicon channel was simulated using the software SRIM which describes the “stopping and range of ions in matter”. After implantation ALD needed to be deposited on the substrate in the areas below the accumulation gates. More on ALD deposition can be found in Appendix C.

2.2.3 AJA sputtering and evaporation

In order to create a NbTiN resonator we deposited a layer of NbTiN on the chip which can be done by a technique called sputtering using the AJA and gold gates and ohmics are deposited using a technique called evaporation. A detailed description of this process can be found in Appendix C.

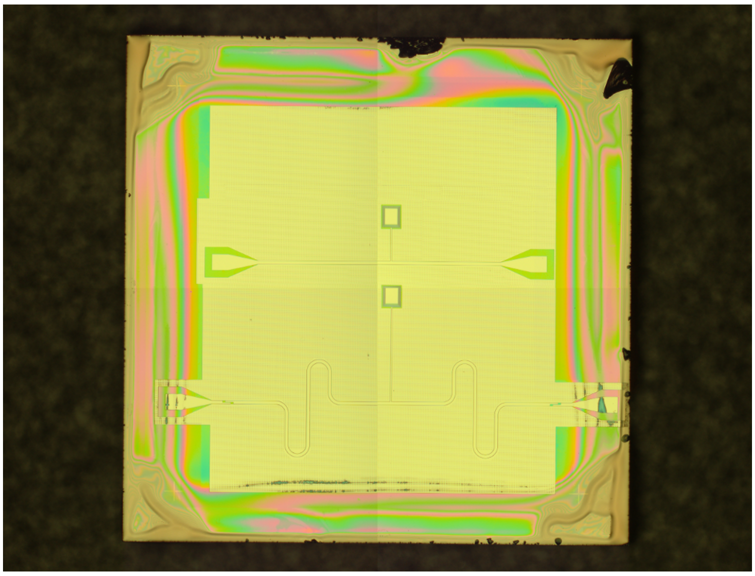

FIGURE 2.4: Optical image of developed resonator design.

When the chip is covered in metal we lifted it off using an acid such as NMP which removes the resist and thus strip the metal everywhere where the resist was not exposed using the Heidelberg photolithography machine. We submerged the chip into NMP heated up to 85°C. The thermal shock of putting the chip in hot NMP made liftoff easier and extra sonication helped remove the metal with photoresist underneath.

The benefits for using liftoff is that it is an in-house process which speeds up the process of making chips. The main drawback of the liftoff method is that it leaves behind debris at the edges of the design making it uneven, but this effect should be reduced by using LOR photoresist as well as AZ1505.

2.3 Measurements

To manipulate on chip elements at milli kelvin temperatures, we connected the chip to outside electronics. This was done by wire bonding teh chip to a PCB, loading this on a motherboard which is mounted on a puck and inserting this puck into the fridge. For information on the cQED daughterboard v2 designed during this project and used to mount the sample, see Appendix E.

The coaxial line setup of Triton 4 can be seen in Appendix D (Fig. D.1) as well as a description of the fridge line setup and attenuation. In order to measure the S21 element of the transmission frequency we used a Vector Network Analyzer. The Rhode Schwartz VNA used in the measurements, as well as the room temperature amplifiers, can be seen in Fig. 2.5.

The power input is measured in dBm which is an absolute measure of power defined as:

$$dBm = 10log(P/1mW)\ . \tag{2.3}$$

The power shown on the VNA is in units dB which is a relative quantity and is defined as:

$$dB = 10log(P1/P2)\ , \tag{2.4}$$

where P2 is the output power and P1 is the input power. More about the scattering matrix and modeling the S21 transmission can be found in Appendix A. If we input -20 dBm through one coaxial cable and it passes through 56 dB of attenuation the amount of power coming out will be -76 dBm, which the VNA converts to an S21 output of -56 dB.

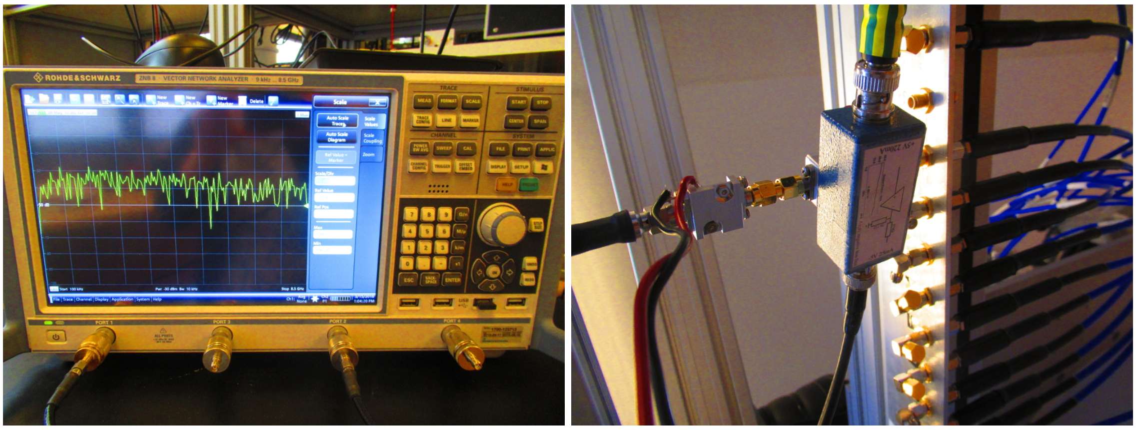

FIGURE 2.5: Photo of VNA (left panel) and room temperature amplifiers (right panel).

Another important feature of the fridge is the multi-axis superconducting magnet which is used to test the behaviour of the samples in a magnetic field. The magnet inside Triton 200 fridges has a range from 0.3T–14T and cancellation coils in order to minimize eddy currents. It also has 3 axis rotation, which means that the magnetic field can be ramped up on a given axis and can also be rotated.

The default power supply is the Mercury IPS which can be controlled remotely and supports the vector rotation of magnets.It can be ramped up to give a current output of 60 A. It is advertised as having low noise, however we found that using the Kepco bipolar operational power supply in order to power the magnet inside the fridge. as a power supply gives considerably less noise on the perpendicular x axis when the mercury supply is held on "CLAMP". The Kepco power supply has to be connected to a Keithly voltmeter which provides a voltage which scales as $1 : 2$ to the current provided by the Kepco — it is important to test using a multimeter before connecting to the magnet that this is the case since too much current will cause the magnet to quench. The Kepco is then connected through a cable to the top of the fridge, and the current to Tesla scale is roughly $1 : 60$. Data comparing field sweeps of a resonator on silicon using different power sources can be found in Appendix F.

Chapter 3

Results

In this section we present and overview of the samples measured. We made 12×12 mm wafers which could be divided into 4 chips. A letter at the end of the name signifies a wafer, while the number signifies the chip. Table 3.1 presents a summary of the chips tested. Fig. 3.1 shows selected images of all the samples at their final stage before bonding.

TABLE 3.1: Description of fabricated samples (Abbreviation: qw = quantum well).

Sample	Substrate	Fridge	Comments
T_res	Si	T4	$\lambda/4$ resonator made by Thorvald Larsen
$V\_res\_Si\_Z$	Si	T7	Tested magnet power sources
$V\_res\_Si\_A1-2$	Si	T4	Different bonding configurations
$V\_res\_SiGe\_Ae3-4$	Si/Ge with qw etched	T4	
$V\_res\_SiGe\_A1$	Si/Ge with qw intact	T4	First measurement
$V\_res\_SiGe\_A3$	Si/Ge with qw intact	T4	Design with added feedline

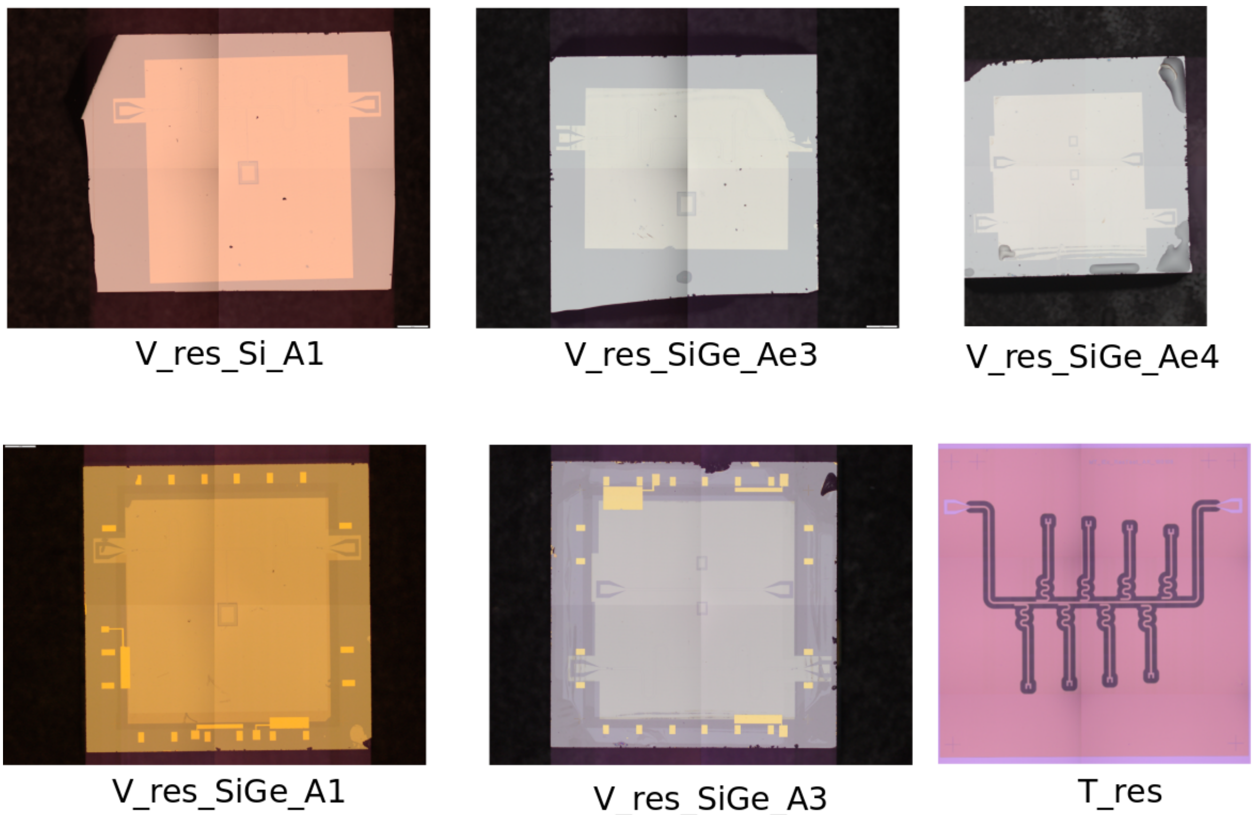

FIGURE 3.1: Selected images of all produced samples.

3.1 $\lambda/4$ resonator with different bonding schemes

In order to test that all elements of the fridge setup, the board and the puck were working, we loaded a known a resonator designed and fabricated by Thorvald Larsen (QDev, Copenhagen, Denmark). This sample can be seen in Fig. B.1. The resonator was designed to be a $\lambda/4$ resonator, and should have 8 resonances at different frequencies between 7 and 9 GHz. Details are given in Appendix B. We wanted to test if the resonators work with bonds just to the bias tee ground plane rather than bonds to the larger ground plane. This is important to our experiment since in order to bias the ground plane using the bias tees connected to the connected ground plane we would need to bond there. It is also conventional wisdom that in order to have a good RF ground one needs to have a lot of bonds to the larger ground plane, and we wanted to test this. Fig. 3.2 shows the different bonding schemes.

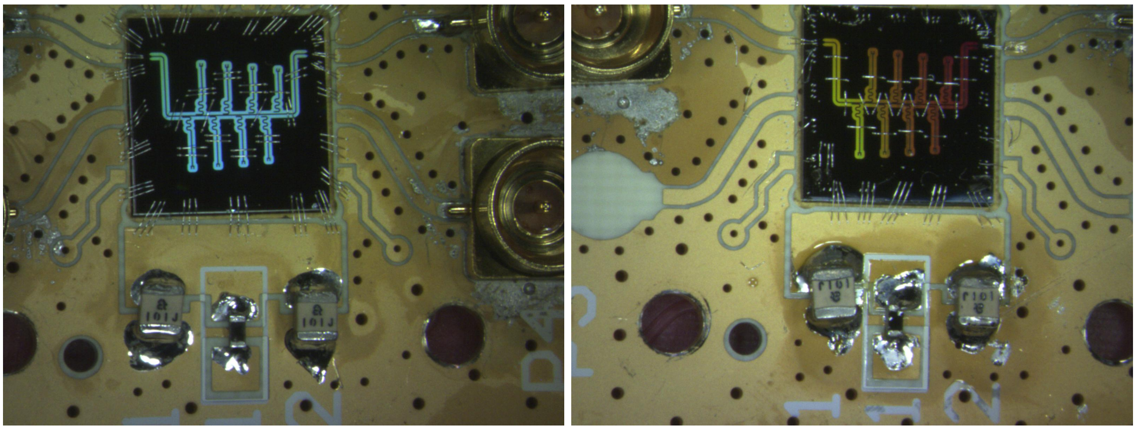

FIGURE 3.2: Bonding of Thorvald's resonator *T_res* for two different cool downs. Left panel: Bonding to both the bias tee ground plane and the real ground plane and across the resonator. Right panel: Bonding with bonds just to the fake ground plane and across the resonator.

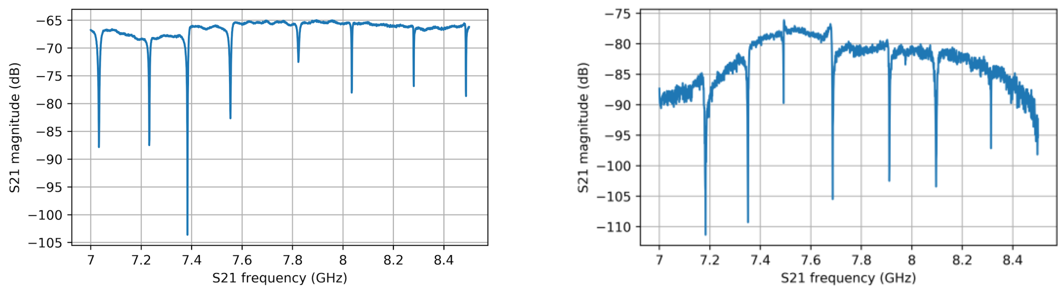

FIGURE 3.3: S21 transmission measurement for *T_res* sample with -20dB input power with two different bonding configurations shown in Fig. 3.2, left and right panels, respectively. The right transmission spectrum is at lower power and more noisy.

Results are presented in Fig. 3.3 together with a reference measurement of self-connected lines 13 and 14 given in Fig. 3.4. From these measurements we concluded that the setup was working. Comparing panels in Fig. 3.3 we can see that making bonds to the ground plane as well as to the bias tee ground plane of the cQED board reduces noise and power loss, though resonances are visible with both bonding schemes. Fig. 3.4 shows transmission starts at the power output (as we expected) and decreases with increasing frequency because of loss in the fridge lines. This indicates that the fridge electronics works.

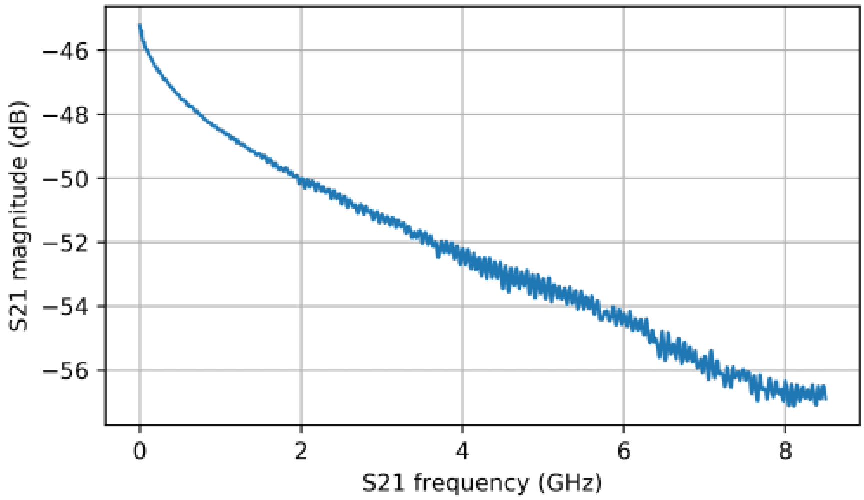

FIGURE 3.4: S21 transmission reference measurement for *T_res* sample through lines 13 and 14, which were shorted in the puck alongside the sample. The transmission is as expected given the fridge attenuation for lines 5 and 11

3.2 NbTiN resonators on silicon

The first measurement of a silicon resonator was used to compare two power sources for the perpendicular direction of the magnet: Mercury IPS and Kepco. It was found that data produced with the Kepco power source are less noisy when all the directions in the Mercury IPS were set to "CLMP". These data can be found in Appendix F.

After this test we measured two identical resonators on Si using two different bonding schemes (Fig. 3.5). In the left panel we have the bonding scheme where the sample is bonded to the general ground plane, while on the right panel we have only made bonds to the bias tee gound plane as well as some bonds across the resonator to connect the ground planes on the chip.

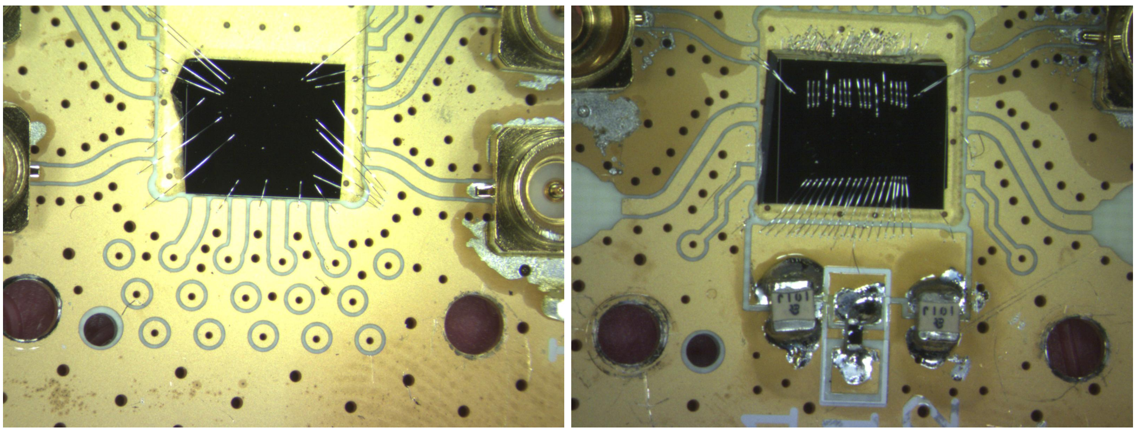

FIGURE 3.5: Bonding for *V_res_Si_A*1 sample (left panel) and *V_res_Si_A*2 sample (right panel).

We used lines 5 and 11 to measure *V_res_Si_A*1 with two room temperature amplifiers of +37 dB and +17 dB. When inputting power we noticed that higher power corresponded to a lower noise level. With -20 dB input power we took the S21 transmission sweep seen in Fig. 3.6. The resonance peak was suspected to be around 5.26 GHz (left panel) with the other smaller peak being a resonance mode on the chip. The resonance peak is clearly seen in the enlarged figure (right panel). The presence of resonance was confirmed by its movement in magnetic field. Resonance frequency changes with magnetic field due to a change magnetic inductance and the formation of Abrikosiv vortices in the superconductor [27]. This has been documented experimentally and more information on this is the Appendix A The perpendicular and parallel magnetic field sweeps are displyed in Fig. 3.7.

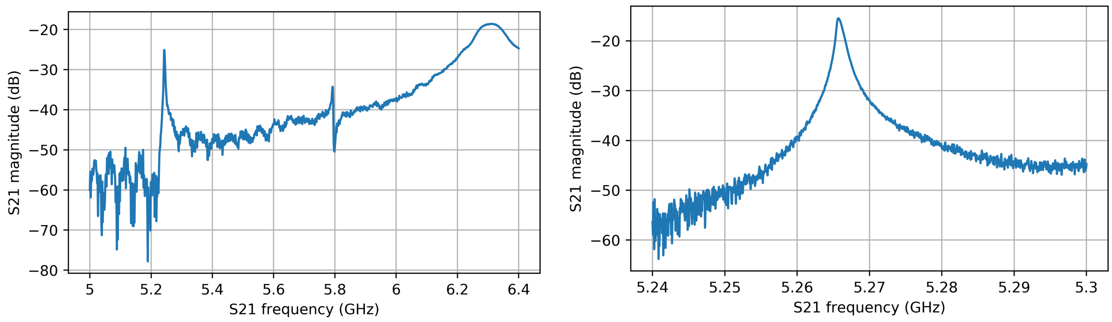

FIGURE 3.6: S21 transmission for *V_res_Si_A*1 sample in range of expected resonance frequencies with -40 dBm input power and two room temperature amplifiers (left panel). Taken with 1000 points and 10 averages. A zoom on the suspected resonance peak at 5.265 GHz (right panel).

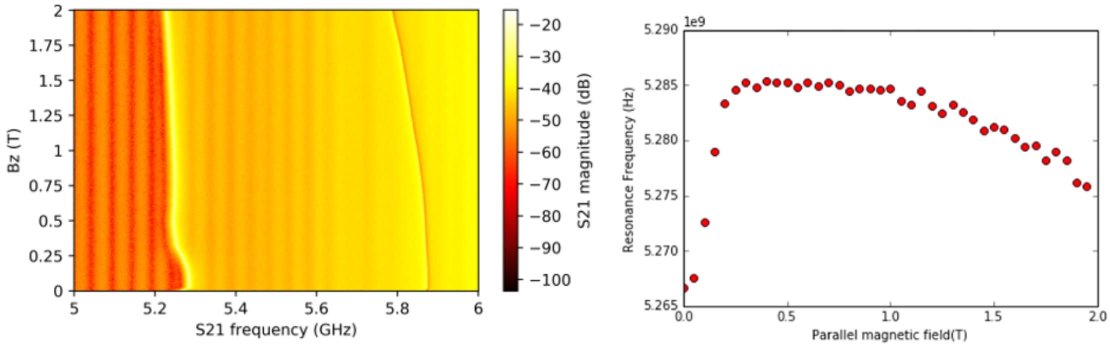

FIGURE 3.7: Results for *V_res_Si_A*1 sample. Left panel: Parallel magnetic field sweep. Right panel: Plot of the resonance frequency vs. magnetic field.

From fitted data we extracted the loaded Q factor to be 10,0056 and the resonance frequency of 5.265 GHz (Fig. 3.8). The fit was done on a linear scale rather than a logarithmic scale since it was easier to fit since the full width half maximum is defined on a linear scale.

We loaded an identical silicon resonator, *V_res_Si_A*2, but this time it was bonded with many bonds to a conecting ground plane that was connected on the cQED board v2 to the larger ground plane through soldered capacitors and resistor. This would be the ideal bonding scheme for our sample as then we can use the on board bias tee to float the ground plane as a large accumulation gate. The bonding scheme can be seen in Fig. 3.5 (right panel). The resonance in this sample (Fig. 3.10) is wider and more asymmetrical when compared to the resonance in Fig. 3.6. This hints that bonds directly to the larger ground plane may be preferable. We can also see that transmitted power is lower than expected, which could be due to the bonding: if the resonator does not see the ground plane as an infinite ground plane power may be dissipated.

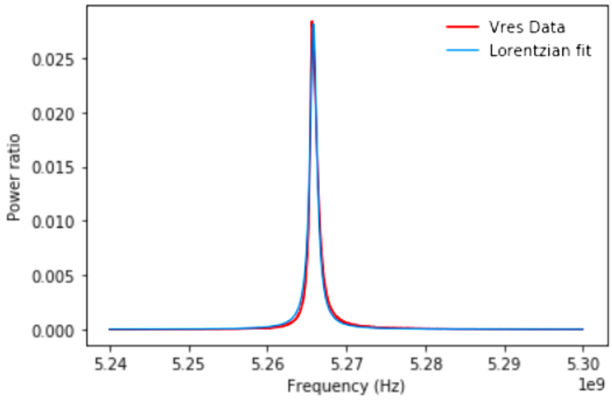

FIGURE 3.8: Lorentzian fit to the S21 transmission data of $V\_res\_Si\_A1$ sample. The loaded Q factor is equal to 10,056.

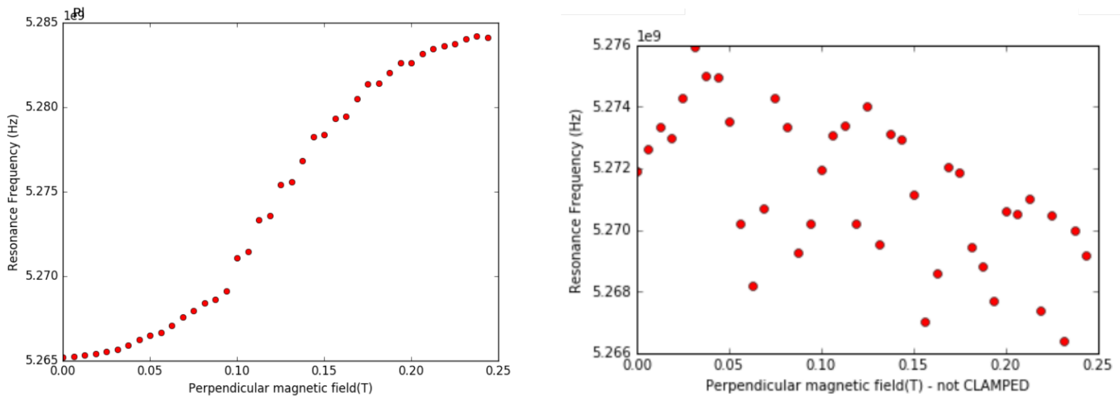

FIGURE 3.9: Resonance frequency vs. perpendicular magnetic field sweep for $V\_res\_Si\_A1$ sample with all other parameters on CLMP (left panel) and on HOLD (right). Right panel shows more noisy data.

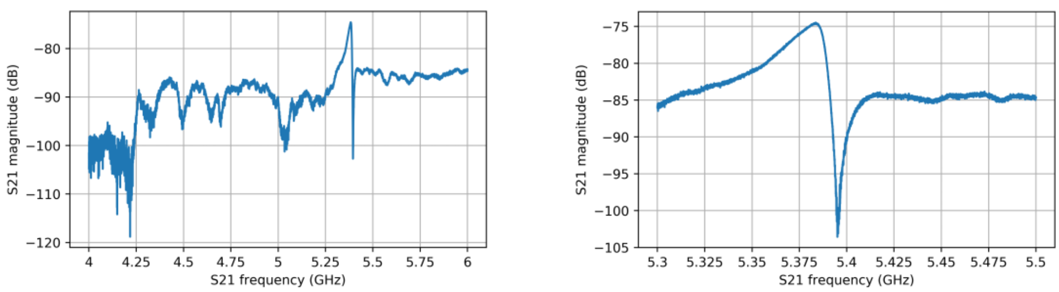

FIGURE 3.10: S21 Transmission for $V\_res\_Si\_A2$ sample with -20 dB input power, taken with 5000 points and 1000 averages (left panel). Zoom into resonance frequency at 5.78 GHz showing an asymetric resonance peak (right panel).

3.3 NbTiN resonator on etched silicon-germanium

The second task was to test the identical resonator design on etched silicon-germanium to see if the substrate change makes a difference. This was bonded straight to the larger ground plane. The S21 transmission can be seen in Fig. 3.11 (left panel) and the parallel magnetic field sweep in Fig. 3.11 (right panel). We had the impression that at 5.25 GHz there could be a resonance peak, but since the peak did not move with magnetic field we speculate whether this was a resonance mode on the chip.

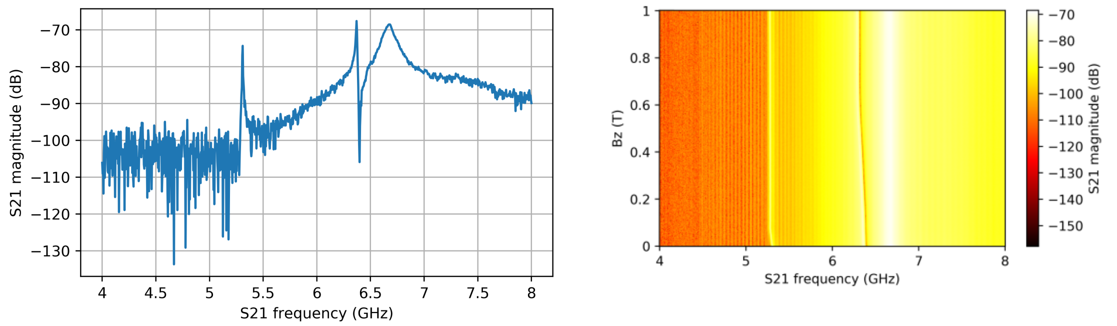

FIGURE 3.11: Raw data for $V\_res\_SiGe\_Ae3$ sample. Left panel: S21 Transmission with -10 dB input power, taken with 1000 points and 100 averages. Right panel: parallel magnetic field sweep.

This was confirmed when we tested the same design with the new bonding scheme of bonding with a lot of bonds to the real ground plane. We saw no resonance and lower S21 transmission compared to what we expected of both the resonator and the strip line (Fig. 3.12). This could be due to an unoptimized etch to the silicon well which left a rough substrate.

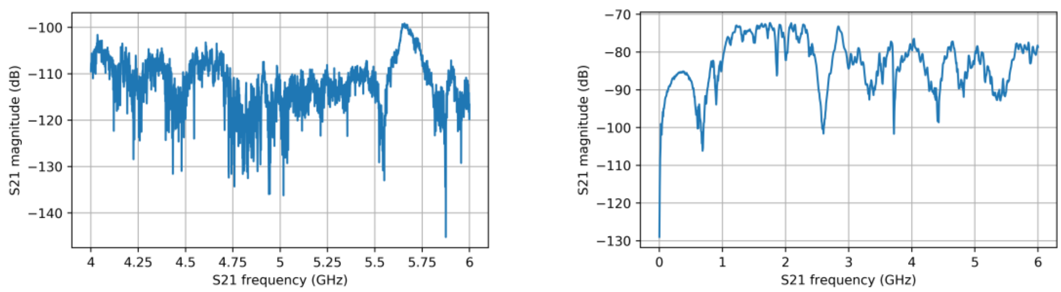

FIGURE 3.12: S21 transmission for $V\_res\_SiGe\_Ae3$ sample. Left panel: S21 Transmission with -10dB input power, taken with 2000 points and 5000 averages. Right panel: S21 Transmission of feedline with -10dB input power, taken with 1000 points and 1000 averages.

3.4 NbTiN resonator on implanted silicon-germanium

The same design was tested on an implanted Si/SiGe substrate with the quantum well intact with accumulation gates and ohmics on the same layer as the resonator. Its recipe is given in details in Appendix C. For information on another tested sample, $V\_res\_SiGe\_A1$, which did not show a resonance refer to Appendix F. The bonding scheme and bonding image for $V\_res\_SiGe\_A3$ can be seen in Fig. 3.13.

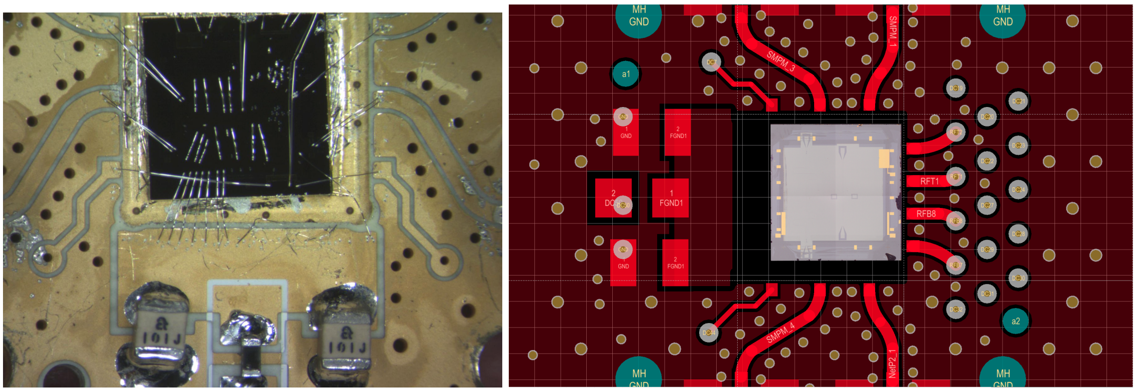

FIGURE 3.13: Bonding image (left panel) and scheme (right panel) for *V_res_SiGe_A3* sample.

Fig. 3.14 (right panel) shows the transmission measurements that indicate a sharp peak at 4.837 GHz which was fitted to give the Q factor of 17,528. However, it can be argued that this is an aritificial Q since we applied -10 dBm of power, while other groups saw a resonance at single photon level powers of around -120 dBm [22]. The resonance was identified due to its movement in parallel and perpendicular magnetic field as seen in Fig. 3.15.

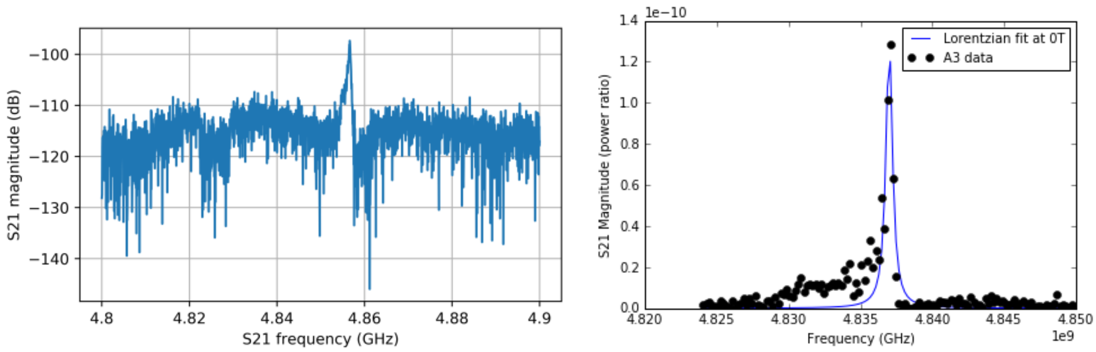

FIGURE 3.14: Raw and fitted S21 transmission data for *V_res_SiGe_A3* sample. Left panel: S21 transmission with -10 dBm input power, 2000 points with 500 averages. This is plotted on a logarithmic power scale. Right panel: Lorentzian fit of resonance peak of at zero field with extracted loaded Q factor of 17,528 and a resonance frequency of 4.837 GHz. This is plotted on a linear scale.

In order to understand how the resonance frequency and the Q factor changed with parallel magnetic field we took samples of magnetic field spaced 0.02 T apart, fitted Lorentzian to the resonance peak at that point, and extracted the Q factor. Fig. 3.16 shows that at 0.02 T the resonance has a jump to the right but returns to the left of the original resonance peak as the parallel magnetic sweep continues. It should also be noted that while the resonance at zero field has a Q factor of around 17,000 this drops at 0.02 T to around 5000 and stays of this order of magnitude for the rest of the sweep.

We also did DC measurements which can be seen in Fig. 3.17. We applied 0.1 mV on the source ohmic, connected the drain ohmic to ground and then changed the voltage on the overlapping top gate, which in these figures was gate 2. The fact that we do not see any current from the source ohmic to drain ohmic indicates that the 2DEG is not accumulated by the top gate. The same experiment was done on the other two gates and gave the same result. This could be because of the way the ALD was applied: we applied it twice, removing it the first time through HF dipping. This could have caused residues to remain that prevented the ohmics from getting contact to the quantum well. We also did not see any effect on the resonance when biasing the ground plane from -2V to 2V.

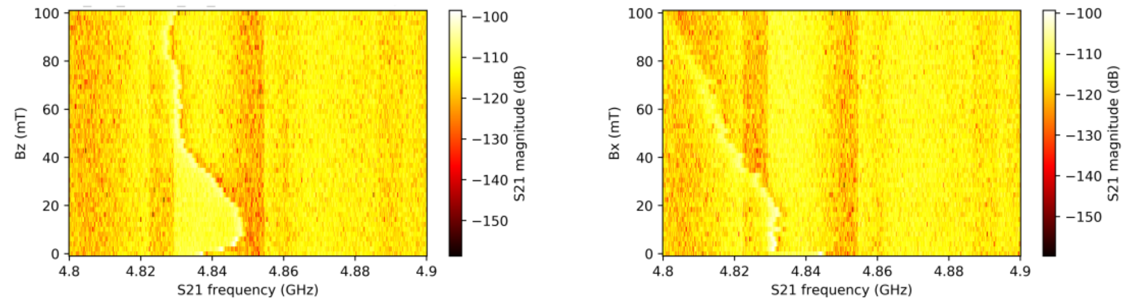

FIGURE 3.15: Magnetic field sweeps for *V_res_SiGe_A3* sample: Parallel magnetic field (Bz) sweep (left panel) and perpendicular magnetic field (Bx) sweep (right panel).

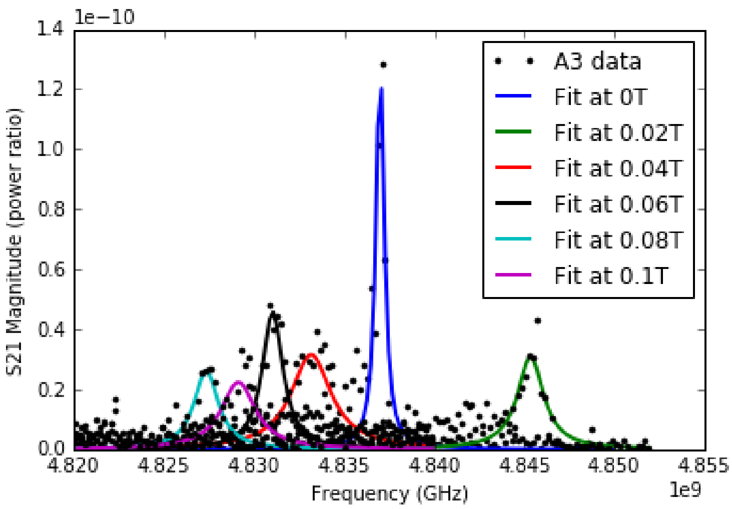

FIGURE 3.16: Lorentzian fit to S21 transmission for *V_res_SiGe_A3* sample at 6 different parallel magnetic field applied on the sample.

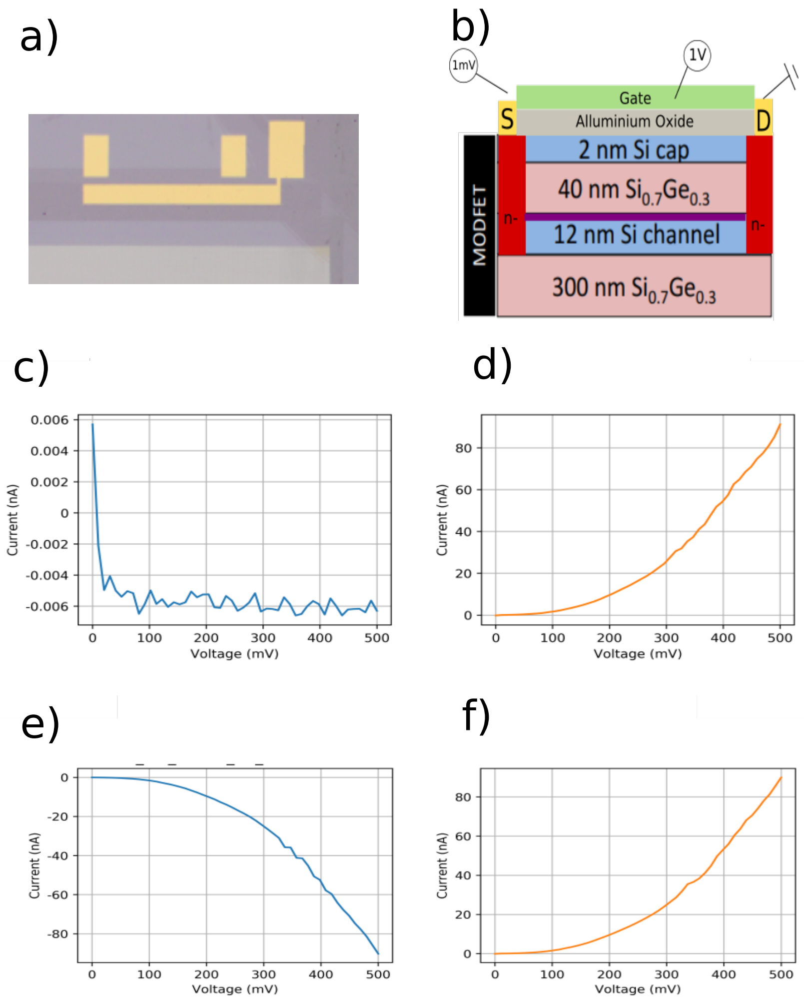

FIGURE 3.17: a) Shows an optical image of the gate and ohmics and their position on the ALD. (b) Cut through heterostructure showing the ohmics and accumulation gate with relation to the implantation region and silicon well in the Si/SiGe heterostructure). DC measurements for *V_res_SiGe_A3* sample with ohmic 31: (c) Current measurement on ohmic 33 while voltage increased from 0 to 500 mV on gate 2 and (d) Current measurement of gate 2 while voltage is being applied. We see a very small leakage however, we also do not see a stable current that would indicate that a 2DEG is accumulated. DC measurements for *V_res_SiGe_A3* sample with ohmic 31: (e) Current measurement on Ohmic 33 while voltage increased from 0 to 500 mV on gate 2 and (f) Current measurement of gate 2 while voltage is being applied. We see a leakage proportional to the current applied on the gate.

Chapter 4

Conclusion

4.1 Discussion

We showed that the fabrication of a resonator with a Q factor of the order 10^3 is possible on Si/SiGe with the quantum well intact, which has not been shown beofre. However questions remain. One question is how to increase the Q factor to a value of 10^5, as has recently been achieved in a paper on strong spin/photon coupling [25]. Secondly, why the resonator on etched silicon germanium showed no resonance, even though groups report a stategy of etching away the quantum well to increase resonator performance [16]. Thirdly it is not clear why we were not able to accumulate electrons in the quantum well underneath the resonator, even though none of the gates showed leakage on one of the devices.

In order to answer the first question we need to find out what is the limiting factor on our Q. In order to be able to say that we see a "low" Q factor we need to simulate the input and output capacitances and extract the intrinsic Q factor of the resonator. This can be done by modelling the S21 transmission given by the formula (1.10) and extracting the external Q factor. This can be done using python or more advanced visual modelling software such as CST and would give a more quantitative comparison, however this was not done for this thesis.

Recently various resonator designs were tested by Mi et al. in order to test whether Q limitations were due to the design or fabrication process. The resonators fabricated can be seen in Fig. 4.1 and the corresponding results in Fig. 4.2.

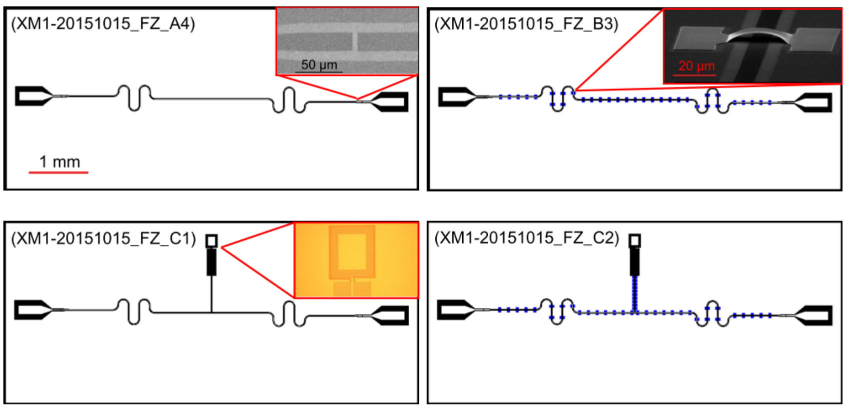

FIGURE 4.1: Design of four different resonators made by Jason Petta's group (Princeton, US). There are respectively added air bridges, LC filtered DC tap, and DC tap with air bridges to find what the limiting factor is for the Q factor. Reproduced from [18].

Their conclusion was that the resonators had an almost identical Q factor of 20,000 at T= 20 mK and a power of -128 dBm. This indicates that the dominant loss mechanism was fabrication

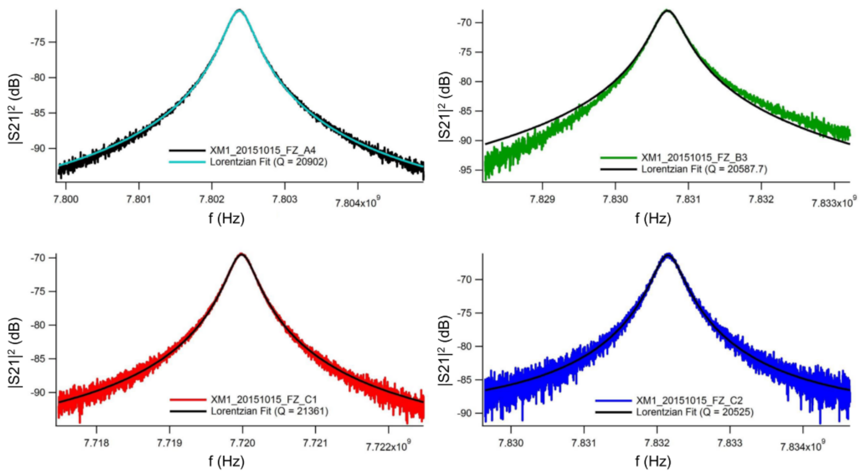

FIGURE 4.2: S21 transmission of XM1 resonators showing almost identical curves indicating that the Q factors for the different designs are the same. Reproduced from [18].

rather than design. They attribute this fabrication related loss mechanism to TLSs. This is a loss mechanism due to fluctuations in two level systems that can be related to defects in the interfaces between metal and dielectric, as well as dielectric and dielectric interfaces which at low temperatures will tunnel between the interfaces. TLSs saturate at a high power, which could explain why we see a resonance at a high power of -20 dBm but not below. Xiao Mi (Princeton University, US) attributes the main source of TLS fluctuations to a layer of aluminum oxide which lies below their resonator, which when removed leads to a Q factor of around 300,000. This is an important observation, and it is possible that dirty remains under our resonator could be causing a similar drop in Q factor [18, 28].

However, Xiao Mi et al. (Princeton University, US) used a significantly different fabrication process. Firstly, they used 50 nm of Nb film to pattern the resonator, while we used 22 nm of NbTiN which should iincrease in kinetic inductance to make a higher impedance cavity. However, we did not do a Piranha etch to clean the chip before patterning which may be worth trying [16].

When comparing designs LC filters (Fig. 4.3) can be used to reduce microwave leakage and have been shown to increae the Q to 100,000. Thus, we could substantially increase the Q in our design by using LC filters in the bias tab.

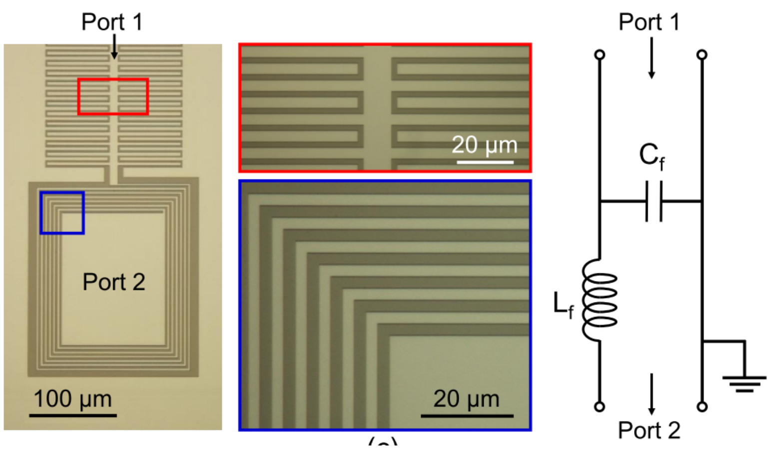

FIGURE 4.3: Left panel: Optical image of a compact LC-filter showing the spiral inductor and a portion of the capacitor. Right panel: Zoomed-in view of the capacitor (red outline)/inductor (blue outline). Reproduced from [16].

The second question to address is the effect of the quantum well on the resonator. In gallium arsenide quantum wells below the resonator center pin needed to be etched away due to resistive loss due to the 2DEG electrons. Xiao Mi et al. noticed that at 4.2 K the quality factor of the bare resonator on implanted degrades from 1000 to 100 once a DC bias of 0.4 V is applied, however this went away at mK temperatures. This is consistent with our data, since we saw a resonance on an implanted Si/SiGe chip at mK temperatures. It is strange that we did not see a resonance on the etched silicon-germanium since Jason Petta's group (Princeton, US), for example, has specifically been etching away the well in order to avoid potential complications. This can be attributed to a non-optimized well etching process [18].

Lack of accumulation could be due to ALD issues in the fabrication process since the ALD was applied twice. While we removed the first layer of ALD using HF etching, it is possible that remains were left and, thus– the ohmics did not make good contact to the quantum well.

4.2 Outlook

An interesting use for resonators is fast and on demand initialization of quantum degrees of freedom of qubits. This is especially important for quantum error correction codes that require frequent initialization of qubits during computation. A combination of two resonators can be used as a tunable heat sink that could potentially be the key to actively initializing superconducting or semiconducting qubits [29]. This is done by fabrication two coupled resonators as seen in Fig. 4.4.

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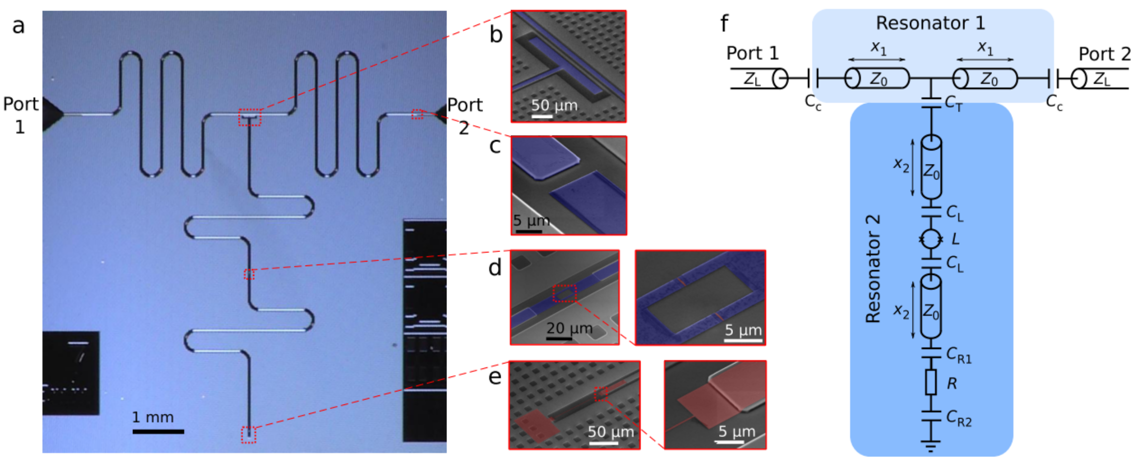

FIGURE 4.4: Schematic illustration of the setup for long distance interaction. Reproduced from [29].

The first resonator has a high quality factor and a fixed frequency – much like the resonator design fabricated in this thesis. The second resonator is designed to have a low quality factor and a tunable frequency. This is done by fabricating an on-chip resistor and the tunability is achieved by using a SQUID (superconducting quantum interference device). When these resonators are in resonance the high Q resonator can be effectively dissipated. The experiments showed that by using the scheme in Fig. 4.4 it is possible to tune a 10^5 Q resonator down to 1000 Q, while not inherently degrading the Q of the resonator, which will need to be high to couple to the qubits. An interesting detail with this device, which was fabricated at VTT (Technical Research Centre of Finland), is that the resonator has a Q of order 10^5 at an input power as low as -140 dB which is equivalent to having a single photon in the cavity. If compared to our resonator, we had to ramp up the input power to as high as -10 dB in order to see a resonance of order 10^3. Here is it perhaps useful to look at their fabrication process in comparison to ours, which has the following key differences:

- hexamethyldisilazane priming
- Ion etching
- Pattern exposed using electron beam lithography

In order to achieve higher Q factors it may be worth attempting to use one or more of their fabrication techniques with 50 nm of NbTiN rather than their 200 nm of Nb. A thinner film not only increases the coupling rate but can also lead to less degregation of Q due to magnetic field by better aligning it with the field [23].

4.3 Summary

Table 4.1 shows a summary of our results.

TABLE 4.1: Summary of properties of our resonators on different substrates

Substrate	Q factor	Resonance frequency
Si	10,056	5.265 GHz
SiGe with quantum well etched	Not identified	Not identified
Si/SiGe with quantum well intact	17,528	4.837 GHz

It can be seen that the $\lambda/2$ NbTiN design showed a resonance on a silicon wafer, and on a Si/SiGe heterostructure with the quantum well intact. This indicates that it is not necessary to etch away the quantum well underneath a resonator on heterostructures for semiconducting quantum dots. This is further supported by the lack of resonance on the Si/SiGe substrate with the quantum well etched away indicating that the Q factor was perhaps too low. Moving from the silicon substrate to the Si/SiGe substrate moved the resonance frequency to a lower value, however had no negative influence on the Q factor. DC measurements on the Si/SiGe heterostructure showed that a 2DEG was not accumulated in the quantum well as there was no current from the source to drain ohmic when voltage was applied to the top gate. This indicates that further work needs to be done on ensuring that the 2DEG accumulates, such as implantation and ALD deposition improvements. As mentioned in the discussion the Q factor can also be improved in a number of ways, such as aggressive cleaning of the chip before resonator deposition, LC filters and perhaps using an etch instead of a liftoff process, though this thesis has shown that a liftoff process also works for making a resonator with a Q factor of order 10^3.

Appendix A

Theory

A.1 Superconductivity

The CPW resonator fabricated in this thesis is made from NbTiN which is a superconducting metal. The characterisation of the resonator relies on its properties as a superconductor. Superconductivity was discovered by Heike Kamerlingh Onnes in 1911 when he saw mercury loosing resistivity in an abrupt manner below a certain temperature. This could not be explained by the Drude model, which modelled the metal as a gas of almost non interacting particles. BCS theory explained this phenomenon by applying quantum mechanics to conductivity. In this theory superconductivity is explained as electrons forming pairs below a certain temperature due to an indirect interaction with the lattice of electron-induced phonons. At this point the resistivity drops to zero because the electrons are now bounded to each other [30].

A.2 Resonator losses

There are two important sources of loss in a coplanar waveguide resonator which are useful in understanding the magnetic field's effect on the resonator. The first source of loss is kinetic inductance. In a superconductor where there is no resistivity the effects of inductance become important. The total inductance per unit length of a resonator can be described as:

$$L_l = L_m + L_k \, , \tag{A.1}$$

where L_m is the magnetic inductance due to an induced or external magnetic flux and L_k is the inductance of the charge carriers in the superconductor. The equations for each of them are as follows:

$$L_m = \frac{\mu K(k')}{4K(k)} \, , \tag{A.2}$$

where K is an elleptical integral and:

$$k_0 = \frac{a}{a+2s} \, , \tag{A.3}$$

$$k_0' = \sqrt{1-k_0^2} \, . \tag{A.4}$$

The kinetic inductance is given as:

$$L_k = \frac{\mu \lambda_L^2}{at} g(a,s,t) \, . \tag{A.5}$$

Both inductances depend on the geometry of the resonator (a, s, t) and λ_L which is the London penetrator depth that characterizes how far a magnetic field penetrates into a superconductor.

Optimally, the film thickness should be less than the penetration depth. For example, the penetration depth for NiTiN is 39 nm, thus, using a thickness of 22 nm is better than 100 nm thickness [7].

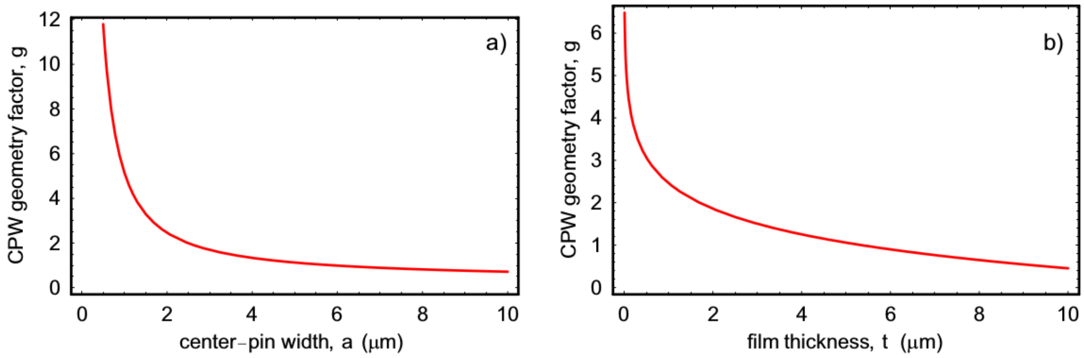

FIGURE A.1: Kinetic inductance vs. center-pin width (left panel) and film thickness (right panel). The kinetic inductance depends on the geometry of the resonator. Reproduced from [7].

The second important source of loss in the resonator is due to Abrikosov vortices that are formed in the superconductor due to applied magnetic field. The CPW used in this experiment is made out of NbTiN which is a type-II superconductor. This means that the field enters the superconductor as flux lines with a quantum of magnetic flux $\Phi_0 = h/2e$. At the center of the lines the cooper pair density goes to zero and creates a vortex. These vortices arrange themselves into a pattern in the film (Fig. A.2). Their separation is given by:

$$a = 1.075\sqrt{\Phi_0 B}\,, \tag{A.6}$$

where B is the applied magnetic field.

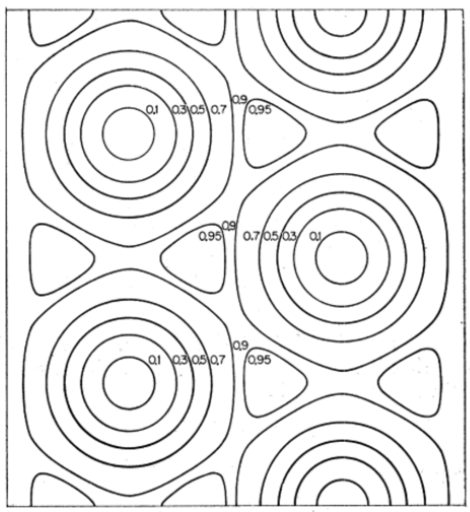

FIGURE A.2: Contour diagram of Φ^2 solutions of the Ginzburg-Landau equations just below the upper critical field. Reproduced from [24].

Vortices occur in less energetically favorable sites of the superconductor. This is why it is important to clean the sample as thoroughly as possible before cool down. However, introducing artificial pinning sites in the form of small holes in the ground plane increased the internal Q factor and allowed the resonance to survive higher applied magnetic fields (up to 5.5 T) [24].

The magnetic field influences the resonance frequency and quality factor. Abrikosov vortices forming in the plane of the resonator as the magnetic field enters the resonator explain the decrease in the Q factor. Resonance frequency changes with magnetic field due to a change in kinetic inductance which is proportional to the magnetic field [27]. This was documented experimentally: Fig. A.3, for example, shows the effect of magnetic field on an NbTiN resonator of different thicknesses.

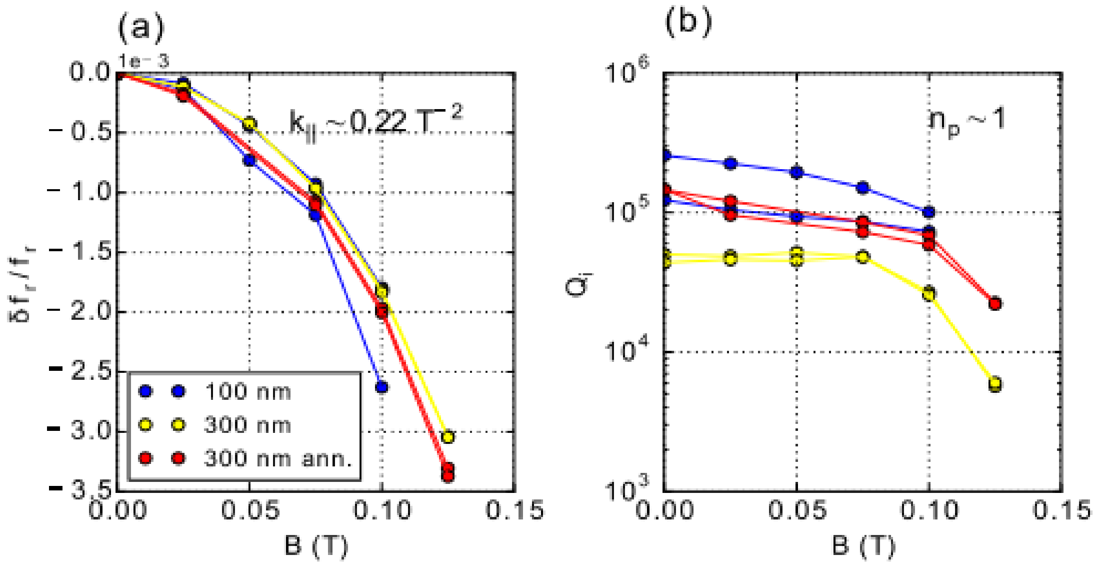

FIGURE A.3: Resonance frequency shift (a) and the Q factor (b) as a function of parallel magnetic field for NbTiN resonators of various film thicknesses. Reproduced from [24].

A.3 Coupling spin qubits with resonator

The energy of an LC oscillator can be expressed as the following Hamiltonian:

$$H = \frac{q^2}{2C} + \frac{\delta^2}{2L}\,, \tag{A.7}$$

where q is the charge in the capacitor and $\delta = LI$ is the flux in the inductor.

A Hamiltonian for a particle in a a harmonic potential is:

$$H = \frac{p}{2m} + \frac{1}{2}m\omega^2 x^2\,, \tag{A.8}$$

where the analogy to the electrical oscillator can be drawn: the charge is the momentum and the flux is the position and $w = \frac{1}{LC}$.

This Hamiltonian can also be expressed in terms of operators:

$$H = \hbar\omega(a^{\dagger}a + \frac{1}{2})\,, \tag{A.9}$$

where a is the photon annihilation operator that can be related back to the flux and charge of the electric oscillator [7].

A single electron functioning as a charge qubit is desribed by:

$$H_a = \frac{1}{2} f_a \sigma_z \;, \tag{A.10}$$

where the qubit transition frequency is:

$$f_a = \sqrt{\epsilon^2 + 4t_c^2}/h \tag{A.11}$$

with ϵ being the DQD energy level detuning and t_c is the interdot tunnel coupling.

The interaction Hamiltonian between these two systems is given by:

$$H_{int} = h(g_c/2\pi) sin\theta (a^\dagger \sigma^- + a\sigma^+) \;, \tag{A.12}$$

where g_c is the charge photon coupling rate and $sin\theta$ is related to the energy and tunnel coupling rate as in [18]:

$$sin\theta = 2t_c/\sqrt{\epsilon^2 + 4t_c^2} \;. \tag{A.13}$$

Appendix B

Design

As mentioned in the main text, coplanar waveguides can have their impedance value adjusted by changing their geometry. The impedance is defined as:

$$Z_{CPW} = \frac{60\pi}{\sqrt{\epsilon_{eff}}}\left(\frac{K(k)}{K(k')} + \frac{K(k_3)}{K(k_3')}\right), \tag{B.1}$$

where K is the complete elliptical integral of the first kind. It depends on the ratio between the strip and the gap, the thickness of the substrate, and the dielectric constant of the substrate (for silicon it is equal to 11.48) [31].

However, a more detailed model also takes into account the kinetic inductance of the superconducting material. Z_{CPW} can also be defined as:

$$Z_{CPW} = \sqrt{\frac{L_k + L_g}{C}}, \tag{B.2}$$

where the kinetic inductance L_k is

$$L_k = \frac{\mu_0 \lambda}{\pi^2 \omega} log\left(\frac{4\omega}{t}\right)\frac{sinh(t/\lambda)}{cosh(t/\lambda) - 1} \tag{B.3}$$

and depends on the center strip width w and the strip thickness t.

The original geometry of the design used in this experiment was Karl Petersson's $\lambda/2$ resonator (Princeton, US) where for a 100 nm thick NbTiN film, the parameters were:

$$\begin{aligned} \omega &= 15\ \mu m \\ g &= 4\ \mu m \\ L_k &= 7.6 \cdot 10^-7\ H/m \\ C &= 3.7 \cdot 10^{-10}\ F/m \end{aligned} \tag{B.4}$$

However it was suggested that in thicker films there is a degradation of the Q factor due to the field not being aligned completely parallel to the chip. Thus reducing the thickness of the strip will increase the Q factor. This will also increase the kinetic inductance of the superconductor which is discussed in the main text. The following parameters were developed for a superconducting resonator made from 22 nm of NbTiN [23]:

$$\begin{aligned} \omega &= 30\ \mu m \\ g &= 1.5\ \mu m \\ L_k &= 4.2\ nH \\ C &= 1.4\ pF \end{aligned} \tag{B.5}$$

with a length of 5650 μm which should fit exactly half a microwave wavelength which is around 1 mm.

These parameters were used in our design and were tested on a resonator produced by Thorvald Larsen (Fig. B.1). The resonator is designed to be a $\lambda/4$ resonator and should, thus, have 8 dips at different frequencies between 7 and 9 GHz.

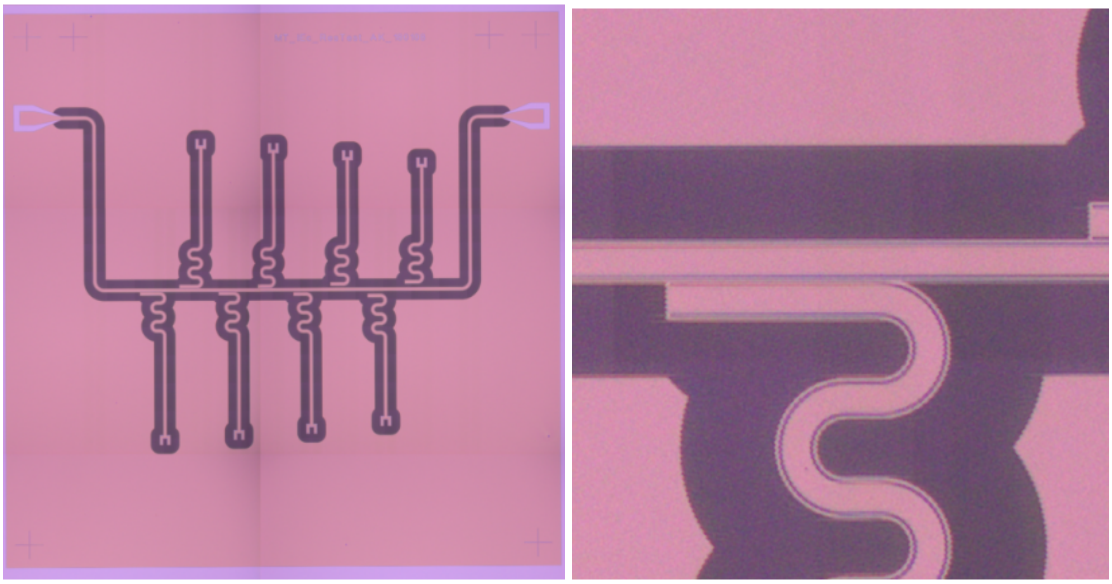

FIGURE B.1: Optical image of *T_res* design.

We can find a resonance frequency expression based on the geometry of the resonator and the parameters of the film. For a $\lambda/4$ resonator the resonance frequency is given in [17, 24] as

$$f = \frac{1}{4l\sqrt{L_k + L_g C}}, \tag{B.6}$$

where a L_k is the kinetic inductance and L_g is the magnetic inductance.

In this thesis we aimed to make a $\lambda/2$ transmission line resonator that behaves as a parallel resonant circuit when the length is $\lambda/2n$. Thorvald's resonator design, however, is a $\lambda/4$ resonator. It is made by fabricating a $\lambda/4$ meandering transmission line capacitively coupled to a feedline along which the high frequency signal propagates. In our design we have the parameters from B.5.

Appendix C

Fabrication

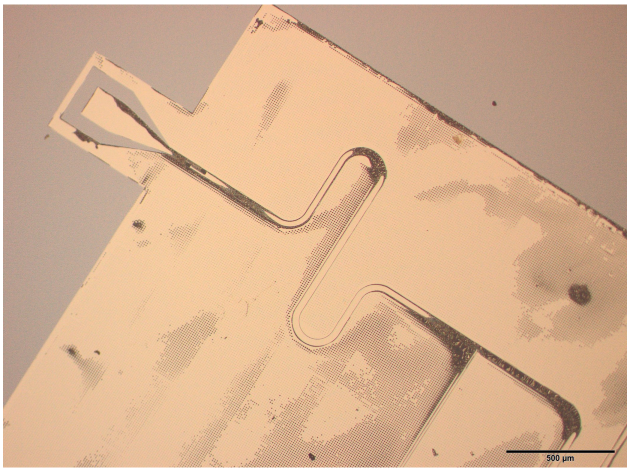

FIGURE C.1: Photos of failed liftoff process due to not ashing before sputtering.

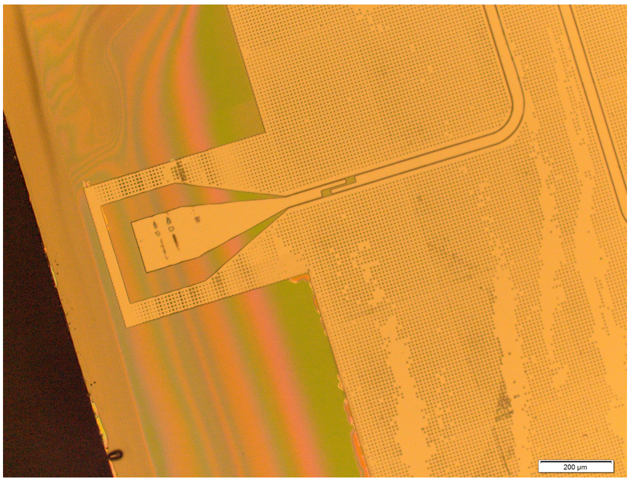

FIGURE C.2: Photo of failed development of Si/SiGeA 4×4 mm chip with inhomogeneous resist.

C.1 Heidelberg optical lithography exposure

In order to expose the design in the Heidelberg photolithography machine the file should be converted to a DXF or GDSII which are compatible with design software such as AutoCAD, Klayout and Clewin all of which are installed on the design room computers at the Center for Quantum

Devices. If a negative design is needed the software beamer can be used to subtract layers from each other.

In order to do alignment in the Heidelberg photolithography machine the chip should have alignment marks. These are exposed first using mask edge alignment and sputtered with NbTiN. These can then be used to expose the rest of the design in the correct place on the chip.

By using the manual alignment function in the Heidelberg photolithography machine one can specify how many alignment marks are on the chip, give their coordinates and locate them one by one on the chip giving the Heidelberg photolithography machine an idea of where to expose the DXF design. It is important that the chip initially used for the mask edge alignment is square. If the chip has a different shape the alignment marks will not be parallel to the edges. This also means that the chip will need to be laser cleaved at DTU (Lyngby, Denmark), which increases the time of the process.

C.2 ALD deposition

To insulate gates from the substrate underneath, one needs to deposit 10 nm of Al_2O_3 on the substrate and then either use liftoff or etching in order to leave the oxide in the particular regions. ALD (atomic layer deposition) is a method that deposits one atomic layer at a time. This is a three step process. First, the TMA pre cursor is pumped into the ALD chamber and bonds to the hydroxyl groups on the surface of the substrate. This reaction releases methane which causes the reaction to be self-limiting as the TMA does not bind to the methane. Then the chamber should be flushed with water which will bond to the free bonds on the surface of the substrate and form a layer of Al_2O_3. This is done over 100 cycles which takes around 6 hours, with the TMA precursor being pulsed for 0.1 s with 60 s waiting time and then the pulsing of water for 0.1 s [32].

C.3 Sputtering and evaporation

During sputtering gaseous plasma is created and ions are accelerated from the plasma to the source material which is usually a crucible with the metal to be sputtered. The plasma particles have enough energy to eject neutral metal particles and they travel to the vacuum chamber until they hit the substrate and coat it with a thin film of the metal [33]. We used the DC energy source and coated the silicon wafer with 20 nm of NbTiN.

Another useful technique is evaporation: an intense electron beam is generated from a filament and steered via electric/magnetic fields to the source material which is the metal we want to evaporate onto the chip. The heat surface of the atoms is enough that they leave the surface and coat the substrate in a similar fashion to the sputtering. On our sample we first did Kaufman milling to remove the silicon oxide and then evaporated 5 nm Ti as a sticking layer and 75 nm Au in order to make the gates and accumulation gates [34].

C.4 Fabrication recipes

Before implantation

Deposition of alignment marks

- Cleave 12×12 mm SiGe chip
- Clean it in dioxolane and IPA then ash it for 4 min and post bake it at 185°C
- Spinning with LOR3B at 4000 rpm and baking for 4 min at 185°C

- Spinning with Az1505 at 4000 rpm and baking for 2 min at 115°C
- Exposure of ALD design using Heidelberg photolithography machine, 22 ms exposure time and -2 defocusing using optical focus
- Development 35 s in MF321
- Hold in MilliQ 35 s
- Ashing 4 min
- Metalize with NbTiN sputtering. Deposit around 20 nm – recipe with 3.5 min
- Leave in NMP hotbath at 85C for one hour (thermal shock is important, make sure that NMP is already at 85°C when submerging chip)
- Put in IPA and look through the microscope to make sure everything is lifted off before drying

Exposure of alignment regions

- Clean it in dioxolane and IPA then ash it for 4 min and post bake it at 185°C
- Spinning with LOR3B at 4000 rpm and baking for 4 min at 185°C
- Spinning with Az1505 at 4000 rpm and baking for 2 min at 115°C
- Exposure of ALD design using Heidelberg photolithography machine, 22 ms exposure time and -2 defocussing using optical focus
- Development 35 s in MF321
- Hold in MilliQ 35 s
- Ashing for 4 min

After implantation

After arrival

- Strip resist using hot NMP at 85°C for 1 hour
- Ash for 2 min and put in RTP sample holder
- Anneal using the RTA

ALD deposition

- Cleam om Acetone + IPA + Ashing 4 min
- ALD deposition, in ALD 1, of 10 nm of Al2O3 at 90°C, pulsing TMA precursor for 0.1 s and waiting 60 s and then pulsing water for 0.1 s and waiting for 60 s. 100 cycles, which correspond to 10 nm.
- Ashing for 4 min

ALD etching

- Spinning with Az1505 at 4000 rpm and baking for 2 min at 115°C
- Exposure of ALD design using Heidelberg photolithography machine, 22 ms exposure time and -2 defocussing
- Development for 1 min 20 s in MF321
- Hold in MilliQ for 35 s
- Ashing for 4 min
- Post baking at 125°C for 2 min
- Etching in HF for 5 min

Resonator Fabrication

- Spinning with Az1505 at 4000 rpm and baking for 2 min at 115°C
- Exposure of ALD design using Heidelberg photolithography machine, 22 ms exposure time and -2 defocussing using optical focus
- Development for 41 s in MF321
- Hold in MilliQ for 35 s
- Ashing for 4 min
- Metalize with NbTiN sputtering. Deposit around 20 nm – recipe with 3.5 min
- Leave in NMP hotbath at 85°C for 1 hour (thermal shock is important, make sure that NMP is already at 85°C when submerging chip)
- Put in IPA and look through the microscope to make sure everything is lifted off before drying

Accumulation gate deposition

- Spinning with Az1505 at 4000 rpm and baking for 2 min at 115°C
- Exposure of Ohmic design using Heidelberg photolithography machine, 22 ms exposure time and -2 defocussing using optical focus
- Development for 41 s in MF321
- Hold in MilliQ for 35 s
- Ashing for 4 min
- Evaporation using the AJA - 5 nm Ti and 75 nm Au, 22.5, 42.5, 1,3
- Lift off in hot NMP (1 hour)
- Ashing for 4 min

Gold Ohmic deposition

- Spinning with Az1505 at 4000 rpm and baking for 2 min at 115°C
- Exposure of Ohmic design using Heidelberg photolithography machine, 22 ms exposure time and -2 defocussing using optical focus
- Development for 41 s in MF321
- Hold in MilliQ for 35 s
- Ashing for 4 min
- Kauffman milling of SiO2, 300 V in AJA2
- Evaporation using the AJA - 5 nm Ti and 75 nm Au, 22.5, 42.5, 1,3
- Lift off in hot NMP (1 hour)
- Ashing for 4 min

NbTiN cleaning from silicon substrate

- Add 100 ml H_2O to small beaker
- Add 10 ml NH_4OH to the same beaker
- Put small beaker inside bigger empty beaker and put it inside the hot bath
- Heat the hot tub to 80°C and check with a thermometer when the water is at 60°C
- Take the small beaker off when the desired temperature is reached
- Add 20ml H_2O_2 to small beaker, see when it bubbles
- Put in chips to be cleaned immediately for 1–1.5 min
- Transfer chips to MilliQ water
- Let cool and transfer to X-waste

Appendix D

Measurements

D.1 Fridge electronics

All the DC and coax lines have to pass from the puck, through all the cooling parts of the fridge, attenuators and amplifiers and come out the top of the fridge. There are 48 DC lines that are used to probe the chip electronically. They are all combined in the cold finger to fit into a nano-D connector which connects through the puck and into the nano-D connector in the board. Inside the fridge they pass through two electrical filters that are on the mixing chamber which help reduce high frequency noise and help reduce the energy of the room temperature electrons before they reach the sample. Then they pass through "bobbins" which provide thermal contact and are on top of the mixing chamber and should always be around 20 mK when the fridge is cold.

When the DC lines come outside the fridge they are plugged into a "break out box" which has a BNC connector for each of the lines and can be in the three following configurations: "ground", "on" and "bias". The ground configuration connects that DC line to the fridge ground, and the on configuration connects it to electronics such as the "Keithly" which can send in voltage and measure the current. The bias line allows multiple lines to be floated at the same time.

The coaxial lines have a different configuration inside the fridge and pass through RF attenuators which are used to reduce the energy of the electrons and make sure that too much input power is not going into the fridge which can heat up parts of the fridge. There are 14 SMP bullet connectors into the cold finger in the puck, where 13 are fast lines and on is the reflectometry line [35].

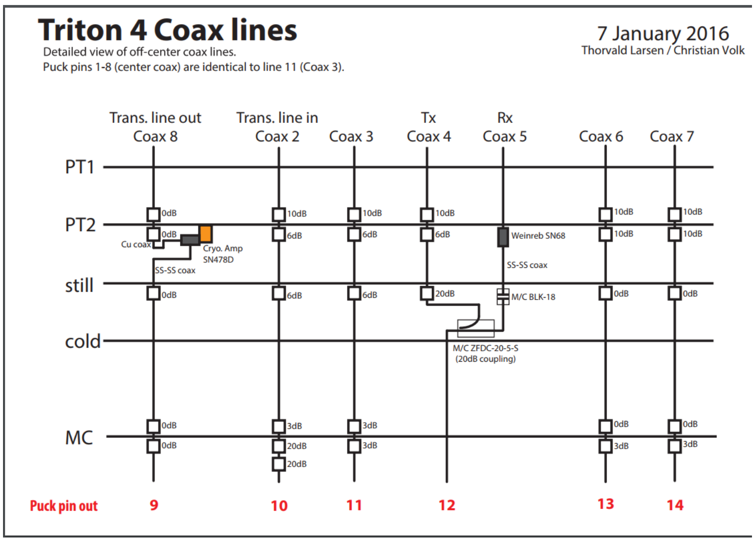

FIGURE D.1: Schematic illustration of coaxial line setup in T4. For measurement we used lines 5 and 11, using this figure as a reference for their attenuation. Reproduced from T4 Wiki.

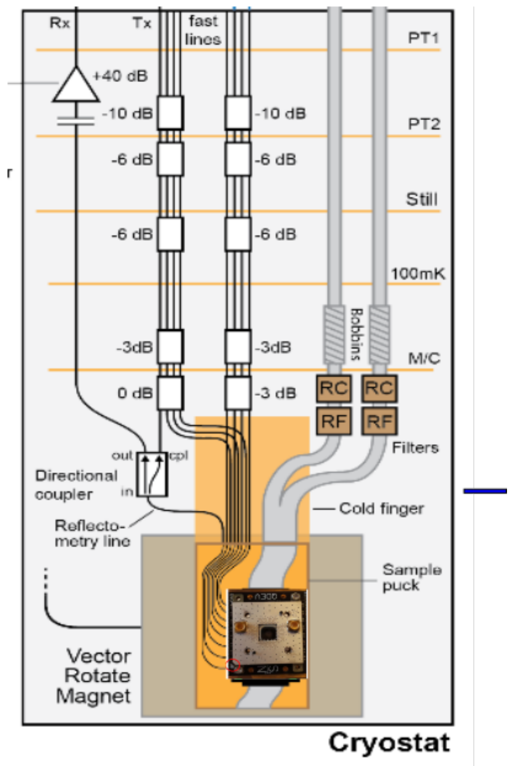

FIGURE D.2: Schematic illustration of fridge electronics connected to the sample. Reproduced from [35].

D.2 Qcodes code for resonator measurements

```
Created on Sat Mar  3 12:26:16 2018

@author: Triton4acq

#Running init file first, remember to initialize all instruments
"""
ZNB.rf_on()
ZNB.channels.S21.start(4.8e9)
ZNB.channels.S21.stop(4.9e9)
ZNB.channels.S21.npts(500)
ZNB.channels.S21.avg(5000)
ZNB.channels.S21.power(-10)

do0d(ZNB.channels.S21.trace)# Doing a 1D trace

do1d(keith.smua.volt,-2,2,50,0.1,ZNB.channels.S21.trace)

magnet.z_ACTN('HOLD')# Setting up the magnet, important
#that the axis you want to sweep in on hold
magnet.y_ACTN('CLMP')
magnet.x_ACTN('CLMP')

do1d(magnet.z_fld,0.1,-0.025,50,12,ZNB.channels.S21.trace)
```

```
magnet.z_fld(0) #Remember to set magnet to zero

magnet.z_ACTN('CLMP')
magnet.y_ACTN('CLMP')
magnet.x_ACTN('HOLD')

do1d(magnet.x_fld,0.1,-0.025,50,12,ZNB.channels.S21.trace)

magnet.x_fld(0)

do1d(Kepco.X_BField, 0, 0.1, 100,2,ZNB.channels.S21.trace)

do1d(ZNB.channels.S21.power,-60,0,60,0.1,ZNB.channels.S21.trace)
```

Appendix E

cQED daughterboard v2

E.1 Available channels

16 lines connected to Nano-D pins on the motherboard. These are also connected to MiniCoax connections on the back of the motherboard via bias tees so they can be used as fast lines too. 4 SMP connectors, P1-4, which can be connected to the Puck SMPs and used for microwave measurements.

E.2 Daughterboard design

The board has dimensions of 24 × 24 mm and the inner cavity has dimensions of 5.6 × 5.5 mm. The SMP connectors are spaced 5.8 mm from each other on the outside, and on the cavity the connections are spaced 2 mm apart. The cavity depth is 0.8 mm. On the left hand side of the board there is space for two capacitors and a resistor which can act as a bias tee.

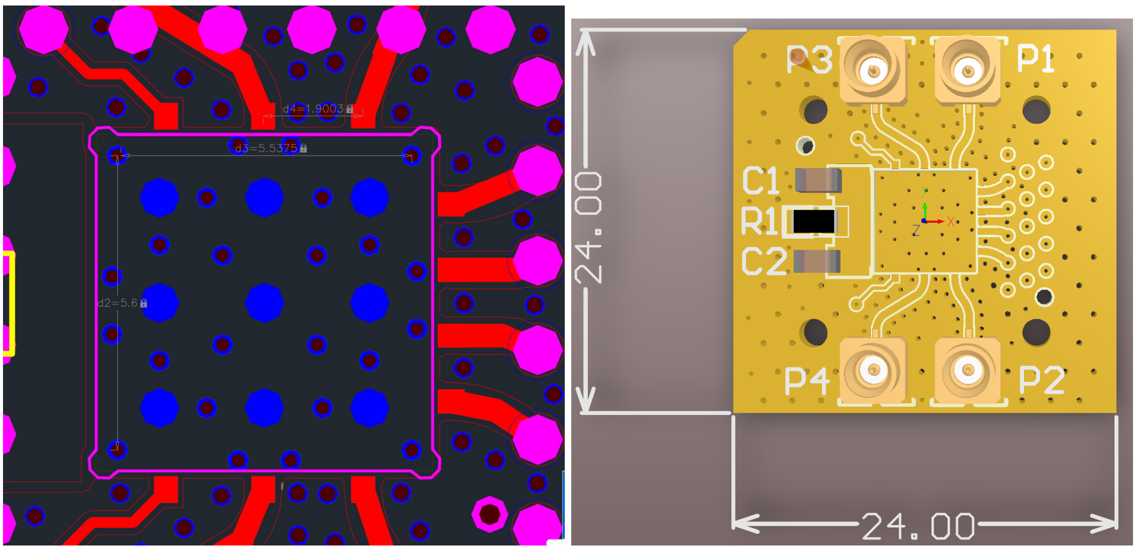

FIGURE E.1: cQED board design. Left panel: Screenshot of DXF file with board design including inner cavity measurements. Right panel: Image of the cQED board v2 and its dimensions.

The daughter board also has place to solder two capacitors and a resistor. Compatible components are given in the Table E.1.

E.3 Mounting the daughterboard

Inside the puck is mounted the Copenhagen motherboard - created at Center for Quantum Devices - and on it as interfacer with fuzz buttons whichinterface with the cavity back plane. In

TABLE E.1: Overview of bias tee components for cQED board v2.

Component	Number	Property
Resistor	ATC700A101JW	100pF
Capacitor	NRG1005-103-D	10k

order to use the DC lines on the board these fuzz buttons can be removed using tweezers. When mounting the daughter board the orientation is important, and the cut off corner on the board denotes the 'north" side of the board.

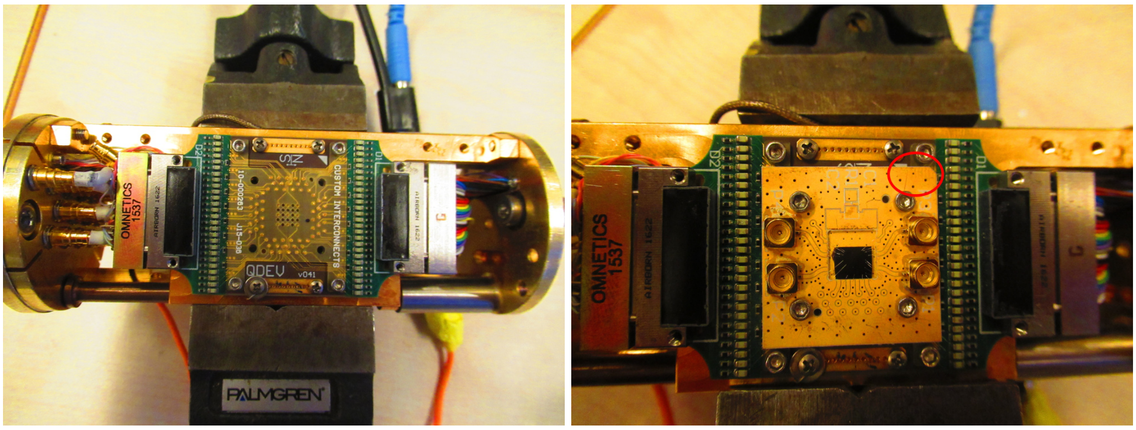

FIGURE E.2: Left panel: Copenhagen motherboard mounted inside large puck with connected NanoDs. Right panel: cQED board v2 mounted on the Copenhagen board.

E.4 DC connections

The board has 19 DC connections, where DC50 is used to bias the ground plane and the other 18 are connected to DC lines through the nanoD. 4 of these DC lines are also fast lines and are marked as "RF" rather than DC in Fig. E.3. RFB8 is connected to DC31, RFB7 to DC33, RFT1 to DC22 and RFT2 to DC19. In order to use the DC lines fuzz buttons should be intact but should be removed from the lines that are not being used and from the side with the capacitors.

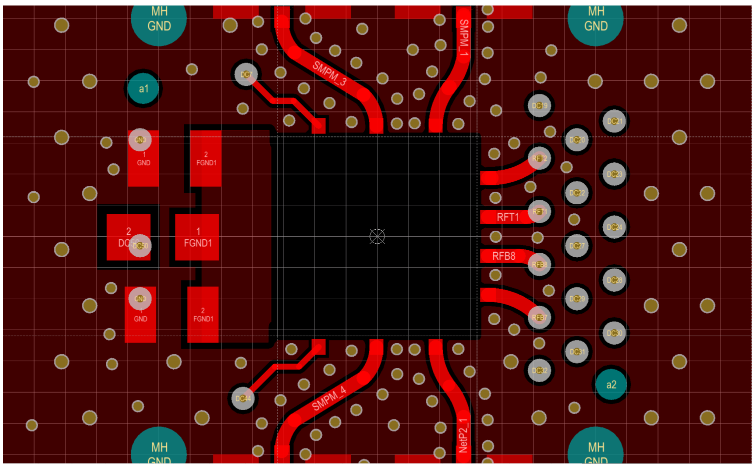

FIGURE E.3: Labelled DC lines and SMP lines on the cQED board v2 with DC lines labelled as DCxx and fast lines labelled as RFxx.

Appendix F

Additional results

F.1 NbTiN resonator on silicon

First we did a power sweep of the sample in order to see if the input power has an effect on the resonance. Fig. F.1 shows that power has no effect. Thus, we chose an input power of -25 dBm.

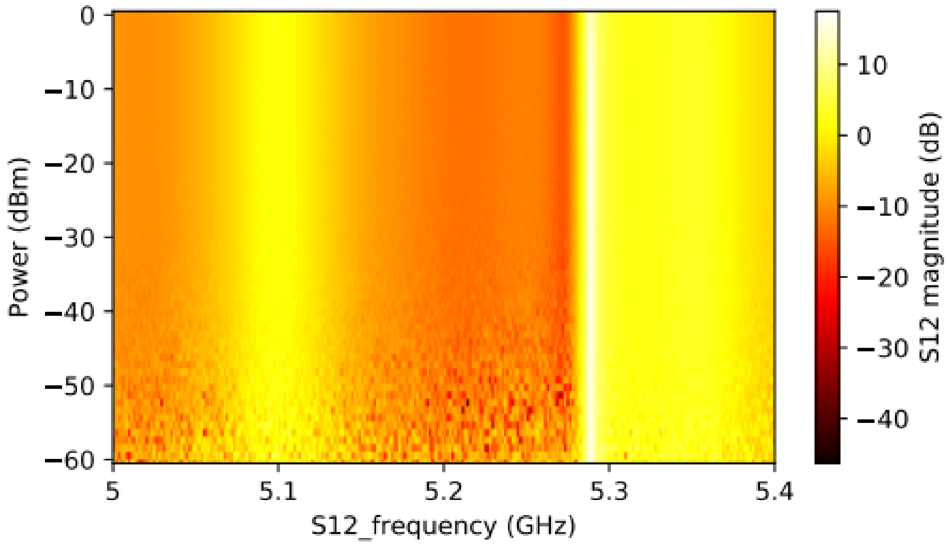

FIGURE F.1: Plot of a 2D power sweep vs. frequency for *V_res_Si_Z* sample.

Next we did a S21 transmission measurement using a vector network analyzer in order to identify the area of the resonance peak which can be seen around 5.27 GHz in Fig. F.2 (left panel).

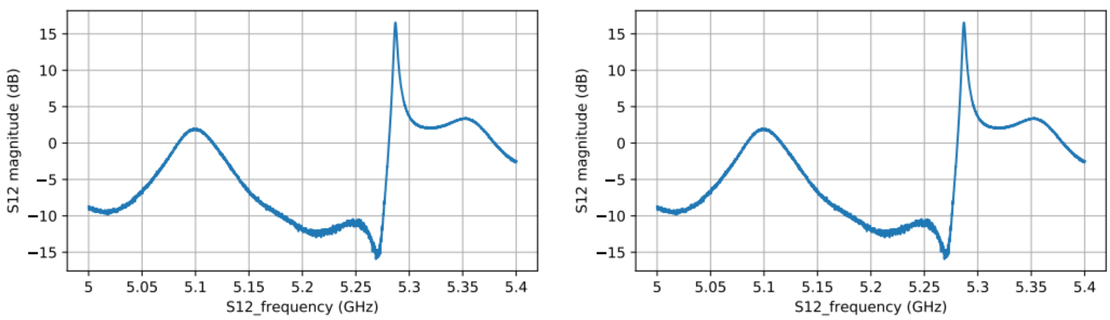

FIGURE F.2: S21 transmission measurements for *V_res_Si_Z* sample: Transmission at zero field (left panel) and Transmission at 200 mT (right panel).

We ramped up the perpendicular magnet (B_x) to 200 mT in order to get the noise measurement and then did a magnetic sweep from 200 mT to -200 mT. The 2D sweep can be seen in Fig. F.2 (right panel). The resonance moves clearly with a jump at zero mT due to hysteresis. However, when we did a similar sweep using the parallel magnetic field (B_z) we observed intensive noise (Fig. F.3 (left panel)).

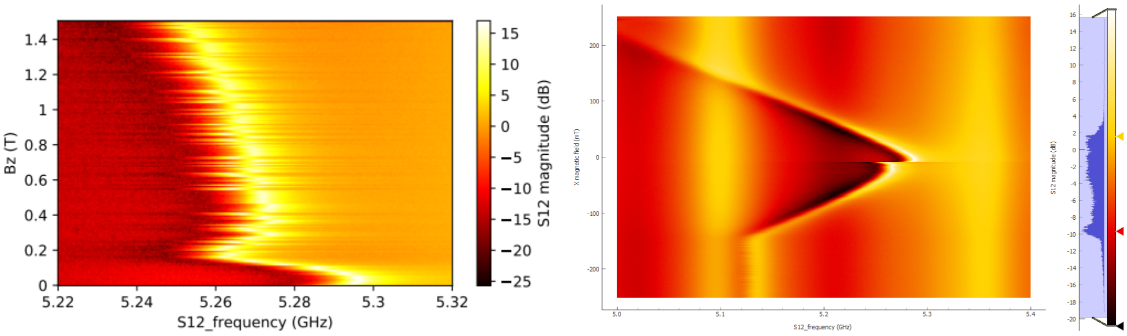

FIGURE F.3: Magnetic field sweeps using the Mercury power source for *V_res_Si_Z* sample: Parallel magnetic field (Bz) (left panel) and perpendicular magnetic field (Bx) (right panel).

To investigate this phenomenon further we studied how the amplitude change of the transmission signal and the frequency fluctuations with the magnet set to two different modes: CLAMP and HOLD. In Fig. F.4 we plotted the amplitude dependence of a frequency to the right of the resonance peak. It is clear that using the Kepco power source while everything on the Mercury power source is set to CLMP gives the least noisy measurements.

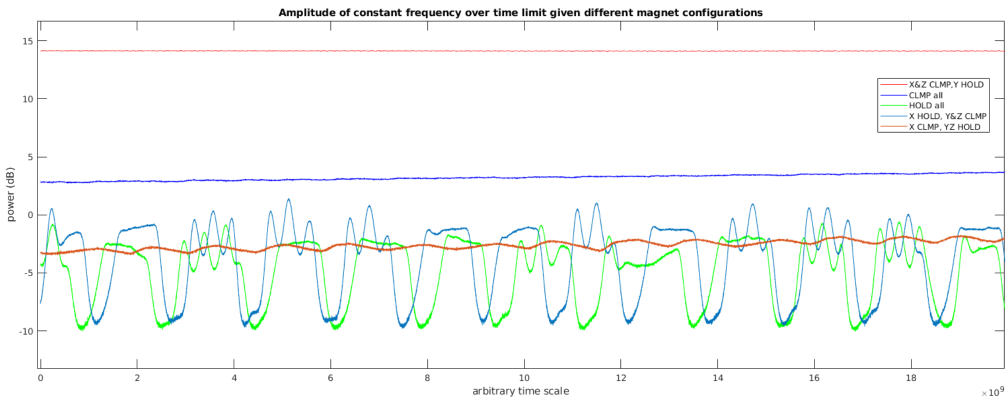

FIGURE F.4: Plot of the amplitude as a function of time for different combinations of HOLD and CLMP for *V_res_Si_Z* sample.

F.2 NbTiN resonator on implanted Si/SiGe

This same design was tested on an implanted Si/SiGe substrate with the quantum well intact. The chip was bonded and loaded on the cQED board v2 and the bonding scheme can be seen in Fig. F.5.

There was no resonance in this sample. Fig. F.6 does not reveal any visible resonance above background noise in a 1D sweep or movement with magnetic field. Power was well below expected (input -20 dBm) $\lambda/4$ resonator using the same lines was at -67 dB. With a 37 dB amplifier we would expect the power output to be at -30 dB rather than at -85 dB. We also saw a constant gate leakage at a constant value of 1.38 uA which was found by applying voltage to the respective gates. This was the same both when the components were grounded and floating.

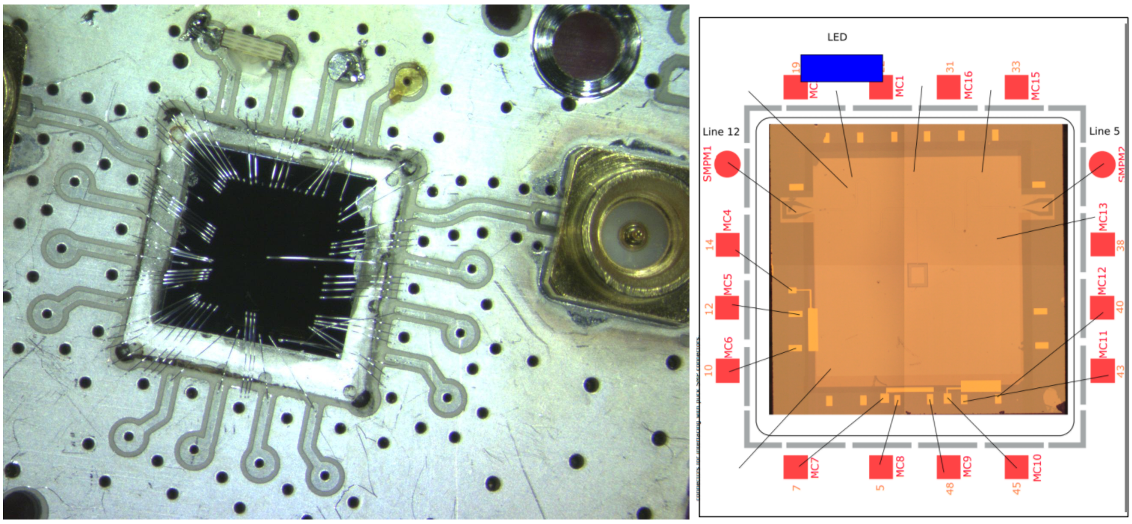

FIGURE F.5: Bonding image (left panel) and scheme (right panel) for *V_res_SiGe_A1* sample. There were made more ground bonds than shown in the schematic as shown on the left panel. An LED was also soldered on to generate electrons in the 2DEG at low temperature.

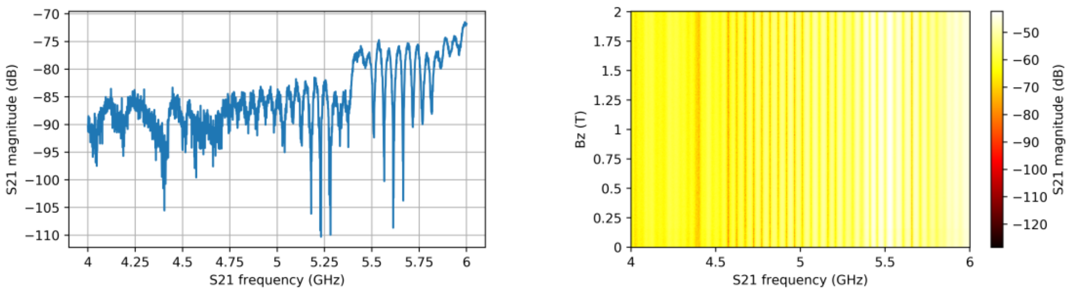

FIGURE F.6: Raw data for *V_res_SiGe_A1* sample: S21 transmission with -20 dBm (left panel) and parallel magnetic field sweep (Bz) (right panel).

There could be a number of reasons for this negative result. First of all, the resonator could be interrupted by impurities during the bonding process. Secondly, the SMP connectors could be soldered in such a way that they were shorted to the ground, causing the RF signal to escape to ground rather than propagate through the resonator. We were able to check the SMP connectors for shorts using a multimeter after unloading. We measured the resistance between the center pin of the SMP connector and ground. If the SMP is shorted then one sees a finite amount of current, while if they are not shorted the multimeter will show the large amount of resistance as OL which means it interprets the resistance as infinite. The third possibility is that the design is not impedance matched to the 50 Ohm line and this is especially visible in the silicon-germanium heterostructure. Since the resonator looked clean in the microscope before bonding, and we checked the SMP connectors for shorts, we decided to go back to fabricating the resonator on a silicon chip with a modified design. The gate leakage could be due to badly grown ALD which we decided to strip from the remaining chips and to apply new.

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