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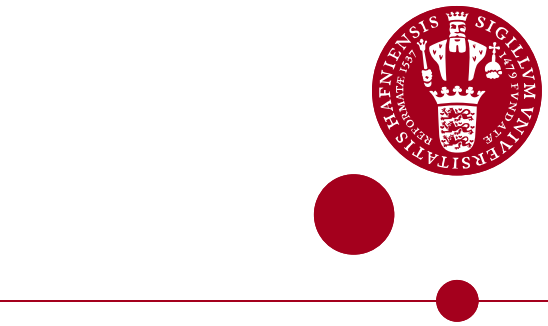
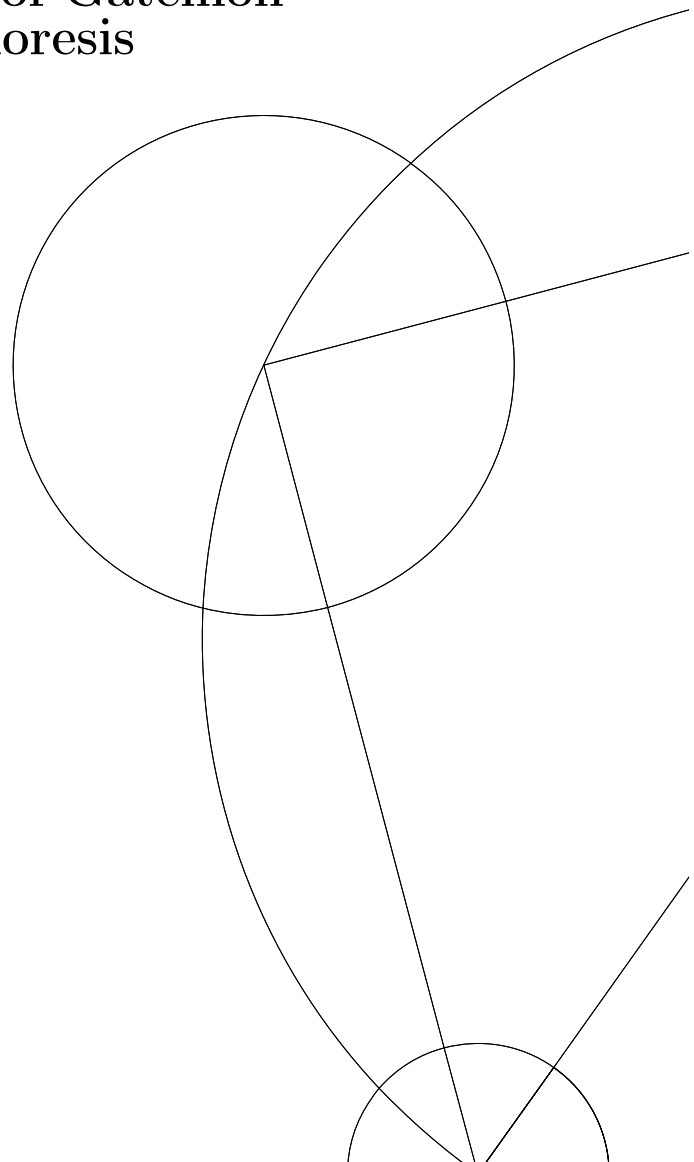


Thesis for the Bachelor degree in Nanoscience

Vita Heidari

Deterministic assembly of Gatemon qubits using dielectrophoresis



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Abstract

This thesis focuses on fabrication and characterization of a four-qubit nanowire-based transmon device using dielectrophoresis. In this method, nanowires suspended in solution are assembled on pre-patterned electrodes on the chip in a deterministic manner. To date, the main challenge to fabricating multi-qubit devices based on nanowire Josephson junctions has been random placement of the nanowires on the device chip. Dielectrophoresis provides possibility to overcome this challenge by means of large scale diposition of nanowires on pre-patterned electrodes and thus opens a new path to fabricating multi-qubit generation devices.

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Chapter 1

1 Introduction

Building quantum computer was proposed by Richard Feynman in 1982 [3]. and has been a subject of interest for many researchers in the area ever since. The fundamental difference in such computers is the employment of quantum mechanically operating bits called qubits, instead of classical bits in conventional computer processors. While bits in classical computers provide information by being either at zero or one state, qubits operate by being superposition of the both states.

One of the promising pathways to building a quantum computer is to use qubits based on superconducting circuits with Josephson junctions [6]. The Josephson junction is called in the honor of Brian Josephson in 1962 where he predicted the Josephson effect. The junction is an isolator or semicondcutor acting as a weak link between two metals or superconductors. These junctions can be formed by etching selectively aluminum shells of III/V nanowires as conducted in this thesis. These junctions contribute to a nonlinear inductance in the qubits and are controlled by gates in proximity of a few nanometer to the junctions. Transmon qubits implement these junctions to provide the necessary anharmonicity required for controlling the quantum states of the qubits.

Millions of qubits are required to be able to build a fault tolerant quantum information processor. This poses a problem for making qubits such as transmon [2] using nanowires. The challenge with the existing methods to deposit nanowires on the devices is that they are time-consuming. These methods include dispersing a large number of wires on the chip using a wipe or using a micromanipulator to place wires individually on the chip. The former method results in randomly placed wires, which require more fabrication steps, thus making the fabrication more complicated. The latter seems more deterministic but it's time-consuming due to individual deposition of wires on the chip. This method is further speculated to damage the wires, although conclusive evidence of this is not provided to date.

This thesis focuses on a new approach to nanowire assembly on silicon substrate using dielectrophoresis [11][4]. The method employs deposition by applying solution containing suspended nanowires on top of electrodes. By applying an alternating voltage, an electric field is initiated between the electrodes, which attracts and aligns the nanowires along the field.

The thesis structure is as followed; In the first section the theoretical background of superconducting qubits to the late gatemon qubits is presented. In the second chapter the Q value measurements on a low loss resonator silicon chip is presented to investigate the effect of dielectric loss on the resonator device. The third chapter presents fabrication steps including optical and electron beam lithography. Setup for the qubit measurements and some data is presented in the forth chapter. In the fifth chapter, results are discussed. Finally the last chapter presents the conclusion based on the results and views a perspective on future possibilities.

Chapter 2

2 Theory

Circuit quantum electrodynamics (cQED) is a field of physics that studies interactions between light and matter. The circuits here represent the qubits as artificial atoms and the resonator cavity as photons. By confining a photon in the cavity, we can study the interaction between the cavity and the qubit before the photon decays. There are various types of qubits for example flux qubit, Cooper pair box qubit, transmon qubits and phase qubit. Transmon qubit was introduced by Koch et al in 2007 [7] as qubits with very low sensitivity of their quantum states to the environmental charge noise and stray fields. These qubits are the objective of this thesis.

2.1 Superconducting Qubits

At very low temperatures and below critical magnetic fields superconductors conduct electricity with zero resistivity. This state is the result of fermionic electrons with opposite spin that behave as bosons, pairing in their ground states [12] The electron pairing favors the so-called Cooper pairs energetically. However the bonding is weak and can be broken at $T > T_c$, which means above the T_c the superconductivity of the material is disappeared.

The electron pairs called Cooper pairs in one electrode can tunnel through a barrier to the other electrode due to the overlap of their superconducting wavefunctions [9].

$$\psi_r = \sqrt{\rho_r} \cdot e^{(i\phi_r)} \tag{1}$$

where ρ_r defines the spatial dependence of density of the charge carriers and ϕ_r represents the spatial dependent quantum phase. The barrier between the two superconductors where Cooper pairs tunnel is called Josephson junction. The junction can be an insulator or a semiconductor, acting as a weak link between the superconductors, providing Cooper pairs tunneling across it. The tunneling ability of the Cooper pairs across the junction is due to the Josephson coupling energy defined as

$$E_J = \frac{I_c \hbar}{2e} \tag{2}$$

where I_c is the critical current and e is the electron charge [5]. Implementing a Josephson junction to the LC oscillator circuit, contributes to non-degenerate energy levels due to anharmonicity. This favors isolation of the lowest energy levels to be able to control and manipulate these quantum states. The flow of supercurrent through the junction at zero voltage is given by first Josephson equation;

$$I_s = I_c sin(\phi_t)$$

where ϕ_t is the time dependent phase difference. When a voltage is built across the junction, the phase varies with time and this results in the second Josephson relation;

$$\frac{d\phi}{dt} = \frac{2\pi}{\Phi_0} V \tag{3}$$

Where Φ_0 is the flux quantum equal to $\frac{h}{2e}$ and V is the voltage. Since the Josephson junction is a link between two superconductor, it also acts as a capacitor with an intrinsic capacitance C_J. The capacitance together with the nonlinear inductance of the junction given as

$$L_J = \frac{\Phi_0}{2\pi . I_c \cdot cos\varphi} \tag{4}$$

makes the junction a nonlinear LC oscillator, where Φ_0 is the flux quantum equal to $\frac{h}{2e}$ and φ is phase difference.

2.2 Cooper Pair Box

The Cooper pair box (CPB) consists of a Josephson junction for tunneling of Cooper pairs between a superconducting reservoir and island. The CPB island is capacitively coupled to a gate voltage for qubit control. The charging energy to transfer a single electron through the junction is given as $E_C = e^2/2C_\Sigma$, where $C_\Sigma = C_J + C_g$ defines the total junction capacitance, where C_J is the capacitance of the Josephson junction and C_g is the gate capacitance. The Hamiltonian of the system can be defined as,

$$H = 4E_C(\hat{n} - n_g)^2 - E_J \cos\hat{\varphi} \tag{5}$$

where $\hat{n}$ is the number operator, $\hat{\varphi}$ is the phase operator and n_g is the gate charge given by

$$n_g = \frac{Q_r}{2e} + \frac{C_g V_g}{2e} \tag{6}$$

Here Q_r represents the offset charge from the environment [7]. The gate charge can fluctuate as a result of environmental charge noise and this can cause decoherence of the qubit.

Depending on the E_C/E_J ratio, qubits are divided into three groups; CPB charge qubits operating in the regime $E_C \sim E_J$, flux qubits and phase qubits in $E_J >> E_C$ regime. In the charge limit $E_C \sim E_J$ the charging energy is large, thus the qubit is designed to be sensitive in adding a single Cooper pair. This can pose problems as the excitation energies are strongly dependent on the charge offset. In this limit charge noise can decrease the coherence.

2.3 Transmon Qubit

Due to the small size of the CPB, it is very sensitive to charge noise and stray fields in the surrounding environment. This implies that even a single Cooper pair can change the offset charge n_g significantly in the charge limit $E_C \sim E_J$.[9].

This problem can be tackled by increasing the E_J/E_C ratio as employed by transmon qubits operating in the $E_J >> E_C$ regime. These qubits with doubled Josephson junctions coupled to two superconductors create a dcSQUID circuit in which the junctions can be tuned by an external magnetic flux Φ . The gate electrodes which are coupled to the island capacitors control the offset charge, hence a modified offset charge given as

$$n_g = \frac{C_g V_g}{2e} \tag{7}$$

This can be achieved by adding large capacitors between the gate and the island parallel to junctions, which results in an energy gap E_{01} that is independent of the fluctuations in the offset charge n_g in the strong-coupling regime $E_J >> E_C$. For $E_J >> E_C$, the anharmonicity approximately given by,

$$\alpha = E_{12} - E_{01} \sim -E_C \tag{8}$$

decreases , thus qubit system becomes nearly harmonic oscillator. However the amount of anharmonicity required for qubit control in this regime is still sufficient. Here E_{12} and E_{01} are transition energies between the first and the second excited states and between the ground and the first excited state respectively.

The sensitivity of the qubit energy levels to gate voltage or offset charge is defined by charge dispersion. By decreasing the charge dispersion, the qubit performance is enhanced. In the transmon regime the charge dispersion is decreased exponentially. This compensates for the linear reduction in the anharmonicity ([7]), which is a significant feature of these qubits.

2.4 Gatemon Qubit

A new transmon qubit called gatemon [8] is introduced by researchers, in which a semiconducting Josephson junction weak link is implemented. The qubit control in this device 1 (a) is performed through a gate coupled to the junction, thus the need to feed flux through the double-junction loop as in conventional transmon qubits is eliminated. The electrostatic gate coupled to the junction controls the Josephson energy of the qubit by depleting charge carriers in the semiconducting junction.

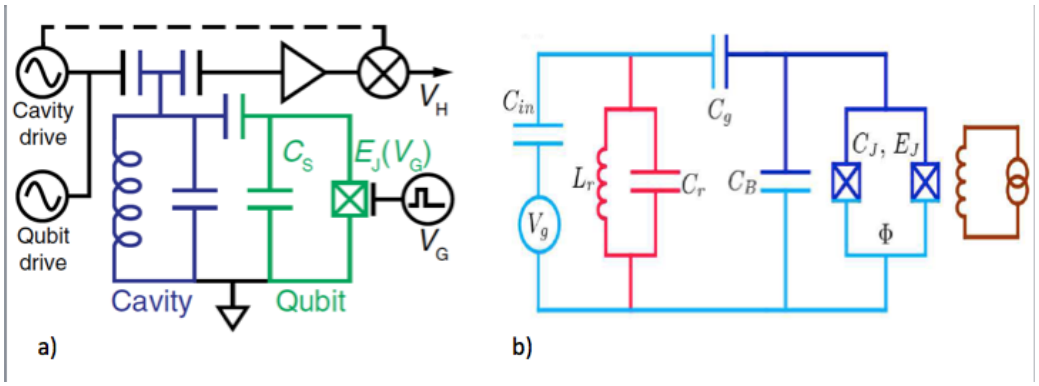

Figure 1: a) Circuit diagram illustrating readout and control of gatemon device[8]. b) Skematic diagram of the transmon with flux-tunable junction loop. The Josephson junctions are illustrated as cross box

2.5 Nanowire Assembly Using Dielectrophoresis

This section focuses on directed assembly of nanowires using dielectrophoresis as an alternative to the conventional deposition method. The method presented here employs depositing suspended dielectric nanowires on the pre-patterned electrodes by applying a non-uniform electric field to attract and align the nanowires on top of the electrodes.[14]

AC field applied in this method minimizes the effects of electrostatic forces arising from charges on dielectric particle surface. In addition It provides a frequency dependent DEP force to control the assembly. The electric field applied across the electrodes polarizes the dielectric nanowires resulting in an induced dipole moment on the nanowire surface. This polarization results in a torque which aligns the nanowires parallel to the field. In an optimally polarized nanowire, the excess negative charge q_- is accumulated in one end and excess positive charge q_+ is accumulated on the other end. The net force exerted on the nanowire is defined as,

$$\vec{F}(\vec{r}) = q_+ \vec{E}\left(\vec{r} + \frac{1}{2} l \frac{\vec{p}}{|\vec{p}|}\right) + q_- \vec{E}\left(\vec{r} - \frac{1}{2} l \frac{\vec{p}}{|\vec{p}|}\right) \tag{9}$$

where $\vec{E}$ is the electric field vector, $\vec{r}$ is nanowire center point spatial coordinate, l is the nanowire length, $\vec{p}$ is the effective induced dipole moment, $\vec{p}/|\vec{p}|$ is a unit vector which points along axis of the wire. The torque exerted is given as,

$$\vec{T}(\vec{r}) = \frac{1}{2} l \frac{\vec{p}}{|\vec{p}|} \times q_+ \vec{E}\left(\vec{r} + \frac{1}{2} l \frac{\vec{p}}{|\vec{p}|}\right) - \frac{1}{2} l \frac{\vec{p}}{|\vec{p}|} \times q_- \vec{E}\left(\vec{r} - \frac{1}{2} l \frac{\vec{p}}{|\vec{p}|}\right) \tag{10}$$

In order to find an equation of the net force on the nanowire as a function of nanowire position one needs to apply Maxwell quasi-electrostatic equations. This requires assuming that the length of nanowire is smaller than the area over which the electric field varies,

and that the presence of nanowire doesn't affect the initial electric field. By applying these assumptions the net force on nanowire as a function of position can be defined as,

$$\vec{f} = Re(\vec{\epsilon}) \cdot \left(\vec{E}\,(\vec{E} \cdot \hat{n}) - \frac{1}{2}(\vec{E} \cdot \vec{E})\,\hat{n} \right) \tag{11}$$

where $\vec{f}$ is the density of surface force at every point on the nanowire, $\vec{\epsilon}$ is the complex permittivity of solution and $\hat{n}$ is the unit vector normal to nanowire surface.

In addition to DEP forces and torque exerted on nanowire, other factors including the uniformity of the nanowire suspension as well as pre-assembly clean-up of the substrate define the optimization of the assembly process. The permittivity of the suspending solution and the polarizability of it relative to that of nanowire are important factors for the assembly. These factors effect the strength of the applied electric field, for example isopropanol solution with dielectric constant of 19 minimizes the interactions between the solution and nanowire, which results in DEP forces being the only factor to control the assembly [14].

Other properties of the suspending solution affecting the assembly is the critical drying point, which if too short, prevents optimal assembly, since nanowires would not have sufficient time to align themselves between the electrode spacing.

Chapter 3

3 Superconducting Resonator Tests

In this section measurements of a silicon sample containing four aluminum resonators is presented in figure 2. The primary goal of the fabrication and measuring this resonator array was to observe how the sample geometry and processing affected the Q values of the resonators. Since the qubits are expected to be limited by similar dielectric loss mechanism, measuring resonators would be a useful diagnostic for qubit devices. The substrate presented here is a high resistivity silicon (100) sample without SiOx layer. The oxide layer contributes to capacitance loss in resonators and qubits due to the environment noise, which is a result of unsaturated two-level system (TLS) in the bulk and surface of the oxide. The resulting noise [13] effects performance of the resonator device, which is appeared as low Q value of the resonator.

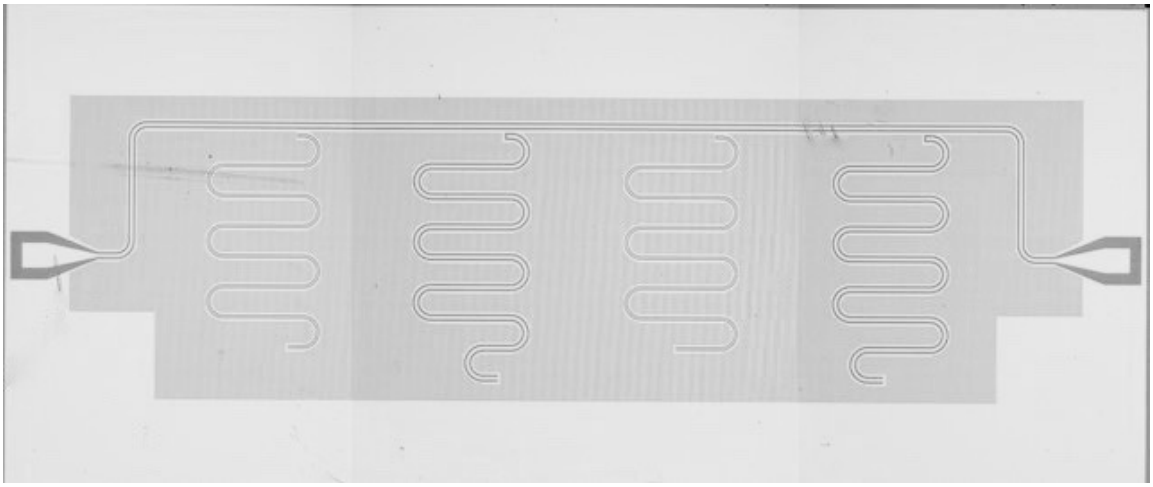

Figure 2: A 2D image of the design illustrating four resonators coupled to a common feed line

The measurements were performed with the sample cooled to < 50 mK using a dilution refrigerator. The sample with dimensions 7 mm x 4 mm is fabricated with optical lithography and wet etch process as presented in the later chapters. The device has four pre-patterned aluminum resonators coupled to a common feed line as illustrated in figure 2. In the device design, the length of the resonators is varying. The resonators with nearly the same length and same center pin distance have similar Q values.

Figure 3 indicates the intrinsic and external Q values of one of the resonators as a function of power. The Q value is related to the coherence time T_1 of the resonator cavity through following relation.

$$T_1 = \frac{Q}{\omega_c} \tag{12}$$

Here ω_c is the angular frequency given by $\omega_c = 2\pi f_c$, where f_c is the cavity resonance frequency.

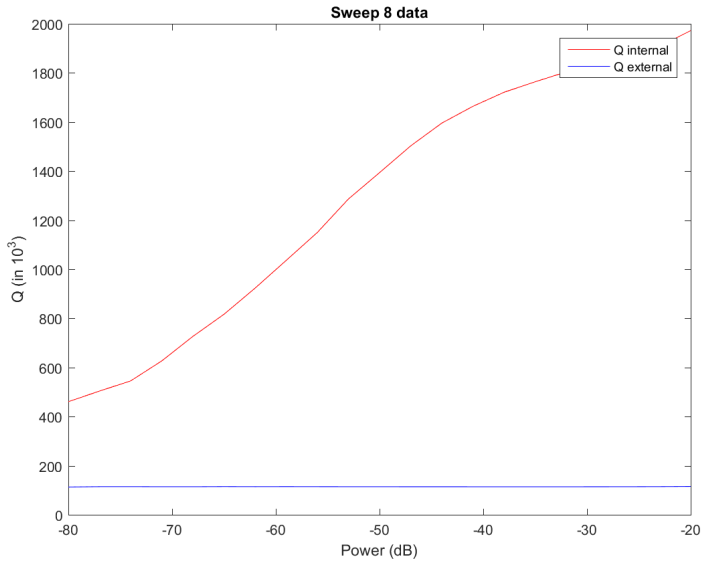

Figure 3: Intrinsic and external Q value measurements on a resonator as a function of power. As indicated, the external Q value is independent of the power applied.

The Q factor measurements at low power indicate that the intrinsic Q factor of the resonators is in the range of $3.5 \cdot 10^5 - 4.8 \cdot 10^5$. This corresponds to a coherence time T_1 of the resonators in the range of $9.5 - 14.5\ \mu s$.

As illustrated in the plots, the external Q value is constant with power. This is expected since it is determined only by the capacitive coupling to the feed line. The observed power dependence of the intrinsic Q values indicates losses are limited by two level systems (TLS) at low powers [1][13]. Thus improving device fabrication techniques such as treatment of the silicon substrate surface and deep etching of the substrate before metal deposition enhances the resonator Q factor significantly [1]. The former is used to eliminate charge noise on the substrate-vacuum interface, while the later reduces residues from metal-substrate interface. The intrinsic Q values also depend on the width of the resonator conductor.

Chapter 4

4 Qubit Device Fabrication

The substrates used in this project are high resistivity silicon without the silicon oxide layer, since the silicon oxide layer contributes to the high loss in resonator cavity, resulting in low coherence time and thus decreases qubit performance. The low loss silicon chips enhances Qfactor and thus increasing the coherent length (T_1 and T_2) of the qubits. The chips are fabricated by lithography methods, which includes patterning the electrode circuit, etching the aluminum, patterning the resist windows,nanowire aligning and patterning the contacts and gates around the nanowires. The design for qubits contains a transmission line and four resonators each capacitively coupled to one of the four qubits. Figure 4 shows a summary of the fabrication steps.

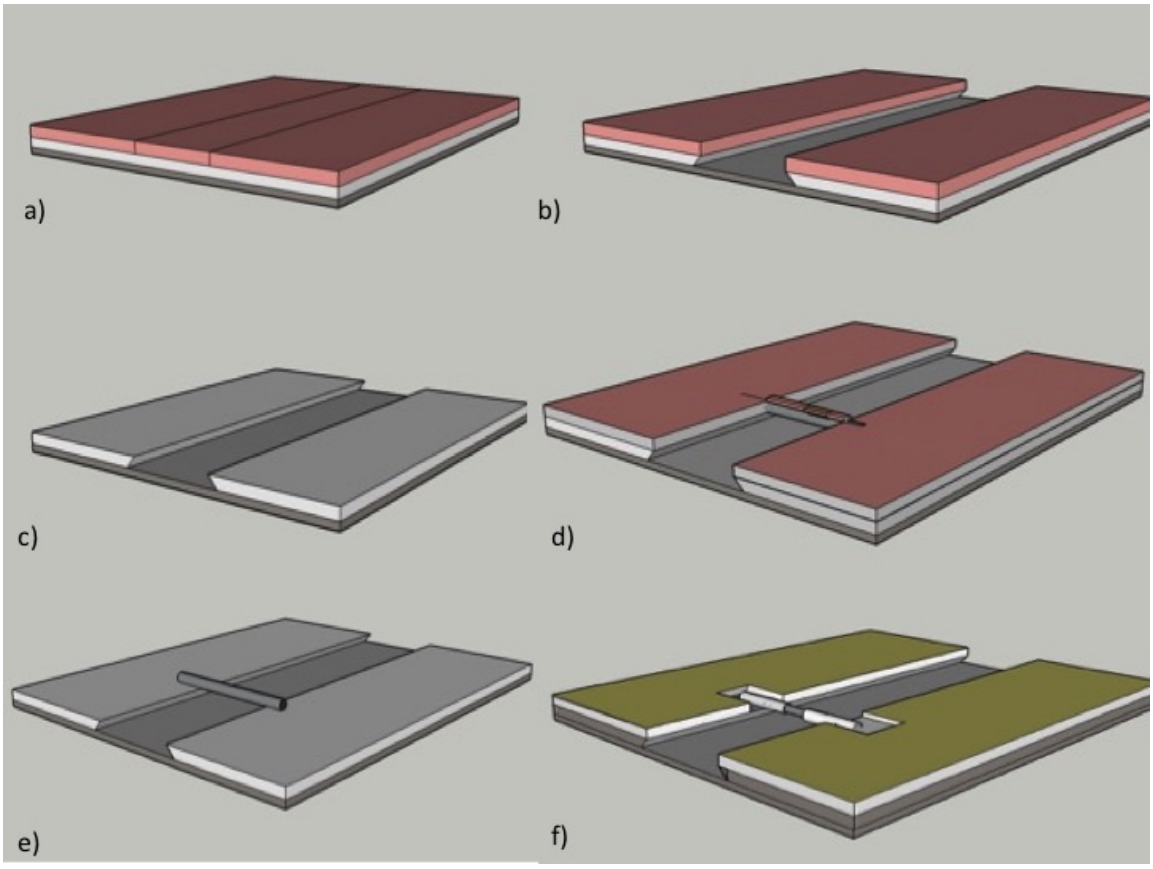

Figure 4: Lithography steps. a) Aluminum is coated on the silicon substrate followed by a photoresist layer on top. The pattern is exposed by uv-lithography. b) The exposed area is developed and the pattern is etched by aluminum etchant. c) Photoresist is removed. d) The chip is spun with PMMA and the windows for trapping nanowires are patterned using EBL. Nanowire are assembled on the chip using dielectrophoresis. e) PMMA layer is removed. f) The chip is spun with PMMA to pattern the areas on the nanowire where the junctions are going to be formed. The exposure is done using EBL. The exposed area is developed and the aluminum shell of the nanowire in the selected area is etched to form the junction.

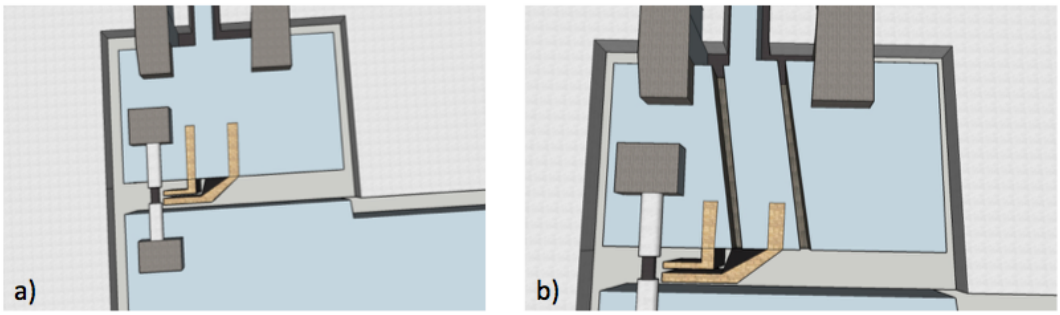

Figure 5: Patterning contacts and gates and removing excess nanowires. a) The chip is spun with PMMA,exposed using EBL and developed. Aluminum is evaporated on the chip, followed by lift-off. The contacts and gates are thus patterned. (The gates are illustrated as yellow in the figure). b) The chip is spun with PMMA and the patterned excess areas and excess nanowires are exposed using EBL. The exposed area also includes two narrow paths grounding the aluminum from both sides, so the gate on the right in the figure in connected to the feel line, while the left gate is grounded. The exposed area is developed and etched using aluminum etchant.

4.1 Electrode Pattern

Before depositing aluminum on the substrate, the substrate surface should be cleaned of any dirt or residue. In order to do this the substrate is bombarded by argon plasma in a process called Kaufmann milling, which is done as an in situ cleaning step before metal deposition. The Argon plasma atoms used in the milling process, are accelerated from ion beam source and bombarded into surface of the substrate. A thin layer of material on substrate surface as well as impurities is removed during the process in order to increase the metal adhesion to the substrate. For milling process, the electron gun takes 1 minute to warm up and the milling process takes about 20 seconds. The substrate is then coated with evaporated aluminum. The solid aluminum is evaporated using an electron beam source with a current of 140 mA and is coated on the substrate sample by a rate of 1.0 A/s. The coated aluminum layer is 100 nm thick. After aluminum coating, the sample is placed in acetone and isopropanol respectively using ultrasound for 5 minutes at high power and low frequency.

The circuit and qubits were designed in Autocad and converted to dxf format compatible for the uv-laser writer (LED). AZ1505 resist is spun on the sample. The control line and qubit patterns are exposed using the laser writer afterwards. The pattern is developed in AZdeveloper followed by immersing in MQ water. After blow drying the sample, it's checked on the microscope for eventual shorting on the wires. A cleaning step in a microwave plasma asher is conducted afterwards to ensure any resist residue on the surface is removed. The sample is exposed to oxygen plasma in the asher for 1 minute

Transene D is a commercial aluminium etchant which is used for patterning the circuit. The etchent solution is heated up to 47 C at heat bath. The chip is immersed into the etchant solution for one minute, followed by rinsing in MQ water twice and blown dry. Twice rinsing in MQ water is to ensure removal of any residual acid on the surface of the chip. After etching, the chip is sonicated in an ultrasonic bath for a couple of minutes and

blown dried.

4.2 Resist Windows

Three different approaches have been used in this project for patterning the resist windows for wire deposition. The first method involves spinning the chip with AZ1505 and patterning the windows using the UV-laser writer. However the windows patterned in this way were attacked by the nanowire solution IPA.

To solve this issue, a double layer of resist was used to be protected against IPA attack. A layer of PMMA ebeam resist was spun on the chip followed by baking at 185 degrees. A photoresist layer is then spun on top of the PMMA resist and was baked at 115 degrees. The bilayer chip is then developed with photoresist developer and immersed in milli-Q water. The windows appeared on the chip still had to be ashed through PMMA. For this reason the chip was ashed in microwave asher for a couple of minutes and were checked afterwards for residual resist on top of the pads. This spinning method was used for the sample with electrode arrays.

The third method suggests spinning the chip with PMMA A6 and exposing the windows layer using electron beam lithography (EBL). Since the pre-patterned aluminum marks can hardly be detected in EBL, some gold marks were patterned around the design as to guide alignment with the patterned design written by laser writer. Using uv-lithography/ebeam lithography for defining the position of the marks followed by evaporation and lift-off is described in details in later chapter. The difference is the large gold marks around the circuit in this section is patterned by uv-lithography, while the small marks around the nanowires is patterned by ebeam lithography.

After depositing Ti/Au marks on the sample, the windows are patterned in PMMA resist using EBL. The windows patterned in this way were small features on the order of 2 μm by 5 μm. The sample is spun with e-beam resist and is exposed on EBL. After exposure the sample is developed in PMMA developer (IMBK:IPA 1:3 solution) and rinsed in IPA before being dried by nitrogen gas. Finaly the sample is terminated in plasma oxygen using the asher in order to remove residual resist in the exposed regions. This method provides the optimal result for the small fine features.

4.3 Nanowire Assembly Using DEP

The main purpose of this section was to study nanowire deposition on pre-patterned electrode structures using AC electric fields. In the first part of this section a test device with aluminum electrode arrays is presented. The electrode arrays are connected to a DEP-suitable circuit board with dimensions of 5 by 10 cm. The process is monitored using an optical microscope and a motorized stage under the sample, to be able to monitor the whole electrode area during nanowire assembly.

The second part of this section presents the same method for nanowire assembly on a transmon device. The nanowires used in these devices are the bottom-up grown InAs

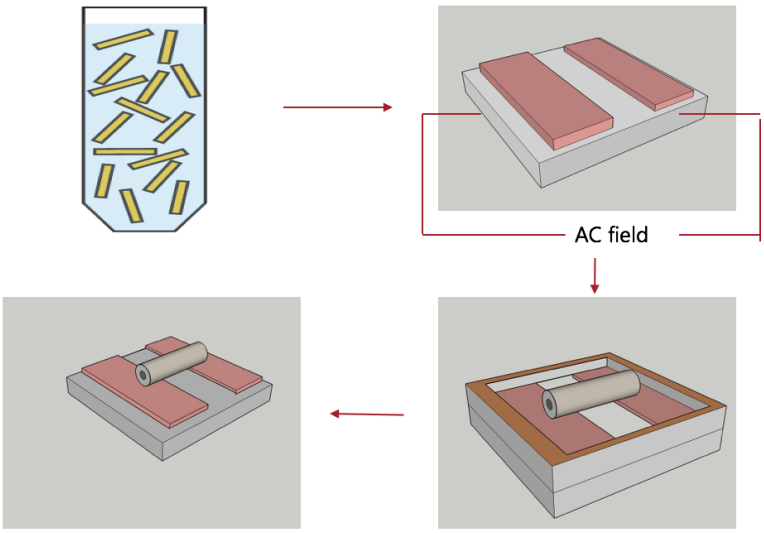

Figure 6: Nanowire assembly using dielectrophoresis.a) Nanowire solution is prepared. b)The electrodes are patterned on the chip. c) Photoresist is spun on the chip to define the windows for nanowire trapping. Nanowires are aligned between the electrodes in the defines windows using DEP. d) The resist is removed.

nanowires with Al epitaxially grown around the InAs core. The aluminum shell has a diameter of 30 nm around a 75 nm thickness of InAs core.

4.3.1 Nanowire Assembly On Electrode Arrays

This section presents nanowire assembly on aluminum electrode arrays using an AC electric field. The effect of the field and the electrode spacing on attraction and alignment of nanowires is investigated. The design contains four electrode groups, each connected to two pads. To provide electric field between the electrodes, one of the pads is grounded and the other is connected to the central pin. Each group contains eight arrays with a width of 20 μm and a length of 250 μm. The spacing between the arrays is 8-14 um. Large windows with varying sizes are designed here to trap the nanowires during the assembly, as indicated in figure(6).

A highly concentrated nanowire solution is prepared by dropping a few ml IPA into a small bottle and placing the nanowire substrate inside. A 2 x 2 mm NW substrate piece is cleaved from the center of the NW substrate to ensure the solution contains a large population of wires. After placing the NW substrate in a suitable bottle, the bottle is sonicated for 10 seconds at medium power and 37 kHz frequency to detach the wires from the growth substrate to provide the suspension solution.

The electrode array surrounding is covered by silicone spacer to ensure the solution does not flow outside the chip. This consideration is to maintain nanowires on the electrodes for a longer time for better nanowire attraction and alignment as well as preventing an nonuniform nanowire suspension on the electrode area. The sample is bonded to the PC

board using aluminum bonds on the aluminum pads, which are already cleaned of resist, to obtain electrical contact to the chip. The resistance of the electrodes was measured prior to deposition to ensure there was not shorting, or residual resist on the pads that could result in low or no conductivity. The sample resistance was measured to be 1.3 kΩ. The circuit board is attached to the microscope stage using carbon tape and is connected to the Agilent microwave generator to drive an electric field between the electrodes. A voltage of 2 Vpp and frequency of 10 kHz was applied to the electrodes to provide DEP forces to attract and align NWs along the field between the electrodes.

The procedure starts by placing a drop of 70 μl nanowire suspension using pipette on top of the electrode area, which is then covered by a glass slide to provide a uniform suspension on the area. An AC field with the mentioned settings is generated by the power generator and is applied on the electrodes until all the nanowires in vicinity of the windows are trapped and aligned to the electrodes.

The stage as well as microscope light produce heat, which contributes to fast drying of the solution. To avoid heating, the microscope light and motorized stage are switched off after applying the solution to the sample. This allows more time for NWs to be attracted and aligned to the electrodes before the solution dries, typically 3-5 minutes. Figure 7(a) and 7(b) indicate images of the electrode patterns and examples of nanowires aligned to the electrodes.

4.3.2 Nanowire Assembly On Transmon Device

The assembly procedure here is identical as for the electrode arrays. The sample here contains four transmon designs, each has four qubits coupled to four resonators. The spacing between the electrode connected to feed line and the T-island capacitor is 5 micron. Six windows with dimensions 7 by 2 microns were designed on the gap between the aluminum electrodes to trap single nanowires.
Figure 7 indicates different alignment yield on the device. Figure 7(c) demonstrates a good alignment with all six windows containing wires, however two of the windows contain doubly-attached wires, which would make them useless because it's hard to separate them to be able to use them for qubits. Figure 7(d) indicates highly populated windows. This might indicate a higher concentration of nanowires in the solution around these electrodes. The missing nanowires in some windows could be related to low concentration of the nanowires in the suspending solution.

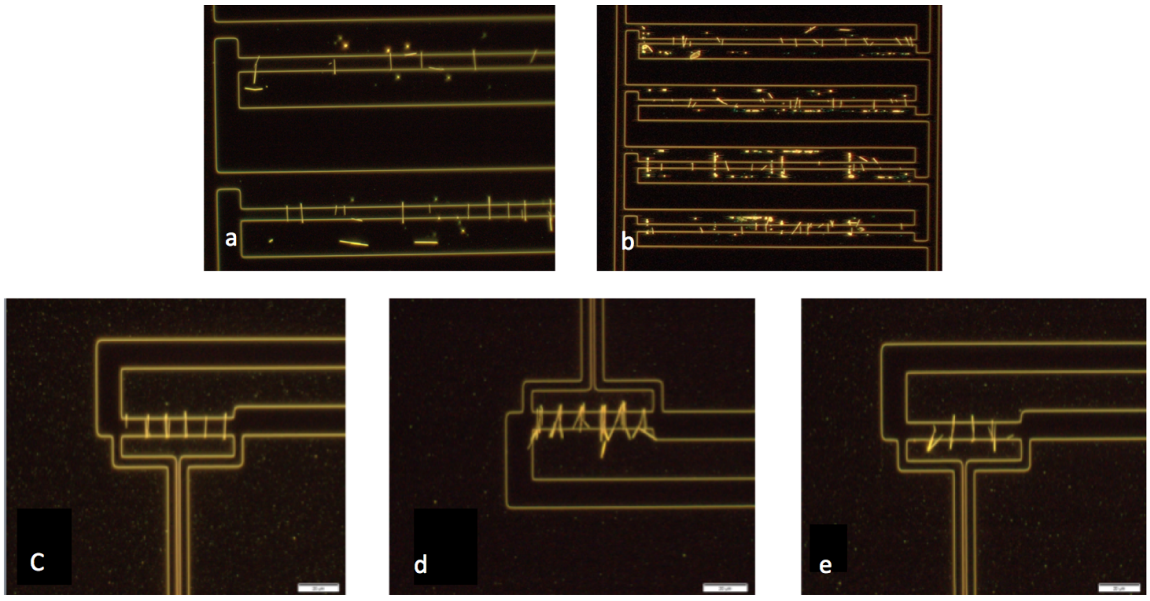

Figure 7: Dark-field optical images of the test sample and transmon sample indicates DEP-employed nanowire assembly. a, b)Indicates nanowires assembled in the electrode spacing. c, d, e) Nanowires assembled on the transmon device.

4.4 Forming Josephson Junctions

Josephson junctions were formed by wet etching a selective area of the nanowire aluminum shell. For this purpose narrow windows with a width of 150 nm were designed between the electrodes, crossing the nanowires in the middle. The process starts with spin coating the chip with PMMA A4 with the usual setup followed by EBL using the Elionix tool. The alignment exposure was done with four point alignment to obtain sufficiently accurate alignment. The exposed windows were developed by PMMA developer, soaked in IPA and blown dry.

Josephson junctions were made by etching the aluminum shell of the nanowires in the exposed areas using etchant, as shown in figure (8). Transene type D aluminum etchant was used for this purpose. The etchant was heated to 50 C in the heat bath. The chip containing the nanowires was dipped into the etchant for a few seconds, followed by dipping into milli-Q water twice. Finally it was soaked in isopropanol solution and blown dry by nitrogen gas.

The etching process with mentioned setup has usually an undercut of approximately 25 nm, therefore the width of the windows was chosen to be 150 nm for both designs to achieve an etched gap width of 200 nm. After the etching, the nanowires with desired etched area were chosen for connecting the gates and contacts to make the junction(see figure 8).

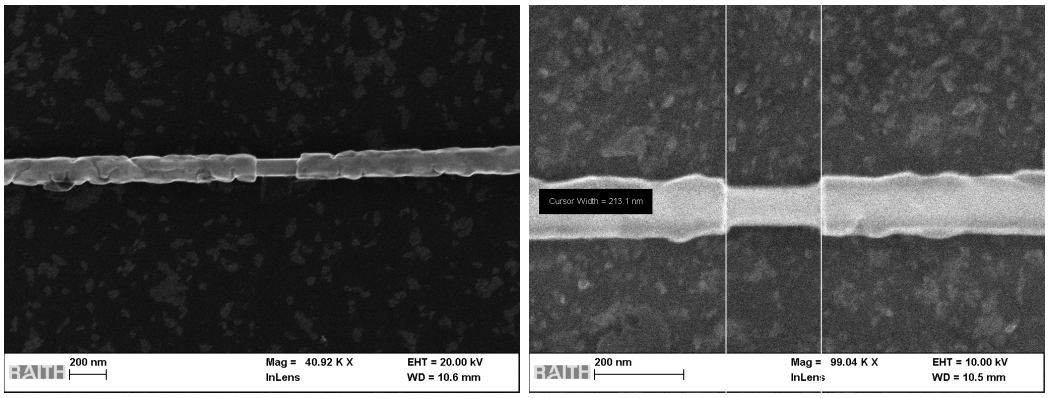

Figure 8: eLine images of the nanowire etched by aluminum etchant to form the Josephosn junctions. The junction is about 200 nm wide.

4.5 Patterning Gold Alignment Marks

Since the contacts and gates should be patterned precisely, there need to be some small gold marks around the nanowires as well as the LED written gold marks, in order to optimize the alignment. The alignment is carried out using the larger marks around the circuit to get the approximate position of the nanowires in combination with the small ones around the wires to obtain a precise alignment for the exposure. The sample is spun with the PMMA resist and is exposed by EBL. The marks layer is developed afterwards with PMMA developer. For the large gold marks exposed by uv-lithography earlier, a photoresist (AZ1505) is used instead. The development is thus done by EBL. After cleaning the surface residues on the chip by oxygen plasma asher, the sample is coated with a titanium/gold film. A layer of 20 nm Ti and 80 nm gold is coated on the chip using an AJA metals deposition system.

4.6 Lift-Off

To remove the Ti/Au layer on top of the patterned resist, a lift-off process in acetone is used. Acetone is heated in the bath at 50 C degrees. The chip is sunken in the solution for a while before agitating the Ti/Au layer with syringe for a few minutes. This is done to help peel off the Ti/Au layer more gently. For the large gold marks exposed by laser writer for the DEP windows the lift-off was followed by sonication for a few minutes. However this method would make potential damage to the nanowires at this stage, either by moving or detaching them from the chip. After lift-off, the chip is rinsed in IPA for a few seconds and then dried.

4.7 Gates And Contacts

The etched junctions need to be contacted properly to the ground aluminum plane and capacitors. Furthermore some gates should be implemented near the junctions to provide control of the qubits.5 The contacts are designed in two ways; one, contacting the nanowire junction leads on both sides, connecting the wire with the feed line from one side and from the other side connecting it with the T-island. These contacts had trapezoidal forms with dimensions of 1 by 4 micron.

The second contacts connect one of the gates to the ground plane. This is described in the next section, by separating the gates, an electric field is initiated between the them when one gate is swept through the feed line. These contacts are designed with dimensions of 5 by 15 um.

The patterned side gates and contacts were exposed on EBL and the exposed areas were developed with PMMA developer. Prior to aluminum evaporation, an ion-milling step is necessary to remove the oxide layer on top of the aluminum as well as improving adhesion of the metal/nanowires and metal/substrate. The Kaufmann milling is done for four minutes, to assure the oxide layer is removed. The residue or dirt particles can also result in charge noise. Since nanowires have a diameter of around 100 nm, an aluminum contact with a width of 150 nm is evaporated on top of them to assure they cover nanowires.

The lift-off process is carried out in the same way as described in earlier section for the Ti/Au evaporated layer. The only difference was the temperature of the acetone, which was lower than was considered for lifting off gold layer. This consideration was to minimize damage to the chip structures.

4.8 Removing Excess Nanowires And Aluminum Contacts

Several nanowires were contacted to aluminum ground plane and capacitors so that the most suitable one is chosen to proceed with. By the most suitable it's meant the nanowire which has the right junction size and the right gate distance to the junction. Since only one nanowire is needed for each qubit, the excess wires with aluminum contacts and gates around them should be etched away. The process is carried out by exposing the area, developing and etching the developed area away using Transene type D Al etchant.5 In order to sweep the gate, one of the designed gates is grounded by etching away a thin area between the gates. A narrow path is designed for this purpose and etched away as in figure 9(top right).

The process starts by selecting the unwanted wires and gates and designing the area covering them in AutoCAD. Here we should consider any undercutting of the Al etchant, which would damage the area around. This introduces some limitations, especially where the wires, gates or contacts are less than a micron away from the selected wire.

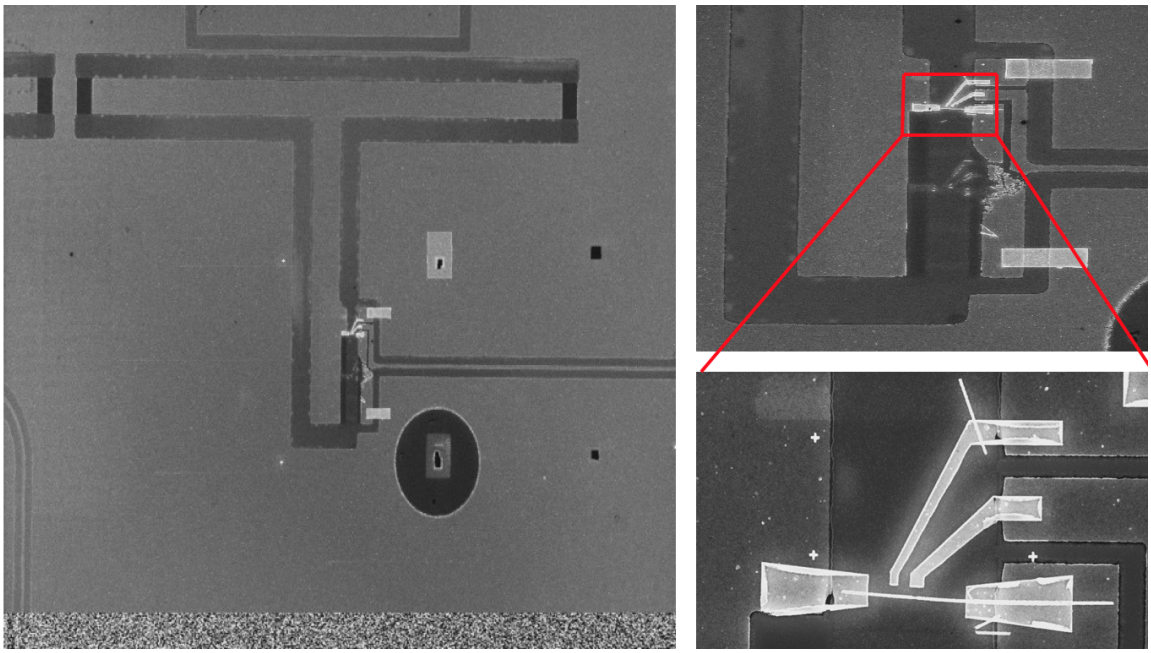

Figure 9: Eline image of the qubit after etching the excess area away and grounding the contacts and gate. The figure on the left indicates the aluminum T-island connected to the nanowire through aluminum contacts. The two contacts on each side of nanowire is connected to the ground aluminum plane. One of the gates is grounded as indicated in the figure on the right.

After spinning the sample with PMMA, the qubits were exposed by EBL tool. The exposed area was then developed and cleaned by plasma asher before proceeding with etch. The etch was done with the usual Transene (D) etchant. The chip was immediately immersed in milli-Q water twice for a few seconds.

Chapter 5

5 Experimental Setup

The fabricated device with dimensions of 7 mm x 3 mm is glued to a printed circuit board. To provide electrical contact to the chip, it is bonded to the board using aluminum wire bonds as indicated in figure 10 The circuit board is placed inside a puck and is shielded from magnetic noise by an indium-sealed aluminum sample box. The puck is mounted into the dilution refrigerator, which provides mK temperatures required to ensure the qubit devices are not thermalized in their ground state.

A Tektronix AWG5014C arbitrary waveform generator was used to drive Rohde and Schwarz SGS100A vector microwave sources for qubit control and readout. The magnitude and phase of the output modulated signal from cavity is plotted against driving frequency. To control the qubit gate voltage, a Keithley 2400 general source meter was used.

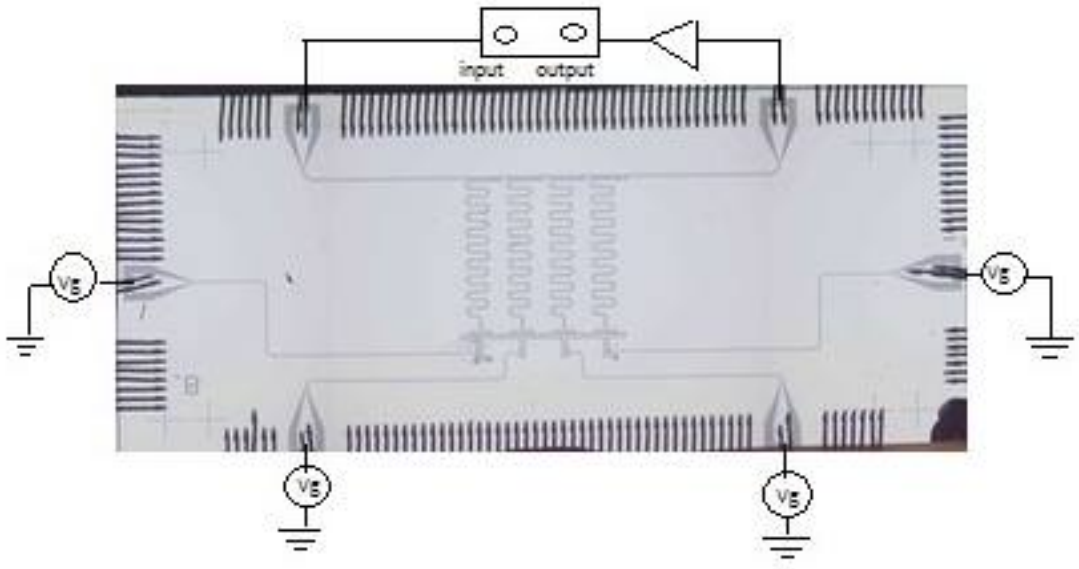

Figure 10: An overview image of the fabricated chip glued to the circuit board and bonded with aluminum-bonded to the PC board

Chapter 6

6 Results And Discussion

The first measurement was to test functionality of the qubits, by sweeping the cavity power and observing the cavity frequency response. The measurement were conducted on two qubits.

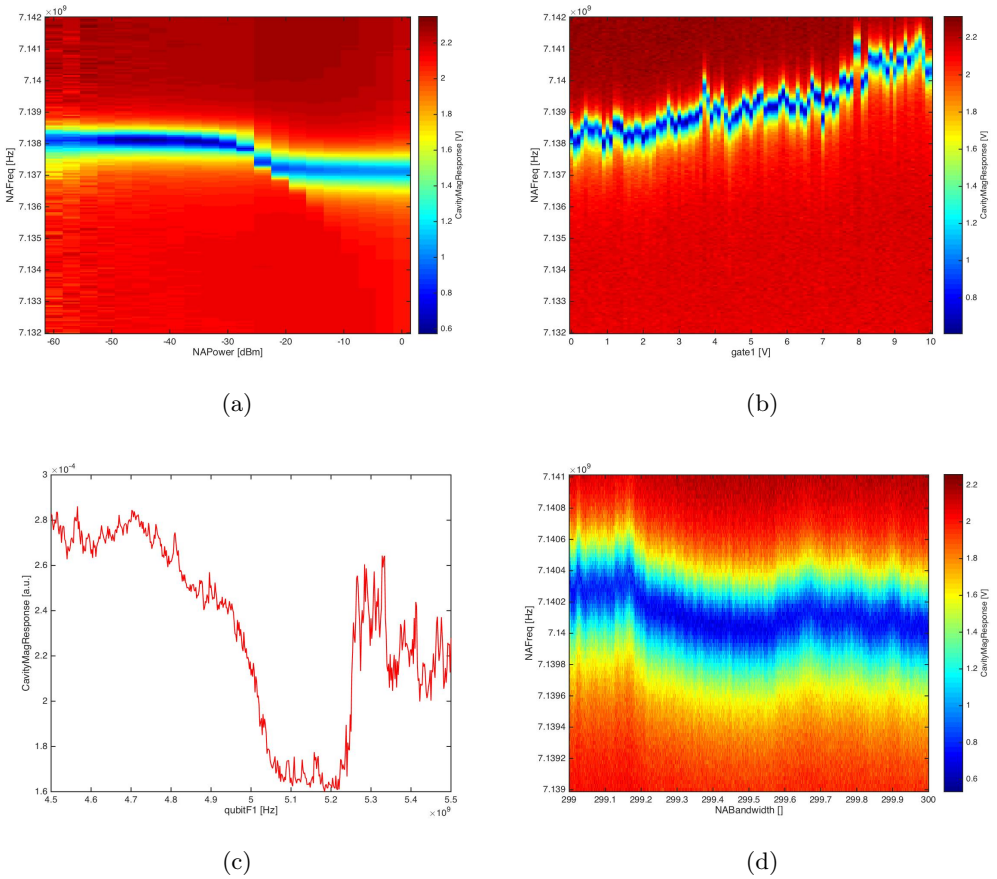

Figure 11: Measurements on a transmon device. a) A power sweep of the cavity indicates the dispersive shift in cavity resonance frequency. b) Driving the qubit through voltage gate shows frequency fluctuations. c) Spectroscopy analysis on the qubit is not successful due to fluctuations. d) A 20 minutes time scan of the qubit

Figure 11(a) indicates a shift in cavity resonance frequency due to coupling to qubit A. The shift is an indication of a functional qubit, coupled to the cavity. The qubit frequency can be obtained from

$$f_q = f_c - \frac{g^2}{\Delta} \tag{13}$$

where the coupling g is 0.1 GHz, detuning Δ is 2.1 GHz and f_c is 7.137 GHz. The qubit

resonance frequency is calculated to be 7.132 GHz. In 11(b), driving the qubit at 0-10 voltage indicates fluctuations in frequency as a function of gate voltage.

As illustrated in 11(c), an spectroscopy analysis on the qubit is performed to find the qubit resonance. Power scan on the qubit through feed line is performed, but the fluctuations in the qubit prevent a clear response in qubit frequency. Due to drifting, the device was left overnight before a time scan was performed to find cavity resonance in 11(d). However the scan result indicates no improvements in the stability of the gate performance.

Possible explanation for the instability of gate performance could be defects in fabrication, which could be connected to the erosion around the contacts and gates. Another suggestion for the drifting gate could be due to nanowire materials. However there is no solid evidence to this, since the nanowire material used in this thesis is untested.

Chapter 7

7 Conclusion And Future Outlook

Employing dielectrophoresis for assembly of nanowires on the transmon devices and testing the functionality of the qubits has demonstrated the method to be an effective alternative to the conventional deposition using a micro-manipulator or a cleanroom wipe. The data obtained from the resonator design indicates a resonator quality factor of $4.8 \cdot 10^5$ at low power, which is consistent with previous measurements obtained in our lab[10]. A higher Q-factor can be achieved by implementing improvements in fabrication steps.

Future outlook would suggest employing a uniform flow of nanowire suspension during assembly to optimize the attraction and alignment of the nanowires in the windows and a high yield in single nanowire deposition. The method provides possibility to rinse away the excess wires around the windows during the assembly once the nanowires are trapped in the patterned windows and aligned in the gaps between the electrodes. Employing this method would probably require different geometries in the electrode design for example employing sharp fingers between the electrodes to direct the wires and help alignment([4]).

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8 Appendix

8.1 Recipes

The recipe used for fabricating the devices is presented here;

(A) Cleaving and cleaning

- Spin AZ1505 4000 rpm, 45 s. Bake 115C for 1 min.
- Scribe/cleave
- Sonicate in acetone/IPA 5 min each at 100 power, 37 kHz, N2 dry.

(B) Aluminum evaporation

- Ion mill for 20s (argon) at 15 sccm, 1 mTorr with 1 min warm up.
- Evaporate 100 nm of Al at 1-2 A/s

(C) Electrode patterning

- Spin coat with AZ1505 at 4000 rpm, 45 s. Bake 115C for 2 min.
- Expose the electrode layer on LED laser writer.
- Develop in AZ-developer 1:1 for 1 min, 30 s DI rinse, N2 dry.
- Oxygen Plasma in asher for 1 min.
- Etch in Al Etch type D for 1 min at 47C. Twice in MQ water for 30s. N2 dry.
- Sonicate in acetone/IPA 2 min each at 50 power, 37 kHz, N2 dry.

(D) Gold alignment marks

- Spin AZ1505 4000 rpm, 45 s. Bake 115C for 2 min.
- Expose gold marks layer on LED writer, aligning to electrode layer
- Develop AZ 1:1 for 1 min., 30 s DI rinse, N2 dry.
- 1 min oxygen plasma ash.
- Evaporate 20 nm Ti at 1 A/s
- Evaporate 80 nm Au at 1 A/s
- Lift-off in acetone at 50C for 20 min. Agitate with syringe to lift off metal after 15 min. 10 s sonication at 50 power, 37 kHz. IPA rinse, N2 dry.

(E) Resist windows

- Spin PMMA A6 4000 rpm, 45 s. Bake 185C for 2 min.
- EBL (Elinoix): align the windows layer on electrode layer
- Develop 1 min. in MIBK:IPA, 10s IPA rinse, N2 dry.
- Oxygen plasma ash for 1 min.

(F) Align nanowires using DEP.

Assembly method using DEP is described in theoretical background section.

(G) Expose etch windows

- spin A4 PMMA at 4000 rpm, 45 s, bake 185 s for 2 min.

- EBL using Elinoix.

- Develop 1 min. in MIBK:IPA, 10s IPA rinse, N2 dry.

- Oxygen plasma ash for 1 min.

(H) etch NW junctions

- Etch in Transene Al Etch type D for 1 min at 47C. Twice for 30s in MQ water rinse. N2 dry.

- Rinse in acetone/IPA 2-3 min each, N2 dry.

- Oxygen plasma ash for 2 min.

(I) Write gates and contacts layer

- Spin A6 at 4000 rpm, 45 s, bake at 185C for 2 min.

- EBL (Elinoix).

- Develop 1 min. in MIBK:IPA, 10s IPA rinse, N2 dry.

- Ion mill for 4 min. 1 min warm up.

- Evaporate 150 nm Aluminum at 1-2 A/s.

- Lift-off in Aceton for 20 min at 47 C, IPA rinse, N2 dry.

- Oxygen plasma ash.

(J) Etch cuts in electrodes.

- Spin A6 PMMA at 4000 rpm, 45 s, bake at 185C for 2 min.

- EBL (Elinoix).

- Develop 1 min. in MIBK:IPA, 10s IPA rinse, N2 dry.

- Etch in Transene Al Etch type D for 1 min at 47C. Twice for 30s in MQ water rinse. N2 dry.

- Rinse in acetone/IPA 2-3 min each, N2 dry.