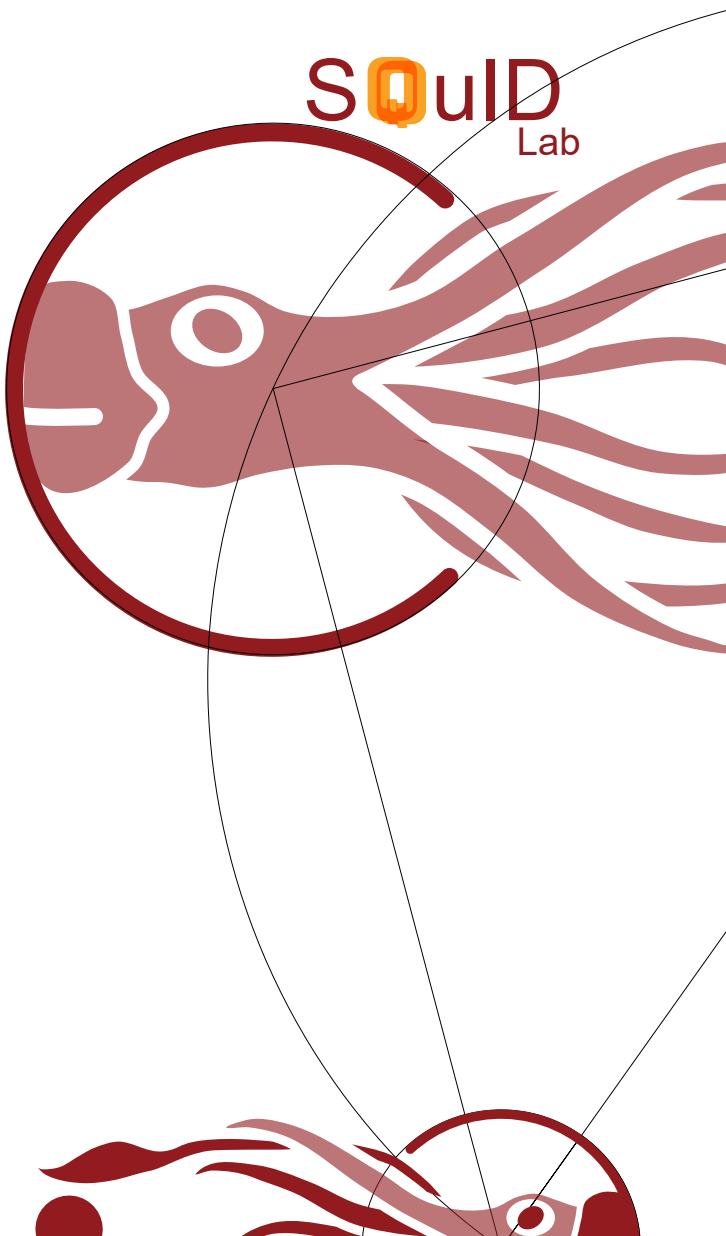
UNIVERSITY OF COPENHAGEN
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Engineering A Single Fluxonium Qubit



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ABSTRACT

Quantum computers have a promising potential to revolutionize technology by addressing problems that are intractable for classical computers due to their unique way of processing information. However, the ideal building blocks for quantum computers have not yet been found. Among the promising candidates, superconducting qubits stand out due to their scalability and ease of fabrication. In particular, the fluxonium qubit shows significant potential due to its low qubit frequencies and high anharmonicity, which are essential for achieving long coherence times and fast qubit control. Fluxonium qubits also offer insensitivity to charge and flux noise, enhancing their stability and coherence time compared to transmons, which are currently the most widely used type. This project aims to target a novel combination of fluxonium parameters, specifically achieving the energy parameters $E_J \approx 4.00\,\mathrm{GHz}$, $E_C \approx 1.0\,\mathrm{GHz}$, $E_L \approx 0.7\,\mathrm{GHz}$ selected based on a comprehensive review of existing experimental and theoretical literature. Using an iterative process of designing, simulating, fabricating, and characterizing the various components of the fluxonium qubit, we have achieved a capacitance energy of $E_C = 1.03\,\mathrm{GHz}$ and a Josephson energy of $E_J = 4.00\,\mathrm{GHz}$. Due to certain constraints, it has not been possible to obtain the desired inductance energy. For qubit readout, we fabricated resonators that exhibited frequencies within 5.3% of the simulated values, with external and internal quality factors in the order of $Q_c \approx 10^4$ and $Q_i \approx 0.5 \cdot 10^6$ in the single-photon regime. This thesis lays the groundwork for a future fluxonium chip design, expected to provide a robust foundation for this research group and which may advance future fluxonium fabrication efforts.

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ACRONYMS

ALD Atomic Layer Deposition. 26

BOE Buffered Oxide Etch. 25, 31

CPW Coplanar Waveguide. 31–33, 53, 54, 66
CVD Chemical Vapor Deposition. 26

FEA Finite Element Analysis. 38

MBE Molecular Beam Epitaxy. 26

PCB Printed Circuit Board. 55, 56
PVD Physical Vapor Deposition. 25

RIE Reactive Ion Etching. 26

SBC Solution Based Chemistry. 26
SI Supplementary Information. 10, 21, 25, 27, 55

TLS Two Level Systems. 29, 31
TWPA Traveling Wave Parametric Amplifier. 57–59, 66

VNA Vector Network Analyzer. 57, 59, 61

1

INTRODUCTION

A normal computer (we could call it a classical computer) computes using bits, which can be in one of two states, either 0 or 1. In contrast, a quantum computer computes using quantum bits, or qubits, which can be in 0, 1 and both simultaneously thanks to quantum mechanics. This fundamental difference in processing information was proposed more than forty years ago by pioneers like Yuri Manin, Paul Benioff, and Richard Feynman [Preskill 2023].

Feynman's talks and lectures are often considered the starting point of quantum computing especially his talk "Simulating Physics with Computers" [Devoret et al. 2004]; [Feynman 1981]; [Mermin 2007]. He proposed a type of computer that was able to perform exact simulations of how nature itself would behave. While classical computers can simulate both classical and quantum physics, they struggle with quantum problems as system size increases. The resources needed for classical simulations grow exponentially with the size of the quantum system, highlighting a fundamental limitation of current classical computation. This raises the question of whether classical computers are limited by their design or if we have reached the limits of classical computation and if a new type of computer, which computes things differently, leveraging quantum mechanics, more efficiently could simulate quantum behavior.

In principle, a quantum computer should be able to reach a point where it can perform tasks that are impossible for a classical computer to solve in a reasonable amount of time. This principle is called quantum supremacy [Preskill 2012]. A milestone in this field was first demonstrated in 2019 by Google, approximately 40 years after the proposal of the quantum computer [Arute et al. 2019]. Google used a 53-qubit quantum processor named Sycamore to sample from a probability distribution that classical computers find extremely challenging to simulate. They claimed their processor completed the task in 200 seconds, whereas the fastest classical supercomputer would need about 10,000 years. However, IBM contested this, suggesting that with optimized methods, the task could be done on a classical computer in just 2.5 days. This debate highlights the ongoing question of whether the limitations of classical computers are due to their design or their inherent capabilities.

The significant global investment in quantum computing by both private and public institutions around the world governments suggests vast potential if a fully functional quantum computer was achieved. While Feynman focused on applications in physics, others have proposed uses in various other fields such as drug development and discoveries, machine learning, cryptography and cyber security, and optimization problems [IBM 2024]; [Preskill 2018].

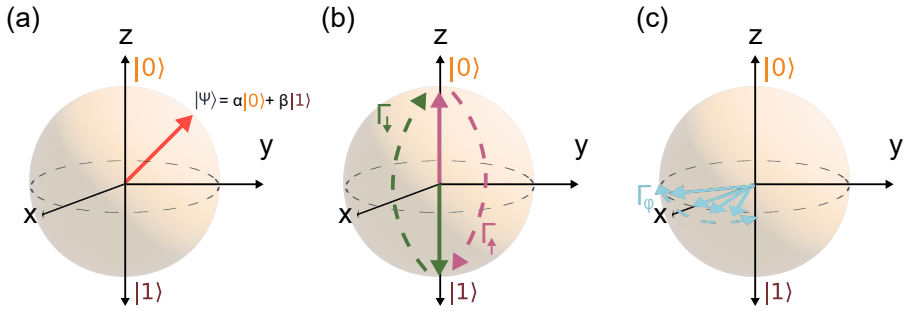


Figure 1: **Computational subspace and decoherence of qubits:** (a) The computational subspace of a single qubit is any quantum state that can be represented as a linear combination (superposition) of the basis states $|0\rangle$ and $|0\rangle$. (b) The qubit relaxation rate due to excitation, $\Gamma_{\downarrow}$, and relaxation, $\Gamma_{\uparrow}$. (c) Qubit relaxation rate due to dephasing, Γ_{φ}.

The criteria of quantum computer

The choice of qubits, the fundamental building block for a quantum computer, is still under development. In 2000, five criteria were proposed for implementing a quantum computer, outlining the necessary properties for these building blocks [DiVincenzo and IBM 2000]. However, with current technology, it is not possible to fulfill all five criteria simultaneously.

One of these criteria is that the qubit must form a well-defined two-level system, which is initializable, e.g., the two first energy eigenstates of the system $|0\rangle$ and $|1\rangle$, and be able to exist in a superposition, $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$ as illustrated in red in Fig. 1 (a). This well-defined two-level system defines the computational subspace, the allowed states of the qubit, in which quantum information is stored and manipulated.

Another criterion, that poses a major challenge in finding a suitable building block for a quantum computer, is the requirement for a long coherence time compared to the gate operation time. Qubit decoherence is when qubits lose their quantum properties and behave classically. The gate time is the time needed to operate, that is to manipulate the qubit state. Decoherence occurs due to qubits experiencing noise from interactions with their surroundings. The decoherence time, T_2, is the total time it takes for a qubit to lose its quantum properties and is given by [Krantz et al. 2019]:

$$\frac{1}{T_2} = \frac{1}{T_1} + \frac{1}{T_\phi} \tag{1}$$

Here, $T_1 = \frac{1}{\Gamma_\uparrow + \Gamma_\downarrow}$ is the longitudinal relaxation time, the time it takes for the qubit to relax to its ground state, and $T_\phi = \frac{1}{\Gamma_\phi}$ is the transverse relaxation time, the time it takes for the qubit to lose its phase information. $\Gamma_{\uparrow(\downarrow)(\phi)}$ indicate the rates of energy release (absorption) and frequency fluctuation, respectively, as shown in Fig. 1 (b) and (c). The decoherence time is crucial for the performance of a quantum computer. The longer the decoherence time, the more calculations the quantum computer can perform before the qubits lose their quantum properties. Understanding the computational subspace and the challenges of decoherence is essential for exploring the various types of qubits and their potential implementations in quantum computers.

Different realizations of qubits

Qubit Type	Two level system	Materials and Components
Superconducting qubits	Energy excitations in an electrical circuit	Superconducting materials fabricated on insulators or semiconductors. Components include resistors, capacitors, and Josephson junctions.
Trapped ions	Excitations of ions trapped in an electromagnetic field	Ions trapped in optical traps. Components include vacuum systems, lasers, and RF coils.
Spin qubits	Spin of electrons or nuclei trapped with electrical or magnetic fields	Semiconductor materials like silicon or GaAs, and magnetic materials for confinement. Components include quantum dots, gates, and magnetic field sources.
Photonic qubits	Polarization, time-bin, or path of photons	Nonlinear optical materials, photonic crystal fibers, and waveguides. Components include lasers, photodetectors, and beam splitters.
Neutral atoms	States of neutral atoms trapped in optical lattices or tweezers	Alkali metals like rubidium or cesium, and laser systems for trapping and manipulation. Components include optical lattices, laser cooling systems, and magnetic traps.

Table 1: **Overview of a selection of different proposed qubit types, how the two-level system is realized, and the materials and components needed for fabrication:** This includes Superconducting qubits, Trapped ions, Spin qubits, Photonic qubits, and Neutral atoms [Blais et al. 2021]; [Cirac and Zoller 1995]; [Devoret et al. 2004]; [Frunzio et al. 2005]; [Girvin 2014]; [Jaksch et al. 1998]; [Knill and La 2001]; [Loss and DiVincenzo 1998].

There are many different proposals for the building blocks of a quantum computer. The most famous include superconducting qubits, trapped ions, spin qubits, photonic qubits, and neutral atoms. Table 1 is an overview of the mentioned selection of different proposed qubit types, how the two-level system is realized, and the materials and components needed for fabrication. Superconducting qubits offer several advantages compared to the other qubit proposals listed below [Devoret et al. 2004]; [Gao et al. 2021]; [Kjaergaard et al. 2020]; [Krantz et al. 2019]; [Stancil and Byrd 2022]:

- **Ease of fabrication and scalability**: Superconducting qubits can be fabricated more easily using well-established semiconductor manufacturing techniques. This allows for scalability and integration into existing technological infrastructure, similar to classical computers.

- **Fast operation times and high fidelity readout**: Superconducting qubits have fast gate operation times, typically in the range of nanoseconds, which is crucial for realizing algorithms that require a series of many gates. Furthermore, superconducting qubits have

demonstrated high-fidelity readout of more than 99% for single-qubit gates, which is essential for performing error correction and achieving fault-tolerant quantum computing in the future.

- **Improved coherence times**: The coherence time of superconducting qubits does not offer a significant advantage over other qubit technologies. However, superconducting qubits are among the most extensively investigated qubits today and due to extensive research and development have led to substantial improvements in coherence times, making superconducting qubits competitive with other qubit technologies.

Due to these advantages namely scalability, fast operation times, and ongoing advancements, superconducting qubits are a compelling choice as building blocks for quantum computers.

Superconducting qubits

Superconductors are used for making qubits because they exhibit a range of remarkable properties at both macroscopic and microscopic scales when cooled below their critical temperature, T_c. Macroscopically, superconductors differ from normal conductors by having two significant properties. Firstly, the magnetic property, known as the Meissner-Ochsenfeld effect, states that a superconductor will expel a weak external magnetic field by creating an equal but opposite magnetization. Secondly, the electrical property, known as persistent current, allows a superconductor to carry a current without an external energy source [Annett 2004]. While both phenomena are fascinating, the electrical property is particularly interesting for quantum computing. It allows superconducting circuits to carry a current without any energy loss, which is crucial for maintaining coherence in qubits. The ability to carry persistent current is due to superconductors exhibiting zero electrical resistivity, $\rho = 0$, and they can therefore carry a flow of electrons without being scattered by phonons or other electrons.

On the microscopic scale, the persistent current is carried by Cooper pairs which are pairs of electrons formed in the superconductor. These Cooper pairs condense into a single macroscopic quantum state, characterized by a complex order parameter, $\psi = |\psi|e^{i\theta}$, where $|\psi|$ can be interpreted as the density of Cooper pairs, and θ is the phase of the superconducting wavefunction. The formation of Cooper pairs leads to an energy gap, Δ, preventing scattering by requiring finite energy to break the pairs. At $T = 0$, the energy gap can be approximated by [Šmidt and Šmidt 1997]:

$$\Delta(0) \approx 1.76 k_B T_c \tag{2}$$

where k_B is the Boltzmann constant and T_c is the critical temperature. The critical temperature is material-dependent, and currently, there are several hundred known superconducting materials [Annett 2004]. However, some superconductors only become superconducting at very high pressures and very low temperatures, and other superconductors are extremely difficult to manufacture. Therefore, only a small selection of the known superconductors is commonly used for fabricating superconducting qubits [Murray 2021]. When fabricating superconducting qubits, we are interested in the different types of superconducting materials and how we can fabricate various components and integrate them into an electrical circuit. Combining the components in different ways allows for the construction of different types of superconducting qubits.

A type of superconducting qubit called a fluxonium qubit offers several key advantages for

quantum computing. Compared to transmon qubits, the most commonly used superconducting qubits, fluxonium qubits are inherently insensitive to charge and flux noise, which significantly enhances their stability and coherence times [Manucharyan et al. 2009]. Additionally, fluxonium qubits have low qubit frequencies and high anharmonicity, which are crucial for achieving long coherence times and fast qubit control [Nguyen, Koolstra, et al. 2022]. Many researchers have become interested in fluxonium qubits due to their unique properties and potential for quantum computing.

This project aims to target a novel combination of fluxonium parameters - specifically the energy parameters E_C, E_J, and E_L - in a configuration that has yet to be experimentally demonstrated. These values have been selected based on a comprehensive study of existing experimental and theoretical literature. The project involves designing, simulating, fabricating, and characterizing the various components of the fluxonium qubit, focusing on each energy parameter individually. The objective of this thesis is to lay the groundwork for a future fluxonium chip design. This initiative is expected to provide a solid foundation for the research group and potentially advance future fluxonium fabrication efforts.

1.1 OUTLINE

In chapter 2 *Background - The components of superconducting circuits and qubits*: The main components of a superconducting circuit will be discussed, and a formalism for describing superconducting qubits will be established. Subsequently, these components will be combined in various configurations to function as superconducting qubits, with their properties discussed in terms of the capacitance energy E_C, the Josephson energy E_J, and the inductive energy E_L. Special attention will be given to the Fluxonium qubit, highlighting its experimental advantages and the discoveries reported in current literature.

In chapter 3 *Nanofabrication and characterization*: The different fabrication techniques used in the thesis are introduced. This includes bottom-up, top-down, double-angle evaporation with an oxidation step, and patching via milling. Further, the general layout of a fluxonium qubit is discussed in terms of the fabrication techniques presented.

In chapter 4 *Targeting EC*: The goal of this chapter is to achieve a capacitance energy of $E_C/h = 1\,\mathrm{GHz}$. We will discuss the different parameters that can be used to tune the capacitance energy and use simulations to optimize the design until the target capacitance is obtained.

In chapter 5 *Targeting EJ - A single Josephson Junction*: In this chapter, we aim to achieve a Josephson energy $E_J/h = 4\,\mathrm{GHz}$ by targeting a specific normal resistance R_N at room temperature. We will discuss the relationship between Josephson energy and critical current, and how normal resistance can be used to determine E_J. The design and fabrication of Josephson junctions, along with simulations and measurements, will be covered to optimize the desired energy.

In chapter 6 *Targeting EL - An array of Josephson Junctions*: In this chapter, we aim to achieve a superinductance energy of $E_L/h = 0.7\,\mathrm{GHz}$. We will discuss the relationship between superinductance energy and normal resistance, and the strategies to achieve the desired E_L. The design, fabrication, and measurement of junction arrays, along with the challenges and optimizations in the fabrication process, will be covered.

In chapter 7 *Targeting wR . Getting the right resonator frequencies*: In this chapter, we aim to design and simulate resonators to achieve knowledge about our quality factors and resonance frequencies. We will discuss the design parameters, fabrication process, and measurement setup. The goal is to match the simulated frequencies with the measured ones and achieve high internal and external quality factors in the single-photon regime.

For the interested reader, a preliminary design for a fluxonium qubit chip will be proposed in the **Outlook chapter** chapter 9. Due to the constraints of this thesis, the design has not been fully finalized yet, and the fabrication is still to be done. In this final chapter, we aim to integrate all the components into a design and outline the steps for further refinement and optimization.

2

BACKGROUND - THE COMPONENTS OF SUPERCONDUCTING CIRCUITS AND QUBITS

In this project, we will work with superconducting circuits, which are electrical circuits made out of superconducting components. Some superconducting circuits can be used as qubits, the fundamental building blocks of a quantum computer. In this chapter, we will investigate how we can describe the superconducting components in terms of current and voltage and express the potential and kinetic energies in our components in terms of flux and charge, a method commonly named circuit quantization. Then, we will discuss how to put the superconducting components together to create different types of superconducting qubits. Finally, we will discuss the fluxonium qubit, which is the qubit we focus on in this project.

2.1 SUPERCONDUCTING CIRCUIT COMPONENTS

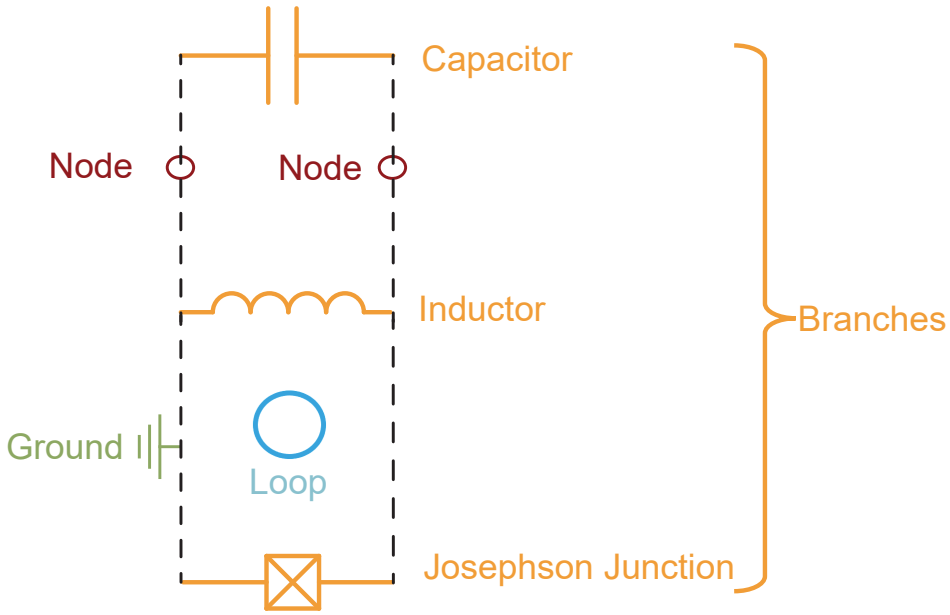


Figure 2: **Diagram of a general superconducting circuit:** Have a capacitor with energy E_C an inductor with energy E_L, and a Josephson junction with energy E_J

The fundamental components in normal electrical circuits are capacitors, inductors, and resistors. As discussed above, when working with superconductors, there is no resistivity. Instead, in superconducting circuits, we typically work with the following components shown in Fig. 2: a capacitor, an inductor, and a Josephson junction. The capacitor contributes to the total circuit energy with a capacitance energy, E_C, and the inductor with an inductive energy, E_L. While

these two elements can be described solely by classical mechanics using Maxwell's equations and Kirchhoff's laws, the Josephson junction behaves quantum mechanically when cooled down to below T_C, where T_C is the critical temperature of the material the Josephson junction is made of. The relation between E_C, E_J, and E_L determines the energy spectrum of the superconducting circuit, which will be discussed later. By combining these components in the right way, we can create a superconducting qubit. In the following sections, we will study the currents and voltages to build a foundation for describing the kinetic and potential energy of the superconducting circuit components.

Just like in classical circuits, we can describe superconducting circuits by nodes and branches. The nodes are the points where different components are connected, indicated by the red dots in Fig. 2. The branches are the wired connections between the nodes containing a single superconducting component, indicated by black lines. Through each branch, there will be a current, I_b, and a voltage difference, V_b, due to the charge and flux difference between the nodes. A flux, Φ_b, can be associated with the voltage difference through the branch. Likewise, a charge, Q_b, can be associated with the current through a branch. We can write the following relations between the voltage and the flux, and the current and the charge.

$$\begin{aligned} \Phi_b(t) &= \int_{-\infty}^{t} V_b\left(t'\right) \mathrm{d}t', \\ Q_b(t) &= \int_{-\infty}^{t} I_b\left(t'\right) \mathrm{d}t', \end{aligned} \tag{3}$$

where one assumes that the system is at rest at $t' = -\infty$. When several branches and nodes enclose a path, we call it a loop. A loop starts and ends at the same node, where no other node is encountered more than once. Each loop will contain an external flux, Φ_{ext}, as indicated in the figure [Krantz et al. 2019]; [Rasmussen et al. 2021]. We are not interested in the dynamics governed by time and will omit the explicit time-dependence in the following, although it is there. Below, we will discuss the energy of the superconducting circuit components.

Capacitors

A capacitor is a linear element also found in normal electrical circuits. The voltage of the capacitor is proportional to the charge stored in the capacitor plates, and the current flow through the capacitor is proportional to the rate of voltage change times the capacitance:

$$\begin{aligned} V(t) &= \frac{q(t)}{C}, \\ I(t) &= C\dot{V}(t), \end{aligned} \tag{4}$$

where C is the capacitance of the capacitor. We can express the energy stored on the capacitor by using the equations in (3) and integrating over the power, $P = V(t)I(t)$, from $t = -\infty$ to $t = t$. This gives us an energy stored in the capacitor often called the kinetic energy [Rasmussen et al. 2021]:

$$T_C = \frac{1}{2} C \dot{\Phi}(t)^2. \tag{5}$$

The kinetic energy, T_C, represents the energy associated with the change in flux across the capacitor.

Inductors

Inductors are found in many places too. The voltage across an inductor is proportional to the rate of change of the current flowing through it.

$$\begin{aligned} V(t) &= L\dot{I}(t), \\ I(t) &= \frac{1}{L}\Phi(t), \end{aligned} \tag{6}$$

Similar to the capacitor, we can integrate over the power from $t = -\infty$ to $t = t$. This gives us the following energy stored in the inductor, refered to as the potential energy [Rasmussen et al. 2021]:

$$U_L = \frac{1}{2L}\Phi(t)^2. \tag{7}$$

The potential energy, U_L, represents the energy stored in the magnetic field of the inductor due to the magnetic flux through it.

Josephson junctions

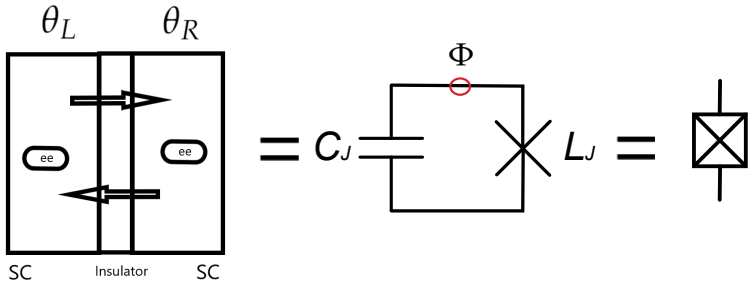


Figure 3: **Schematic drawing of a Josephson junction:** The θ_L and θ_R are the phase of each superconductor. The $\psi_L(\psi_R)$ is the order parameter of the macroscopic quantum state that the Cooper pairs condense into on the left(right) superconductor.

The Josephson junction consists of two superconductors separated by a thin insulating barrier as seen in Fig. 3, also called an SIS junction. In each of the two superconductors, there is an associated superconducting phase, θ_L and θ_R, respectively. The current through the SIS Josephson junction is carried by Cooper pairs, which are pairs of electrons formed by an attractive force that forms in the superconducting regime. An important feature of the Josephson junction is its ability to carry dissipationless current, also called the supercurrent, between the two superconductors. This is called the Josephson effect and is due to the fact that the Cooper pairs can tunnel from one superconductor to the other. The two Josephson equations describing the current and voltage across a Josephson junction are given by [Annett 2004]:

$$\begin{aligned} I(t) &= I_c \sin[\Delta\theta(t)], \\ V(t) &= \frac{\hbar}{2e}\Delta\dot{\theta}(t) \end{aligned} \tag{8}$$

where the phase difference is given by $\Delta\theta(t) = \theta_L(t) - \theta_R(t)$, $\hbar$ is the reduced Planck constant $\frac{h}{2\pi}$, and I_c is the critical current of the Josephson junction. The critical current is the maximum supercurrent that can run through the junction. The critical current is dependent on the geometry

and material of the insulating layer, which we will further discuss in the next sections. When $I(t) > I_c$, the junction will start to dissipate energy and the supercurrent will be destroyed. Combining these equations with the equations in (3), we can relate the charge and the flux.

$$I(t) = I_c \sin\left[\frac{2e}{\hbar}\Phi(t)\right] \tag{9}$$

The Josephson junction can also be described as an electrical circuit with a nonlinear inductance L_J and a parallel capacitance C_J. The Josephson junction works as a flux-dependent inductance, which is given by the following equation [Rasmussen et al. 2021]:

$$L(\Phi) = \left(\frac{\partial I(t)}{\partial \Phi(t)}\right)^{-1} = \frac{\frac{\hbar}{2eI_c}}{\cos\left(\frac{2e}{\hbar}\Phi(t)\right)} \tag{10}$$

Here we see, that the Josephson junction results in a nonlinear inductance. We can write the Josephson inductance as $L_J = \frac{\hbar}{2eI_c}$ and this is related to the dissipationless movement of the Cooper pairs. An attempt at deriving the energy stored in the Josephson junction can be found in SI. The expression for the potential energy can be expressed as [Blais et al. 2021]:

$$U_J = -E_J \cos\left(\frac{2e}{\hbar}\Phi(t)\right), \tag{11}$$

where the Josephson energy is given by $E_J = \frac{\hbar I_c}{2e}$. As we are interested not in the dynamics of our system but in the energy levels, we will omit the time dependence in the following.

2.2 FORMALISM FOR DESCRIBING SUPERCONDUCTING CIRCUITS

Describing superconducting circuit elements in terms of reduced flux

In the previous section, we found expressions for the energies in terms of flux for our three superconducting components. Now we will put these components together in different ways to form superconducting qubits. First, we will introduce the reduced flux given by:

$$\phi = \frac{2\pi}{\Phi_0}\Phi \tag{12}$$

where Φ_0 is the flux quantum equal to: $\Phi_0 = \frac{h}{2e}$. We can write the potential and kinetic energies of our circuit components in terms of the reduced flux. If we do this, we get [Krantz et al. 2019]:

$$\begin{aligned} \text{Capacitor:} \quad & T_C = \frac{C}{2}\left(\frac{\Phi_0}{2\pi}\right)^2 \dot{\phi}^2, \\ \text{Inductor:} \quad & U_L = \frac{1}{2L}\left(\frac{\Phi_0}{2\pi}\right)^2 \phi^2, \\ \text{SIS junction:} \quad & U_J = -E_j \cos(\phi). \end{aligned} \tag{13}$$

From circuit diagram to the Hamiltonian operator

Even though the energy of the capacitance and inductor has a classical description, we need to describe them quantum mechanically when they work as superconducting circuit elements. The system is governed by the time-dependent Schrödinger equation given by:

$$\hat{\mathcal{H}}|\psi(t)\rangle = i\hbar\frac{\partial}{\partial t}|\psi(t)\rangle \tag{14}$$

where the Hamiltonian, $\hat{\mathcal{H}}$, is the operator that describes the total energy of the system, and $|\psi(t)\rangle$ describes the state of the superconducting circuit. The Hamiltonian of the system can be derived from the Lagrangian of the given system and is the difference between the kinetic and potential energy of the system:

$$\mathcal{L} = T - U \tag{15}$$

The kinetic energy is the energy of motion and the potential energy is the energy of position.We can derive the quantum mechanical Hamiltonian operator of the system by quantizing the Hamiltonian found using the Lagrangian. The steps to obtain the quantum Hamiltonian are as follows [Devoret et al. 2004]; [Krantz et al. 2019]; [Møller n.d.]:

1. Draw the circuit diagram of your superconducting circuit.

2. Label the nodes and branches. To every branch, you can associate a reduced flux ϕ_b.

3. In every superconducting loop, a supercurrent occurs that you can floxoid quantize by a 2 π period. Make the sum of every reduced flux quantum in the loop equal to zero to make the rest of the recipe easier. If possible, use this to reduce the number of flux variables.

4. Setting up the Lagrangian of the system in terms of the reduced flux

$$\mathcal{L} = \sum_i (T_C(\phi_i) - U_L(\phi_i) - U_J(\phi_i))$$

   where i denotes a branch containing only one superconducting element and an associated reduced flux.

5. Define the momentum conjugate to the flux.

$$Q = \frac{\partial \mathcal{L}}{\partial \dot{\Phi}} = \frac{\partial \mathcal{L}}{\partial \dot{\phi}}\frac{2\pi}{\Phi_0}$$

6. Write the Hamiltonian for the system.

$$\mathcal{H} = \sum_i Q_i\dot{\Phi}_i - \mathcal{L} = \sum_i \frac{\partial \mathcal{L}}{\partial \dot{\phi}_i}\dot{\phi}_i - \mathcal{L}$$

7. We can now quantize the classical Hamiltonian to be able to describe the quantum behavior of the system. For this, we need to define the commutation relation between the flux and the charge.

$$[\hat{\Phi}, \hat{Q}] = i\hbar$$

Like the reduced flux, we can define the reduced charge, also called the number operator which counts the number of Cooper pairs on an island.

$$\hat{n} = \frac{\hat{Q}}{2e}$$

Which fulfills the following commutation relation:

$$[\hat{\phi}, \hat{n}] = i$$

Following this procedure will help us obtain the quantized Hamiltonian, $\hat{\mathcal{H}}$, of a simple arbitrary superconducting circuit. The Hamiltonian will be used to find the eigenvalues and eigenvectors of the system. The eigenvalues will give us the energy levels of the system and the eigenvectors will give us the wave functions of the system. However, inserting the Hamiltonian in Eq. (14) and finding the energies in this way can be quite tricky. Instead, we can perform a numerical analysis of the Hamiltonian operator, which we will discuss in the next section.

Numerical analysis of the Hamiltonian operator

In order to make a numerical analysis of a Hamiltonian, we need a discrete matrix representation. We can then diagonalize the Hamiltonian to find the eigenvalues and eigenstates. For convenience, either the flux basis or the charge basis is chosen [Aumann et al. 2022].

Flux basis

In the Flux basis, the reduced flux can be written as a diagonal matrix [Aumann et al. 2022].

$$\hat{\phi} = \begin{pmatrix} -\phi_{\max} & & & & \\ & -\phi_{\max}+\delta & & & \\ & & \ddots & & \\ & & & \phi_{\max}-\delta & \\ & & & & \phi_{\max} \end{pmatrix} \tag{16}$$

Where δ is the step size defined as $2\Phi_{max}/(N-1)$, where N is the dimension of the matrices defining how good our approximation is. We take ϕ_{max} to be 2 π periodic making the grid go from $-\pi$ to π. In the flux basis, the number operator can be expressed as $\hat{n} = \frac{\hat{Q}}{2e} = -i\partial/\partial\hat{\phi}$ and $\hat{n}^2 = -\partial/\partial\hat{\phi}^2$. The charge operator can be written as a matrix of the form:

$$\hat{n} = \frac{-\mathrm{i}\hbar}{4\mathrm{e}\delta}\begin{pmatrix} 0 & 1 & & & \\ -1 & 0 & 1 & & \\ & & \ddots & & \\ & & -1 & 0 & 1 \\ & & & -1 & 0 \end{pmatrix}, \hat{n}^2 = \frac{-\hbar^2}{4\mathrm{e}^2\delta^2}\begin{pmatrix} -2 & 1 & & & \\ 1 & -2 & 1 & & \\ & & \ddots & & \\ & & 1 & -2 & 1 \end{pmatrix} \tag{17}$$

For some circuits, it can be useful to describe the system in the charge basis instead of the flux basis. This approach is described below.

Charge basis

In the charge basis, the charge is a diagonal matrix and the number operator can be expressed as [Aumann et al. 2022]:

$$\hat{n} = \begin{pmatrix} -n_{cutoff} & & & & \\ & -n_{cutoff}+1 & & & \\ & & \ddots & & \\ & & & n_{cutoff}-1 & \\ & & & & n_{cutoff} \end{pmatrix} \tag{18}$$

Where the n_{cutoff} is the maximum number of Cooper pairs on the island. The precision of our simulation, N, is now defined as $N = 2 \cdot n_{cutoff}$ where n_{cutoff} is an integer. In the charge basis, the reduced flux is expressed in terms of cosine:

$$\cos\left(\hat{\phi}\right) = \frac{1}{2}\left(e^{i\phi} + e^{-i\phi}\right) \tag{19}$$

Where the exponential can be written in terms of a matrix of the form:

$$e^{i\frac{\hat{\Phi}}{\Phi_0}} = \left(e^{-i\frac{\hat{\Phi}}{\Phi_0}}\right)^{\dagger} = \begin{pmatrix} 0 & & & \\ 1 & 0 & & \\ & \ddots & & \\ & & 1 & 0 \end{pmatrix} \tag{20}$$

By representing the Hamiltonian in one of the two discrete bases mentioned above, we can numerically calculate its eigenvalues and eigenvectors. This will be useful later when we analyze different superconducting circuits to determine which ones are suitable for use in a quantum computer.

2.3 SUPERCONDUCTING BUILDING BLOCKS FOR A QUANTUM COMPUTER

Now we have studied the current and voltages running in the three superconducting components; inductors, capacitors, and Josephson junctions. We have also learned how to describe superconducting circuits containing these components. We saw how we could get the quantized Hamiltonian of our circuit, as well as how to numerically analyze the energy levels of the system by writing the Hamiltonian in either the flux basis or the charge basis. Now we will use these procedures to describe and analyze different superconducting circuits. Along the way, we will discuss what properties we want our qubits to have and what combinations of the superconducting components will give us the right properties.

2.3.1 *The LC circuit - Quantum harmonic oscillator*

Let's start with one of the simplest circuits, the LC harmonic oscillator. The LC harmonic oscillator is a circuit consisting of a capacitor and an inductor as seen in fig.4 (a). We can follow the steps discussed above. Since we have no enclosed path, we also do not have any loops, and we can go directly to write down the Lagrangian of our circuit:

$$\mathcal{L}_{LC} = \frac{C}{2}\left(\frac{\Phi_0}{2\pi}\right)^2 \dot{\phi}^2 - \frac{1}{2L}\left(\frac{\Phi_0}{2\pi}\right)^2 \phi^2 \tag{21}$$

We can then get the momentum conjugate to the flux and write the quantized Hamiltonian of the system in terms of the reduced charge:

$$\hat{\mathcal{H}}_{LC} = 4E_C\hat{n}^2 - \frac{1}{2}E_L\hat{\phi}^2 \tag{22}$$

where we have the capacitive energy, E_C and the inductive energy, E_L, to be:

$$E_C = \frac{e^2}{2C}, E_L = \left(\frac{\Phi_0}{2\pi}\right)^2 \frac{1}{L}.$$

We can find the spectrum of the quantized Hamiltonian numerically and get the potential, eigenenergies as well as the wave functions of the LC circuit using the flux basis. This is shown in Fig. 4 (b) where the blue is the potential plotted along with the first 4 energy levels. The dashed lines are the eigenenergies of each state $|m\rangle$ and the solid lines are the corresponding wave function. As seen in the figure, the Hamiltonian in Eq. (22) describes a quantum harmonic oscillator.

The energy difference between two energy states, let us say between $|0\rangle$ and $|1\rangle$, are given by $hf_{10} = E_1 - E_0$. The anharmonicity, α, is defined to be the change in energy difference between eigenstates. One often associate the anharmonicity, α, between the the first two energy transitions, ω_{10} and ω_{21}. The anharmonicity is given by $\alpha_1 = \alpha = \omega_{10} - \omega_{21}$ where $\omega = f \cdot 2\pi$. As seen in fig. 4 (b), the energy levels are equally spaced, meaning there is no anharmonicity $\alpha = 0$ and $\omega_{10} = \omega_{21} = \omega_{32} = \omega_{43}$. We want a large anharmonicity between the two lowest energy levels, $hf_{10} = E_0$ and E_1, and the $hf_{21} = E_1$ and E_2 if we are going to use the circuit as a qubit. This is because you want to be able to manipulate the qubit without exciting it to higher energy levels. If there is an equal spacing between the energy levels, you cannot control which state you excite.

Therefore, the LC circuit is not a good building block for a quantum computer as there is no anharmonicity. We need to come up with another circuit containing a nonlinear element that introduces anharmonicity to our system. The commonly used superconducting component for creating anharmonicity is the Josephson junction.

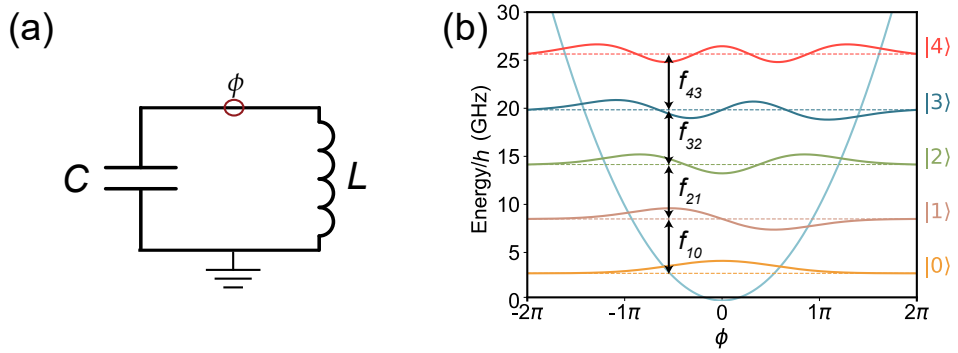


Figure 4: **Circuit diagram and energy spectrum of the LC circuit:** (a) Circuit diagram of the LC circuit. (b) The energy levels of the LC circuit as a function of the reduced phase. The dashed lines are the eigenenergies of each state $|m\rangle$ and the filled lines are the corresponding wave function.

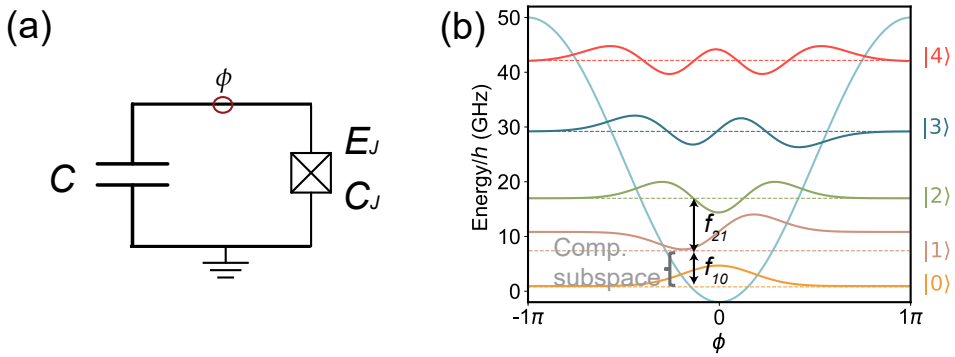


Figure 5: **Circuit diagram and energy spectrum of the CJ circuit:** (a) The circuit diagram of a CJ circuit. (b) The energy levels of the CJ circuit as a function of the reduced phase ϕ simulated in the flux basis. The potential is shown in blue and the dashed lines are the eigenenergies of each state $|m\rangle$ and the solid lines are the corresponding wave function.

2.3.2 *The CJ circuit - Cooper Pair Box*

The most simple circuit we can think of which contains a Josephson junction, is a capacitor in parallel with a Josephson junction. This circuit is called a Cooper pair box or a charge qubit and its circuit diagram is shown in Fig. 5 (a) [Krantz et al. 2019]; [Nakamura et al. 2002]. The Hamiltonian of the Cooper pair box is given by:

$$\hat{\mathcal{H}}_{CPB} = 4E_C\left(\hat{n} - n_g\right)^2 - E_J\cos(\hat{\phi}) \tag{23}$$

Where E_C is the charging energy, E_J is the Josephson energy.

$$E_C = \frac{e^2}{2C_\Sigma}, E_J = \frac{I_c\Phi_0}{2\pi}.$$

The total Capacitance, $C_\Sigma = C + C_J$, is the sum of the different capacitances in our system. The charge offset, n_g, can shift the energy levels of the superconducting quantum circuit. As seen in the Fig. 5 (b), the anharmonicity, $\alpha = (f_{21} - f_{10})2\pi$ is nonzero oppose to the LC circuit.

Therefore, the Cooper pair box is a simple circuit that can be used as a qubit. The Cooper pair box is used as a qubit by manipulating the two lowest energy states, $|0\rangle$ and $|1\rangle$, of the circuit, which is now our computational subspace. The eigenenergies of the first five states are shown in Fig. 6(b). The energy of the states changes with the offset charge, which is a disadvantage when controlling the qubit, as fluctuations in the charge change your energy and thereby your computational subspace.

2.3.3 *The CJ circuit - Transmon qubit*

In the regime where $E_J >> E_C$ which is around $E_J/E_C = 50$, the energy is insensitive to the charge offset as seen in Fig. 6 (c), meaning the computational subspace will not change if there is small fluctuations of the charge around the qubit. We say that the qubit is insensitive to charge noise. This regime is called the Transmon regime and the associated qubit is called a Transmon

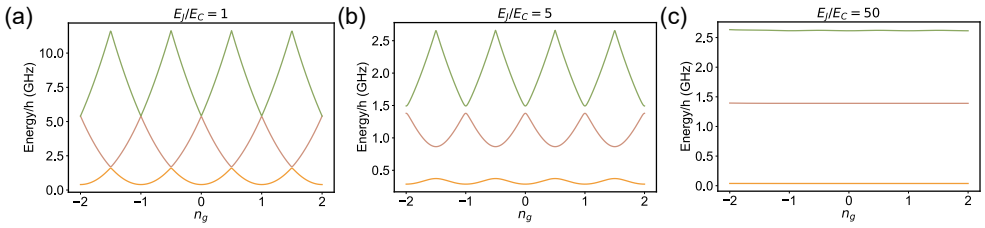


Figure 6: **Energy ratio regimes of the CJ circuit:** The first 3 energy levels of the CJ circuit as a function of the offset charge for 3 different regimes. The energy levels are computed using the charge basis. (a) and (b) The 2 first regimes $E_J/E_C = 1$ and $E_J/E_C = 5$ is in the Cooper pair regime as the energy is dependent on the offset charge. (c) The last regime $E_J/E_C = 50$ is the Transmon regime and the energy levels are insensitive to the charge offset.

qubit. The Hamiltonian of the Transmon is essentially the same as the Cooper pair box except that it is now insensitive to the charge offset.

$$\hat{\mathcal{H}}_{Transmon} = 4E_C(\hat{n} - n_g)^2 - E_J\cos(\hat{\phi}) \tag{24}$$

The Transmon qubit is a very popular building block in quantum computers due to its simplicity and the insensitivity to charge noise [Houck et al. 2009]. The Transmon qubit frequency, $\omega_q = (f_{21} - f_{10}) \cdot 2\pi$, is typically designed to be around 3-6 GHz [Krantz et al. 2019]. These are the optimized values if one still wants to fulfill the condition $E_J >> E_C$. However, being in this regime results in small anharmonicity, α_1, around 100-300 MHz which is very small compared to the qubit frequency. This low anharmonicity limits the protection from leakage to higher states than the one in our computational subspace and also limits the speed of gate execution. The highest coherence time, that is the lifetime in which one can operate the qubit in the quantum regime, is currently around 0.5 ms [Wang et al. 2022]. However, as mentioned before, one wants to be able to make many operations on each qubit which is why one seeks different qubits with longer decoherence times. The Transmon is only using two out of the three superconducting components available. The last component is the inductor which we will discuss in the next section.

2.3.4 *The CLJ circuit*

We will now look at the simplest circuit containing all three superconducting components, namely the inductor, capacitor and Josephson junction. The circuit diagram for the CLJ circuit can be seen in Fig. 7 (a). Since we have a closed path, a loop, we have an external flux given by:

$$\phi_{ext} = \phi_1 + \phi_2 \Leftrightarrow \phi_1 = \phi_{ext} - \phi_2 \tag{25}$$

The Hamiltonian of this circuit is given by:

$$\hat{\mathcal{H}}_{CLJ} = 4E_C\,(\hat{n})^2 - E_J\cos(\phi_{ext} - \hat{\phi}_2) - \frac{1}{2}E_L\hat{\phi}_2^2 \tag{26}$$

Where we have the capacitive energy, E_C, the inductive energy, E_L, and the Josephson energy, E_J to be:

$$E_C = \frac{e^2}{2C_\Sigma}, E_J = \frac{I_c\Phi_0}{2\pi}, E_L = \left(\frac{\Phi_0}{2\pi}\right)^2\frac{1}{L}.$$

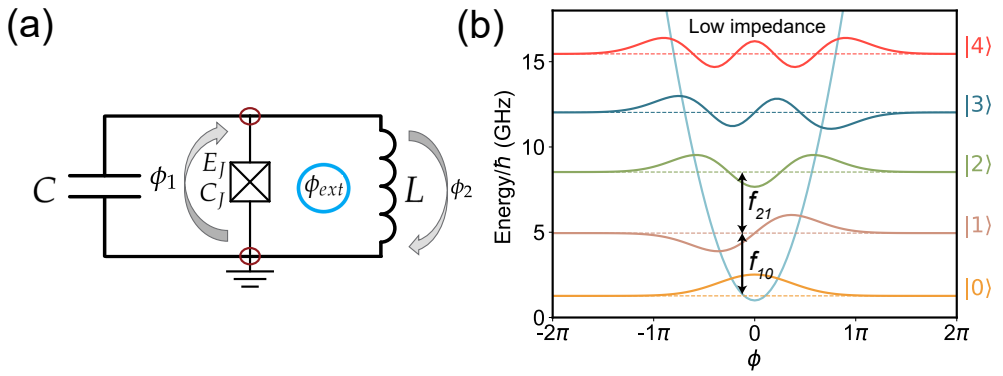


Figure 7: **Circuit diagram and energy spectrum of a CLJ circuit:** (a) The Circuit diagram of a CLJ circuit. (b) The energy levels of the CLJ circuit as a function of the reduced phase ϕ. The energy difference between the levels is not equally spaced meaning $f_{21} - f_{10} \neq 0$.

Where $E_L >> E_J$. This circuit reminds of a fluxonium qubit, except that in this case, the circuit contains a normal inductor and not a superinductor. The relation between the energies, E_C, E_J, and E_L determines the shape of the potential.

If the inductor is modeled as a thin wire with length, $l \propto L$ and $l \propto C$, where L is inductance and C is the self capacitance, then the impedance is similar to the one of a resonator with impedance $Z_L = \sqrt{L/C}$. Likewise, the eigenfrequency of the inductor is $\omega_L = 1/\sqrt{LC} = Z_L/L$. The inductor frequency decreases with increasing length. When the length of the wire is increased, the self-capacitance increases correspondingly which is why the order of the impedance does not change but stays constant. The impedance stays around, 377Ω, which is much less than the resistance quantum, R_Q where $R_Q = h/(2e)^2 \approx 6.5k\Omega$ [Manucharyan et al. 2009]. The frequencies corresponding to this impedance are in the GHz range which is the same range in which the superconducting qubits are manipulated. The eigenfrequency of the inductor, ω_L should not match or be smaller than the qubit frequency, as you might excite the inductor instead of controlling the state of the qubit. Therefore using a wire as an inductor for these types of circuits can be problematic.

Instead of using a traditional wire as an inductor in the CLJ circuit, we can construct the inductor using an array of Josephson junctions to achieve a linear kinetic inductance. Instead of using a wire as an inductor, we can try to construct the inductor differently. We can use an array of Josephson junctions to make a linear kinetic inductance. Using this approach will result in a higher impedance and thereby also higher frequencies of the inductor which we will see in the next section.

Superinductance

The circuit diagram for the CLJ circuit where the inductor, L, is replaced with an array of N Josephson junctions each with Josephson energy, E_{JA}, can be seen in Fig. 8. We assume that the

reduced flux, ϕ_2, is divided equally among all the Josephson junctions in the array leading to a flux of $\phi_2/N = \phi_2'$ over each junction. The potential of the array can then be written as:

$$U_{JA} = -NE_{JA}cos\left(\frac{\phi_2}{N}\right) \tag{27}$$

When N becomes large, $\frac{\phi_2}{N}$ becomes small and we can expand the potential in terms of the cosine. Note that f_T is the taylor polynomial taking in the function $U_{JA}\left(\frac{\phi_2}{N}\right)$

$$\begin{aligned} f_T\left(U_{JA}\left(\frac{\phi_2}{N}\right)\right) &= U_{JA}(0) + \frac{U'_{JA}(0)}{1!}\left(\frac{\phi_2}{N}\right) + \frac{U''_{JA}(0)}{2!}\left(\frac{\phi_2^2}{N^2}\right)\dots \\ U_{JA}\left(\frac{\phi_2}{N}\right) &= -NE_{JA}cos\left(\frac{\phi_2}{N}\right) \rightarrow U_{JA}(0) = -NE_{JA} \\ U'_{JA}\left(\frac{\phi_2}{N}\right) &= NE_{JA}sin\left(\frac{\phi_2}{N}\right) \rightarrow \frac{U'_{JA}(0)}{1}\left(\frac{\phi_2}{N}\right) = 0 \\ U''_{JA}\left(\frac{\phi_2}{N}\right) &= NE_{JA}cos\left(\frac{\phi_2}{N}\right) \rightarrow \frac{U''_{JA}(0)}{2!}\left(\frac{\phi_2^2}{N^2}\right) = \frac{E_{JA}}{2N} \end{aligned} \tag{28}$$

We stop at the second-order term, as all the odd terms will contain a sine component, resulting in zero, and higher even terms, such as the fourth order, become negligibly small as you divide by N to a high power. Putting everything together, we end up with the following potential for the Josephson array containing N Josephson junctions:

$$U_{JA} = -NE_{JA} + E_{JA}\frac{1}{2N}\phi_2^2 \tag{29}$$

The first term is a constant that is not dependent on the reduced flux, ϕ_2, and can be shifted to zero. The second term is the inductive energy of the array of Josephson junctions. This looks like the potential energy of a linear inductor and the final expression for the array is given by:

$$U_{JA} = E_{JA}\frac{1}{2N}\phi_2^2 \tag{30}$$

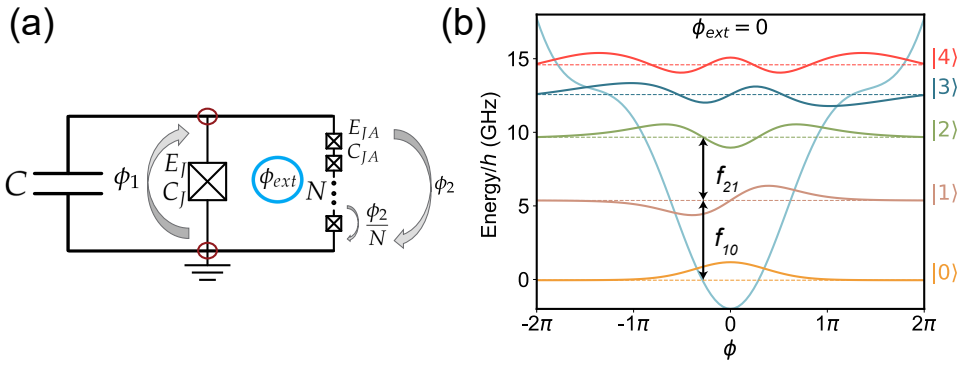


Figure 8: **Circuit diagram and energy levels of a Fluxonium qubit** (a) shows the circuit diagram of a Fluxonium qubit circuit. (b) The energy spectrum of a Fluxonium qubit at $\phi_{ext} = 0$. The energy levels are simulated using the flux basis. The energy levels are not equally spaced meaning $f_{21} - f_{10} \neq 0$.

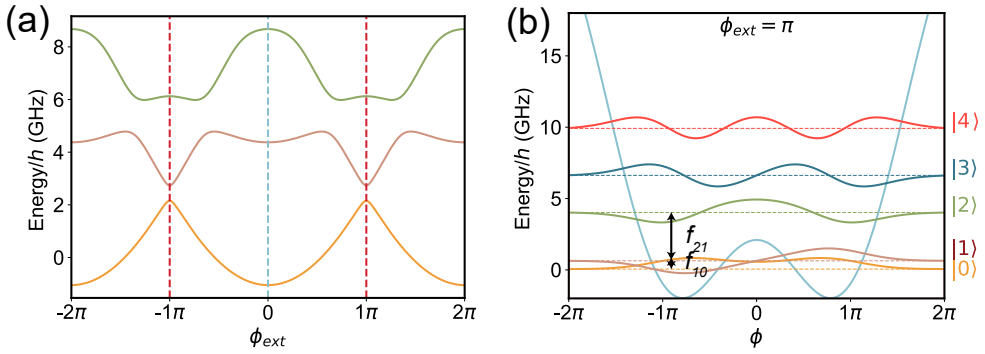


Figure 9: **Energy levels of the Fluxonium qubit at $\phi_{ext} = 0, \pm\pi$:** (a) The Energy as a function of the external flux, ϕ_{ext}, for the first three states of a FLuxonium circuit. Highlighted is the $\phi_{ext} = 0$ in blue and the two sweet spots, $\phi_{ext} = \pm\pi$ in red. (b) The energy levels of the Fluxonium qubit as a function of the reduced phase $\phi_2 = \phi$ at the sweet spot, $\phi_{ext} = \pi$. The energy levels are computed using the flux basis.

Even though a single Josephson junction is associated with a nonlinear inductor, the array of N Josephson junctions can be approximated as a kinetic linear inductor with impedance, $Z_L > R_Q$, larger than the resistance quantum. The inductor fulfilling this criterion is called a superinductor and this type of component is very useful as we can now obtain $\omega_L >> \omega_q$, that the eigenfrequency of our inductor is much larger than our qubit frequency. Replacing the geometric inductor with the new kinetic superinductor in the CLJ circuit can be used to create a Fluxonium qubit described in the following section.

2.3.5 *The CLJ circuit - Fluxonium qubit*

The Fluxonium qubit consists of a capacitor coupled in parallel to a Josephson junction and an array of Josephson junctions, which is approximated as a superinductor, as seen in Fig. 8 (a). The Hamiltonian is given by [Krantz et al. 2019].

$$\hat{\mathcal{H}}_{Fluxonium} = 4E_C\hat{n}^2 - E_J cos(\hat{\phi}_2 - \phi_{ext}) + \frac{1}{2}E_L\hat{\phi}_2^2 \tag{31}$$

Where we have the capacitive energy, E_C, the superinductive energy, E_L, and the Josephson energy, E_J to be:

$$E_C = \frac{e^2}{2C_\Sigma}, E_{J1} = \frac{I_c\Phi_0}{2\pi}, E_L = \frac{E_{JA}}{N}.$$

The Fluxonium regime is fulfilled when the relationship of the energies satisfies:

$$1 \geq \frac{E_J}{E_L}, \frac{E_J}{E_C} \geq 10 \tag{32}$$

where one often take the number of junctions, $N = 100$ [Nguyen, Koolstra, et al. 2022]. By changing the ratio between ϕ_{ext}, E_C, E_J, and E_J we can modify the energy spectrum. We will explore the effects of varying parameters through a numerical analysis of the Hamiltonian in the flux basis, allowing us to systematically alter each parameter and observe its impact.

Changing the external flux, ϕ_{ext}, changes the gap between the energy levels as seen in Fig.

9 (a). At $\phi_{ext} = 0$ our computational subspace, that is the qubit frequency $\omega_q = \omega_{10} = E_2 - E_1$, are large and the anharmonicity, $\alpha = \omega_{21} - \omega_{10}$ is small. This is indicated in the blue dashed line. We see the opposite at $\phi_{ext} = \pm\pi$, indicated by the dashed red lines, where the qubit frequency is small and the anharmonicity is large. In order to minimize the leakage to energy levels outside the computational subspace, one wants to aim for a large anharmonicity. Increasing anharmonicity decreases the probability of leaking to higher energy levels than the computational subspace [Nguyen, Koolstra, et al. 2022]. Therefore, we want our external flux, ϕ_{ext}, to be π. This is also called the flux sweet spot which also features insensitivity to flux noise up to first order [Krantz et al. 2019].

Changing the capacitance energy, E_C is equivalent to giving the Cooper pairs more potential energy. This will increase the spacing between all the energy levels. Having a larger value of E_C can be good because it makes a large anharmonicity. $\alpha = \omega_{21} - \omega_{10}$. However, it should not be too large as it will separate the two first levels and make f_{10} too large which will reduce the coherence time.

The last thing we will look at is the ratio between E_J and E_L. This ratio shapes the potential of the circuit as well as the anharmonicity between the states. For small ratios $E_J/E_L \approx 1$, the potential will have a single well as seen in Fig. 7 (b) and for larger ratios $E_J/E_L > 3$, the potential will be a double well. The larger the difference between E_J and E_L, the larger the anharmonicity between ω_{01} and ω_{12}. At first glance, this is what we wish to obtain, but too large E_J/E_L will also make the qubit frequencies too large.

Until now, we have only discussed the ratios, and not the actual values of the energies. In the next section, we will look at different articles and based on these, we will optimize the ratios between the three energies, E_C, E_J, and E_L to obtain the optimal values for the Fluxonium qubit. At this initial step of qubit device design and fabrication, we want to optimize to the two coherence times T_1 and T_2. The T_1 (longitudinal) relaxation time says something about the energy relaxation process and how fast it decays from the ground state to the excited state. The T_2 (transversal) relaxation time, says something about the phase relaxation process and how long time the superposition (the quantum behavior of the qubit) is preserved. There are different ways of optimizing qubits than based on their coherence times, however, we will not touch upon these in this thesis.

Experimental discoveries of Fluxonium fabrication so far

After the proposal of utilizing quantum mechanics to build a quantum computer by Benioff and Feynman in the beginning of the 80s, it was not until 1997, that the first superconducting building block, the Cooper pair box, was proposed [Benioff 1980]; [Feynman 1981]; [Shnirman et al. 1997]. One of the first Cooper pair boxes only had a coherence time (T_1) of 0.0016 µs [Nakamura et al. 2002]. The coherence times (T_1 and T_2) as a function of the year, are plotted in Fig. 10 where Fig. 10 #1 is the coherence time of the Cooper Pair Box. One of the reasons the coherence time was so low, was due to the high sensitivity to charge noise.

The Transmon, a specific version of the Cooper Pair Box, was proposed in 2007 by Koch et al. [Koch et al. 2007]. The Transmon qubit was a big improvement from the Cooper pair

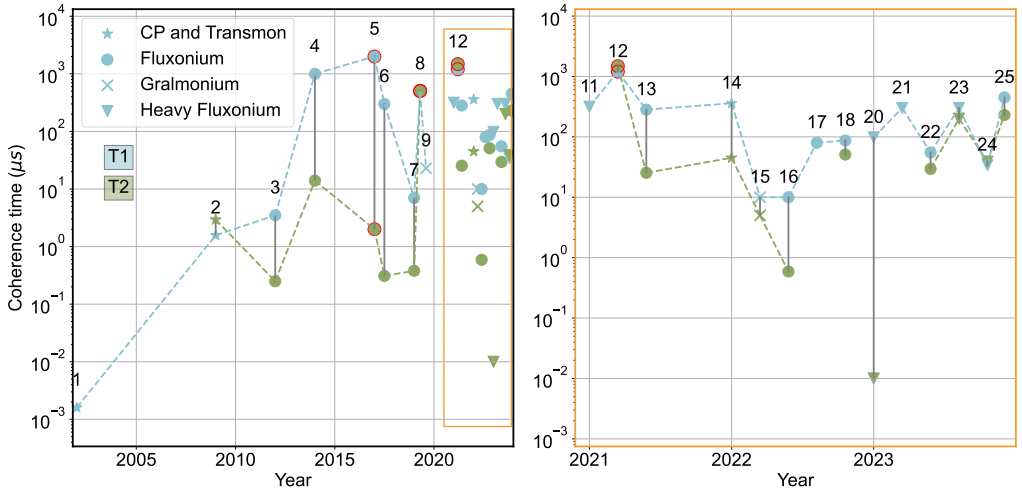


Figure 10: **Timeline of single fluxonium qubit coherence times (T_1 and T_2):** The coherence times (T_1 in blue and T_2 in green) of the fluxonium qubit is plotted as a function of the year. The coherence times are plotted as a log scale. Each paper is marked with a number corresponding to the following references (in chronological order) [Bao et al. 2022]; [Ciani et al. 2022]; [L. Ding et al. 2023]; [Ficheux et al. 2021]; [Grünhaupt et al. 2019]; [Gusenkova et al. 2022]; [Hazard et al. 2019]; [Houck et al. 2009]; [Kou et al. 2017]; [Lin et al. 2017]; [Manucharyan et al. 2009]; [Moskalev et al. 2023]; [Najera-Santos et al. 2023]; [Nakamura et al. 2002]; [Nguyen, Lin, et al. 2019]; [Pita-Vidal et al. 2020]; [Pop et al. 2014]; [Rieger et al. 2022]; [Simakov et al. 2023]; [Somoroff, Ficheux, et al. 2021]; [Somoroff, Truitt, et al. 2023]; [Sun et al. 2023]; [Wang et al. 2022]; [Zhang, Chakram, et al. 2021]; [Zhang, C. Ding, et al. 2023]. The first two points, #1 and #2, are the first Cooper pair box qubit and the Transmon qubit, respectively. The graph on the right is a zoom-in on the coherence times of the fluxonium qubit from the year 2021 to 2023. The distances between the points on the x-axis have been adjusted for visibility, and are only accurate to the year, not the specific month. The circles indicate regular Fluxonium, the triangles indicate Heavy Fluxonium and the cross indicates Fluxonium qubits made of Granular Aluminum (Gralmonium). The full study of the papers mentioned above can be found in SI.

box as it was insensitive to charge noise. The T_1 coherence time of some of the first Transmon qubits was around 1.57 µs as seen in Fig. 10 #2 [Houck et al. 2009]. This was an improvement of almost 10^3 times. Now in 2022, more than 10 years after the first Transmon, the T_1 coherence times of Transmons have just barely improved to 0.5 ms while limited of the T_2 coherence time of 45 µs [Wang et al. 2022] Fig. 10 (c). One of the challenges with the Transmon qubit is the small anharmonicity of around 100-300 Mhz which originates from the large ratio between the Josephson energy, E_J, and the inductive energy, E_L. This limits the protection from leakage to higher states than the one in our computational subspace and also limits the speed of gate execution [Kjaergaard et al. 2020].

The first Fluxonium device was suggested by Manucharyan et al. in 2009 as a part of his work as a PhD work [Catelani 2019]; [Manucharyan et al. 2009]. In his paper, they proposed four main criteria for making a Fluxonium qubit:

1. The inductance of the array should be much larger than the inductance of the single Josephson junction:
$$NL_{JA} \gg L_J$$
2. The impedance of the array $Z_{JA} = \sqrt{L_{JA}/C_{JA}}$ and also tells us something about the minimum size of the array junctions necessary to reduce the offset charge:
$$e^{-8R_Q/Z_{JA}} << 1$$
3. One wants to reduce the size of the quantum phase slip. The quantum phase slip changes the phase of our quantum state which makes the energy of the qubit shift. Therefore, $Z_{JA} >> Z_J$ leading to the relation:
$$Ne^{-8R_Q/Z_{JA}} << e^{-8R_Q/Z_J}$$
4. The capacitive coupling to the ground should be less than the capacitive coupling to the individual junctions in the array - it is this last point that limits the maximum number of junctions and hence the maximum inductance:
$$N < (C_{JA}/Cg)^{1/2}$$

However, it should only be in 2014 that the Fluxonium qubit could obtain T_1 coherence times longer than the Transmon of almost 1000 µs and with T_2 coherence times of around 14 µs [Pop et al. 2014]. A peak can be seen in Fig. 10 #5 with a $T_1 \approx 2000$ µs however, this Fluxonium is heavily limited by $T_2 \approx 2$ µs [Lin et al. 2017]. In the theoretical paper, *Right-sizing fluxonium against charge noise*, they talk about how to make the array in the fluxonium qubit the right size in terms of charge noise [Mizel and Yanay 2020]. They state that the number of junctions, N, in the array, should depend on the energy values, E_J, E_C, and E_L. They claim, that if you do not have the right N for the given energies, it will limit the T_2 coherence time. They even looked at the previous paper mentioned namely [Lin et al. 2017], where they found that for their energy parameters, they should have had $N = 12$ which was very different from their experimental value of 102 Junctions. This can be some of the explanation for the low T_2 compared to T_1.

Paper	**# 8**	**# 12**	**Blueprint**	**Target Values**
$E_J(GHz)$	3.43	5.57	4	4
$E_C(GHz)$	1	1.08	1	1
$E_L(GHz)$	0.58	0.64	1	0.7
$T_1(\mu s)$	500	1200	-	-
$T_2(\mu s)$	510	1480	-	-
$\omega_q/2\pi$ GHz	0.395	0.163	0.58	0.34
$\alpha/2\pi(GHz)$	-	-	3.39	3.6
E_J/E_L	5.913	8.7	4	6
E_J/E_C	3.43	5.157	4	4
N	144	82	100	-

Table 2: **A table highlighting the E_J, E_C, E_L, T_1, T_2, ω_q, α, E_J/E_L, E_J/E_C, and N (number of Josephson junctions in the array) for 3 different papers and the target values throughout the thesis**. Of the 4 columns, 2 of them are high-coherence Fluxonium papers, namely #8 and #12 in Fig. 10, the third one is the proposed parameters in the paper *Blueprint for a High-Performance Fluxonium Quantum Processor*, and the last column are the values we are going to target in this thesis [Nguyen, Koolstra, et al. 2022]; [Nguyen, Lin, et al. 2019]; [Somoroff, Ficheux, et al. 2021].

Another turning point for the realization of Fluxonium qubits until now, is indicated by the point in Fig. 10 #12 which is a paper from 2021 published by researchers at Maryland University. This qubit showed $T_1 \approx 1200\,\mu s$ and $T_2 \approx 1480\,\mu s$ with single gate fidelities $F = 99.99$ [Somoroff, Ficheux, et al. 2021]. The fidelity is the precision or reliability of a quantum operation of the qubit. Not only did they have high coherence times, but they also showed that they could do gates on the qubit.

It is worth mentioning some of the fluxonium subgroups like the work on Heavy fluxonium qubit exploring the low-frequency limit and operating in the regime where E_J/E_C is large proposed in 2018 [Earnest et al. 2018] [Nguyen, Koolstra, et al. 2022] [Najera-Santos et al. 2023]; [Sun et al. 2023]; [Zhang, Chakram, et al. 2021]; [Zhang, C. Ding, et al. 2023]. These are indicated with a triangle in Fig. 10. Heavy Fluxonium has shown very nice results in 2023 regarding coherence times $T_1 \approx 300\,\mu s$ and $T_2 \approx 200\,\mu s$ [Zhang, C. Ding, et al. 2023]. Another variation of the fluxonium qubit is the Granular aluminum fluxonium qubit, also called Gralmonium, which was first time realized in a paper around 2019 [Grünhaupt et al. 2019] [Rieger et al. 2022]. The papers on Granular aluminum are indicated with a cross in Fig. 10. The idea was to use granular aluminum as a kinetic inductor instead of an array of Josephson junctions as theory suggests it could also work as a superinductor. The coherence times of Fluxonium made of granular aluminum are $T_1 \approx 87\,\mu s$ and $T_2 \approx 51\,\mu s$ [Bao et al. 2022]; [Moskalev et al. 2023].

After the high coherence Fluxonium paper in 2021, [Somoroff, Ficheux, et al. 2021], many of the groups changed the focus from aiming at higher coherence times to doing single qubit gates and focusing on coupling two or more fluxonium qubits. This can also be seen on the right graph in Fig. 10. From 2021 to 2023 none of the papers claim to have obtained higher coherence times, but there is almost a drop in coherence times with $T_1, T_2 \approx 10\,\mu s$ to $1.5\,ms$. We have chosen to highlight 2 of the experimental Fluxonium qubits namely the paper from 2019 Fig.

10 #8 and from 2021 10 #12 where the parameters are seen in table 2. The special about these two fluxonium qubits is that the two coherence times are very similar $T_1 \approx T_2$. This is very interesting as it is the only one of all the 25 papers in the Fig. 10.

In the theoretical paper *Blueprint for a High-Performance Fluxonium Quantum Processor* from 2022 is a paper suggesting different values for the three energies, E_J, E_C, and E_L depending on what setting and what optimization you are aiming for [Nguyen, Koolstra, et al. 2022]. The paper proposes a roadmap for realizing a scalable Fluxonium qubit chip going through important steps to consider during Fabrication, Readout and reset, Design and Layout, and making logic gates. As previously mentioned, we are aiming to optimize according to coherence times T_1 and T_2 for single Fluxonium qubits. Even though the paper thoroughly goes through optimizing the Fluxonium chip design focusing on scaling, there are many of the parameters that they touch upon such as AC-stark shift and static ZZ rate which we will neglect in this thesis.

They propose the following parameters for the paper: $E_J = 4\,\text{GHz}$, $E_C = 1\,\text{GHz}$, and $E_L = 1\,\text{GHz}$ as seen in table 2. This is the energy corresponding to a "regular" Fluxonium qubit. This will give a qubit frequency of $f_q = 0.58\,\text{GHz}$ and an anharmonicity of $\alpha/2\pi = 3.39\,\text{GHz}$. For long coherence times, they suggest having a qubit frequency range between 0.2 to $1.2GHz$ and for the readout resonators, they propose frequencies around $\omega_R/2\pi \approx 7\,\text{GHz}$.

Targeting Fluxonium parameters

Based on the above analysis of the Fluxonium papers, the strategy of this thesis will be to choose parameters that lie in between the values in the three papers in table 2. Two of the papers are state-of-the-art high coherence Fluxonium papers with $T_1 \approx T_2$ coherence times between 0.5-1.5 ms. The third paper is a theoretical paper suggesting parameters for a high-performance Fluxonium quantum processor based on extensive simulations, calculations, and optimizations. The target values are:

$$E_J \approx 4.00\,\text{GHz}, \quad E_C \approx 1.0\,\text{GHz}, \quad E_L \approx 0.7\,\text{GHz}$$

The ratios between these energies are: $E_J/E_L \approx 6$ and $E_J/E_C \approx 4$ as seen in table 2. As our fabrication is not state-of-the-art, we have chosen to target nice values for the energies without too many decimals as any variation in fabrication can lead to large deviations in the final values. The qubit frequency is simulated in the flux basis to be $\omega_q = 0.34\,\text{GHz}$ and the anharmonicity is $\alpha/2\pi = 3.6\,\text{GHz}$. In order to read out our qubits, we will aim for a frequency of our Readout resonators in the regime 5.2 GHz to 7 GHz.

In the next section, we will look at some of the methods and materials that are crucial for fabricating Fluxonium qubits. We will also go over how the structure of the chip layout is organized.

3

NANOFABRICATION METHODS AND MATERIALS

Nanofabrication techniques such as lithography, self-assembly, and molecular beam epitaxy, are crucial for the development of superconducting qubits due to their high precision and control [Ranjan Sahu and Huang 2023]. In this chapter, we will introduce the different nanofabrication methods and techniques used in this thesis. Subsequently, we will then present a layout for a general fluxonium qubit and discuss the methods and materials for the constituent layers of the layout.

3.1 FABRICATION METHODS

In this section, we will introduce some of the most important nanofabrication methods used for fabricating fluxonium qubit components. First, we will introduce common techniques including liftoff and etching, lithography, and deposition. Subsequently, we will talk about how these techniques are used in methods such as *Top-down* and *Bottom-up*, double angle evaporation, and patching. For each of these methods, we will provide an overview of the steps and techniques used. A complete recipe of all the fabrication methods can be found in the SI.

Surface preparation techniques

Before starting the fabrication process, and between each fabrication step, the surface must be free of contaminants or unwanted materials like native oxides. This can be obtained by cleaning the surface in various ways e.g.; with chemicals, oxygen plasma ashing, heating (annealing), or milling with argon to name the ones used in this thesis [Franssila 2010]. Different techniques are used to avoid different types of contaminants. For example, one can remove unwanted oxides by using BOE or argon milling before depositing the metal layer. Water can be removed by heating the sample or one can use oxygen plasma ashing to remove contaminants after removing resist masks. Oxygen plasma and heating can, besides removing residues, also be used as a surface activation technique as the oxygen plasma and heating can increase the surface energy and create broken active bonds which can benefit adhesion (the ability to bond to other materials) [Franssila 2010].

Thin film deposition techniques

Deposition techniques are used to deposit thin films of materials onto a substrate. A thin film layer has a thickness ranging from one nanometer to a few micrometers, and the materials used can be metals, semiconductors, polymers, etc. [Ranjan Sahu and Huang 2023]. Thin film deposition techniques can be divided into three categories; Physical vapor deposition (PVD)

such as molecular beam epitaxy (MBE), magnetron sputtering, and electron beam evaporation. Then there is chemical vapor deposition CVD such as atomic layer deposition ALD, and lastly solution-based chemistry SBC such as spin coating [Ukoba et al. 2018]. Each of these different techniques is commonly used for different materials and applications. In this thesis, we will use electron beam evaporation under high vacuum for depositing metals and spin coating for depositing the resist masks. Electron beam evaporation uses a high energy focussed beam of electrons to heat the material until it reaches a vapor form. The vapor is then directed to the substrate where it condenses and creates a thin film on top of the surface [Eichinger 2023]. Spin coating is a technique where a liquid is spread on a substrate and spun at high speed to spread the liquid evenly over the surface.

Lithography techniques for patterning

Lithography is a technique used to pattern thin films or substrates. There are two main types of lithography techniques: photolithography and electron beam lithography, which use a beam of focussed light and electrons, respectively, to transfer a pattern. Both techniques are used in the fabrication of superconducting qubits. Typically, electron beam lithography allows for patterns and structures of higher precision and finer structures than photolithography [Ranjan Sahu and Huang 2023]. Since the Josephson junction fabrication needs precision down to the nanometer scale, the electron beam lithography for patterning is used in this thesis.

Liftoff and etching techniques

Liftoff and etching are two techniques used to remove materials from a surface and are often used in combination with lithography and deposition techniques. Both techniques are highly used throughout the thesis. Liftoff is a process where the resist is dissolved in a solvent, leaving the patterned material behind also showed in step E (green) in Fig. 11. It is common to do liftoff using an ultra-sonic bath to dissolve the resist or to leave the sample in a solvent for a longer time [Ranjan Sahu and Huang 2023]. Etching is a process where the material is removed by either a physical or chemical reaction shown in step D (red) in Fig. 11. There are two main types of etching: wet etching using an isotropic chemical etchant such as Transene D, and dry etching, which uses high-energy ions to remove surface material, like Reactive ion etching RIE or argon milling which uses argon ions to physically sputter material from the surface [Eichinger 2023].

Top-down and Bottom-up methods

Two common methods for electronic device fabrication are the *Top-down* process and *Bottom-up* process. The *Top-down* process is a subtractive method used to create patterns by breaking down the materials and converting them from bulk to the nanometer scale substances [Ranjan Sahu and Huang 2023]. In contrast, the *Bottom-up* process is an additive method where the pattern is built up from the bottom atom by atom or layer by layer. The steps for these two processes are shown in Fig. 11 A-F. Step A-C is included in both the *Top-down* and *Bottom-up* fabrication flow. D-F (red) is the steps in the *Top-down* process and D-F (green) are the steps for the *Bottom-up* process. The first step in the two processes, A), is to spin coat an organic resist mask onto the substrate. There are many different types of resist masks, but the most common are the positive and negative resists. The thickness of the resist mask is controlled by the type of resist and

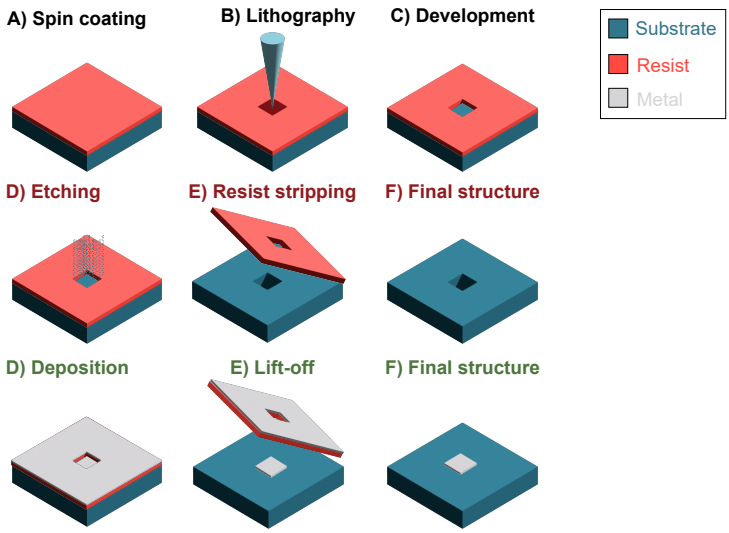


Figure 11: **Schematic of the *Top-down* and *Bottom-up* fabrication flow:** Step A-C are included in both the *Top-down* and *Bottom-up* fabrication flow. Red D-F are the steps in *Top-down* process and green D-F are the steps for the *Bottom-up* process. The first step in the two processes, A), is to spin coat an organic resist mask onto the substrate followed by, B), either electron- or light-beam lithography. C) Then the pattern is chemically developed. For the *Top-down* D) (red), the pattern is then subtracted from the substrate by etching. Lastly, the final structure is obtained after liftoff E). For the *Bottom-up* D) (green), a metal layer is deposited and after liftoff, E), the added pattern is visible F).

the spin speed used. The resist is then baked to harden it. The next step, B), is to use either electron-beam or light-beam lithography which will change the solubility of the resist mask where the beam focuses. This will create a pattern in the resist mask. In step C) the pattern is then developed using a chemical that will either remove the exposed area (positive resist) or the unexposed area (negative resist). For the *Top-down* D) (red), an etchant is used to subtract the pattern area from the substrate. The etching step is highly temperature- and time-sensitive. E) Lastly, the final structure is obtained after liftoff. For the *Bottom-up* D) (green), a metal layer is deposited and after liftoff, E), the added pattern is visible F).

The techniques presented above are the ones we mainly are going to use for the different methods presented in the next section. More information about the fabrication methods and materials can be found in the SI.

Double angle evaporation method with intermediate oxidation step

A variation of the bottom-up process is the double-angle evaporation technique, which is commonly used to fabricate Josephson junctions. As discussed earlier, the Josephson junctions consist of two superconductors (which we will call junction electrodes) separated by an insulating barrier. We start by spinning a double-layer of two different resists as seen in Fig. 12 A). The bottom resist will work as an undercut aiding the liftoff and preventing sidewalls. Then we carve out the pattern by lithography followed by development. B) The first of two depositions with tilt angle, θ_1, and thickness, t_1, is performed. C) The next and crucial step is oxidation, which will create the insulating barrier between the two Josephson junction electrodes. The sample

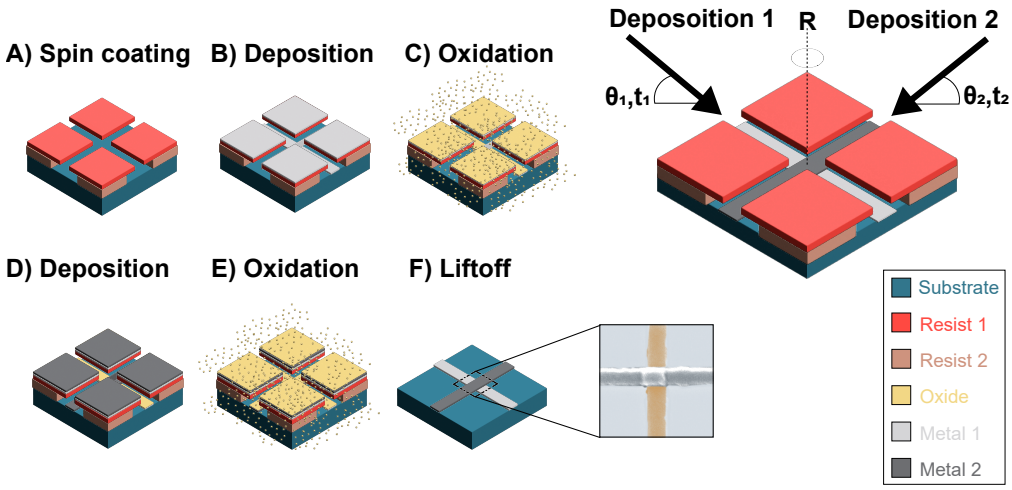


Figure 12: **Schematic of the Manhattan style junction fabrication flow:** A) The first step is to spin coat a double-layer resist mask onto the substrate. Then we carve out the pattern by lithography followed by development. B) Then the first out of two depositions with tilt angle, θ_1, and thickness, t_1, shown in red is performed. C) Oxidation is performed to create the insulating barrier. The sample is then rotated with rotation, R. D) The second deposition with tilt angle, θ_2, and thickness, t_2, shown in grey is performed. E) Another oxidation that now works as a capping layer. F) The final structure is obtained after liftoff.

is then rotated with rotation, R, which will typically be 90 degrees so that the two arms are perpendicular. D) The second deposition with tilt angle, θ_2, and thickness, t_2, are then performed. E) Lastly, another oxidation that now works as a capping layer (to make the oxide distributed on top of the metal, as controlled and homogenous as possible). F) The final structure is obtained after liftoff, where a corresponding false-colored SEM image is provided. The bottom junction electrode is highlighted in red, and the top junction electrode in grey.

Patching method

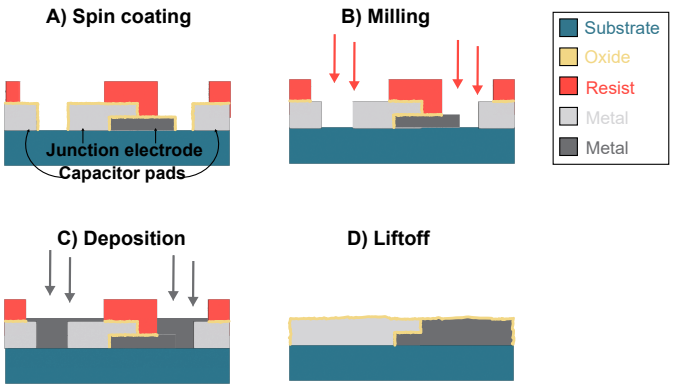


Figure 13: **Patching fabrication flow:** A) Spin coating followed by electron beam lithography and development to obtain the wanted pattern. B) Milling is used to remove the oxides on top of the metal. C) Deposition of new metals to create a good galvanic connection between the junction electrodes and the capacitor pads. D) The final structure is shown after liftoff.

Patching is a technique used to ensure a good galvanic connection between two interfaces. It can be necessary to use after, for example, the double angle evaporation method described above. In Josephson junction fabrication, it is used to make sure, that the junction electrodes are well connected to the capacitor pads [Murray 2021]. The steps in the patching fabrication flow can be found in Fig. 13 A-D. The figure shows a cross-section of a substrate containing two junction electrodes and two capacitor pads. Due to ambient conditions after the junction fabrication, oxides may have formed on top of the electrodes and the capacitor pads. If one wants to secure a good connection between the capacitor pads and the Josephson junction, the following patching method can be used. A) Spin coating followed by electron beam lithography and development to obtain a resist mask that only exposes the area where the patch is going to be located, while protecting the rest of the surface. B) Then milling is used to remove the oxides on top of the metal. In this thesis we will use argon milling. C) Now one can make a good connection between the Josephson junction and the shunt capacitor by depositing new metals. This is sometimes referred to as a bandage. In D), the final structure is shown after liftoff.

3.2 THE LAYOUT OF A GENERAL FLUXONIUM QUBIT

In this section, we will introduce a general layout of a single fluxonium qubit circuit and discuss the material qualities and methods used to fabricate each of the constituent layers. There are many ways to quantify a material such as film thickness, resistivity, interface quality, etc. [Franssila 2010]. The aim of this thesis is to target specific energy parameters determined by studying the combinations of energies that result in the longest coherence times, T_1 and T_2, found from a selection of different articles. However, the coherence times of the qubit are highly dependent on the materials used and how the different steps in the fabrication process are done. For example, the coherence time of the qubit can be affected by the presence of oxides on the surface of the substrate, causing traps between the metal layer and the substrate. This can cause two-level-system (TLS) losses, which are a source of decoherence and will therefore lower the coherence time of the qubit [Murray 2021]. One usually quantifies the coherence time of the qubit in terms of the quality factor, Q. The quality factor is used as a measure of how well each of the qubit components is at storing the transmitted energy (photons), indicating how lossy they are in terms of photons. The relationship between the coherence time, T_1, and the total qubit quality factor is given by:

$$\frac{1}{T_1} = \frac{\omega_q}{Q_q} \tag{33}$$

where ω_q is the qubit frequency and Q_q is the qubit quality factor. The qubit quality factor is a sum of different contributions:

$$\frac{1}{Q_q} = \frac{1}{Q_{TLS}} + \frac{1}{Q_{pur}} + \frac{1}{Q_{qp}} + \frac{1}{Q_{rad}} + ... \tag{34}$$

Where Q_{TLS} is the TLS loss, Q_{pur} is the Purcell decay, Q_{qp} is the quasiparticle loss, and Q_{rad} is other radiation losses not related to Purcell losses [Biznárová et al. 2023]. Quantifying the various contributions to the loss mechanisms is extremely difficult, and we will not pursue to give it a try in this thesis. Instead, this is a brief summary of some of the loss mechanisms that may be encountered which is mentioned here to help explain some of the material choices discussed in the next section.

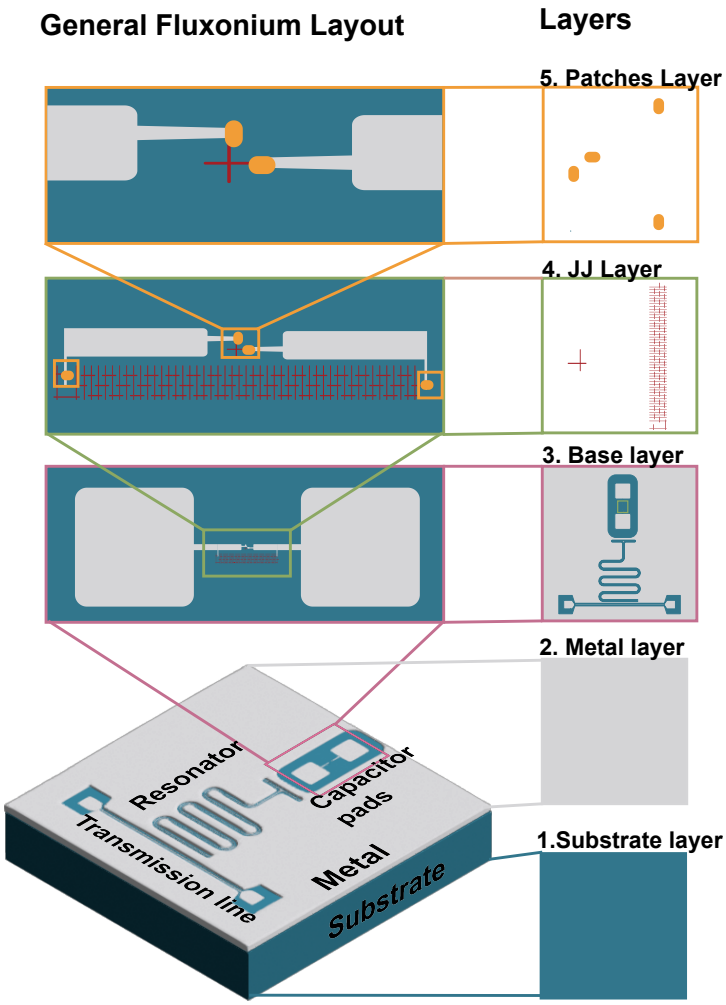


Figure 14: **Layout of a general fluxonium qubit circuit:** The general layout of a single fluxonium qubit circuit consists of a transmission line, resonator which is capacitively coupled to two shunting capacitors. In between the capacitor pads, we have both an array of Josephson junctions and a single Josephson junction. The layout can be divided into 5 layers: 1. The substrate, 2. The metal layer, 3. The base layer, 4. the Josephson junction layer, 5. The patches layer. Each layer contains a different fabrication process.

Fig. 14 shows the layout of a general fluxonium qubit circuit. It consists of a microwave resonator and transmission lines which aid qubit readout. The resonators are capacitively coupled to two shunting capacitors. In between the capacitor pads, we have both an array of Josephson junctions and a single Josephson junction. From a material point of view, the layout can be divided into five layers: 1. The substrate layer, 2. The metal layer, 3. The base layer, 4. the Josephson junction layer, 5. The patches layer. Each layer contains a different fabrication process with carefully revised step-by-step fabrication methods. In the following, we will discuss the materials and methods used to fabricate the different layers of the fluxonium qubit.

3.2.1 *1. Layer - The substrate*

The substrate is the bottom layer of the chip and is what keeps everything in place, as seen in Fig. 14. Two common substrates currently used for fabricating superconducting qubits are high

resistivity silicon (Si) and sapphire (Al_2O_3) [Eichinger 2023]. The dielectric loss tangent, tan (δ), is a measure of the energy lost, when an electromagnetic field interacts with a material. For these two materials the values are around $\delta_{sapphire} = 10^{-9}$ for sapphire and $\delta_{Si} = 10^{-6}$ for purified high resistivity Si. Even though sapphire has a much lower loss tangent, Si is the key material used in the industry to build microchips, and therefore its material properties are much more extensively investigated. In this thesis, we will use Si as the substrate for all our fabrication. The preparation of the substrate is crucial as Si develop a native oxide when exposed to ambient conditions. If left untreated, this oxide layer will sit at the interface between the substrate and the metal causing TLS. The loss tangents of native oxide layers and contamination at interfaces and surfaces are in the order of 10^{-2} to 10^{-3} [Quintana et al. 2014]. To minimize the oxide formed at the substrate metal interface, the substrate is surface treated by dipping into HF 5% for 1 min to clean the surface and remove the Si Oxide on top. This process is called buffered oxide etch BOE. The substrate is then ready for the next layer which involves the deposition of metal.

3.2.2 *2. Layer - The metal layer*

The metal layer consists of a thin film of superconducting material such as Al, Ta, Nb, NbN, NbTiN, TiN [Eichinger 2023]. The two most common superconductors used for the fluxonium qubits studied in the previous chapter 2 are Al or Nb-based superconductors. In general, Aluminum is the most common superconductor for superconducting qubit fabrication typically because it is also the material used for the Josephson junction fabrication. In this thesis, we will use Al as the only superconducting metal.

In the paper *Mitigation of interfacial dielectric loss in aluminum-on-silicon superconducting qubits*, [Biznárová et al. 2023], from 2023, the authors investigated how coherence times and quality factors for aluminum on si transmon qubits change with the thickness of the aluminum thin film layer. They investigated thickness from 150 nm to 500 nm where they showed that the internal quality factors improve with an increase in thickness where 500 nm was the best. However, the improvement was already seen in thickness above 300 nm. Via a loss analysis of CPW resonators, they found a reduction of TLS loss due to reduced oxides at the substrate metal interface for increased Al thickness. They explained this finding with the tendencies of Al grain size growth. A thicker layer of Al leads to larger grains with fewer boundaries and therefore containing less oxides at the metal substrate interface. Even though the 500 nm Al showed the best Q factors, we have settled on fabricating 300 nm Al in this thesis due to the difficulties in wet etching 500 nm Al.

3.2.3 *3. Layer - The base layer*

After depositing the metal layer of 300 nm Al, we will use the top-down method to wet-etch the transmission line, resonators, and capacitor pads, as seen in Fig. 14. Wet etching is very temperature- and time-sensitive. Wet etching is highly temperature- and time-sensitive. If the etching time is too short, metal residues may remain, which can short-circuit the system or create two-level system (TLS) losses. However, if the etching time is too long, the more delicate structures in the design might be damaged or vanish. The transmission line and the resonators on our chip are used for reading out the qubit state. Each end of the transmission line is connected

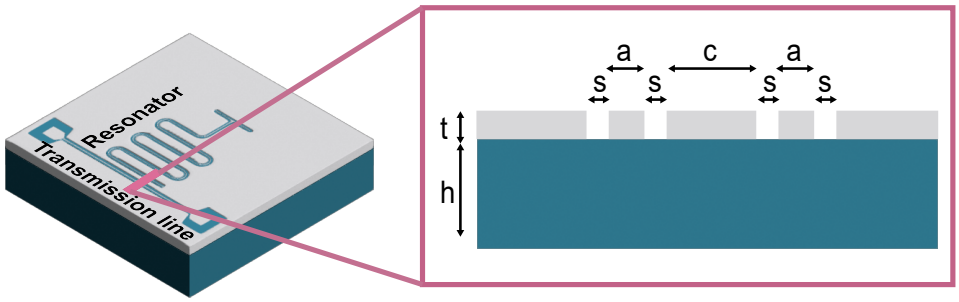


Figure 15: **Coplanar waveguide:** This is a model of a Transmission line capacitively coupled to a CPW resonator. The left side is a picture of the top view of the whole chip. The right is a picture of the cross-section taken at the pink line. The grey region represents a superconducting film and the blue represents the substrate. The superconducting film is etched to create the resonators and the transmission line. They both have width (a) and distance (s) to the rest of the superconducting film for impedance matching. The distance (c) between the transmission line and the resonator determines the capacitive coupling between the two.

to bonding pads that connect to the cables leading out of the fridge. The typical impedance of fridge cabling is 50 ohms. To minimize unwanted reflections and power loss, it is essential to match the impedance of the resonators and the transmission line as closely as possible to 50 ohms [Pozar 2012]. The impedance of the resonator and the transmission line depends heavily on their geometry and design. Fig. 15 shows the geometry of a resonator capacitively coupled to the transmission line. The left side provides a top view of the entire resonator and transmission line, while the right box shows a cross-sectional view highlighting the device geometries. The grey regions represents a superconducting film with thickness, t, and the blue substrate with thickness, h. Both resonator and transmission line have the same width, a, and distance, s, to the rest of the superconducting film which results in the same impedance. The distance, c, between the transmission line and the resonator determines the capacitive coupling between them. We can model the resonator as an LC lumped element which gives the following expression for the impedance and frequency [Pozar 2012].

$$\begin{aligned} Z &= \sqrt{\frac{L}{C}} \\ \omega &= \frac{1}{\sqrt{LC}} \end{aligned} \tag{35}$$

Where Z is the impedance, L is the total inductance and C is the total capacitance of the resonator. The inductance and capacitance of the resonator can be expressed as:

$$\begin{aligned} L &= \frac{2}{\pi^2 n^2} L_\ell \ell \\ C &= \frac{1}{2} C_\ell \ell \end{aligned} \tag{36}$$

The ℓ is the length of the resonator and C_ℓ is the capacitance pr. length can be written as:

$$C_\ell = 4\varepsilon_0 \varepsilon_{eff} \frac{K(k)}{K(k')} \tag{37}$$

ε_0 is the vacuum permittivity, and ε_{eff} is the dielectric constant of the substrate and. Both $K(k)$ and $K(k')$ are elliptical integrals of the first kind with arguments:

$$\begin{aligned} k &= \frac{a}{a+2s} \\ k' &= \sqrt{1-k^2} \end{aligned} \tag{38}$$

Where a is the width of the center conductor and s is the gap width as seen in Fig. 15. The inductance, L_l, depends highly on the geometry and material properties and is given by the two terms [Schuster 2007]:

$$\begin{aligned} L_\ell &= L_m + L_k \\ L_m &= \frac{\mu_0}{4}\frac{K(k')}{K(k)} \\ L_k &= \mu_0 \frac{\lambda_L^2}{Wt} g(s,a,t) \end{aligned} \tag{39}$$

L_m is the magnetic inductance and L_k is the kinetic inductance [Schuster 2007]. μ_0 is the vacuum permeability and $g(s,a,t)$ is a geometrical function dependent on the gap, s, and width, a, of the resonator as well as the thickness, t, of the Al layer. There are many tools available that can help you calculate the impedance of your CPW. In this thesis, we have used *appCAD* to find the right parameters of our resonators and transmission line. For $t = 300\,\text{nm}$ Al on top of $h = 525\,\mu\text{m}$ Si, the dimensions of our CPW have the dimensions $s = 6\,\mu\text{m}$ and $a = 10.7\,\mu\text{m}$. This results in an impedance of $Z = 48.8\,\Omega$. Achieving the exact target impedance of $50\,\Omega$ can be a bit tricky and in the end, it dependent on the precision of the fabrication process. Therefore, an impedance of $Z = 48.8\,\Omega$ wil be used for the remainder of this thesis.

3.2.4 *4. Layer - The Josephson junction layer*

Fluxonium contains a single Josephson junction and an array of Josephson junctions. In this thesis, we fabricate *Manhattan-style Josephson junctions*, which often have the shape of a cross. The steps in the Manhattan-style junction fabrication are the same as the double-angle evaporation method with an intermediate oxidation step, as seen in Fig. 12. There are many different parameters one can change in the fabrication of Josephson junctions. The most important parameters are the resist mask, the deposition angle, the oxidation rate, and the oxidation time. Some of these parameters will be discussed in more depth in Chapter 5.

3.2.5 *5. Layer - The patches layer*

The last layer is the patches layer, implemented to ensure a good connection between all the different components, specifically the junction electrodes and the capacitor pads. In this thesis, we will use the patching method shown in Fig. 13 after our junction fabrication. In the milling method, we spin coat a layer of resist (sometimes it can be favorable to spin a double layer). Then, we use e-beam lithography to access only a small area of both the capacitors and the electrodes. This area is then milled, followed by a thin film deposition of a conducting metal. Since we use aluminum for both the Josephson junction fabrication and the capacitor pads, it is natural to also use aluminum when depositing the patches. The reason why we do not simply mill before the junction deposition and thereby skip the patches layer is due to a study from

2017 [Dunsworth et al. 2017], which shows an increase in the dielectric loss tangent, $tan(\delta_0)$, by orders of magnitude when Argon milling was performed before junction fabrication. This indicates that using ion milling on the substrate would damage it, causing two-level systems (TLS) and decreasing coherence times.

Summary

This chapter discusses the nanofabrication methods and materials used for developing superconducting qubits. It introduces key techniques such as lithography, deposition, and etching, and details about the fabrication processes for each layer of a fluxonium qubit circuit. The chapter also explains the importance of material properties and precise fabrication steps in achieving long qubit coherence times, highlighting various loss mechanisms and their impact on performance.

Up until now, we have introduced the theory behind superconducting circuits and dwelled upon the fluxonium qubit circuit. We have talked about what experimental advantages there have been throughout the years and what parameters could be optimal for making a fluxonium qubit in terms of coherence times T_1 and T_2. We have also introduced the Fabrication methods, the layers, and the materials you need to build a fluxonium qubit. Now we will put this knowledge together and dive into the different components that control the energies of the fluxonium qubit, namely the capacitor pads, the Josephson junctions and the array of the junctions. We will go through each of these components and come up with a strategy on how to get the proposed target values which are:

$$E_J \approx 4.00\,\text{GHz}, \quad E_C \approx 1.0\,\text{GHz}, \quad E_L \approx 0.7\,\text{GHz}.$$

Each of the three sections is built up in the same way. We will start by discussing the strategy for obtaining the right energy for the component, then we will discuss the design of the component, then we will discuss the simulations of the component, then we will discuss the fabrication of the component, then we will discuss the characterization of the component and finally we will discuss the measurement of the component. When we have all the components for building up the fluxonium qubit, we just need to put them together and find a way to control and read out the qubit. For this, we will also add a section, where we talk about the readout line, resonators, drive lines, and flux lines. This is crucial for building a single fluxonium qubit which can work as a building block for a quantum computer.

4

TARGET EC - CAPACITOR PADS

The goal of this chapter is to target the capacitance energy of $E_C = 1\,\text{GHz}$. The capacitance energy of a single fluxonium qubit can be written in terms of the capacitance using the following relation:

$$E_C = \frac{e^2}{2C_\Sigma} \tag{40}$$

where e is the elementary charge and C_Σ is the total capacitance. By inserting the target value for the energy and isolating the capacitance, we get:

$$C_\Sigma = \frac{e^2}{2h \cdot 1\,\text{GHz}} = 19.37\,\text{fF} \tag{41}$$

This is the target capacitance we aim to achieve. This will be done by examining the different components commonly found on a fluxonium chip and investigate their respective contributions to the overall capacitance. Lastly, the total capacitance will be calculated by simulating the capacitance matrix using Ansys Maxwell 3D for different geometries of our fluxonium qubit design until the desired capacitance energy value is obtained.

4.1 CAPACITANCE CALCULATION

The total capacitance, C_Σ, has contributions from all the different components in our circuit, including the capacitor pads, the ground plane, the Josephson junction, and the array. Looking at a typical system for controlling a fluxonium qubit, you will additionally have a readout line (resonator), a drive line, and a flux line all capacitively coupled to your qubit. The circuit diagram for the full system can be seen in Fig. 16. Note that it is only the capacitances that directly affect the total capacitance of the qubit that have been shown. The capacitances between e.g., the flux line and the drive line are not shown in the diagram neither are the voltage sources to the flux- and the drive line even though they are present. The total capacitance of the isolated qubit, $C_{\Sigma qubit}$, is in parallel with C_{top} and C_{bot}, where C_{bot} and C_{top} are in series. The total capacitance, C_Σ, is given by:

$$C_\Sigma = C_{\Sigma qubit} + \frac{C_{\Sigma bot} \cdot C_{\Sigma top}}{C_{\Sigma bot} + C_{\Sigma top}} \tag{42}$$

The terms in the total capacitance can be broken down into their contributions shown in the schematics in Fig. 16. To make the circuit diagram more comprehensible, we will discuss each term in the total capacitance individually, starting with the capacitance of the fluxonium qubit itself.

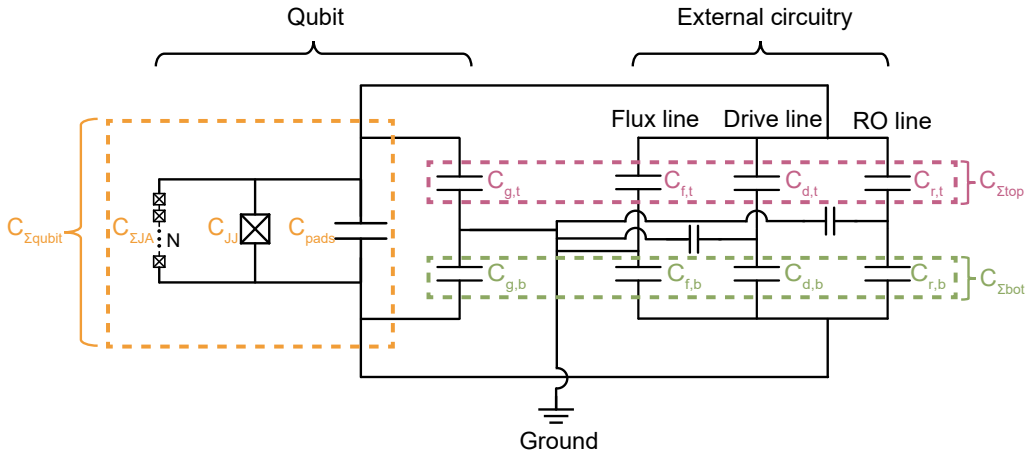


Figure 16: **Circuit diagram of a system containing a single fluxonium qubit and external circuitry (Flux line, drive line, and readout line (resonator)):** The fluxonium qubit has capacitance contributions from the array, $C_{\Sigma JA}$, the single Josephson junction, C_{JJ}, and the capacitor pads, C_{pads}. The sum of these three contributions constitutes the total capacitance, $C_{\Sigma qubit}$. The external circuitry consists of a flux line, a drive line, and a readout line (resonator). These three elements are capacitively coupled to both the top and the bottom pad of the qubit. The sum of all the top(bottom) contributions can be collected into a total contribution, $C_{\Sigma top(bot)}$.

Contributions from the qubit

The qubit has the following contributions:

$$C_{\Sigma qubit} = C_{pads} + C_{JJ} + C_{\Sigma JA} \tag{43}$$

where C_{pads} is the capacitance between the two pads, C_{JJ} is the capacitance of the single Josephson junction and $C_{\Sigma JA}$ is the total capacitance of the array.The capacitance contribution from the Josephson junction can be approximated by the capacitance between two parallel plate capacitors with a distance, d, and a dielectric in between which is different from vacuum [Young et al. 2008]:

$$C_{JJ} = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A}{d} \tag{44}$$

where ε_r is the relative permittivity of the insulating barrier, which in this case is $AlOx$, ε_0 is the vacuum permittivity, A is the overlapping area of the two junction electrodes, and d is the distance between the junctions (corresponding to the thickness of the $AlOx$ layer). The relative permittivity of $AlOx$ is taken to be $\varepsilon_{AlOx} = 9.34$ [ucl 2024]. From eq. 44, one notes that the capacitance is inversely proportional to the thickness of $AlOx$. We assume the thickness to be approximately 5 nm [Osman et al. 2023]. For the single Josephson junction in the context of a Fluxonium qubit, the target areas typically range between 0.01 μm^2 and 0.04 μm^2 corresponding to junction electrode widths of $100 - 200nm$. This will be discussed further in the next chapter. These area and barrier thickness values correspond to a capacitance of $C_{JJ} \approx 0.1654\,\text{fF} - 0.662\,\text{fF}$. Given the total capacitance, $C_\Sigma = 19.37\,\text{fF}$, this is a contribution of approximately $C_{JJ} \approx 0.85\% - 3.42\%$. For simplicity we will assume a contribution from the single josephson junction of $C_JJ = 0.5\,\text{fF}$ in the capacitance calculations.

In the array, the Josephson junctions are placed in series, giving the total capacitance: $C_{\Sigma JA} =$

Contribution	**Capacitance** (fF)
$C_{r,t}$	0
$C_{r,b}$	4
$C_{d,t}$	4
$C_{d,b}$	0
$C_{f,t}$	4
$C_{f,b}$	4

Table 3: **A table highlighting the chosen values for the capacitances between the qubit and the external circuitry:** $C_{r,t}$**,** $C_{r,b}$**,** $C_{d,t}$**,** $C_{d,b}$**,** $C_{f,t}$**, and** $C_{f,b}$. The values of the capacitances are chosen according to the distance from the external circuitry element to the top or bottom capacitor pad. The elements close to the top(bottom) pad are given the value 4 fF and the elements far away from the top(bottom) pad are chosen to be omitted resulting in $C_{r,b} = C_{d,t} = C_{f,t} = C_{f,b} = 4\,\text{fF}$ and $C_{r,t} = C_{d,b} = 0$

C_{JA}/N where C_{JA} is the capacitance of each Josephson junction and N is the number of junctions in the array. Here, we assume that each of the N Josephson junctions is identical. The array typically contains junctions with larger overlapping areas than that of the single junction. For now, let us assume that the area of each junction in the array is $0.25\,\mu\text{m}^2$ corresponding to $500nm$ electrode width. Then, the capacitance of the array will be: $C_{\Sigma JA} \approx 4.135\,\text{fF}/100 = 0.04135\,\text{fF}$. This corresponds to a contribution of $C_{\Sigma JA} \approx 0.21\%$ to the total capacitance, and we will therefore omit this from the total capacitance in further calculations.

Contributions from external circuitry

The $C_{\Sigma top}(C_{\Sigma bot})$ has contributions only from the top(bottom) pad to the rest of the circuitry (readout line, flux line, drive line, and the ground). The contributions are shown in Fig. 16 and the total capacitances can be written as:

$$\begin{aligned} C_{\Sigma top} &= C_{g,t} + C_{r,t} + C_{d,t} + C_{f,t} \\ C_{\Sigma bot} &= C_{g,b} + C_{r,b} + C_{d,b} + C_{f,b} \end{aligned} \tag{45}$$

where $C_{g,t}(C_{r,t})(C_{d,t})(C_{f,t})$ is the capacitance between the top pad and the ground(readout line)(drive line)(flux line). The same applies for the bottom pad. The flux line, drive line, and resonator are all components whose contributions can be modified by changing their distance to the qubit. If we increase the distance to, for example, the resonator, the capacitance contribution will increase, and this also applies to the flux and the drive line. Therefore, we assume that the capacitance contributions from these elements are constant. The chosen values from these contributions can be seen in table 3. The flux line is commonly placed close to the array which is located between the capacitor pads. Therefore the capacitance between the flux line and the top(bottom) pad, $C_{f,t}$ ($C_{f,b}$), should have the same value, which we have taken to be 4 fF. The drive line is placed on one end, for example, close to the top pad, and the readout line is placed on the other end, close to the bottom pad, making the capacitance contributions from elements far away from a pad, $C_{d,b}$ and $C_{r,t}$, to be zero and the contributions close to a pad, $C_{d,t}$ and $C_{r,b}$, to be 4 fF. The contribution from the Josephson junction is assumed to be 0.5 fF corresponding to an overlapping area of $0.04\,\mu\text{m}^2$ as shown in the previous section.

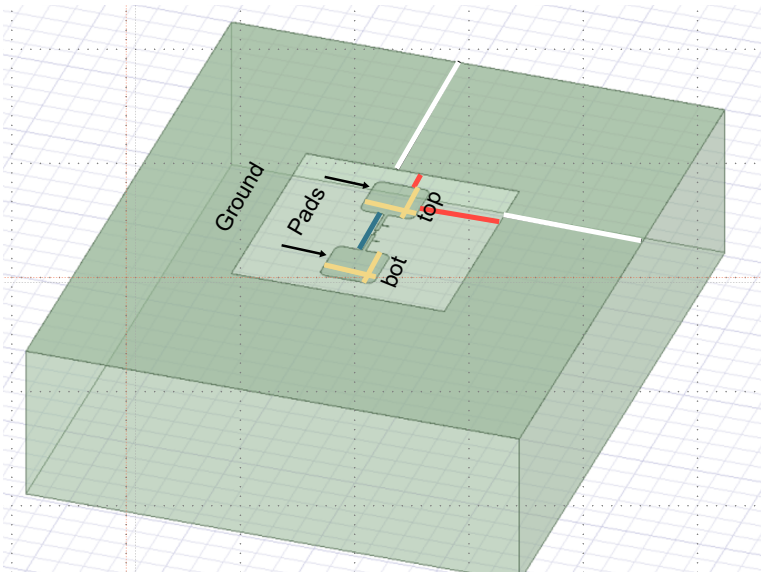


Figure 17: **Ansys Maxwell 3D capacitance simulations of the two capacitor pads and the ground:** The image shows a picture of the Ansys Maxwell 3D simulation of the two capacitor pads of the fluxonium qubit and the ground. The white line indicates the size of the ground plane, the red lines indicate the distance between the pads and the ground plane, the yellow lines indicate the size of the capacitor pads and the blue line indicates the length of the capacitor arms.

Keeping these capacitances constant, we wish to simulate how different variations in the qubit design influence the capacitance. The strategy is to get an idea of how the three capacitances, C_{pads}, $C_{g,t}$, and $C_{g,b}$, change as a function of our qubit dimensions and how this affects E_C. By quantifying these values, the total capacitance, given by eq. 42, can then be computed, allowing us to calculate E_C for each capacitance value.

4.2 SIMULATIONS

To estimate the theoretical value of the total capacitance C_Σ, we use Ansys Maxwell 3D simulation software which is a powerful tool using finite element analysis (FEA) to compute electromagnetic fields for many different types of objects and applications. In this paper, it is used to estimate the capacitance matrix consisting of three entries, namely the the two capacitor pads and the ground plane. Ansys allows you to import a design file in the vector file format, (.DXF). The design file is coded in Python using the module Gdspy. The chosen design for the capacitor pads of our fluxonium is imported into Ansys as a 2D sheet design. The design is then extruded into a 3D design where appropriate materials are assigned to the 3D objects. To imitate our Al layer at temperatures below T_C, we assign a perfect conductor for the substrate, a $525um$ Si box is added underneath, and lastly, a vacuum is added as a big box covering all the surfaces. The imported design can be seen in Fig. 17. The figure highlights the different parameters which can be modified in our design. The white lines indicate the size of the ground plane, the red lines indicate the distance between the pads and the ground plane, the yellow lines indicate the width/length of the square capacitor pads, and the blue line indicates the distance between the two capacitor pads. When executing the simulation it gives out a capacitance matrix, where one can extract the different capacitances.

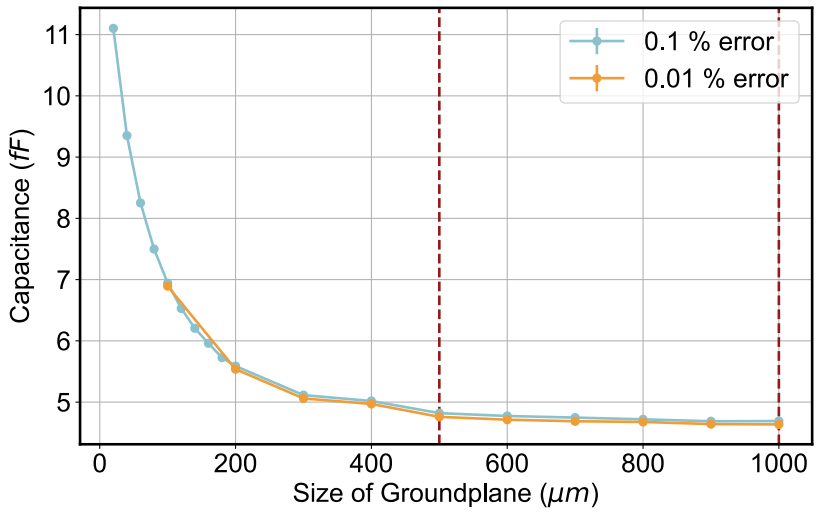


Figure 18: **Ansys Maxwell 3D capacitance simulation changing the ground plane size** The ground plane size is ranging from $20 - 1000\,\mu m$. The graph stabilizes for ground plane sizes above $500\,\mu m$.

Groundplane size

The size of the ground plane is not supposed to affect the capacitance, however, when chosen too small, it will have a great impact on the capacitance value, leading to an inaccurate estimate of the total capacitance. To ensure the correct size of the ground plane is chosen, a range of $20 - 1000\,\mu m$ ground plane sizes was simulated to determine when the capacitance stabilizes, seen in Fig. 18. The figure shows the capacitance as a function of the size of the ground plane for two different convergence criteria. The convergence criteria is a measure of how accurate the simulations will be to the true value. Smaller convergence errors ensure higher precision but at the cost of simulation time. In this simulation a convergence of 0.1% error (the blue line) and 0.01% error (the orange line) is chosen.

The capacitance is found to be stable for ground plane sizes above $500\,\mu m$ as indicated by the red dashed line but for the sake of precaution all the simulations in the following have a ground plane size of $600\,\mu m$.

Dimensions of capacitor pads and their distance to the ground plane

We begin by varying the dimensions of our square capacitor pads, ranging from $100\,\mu m$ to $600\,\mu m$, for three different distances to the ground plane, specifically $100\,\mu m$, $200\,\mu m$, and $300\,\mu m$. The capacitance from the simulations along with the total capacitance energy is shown in Fig. 19. Figure (a) shows E_C as a function of the width/length of the square capacitor pads for three different distances to the ground plane, namely $100\,\mu m$, $200\,\mu m$, and $300\,\mu m$. Figure (b) shows the contributions from the different capacitances C_{pads}, $C_{g,b}$, and $C_{g,t}$ as a function of the width/length of the capacitor pads. All the Ansys simulations have a convergence error of 0.1%. From (a), one observes that the dimensions of the capacitor pads have a larger impact on E_C than the distance to the ground plane. In figure (b), one can see that $C_{g,t}$ (capacitance between the ground and the top pad) and $C_{g,b}$ (capacitance between the ground and the bottom pad) follow the same trend, and that these contributions are much larger than C_{pads} (capacitance between the

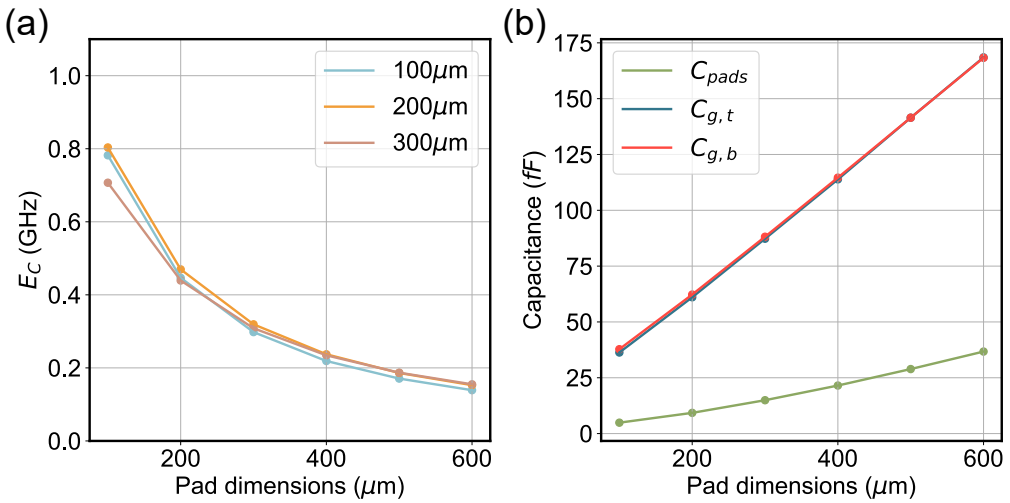


Figure 19: **Ansys Maxwell 3D capacitance simulation varying the length/width of the qubit capacitor pads and the distance between the pads and the ground plane.** The ansys simulations all have a convergence error of 0.1%. (a) The figure shows E_C as a function of the width/length of the square capacitor pads ranging from 100 µm to 600 µm for three different distances to the ground plane, namely 100 µm, 200 µm, and 300 µm. (b) The figure shows the contributions from the different capacitances C_{pads}, $C_{g,b}$, and $C_{g,t}$ as a function of the width/length of the capacitor pads.

top pad and the bottom pad). To explain this, one can think of the capacitor pads and the ground to be coplanar strips with length L, width w, and a distance d between them. The capacitance between the two strips can be approximated by the formula [Zypman 2019]:

$$C \propto \frac{L}{log(d/w)} \tag{46}$$

This proportionality indicates that the capacitance scales linearly with the length the two strips have in common, L, whereas it only scales logarithmically to the distance between the two strips, d. This is why the impact of increasing the length of the capacitor arms is much less than increasing the width/length of the capacitor pads. As the capacitor pad increases in length, you will increase the common length, L, that the pads and the ground plane share, thereby increasing the capacitance contribution.

The maximum value for E_C obtained in the plot in Fig. 19 (a) is around 0.81 GHz. To obtain a larger E_C, one needs to aim for a smaller capacitance, which can be achieved by decreasing the size of the capacitor pads or increasing the distance between them.

Distance between the two capacitor pads

We will now keep the size of the pads at 80 µm and vary the distance between the two capacitor pads from 200 µm to 600 µm. Since the array and the Josephson junction are located between the pads, we cannot simply separate the two capacitor pads from each other. The strategy is instead to elongate the arms connected to the pads. The results from the simulations are shown in Fig. 20. (a) shows E_C as a function of the length of the capacitor arms, and (b) shows the contributions from the different capacitances C_{pads}, $C_{g,b}$, and $C_{g,t}$ as a function of the length of

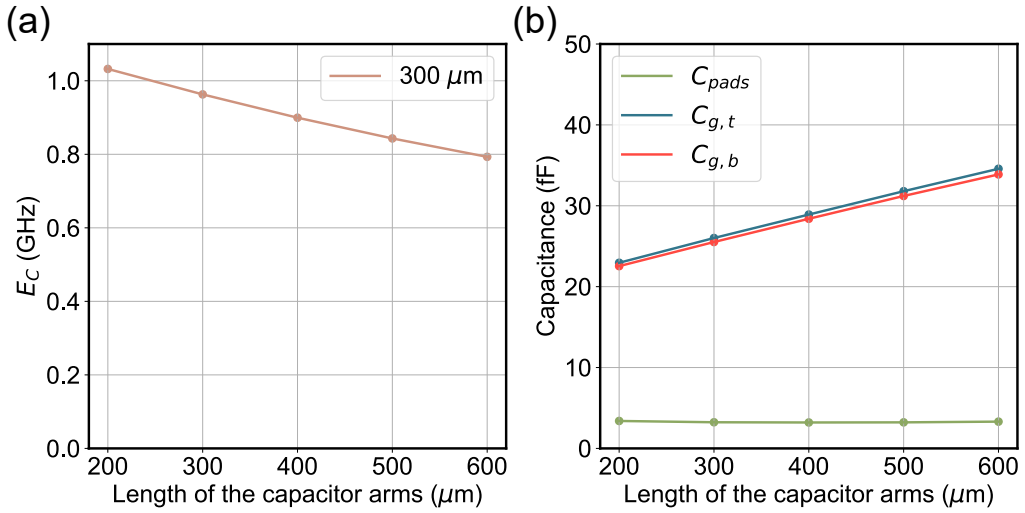


Figure 20: **Ansys Maxwell 3D capacitance simulation varying the length of the capacitor arms:** To achieve the desired capacitance range, we varied the length of the capacitor pads from $200 - 600\,\mu m$. The simulations are performed with a convergence error of 0.1%. (a) Shows the total capacitance energy as a function of the length of the capacitor arms. (b) Is the capacitance as a function of the length of the capacitor arms for the three contributions, C_{pads}, $C_{g,t}$, and $C_{g,b}$.

the capacitor arms. Again, the contributions from the pads to the ground dominate compared to the capacitance between the two pads. $C_{g,t}$ and $C_{g,b}$ increase with the length of the capacitor arms which is in agreement with eq. 46. When we elongate the arms, the common length L increases causing the capacitance to increase which decreases E_C. A desired capacitance energy, $E_C = 1.03\,\text{GHz}$, is obtained for a length of the arms of $200\,\mu m$. This corresponds to a total capacitance of $C_\Sigma = 18.7\,\text{fF}$ with contributions from $C_{pads} = 3.39\,\text{fF}$, $C_{g,t} = 22.9\,\text{fF}$, and $C_{g,b} = 22.5\text{fF}$.

Summary

Through Ansys simulations, we have not obtained a total capacitance of $C_\Sigma = 18.7\,\text{fF}$, corresponding to the energy $E_C = 1.03\,\text{GHz}$, aligning with the target value within the uncertainty of the fabrication. This capacitance energy is obtained for a length of the capacitor arms of $200\,\mu m$, a pad size of $80\,\mu m$, and a distance to the ground plane of $300\,\mu m$. However, the contributions from the drive line, the flux line and the resonator have just been assumed constant. Note that there is not only one specific combination of C_{pads}, $C_{g,t}$, and $C_{g,b}$ which gives the right C_Σ. One can play around with the different values, and change the design accordingly. Furthermore, the shapes of the capacitor pads could be changed, for example, to a circular or oval shape

5

TARGET EJ - A SINGLE JOSEPHSON JUNCTION

As discussed in the background chapter 2, the Josephson energy we aim to target is $E_J/h = 4\,\mathrm{GHz}$. To remind ourselves, the Josephson energy can be written in terms of the critical current using the following relation:

$$E_J = \frac{\Phi_0 I_c}{2\pi} \tag{47}$$

The critical current is the amount of dissipationless current that can flow through the Josephson junction below the superconducting temperature, T_C. However, Josephson junctions behave like a normal resistor when probed at room temperature. Fortunately, we can relate the critical current with the resistance at room temperature, R_N, called the normal resistance using Ambegaokar-Baratoff relation [Ambegaokar and Baratoff 1963][Bruus and Flensberg 2004]:

$$I_C = \frac{\pi\Delta(0)}{2eR_N} \tag{48}$$

Where $\Delta(0)$ is the superconducting gap of the Josephson material evaluated at $T = 0K$. Combining the two equations we get the Josephson energy in terms of the normal resistance at room temperature:

$$\frac{E_J}{h} = \frac{\Phi_0\Delta(0)}{4ehR_N} \tag{49}$$

The superconducting gap is dependent on the material used for the junction. Josephson junctions made of thin film Al typically have a superconducting gap of $\Delta(0) = 150 - 200\,\mu\mathrm{eV}$ [Gao et al. 2021]. We will assume $\Delta(0) = 200\,\mu\mathrm{eV}$ for the calculations giving a Josephson energy of:

$$\frac{E_J}{h} \approx \frac{1}{R_N} \cdot 155\,\mathrm{GHzk}\Omega \tag{50}$$

For the Josephson energy of 4 GHz, according to the equation above, we need a normal resistance of $R_N \approx 38.75\mathrm{k}\Omega$. We will use this relation to target the Josephson energy by targeting a normal resistance using room temperature 4-probe measurements.

5.1 DESIGN AND FABRICATION OF JOSEPHSON JUNCTIONS

The normal resistance, R_N, depends on the overlapping area of the two junction electrodes and the thickness of the insulating barrier in between. Starting from scratch, we want to understand how different designs and fabrication parameters affect the normal resistance, and how to adjust these parameters to achieve the desired resistance range. We design a chip layout with many single Josephson junction structures arranged in a grid, using the Manhattan-style junctions as depicted in Fig. 21. The widths of junction electrodes, A and B, are detailed in the zoomed-in

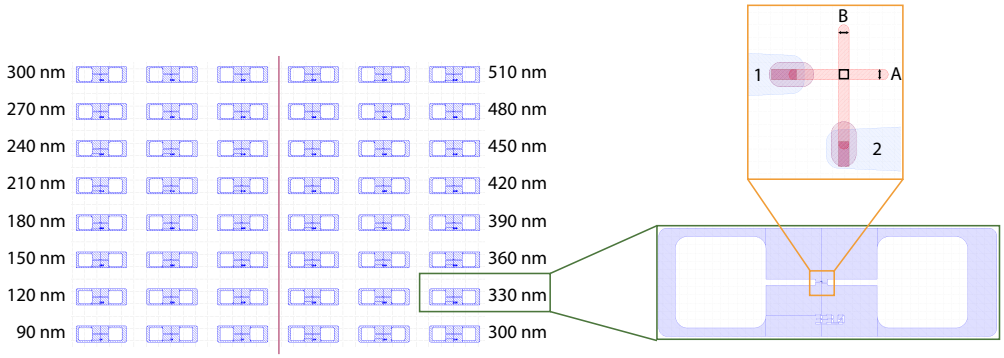


Figure 21: **Design for single junctions test:** The figure illustrates the chip layout used for testing single Josephson junctions. The layout is organized into a grid with 6 columns and 8 rows. The zoomed-in section on the right provides a detailed view of the typical junction design, where A and B denote the widths of arm 1 and arm 2, respectively. Both electrodes are designed to have the same widths ranging from 90 nm to 510 nm, with a total of 3 of each width on the chip layout. The junctions are designed in a Manhattan style.

section on the right. Both electrodes are designed to have the same widths ranging from 90 nm to 510 nm, with a total of 3 of each width on the chip layout.

The fabrication is performed on a 10×10 mm chip with a 525 µm thick Si substrate and a 300 nm thick Al metal layer on top. The Top-Down method, using Transene D etchant on the Al metal layer, creates the pad structures for the single Josephson junctions test devices. The Manhattan-style Josephson junctions are fabricated using the double-angle evaporation technique with oxidation in between using a Plassys, as detailed in the previous chapter 3. Al is used as the superconducting material, and AlOx is used for the insulating barrier, forming an Al/AlOx/Al Josephson junction.

We use MMA EL 13 as the first resist and CSAR 9 as the second resist, achieving a total height of the double resist stack of approximately 600 nm. Taking into account the thickness of the resist stack and the largest junction width of 510 nm, we should use a tilt angle of maximum 45° upon Al deposition in order to shadow the junctions. To be sure, not to short our junctions, we will use an evaporation angle of 35°. The deposition thicknesses are 50 nm for the first arm and 110 nm for the second arm. The oxidation step between the two depositions in the double angle evaporation is critical, as it determines the thickness of the AlOx insulating barrier and thereby the normal resistance. The three key parameters for controlling the thickness of the AlOx are oxidation time, flow, and pressure. In this chapter, we will keep the oxidation pressure at 120 mbar and oxidation flow of 5000 sccm and vary the oxidation time between 6 and 8 minutes. Finally, to ensure a good galvanic connection between the junction electrodes and the pads, the last step in chip fabrication involves argon milling followed by the deposition of a 200 nm thick Al layer using electron beam evaporation in the Plassys.

An optical image of the fabricated chip is shown in Fig. 22. The figure shows an optical image of the fabricated chip with single Josephson junctions. An enlarged image of one of the junction pads is shown in the inset. in addition, an SEM picture of the two junction electrodes is added.

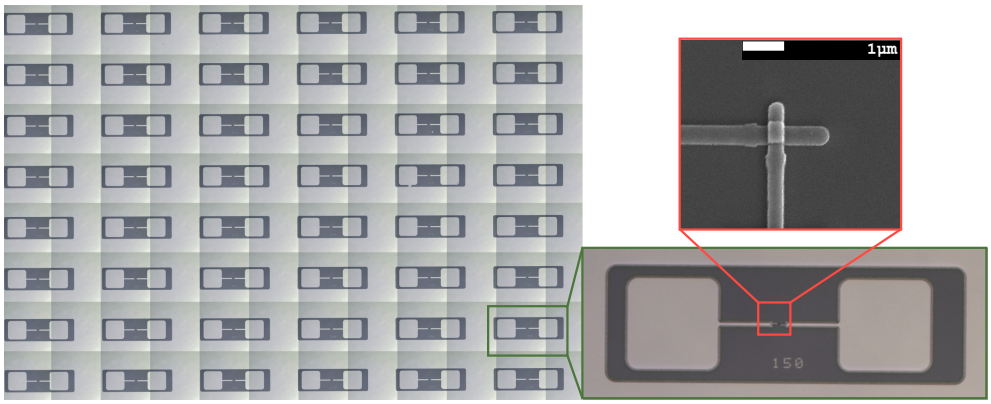


Figure 22: **JJ fabrication:** The figure shows an optical image of the fabricated chip with single Josephson junctions. The junctions are designed in a Manhattan style with varying widths ranging from 90 nm to 510 nm. The junctions are fabricated using the double-angle evaporation technique with oxidation in between. The chip is 10×10 mm with a 525 µm thick Si substrate and a 300 nm thick Al metal layer on top. The junctions are made of Al/AlOx/Al. An enlarged image of one of the junction pads is shown in the inset. in addition, an SEM picture of the two junction electrodes.

5.2 MEASUREMENTS AND RESULTS

To extract the normal resistance R_N manual 2-probe and 4-probe measurements are performed using the setup shown in the schematic Fig. 23. Figure (b) shows the 2-probe measurement setup, where a current is sent through contact 1, and a voltage is measured through contact 2. The combined current and voltage source used in the measurements is a Keithley Sourcemeter. The probes and wiring add a small fraction of resistance to the measurement, resulting in a total resistance given by:

$$R_{\Sigma_2} = \frac{V}{I} = 2R_{contact} + 2R_{wire} + R_N \tag{51}$$

In 2-probe measurements, it is not possible to corrugate for the contact and wire resistance due to the indistinguishable potential drop caused by the current source. However, 4-probe measurements allow for the suppression of this resistance, isolating the normal resistance. The figure in 23 (b) illustrates the 4-probe measurement setup, where the current is applied through the outer probes (1 and 4), and the voltage is measured through the inner probes (2 and 3). The voltmeter used is a Keysight Digital Multimeter and the current source used is a Keithley Sourcemeter. Despite the voltmeter having parasitic resistance, it is significantly smaller due to the high input impedance and minimal current flow. Hence, the voltage drop measured by the voltmeter can be considered to be that over the device. The total resistance in the 4-probe setup is given by:

$$R_N = \frac{(V_{out} - V_{in})}{I_{out} - I_{in}} \tag{52}$$

The normal resistance R_N from each device is calculated using Ohm's law by fitting the voltage as a function of the current to a linear function. Measurements are conducted with the lights off and under consistent conditions. Data is stored as a database file (.db format) and subsequently extracted and fitted using Python. The resistance for all the devices is then plotted against the junction area. Both the 2-probe and 4-probe measurements were performed, and for our devices, the difference in the normal resistance R_N found was not that different. We therefore use both

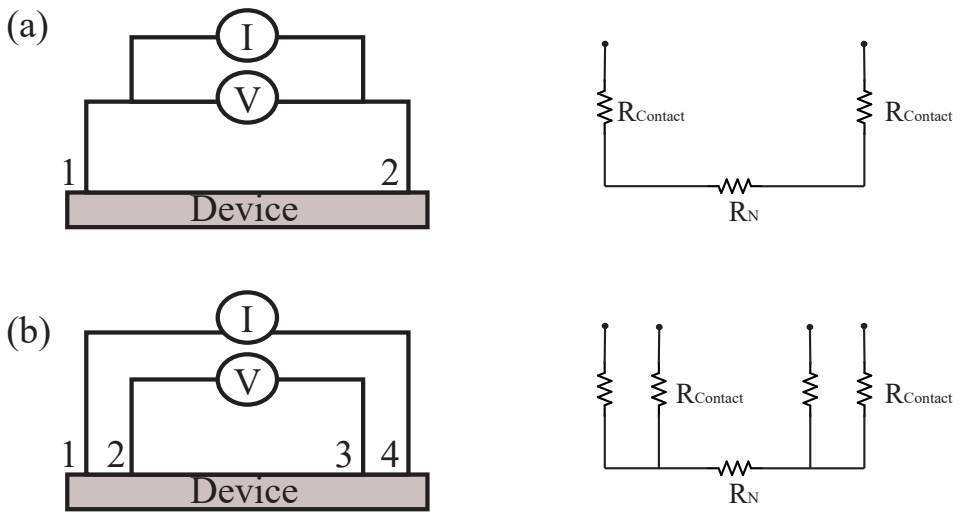


Figure 23: **2-probe and 4-probe measurement setup:** (a) A schematic of a 2-probe measurement setup with corresponding circuit diagram. The 2 contacts act as both a voltage and a current probe. (b) 4-probe measurement setup with corresponding circuit diagram. The current is applied through the outer probes (1 and 4), and the voltage is measured through the inner probes (2 and 3).

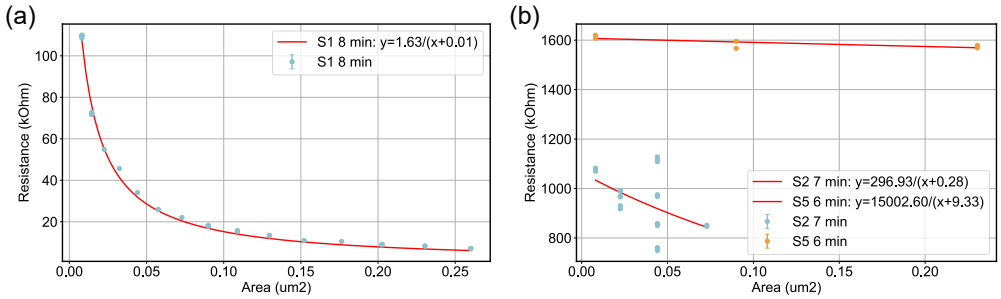


Figure 24: **Resistance as a function of area:** The extracted resistance from an I-V measurement plotted as a function of area for samples: (a) ”S1 8 min”, (b) ”S2 7 min”, and (b) ”S3 6 min”. All samples are fabricated using the same recipe, with only the oxidation time varied.

measurement setups to extract the normal resistance R_N and will not specify which one we have used for the performed measurements.

Fig. 24 shows the extracted resistance from I-V measurements as a function of the area of the fabricated Josephson junctions. The plot includes resistances for three different samples. Fig. A displays the resistance for sample ”S1”, while Fig. B shows the resistance for samples ”S2” and ”S3”. All samples were fabricated using the same recipe, with only the oxidation time varied. Specifically, sample S1 was fabricated with an oxidation time of 8 minutes, sample S2 with 7 minutes, and sample S3 with 6 minutes.

Typically, a shorter oxidation time results in a lower resistance due to a thinner oxide layer. However, the opposite trend is observed in Fig. 24. Sample S1 exhibits resistances between $10 - 100\,\mathrm{k\Omega}$, following a hyperbolic trend where the highest resistance corresponds to the

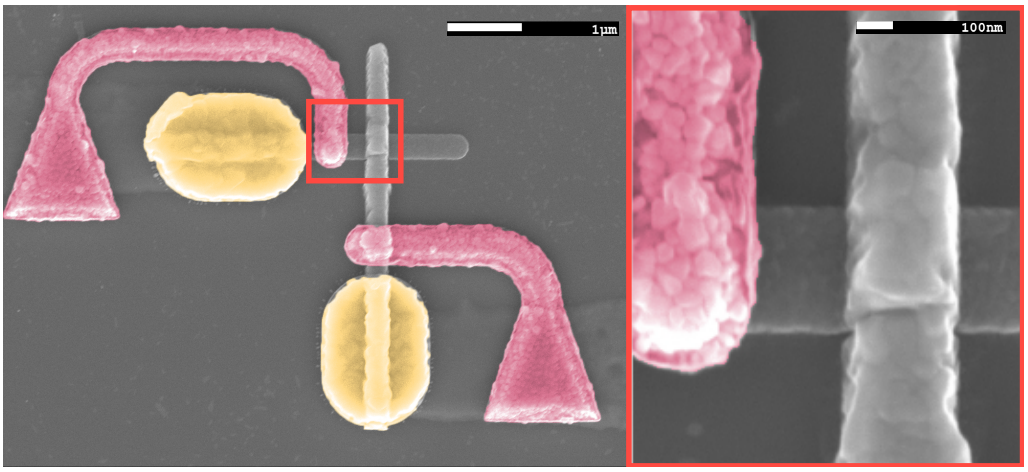


Figure 25: **Repatching the junctions:** Repatching consisting of argon milling and Al deposition was performed in the AJA. The figure shows a false-colored SEM image as an example of this process for a 240 nm junction. The yellow area indicates the first patch and the pink area indicates the repatching of the junction electrodes.

smallest junction area. In contrast, samples S2 and S3 in Fig. B exhibit significantly higher resistances, in the range of $1000 - 1500\,\mathrm{k\Omega}$. This unexpected behavior suggests potential issues with the junction electrodes, such as detachment during fabrication, or a lack of connection from the capacitor pad to the junction electrodes.

Repatching the samples and troubleshooting the fabrication

To test if the unexpected high resistance was caused by a lack of connection between the capacitor pad and the junction electrodes, samples S2 and S3 were repatched using another fabrication tool to perform argon milling and aluminum deposition. An example of the repatching can be seen in Fig. 25. The figure shows a false-colored SEM image as an example of this process for a 240 nm junction. The yellow area indicates the first patch and the pink area indicates the repatching of the junction electrodes.

The resistance of the repatched samples is plotted as a function of the junction area in Fig. 26 (a). The figure shows the resistance of the Josephson junctions for samples S2 and S3 after repatching. The resistance of the repatched samples is significantly lower than the initial measurements, with resistances now ranging from a few $1 - 20\,\mathrm{k\Omega}$. This indicates that the high resistance observed in the initial measurements was likely due to a lack of connection between the capacitor pad and the junction electrodes. The repatching process successfully resolved this issue, resulting in more consistent and reproducible resistance measurements.

Fig. 26 (b) shows the Josephson energy E_J plotted as a function of the junction electrode overlapping area for the three samples, S1, S2, and S3. Highlighted with a blue circle is the resistance and Josephson energy that we initially targeted. This data correlates with the data for sample S1, which had an oxidation time of 8 minutes. The value of the datapoint in the blue circle is for a junction overlapping area of $0.04\mu\mathrm{m}^2$ which corresponds to a junction electrode width of 200 nm and a normal resistance of $R_N \approx 34\,\mathrm{k\Omega}$.

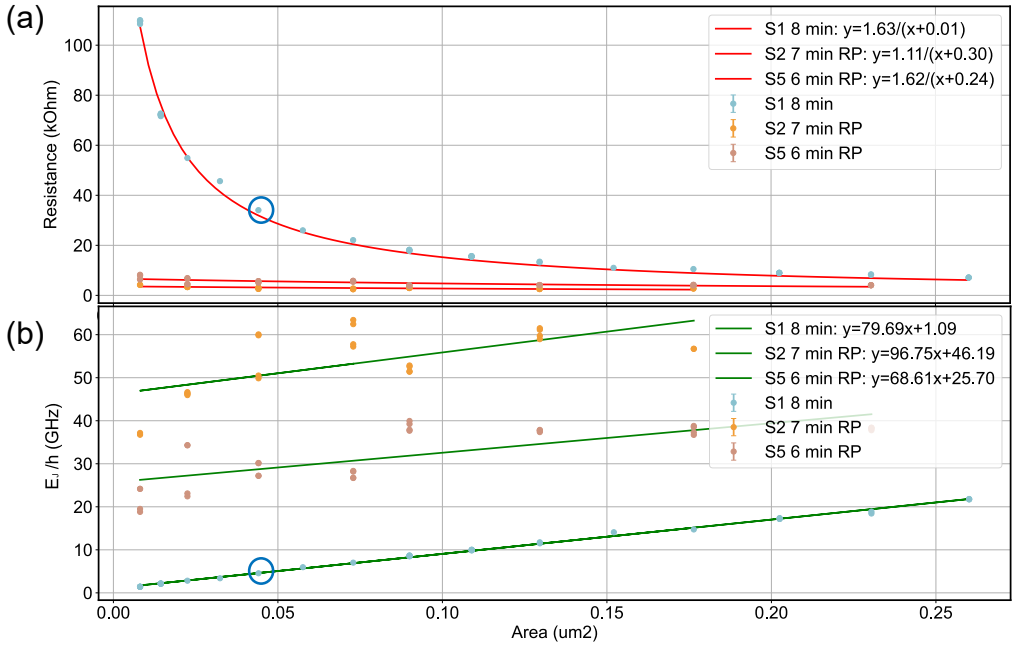


Figure 26: **Final results from the single Josephson junction measurements:** (a) The resistance is plotted as a function of the area for the sample S1 and the repatched samples S2 and S3. (b) figure shows the Josephson energy E_J plotted as a function of the junction area for the sample S1 and the repatch samples, S2, and S3. The blue circle highlights the resistance and Josephson energy that we initially targeted at $E_J = 4\,\text{GHz}$.

Reproducibility

Before we move to the next section, where we will investigate the design and fabrication of the array, we need to ensure that we can reproduce the Josephson junctions with such precision that the inductive energy, E_L, will not change significantly or be too unreliable. From the data in the previous section, it does not seem like we can consistently produce the samples, as the resistance for samples S2 and S3 is not consistent. However, colleagues from the same lab team have continued working with the junctions using the same recipe and have observed that for an oxidation time of 8 minutes, the results show the same trend as for sample S1, with a variation of less than 10%. This consistency is observed only when the machines we are using are working properly. Therefore, we believe that the fabrication recipe and workflow are reproducible.

If we have 100 JJ in the array and each JJ has a 10% variation, then the error on E_L will be a 1%. The fabrication of fluxonium is good at withstanding imprecision in fabrication for this reason [Nguyen, Koolstra, et al. 2022].

Another variable to take into account is the aging of the Josephson junctions. There is currently not much information available on this topic yet. However, even though we, do not know much about this yet, it should have the same effect on E_J as on E_L, and these effects are therefore suppressed in fluxonium. If we wanted to have even less variation, we could consider adding a laser annealing step in the fabrication recipe. This is because there can be random fluctuations in the oxide layer, which can change the energies E_J and E_L. This procedure couple increases

the precision of the nanofabrication technique of Manhattan junctions and is improved by a dispersion of 0.3%, which corresponds to a frequency variation $\sigma_f \leq 10\,\text{MHz}$ for both E_J and E_L [Nguyen, Koolstra, et al. 2022].

The fabrication process has many steps, and different parameters have varying levels of sensitivity to the reproducibility of the Josephson junctions. This is important for the single Josephson junction, but as the calculations show above, it is also crucial for making the array.

Summary

The aim of this chapter was to achieve a Josephson energy $E_J/h = 4\,\text{GHz}$ for our Josephson junctions, using the relation between Josephson energy, E_J, and the normal resistance, R_N. From this relation, we estimated that with thin film Al, we need an $R_N \approx 38.75\,\text{k}\Omega$ to reach our target. We designed and fabricated junctions with varying electrode widths on a $10 \times 10\,\text{mm}$ chip using the double-angle evaporation technique. Room temperature measurements of R_N were performed using 2-probe and 4-probe setups. Initial results showed inconsistent resistance for samples S2 and S3, likely due to poor connections. Repatching with argon milling and Al deposition resolved this issue, achieving more consistent resistance. Further reproducibility tests confirmed that with proper machine functioning, junctions could be fabricated with less than 10% variation. The closest value to one of the targets was obtained for a junction overlapping area of $0.04\,\mu\text{m}^2$, which corresponds to a junction electrode width of 200 nm and a normal resistance of $R_N \approx 34\,\text{k}\Omega$. From the data of the single Josephson junctions, we could calculate, that with 100 junctions where each would have a 10% variation, the error on E_L would be 1%. This is good enough for the array for now. In the next section, we will investigate the design and fabrication of the array.

6

TARGET EL - AN ARRAY OF JOSEPHSON JUNCTIONS

The superinductance energy we aim to target is $E_L/h = 0.7\,\mathrm{GHz}$. To remind ourselves, the superinductance energy is given by:

$$E_L = \left(\frac{\Phi_0}{2\pi}\right)^2 \frac{1}{L} = \frac{E_{JA}}{N} \tag{53}$$

We can use eq. 47 to 49 from the previous chapter to express E_L in terms of the normal resistance of the junctions:

$$\frac{E_L}{h} = \frac{\Phi_0 \Delta(0)}{4eh \cdot N R_N} = 155 GHz k\Omega \frac{1}{N \cdot R_N} \tag{54}$$

where R_N is the normal resistance of the junctions. For a super inductance energy of $E_L/h = 0.7\,\mathrm{GHz}$, we get the following relation:

$$N \cdot R_N \approx 221 k\Omega \tag{55}$$

We can obtain the right inductance energy in two ways. We can either fix the number of junctions in the array and vary the width of each junction in the array or we can fix the width of the junctions and vary the number of junctions in the array. If we choose the first option and fix the number of junctions in the array at $N = 100$, the energy relation to the normal resistance would take the form:

$$\frac{E_L(R_N)}{h} = 1.55\,\mathrm{GHz} \frac{1}{R_N} \tag{56}$$

This corresponds to a normal resistance for each junction in the array to be $R_N = 2.21 k\Omega$. This can be obtained by either a large junction width or a short oxidation time. Small oxidation times can be difficult to control and can lead to a large spread in the junction resistance.

Another strategy can be to fix the junction width and very the number of junctions. If we fix the junction width to $w = 420\,\mathrm{nm}$ corresponding to a resistance of $R_N \approx 10.5 k\Omega$, and vary the number of junctions in the array. If we do this, we get the following expression for the inductance energy:

$$\frac{E_L(N)}{h} = \frac{14.76\,\mathrm{GHz}}{N} \tag{57}$$

The results from these two strategies are just the expected normal resistance and number of junctions. The actual resistance and number of junctions in the array will be determined in the next section.

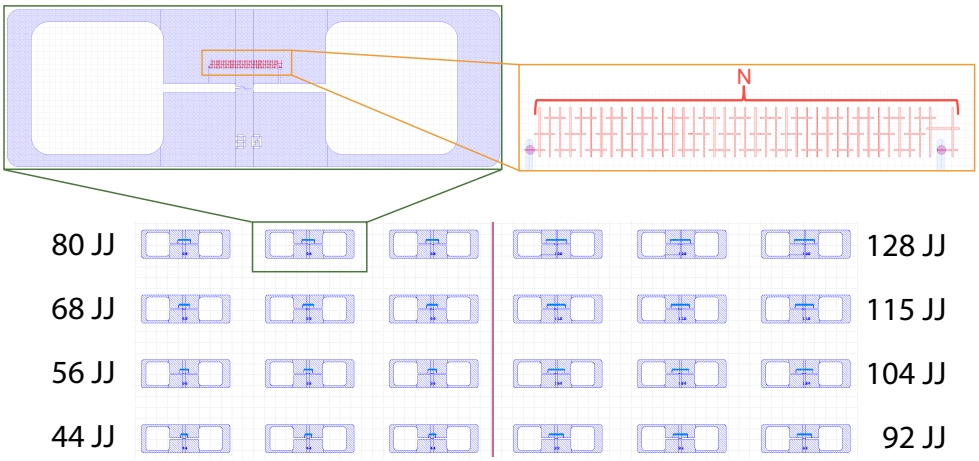


Figure 27: **Design for test array:** The figure illustrates the chip layout used for testing array of junctions. The layout is organized into a grid with 6 columns and 4 rows. The zoomed-in section above the grid provides a detailed view of the typical array design, where the number of junctions is varied between 44 to 128 junctions. All the junctions in the array are designed to have the same width of 420 nm. The junctions are designed in a Manhattan style. The design of the array is made in gdspy.

6.1 DESIGN AND FABRICATION OF THE ARRAY

The strategy to achieve the desired superinductance energy is to create many devices with different numbers of Josephson junctions, as shown in Fig. 27. The figure illustrates the chip layout used for testing arrays of junctions. The layout is organized into a grid with 6 columns and 4 rows. The zoomed-in section above the grid provides a detailed view of the typical array design, where the number of junctions varies between 44 to 128 junctions. All the junctions in the array are designed to have the same width of 420, nm. The junctions are designed in a Manhattan style. The design of the array is made in gdspy. The recipe for the array fabrication is the same as for the single junctions, with an oxidation time of 8 minutes.

The fabricated chip is shown in Fig. 28. The bottom figure shows an optical image of some of the devices on the chip, while the top figure shows an SEM image of one of the junction arrays. We will characterize the arrays using manual 2 and 4 probe measurements, and the results are discussed below.

6.2 MEASUREMENTS AND RESULTS

The normal resistance, $R_{N\Sigma JA}$, was measured using manual 2 and 4 probe measurements under the same conditions as for the single junctions. The results are shown in Fig. 29. In the top plot, the resistance is plotted as a function of the number of junctions in the array and fitted to a linear function. In the bottom plot, the superinductance energy is plotted as a function of the number of junctions in the array and fitted to a hyperbolic function. The resistance of the array increases with the number of junctions in the array, which makes sense because the total overlapping area increases with the number of junctions. Conversely, the superinductance energy decreases with the number of junctions in the array. This is expected since the resistance of the array increases

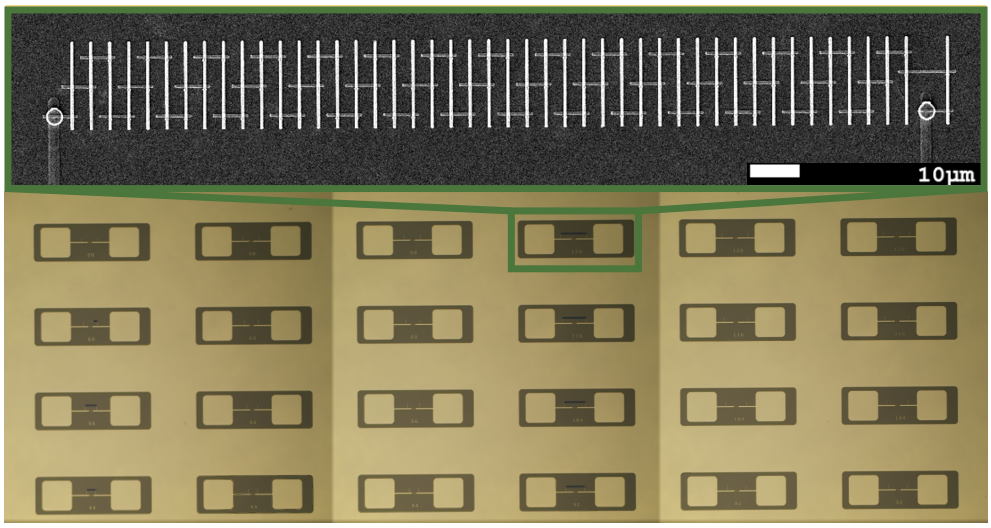


Figure 28: **Fabrication of the arrays:** The array is fabricated using Manhattan double angle evaporation in Plassys electron beam evaporator. The bottom figure shows an optical image of some of the devices on the chip. The top figure shows a SEM image of one of the junction arrays.

with the number of junctions, and resistance is inversely proportional to the inductance energy according to Eq. 54. These arrays are fabricated on the same chip as sample S1 for the single Josephson junctions, as shown above.

We did not manage to achieve the desired superinductance energy. One reason for this could be our inability to produce reproducible single junctions during the period when we were conducting experiments, as the milling and subsequent patching were not working properly. As discussed in the previous section, we have gained more knowledge about the machine we are using and can now make somewhat reproducible junctions. Another reason for the failure in achieving the target energy was the width of the Josephson junctions. Producing junctions with small resistances is necessary for obtaining the correct inductance energy, but small resistances correspond to very large junctions. If we wish to have 100 junctions in the array, then we need even larger junction widths than $w = 510\,\mathrm{nm}$, which was the largest junction width that we have produced. However, if we increase the width of the junctions significantly, we also need to adjust the deposition angles accordingly to ensure proper shadowing of the opposite arm during deposition. Therefore, the next step is to fabricate junctions with larger widths, as this corresponds to lower resistance. Once we have successfully fabricated single junctions with smaller widths, we can then fabricate arrays. For the array fabrication, it could be advantageous to maintain an array of $N = 100$ and vary the widths of the junctions.

Summery

In this chapter, we aimed to achieve a target superinductance energy of $E_L/h = 0.7\,\mathrm{GHz}$. For this purpose, we used the relation between the normal resistance R_N and the superinductance energy, E_L, and the number of junctions in the array, N. The strategy was to keep the width of the junction arms to $w = 420\,\mathrm{nm}$ and then vary the number of junctions in the array. We designed arrays with junction numbers ranging from 44 to 128. The arrays were fabricated using Manhattan double-angle evaporation with an 8-minute oxidation time. Measurements

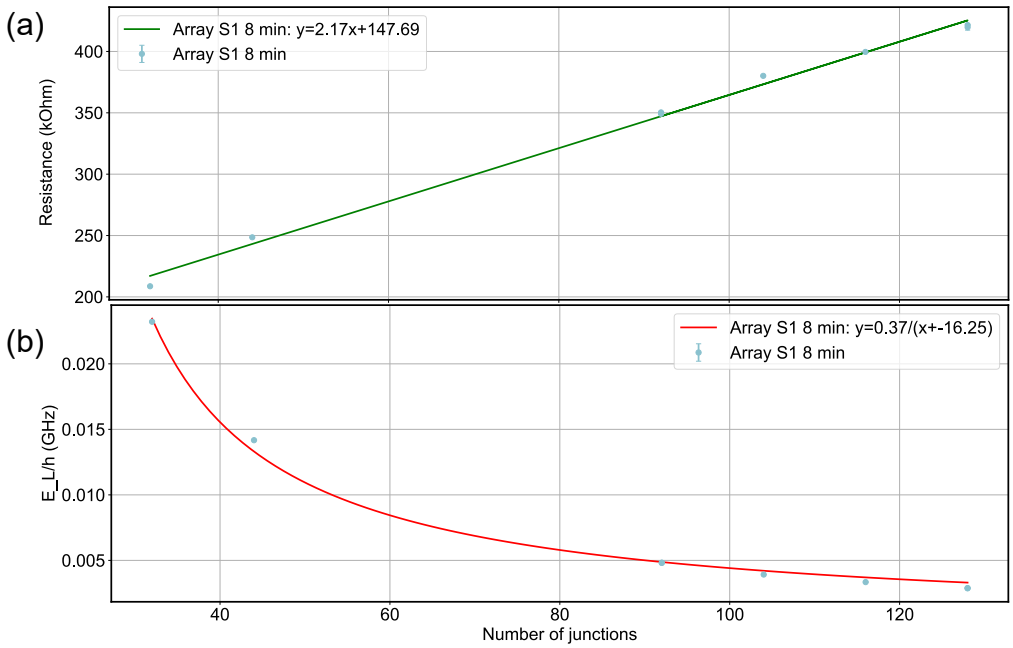


Figure 29: **Resistance and superinductance as a function of number of JJ:** In the top plot, the resistance is plotted as a function of the number of junctions in the array. In the bottom plot, the superinductance energy is plotted as a function of the number of junctions in the array.

using manual 2 and 4 probe techniques revealed that resistance increased and superinductance energy decreased with the number of junctions. Challenges included difficulties in producing reproducible single junctions and the need for larger junction widths to achieve small resistances. Refinements in our fabrication process, including adjustments to deposition angles, allowed us to produce more reproducible junctions. However, due to the time constraints of this thesis, we have not yet succeeded in producing reproducible arrays with the desired superinductance energy. Future work involves fabricating single junctions with smaller widths and constructing arrays with $N = 100$ while varying junction widths to achieve the target superinductance energy.

7

TARGET WR - READOUT RESONATORS

Resonators are a crucial part of the external circuitry of a superconducting qubit chip. It is the components that route everything together and aid the readout of the qubit state. However, it is also responsible for possible losses between the components if the dimensions of the resonator are chosen carelessly. Bare resonators (that is resonators that are capacitively connected to a transmission line without any qubits on them) can be fabricated, to give an idea of the quality factors and thereby what loss mechanisms dominate the qubit coherence time. In general, higher quality factors indicate fewer loss mechanisms. In the following, we will take a look at two different types of coplanar waveguide configurations namely λ_2 and λ_4 resonators. We want to know how we can target the frequencies using simulations and how close to these we will get when the resonators are fabricated. In this regard, we will also measure the internal and external quality factors which are obtained for the dimensions found in the previous section.

7.1 DESIGN AND SIMULATION OF RESONATORS

Coplanar waveguide resonators CPW can be modeled as LC lumped elements where the expression for the impedance and frequencies was given in section 3.2.3. We are mainly working with half-wave ($\lambda/2$) and quarter-wave ($\lambda/4$) resonators [Pozar 2012]. These two types of resonators can be engineered as a coplanar waveguide with one end that is open and another end that is either shorted (λ_4) or open(λ_2) as seen in Fig. 30. The resonator dimensions are chosen to impedance match to $48.8\,\Omega$. The transmission line and the resonators have a center conductor $a = 10.7\,\mu\text{m}$, and a gap width of $s = 6\,\mu\text{m}$ to the ground plane seen in Fig. 30. In addition, the coupling length, L_C, the coupling distance L_b, and the length, l, of each of the resonators will be varied so as to change the capacitance to the transmission line and the frequency. The resonance frequency of the $\lambda/2$ and $\lambda/4$ resonators can be written in terms of their length combining eq. 35 - 39. Writing the frequency in terms of $f = \omega \cdot 2\pi$ we get:

$$\begin{aligned} f_{r,\lambda 2} &= \frac{1}{\sqrt{L_\ell C_\ell}} \frac{1}{2l} \\ f_{r,\lambda 4} &= \frac{1}{\sqrt{L_\ell C_\ell}} \frac{1}{4l} \end{aligned} \tag{58}$$

Where $2l = \lambda_2$ and $4l = \lambda_4$ is the wavelength of the resonator mode [Göppl et al. 2008]. The frequency of $\lambda_2(\lambda_4)$ is directly proportional to the length of the resonator. The quality factor is a measure of how lossy our resonators are in terms of photons [Schuster 2007]. When the resonator is coupled to a transmission line, we can divide the quality factor into the internal Q_i

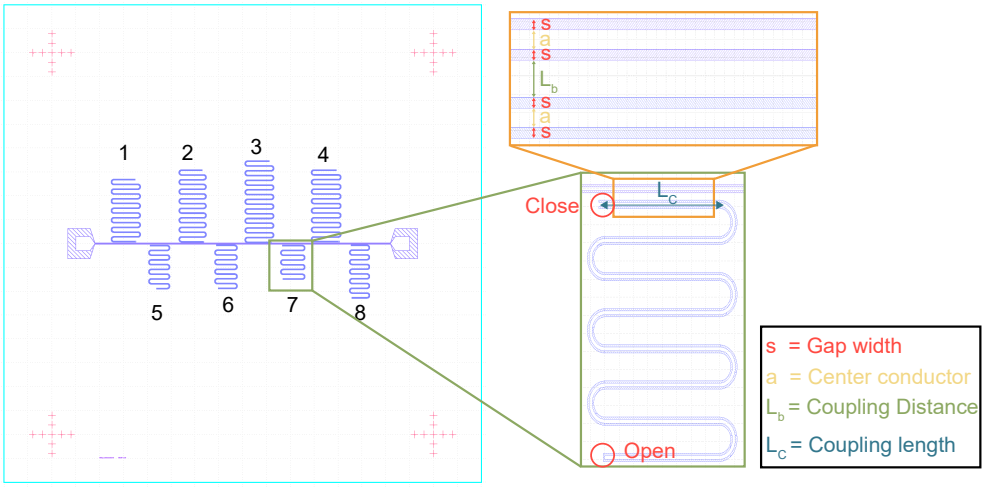


Figure 30: **Design for λ_2 (half wave) and λ_4 (quarter wave) CPW test resonators:** The design for the resonator is made in GDSpy in python. There are four λ_2 resonators and four λ_4 CPW test resonators labeled 1-8 seen in table 4. If we zoom in on resonator 7 (a λ_4 resonator), we can see the dimensions of the resonator. It has an open end and a shorted (closed) end. The center conductor is abbreviated as a, the gap width as s, the coupling length as L_C, the coupling distance as L_b, and the length of the resonator as l.

and coupled Q_c quality factors of the resonator. The total quality factor is a sum of the two and can be expressed as:

$$\frac{1}{Q_r} = \frac{1}{Q_e} + \frac{1}{Q_i} \tag{59}$$

The internal quality factor is a measure of how lossy the resonator is when it is not coupled to external circuitry. The external quality factor is a measure of how many photons are lost to the environment and depends on how strongly coupled the resonator is to the transmission line. Both the internal and the external quality factors can be expressed in terms of the scattering matrix of the resonator. The scattering matrix gives a description of how an incident wave is transmitted, reflected and scattered [Pozar 2012]. In this context, the matrix is used to relate the incident voltage with the reflected. We are mostly interested in the transmission,S_{21}, defined as [Khalil et al. 2012]:

$$S_{21} \equiv \frac{V_{out}}{V_{in}} \tag{60}$$

Where V_{in} is the voltage going into the transmission line and V_{out} is the voltage going out of the transmission line. For capacitively coupled hanging resonators, like the ones in Fig. 30. At the resonance frequency, ω_r, a large fraction of the photons will occupy the resonator instead of the transmission line resulting in a dip in S_{21}. When comparing resonators with the same geometry, the transmission is related to the quality factors of the resonator with the formula [Flanigan 2018]:

$$S_{21}(f) = 1 - \frac{\frac{Q_r}{Q_c}(1 + iA)}{1 + i2Q_r(\frac{f - f_r}{f_r})2\pi} \tag{61}$$

Where Q_r is the total quality factor of the resonator, Q_c is the coupling quality factor of the resonator, and A is an asymmetry commonly occurring at resonance due to parasitic coupling of the resonator to the transmission line. If we assume symmetric resonance, $A = 0$, the output power at resonance, that is $f = f_r$, reaches a minimum value given by $P_{out} = min(|S_{21}|)$

[Zmuidzinas 2012]. Combining this with eq. 61 we get the following approximation for the internal and external quality factors:

$$Q_c = \frac{Q_r}{1 - \min(|S_{21}|)}$$
$$Q_i = \frac{Q_r}{\min(|S_{21}|)} \tag{62}$$

Usually, the resonators are designed according to if you are making a chip with or without qubits on it. The goal of this section is to investigate quality factors and see how close our simulated frequencies are to the fabricated ones. In this regard, we have engineered Q_c such that it is close to the value of Q_i meaning it should be in the order of 10^5. One always wants as high Q_i as possible and we are typically aiming for values in the order of $10^5 - 10^6$. Note that this should be obtained in the single photon regime so as to imitate the settings for when we do actual qubit control. To measure if we are in the single photon regime, we use the relation between the average photon number and the input power [Biznárová et al. 2023]:

$$\langle n_{ph} \rangle = \frac{2}{\hbar\omega_r^2} \frac{Q_r^2}{Q_c} \frac{Z_0}{Z_r} P_{in} \tag{63}$$

Where P_{in} is the power going from our measurement setup into the transmission line, ω_r is the frequency of our resonator. Z_0 is the impedance of the transmission line, and Z_r is the impedance of the resonator. These two are impedance matched to 48.8 Ω and the two contributions therefore cancel out.

Using the relations above, the strategy is to design four of each, λ_2 and λ_4, type of resonator keeping the device geometry and only changing the l, L_C, and L_b. Changing these parameters will change the coupling and the frequency. The design of the eight resonators is programmed in Python using Gdspy and can be found in Fig. 30 labeled 1 to 8. To get an idea of the expected resonance frequencies, each of the eight resonators is simulated in Ansys HFSS. Table 4 is an overview of eight resonators and the corresponding length, l, coupling length, L_C, coupling distance, L_b, and configuration of the resonator (if it is $\lambda_2(4)$). The simulated frequencies are found to be between 5.28 and 7 GHz and are shown in the outer right column.

7.2 FABRICATION AND BONDING OF RESONATORS

The fabrication process of the resonator imitates the first three layers of an actual qubit chip as se discussed in chapter 3. The substrate layer consists of 525 µm thick Si with an area of $10x10$ mm. A 200 nm Al layer is deposited by electron beam evaporation using Plassys. The thickness of the metal layer is controlled by the rate of the evaporator. We use a rate of 1nm/s as a default. The deposition is done under a high vacuum and is typically between $6 - 7 \cdot 10^{-7}$ mbar. The metal layer is then patterned using electron beam lithography and developed. We use wet etching by dipping it into Transene D. For a more detailed recipe for the bare resonator chip see SI. An optical image of the final fabricated chip can be seen in Fig. 31 (a). The chip is then bonded to a qubit chip carrier PCB from Quantum Machines see in Fig. 31 (b). The bonding is done using a semi-automatic bonder named *F/S Bondtec 5630* using Al thread. (c) The chip is connected to a puck, loaded into a dilution fridge and cooled down to around 30mK. The resonator is then connected to a VNA and the resonator frequencies are found described in the next section.

Res #	l **(mm)**	L_c **(mm)**	L_b (μ **m)**	$\lambda_{2/4}$	f_{sim}
1	8.918	440	18	λ_2	6.755
2	9.631	440	16	λ_2	6.257
3	11.466	475	4	λ_2	5.276
4	10.470	510	17	λ_2	5.757
5	4.624	217	19	λ_4	6.510
6	5.016	440	16	λ_4	6.002
7	4.304	400	20	λ_4	6.989
8	5.471	310	14	λ_4	5.506

Table 4: **Table showing resonator simulation frequencies for eight resonators:** For each of the eight resonators is noted the corresponding length, l, coupling length, L_C, coupling distance, L_b, and configuration of the resonator (if it is $\lambda_2(4)$). The eight resonators are simulated in Ansys. The resonance frequency can be seen in the outer right column and is found to be between 5.28 GHz and 7 GHz.

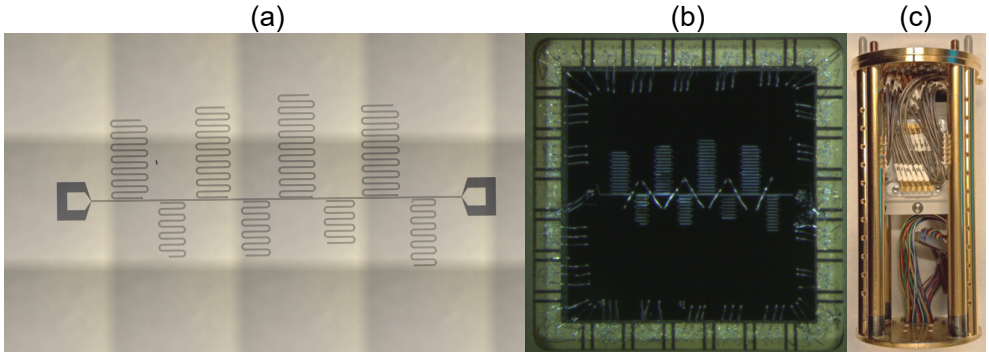


Figure 31: **Resonator fabrication:** The resonator is fabricated using the Top-Down fabrication method using Transene D as an etchant. (a) Is an optical image of the fabricated chip. (b) The chip bonded to a qubit chip carrier PCB from Quantum Machines see in Fig. 31. (c) The chip is connected to a puck, loaded into a dilution fridge and cooled down to around 30mK. The resonator is then connected to a VNA and the resonator frequencies are measured described in the next section.

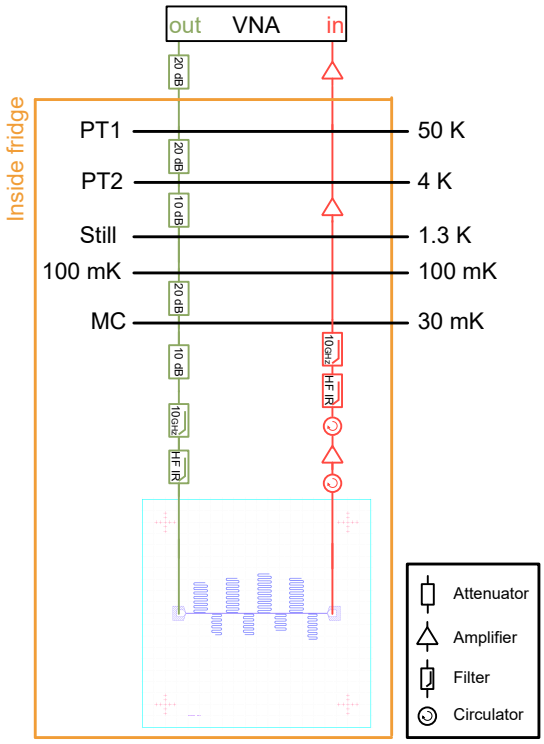


Figure 32: **Schematic of Resonator measurement setup:** The resonator chip is loaded into a dilution fridge and cooled down to around 30mK. From the fridge, it is connected to a vector network analyzer VNA, which can send in microwave photons. The orange square in the figure indicates the wiring inside the fridge. Inside the fridge are five stages (PT1, PT2, Still, 100 mK, and MC) having different temperatures where the coldest is 30 mK where the puck is connected to. A total of 60dB attenuation is added to the fridge spread over the five stages.

7.3 MEASUREMENTS AND RESULTS

The measurement setup including a fridge wiring diagram can be seen in Fig. 32. The figure shows the outer control hardware consisting of a Vector Network Analyzer VNA. The orange square in the figure indicates the wiring inside the fridge. Inside the fridge are five stages (PT1, PT2, Still, 100mK, and MC) having different temperatures where the coldest being around 30 mK. It is at this stage, the puck is connected to. A total of 60dB attenuation is added to the fridge spread over the five stages. The VNA are capable of sending and reading microwave signals and for our purpose, it is used to measure the transmission, S_{21} of the transmission line.

Frequency sweep

The resonator frequencies are found by sweeping the frequency of the VNA and looking for dips in the transmission indicated by the red circles in Fig. 33. The frequency range swept over, is from 5 GHz to 8 GHz. However, the figure only shows the range from 5 GHz to 6.6 GHz due to a Traveling Wave Parametric AmplifierTWPA eigen frequency around 7 GHz interfering with the resonator frequencies. Knowledge about the TWPA frequency was not obtained before the fabrication of the chip. However, this should be taken into account in future designs. The resonator peaks found in the sweep are compared to the simulated values and the deviation in percent is shown in table 5. The resonator frequencies are found to be within 5.3% of the

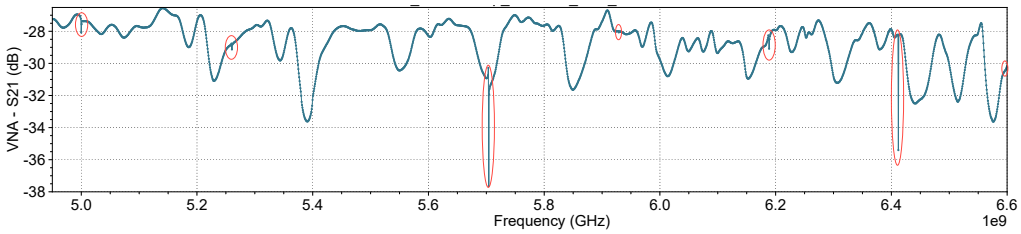


Figure 33: **Resonator sweep from** 5 GHz **to** 6.6 GHz**:** This plot show a resonator sweep from 5 GHz to 6.6 GHz done to get an overview over where the resonance frequencies of the resonator chip lye. At around 7 GHz, the frequency of the Traveling Wave Parametric AmplifierTWPA has its eigenfrequency interfering with the resonator frequencies and therefore these are not included in the plot.

Res #	Simulated	Measured	Difference	Percent off
1	6.755	6.65079	0.10421	1.542709
2	6.257	6.188275	0.068725	1.09837
3	5.276	5.000277	0.275723	5.225986
4	5.757	5.70416	0.05284	0.917839
5	6.51	6.41214	0.09786	1.503226
6	6.002	5.92884	0.07316	1.218927
7	6.989	-	-	-
8	5.506	5.260185	0.245815	4.464493

Table 5: **Resonator frequencies:** The table shows the simulated and measured frequencies for the eight resonators. The difference in absolute value and in percentage is also shown. The resonator frequencies are found to be within 5.3% of the simulated frequencies.

simulated frequencies. It is suspected, that the resonator 7 is not visible due to interference with the eigenfrequency of the TWPA. Note that the comparison of which measured frequencies correspond to which simulated frequencies, is only a guess. The paring of these can indeed be a lot different than one expect. A deviation in the frequency can be due to a lot of different factors. For instance, we saw a slight over-etch in the gap between the center conductor and the ground, which could also indicate, that some of the thickness of Al had been etched away. This should be further investigated, to say for certain, what the cause of the deviation is. We will not go into more detail about this and only focus on a selection of the three best resonators and look at their quality factors.

Powerscan

For each of the resonator frequencies, we then do a powerscan, to see more precisely the frequency and then to be able to fit the data to get an idea of the quality factor of the resonator. An example of a powerscan can be seen in Fig. 34. The powerscan is a repeated sweep over a

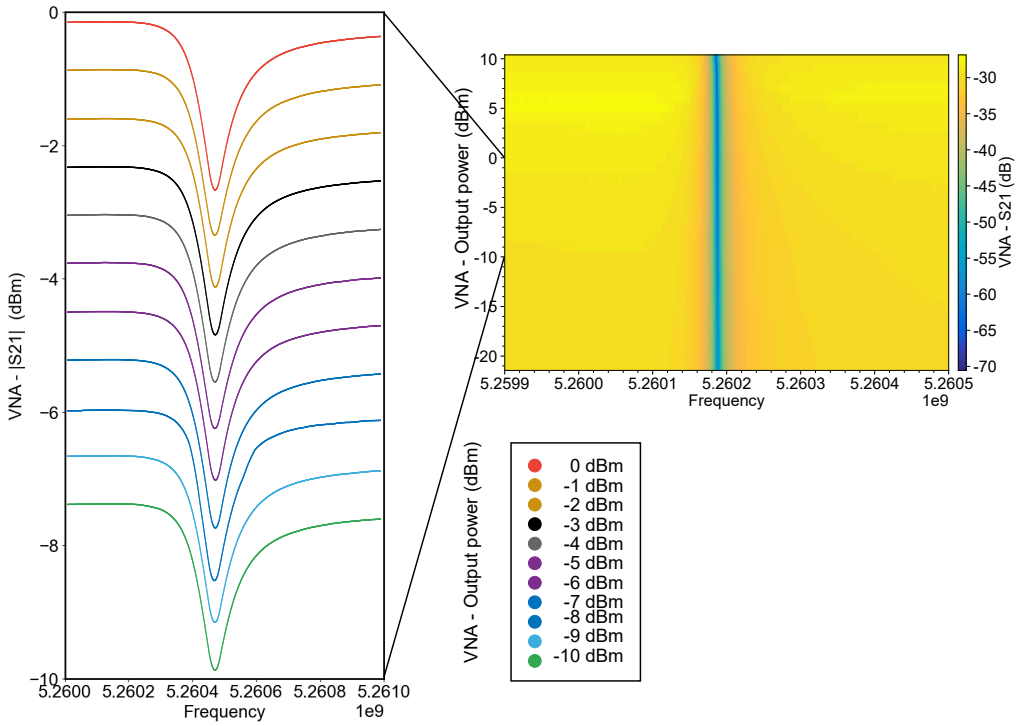


Figure 34: **Resonator powerscan:** The figure shows a powerscan in the frequency range 5.299 GHz to 5.2605 GHz. A zoom-in on the powerscan shows that it constitutes of small frequency range sweeps at different VNA output powers. The power ranges from 10 to −20 dB.

short frequency range only changing the VNA output power between each sweep. The powerscan is done to see how the resonator behaves at different input powers and for the powerscan shown in the figure the power ranges from 10 to −20 dB. However, the output power of the VNA is not the same as the power going into the resonator. The power going into the resonator is the output power of the VNA minus the attenuation at room temperature, the attenuators in the fridge and ideal oså the attenuation from all other components like the cables, the bonding etc. However, the attenuation of the last mentioned components is difficult to quantify and can vary from setup to setup.

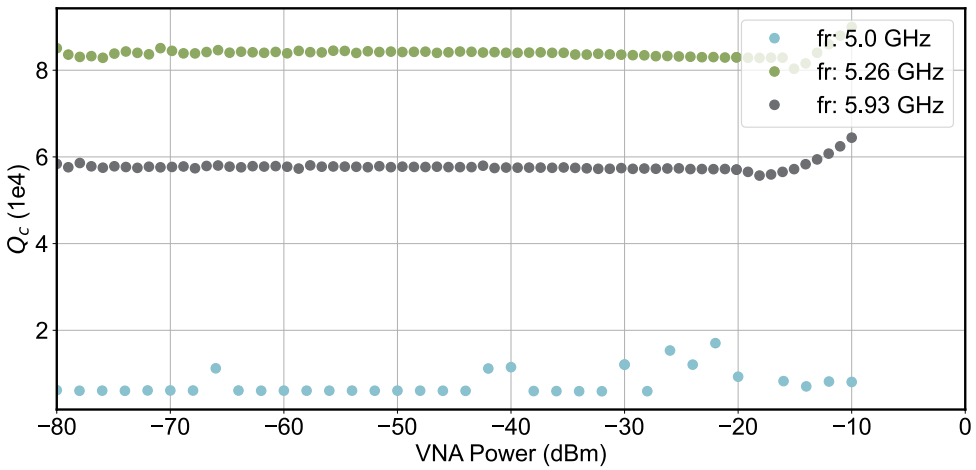


Figure 35: **Coupled quality factor plotted as a function of VNA output power:** The Coupled quality factor as a function of output power for three different resonator frequencies namely 5.0 GHz, 5.26 GHz, and 5.93 GHz. This is the external Quality factors as a function of the VNA power. Included in the x-axis values is an attenuator of 20 dB.

Quality factors

The data from the powerscans are extracted and the resonator frequencies are then fitted using a Python package called Resonator which uses the relations between S_{21}, Q_i, and Q_c shown in eq. 61 to 62 to fit the resonator peaks and calculate the quality factors. Specifically, are we interested in the internal and external quality factors. In fig. 35 shows the extracted external quality factor as a function of the VNA output power for the three frequencies 5.0 GHz, 5.26 GHz, and 5.93 GHz. The external quality factors are found to be in the order of 10^4 respectively. The external quality factors in Fig. 35 are found to be pretty stable as a function of VNA output power. This is different from the internal quality factors shown in Fig. 36.

Internal quality factors for the three resonators all have $Q_i \approx 0.5 \cdot 10^6$ seen in Fig. ref 36. The average number of photons can be calculated from the formula in eq. 63. The output power is proportional to the number of photons. When calculating the average photon number, one need to take into account the total added attenuation of 60 dB from the fridge, the 20 dB room temperature attenuator at the VNA and the additional attenuation from the cables. For the latter an attenuation of 10 dB is assumed. This gives a total of 90 dB attenuation. The power going into the resonator can be estimated to be $P_{in} = -80 - 90 = -170$ dBm. As before mentioned, the attenuation can vary depending on the cables, and the bonding wires on the chip, and can even vary from when the fridge is cooled down to when it is at room temperature. The true value is therefore hard to estimate and $\langle n_{ph} \rangle$ can be viewed as an upper limit [Bruno et al. 2015]. The average photon number for the resonator frequencies 5.26 GHz and 5.93 GHz are found to be in the order of 50 photons and the resonator at frequency 5.00 GHz in the order of a few photons. Thus, according to the estimated attenuation, only the last resonator can be said to have been operated in the single photon regime.

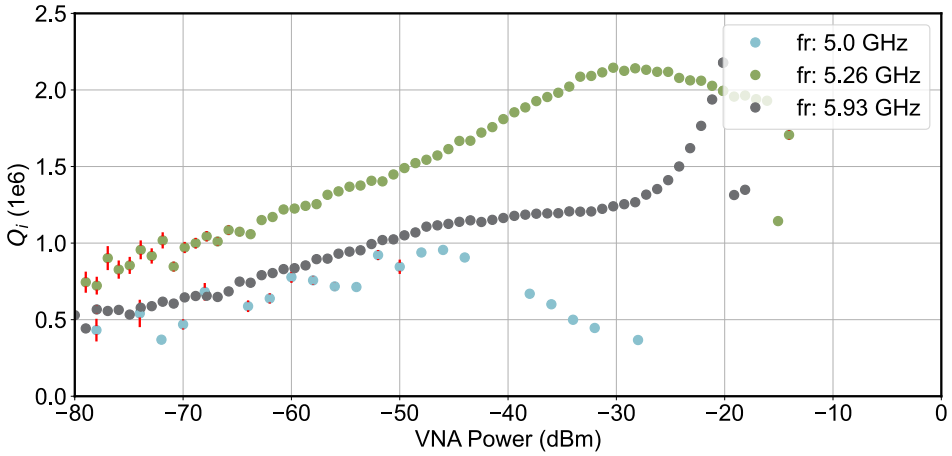


Figure 36: **Internal quality factor plotted as a function of VNA output power:** The internal quality factor as a function of output power for three different resonator frequencies. This is the external Quality factor as a function of the VNA power. Included on the x-axis values is the effect of the room temperature attenuator of 20 dB.

Summary

We have designed, simulated, fabricated, measured, and characterized eight resonators with frequencies between 5.25 GHz and 7 GHz. The resonators were designed in gdspy and simulated in Ansys HFSS and fabricated using electron beam evaporation and wet etching. We measured the resonators in a dilution fridge using a VNA. The quality factors were extracted from the transmission S_{21} using the Python package called Resonator. The resonator frequencies were found to be within 5.3% of the simulated frequencies. The external and internal quality factors were found to be in the order of 10^4 and $0.5 \cdot 10^6$ respectively in the single photon regime.

8

CONCLUSION

Fluxonium qubits present a promising avenue for advancing quantum computing due to their insensitivity to charge and flux noise. This type of qubit exhibits low transition frequencies and high anharmonicity, which are essential for enhancing coherence times and enabling rapid qubit control. This project has focused on the design, simulation, fabrication, and characterization of fluxonium qubit components. The goal was to achieve the target values $E_C/h = 1\,\text{GHz}$, $E_J/h = 4\,\text{GHz}$, and $E_L/h = 0.7\,\text{GHz}$ decided through a comprehensive study of existing experimental and theoretical literature.

The first component we explored was the capacitor pads of the fluxonium qubit. We aimed to achieve a capacitance energy of $E_C/h = 1\,\text{GHz}$ by targeting a total capacitance of $C_\Sigma = 19.37\,\text{fF}$. The total capacitance, in principle, has contributions from all the different components in our circuit. We omitted some small contributions and kept the contributions from the junction, the flux line, the drive line, and the readout line constant. Using Ansys Maxwell 3D simulations, we optimized the design to meet the desired capacitance energy by adjusting the size of the capacitor pads, the distance between the capacitor pads and the ground, and the distance between the pads. This iterative simulation workflow allowed us to achieve a successful capacitance energy of $E_C/h \approx 1.03\,\text{GHz}$ with a total capacitance of $C_\Sigma = 18.7\,\text{fF}$, within the fabrication uncertainties.

The second component we investigated was the Josephson junction. We targeted the Josephson energy $E_J/h = 4\,\text{GHz}$ by aiming for a normal resistance $R_N \approx 38.75\,\text{k}\Omega$. We explored the relationship between normal resistance and fabrication parameters by designing a series of Josephson junctions with varying electrode widths and oxidation times. Through careful fabrication using Manhattan style double angle evaporation technique and room temperature 2- and 4-probe measurements, we successfully reached the target for the Josephson energy with a junction overlapping area of $0.04\,\mu\text{m}^2$, corresponding to a normal resistance of $R_N \approx 34\,\text{k}\Omega$ and a junction width of 200 nm. It is believed that the variance on our junction fabrication is around 10%, which should be sufficient for fabricating the array.

The final component of the fluxonium qubit is the array of Josephson junctions. We aimed to achieve a super inductance energy of $E_L = 0.7\,\text{GHz}$ which can be done in two ways. We can either fix the number of junctions in the array and vary the width of each junction in the array or we can fix the width of the junctions and vary the number of junctions in the array. We designed and fabricated arrays of Josephson junctions with widths of 420nm, varying the number of junctions to meet the target inductance energy. However, we have not yet achieved the desired superinductance energy and further optimization is needed.

In the last chapter, we investigated the fabrication, design, and simulation of resonators for reading out the qubit state. We performed simulations in Ansys HFSS, designed and fabricated resonators using wet etching of Al on Si, and characterized them with Vector Network Analyzers in dilution fridges. The fabricated resonators had frequencies within 5.3% of the simulated values, with external and internal quality factors in the order of 10^4 and approximately $0.5 \cdot 10^6$, respectively, in the single-photon regime.

While we have yet to design and fabricate a complete fluxonium qubit chip, the designs and simulations of the individual components provide a robust foundation for future work. The next steps involve refining the fabrication process, particularly the Josephson junction arrays. With continued effort and optimization, realizing a fully functional fluxonium qubit chip using these target parameters is within reach.

9

OUTLOOK

9.1 PRELIMINARY SINGLE FLUXONIUM QUBIT DESIGN

In this thesis, we have designed and simulated the different components of the fluxonium qubit, aiming to achieve the target values:

$$E_C/h = 1,\text{GHz}, \quad E_J/h = 4,\text{GHz}, \quad E_L/h = 0.7,\text{GHz} \tag{64}$$

In the following, we aim to integrate all the work we have done so far to propose a design for a fluxonium qubit chip. The primary design of a fluxonium qubit chip of size 10 mm x 10 mm is shown in Fig. 37. The design contains four identical fluxonium qubits (a). Each qubit has a flux line (b), a drive line (c), and a readout resonator (d), all capacitively coupled to the qubit. Additionally, the design includes three test structures for the array (e) and three test structures for the Josephson junctions (f). These test structures are used to verify that the fabrication process is working as intended.

(a) Qubit design

The values we have aimed to target in this thesis are primarily focused on the qubit itself. We found that we could achieve a capacitance energy of $E_C \approx 1.03\,\text{GHz}$. This energy was obtained for the combination of $C_{pads} = 3.3938\,\text{fF}$, $C_{g,t} = 22.9\,\text{fF}$, and $C_{g,b} = 22.5\,\text{fF}$. . However, the contributions from the flux line, drive line, readout line, and single Josephson junction were kept at a constant value of $C_{r,b} = C_{d,t} = C_{f,t} = C_{f,b} = 4\,\text{fF}$ and $C_{r,t} = C_{d,b} = 0$, $C_J = 0.5\,\text{fF}$. The next step in this regard is to simulate the capacitance energy, taking these values into account properly, as they might differ significantly from what was initially proposed.

The Josephson energy was found to be $E_J \approx 4\,\text{GHz}$ corresponding to a normal resistance of $R_N \approx 38.75\,\text{k}\Omega$ electrode with of 200 nm and an area of 0.04 µm. Colleagues from the same team have continued working with the junctions using the same recipe and observed that for an oxidation time of 8 minutes, the variation in the junctions is less than 10%. However, the next step regarding single Josephson junction fabrication is to verify that we can achieve the same variation in the junctions as our colleagues. Even when using the same recipe, junction fabrication might vary depending on the person who fabricates it.

The array fabrication faced some challenges, including producing reproducible single junctions and the need for larger test junction widths to achieve smaller resistances. However, due to the time constraints of this thesis, we have not yet succeeded in producing reproducible arrays with the desired superinductance energy. Future work involves fabricating single junctions with

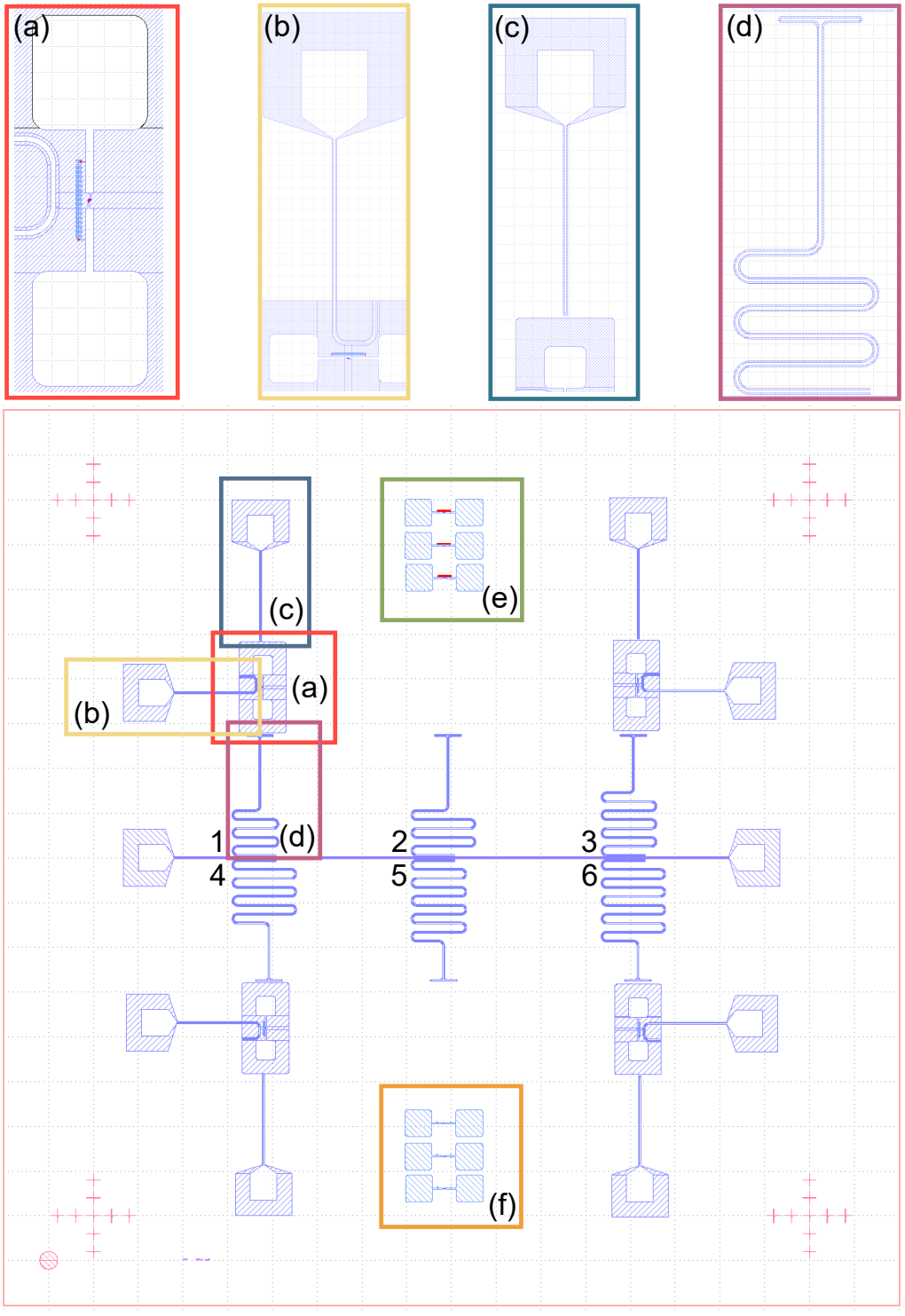


Figure 37: **Prelimary design of fluxonium qubit chip:** The total size of the design fits a 10 mm x 10 mm chip. The design contains four identical fluxonium qubits (a). Each qubit has a flux line (b), a drive line (c), and a readout resonator (d), all capacitively coupled to the qubit. Additionally, the design includes three test structures for the array (e) and three test structures for the Josephson junctions (f). These test structures are used to verify that the fabrication process is working as intended.

Res number	**1**	**2**	**3**	**4**	**5**	**6**
Resonator Length (μm)	4410	4545	4680	4874	5069	5264
Coupeling length L_c	440	440	440	440	440	440
Frequency (GHz)	6.73976	6.53932	6.35047	6.09741	5.86259	5.64519

Table 6: **Table of resonator frequencies of Single Fluxonium qubit chip:** Each of the resonator numbers corresponds to the number on the fig. 37. The resonator frequencies have a spacing of around 200 MHz.

smaller widths and constructing arrays with $N = 100$ while varying junction widths to achieve the target superinductance energy.

(b) Flux line and (c) Drive line

The drive line and the flux line both have the same dimensions as the resonators discussed in the fabrication section 3. They share the same geometry as our coplanar waveguide CPW: $s = 6\,\mu\text{m}$ and $a = 10.7\,\mu\text{m}$. This configuration provides an impedance of $Z = 48.8\Omega$ ensuring impedance matching with the rest of the circuitry. The next step is to properly engineer the drive and flux lines, optimizing their distance from the qubit for capacitive coupling, as detailed in Chapter 4.

(d) Readout resonators

The readout resonators investigated in Chapter 7 have frequencies between 5.25 GHz and 7 GHz. The resonator frequencies were found to be within 5.3% of the simulated frequencies. The external and internal quality factors were found to be on the order of 10^4 and $0.5 \cdot 10^6$, respectively, in the single photon regime. However, the design of the resonators on the preliminary chip has been slightly modified from those investigated in Chapter 7, as seen in Fig. 37 (numbered 1-8). The reason for these changes is, among other factors, to ensure that the resonators have stronger capacitive coupling to the qubit, enabling effective readout. Additionally, to avoid the TWPA eigenfrequency, the resonators should be below 7 GHz, as this is the eigenfrequency of the TWPA. Lastly, to prevent interference, the frequency difference between two qubits on the same processor should be $f_{q2} - f_{q1} \geq 20$ MHz ensuring no rotation of nearest neighbor qubits upon driving one qubit [Nguyen, Koolstra, et al. 2022].

The resonator frequencies of the new design are shown in Table 6. One could fabricate a chip with bare resonators using the new design to verify if the frequencies and quality factors match expectations. However, this should not be the primary focus, as other team members have already fabricated resonators with similar designs and observed good results.

Summary

As seen above, there is much more work to be done before a final design can be proposed. The fabrication process should follow the steps outlined in Chapter 3, specifically as shown in Fig. 14. The next steps are to fabricate the design and characterize the qubits. The qubits will be characterized by measuring their frequency, anharmonicity, and coherence times. The latter is a crucial step to verify whether these parameters, which are not yet seen in the literature, can help advance future fluxonium fabrication.

SUPPLEMENTARY INFORMATION

https://1drv.ms/f/s!Aiu2rBZS3805jr9WRoQ-A49aJX63Sg?e=kUUj4k
In this folder, you will find the supplementary information containing:

- Data treatment
  - Reliability of probe station
  - Review of fluxonium papers
- Derivations
  - Derivation of JJ
- Designs
  - Fluxonium
  - Resonator
  - Wafer
  - JJ
- Manuals
  - AJA
  - AFM
  - Auto bonder
  - Beamer
  - Elionix 125kV
  - Elionix 100kV
  - JEOL jsm 7800F
  - Laurell Spin coater
  - Load puck into fridge
  - Plassys
  - Probe station
  - VNA
- Recipes
  - JJ and Array
  - Resonators
- Simulations
  - Requirements.txt

  - Energy of fluxonium
  - Energy transmon flux basis
  - Energy transmon charge basis
  - Energy of fluxonium simulation explained
- Software
  - Ansys HFSS
  - Ansys Maxwell 3D
  - appCAD resonator calculator
  - Besidin calculator

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