Transport through quantum dots at the $LaAlO_3/SrTiO_3$ interface

Master Thesis

Written by *Anders Valdemar Bjørlig*

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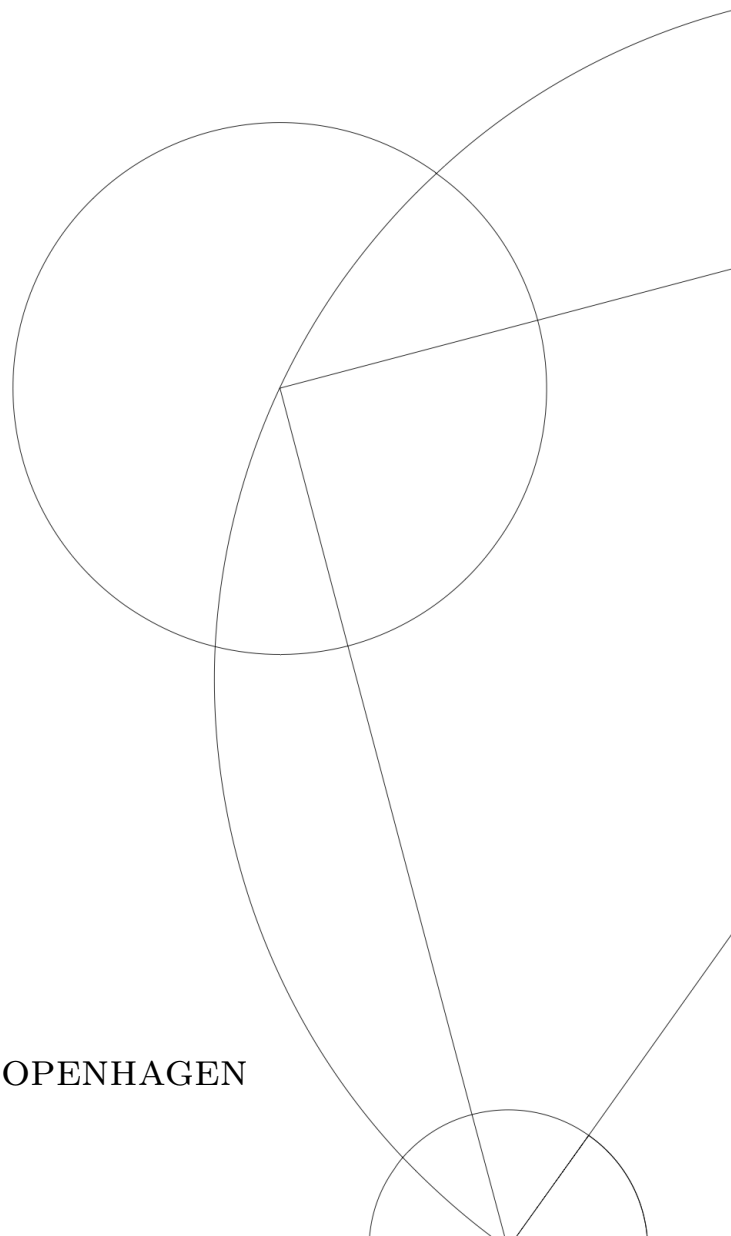
Supervised by

Thomas S. Jespersen



University of Copenhagen

UNIVERSITY OF COPENHAGEN

Faculty:	Faculty of Science
Institute:	Niels Bohr Institute
Author(s):	Anders Valdemar Bjørlig
Email:	lmd944@ku.dk
Title and subtitle:	Transport through quantum dots at the $LaAlO_3/SrTiO_3$ interface -
Supervisor(s):	Thomas S. Jespersen
Handed in:	November 20^{th}, 2017
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Abstract

The 2DEG formed at the $LaAlO_3/SrTiO_3$ interface has seen a huge growth of interest since its discovery[1]. Researchers have discovered a large variety of phenomenons like gate-tunable superconductivity[2], magnetic ordering[3] and spin-orbit coupling[4]. As researchers improve device fabrication new and exciting results are appearing. Currently the material is still in a state where new fabrications methods and ideas for novel devices could lead to further understanding of the underlying physics. Quantum dots formed at the interface have displayed themselves as effective probes resulting in interesting phenomena like formation of electron pairing without superconductivity[5] and negative charging energies[6] telling a completely different story than what is known from semiconductor nanostructures.

This thesis is a study in new fabrication methods of oxide heterostructure devices and transport measurements of quantum dots. Work has been done to implement a new single-step electron beam lithography fabrication method. Here PMMA resist is used as a hard mask, a role normally appointed to a deposited layer of insulating material on the $SrTiO_3$ surface. The method hinges on implementation of a treatment that cleans the surface of the $SrTiO_3$ prior to $LaAlO_3$ deposition. The validity of the fabrication method is tested through transport measurements on specially designed devices. The surfaces are cleaned with a simple treatment of oxygen plasma ashing and water cleaning. It is observed that using this technique results in conductive samples and that the 2DEG is defined by the patterned design. Nano scale split-gate devices are also fabricated using this method. To test their abilities electrical transport measurements are carried out at $\sim$ 12 mK in a ^{3}He - ^{4}He dilution refrigerator. The split-gates modulate the conductance through a narrow channel with characteristics dominated by the electric field dependence of the dielectric constant in $SrTiO_3$. The results further underline the validity of the fabrication method yet the side-gates do not result in any quantum phenomena.

An established method developed by Trier *et al.* [7] is also used to fabricate quantum dot structures using metallic electrodes as gates. The method uses a deposited layer on the $SrTiO_3$ surface to protect the quality of the surface during lithographic steps. Two types of designs are tested; a simple split-gate setup and a modified version designed to outline the shape of an island. Dots are formed in the modified design in two samples. The dependence on energy levels of the dot in an applied magnetic field is tested revealing the appearance of higher spin states accompanied by fluctuations in the g-factor between $\sim 0.35 - 3.2$. The higher spin states are attributed to exchange interactions between the electrons while the fluctuations are a result of different spin and orbital contributions from the individual energy levels. Results from a superconductive sample is also briefly presented.

Contents

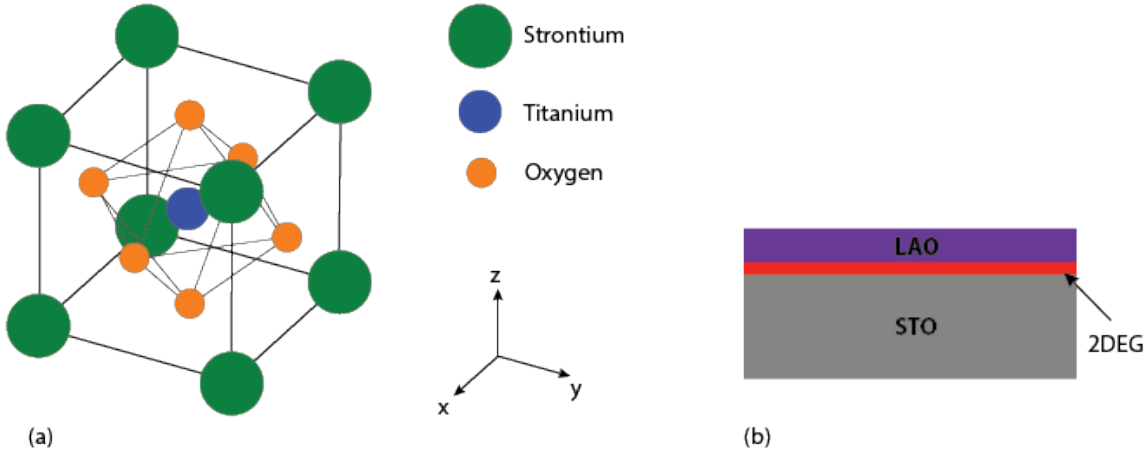

Figure 1: Crystal structure of STO. (a) Schematic of the unit cell of the perovskite crystal structure. The titanium sits at the center surrounded by 6 oxygen atoms. (b) Simple schematic of the LAO/STO interface. The base is made up of a $SrTiO_3$ crystal, called the base substrate. On top a thin layer of LAO is deposited which results in a 2DEG forming in between.

1 Introduction

1.1 Oxides introduction.

The Two-dimensional Electron Gas (2DEG) found at the interface between Lanthanum-Aluminum-Oxide ($LaAlO_3$) and Strontium-Titanate-Oxide ($SrTiO_3$) has seen a large growth in academic interest since its discovery in 2004 by A. Ohmoto and H. Y. Hwang[1]. Both of these materials are band gap insulators in bulk form but surprisingly if sandwiched together into a heterostructure (a layer by layer stacking of the materials) exotic behaviors appear including ferroelasticity[8], magnetism[3], spin-orbit coupling[4] and superconductivity[2]. Several of these phenomena turn out to be gate-tunable by a local electrostatic gate. The intermixing of this multitude of phenomena have great interest for fundamental science and industry alike. The $LaAlO_3/SrTiO_3$ interface are far from the only oxide heterostructure of interest, several materials following the same building structure show great qualities in different areas[9]. Oxide materials come in two forms the heterostructure, made up of several materials, and single oxides, like SiO_2 made of one oxidized material. While single oxides exists as a stable part of the electronics industry the oxide heterostructure is in a much earlier stage. Due to advances in growth and fabrication methods over the recent years heterostructures are currently in a place were researchers reliably can create experimental circuits of high enough quality to investigate the faucets of oxides[10].

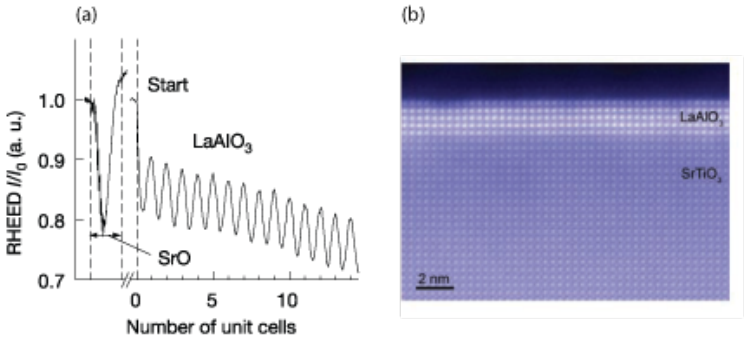

Figure 2: Growth of LAO. (a) RHEED plot during growth of c-LAO. Each peak corresponds to a new crystal plane. Figure is taken from reference[1]. Transmission electron microscopy image of the LAO/STO interface displaying the good match between the two materials. Figure taken from reference[48]

1.2 The $LaAlO_3/SrTiO_3$ heterostructure

The overall name for materials like LAO and STO is Transition-Metal-Oxides (TMO's), which as the name suggests is oxide materials containing elements from the transitionmetal group of the periodic system. They have the general formula ABO_3 [11]. Here A and B are metals, typically A is a rare earth or alkaline element while B is the transition metal and O is oxygen. At room temperature these elements pack into lattice structure known as the perovskite structure, see fig. 1.(a) visualized with STO. The A atom is placed in the corners while the B atom is placed in the center surrounded by 6 oxygen atoms. STO and LAO can be grown together using modern deposition processes with few lattice defects as long as the LAO films are kept relatively thin. The lattice mismatch is only 3% yet thick films of LAO will result in cracks (thick is above 15-20 nm)[12]. If the right conditions are met a 2DEG will emerge, see fig. 1.(b). The complete heterostructure will have alternating planes of BO and AO_2 stacked on top of each other. This results in alternating layers with neutral charge for STO while LAO will have layers switching between positive and negative charge.

1.3 The formation of the 2DEG in LAO/STO

Formation of the 2DEG in LAO/STO have been achieved in a number of different ways. To display the diversity of the oxide materials three of these shall be discussed here along with the proposed mechanisms for the 2DEG. Ohmoto and Hwang[1] prepared samples by depositing a thin crystalline-LAO film (c-LAO) on a (001) STO substrate using pulsed laser deposition (PLD). Here a high energy laser is pulsed on a substrate target, evaporating it and letting it condense on the mounted sample. By Reflection high-energy electron diffraction (RHEED) the formation of individual planes can be observed, commonly stated in no. of unit cells, see fig. 2. This fabrication turned out to be highly depending on parameters including the oxygen pressure in the growth chamber (PO_2), temperature during growth, amount of unitcells of LAO grown and interestingly the surface termination of the STO substrate[1]. Samples do not become conductive with PO_2 above 10^{-4} Torr so typical values of

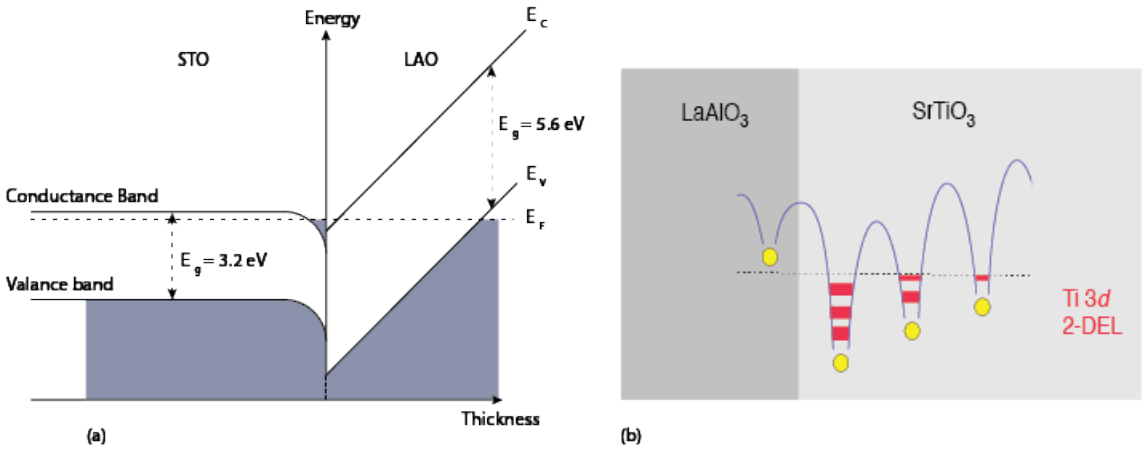

Figure 3: Polar catastrophe in LAO/STO. (a) Schematic of the conduction band and valence band around the interface. E_F is the Fermi energy. The bandgap energies have been stated in the two materials. (b) Schematic showing the location of the carriers. The titanium atoms create potential wells that confine the electron close to the interface. Figure is taken from reference[48]

10^{-4} - 10^{-6} Torr is used. High temperatures are essential for the crystalline formation of the LAO and single unit cell deposition control. Typically 600 - 800°C are used. By measuring samples post deposition with a conductive atomic force microscope (c-AFM) it was discovered that the entire STO substrate was conductive[13]. To counter this a second annealing step was introduced in a higher oxygen pressure of about 400 mbar. Indeed after this the c-AFM revealed that conduction was located in a sub 10 nm thick area below the interface[9]. Additionally it is required that at least 4 unit cells of LAO is grown on the sample and that it is grown on TiO_2 terminated STO and not with a SrO layer.

These requirements for formation of the 2DEG have led to various proposed mechanisms of which two is discussed here. The first is based on the potential difference across the LAO/STO interface. The alternating charged layers of $(LaO)^+$ and $(AlO_2)^-$ in the $LaAlO_3$ layer results in an electric field which causes a potential build up. If the $SrTiO_3$ is terminated by TiO_2 the valence band and conduction band of the $LaAlO_3$ will increase with film thickness, see fig. 3.(a). When the valence band of the LAO exceeds the conduction band of the STO energy can be gained by moving electrons across the interface to the STO. This incidentaly happens when the LAO has grown to a thickness of 4 u.c., known as the critical thickness. If the STO is terminated by a SrO layer the same effect could lead to a hole gas forming at the interface yet this has not been experimentally confirmed. This theory is formally referred to as the polar catastrophe develop by Nakagawa *et al.* in 2006[14]. Due to this need for perfectly TiO_2 surfaces a great step forward in quality of devices was made with the discovery of a method based on etching with chemical etching and oxygen annealing[15].

It is quite well established that heating bulk STO in low pressure will result in conductance throughout the entire substrate due to oxygen diffusion outwards. When the oxygen leaves one electron is freed changing the valence of the titanium from Ti^{4+} to a mix of Ti^{3+} and Ti^{4+}. While the appearance of these vacancies do explain the conductive ability of LAO/STO they do not explain why a critical thickness of c-LAO is needed to get conductive samples. They are however the primary explanation when the LAO film is grown at room temperature resulting in an amorphous thin film.

It was believed for a long time that a-LAO grown on STO would result in insulating properties yet in 2011 Chen *et al.* showed that LAO grown at conventional growth parameters resulted in a conductive interface[16]. Here oxygen vacancies was confirmed by x-ray photoelectron spectroscopy (XPS) that revealed a growing Ti^{3+} peak with increasing film thickness and when heated in a oxygen rich environment the interface conductivity disappeared both consistent with oxygen vacancies. It was further argued that the oxygen was diffusing towards the deposited material during growth to oxidize the plasma. Other phenomena are cited as playing a part in forming the 2DEG such as Lanthanum incorporation into the STO during growth.

While this ends the summary of the theories for formation of the 2DEG in $LaAlO_3/SrTiO_3$ the actual position of the carriers have not been mentioned. It has been hinted that the carriers are electrons, resulting in a n-type conductor and that they are connected to the titanium atoms in the STO lattice. As it turns out the most important bands for conduction in STO is the five-fold degenerate d-band of the titanium atom. The surrounding oxygen atoms break this degeneracy splitting the d-band into a high energy doublet state, the e_g states, and a low energy state, the t_{2g} state[9]. The lowest lying state is split into 3 states, the d_{XY}, d_{XZ}, d_{YZ}. This is backed by XPS measurements of LAO/STO, that also reveal that the carriers are limited close to the interface. They are pinned in place close to the Ti atoms due to the coulomb potential of the atoms that create sharp quantum wells while a slight band bending restrict the carriers close the interface, probably located in different Ti-planes[17], see fig. 3.(b). The d-bands couple readily in the plane of the interface through the p-orbitals of the oxygen atoms that are placed in between. The bands extent far more in the plane of the interface than out of it resulting in high mobile carriers along the interface while transport out of it is highly suppressed.

1.4 Fabrication of nanodevices on LAO/STO

Currently realization of nanocircuits for transport measurements on LAO/STO is a field of research. A selection of fabrication methods have shown themselves as fertile proving grounds for experiments but researchers are still developing new processes. In this section some of the most prominent fabrication methods will be discussed.

1.4.1 Fabrication styles

Conventional lithography can be used on the interface without the need for any etching or milling of the sample owing to the short depth placement of the 2DEG. It is however very important to keep the STO surface clean of any resist residue as this has been shown to lead to insulating samples[7]. To ensure this two methods are commonly used. The first one exploits the critical thickness of c-LAO devices, and as such is not usable for amorphous samples[18]. By depositing 2 unit cells of LAO the surface is shielded yet remain insulating, see fig. 4.(a). Lithography can then be used to define the conductive areas without damaging the STO surface. Typically a layer of amorphous material like a-LAO or a-STO is deposited were the sample should remain insulating. Then the crystalline LAO can be grown to the critical thickness of 4 u.c. while the LAO on the amorphous regions likewise will be amorphous and remain insulating.

A different approach is taken when the top film is amorphous. By depositing a suitable top layer across the entire sample, much like the first 2 u.c. of LAO from before, the surface can once again be protected. Following lithography on this top layer it can be selectively wet-etched with chemicals

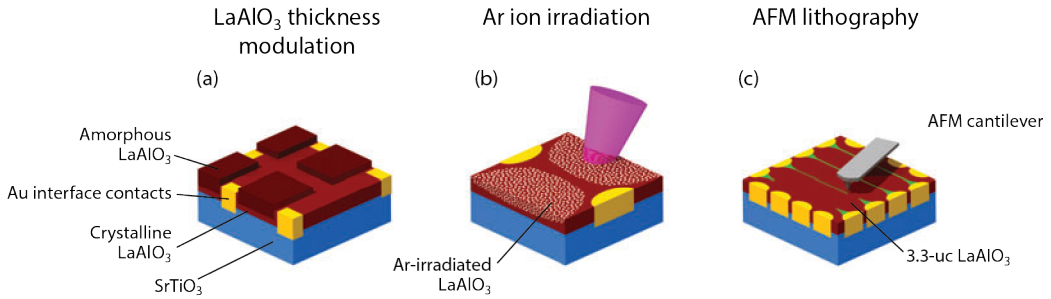

Figure 4: Common fabrication methods of devices on LAO/STO. (a) LAO top layer method. First a thin layer of c-LAO is deposited. Lithography are conducted on this top layer. When c-LAO is grown later above the critical thickness defined parts will grow a-LAO instead limiting the 2DEG. (b) by local ion irradiation with Argon the LAO/STO interface can be made insulating. (c) Using a c-AFM conductive regions can be sketched by moving the tip around the surface. All three figures are taken from reference[9]

revealing the STO surface for deposition[7]. Apart from the need for the top layer to be etch-able it is required that it does not make the STO conductive. Fabrication of devices based on this method have been achieved by application of AlO_x[19] and LaSrMgO (LSM)[7] as protective top layers. Especially the LSM have proven itself through its high versatility to stay insulating under a wide variety of growth parameters[16]. The resolution limit of different types of lithography means that devices can be made ranging from 1 μm to $\sim$ 50 nm using these two methods[9].

Argon irradiation have been used to define conductive regions of LAO/STO[20]. By coating STO in c-LAO above the critical thickness the STO surface is protected yet the entire sample is conductive, see fig. 4.(a). By covering the parts of the sample that should remain conductive using lithography and bombarding the rest of the sample with Argon ions the non-covered areas will become insulating. Typical device resolution is in the range of 50 nm.

One of the most interesting ways devices have been fabricated on the LAO/STO interface by the use of an c-AFM tip[21]. First a layer of c-LAO is grown just below the critical thickness, 3 u.c. By applying a voltage to the tip of the AFM and moving it into close proximity of the LAO/STO substrate the sample can be turned conductive in a highly local region. The tip can then be moved around the interface effectively drawing, or sketching, the wanted device. The mechanism for surface conduction is based on protonation through the addition or subtraction of water at the surface[22]. Owing to the small size of the c-AFM tip devices can be made with sizes down to 5 nm.

1.5 Quantum dots in LAO/STO

A wast amount of different quantum devices have been fabricated using the above techniques including Hall bars[7], Josephson junctions[19], rings[18], weak links[23] and 1D channels[24] all revealing interesting physics. In this study the focus is on the realization of a quantum dot (QD) on the LAO/STO interface. Quantum dots are a perfect tool to study the inherent electron-electron interaction owing from the Ti d-bands as the energy scale from these interactions are dominant[25]. This section will run down the basics of quantum dot physics and discuss some of the prominent results acquired from previous research done with QD's in LAO/STO.

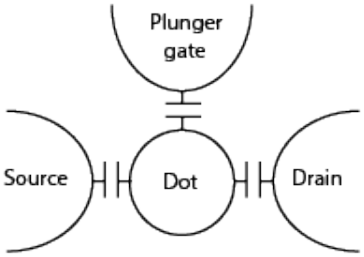

Figure 5: Schematic drawing of a quantum dot visualized with one gate. The dot is capacitively coupled to the source, drain and gate.

1.5.1 The basics

Quantum dots are formed when electrons are confined into small areas, commonly defined with electrostatic gates depleting the surrounding area of carriers, see fig. 5. The dot will be capacitively coupled to its surroundings, the source, drain and gates, here referred to as the plunger gates, that can tune the electron density of the dot. The dot is characterized by two tunnel couplings, Γ_1 and Γ_2, that describes the probability of tunneling through the dot and the chemical potential of the dot μ_N, which represents the energy it would require to add one more electron to the dot. When several electrons are confined on a small island the act of adding a new one requires energy due to the coulomb repulsion between negative charges. This energy, called the charging energy E_C, can be determined from the capacitance of the dot. The electrostatic energy of a dot with N electrons will be given as

$$E_{elstat} = \frac{e^2 N}{2C} \tag{1}$$

with e being the electron charge, meaning that the difference between N and N + 1 electrons can be expressed as

$$E_C = \frac{e^2(N+1)}{2C} - \frac{e^2 N}{2C} = \frac{e^2}{C} N \tag{2}$$

in the limit $N \gg 1$. If we assume that the dot is a disc with radius r then the capacitance of the dot will be $C = 8\epsilon\epsilon_0 r$ where ϵ and ϵ_0 is the relative dielectric of the material and vacuum permittivity respectively. This will result in an inverse dependence of E_C on ϵ. For STO the dielectric constant is $\approx$ 20000 at sub-Kelvin temperatures[26]. This leads to a suppression of the electrostatic energy of the material which will make the next energy scale even more important, the single-particle level spacing. This energy, also called the confinement energy, Δ, arises due to the discrete quantum states inside the dot. These are governed by the density of states of the specific dot.

For these energies to be measurable some requirements have to met. First the thermal energy of the system have to negligible compared to the both E_C and Δ

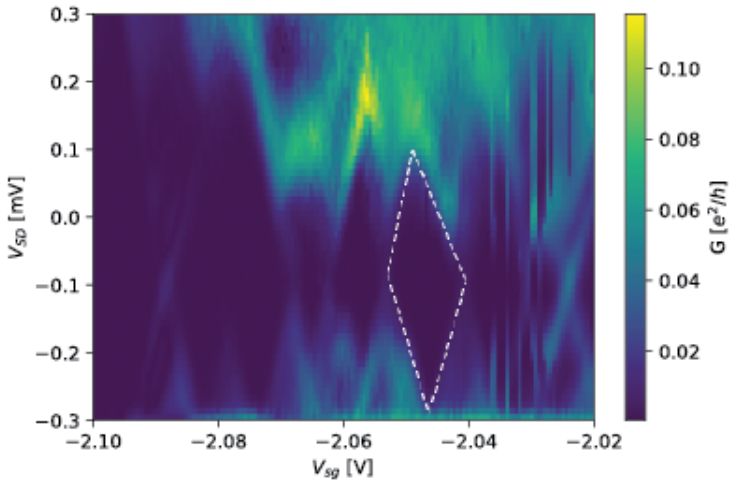

Figure 6: Coulomb diamonds from a device made in this work. One of the diamonds have been outlined by a dashed line.

$$k_B T \ll E_C, \quad k_b T < \Delta \tag{3}$$

were k_B is the Boltzmann constant. If this requirement is not met thermal excitations will smear out the transport features. Additionally the Heisenberg's uncertainty principle can give us a limit on the tunneling resistance R_C. The uncertainty principle states that

$$\Delta E_C \Delta t > h \tag{4}$$

with h being the Planck constant and $\Delta t = R_t C$ the time associated with adding a new electron to the dot. Combining these terms with our prior expression for E_C we get

$$R_t > \frac{h}{e^2} \tag{5}$$

meaning that the resistance resulting from tunneling to the quantum dot has to be larger than the resistance quantum $h/e^2 \approx 25.8k\Omega$. If these conditions are met transport over the quantum dot will occur as resonance peaks, called coulomb peaks, in conductance when energy levels line up with the source and drain. Off resonance conductance will be blocked. This phenomena is called coulomb blockade and has been studied intensively in semiconductor structures. If the plunger gate is measured against the source drain bias (V_{SD}) a very recognizable pattern of diamond structures appear, see fig. 6, with the conductance peaks outlining the structure. As V_{SD} is increased the current becomes non-linear so the differential conductance dI/dV_{SD} is measured instead.

While we have established a framework for understanding the energy level structure of the dot the actual mechanics allowing current to flow still have to be explained. If we extent the use of the chemical potential from the dot to the source and drain as well we can picture the system as seen

in fig. 7. The chemical potential of the dot with population N, μ_N, is still defined as the energy required to add the N'th electron to the dot while the chemical potential of the source and drain is defined in the conventional way as the highest energy level occupied by electrons in the conduction band. The voltage applied to the plunger gate will modify the chemical potential following the relation

$$\mu_N(V_{pg}) = \mu_N(V_{pg}^0) - e\alpha_{pg}\Delta V_{pg} \tag{6}$$

with $\Delta V_{pg} = V_{pg} - V_{pg}^0$ being the change in plunger gate. α_{pg} is a constant called the lever arm that functions as a measure of the coupling between gate and dot. Note by solving the capacitance matrix of the entire system for the potential on the dot α_{pg} is extracted as the relation between the capacitance of the gate electrode and the sum of capacitance's in the entire system $\alpha_{pg} = \frac{C_{pg}}{C_\Sigma}$. Similarly increasing the source drain bias modify the chemical potentials of source and drain opening a window for current to flow following

$$\mu_S - \mu_D = -eV_{SD} \tag{7}$$

With these effects in mind we can now explain the coulomb blockade effect. At zero source drain bias the diagram is a flat energy profile with the dot energy levels in between, see fig. 7. As the plunger gate voltage is moved the energy levels of the dot move and when an energy level aligns with the source and drain a resonance is hit and electrons can move over the dot through the energy level causing a current to flow. If the source drain bias is swept instead the bias window opens up and when an energy level is placed in between the electron can jump across the dot, fig. 7.(c). This creates windows of current flow in the V_{SD} - V_{pg} space defined by the equation

$$|V_{SD}| = \frac{\Delta V_{pg}}{\alpha_{pg}} \tag{8}$$

This relation results in the diamond shapes as seen in fig. 6 as the window of conductance in V_{pg} rises with increasing V_{SD}. Equation (8) also provides a relation to calculate the lever arm for the gate electrode as the slope of the diamonds. This simple picture explains sequential tunneling of electrons across the ground states of a QD. The picture can be extended further by including excited states and higher order tunneling processes but that is omitted in this work.

A final interesting remark on quantum dots is how the energy levels change based on outside interference, here specifically the dependence on an applied magnetic field. We can write up an equation for the addition energy that includes the Zeeman effect

$$E = E_C + \Delta + E_Z \tag{9}$$

The Zeeman energy includes the interaction between the magnetic field and spin of the electrons on the dot. This expression excludes any types of interactions between the electrons and any orbital effects. While other effects have been recorded in dots in LAO/STO it is still viable to initially start with a simple picture. The Zeeman energy is given by

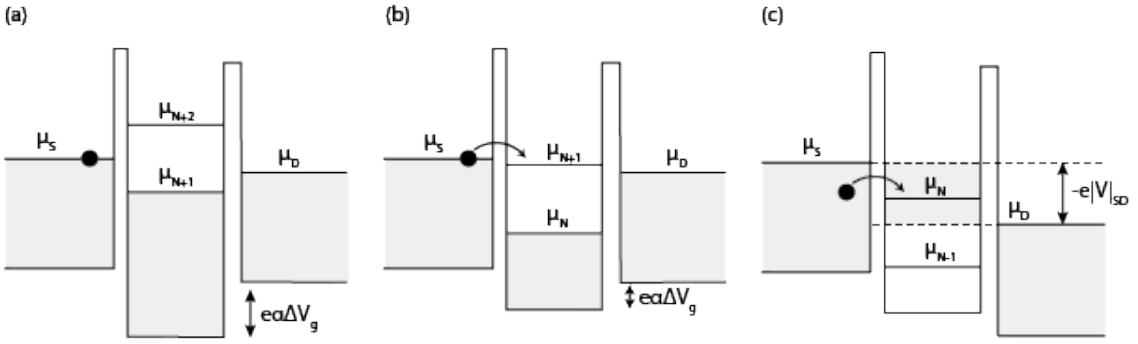

Figure 7: Transport scenarios over a quantum dot. (a) No state is near the source and drain potentials. Current is blocked. (b) By changing the plunger gate voltage the levels inside the dot move and when they line up with source and drain current can flow. (c) By varying source drain bias the potentials of source and drain change allowing for current as well.

$$E_Z = g\mu_b SB \tag{10}$$

here μ_b is the Bohr magneton, S the spin and g the electronic g-factor. The other terms in the energy equation are independent of the magnetic field meaning the Zeeman energy will be the only term acting with the magnetic field. What we can gather from equation (10) is that the energy levels will move as a function of B-field with a sign defined by the spin of the state and a slope defined by the g-factor.

1.5.2 Dot studies

The basic device structure for successful studies are either based on split-gates defined near the interface[6] or c-AFM sketched dot structures[5]. Currently some of the interesting results coming from these studies are connected to the electron phenomena of superconductivity. Superconductivity is explained as the formation of so called Cooper pairs which is a pair of electrons behaving like one particle owing to a positive interaction between the two mediated by phonons. These pairs are formed at a critical temperature T_C where the material undergo a phase change and become superconductive. Interestingly this pairing of electrons stay in effect even when tuned out of the superconductive regime in dot structures on LAO/STO[6], see fig. 8. This was observed exactly by studying the energy level shift with applied magnetic field. Over some critical pairing field B_P the energy levels split into two new levels moving according to the Zeeman splitting discussed above. QD's on LAO/STO have also been reported to display a negative charging energy which would constitute an energy gain for placing more than one electron in each energy level which again generates a pairing effect of electrons without a superconductive phase[6]. Further study of these effects and their connection to superconductivity might yield very interesting results.

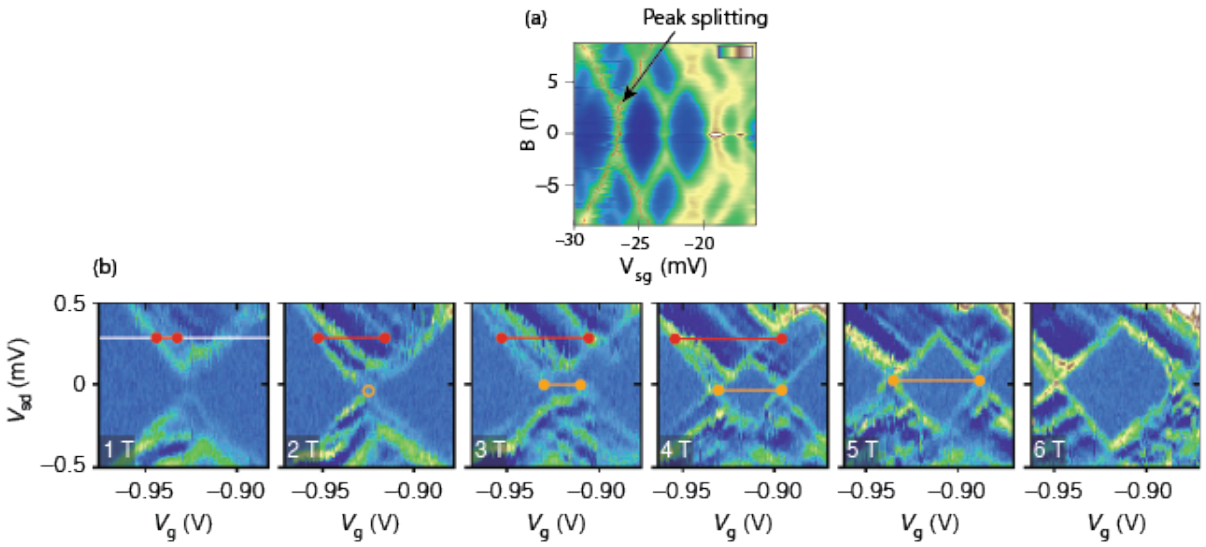

Figure 8: Electron pairing in LAO/STO without superconductivity. (a) Shift of two peaks with magnetic field. At some pairing field, B_p, the peaks split into two. Figure is taken from reference[5]. (b) Coulomb diamonds at different magnetic field. As the field increases the peak between the two diamonds split creating a new diamond in between. Firgure is taken from reference[6].

1.6 Focus of this study

To end this sections the different focus points for this work will be layed out. The work have revolved around fabrication of nanostructures on LAO/STO with the goal of making a working quantum dot and perform transport experiments. The fabrication is based on the patterning method by Trier *et al.*[7] that have been used to make working dots[6]. The patterning of the electrostatic gates on these structures was done with conventional electron beam lithography and tests were made to implement photo lithography as it could introduce a time save in fabrication. A whole new way of fabrication was also implemented utilizing PMMA resist as a masking layer prior to LAO deposition. A large variety of device geometries were tested throughout the study.

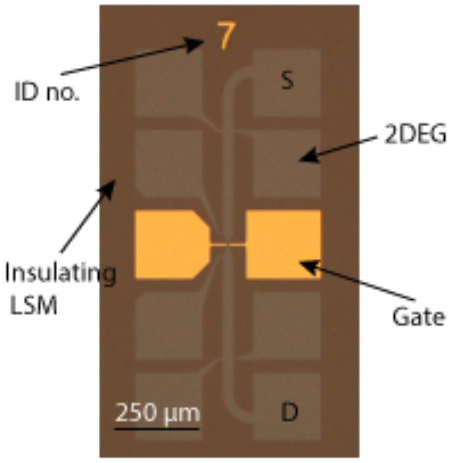

Figure 9: Optical microscopy image of a Hall bar patterned using a LSM top layer. The different features have been outlined with arrows. S and D are printed on the two bond pads designed as source and drain.

2 Methods - fabrication procedures

2.1 Sample preparation and fabrication

A substantial part of this project has been testing different designs and fabrication methods with the end goal of mesoscopic transport measurements of the 2DEG in the interface of $SrTiO_3/LaAlO_3$. During this section an overview of the fabrication ideas and their motivation will be given followed by explanations of the different methods used during the work.

2.2 Fabrication overview

All devices created in this work have taken up the same form, an example can be seen in fig. 9. A conductive Hall bar is patterned on the substrate designed such that there is an elongated channel with four contacts on either side. Two is source and drain with a large channel connecting to a bond pad while the rest are voltage probes set up in a formation such that the longitudinal and transverse voltages can be measured on either side of the elongation. In the middle of the channel gate electrodes are deposited connected to two large bond pads. Two of the voltage probes are located closer to the middle of the channel such that the voltage drop over the gates can be measured locally. The interface in all samples was created with a-LAO/STO.

During this work three different patterning ideas were tested for realizing this base design that can be separated into two groups. The first group uses a LaSrMgO (LSM) top layer deposited on the STO substrate to protect it during lithography and chemical steps. When these are done the layer is selectively wet-etched revealing parts of the STO for a-LAO deposition. With this top layer two different lithography procedures was tested. The first was Electron Beam Lithography (EBL). EBL has a high resolution down to the nanometer scale and has been used successfully a number of

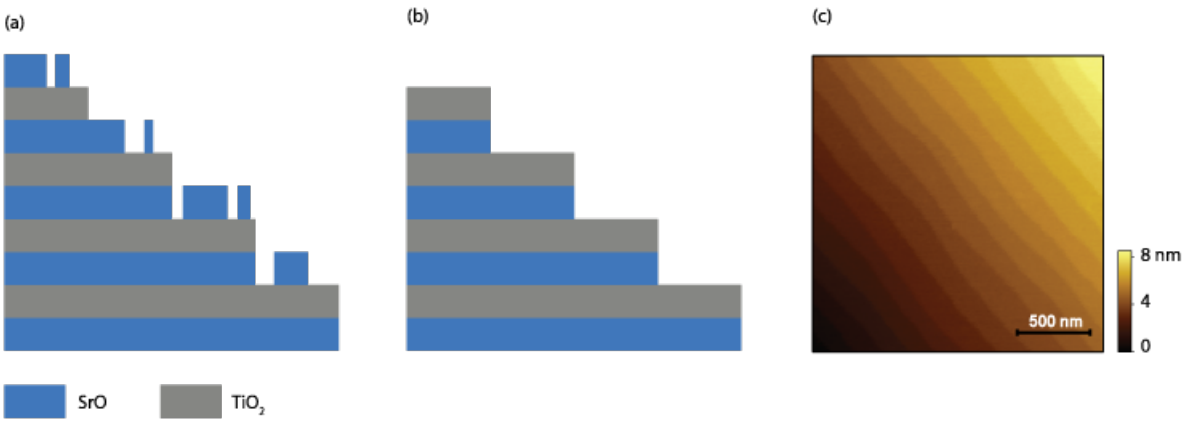

Figure 10: Schematic of the surface change during substrate treatment of $SrTiO_3$. (a) The untreated substrate. The terrace structure is visible in this visualization and additional SrO islands can be seen in profile. (b) Structure after substrate cleaning and etching in aqua regia. The terrace structure is clearly visible. Each step should correspond to an integer value of the unit cell. (c) AFM image of a sample following treatment. Several of the terraces are visible.

times on LAO/STO[6, 27]. A full EBL exposure is however quite time consuming. To improve on this photo lithography was implemented into the lithography step. Photo lithography has a lower resolution down to about 1 μm[28] so it can only be used to define large structures. For the devices created in this work that is however more than enough to pattern everything except the side-gates that still have to be made with EBL. In this work devices made only with EBL and devices with photo lithography implemented was fabricated and measured.

The second group omits the LSM top layer entirely and uses PMMA resist exposed with EBL as a hard mask directly on the STO substrate with side-gates made out of the 2DEG itself. Prior studies have observed that a-LAO/STO substrates stay insulating if the surface have been in contact with resist. In this study a surface treatment step will be implemented after the lithography to remove any residue left in the exposed areas.

2.3 Substrate treatment

The base $SrTiO_3$ substrates are 5x5 mm and are obtained from CrysTech. The substrates are cut with an angle of 0.5° to the [001] plane such that a terrace structure appears at the surface with steps of 4 Å, the unit cell height. The first procedure with the STO substrate is to chemically treat it such that the surface is TiO_2-terminated, see fig. 10. The substrate is first cleaned by sonication in Ethanol and Acetone. This is followed by sonication in MQ water for 20 minutes during which Sr-hydroxide complexes (Sr-OH) are formed at the surface. These are removed by a chemical etch in an acid solution of HCl, HNO_3 and H_2O - 3:1:16 (HCl(37%):HNO_3(66%):H_2O) commonly known as Aqua Regia. The substrate is then cleaned for leftover acid by sonication in MQ water for 30 seconds. The substrate is then annealed in an oven at 1000°C. To avoid breaking the samples the oven increases its temperature by 100°C per hour until it reaches maximum temperature. Then it

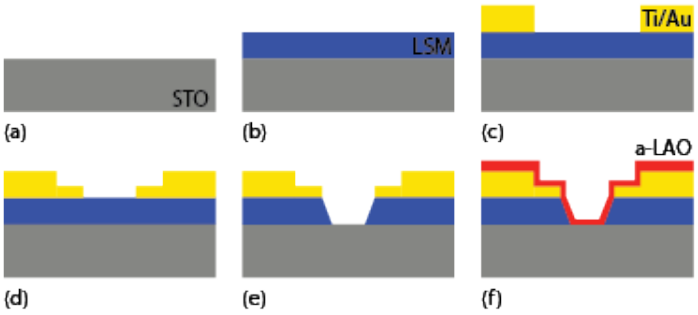

Figure 11: Schematic of the full fabrication using photo lithography. (a) The procedure starts with a TiO_2 terminated $SrTiO_3$ substrate. (b) LSM is deposited on the surface using PLD. (c) Large scale titanium-gold structures are patterned and deposited using photo lithography. (d) Smaller metal structures are patterned and deposited using EBL. (e) The etch mask is exposed using photo lithography and the LSM layer is etched. (f) a-LAO deposition using PLD.

sits at this temperature for 1 hour and then cools down similarly. The entire process takes about 24 hours. During the annealing a small amount of oxygen is fed into the system. After this the substrate is measured in an AFM. Here the terrace structure of the surface can be observed indicating that the treatment was successful, see fig. 10.(c) for an example.

2.4 Deposition of the protective top layer

Following substrate treatment some samples had a protective top layer deposited. The material used in this work is LaSrMgO (LSM). This material has some properties that makes it an excellent top layer. The primary one is that the LAO/LSM/STO interface will stay insulating independently of temperature and oxygen pressure during growth. It can be selectively wet etched with a diluted acid solution of 1:1:37 HCl(37%):KI(2mol):H_2O without destroying the STO surface. It is therefore possible to define which areas of the STO substrate that will become conductive after the lithography have been completed.

The deposition was carried out at Risø labs, DTU, using Pulsed Laser Deposition (PLD). Here a high energy laser strikes a target in bursts releasing material that is transferred to a substrate. Integrated RHEED allows for in-situ measurements of the forming of atomic planes. The LSM films are grown at room temperature and thus lack the necessary energy needed to become crystaline. Since the amorphous film does not create planes the RHEED detector was not used during these growths. A film of 45 nm was deposited, the exact height was determined by AFM on a etched part of the sample later.

2.5 Fabrication with photo lithography

The full lithographic procedure including photo lithography went as follows

1. Photo lithographic step exposing large Ti/Au structures followed by metal deposition and lift off.

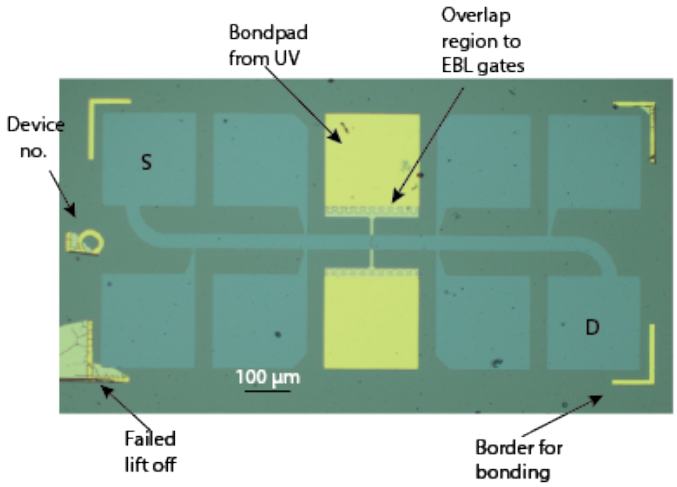

Figure 12: Optical microscopy image of a side-gated Hall bar patterned with UV and EBL. First the gold borders and bond pads are exposed and deposited using UV lithography. Then the nano sized gates are patterned overlapping with the previous layer. Finally the Hall bar is etched into a UV resist mask.

2. EBL exposing Ti/Au side-gates followed by metal deposition and lift off.
3. Photo lithography exposing the Hall bar etch-mask followed by etching.

This section will focus on step 1 and 3. Explanation of the EBL step will follow in the next section. The full procedure including photo lithography can be seen in fig. 11.

Photo lithography is a process used to fabricate micro structures on substrate wafers or chips. Light is emitted onto a substrate which has been surface coated with a dense, plastic based, chemical known as resist. Light can be emitted through a solid mask that defines the micro structures or it can be locally exposed to the sample effectively drawing the design. The latter is used in this work. When the resist has been exposed to light either the exposed areas or unexposed areas can be removed with a chemical solution, called a developer. The remaining resist can now act as a mask of the design which can be etched or deposited with a layer of metal. The resist coating can be completely removed with N-Methyl-2-Pyrrolidone (NMP).

The exposures were done with a Heidelberg uPG 501 LED-writer at UCPH. The LED-writer allows for definition of an exposure time, comparable to an intensity parameter, and a defocus value. All fabrications used 18 ms exposure time and -2 defocus in this work. The sample is held on to a plate using vacuum inside a chamber with ambient pressure. The machine can hold samples of sizes ranging from 6 inch wafers down to 4x4 mm chips. Focusing of the system was done using pressurized air, which is a convenient option as the LSM/STO chips are transparent. With the sample held in the LED writer the design file can be converted to the machine format and then exposed. The top rate for exposing with this system is 44 mm^2/s though it is highly subjected to patterning parameters such as the resist thickness.

Prior to the step 1 exposure two layers of photo resist was spun on the substrate. The bottom layer was L0R3B and the top layer AZ1505. Both layers were spun at 4000 RPM for 1 minute with 5

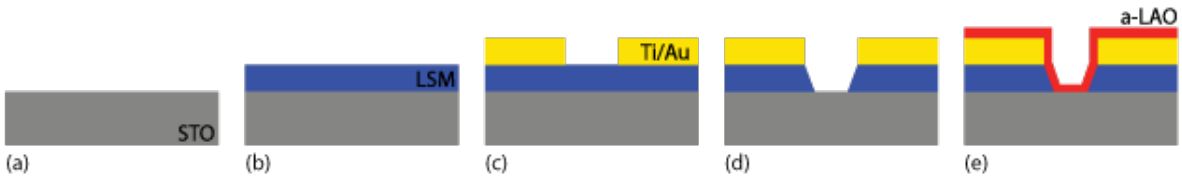

Figure 13: Schematic of the full fabrication using EBL. (a) The STO substrate is TiO_2 using the chemical procedure. (b) LSM is deposited using PLD. (c) All metal structures are defined in one step using EBL followed by metal deposition and lift off. (d) The etch mask is exposed using EBL and etched. (e) Deposition of a-LAO using PLD.

seconds of wind up time. The AZ1505 layer was hard baked at 115°C while the L0R3B layer was baked at 185°C both for 1 minute. The two layers of resist are designed to create a space around the evaporated metal that will help with the lift off process later. Two layers of resist was used throughout the project when exposing layers for metal evaporation. Prior to step 3 only a single layer of AZ1505 was exposed on the substrate. After the exposure the substrate was developed by stirring the substrate slowly 1 minute in AZ developer and 1 minute in MQ water. Exposure of the largest designs took approximately 20 minutes from loading to unloading.

The large structures exposed in step one were 200x200 μm bonding pads, alignment crosses taking up a 50x50 μm area with 10 μm wide arms positioned in the four corners of the substrate, 10 μm wide border lines around the Hall bars for easier bonding and a sample ID stamp at the top, see fig 12. The bonding pads were designed such that spiked gold arms reached out in the direction where side-gates would be exposed later. The arms increase the area of contact when depositing the next layer of gold which should help join the two layers properly together. One chip contained 12 Hall bars 6 of these with Ti/Au side-gates and 6 left with increased space such that top gates could be placed later.

Prior to metal deposition samples would first be put into a plasma asher. Here an oxygen plasma is applied on the surface of the chip which effectively burns the resist into ash which is pumped away. Ashing was done for 1 minute which should clean the developed areas from any left over resist while not burning away too much of the covered areas.

After ashing the substrate was placed in a metal evaporation system from AJA international. Here metal was evaporated onto the sample using electron-beam evaporation under high vacuum, ~ 10^{-8} bar. For the LED defined structures 20 nm of titanium was evaporated first, to act as a sticking layer, and then 130 nm gold on top. This was done at a rate of 1 Å/s measured by the system using a piezo crystal. This is followed by a lift off process by substrate submersion in 85°C NMP for 1 hour. After that time has passed the success of the lift off can be determined in an optical microscope. The sample must however be kept as the lift off process will end if the resist dries. If the liftoff was unsuccessful the sample can be submerged for another 30 minutes in new NMP. If unwanted gold continues to stick to the sample it can be sonicated in a ultrasonic bath. The effect of sonication on the sample is not known so it is preferably avoided. Lift off dealing with LED defined structures did prove difficult in about 2/3's of the samples made and these were sonicated submerged in acetone which in all cases removed all unwanted gold.

2.6 Fabrication with EBL

E-beam lithography greatly resembles photo lithography, see fig. 13. Here a beam of electrons are focused using a series of electrostatic or magnetic lenses onto the substrate which have been coated in e-beam resist. Using the beam of electrons structures can be patterned on the substrate with feature sizes down to 10's of nano meters. Similarly the resist can now be developed and the nano structures etched or filled with metal. E-beam resist is also removed from the substrate using NMP.

The EBL steps were carried out in an Elionix system with acceleration voltage of 100 kV. The substrate is positioned on a stage and kept in place using a small pin. The exposures are conducted under high vacuum below $3 \cdot 10^{-10}$ bar. A very important effect that needs to accounted for is beam widening of the electron beam due to electron scattering in the resist and substrate material. These can be accounted for by using a software program called Beamer. Beamer can reduce the dose time, equivalent to the intensity of the beam, of a pattern based on the material and resist. STO/LSM is not one of the material options so for this work the program was executed with a 100 nm resist on sillicon setting which gives good results. The program also splits the design into write fields that are exposed one at a time. In this work 300 μm write fields was used for all parts of the design except the bond pads which were done with 600 μm write fields. Similarly a beam current of 1 nA was used for all structures except the bond pads which were exposed with 40 nA. An exposure of a full chip (~ 12 Hall bars) takes about 2 hours.

Exposure of metal structures were done with two layers of resist. First a co-polymer, EL6, and then A2 both spun coated at 4000 RPM with 5 seconds wind up time and post baked at 185°C. Since both STO and STO/LSM are insulators the electron beam will build up surface charge which will distort the exposure due to beam deflection. This can be resolved by spin coating of a conductive polymer (or an espacer) onto the resist stack that will function as a discharge layer. The espacer used here is called SX-AR-PC. The espacer is water solvable therefore it can be removed as the first step of development by stirring in MQ water for 1 minute. Then the e-beam resist is developed by stirring in a mix of 1:3 Methyl-Isobutyl-Ketone and Isopropanol (MIBK:IPA) followed by 5 seconds in one IPA batch and then 20 seconds more in another IPA batch to ensure the resist doesn't reapply inside the IPA.

Hall bar etch masks were exposed with a single layer of A4 and the single step EBL directly on STO was exposed on a single layer of A2. A2 is chosen for the single step as it is the thinnest layer with a height of ~ 100 nm[29]. If the resist stack is too high the LAO might not be able to reach the surface during growth. A4 is about 200 nm and is chosen to ensure cover of the STO/LSM surface during the etching step.

Metal deposition was carried out as explained earlier. After EBL 5 nm of Ti was deposited followed by 45 nm of Au. When depositing on top of the LED defined layer the deposition was carried out at an angle of 30° with slow rotation of the sample. This way the metal layers covered the existing metal structures better ensuring good contact between the layers.

2.7 Etching

After the etch masks have been developed following the last lithographic steps the revealed LSM topl ayer is etched away. As stated it can be etched by submersion in a mix of KI, HCl and H_2O. For the 45 nm layer of LSM that were deposited on the samples an etching time of 30 seconds was

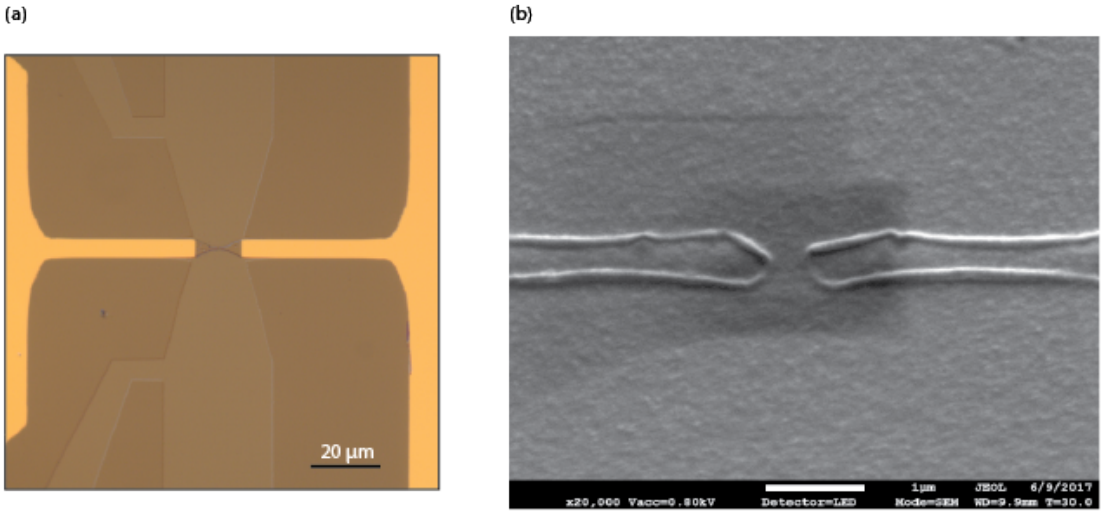

Figure 14: Device images after etching with KI:HCl. (a) Optical microscopy image taken after etching of the Hall bar. The prism build into the microscope was used resulting in the depth effect and color. Where the metal has been exposed to the etch it has changed color because it is no longer gold but the thin titanium sticking layer that remains. (b) Scanning electron microscopy image of a split-gate after etching. Note it is not the same device as in (a). After etching the gates look deformed yet they still retain the desired overall shape.

found to etch away the LSM with little over-etching. This etching time was discovered by Ricci Erlandsen and Rasmus Tindahl. The success of the etch was determined by AFM images of the underlying terrace structure of the STO. An etched device can been seen in fig. 14. As can be seen there is a change in color of the gold side-gates that was revealed during the etching. At first it was believed to be nothing, perhaps some optical phenomenon generated by the STO. Later it was discovered that the LSM etch used is also a great gold etchant. Gold and iodine can form a bond as seen below

$$2\ \mathrm{Au} + \mathrm{I_2} \rightarrow 2\ \mathrm{AuI}$$

This reaction is easier diluted in the mix when KI is also present[30]. The etching rate of gold in this mix is 1 μm/min. This means that when the LSM is etched away after 30 seconds, the 45 nm of Au has completely vanished along with it.

Due to this discovery some changes were made and tests were carried out. First all samples with gold gates made after this discovery had a reduced Hall bar channel around the gates. It was narrowed in from 30 μm to 10 μm in the first implementation and then further down to 3 μm in the last implementation. Tests were carried out to find an alternative etchant of the LSM. Previous studies have used both buffered Hydroflouric (HF) acid and concentrated HCl as etchants on oxides[31]. Neither of these etch gold but they do however both etch titanium. It was speculated that it might be possible to find an etch time that would remove the LSM without removing the titanium or maybe leave the gold in place despite some Ti removal. Buffered HF left almost no noticeable change after 1 minute when analyzed with an optical microscope. Concentrated HCl was much more promising, over etching the LSM layer remarkably after 1 minute. To test HCl further etch-tests were carried

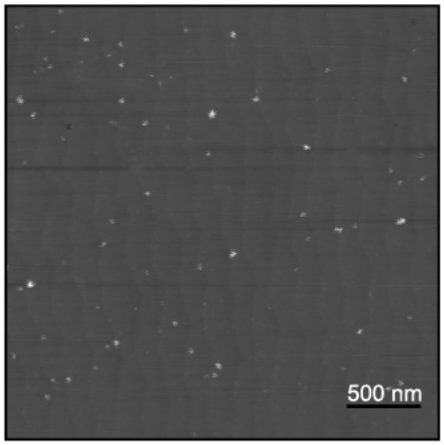

Figure 15: AFM image of the STO surface revealed by etching. Several particles are present on the sample identified as dirt or Sr. Terraces are present in this picture but due to the scale they are very hard to see.

out with concentrated and water diluted mixes. While the HCl did continue to etch the surface it did also destroy Ti/Au structures which was tested on alignment marks. AFM images of the etched areas did not reveal any terrace structure which might be an indication that the HCl also etches the surface to some degree. Ultimately as a final test Ti gates were deposited on one sample that was then etched by the KI/HCl/H_2O etchant. The echtant did not damage the Ti in any observable way in an optical microscope. A thin film or patches did however form on the Ti which is assumed to be TiO. Three devices with Ti gates were fabricated.

2.8 Cleaning of the STO surface

After etching of the LSM layer or development of PMMA resist AFM images as seen in fig. 15 was achieved. As can be seen small particles have formed at the surface of the STO and since the terrace structure is checked prior to fabrication they must be formed after this. This would mean that they are either formed as a by-product of one of the patterning steps or that they develop over time. J. G. Connel *et. al.*[32] discovered a similar formation in their work which they explain as diffusion of Sr towards the surface over time. They remove the particles by treating the substrate in DI-water and annealing them which they reported not only removed the particles but that they had not returned after a period of 60 days.

For this work an adaptation of this treatment is used. When the STO surface was revealed, either through LSM or PMMA, the samples were first plasma ashed for 2 minutes, which has been calibrated to remove 10 nm of A2 PMMA resist. Following the plasma ashing the substrate was cleaned in MQ-water, by stirring in a beaker for 2 minutes followed by a rinse in IPA, which has the benefit of not dissolving the PMMA resist. This treatment did not remove all particles universally, but it drastically reduced the amount.

Following the cleaning of the surface the samples were transported to Risø where 12 nm a-LAO

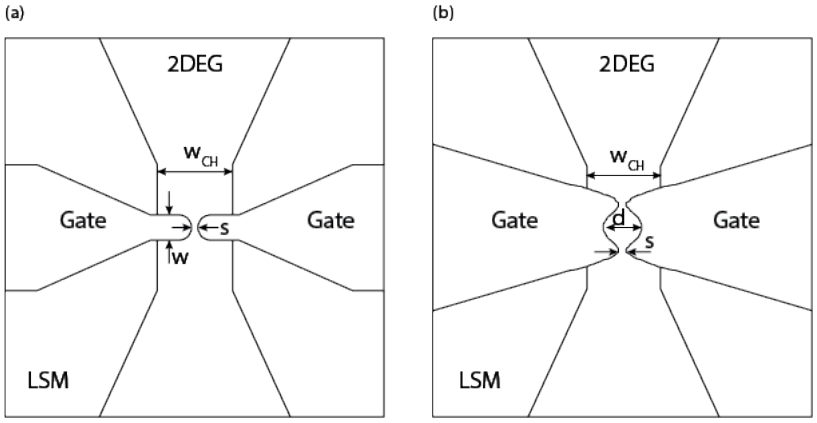

Figure 16: Schematic drawing of the two main devices patterned on the LSM samples. The figures are not to scale. (a) The QPC variant. The geometry is defined by the final gate thickness, w, the spacing between split-gates, s, and the channel width, w_{CH}. (b) The dot variant. The geometry is defined by the diameter of the center island, d, the smallest spacing between the split-gates, s, and the channel width, w_{CH}.

were deposited using PLD as with the LSM. The samples were then transported back to UCPH for transport measurements. During this work nine samples were fabricated using the above methods each carrying 12-18 devices. I was present at all steps of fabrication and treatment for seven of the samples though all PLD operation was carried out by one of the PhD students at Risø: Wei, Yu and Yulin. The final two samples was treated by either Yu or Guen, a previous PhD student. I carried out all fabrication from there on. Three of the samples were fabricated with photo and e-beam lithography on LSM, three only with EBL on LSM and 3 with EBL directly on STO. Of these 9 samples 6 were experimented on at sub-Kelvin temperatures.

3 Methods - devices and setups

The previous section described the fabrication processes and displayed the basis structure of the devices patterned on STO/LAO. In this section the geometries of the small nanoscale gates and their surrounding area will be discussed. Devices patterned on PMMA and LSM will be described separately. Following this a rundown of the measurement setup will be given including the bonding of the devices and mounting in a cryostat for sub-Kelvin measurements. See table 1 for an overview over the different samples.

3.1 Metal gated devices

Two types of side-gates were patterned on LSM/STO. The first was designed as a quantum point contact, see fig. 16.(a). Initially the gates were designed with widths, w, of 250 nm and spacings, s, of 500 nm. Following the first etch of such a pair of gates it became evident that they were too small as they broke off. The gate width was increased to 1 μm and the channel width, w_{CH}, was reduced

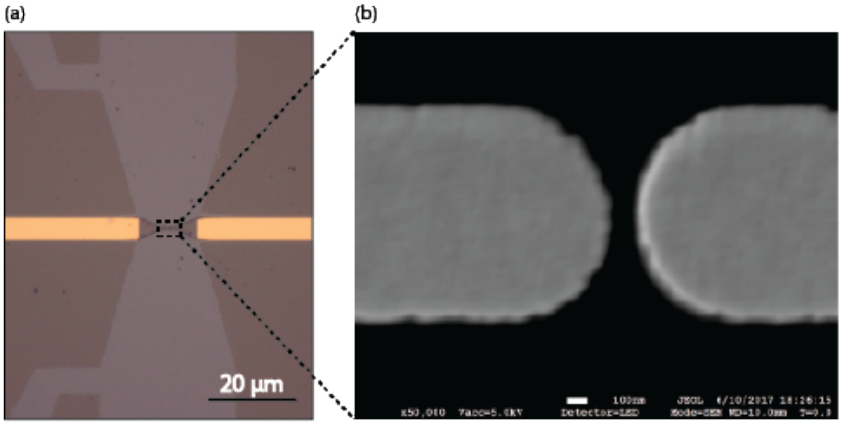

Figure 17: SEM image of metal structures on $SrTiO_3$. (a) Optical microscopy with the largest magnification of a split-gate. It is barely visible that the two gates have a gap in between. Dashed line outline the zoomed area in (b). (b) SEM image of split-gate device taken without a spin coated espacer prior to etching. The gap between the two side-gates are ~ 100 nm which is what it was designed to be.

from 30 μm to 10 μm locally at the side-gates to reduce the etched area of the gate. After these changes none of the gates broke off. The channel width was further reduced to 3 μm later to improve device performance. This channel width reduction was done for all devices on the samples. Devices of this type was made with spacing's varying from 50 nm to 250 nm. The second type of side-gates was a slight modification to the standard QPC, see fig. 16.(b). The gate has been stretched out in two places creating an island in the middle. This way the side-gates are closer where they are supposed to close off normal transport, such that the device geometry itself helps form the tunnel barrier, and a quantum dot can form inside the island. All devices of this type was made with a spacing of 100 nm while the diameter was either 500 nm or 250 nm.

A design of a full LSM sample can be seen in fig. 18. The sample is outlined by alignment marks that allow for fine alignment using both EBL and UV lithography. Inside 12 Hall bars are placed in a grid in this example nine of them are side-gated though this number varies, see table1. At the very top a identification mark has been printed in metal. This eliminates any possible mix up of samples. Devices have similarly been labeled in metal to simplify the bonding of the sample. To properly measure that the lithography of the small split-gates have been successful, optical microscopy simply cannot be used as it has to low resolution. The gates have therefore been pictured using a JEOL 7800F Scanning Electron Microscope (SEM), see fig. 17. The SEM functions like the Elionix EBL machine only instead of having a moving stage and beam blanker for resist exposure it comes with a detector that can collect scattered electrons which can be converted to a signal. As with the Elionix surface charges accumulating on the substrate will ruin the image. An espacer layer was employed here as well which resulted in good images. The espacer was however observed to burn onto the sample following imaging. Pictures can be taken without the espacer but the quality is greatly reduced. It can however be observed from the SEM pictures that was taken that the structures turn as designed prior to etching.

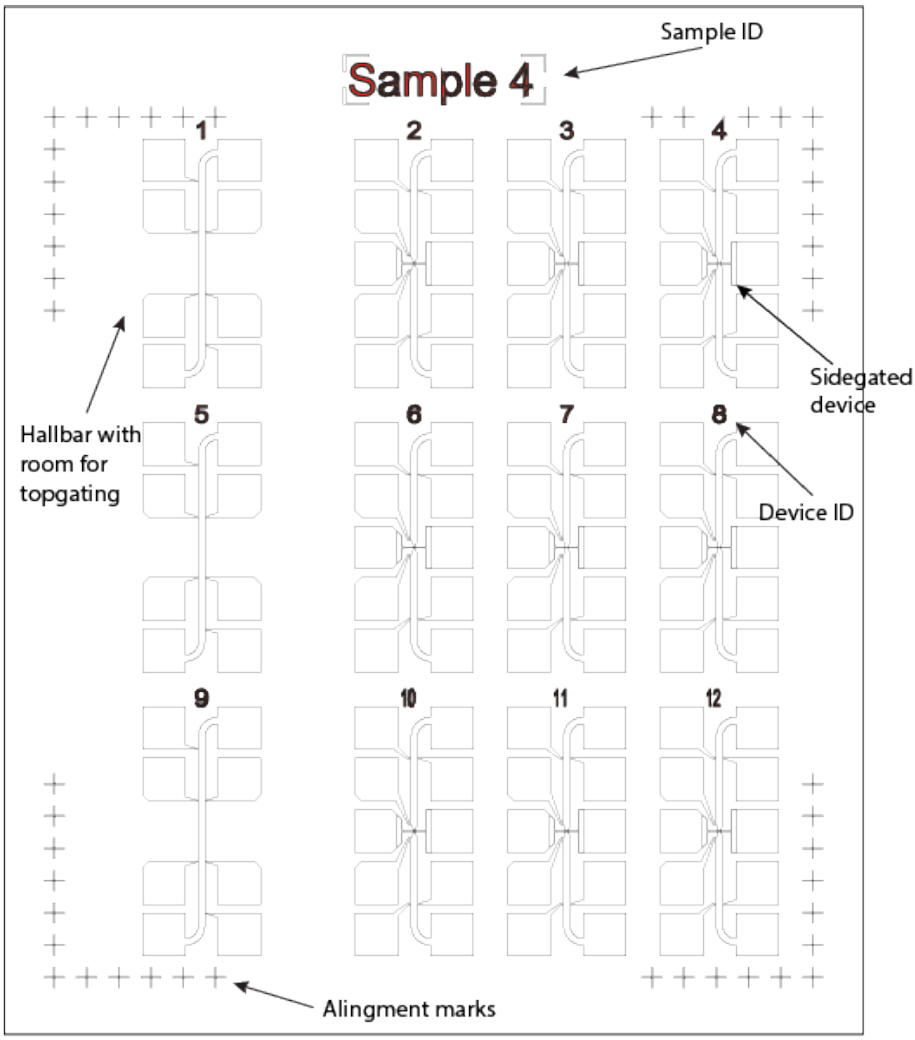

Figure 18: Overview image of sample 4. This is a design CAD file with all colors turned black. The arrows point out some of the key features on the sample.

3.2 Resist devices

To characterize the conductive ability of devices patterned on PMMA resist two devices were created. The first was two 200x200 μm bond pads connected by five parallel wires, see fig. 19.(a). The wires are 5 μm wide and 100 μm long. At the center of the wire a 5 μm long part of the wire is narrowed in. With such a device it can be determined if the 2DEG even emerges and by varying the thickness it can be determined if the conductance is defined by the PMMA structures. Several wires are placed in parallel to avoid any variance from the individual wire. Five of these devices were created and as a group they will be referred to as the wire series. Besides creating structures that actually conduct it

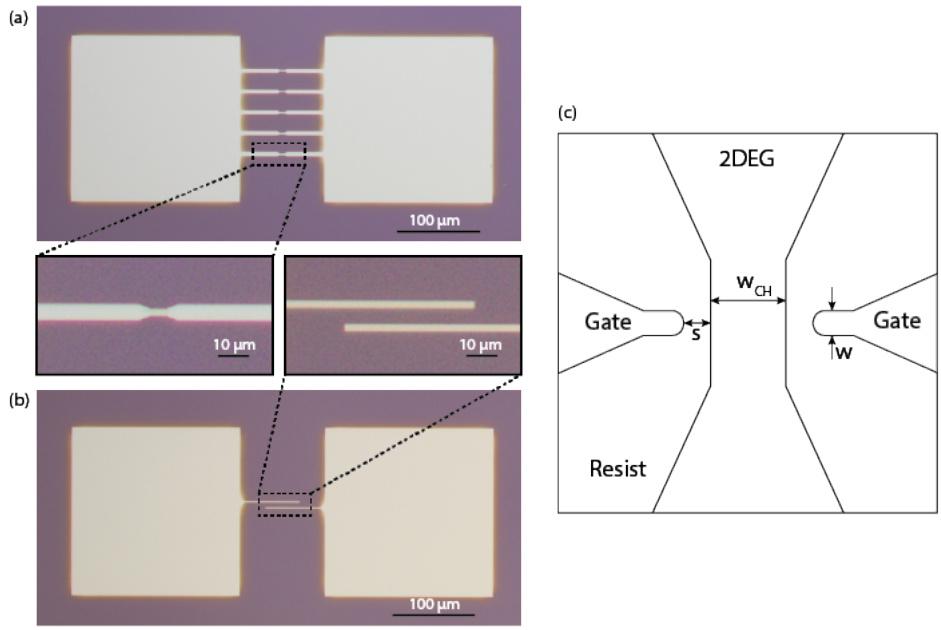

Figure 19: Devices patterned on with PMMA on $LaAlO_3/SrTiO_3$. (a) Optical microscope image of the wire series. The wires narrow in from 5 μm to 2 μm in the center which can be seen in the cutout marked by the dash line. (b) Optical microscopy image of the leak series. The 2μm wires are spaced 5 μm apart. (c) Schematic of the split-gate devices designed for the PMMA samples.

is also crucial to determine how close structures can be placed to each other without leaking to each other. To measure this a device was created of two 200x200 μm bond pads with a wire extending from the center, see fig. 19.(b). The wires are 2 μm wide and 60 μm long and have been placed with an offset compared to each other such that they run in parallel over a 40 μm range. By varying the offset between the wires the leak between structures can be studied. Five of these devices were created and they are named the leak series. The width in the wire series and the spacing in the leak series was tested with the same parameters: 5,2,1,0.5 and 0.25 μm .

To test the ability for PMMA devices to function in a side-gate setup such devices was created, see fig. 19.(c). The setup is very similar to the QPC device on LSM yet the gates have to be created outside of the Hall bar channel such that the geometry is now defined by the spacing between channel and side-gates, still denoted s. In the initial round of fabrication three devices of this type were fabricated where the design parameters were kept equal at 100 nm, 300 nm and 500 nm. The next generation kept the channel width at 100 nm, the gate width at 200 nm and varied the spacing. Lithography was greatly improved between the two generations which opened up the way to test some prototypes of more advanced devices. These waere ring structures that could show interference effects and dot structures with three sets of split-gates, two sets for pinching off the 2DEG and one set working as a plunger gate, see fig. 20. The ring structure was made in two versions with two different diameters of the circle, 100 nm and 150 nm. The width of the side-gate was kept at 1 μm and the distance between ring and side-gate was kept at 200 nm. The parameters for the advanced

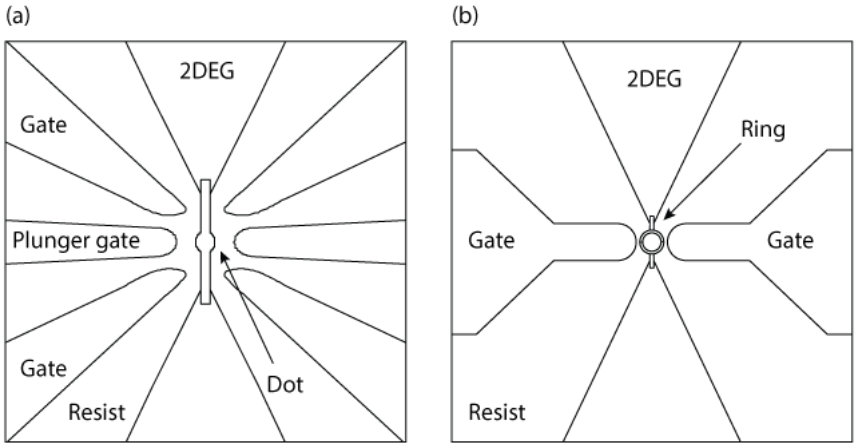

Figure 20: Schematics of advanced devices patterned with PMMA. (a) Schematic of the six-gate dot structure. Figure is not to scale. (b) Schematic of the gated ring structure. Figure is not to scale.

dot were more varied. Gate widths were kept at ~ 100 nm while distances in between the gates and the dots were changed between 100 nm and 200 nm. The dot and ring Hall bar channels were kept at 100 nm with the dot increasing to 150 nm in the middle. The layout of the PMMA samples greatly resembles that of fig. 18 only there are no alignment marks as no alignment will ever be done on these samples. The success of the lithography of these samples was not checked using SEM but instead AFM was incorporated after development of the resist.

Sample no.	Type	Lith.	Hall bars	QPC's	Dots	Top gates	Rings
1	LSM	EBL/UV	6	5	1	-	-
2	LSM	EBL/UV	-	5	1	-	-
3	LSM	EBL	6	4	2	-	-
4	LSM	EBL	4	2	-	-	-
5	PMMA	EBL	4	3	1	-	-
6	LSM	EBL	2	4	2	3	-
7	PMMA	EBL	1	5	4	-	2
8	PMMA	EBL	1	5	4	-	2
9	LSM	EBL	-	7	5	-	-

Table 1: Full description of all the samples made in this work. Samples were named in chronological order of creation. While all samples of course contain plenty of Hall bars the number cited here under the "Hall bars" tab is Hall bars left free, either for hall measurements or for potential top gating.

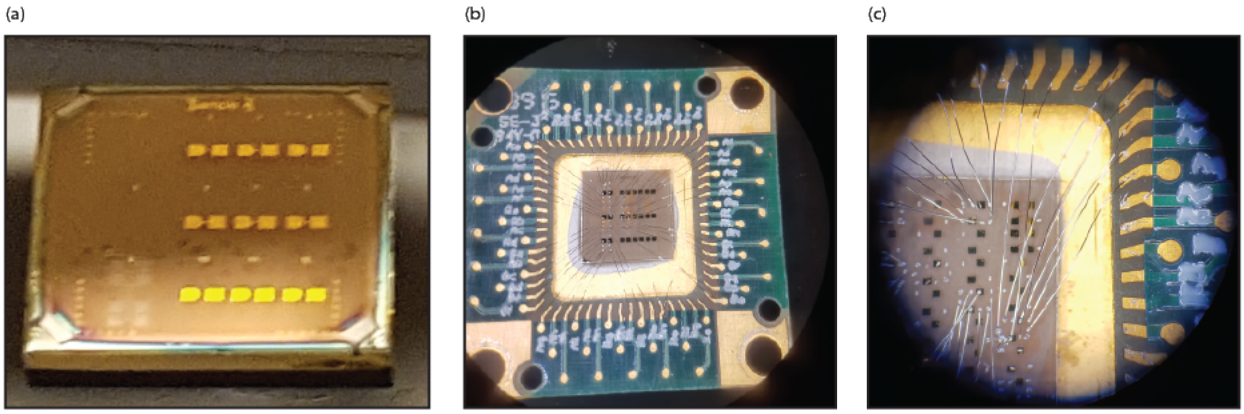

Figure 21: Bonding of the $LaAlO_3/SrTiO_3$ samples. (a) Picture taken of a LSM sample. The gold pads and one of the etched Hall bars can be seen. The edges clearly show that this sample is covered in resist. (b) A sample glued into the chip carrier with silver paint and bonded to the carrier using aluminum wires. (c) Close up of the bonded wire (different sample than (b)).

3.3 Device bonding

The finished samples were glued into a Qdev daughter board using a conductive silver paint, see fig. 21. Other than as a binding agent the silver paint also function as an electrostatic back gate to the sample used in several of the experiments. The bonder used was a FS autobonder using 25 μm diameter aluminum wires bonded to the sample using ultrasound. The setup conveniently has an optical microscope attached that is able to resolve structures like the etched Hall bars that would otherwise be very hard to see as the material is transparent. The sample were attached onto a plate that comes with a heater. During the bonding the samples were held at 50°C to improve bonding quality. The sample board allowed for 48 individual lines to be bonded at once equal to four fully bonded side-gated Hall bar devices. Generally the bonds were made as close to the probe arms as possible. After bonding the sample was mounted into a puck, see fig. 22. The puck is effectively a wired copper cage with a shield around it. The wires used for measurements run through the cryostat into the sample inside the puck. Outside the wires are hooked up to a breakout box.

3.4 Dilution fridge

The bulk of measurements carried out in this work was done in a Oxford triton ^{3}He -^{4}He dilution refrigerator (or cryostat) setup with a mercury IPS vector magnet that allows for the independent control of the field with the maximum field strengths [1T,1T,6T]. The system can be cooled to about 11 mK. The cryostat is a highly engineered piece of equipment yet some building blocks can be identified that underlines the basic idea, see fig. 23. Placed at the top of the fridge are two ^{4}He bath continuously cooled by a pulsed tube cooler to 4.2 K and 1.5 K respectively[33]. These baths are thermally connected to the pre-cool loop inside the cryostat. When the cryostat is at room temperature ^{3}He -^{4}He mix is cycled through the pre-cool loop which will cool the system until the mixing chamber at the bottom of the fridge drops to 10 K after which the pre-cool loop is evacuated

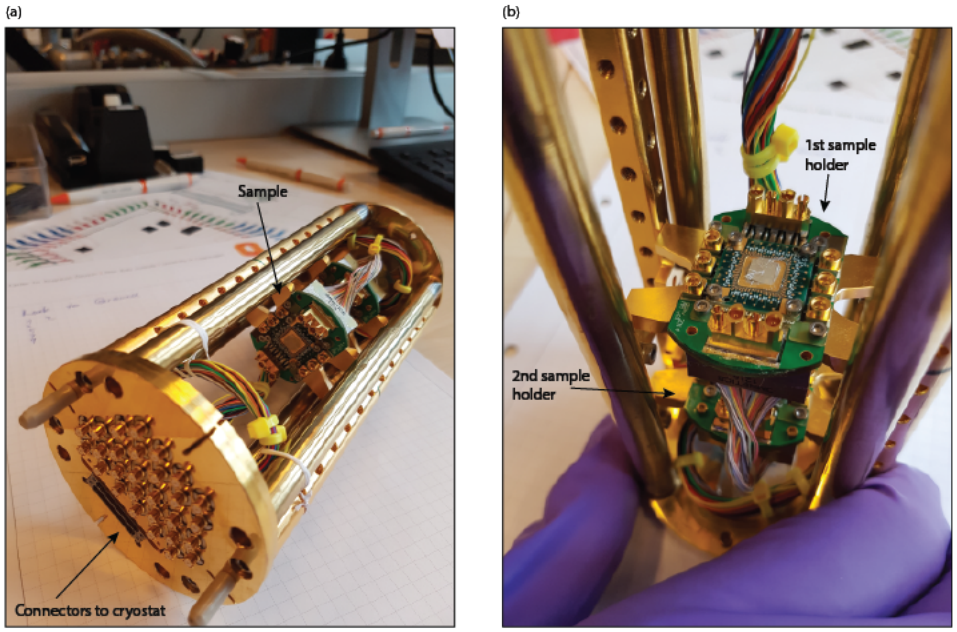

Figure 22: Images of the puck used to mount the sample into the cryostat. (a) Side view of the puck. The connectors that run into the cryostat have been outlined. (b) Top view of the puck. Two sample holders are mounted into the puck allowing for two samples to be measured at the same time.

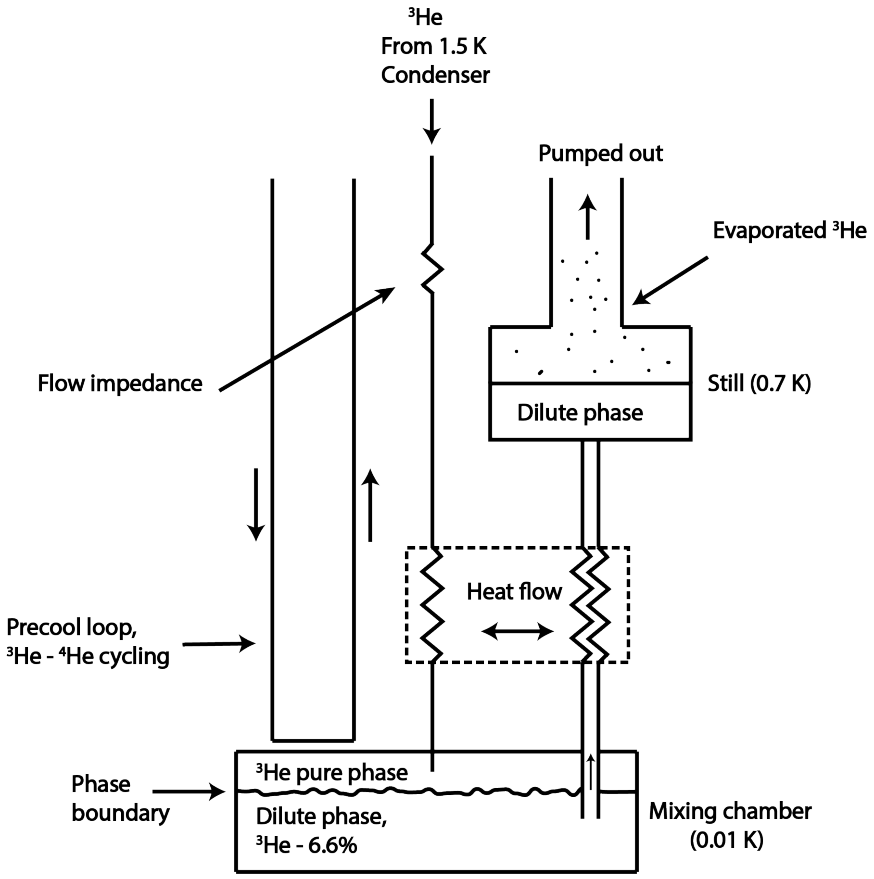

Figure 23: Schematic view of the ^{3}He - ^{4}He dilution refrigerator. The precool loop on the right cool the system down by cycling of helium mix coonected to a pulse tube cooler (not shown). The helium condenses in the mixing chamber at the bottom of the cryostat. Evaporation of ^{3}He in the still forces ^{3}He to mix with ^{4}He requiring energy taken from the surroundings resulting in cooling. The evaporated ^{3}He is cycled back into the cryostat.

with a turbo-pump.

To cool further the ^{3}He -^{4}He mix is cooled to 1.5 K and pressurized by a condenser and is then transported down through the main flow line. On the way it moves through a series of of impedance that increases the pressure and cools the mix further. Heat exchangers allows the mix leaving the cryostat to further cool the mix entering it. At the bottom, in a chamber called the mixing chamber, the mix condenses into a liquid with two different phases. On the top is the pure ^{3}He while the diluted mix of ^{4}He with 6.6% ^{3}He lays on the bottom. The diluted phase is connected to a still. In the still ^{3}He evaporates forcing ^{3}He in the pure phase in the mixing chamber to cross the phase boundary which draws energy from the environment. The evaporated ^{3}He are recycled into the cryostat resulting in a continuous refrigeration process. The sample can be attached to the mixing chamber through the bottom of the cryostat.

4 Results and discussion - PMMA defined structures on STO

Electron beam lithography is the one of the best understood methods for patterning of nanostructures on semiconductor materials. Should it be possible to use a single step lithographic process directly on the $SrTiO_3$ surface the way would be opened for implementation of a large array of device geometries known from semiconductor studies. In this section the results generated from PMMA devices made with EBL will be reviewed and discussed. The experiments were done in three rounds. Initially measurements were done on the leak and conductive wire series on sample 5 discussed in section 3.2 at room and sub-Kelvin temperatures. Split-gate devices and Hall bars were measured at sub-Kelvin temperatures and also side and back gate dependence were investigated.

4.1 Leak and conductive wire series

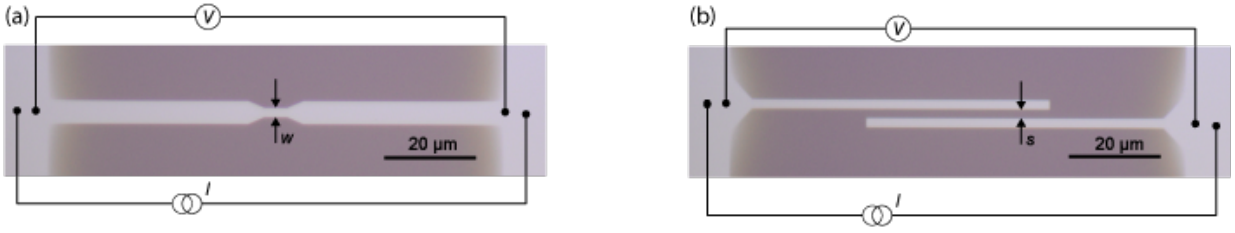

Figure 24: Measurement setups for leak and wire series displayed with the 1 μm devices. (a) The wire series are wired into a 4-point setup were the voltage is measured between the inner probes and the current between the outer. The varied variable is the width, w, of the center stretch of the wires. (b) similar setup as (a) only for the wire series. Here the varied variable is the spacing, s, between the wires.

The leak and wire series were measured in a 4-point setup as seen in fig. 24. At room temperature a voltage was sourced using a National Instruments Data Acquisition Card (daq) which has a range of ± 10 V output. The voltage was sourced through a 10 MΩ series resistor to the device.

The current was measured with an Ithaco-preamp that converts the signal from current to voltage with a variable scale, here set to $10^{-8}A/V$ as the current signal was in the nA range. The output was connected to an input channel on the daq that recorded the signal. The 4-point voltage signal was connected to a Stanford SR560 voltage amplifier that amplifies the voltage signal for measurement by the daq. A gain of 2 was used for these measurements.

When sweeping the source-drain voltage on the leak series, two different types of IV curves were measured, see fig. 25 (a). The two devices with the smallest spacings (500 nm and 250 nm) are non-conductive at low bias voltage as expected yet as bias voltage is increased the current start increasing in a non-linear fashion. The smallest spaced device displayed a non-linear current increase outside the bias voltage range [-2.35V, 2.4V] defined as the point where the current hits 1 nA. The data from the 500 nm spaced device is not shown due to an overload error in the voltage amplifier though the behavior can be inferred from the current measurements. The 5 μm ,2 μm and 1 μm all stayed non-conductive within the daq voltage limit.

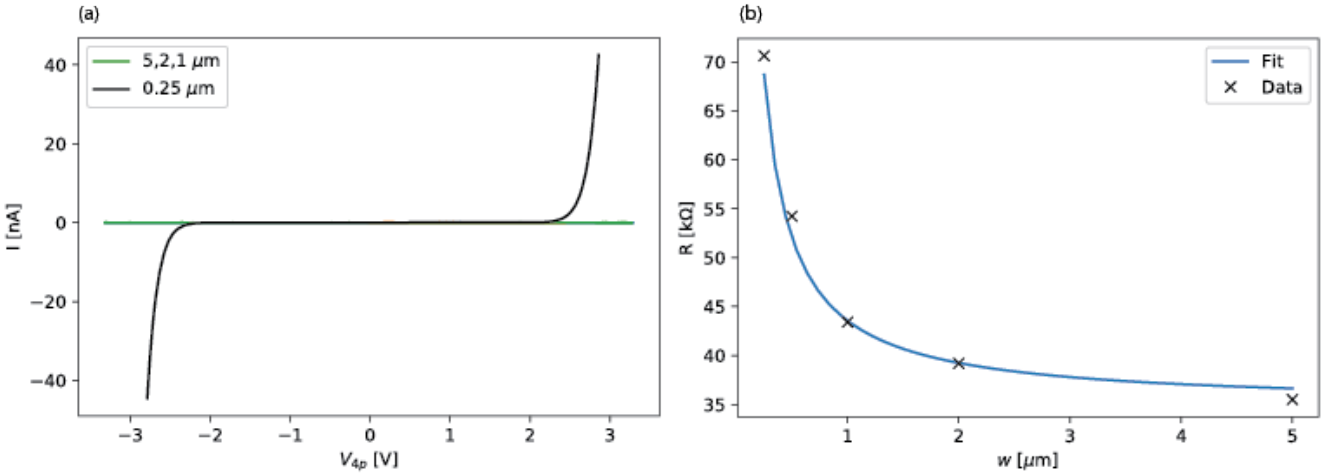

Figure 25: Results from the room temperature measurements of the leak and wire series. (a) IV curves resulting the different leak devices. The device with the smallest spacing start to at certain points in 4-point voltage. The rest of the devices follow the flat line. The 500 nm also displayed leaking but it is not shown here due to an overload error. (b) Resulting resistances from each wire device. The blue line is a fit to the data following the model of equation 11.

The conductive wire series was measured in a similar fashion revealing linear IV curves for all wire widths from which the resistance of the wire can be fitted. All the wires are conductive and it is observed that resistance increases with reduced wire width. The resistances show a $R \propto \frac{1}{w}$, see fig. 25.(b).

By analyzing this data it will be possible to determine if there is any deviation in the size of the 2DEG compared to the defined window in the PMMA. This result could arise either due to oxygen diffusion under the PMMA increasing the width of the 2DEG or perhaps the LAO layer cannot properly approach the sides of the PMMA resulting in a smaller width than defined. If the diffusion extended 125 nm underneath the PMMA the smallest wire series would have been conductive from 0 bias. Instead we observe no leak and can thus assume that the diffusion is at least lower than ~ 100 nm under the PMMA. Furthermore we can fit the resistance data gathered from the wire series with a simple model. The resistance measured over the full wire should be given by the equation $R = L/W \cdot R_S$, with L and W being the width and height of the wire and R_S the sheet resistance. The wire can be split into three sections, the long wires of which there are two and the small wire that narrows in. The aspect ratio L/W is roughly 20 for the two long wires and the total resistance can be modeled as

$$R = \left(\frac{L}{w + w_0} + 20 \right) R_S \tag{11}$$

where w_0 is added as the possible extra width of the wire outside of the defined PMMA that will be used as a fit parameter. The resulting fit can be seen in fig. 25 (b). The resulting parameters are $R_S = 1.7 \pm 0.03$ kΩ/□ and $w_0 = 8 \pm 11$ nm. This value for w_0 indicates a negligible change of the

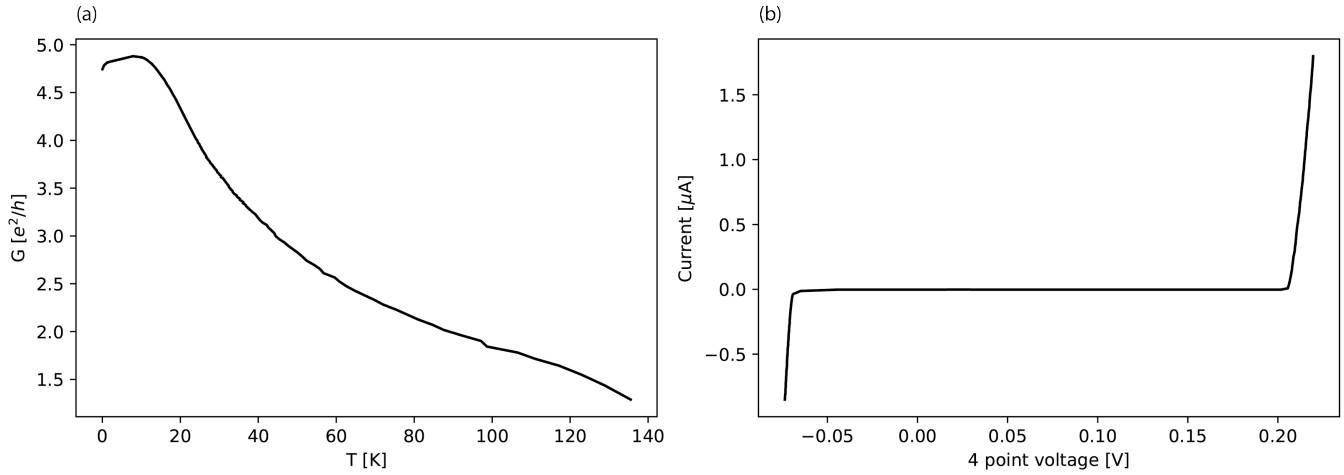

Figure 26: Low temperature measurements on the leak and wire series. (a) Cooldown profile of the 1 μm device from 135K down to ~ 16 mK. (b) IV curve from the 250 μm leak device displaying the same behavior as at room temperature.

2DEG size compared to the defined PMMA window, indeed the data can be fitted with w_0 forced to 0 resulting in a fit with almost the same values.

During cooling to ~ 16 mK the conductance of the three widest wires were measured. Instead of a daq card several Stanford SR830 lock-ins were used to measure drain current voltage. For this cooldown the lock-ins sourced a 5 V AC signal which was sourced through a 100 MΩ series resistor. The drain current is measured by a Physics Basel SP 983 preamplifier and the voltage amplified by a NF electronics voltage amplifier. In fig. 26.(a) the cooldown profile of the 1 μm wire device is plotted. As the temperature drops the conductance through the wires increase similar to the behavior observed in metals[25]. As the temperature in the samples drops the electron-phonon scattering, the interaction between electrons and lattice vibrations, drops and the conductance rises as a result. At very low temperatures the conductance will settle on a value defined by the amount of impurities present in the sample. In STO this behavior has been observed to be accompanied by a change in conductance affiliated with the dielectric constant, ϵ, and the oxygen vacancies present. It has been shown that the oxygen vacancies can function as charge traps for the electrons if the thermal energy is high enough[34]. As the temperature drops fewer of these charged impurities will exist increasing the conductance. Simultaneously the decrease in the dieletric constant will result in a lower screening of the impurities resulting in a decrease in conductance. The full picture was modeled for the sheet resistance by Fuchs *et al.*[34] as

$$R_S = A\left[1 - \exp\left(-\frac{T_A}{T}\right)\right]\left[\frac{T_1}{2}\coth\left(\frac{T_1}{2T}\right) - T_0\right]^2 + B \cdot T^2 \tag{12}$$

Here the first term has two parts. The left square bracket is the decrease of charged impurities with decreasing temperature where T_A is the activation temperature for the vacancies to function as charge traps and A is a constant. The right square bracket is the change of the dielectric constant with temperature also known as the Barret formula[35]. Together the first term accounts for changes

in resistance due to impurity scattering. The second term represents the electron-phonon scatterings, where B is a constant. Fuchs *et al.*[34] uses this model to fit cooldown data that greatly resembles the results reported in fig. 26 (a), yet the data reported here were not fitted to the model.

Cooldown profiles of this kind were measured for the three thinnest wires. At ~ 16 mK all five wire devices are conductive, see table 2. As can be seen the conductance no longer follows the same order as observed at room temperature. Instead conductance as function of wire width seem to follow some random correlation. It is possible to explain this behavior through appearance of domain structures in STO/LAO at low temperatures[36]. The formation of these domains have been shown to modify the conductance of the STO[37]. As the five wire devices were placed as a band across the middle of the sample they would be highly sensitive to conductance fluctuations across the sample. IV curves were measured on the leak series in similar fashion as at room temperature. This time all devices displayed the same behavior. At low bias the wires are non-conductive but as the bias increases the current begins to increase in a non-linear fashion. The 4-point voltage measurement suffered from an overload error from the voltage amplifier in every data sets except for the smallest spacing (250 nm). The results from this device can be seen in fig. 26.(b), its non-conductive range was [-70 mV, 220 mV]. Data of conductance and leak breakpoints can be seen in table 2. In summation the wire and leak series at room temperature showed us that separate structures with no electrical contact can be made down to 250 nm feature size. Additionally fitting of the data indicated that the 2DEG was defined by the lithography and not any other effects like oxygen diffusion. The behavior was the same at low temperatures only the ranges with no leak was reduced compared to room temperature that only displayed leak for the two devices with the smallest spacing.

Dimension	5 μm	2 μm	1 μm	0.5 μm	0.25 μm
Wire series : G $[e^2/h]$	2.75	2.89	4.75	2.93	4.11
Leak series : Non-leaking range [V]	[-,6.6]	[-4.95,4.3]	[-1.0,1.4]	[-0.49,0.51]	[-0.14,0.16]

Table 2: Table of results from sub-Kelvin measurements on wire and leak series. Note the 5 μm leak device does not have a negative leak limit denoted by a -.

4.2 Hall measurements

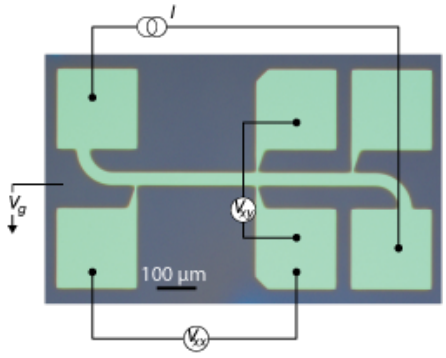

Figure 27: Hall setup for the resist devices. The Hall bar viewed originates from sample 8. Similar Hall bar structures were patterned on all the samples. The V_g connection on the side is a display of the back gate possibility.

Hall measurements were carried out on the Hall bar devices to determine n_s and μ, the sheet electron density and mobility respectively. The classical Hall effect is well understood and explains the movement of electrons in a conductor under an applied magnetic field normal to the current flow. The electrons flowing through the conductor will experience a force from the magnetic field known as the Lorentz force, $F = a(\mathbf{E} + \mathbf{v} \times \mathbf{B})$. The effective force drives the electron towards the edges of the conductor resulting in a potential difference build up across the sides of the conductor. This voltage called the transversal voltage, V_{xy}, will increase linearly with B while the longitudinal voltage,V_{xx}, is independent of B. The linear coefficient in V_{xy} is called the Hall coefficient, R_H. The measurements were done with lock-in techniques. While set up in the configuration seen in fig. 27 the perpendicular magnetic field was swept from −6 T to 6 T. The resulting measurement from sample 8 of R_{xx} and R_{xy} can be seen in fig. 28, here $R_{xx} = V_{xx}/I$ and $R_{xy} = V_{xy}/I$. Compared to the normal hall effect, there are some clear differences. Both curves show a general non-linear behavior around 0 field that becomes more linear at high field. The behavior of R_{xx} can be explained by conduction through a two-band model which has been studied by Kane et. al. [38]. The idea of a multi-band conduction model makes sense for LAO/STO devices. As have been stated in the theory section the carriers are located in the STO right below the interface in the 3 d-bands which have all been showed to add to the conduction[39]. The premise for the 2-band model stems from the drude model in a magnetic field. By solving the equation for the Lorentz force equations for the drift velocity of the electrons in the channel can be found. With the drift velocity at hand it is possible to equate this with the current density, j.

$$\vec{j} = -n_s e \vec{v} \tag{13}$$

Here n_s is the carrier density and e the electron charge. If this is solved in two dimensions it results in a 2x2 matrix filled with the conductance, σ, which equates the current density with the electric field, E.

$$\vec{j} = \begin{pmatrix} \sigma_{xx} & -\sigma_{xy} \\ \sigma_{xy} & -\sigma_{xx} \end{pmatrix} \cdot \vec{E} \tag{14}$$

where the elements of the matrix is given as

$$\sigma_{xx} = \frac{en\mu}{1 + (\mu B)^2} \tag{15}$$

$$\sigma_{xy} = \frac{en\mu^2 B}{1 + (\mu B)^2} \tag{16}$$

In the presence of two conductive bands a matrix can be built for each band and the total matrix will simply be the sum of these where we can attribute a mobility and density to each band. To find an expression for the resistivity, ρ, this matrix is inverted giving us ρ_{xy} and ρ_{xx} which can be related to the transversal and longitudinal resistance that is measured. The resulting dependence of R on B is not a simple one so directly seeing that the data presented in fig. 28 results from this model cannot be done. To make a rough statement we can look at the complete expression for ρ_{xx}

$$\rho_{xx,2-band} = \frac{en_1\mu_1(1 + B^2\mu_2^2) + en_2\mu_2(1 + B^2\mu_1^2)}{(en_1\mu_1)^2 + (en_2\mu_2)^2 + 2e^2 n_1 n_2 \mu_1 \mu_2 + (en_1 + en_2)B^2\mu_1^2\mu_2^2} \tag{17}$$

in the numerator we find a B^2 term which would result in parabolic dependence of ρ_{xx} on B which is what we observe including a shift in the slope which appears if the mobilities in the two bands differ. While this picture can explain the appearance of a change in ρ_{xx} with B there are still some problems with the ρ_{xy} data. The ρ_{xy} value at no field is not 0 which it should be even in the 2-band model. This effect is most likely a result of some slight misalignment of the voltage probes used to measure V_{xy}. This would lead to a small measurement of V_{xx} seeping into the V_{xy} measurement. Even if this is the case it is assumed that the data can be used to calculate the density and mobility. One of the result that Kane *et al.*[38] presented in their study was a simplified expression for ρ_{xy} at the high magnetic field limit

$$\rho_{xy} = \frac{1}{e(n_1 + n_2)}, \quad \text{(high field)} \tag{18}$$

here we can see that at high field limits the resistivity is simply given as the sum of the two bands. Therefore by restricting our analysis of this data to high fields (4 T and above) we can calculate the total carrier density using the much simpler equations for a 1-band model. This way we will not be able to estimate parameters for each individual band, but the simplification is significant. Additionally the R_{xx} data has an unexplained dip in resistance at 0 B-field. The fact that this dip breaks quickly as the field is increased and that $LaAlO_3/SrTiO_3$ is known to house spin-orbit coupling indicates that this effect can be explained as Weak Anti-Localization (WAL). WAL is a quantum mechanical effect connected to the interference of timereversed electron paths. Due to spin-orbit coupling this intereference becomes destructive [25]. The appearance of WAL has been reported in other experiments on LAO/STO[4]. Using the 1-band model the Hall coefficient can be found by fitting the V_{xy} data with the equation

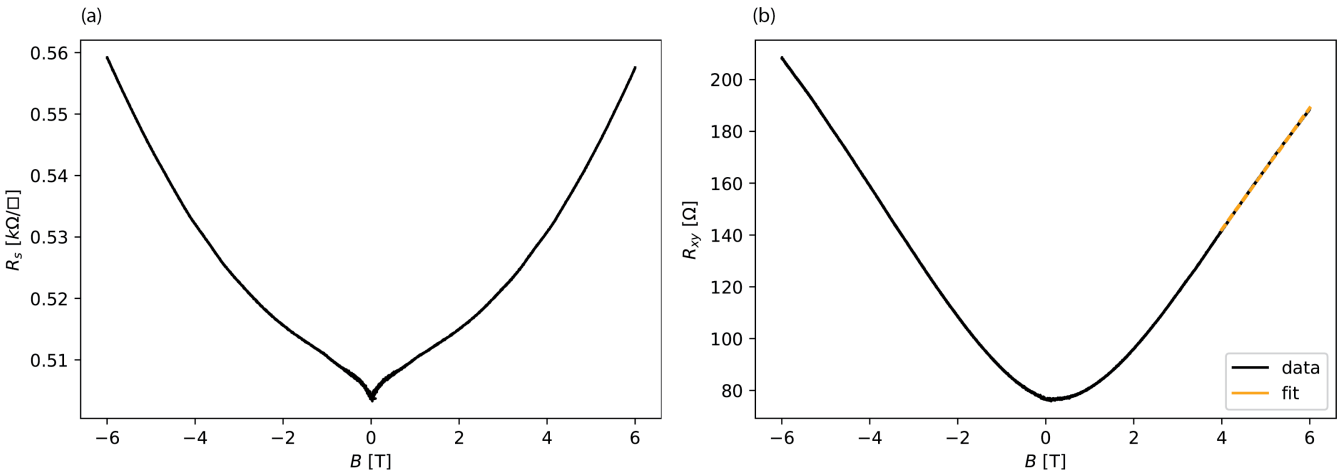

Figure 28: Hall measurements with perpendicular magnetic field from sample 8. (a) R_{xx} as function of magnetic field. (b) R_{xy} as a function of magnetic field. The dotted line indicates where the data have been fitted to find the carrier density n_s.

$$V_{xy}/I = R_H \cdot B \tag{19}$$

the resulting value for the Hall coefficient was $R_H = 24\ \Omega/\mathrm{T}$. This can be used to calculated the total sheet carrier density using the relation

$$R_H = -\frac{1}{en_{s,tot}} \tag{20}$$

with e being the electron charge. This yields $n_{s,tot} = 2.7 \cdot 10^{13}\ cm^{-2}$. A similar simple derivation for the mobility in the 2-band model cannot be made. Instead we continue with the 1-band model where the electron mobility can then be calculated from n_s using

$$\mu = \frac{I/e}{n_s \cdot V_{xx} \cdot (W/L)} \tag{21}$$

with W and L being the width and length of the Hall bar respectively. This results in $\mu = 1100\ cm^2/\mathrm{Vs}$. Kane *et al.*[38] reported that the high field limit would be dominated by the low mobility carriers. If we accept that statement the mobility calculated using equation 21 will not give an exact number for the total mobility but it gives an insight into the band with the lowest mobility. These measurements were also carried out on sample 5 where the B-field dependence of the resistance was similar and the values generated from the calculations were $R_H = 31\ \Omega/\mathrm{T}$, $n_s = 2.0 \cdot 10^{13}\ cm^{-2}$ and $\mu = 630\ cm^2/\mathrm{Vs}$. Both mobility and carrier density are comparable to values recorded in other experimental works, though the mobility is ≈ 15% of the highest recorded mobility in LAO/STO[9]. This result could be an artifact of the PMMA fabrication method yet it could also be argued that it reinforces our belief in the 2-band model as we report low mobilities relative to

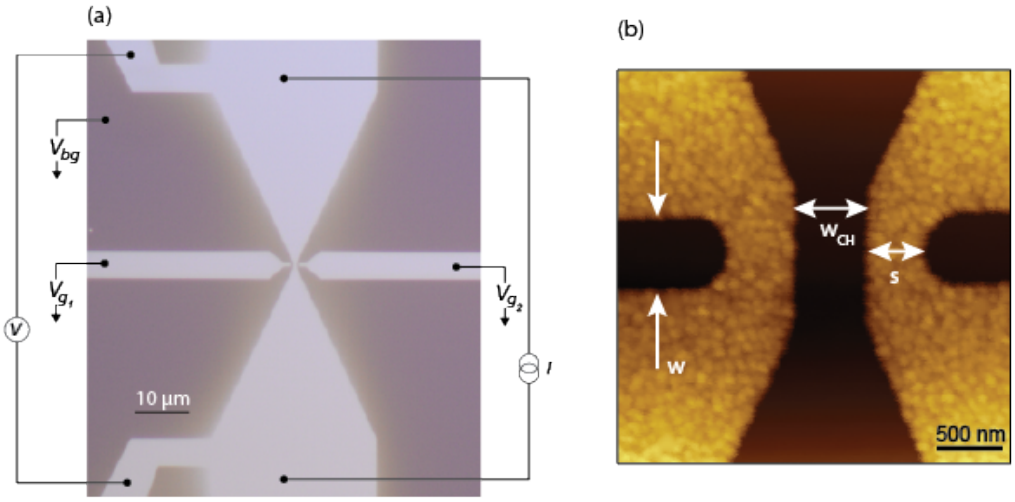

Figure 29: Setups for split-gate measurements. Both pictures originate from sample 5. (a) Optical microscopy image of the split-gate tested on sample 5 with the measurement setup. (b) AFM image of the split-gate area from (a).

other studies. Hall measurements on all devices displayed this same behavior and the analysis was in all cases similar to this. The fact that the carrier densities are comparable to results reported in other works is a great sign for the PMMA based fabrication.

4.3 Split- and back-gating

Two variations of split-gates defined with PMMA were fabricated and measured on sample 5 and 8 respectively. The different device geometries can be seen in table 3. Both devices were measured using the setup seen in fig. 29. Stanford lock-ins were once again used to source the voltage and measure the current and voltage. The side-gates and back gates are hooked up to two Keithley voltage sources, model 2400 and 2600B respectively. The Keithleys function as voltage sources and can simultaneously measure the current through the gate allowing for a measure of the leakage current. Initially the split-gates would be moved in negative voltage until they started leaking. This would then be repeated for positive voltage and a safe range for split-gate operation would be defined. The back gate do not leak in any considerable manner to the substrate and can be operated within ± 200 V.

	Sample 5	Sample 8
w	500 nm	200 nm
s	500 nm	200 nm
w_{CH}	500 nm	100 nm

Table 3: Table over device geometries tested with PMMA defined devices. Noted is the width of the split-gates, w, the spacing between gate and channel, s, and the width of the Hall bar channel w_{CH}.

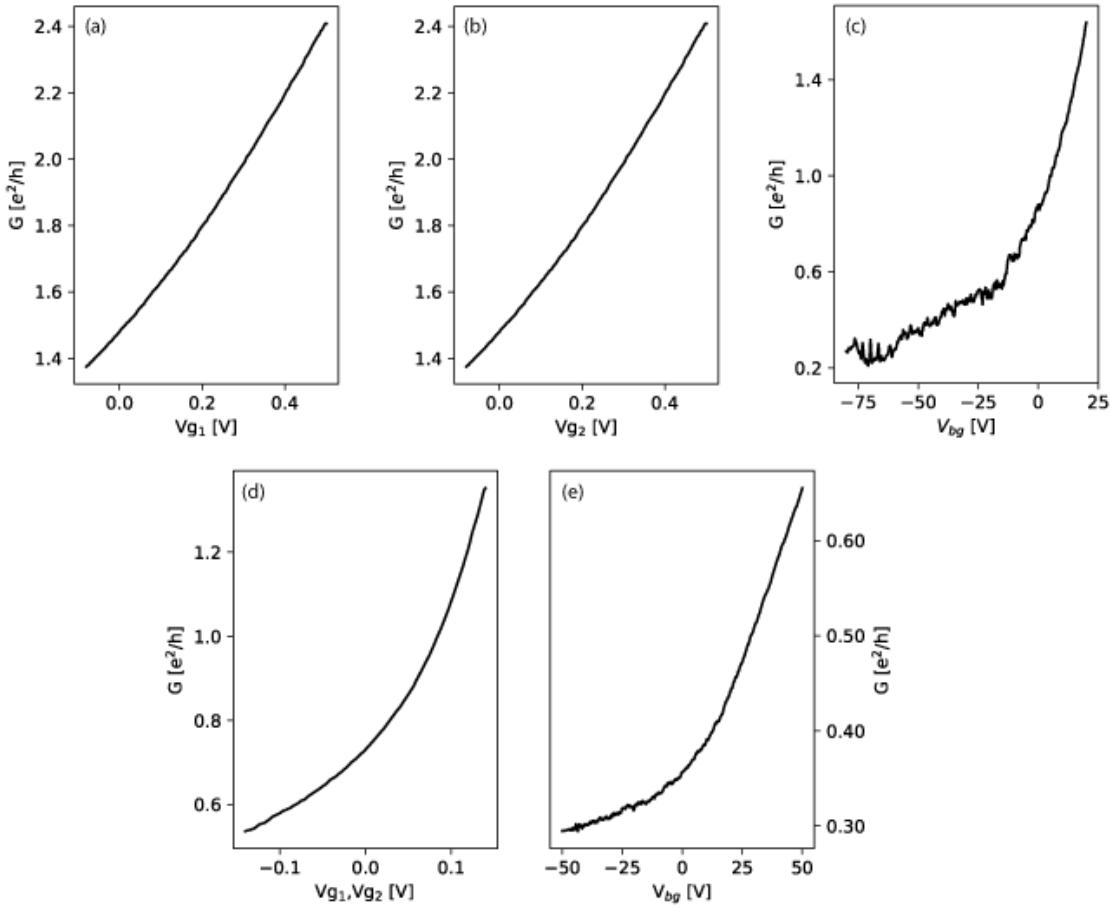

Figure 30: Gate cuts from (a-c) sample 5 and (d-e) sample 8 showing the change in conductance in e^2/h. (a) and (b) are individual side-gate sweeps. (c) is the back-gate sweep from sample 5. As can be seen the conductance of the back-gate have a lower onset than the side-gates. This is due to hysteresis induced largely by the back-gate. The sweeps plotted here are taken after having moved the gate around. (d) is the combined side-gate sweep on sample 8 and (e) is the back-gate sweep on sample 8. Conductance onset in similarly shifted for the back-gate.

In fig. 30 side- and back-gate sweeps are displayed for the two devices. Leakage current occurred at slightly different points during different sweeps on the same devices depending on speed of voltage sweep and thermal cycling of the samples. The largest ranges recorded was [-150 mV, 1 V] for the 500 nm device and [-140 mV, 140 mV] for the 200 nm device. Both devices show the same general change in conductance with a large change in the beginning which flattens out prior to closing of the channel, if the gates do not leak prior to this. The devices do not function as quantum dots or display quantized conductance.

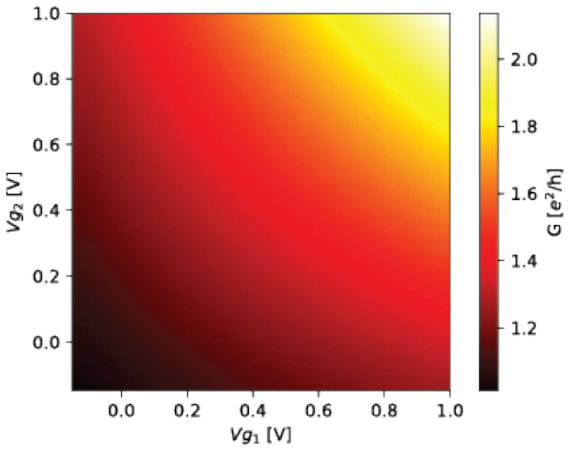

Figure 31: 2D map of the conductance modulated by the two split-gates from sample 5. Gates show identical coupling to the 2DEG with ~ 4 times larger modulation when combined.

To test the effect of the two gates on the 2DEG a measurement was setup sweeping the two gates against each other from -0.15 V to 1 V. The resulting plot can be seen in fig. 31. The data is symmetric around the diagonal, corresponding to sweeping the gates together, indicating that the gates are coupled identically to the 2DEG. Individually the modulation is ~ 1/4 $(e^2/h)/V$ while together it is ~ 1 $(e^2/h)/V$, a very similar behavior to the results recorded by Monteiro et al.[19] a study that also used the 2DEG as side-gates, with different geometrical values. This is a good indication of the reliability of the method and also reinforces the use of PMMA as hard mask. Note the different scales of conductance between side-gates and back-gate. This change in conductance is due to a hysteresis effect in the material. A similar behavior is discussed by Bark et al.[40] where it is explained as movement of the oxygen vacancies with applied E-field that reconstructs after a full forward and backward sweep. Quite typically the back-gate measurement were done by moving the back-gate down in voltage then up and then take the full sweep reported in this work. The initial back-gate sweep starts at roughly the same conductance as the side-gates. Due to this effect the back-gate sweeps on the samples are always saved for last as not to change the conductance prior to for example Hall measurements.

The gate dependence was further examined by sweeping both side-gates together against the back-gate. The resulting figure can be seen in fig. 32. At high back-gate voltage the side-gates are able to modulate the conductance the greatest and as the back-gate voltage drops the modulation decreases until a certain point where it is practically negligible. The declining modulation of the conductance with increasing gate voltage is due to the electric field dependence of the dielectric constant of STO. In the previously mentioned paper by Monterio *et al.*[19] the dielectric constant as a function of applied electric field is modeled as

$$\epsilon = 1 + \frac{B}{[1 + (E/E_0)^2]^{1/3}} \tag{22}$$

were E_0 and B are constants and E is the electric field. As the electric field from the back-gate increases the dielectric constant of the STO drops which leads to a reduction of the capacitative

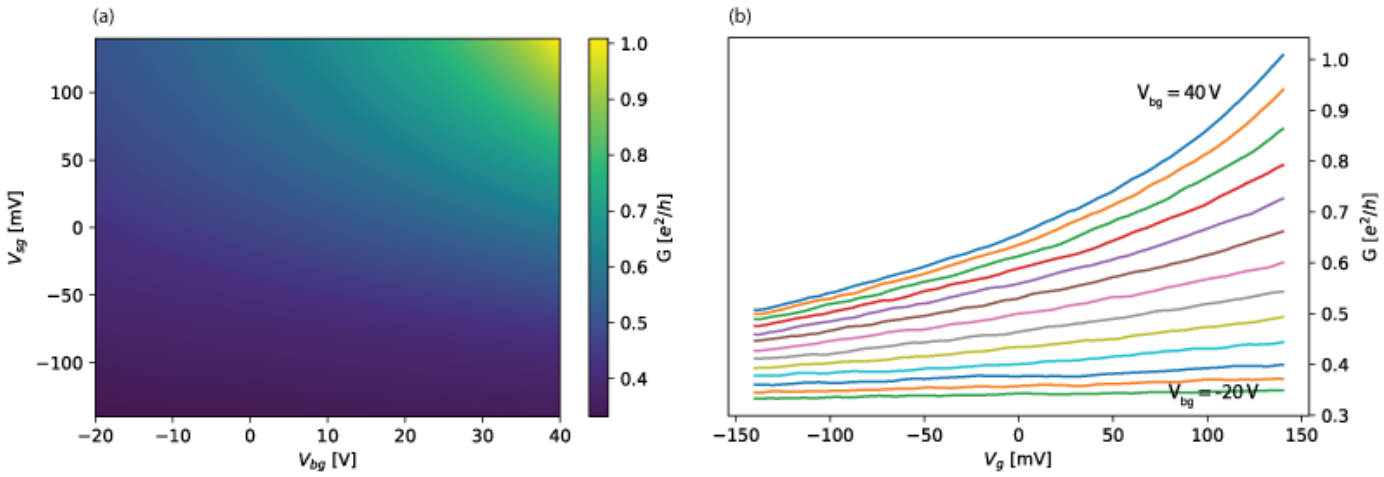

Figure 32: Results from side-gate versus back-gate characterization on sample 8. (a) 2D spectrum from side- and back-gate displaying change of the conductance. (b) Cutouts of (a). Lowest curve is -20 V with each subsequent curve being incremented 5 V.

coupling between the side-gates and the 2DEG. This relation also describes the declining modulation observed for the side-gate traces in fig. 30. As the voltage on the side- or back-gates are increased the dielectric constant drops and this causes the conductance modulation to decrease. This behavior was also observed in the LSM etched samples. Why the total modulation of the side-gates is increased with back-gate is currently unknown. Two obstacles present themselves that have to be addressed before these structures can realize quantum phenomena which is the low voltage range without leak and the coupling between the gate and the channel.

5 Results and discussion - LSM etched samples

Several devices were made with metallic side-gates on an LSM top layer following the schematics presented in section 3.1. Source drain spectroscopy is conducted to reveal coulomb blockade on the structures. Measurements on working dots are centered around magnetic field dependence which can grant insight into the interactions between electrons in $LaAlO_3/SrTiO_3$.

5.1 General device performance

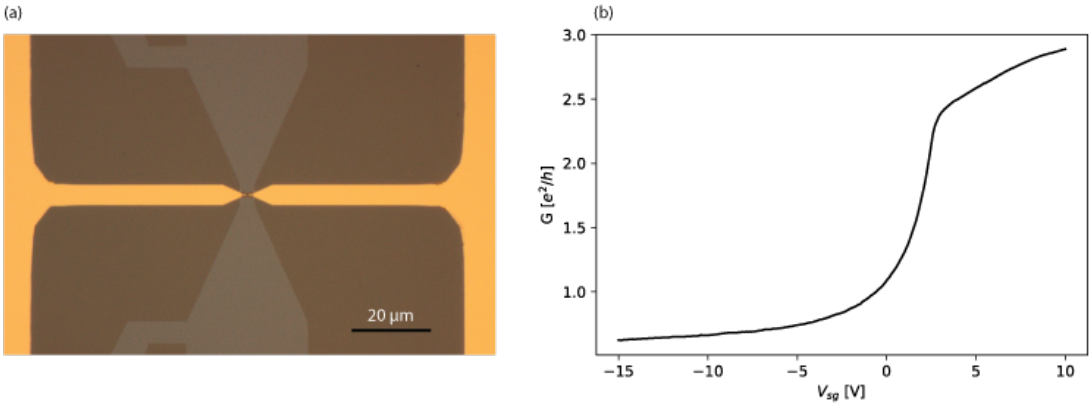

Figure 33: Results from sample 9. (a) Optical microscopy image of device 8 on sample 9. This is a QPC style split-gate with 250 nm spacing. The etched channel is 3 μm wide. The distance between the two split-gates is 250 nm. (b) Conductance during a combined side-gate sweep. A new behavior is observed at about 3 V were the conductance modulation drops similar to the negative range.

Measurements on metal gated devices were done on four different samples during five cooldowns in a dilution fridge. The main results for this thesis came from sample 4 were a quantum dot formed and was extensively measured. The highest quantity of devices measured however was the simple split-gate design seen in fig. 33.(a). Using lock-in techniques and Keithley voltage sources analogous to the PMMA split-gate measurements. Different device geometries were tested on ~ 15 individual split-gate devices and no indication of quantum dots or quantized conductance was observed. It is assumed that the etching of the gold away from the area of the split-gates that are in closest proximity to the 2DEG has a large impact on device performance. To test this assumption and attempt creating a dot with this geometry four different tests were performed:

1. Top-gating of the LAO/STO. As mentioned previously space was left open on the samples for top-gating with Ti/Au electrodes. These were deposited with the same procedure as the split-gates. While top-gating has been used succesfully before on c-LAO/STO[42] the gates made here leaked directly to 2DEG from 0 bias. While devices might be possible if an extra oxide is introduced below the electrode this was not pursued.
2. LSM can be etched by other etching solutions than the Ki/HCl mix therefore etch tests were made using buffered HF and HCl. The tests indicated that HCL in a diluted mix could etch the

LSM in a reliable manner yet HCl targets titanium rather violently releasing a lot of thermal energy that rips the entire electrode off the sample.

3. As the gold is the metal that is targeted by the KI an attempt was made using only titanium as a gate electrode. While the titanium did work as a gate electrode the results were weird and ultimately the endeavor was abandoned.

4. In the final iteration of the Ti/Au electrodes tested the width of the Hall bar channel was shrunk down to 300 nm to limit the destruction of the gates. One device was also specifically designed with a 1 μm wide channel where the side-gates were situated outside the etching window such that they were not destroyed. Interestingly this completely removed the leak from the side-gates that could be operated in a range ± 20 V, see fig. 33.

As can be seen a whole new part of the side-gate spectrum is opened up when leak is dropped. Equation (22) is symmetric in electric field so we would expect to see the same behavior when moving to positive gate voltages. Without the leak we can now observe this behavior. Measurement of geometries that do function as quantum dots combined with this reduced etching window is highly interesting as it would allow for operation of the quantum dot in a much larger range but it was not done due to time constraints.

5.2 Quantum dot

Quantum dots formed in the split-gates with geometries as explained in section 3.1. Dots were measured on 2 samples with three cooldowns. The primary data discussed in this section was measured on sample 4 on a device with a diameter of 500 nm which can be seen in fig. 34.(a). Due to dirt particles in the resist formed during spin coating the acid used to etch was able to make contact with the LSM where it shouldn't have. This is the reason for the observed spots of revealed STO around the channel.

A cooldown profile from sample 4 is visible in fig. 34.(b). The same dependence on the conductance as described before is present here. In fig. 34.(c,d) a set of Hall measurements are visible. R_{xx} dependence is very similar to the previous dataset shown though the dip attributed to WAL is much smaller than previous. The R_{xy} has an offset of ~ 1 T compared to the expectation that the minimum is at 0 T. Currently this is not well understood but it could be hysteresis similar to the results seen by Brinkmann *et al.*[3]. The fit shown in fig. 34.(c) resulted in a density $n_s = 3.1 \cdot 10^{13} cm^{-2}$ and a mobility $\mu = 440 cm^2/Vs$. Again quite similar results as seen before and the mobility is still relatively low. In fig. 34.(a) the measurement setup for gate characterization can be seen. The setup is similar to the PMMA split-gate setup only the AC voltage source is wired through a voltage divider that reduced the voltage with a factor 1000.

In fig. 35.(a) the conductance is plotted as function of V_{SG}. As the gate voltage is swept down the conductance first get very noisy, yet with a finite condutance, and then finally drops to 0 followed by peaks of conductance similar to coulomb peaks in a quantum dot described in section 1.5.1. The change occurs as energy levels of the dot in and out of conductive regimes as described in section 1.5.1. In fig 35.(b) a gate sweep with higher resolution is plotted that shows the same behavior. The peaks are not easily identifiable between the two plots and the general spectrum have shifted.

The measurement setup is now changed. The National Instruments daq card is connected to source a DC bias voltage through a 1:1000 voltage divider while the lock-ins add an AC signal that runs through 1:10000 voltage divider. The voltage signal is split into two; one goes to the daq that

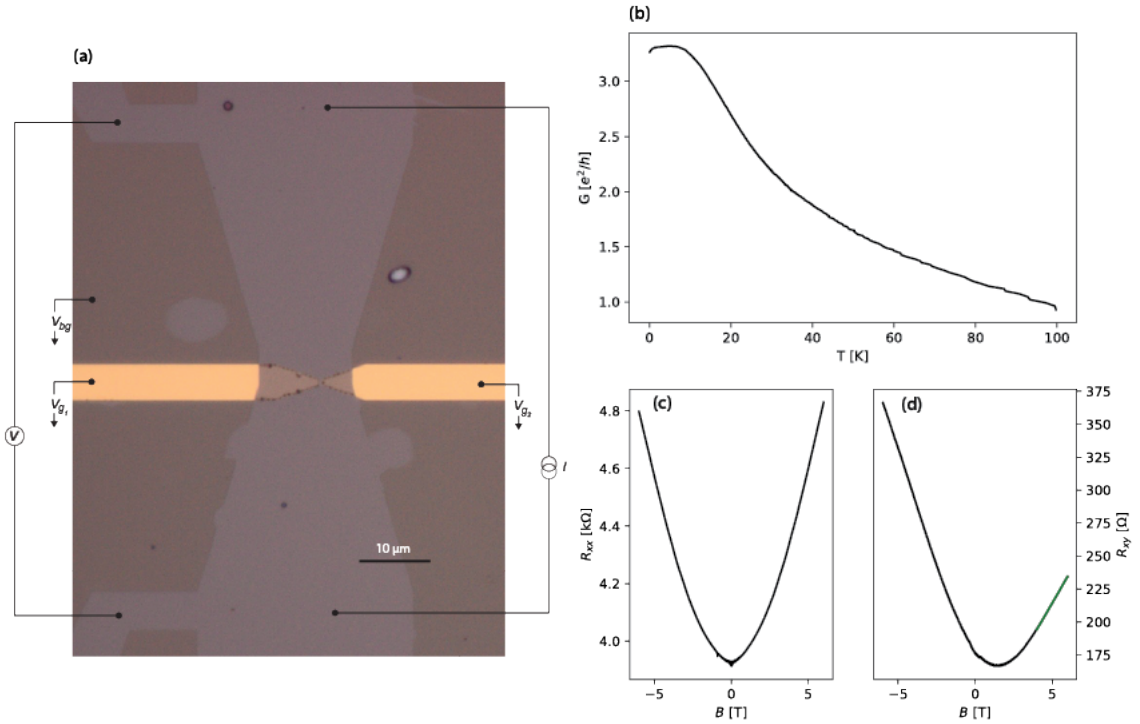

Figure 34: Sample 4 overview. (a) Optical microscopic image of the measured dot device from sample 9. The conductive channel is 3 μm wide and the diameter of the center 500 nm. (b) Cooldown profile from device 3 on sample 4. Device 3 is a QPC type device with a 200 nm spaced channel. (c) R_{xx} measurement from sample 4. (d) R_{xy} measurement from sample 4. On the right side the data (black) is covered by a linear fit (green) used to determine n_s.

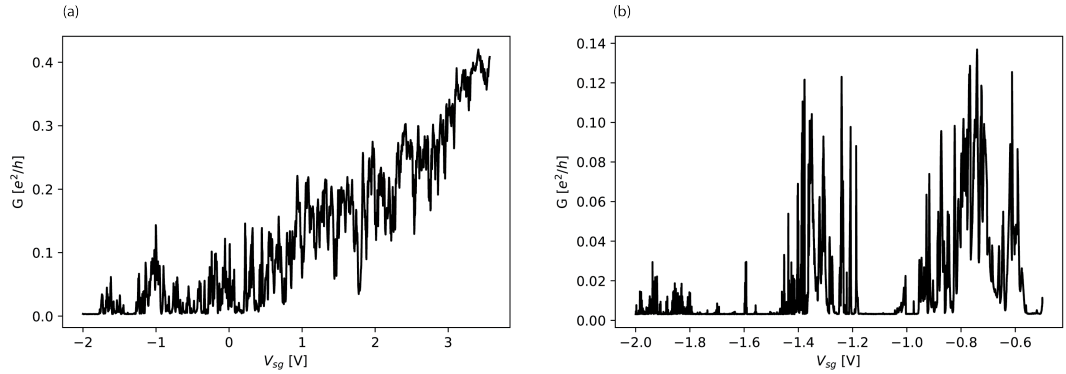

Figure 35: Data from V_{sg} sweep on device 11 on sample 4. (a) Fullrange gate sweep down to -2 V from 3.56 V. Outside this range the gate leaks. (b) Fine gate sweep in the negative voltage region displaying the peaks with higher resolution.

measures the DC voltage, the other runs to the lock-in that measures the AC voltage such that the conductance and differential conductance are now measured at the same time. The gates are also moved to the daq card as it can operate much faster although it cannot track the leak current. A bias spectroscopy was done by measuring the conductance with the bias voltage, V_{SD}, sweeping -1 mV to 1 mV against V_{sg} 0 V to -2 V. The result can be seen in fig. 36. The diamond structure is clearly visible with very different sizes of diamonds present which could be an indication that the energy level spacing is a dominant energy scale. Around 1.2 V V_{sg} we see very large diamonds that extend beyond the measured bias range. There are not well-defined peaks in between these diamonds. In the cutout shown in fig. 36.(b) smaller size diamonds can be seen with well defined peaks in between. At -0.96 V V_{sg} a sudden change in the system occurs as a peak appears out of nowhere. This "switching" can also be seen in the cutouts i fig. 36 (c) where a vertical drop with no line width can be seen. These switches are present in the full range of the side-gates. Around the diamonds the differential conductance stay at finite values that generally are quite noisy. No excited states are clearly visible in this data set. From fig. 36 (c) it is however clearly visible that we can see individual peaks in the spectrum. Note that "zero bias" is shifted down to roughly -0.1 mV probably due to some offset from the preamplifier.

By applying a magnetic field the energy levels will shift as explained in section 1.5.1. The slopes of energy levels can be used to calculate the g-factor of the electronic states in the quantum dot. Instead of following a single peak a gate range is found that encloses several peaks. This has several benefits primarily that the g-factor can be calculated from the evolution of the distance between neighboring peaks, ΔV_{SG}. These should evolve as

$$E_Z = g\mu_b B \tag{23}$$

Should any global shifts be present in the system these will be circumvented by measuring the g-factor in this manner. Data sets resulting in g-factors were measured in three areas of V_{SG}. The procedure was as follows. First a suitable gate range was chosen from a V_{SG} sweep at 0 bias voltage. A suitable range has several free standing peaks within a narrow voltage range. Within this voltage range a constant sequence of measurements were done. Initially a bias spectroscopy was collected from which the lever arm can be determined as the slope of the diamonds with the equation

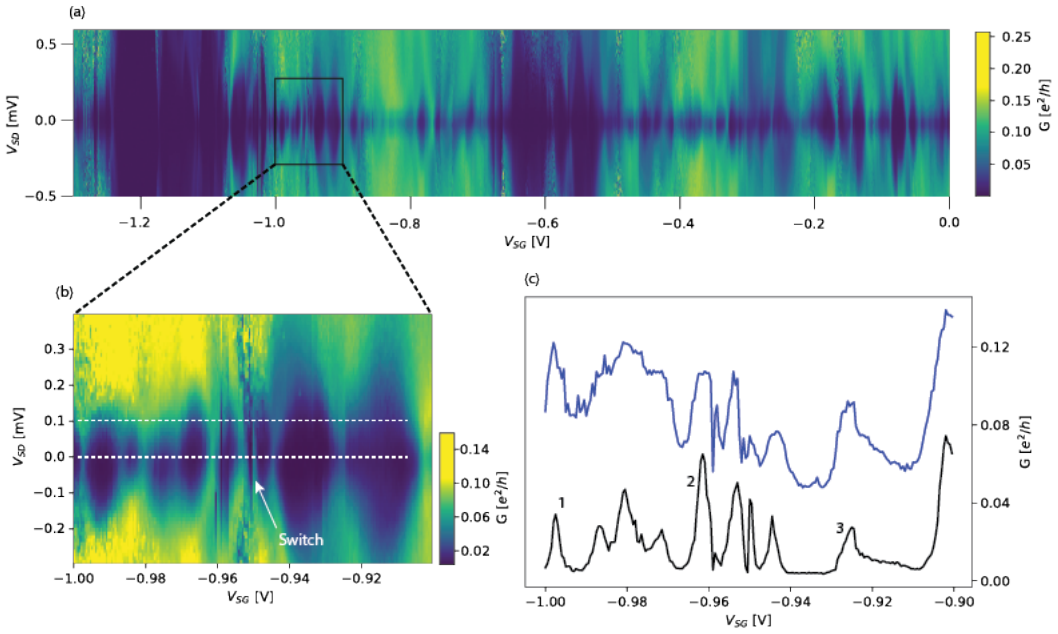

Figure 36: Bias spectroscopy of device 11 on sample 4. An offset of -0.1 mV has been corrected in all 2D plots. (a) Full range bias spectroscopy. The bias range has been cut down to -0.5 mV to 0.6 mV for visibility of the small diamonds. Cutout box shows the area plotted in (b). (b) Cutout of (a), giving a smaller view of the diamond structure. The two lines represent the profiles plotted in. (c) Line cuts of the bias spectroscopy. The blue data has been shifted artificially for clarity. Numbers 1, 2 and 3 are placed near peaks that could be traced.

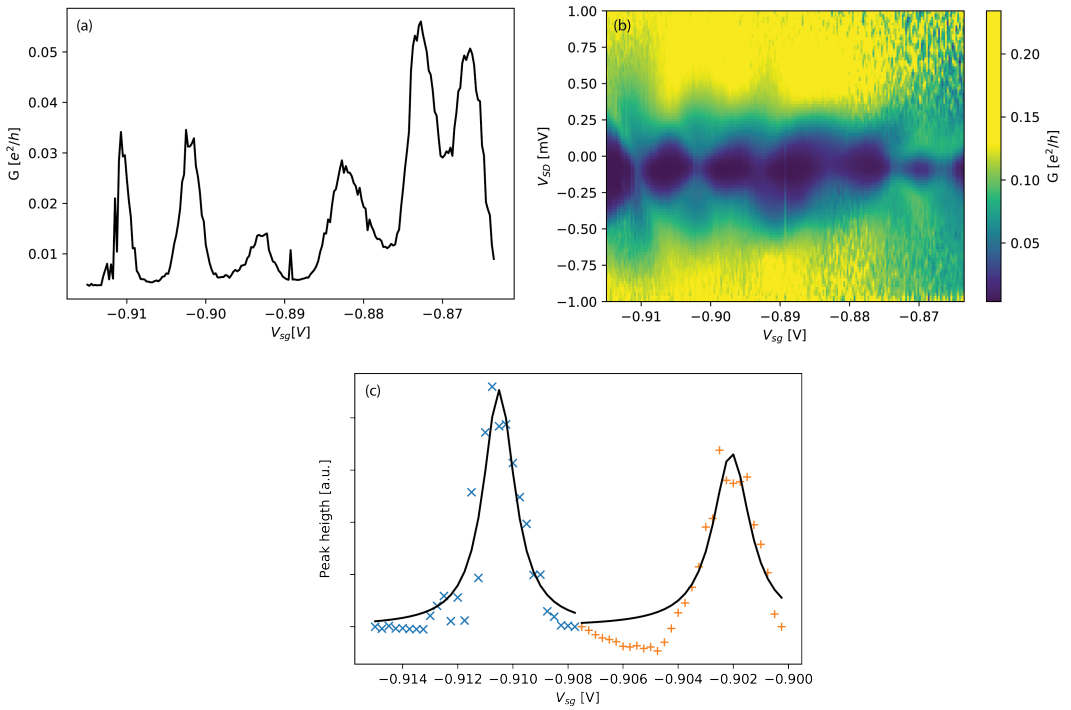

Figure 37: Bias spectroscopy for data set 1. (a) Zero bias (-0.13 mV) cut showing 6 coulomb peaks. The two left most are especially well defined. (b) 2D bias spectroscopy from data set 2. The white lines indicate the diamond used to determine α. (c) Zero bias peaks of the diamond highlighted in (b). The symbols are the fitted data points and the curves are the Lorentzian fits.

$$\alpha_{pg} = \frac{\Delta V_{SD}}{\Delta V_{sg}} \tag{24}$$

here ΔV_{SD} is half of the height of the diamond and ΔV_{sg} as the width of the diamond. In fig. 37 (a) and (b) the bias spectroscopy for data set 2 can be seen along with a cutout of the conductance peaks at 0 bias. The height of the diamonds can be extracted from the 2D plot while the width can be determined by fitting the two zero bias peaks, see fig 37 (c). The data containing individual peaks are singled out and then the background that offsets the peak edges from 0 is removed. This makes the fitting function more reliable than if the raw data for each peak is used. The data is then fitted to a Lorentzian line shape. The peaks are fitted to this function due to tunnel broadening of the energy levels originating from the transmission probability in the setup. The Lorentzian fit function looks like this

$$L(x) = C \cdot \frac{\Gamma^2}{(x - x_0)^2 + \Gamma^2} \tag{25}$$

Here C is a constant, Γ a parameter defining the width and x_0 the center of the peak. By extracting x_0 for the two fits lever arm calculated. The side-gates are now swept against the magnetic field.

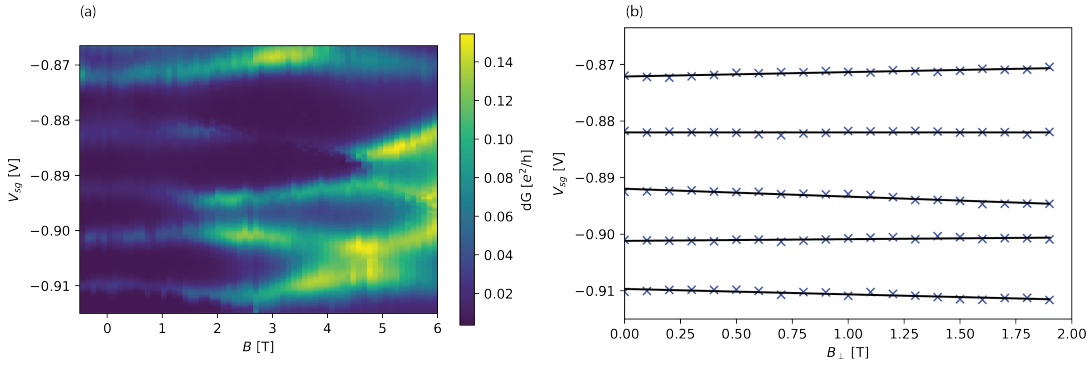

Figure 38: Peak dependence on B-field for data set 2. (a) V_{sg} vs. B diagram. The data has been realigned around 2.7 T to fix a shift. (b) the positions tracked by the Lorentzian fitting function up to 2 T. The crosses are data points and solid lines the fit.

All of the sweeps showed a tendency to switch between different states. Often this would result in a data set scrabbled in between several states such that individual peaks cannot be tracked. Because of this the measurements were done in constant sequence as to increase the chance of a good data set. In fig. 37 the peak position as function of B field can be seen for data set 2. This data set did in fact shift at 2.7 T but it was not a change of state so the peaks could be realigned to the plot seen in fig. 38.(a). By fitting a Lorentzian similar to before the peak position can be tracked. In fig. 38.(b) the peak position up to 2 T has been plotted. After 2 T the peaks broaden quite a bit more and one of the peaks vanish. From the peak positions in fig. 38 (b) ΔV_{SG} can be extracted and the g-factor fitted as the slope.

Data set 1 and 3 were measured with $B_\perp$ while data set 2 is from $B_\parallel$. After measurement of data set 3 the fridge blocked due to contamination build up in the LN_2 trap. The sample was thermally cycled to room temperature as the fridge was cleaned. After recooling the device performance was greatly reduced. It was possible to generate a dot using the back-gate. The depletion curve was similar to fig. 35 with pinch off of the conductance from -2.5 V V_{BG} and well separated peaks towards -10 V with fairly good stability. Data recovered from this setup did however only display one peak shifting with B therefore it is omitted in favor of a focus on the $|DeltaV_{SG}$ data. Below is three figures, 39 40 41, giving an overview of the 3 data sets and the resulting g-factors.

Ideally the conductance peaks seen in fig. 35 (b) would be narrow, well separated peaks broadened slightly by thermal broadening and the tunnel coupling. What is seen in the data is much more broadened peaks that do exist separately in some cases but also in clusters of peaks that have turned a larger range of V_{sg} conductive. This behavior is further evident from the diamond structure seen in fig. 37.(a). Comparable dot structures in 2DEGs on semiconductor materials show regions of non-conductive followed by sharp peaks of conductance that outline the diamond structure including excited state peaks. For our structure the diamonds vary greatly in size and they are surrounded by conductive regions with no excited states clearly visible. These results are quite similar to the work done by Maniv *et al.* from 2016 [27]. Here a similar split-gate geometry on c-LAO interface is used to confine the 2DEG into a quantum dot configuration. The sizes of the diamonds vary due to the suppression of the charging energy $E_C = \frac{e^2}{C}$ in STO due to the dieletric constant measured to about 20 000. If E_C was dominant we would expect to see diamonds of similar size controlled by this energy scale. The energy levels are more chaotic resulting in varying diamond sizes. Assuming

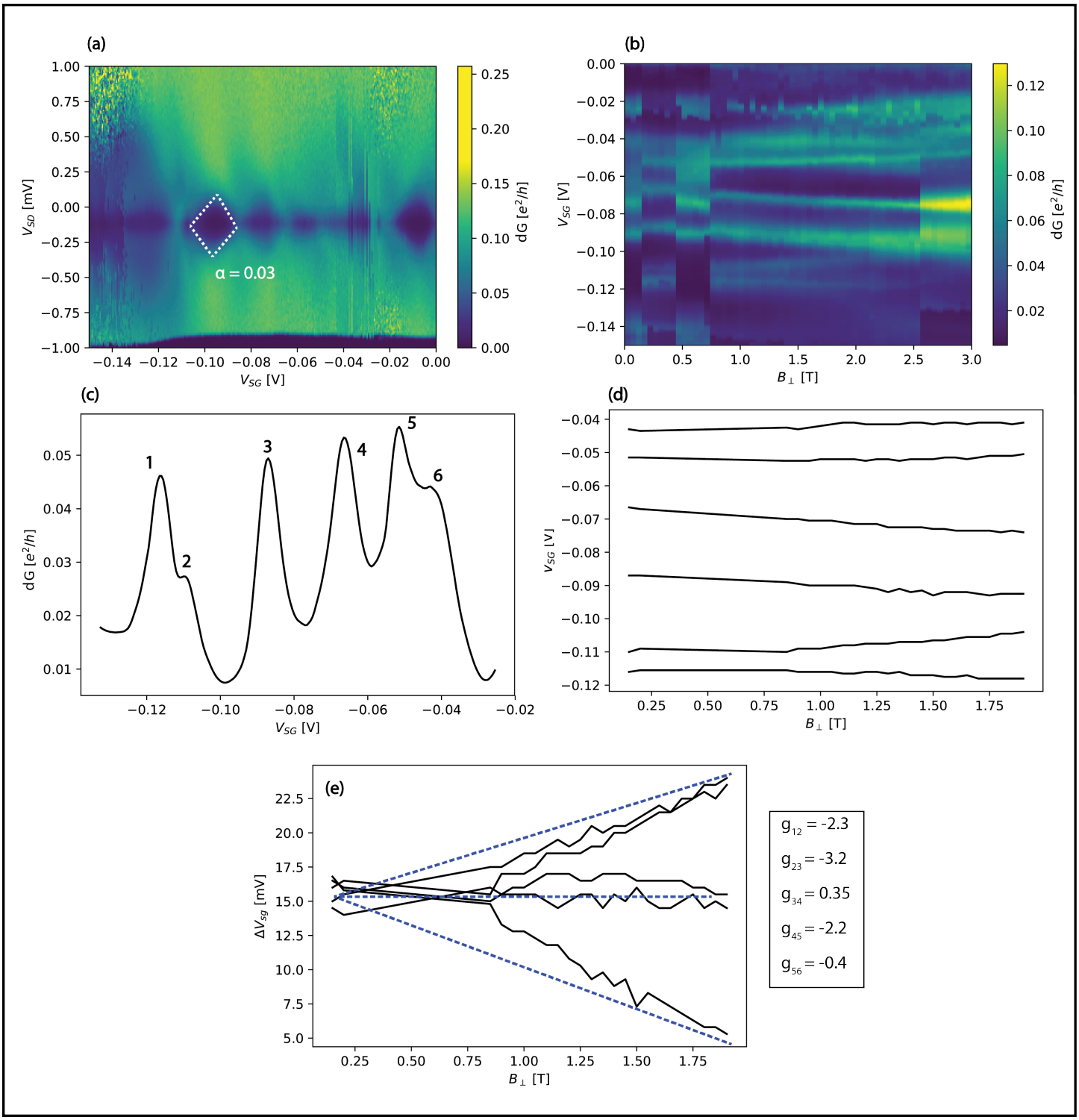

Figure 39: Data set 1. (a) Bias spectroscopy with the diamond used to calculate α outlined (b) Peak shift in B field. (c) Peak identification. (d) Peaks tracked by the Lorentzian fitting function. (e) Peak distance offset artificially to same origin along side g-factors. Dashed line is just a guide for the eye.

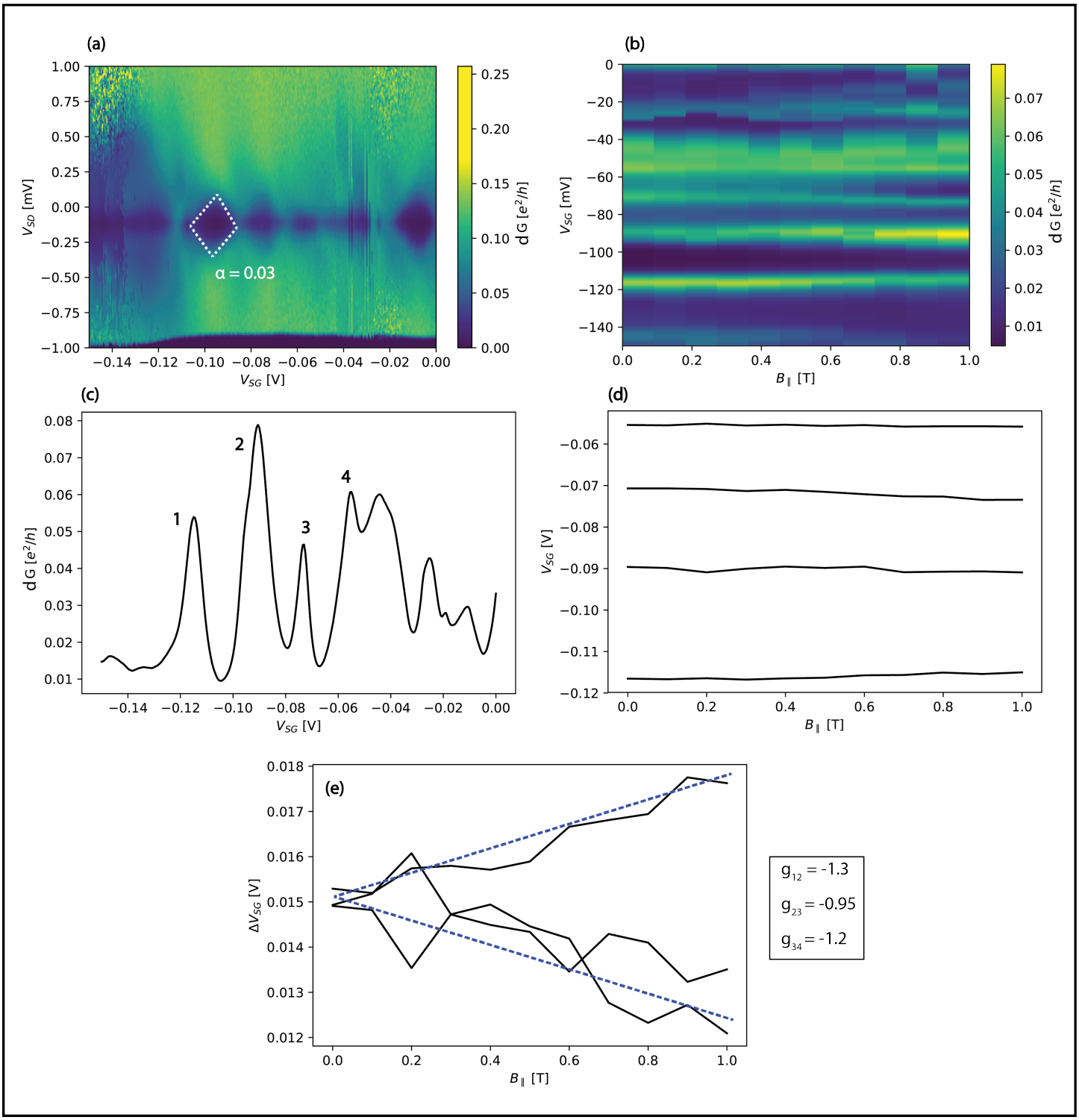

Figure 40: Data set 2. (a) Bias spectroscopy with the diamond used to calculate α outlined (c) Peak identification. (d) Peaks tracked by the Lorentzian fitting function. (e) Peak distance offset artificially to same origin along side g-factors. Dashed line is just a guide for the eye.

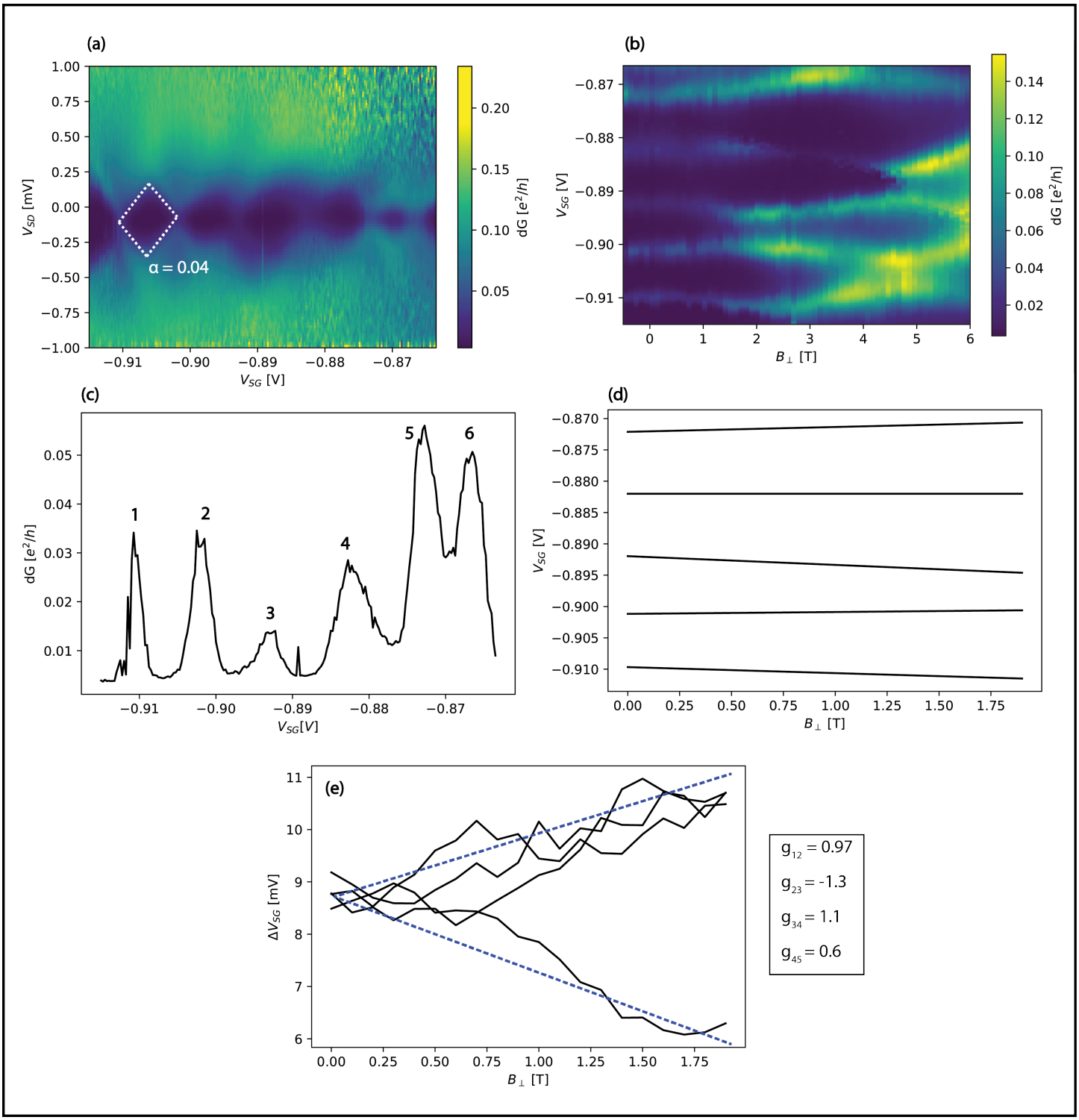

Figure 41: Data set 3. (a) Bias spectroscopy with the diamond used to calculate α outlined (c) Peak identification. (d) Peaks tracked by the Lorentzian fitting function. (e) Peak distance offset artificially to same origin along side g-factors. Dashed line is just a guide for the eye.

the dot takes the form of a disc the capacitance is expressed as $C = 8\epsilon_0\epsilon_r R$. Follwoing this the charging energy will be proportional to $1/\epsilon_r$ and is greatly suppressed compared to semiconductor systems. The switching behavior can be explained by the potential landscape created by the gates. John A. Nixon and John H. Davies[43] described how the potential in a heterostructure would vary with an applied gate voltage. Rather than a smooth function the potential landscape was found to be made up of random "puddles" connected throughout the device due to randomly spaced donors. As the voltage on the gate was dropped into the negative range the puddles became disconnected and potential valleys where electrons can reside are created. If such a puddle forms inside the device measured here it would work as a quantum dot. The dot is however highly sensitive to charges around it. If a charge in a nearby puddle shifted, for example due to an applied E-field, it would effect the dot changing the electrostatic energy.

The lever arms measured is in fine agreement with data from other studies in STO/LAO[27]. It can however be noted that due to the diamonds not being sharply defined some error is introduced in the calculation primarily from determining the diamond height. The diamonds used to calculated α has been outlined in the data overviews. In the B vs. V_{sg} diagram in fig. 38 the movement of the energy levels can be tracked. From 0 T to 2 T the peaks vary linearly with B-field. At 2 T the two peaks between -0.9 V and -0.89 V V_{sg} almost touch each other before they deflect. Generally coulomb peaks in quantum will not cross as the charging energy still have to be paid.

ΔV_{SG} measurements from data set 1 can be seen in fig. 39.(e). As expected the peaks move either up or down with the slope $g\mu_b$ but two of the peaks are flat resulting in a g-factor close to 0, i.e. two neighboring peaks have been moving with the same slope as a function of B-field. This can be explained as the addition of an electron with the same spin as the previous energy level. According to equation (10) such states would indeed shift identically. Quite the similar scenario was observed by Folk *et al.*[44]. They studied a semiconductor chaotic quantum dot were they saw the same addition of equal spin states in neighboring peaks. They discussed their results on the basis of a Hamiltonian that excluded spin-orbit coupling and superconductivity yet retained the exchange interaction between electrons which adds the term

$$JS(S+1) \tag{26}$$

were J is the exchange constant or the exchange integral. The exchange interaction introduces an energy correction that favors similar spin states. This would lead to $S<1/2$ which would lead to the picture seen in data set 1. These three directions of the peak distances could also be a result of some orbital effect coupling to the magnetic field. If this was true one would expect to see a larger spread of the peak directions while the good agreement between g-factors for the up and down slope indicate that this is related to the spin of the system. These higher spin states were only observed in the coulomb peaks from data set 1.

g-factors reported in other studies on LAO/STO vary a between 0.3 and 2[4] while the most common value is about 1.5[6]. What is observed from this data is quite a big spread in g-factors between ~ 1 and 2.5. While this variety could be an artifact of the device quality global shift of the data was corrected for by using the peak distance instead of individual peak position. Fluctuations in g-factor are however reported in semiconductor structures. M. T. Björk *et al.*[45] recorded variable g-factors in InAs nanowires related to the size of the quantum dot. The size of the quantum dot was varied during growth by InP barriers resulting in g-factors varying from the bulk value of 2 all the way up to 13. It was reported that the g-factors were suppressed as the dot size was reduced. Fluctuations in g-factor were also reported by Csonka *et al.*[46]. Similarly in InAs nanowires. Here splitting of

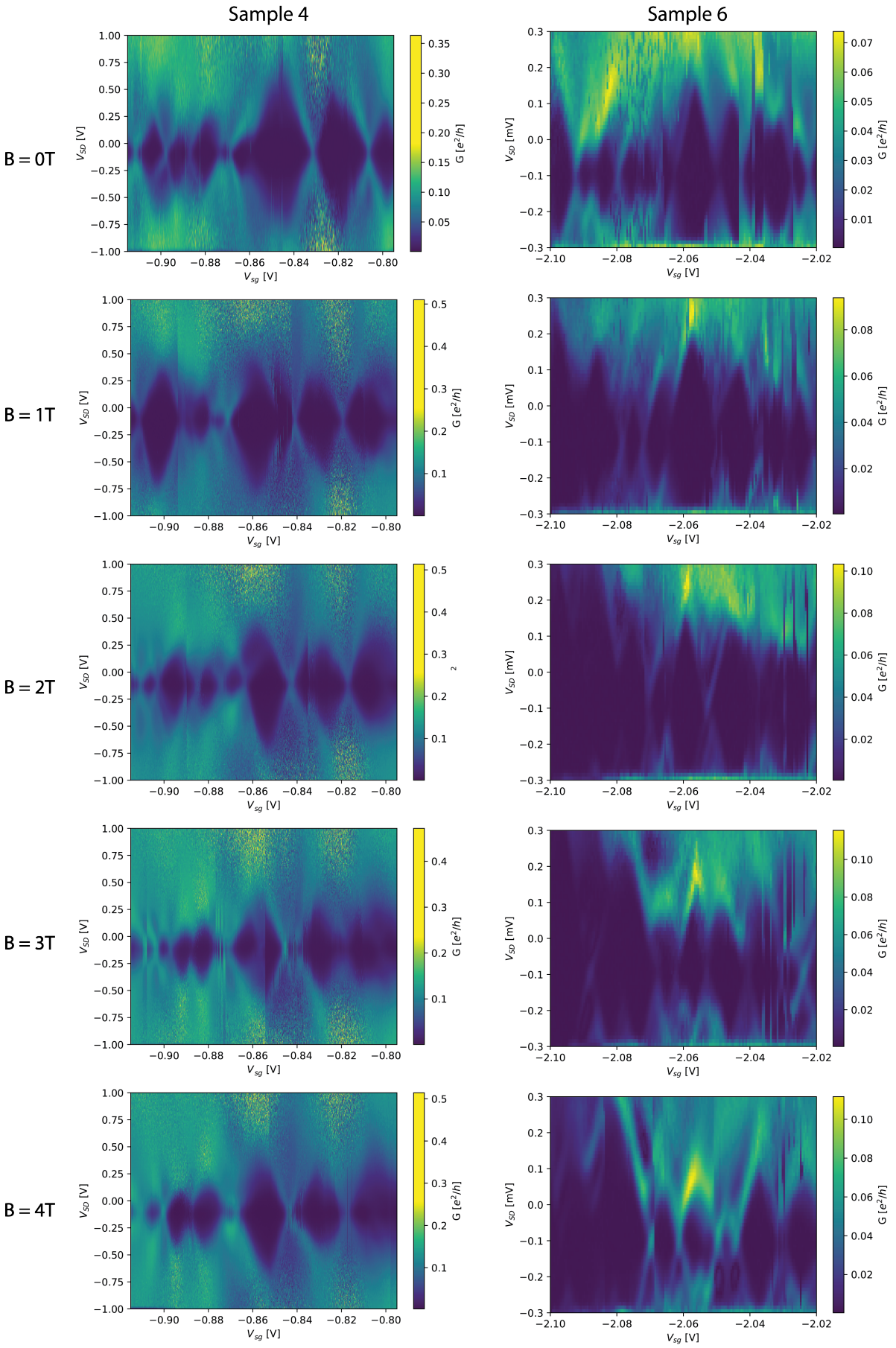

Figure 42: Bias spectroscopy from sample 4 (left column) and sample 6 (right column) at different magnetic fields. The top row is 0 T then 1, 2, 3 and 4 T downwards in $B_\perp$.

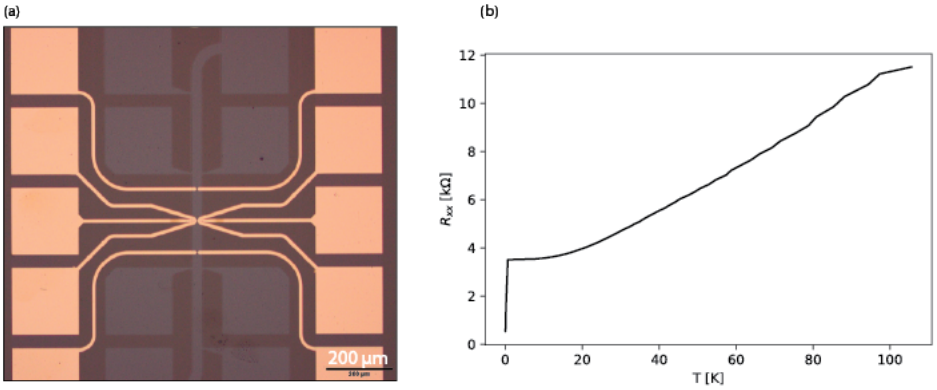

Figure 43: Overview and cooldown profile from sample 6. (b) Optical microscope image of the measured Hall bar on sample 6. (b) Cooldown profile of the Hall bar seen in (a). At ~ 100 mK the resistance drops to ~ 0 as the sample goes superconductive.

kondo peaks was used to determine the g-factor instead of coulomb peaks. Large fluctuations in g-factor were explained by the spin-orbit effect in InAs. The wave function for each of the energy levels, which are not readily available, will show different dependence on spin and orbital effects resulting in varying g-factors for each energy level. This picture is also viable in $LaAlO_3/SrTiO_3$ where spin orbit effects have been displayed previously. The nature of the spin orbit coupling effect on the energy levels can be studied by looking at data set 1 and 2. The two display the same peaks but shifting in perpendicular and parallel field respectively. The spin orbit coupling can be modeled as an effective field B_{SO} coupling to the spin. Dependent on the direction of an applied B-field compared to the spin orbit field different effects will be observed. In this experiment that should result in different g-factors. The g-factors are smaller in data set 2 compared to data set 1 but as can be seen the peaks have shifted around a bit (panel (c) for both figures) spreading some doubt on the results. With a more stable device or measurement it should be possible to better determine the presence of spin orbit interaction in $LaAlO_3/SrTiO_3$ quantum dots.

In addition to sample 4 sample 6 did also have a working dot of the same geometry only sample 6 showed superconductivity below ~ 100 mK. By comparing data from a superconductive dot with a non-superconductive dot some insight into the electron pairing phenomena described earlier may be gained. Electron pairing would show itself in the bias spectroscopy at different perpendicular B-field values. Here the diamonds will split into smaller diamonds when the electron pairing is broken. Bias spectroscopy in sample 4 and 6 with $B_\perp$ from 0 T to 4 T can be seen in fig. 42. No splitting of peaks are observable in this data set. What can be seen in the right column of data is that the superconductivity in sample 6 is suppressed at these gate voltages most likely by reduction of the local carrier concentration around the side-gates. Because of this no conclusion can be made on the topic of electron pairing from these data sets.

5.3 Superconductive Hall bar

As stated sample 6 did become superconductive at sub-Kelvin temperatures. While a comprehensive study of the superconductivity is beyond the scope of this study some measurements was done on a

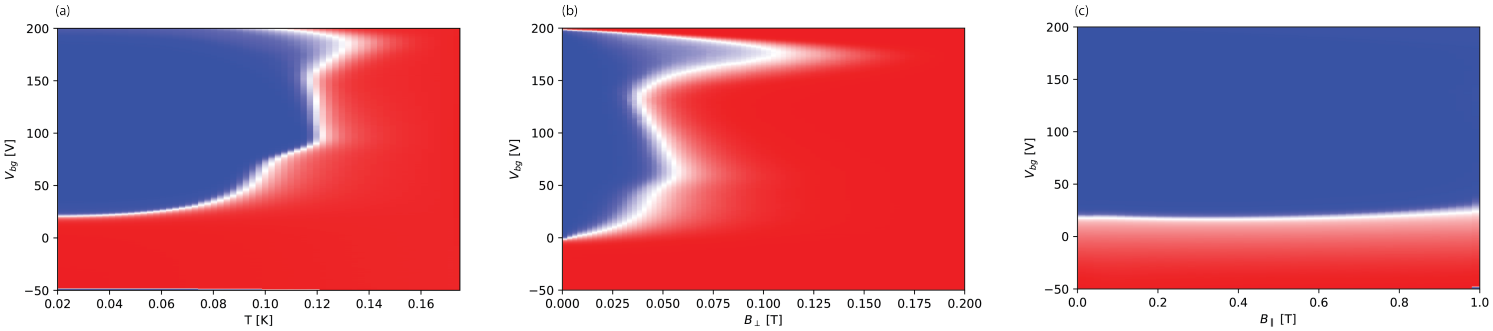

Figure 44: Superconductive Hall bar results from sample 6. Blue is superconductive and red is normal. (a) Temperature break down of superconductivity at different back-gate voltages. The data has been scaled compared to the normal state for clarity. (b) Perpendicular magnetic field breakdown at different back-gate voltages. Data scaled compared to normal state. The dome shows a dominant peak at 150 V. (c) Parallel magnetic field breakdown at different back-gate. The dome is only outlined by the curvature of the dome.

Hall bar structure. The lack of superconductivity in the remaining samples is as of yet undiscovered. The Hall bar can be seen in fig. 43.(a). Several metallic gates have been deposited on the surface of the LAO/STO. These are the top-gates mentioned earlier. During cooldown the setup mirrored the one discussed previously with standard lock-in techniques used to measure I, V_{xx} and V_{xy}. The cooldown profile can be seen in fig. 43.(b). Below 100 mK the resistance drops suddenly corresponding to superconductivity. Hall measurements reveal a density n_s = $3.2 \cdot 10^{13} cm^{-2}$ and mobility μ = $420 cm^2/Vs$ which is comparable to the numbers acquired from non superconductive samples with both resist and LSM.

The voltage divider is now switched out for a 100 MΩ series resistor. By sweeping the back-gate voltage negative and positive the superconductivity can be switched on and off. This dependence is tested versus temperature, $B_\perp$ and $B_\parallel$. The result is a superconductive dome shape in the different diagrams which can be seen in fig. 44. The dome shape is not fully visible in fig. 44.(c) but the lower superconductive border is curving upwards consistent with a dome shape. The sample was oriented such that the perpendicular field had maximum field strength. The $B_\perp$ and temperature domes are non-smooth and especially $B_\perp$ has a large peak in critical field at 150 V. The reason for this is currently unknown. During the first sweeps the dome structure was visible within the voltage range [-50 V, 150 V] so to show the entire dome structure the back-gate was increased to 200 V. Instead of seeing the declining right side of the dome and a normal conductive region the dome simply shifted with the increase in voltage. This explains why the superconductive region has gained an offset to 0 V_{bg} in fig. 44 (a). Following this the setup was changed to a DC sourced system with the aim of measuring super currents against different temperatures, $B_\perp$ and $B_\parallel$. A discussion of the measurements are not included here as they extend beyond the scope of the work.

6 Conclusion

The experiments described here explored the 2DEG emerging at the $LaAlO_3/SrTiO_3$ interface. Work was done in two distinct areas. A new simple fabrication method for creating nanostructures on LAO/STO was implemented based on using PMMA resist as a mask directly on the STO surface prior to LAO deposition. Previously PMMA resist used in this way have been shown to result in insulating samples. The new approach used here included a cleaning treatment of the STO surface after development of the resist. By plasma ashing the samples for 2 minutes followed by submersion in water and IPA the samples became conductive. The limits of the method were tested by electrical measurement of nano scale devices fabricated with the resist. Two novel series of devices were created one designed as wires with alternating widths and one with wires spaced out by alternating distances. These devices were measured in a 4-point setup at room temperature and at sub-Kelvin measurements in a Oxford Triton ^{3}He-^{4}He dilution refrigerator. The resulting data concluded that the 2DEG formed followed the geometry exposed in the resist. Hall bars were also fabricated and measured. The data was explained by a 2-band conduction model. From this the total density of carriers was calculated and the result was similar to densities recorded by other studies. The samples did however not become superconductive which they should below 460 mK (maximum recorded T_C)[47]. Of all the samples used in this work including all fabrications methods only one became superconductive so it is not expected that the PMMA fabrication method affected the emergence of superconductivity. The exact reason for this absence of superconductivity is unknown. Using this new fabrication method split-gate devices were patterned and experiments were carried out testing their functionality. All gates showed leaking to the 2DEG within 1 V at 12 mK. The effect of these gates on the 2DEG was found to be heavily dependent on the dielectric constant of STO. As voltage on the split-gates or back-gate was increased the conductance modulation dropped and eventually leveled. An electric field dependent model of the dielectric constant was displayed that explains this behavior. The split-gates were unable to pinch off the conductance and the devices did not function as quantum dots or quantum point contacts. It is concluded that this new fabrication method is able to create conductive samples with the same quality as devices made with conventional less invasive methods. The fabrication method worked excellently for making Hall bar devices, but it was not well suited for split-gate devices.

Studies in quantum dots patterned on LAO/STO have been carried out by other researchers with interesting results. Among these are the existence of electron pairs without superconductivity and negative charging energy. Here quantum dots have been fabricated using a proven technique created by Trier *et al.*[7]. The STO surface is covered in a protective top layer that remains insulating and can be selectively wet etched. On this LSM layer metallic gates are defined using both photo and electron beam lithography. A crucial error is recorded as the chemical used to etch the top layer also etches the gold used as gate metal. To counter this tests were made using different acid solutions and different gate materials. Ultimately it was discovered that simply reducing the etching window covering the metal gates was a simple solution improving device qualities. Split-gates designed as simple QPC's did not behave as quantum dots and instead displayed the same reduction in conductance modulation due to the electric field dependence of the dielectric constant. A different geometry shaped such that an island of 2DEG resides in the middle did however show coulomb blockade on two different samples. The primary results came from one where coulomb peaks were studied as they shifted in applied magnetic fields. By tracking the distance between neighboring peaks the g-factor could be calculated as a slope and two interesting phenomena appeared. Firstly slopes of ~ 0 appeared corresponding to the appearance of higher spin states. A mechanism that have been recorded in other studies of quantum dots and which can be explained by exchange

interactions in LAO/STO that favor the appearances of equal spin. Secondly the g-factors recorded showed fluctuations between ~ 0.3- 3. Fluctuations in the g-factor can either be due to a change in the size of the dot or that the wave functions of the energy levels have different orbital and spin couplings resulting in different g-factors for each level. g-factors resulting from perpendicular and parallel B on the same levels were different which could be a sign of spin orbit coupling. With more recorded data a more complete story could be unveiled. A few results of the gate-tunable superconductivity is also displayed.

7 Outlook

To complete this thesis this section will describe some possible directions for future research. The primary result from this work is the fluctuating g-factors from three complete data sets. From here two paths exists. Either take the design that is working now and measure more dots. Larger statistics will bring out a more complete picture of the underlying physics.

Further research could also pick up from here and improve on the design to make more stable dots. A hint towards better devices has already been observed as leakage from the gates was greatly reduced when the etching of the side-gates was reduced. Initial tests could be made on that type of devices but depending on results it is worthwhile considering alternative ways of avoiding etching the gates. A simple way would be to etch the Hall bars as the first thing. The design would have to be changed to allow room for alignment which using EBL would result in about 50 nm extra free space. Other gate materials or different chemicals for etching could also be explored.

Alternatively a combination of the two fabrication methods could be used. The PMMA fabrication showed that lithography could be made directly on the surface of STO as long as it was treated afterwards. Perhaps it could be possible to use lithography to pattern split-gates on the STO surface. These would have to be accompanied by an oxide like LSM or perhaps SiO_2 to avoid leakage between gate and 2DEG. Following gate fabrication the 2DEG could be defined using PMMA as was done in this work.

8 Acknowledgments

Throughout this work I have had the pleasure of working alongside a bunch of talented and nice people that were a part shaping this project. First of all I would like to thank my supervisor Thomas Jespersen for presenting me with an interesting project and helping me along the way. Thank you to Merlin von Soosten who helped me get familiar with oxide heterostructures and taught me about the dilution refrigerator. Thank you to Damon Carrad for a informative and entertaining corporation in measuring the bulk of the quantum dot data presented here. Thank you to the technical staff Nader, Shiv and Petur who taught me how to use all the different fabrication equipment's and was very engaged in aiding with optimization of fabrications. Thank you to the entire team at Risø for all the work with sample preparations, film depositions and always being welcoming. Finally thank you to Ricci Erlandsen and Rasmus Tindal Dahm for some nice joined trips to Risø and some very focused AFM sessions.

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A Procedure manuals

Following section contains the various procedures that I used during the work for reference.

A.1 Substrate treatment

This procedure was developed by Dennis V. Christensen, Felix Trier and Yunzhong Chen.

Chemical treatment

1. **Preheat water** in an ultrasonic bath to $70°C$ (7/8 filled).
2. **Immerse substrate in EtOH** and sonicate for 5 minutes at RT followed by drying and defect/dirt inspection.
3. **Repeat** step 2 **with acetone.**
4. **Immerse** substrate **in milli-Q water** (or de-ionized-water) and sonicate for 20 min. at $70°C$ followed by drying and defect/dirt inspection.
5. Prepare an $3:1:16$ $HCl(37\%):HNO_3(66\%):H_2O(milli-Q)$ acid solution (e.g. 9ml:3ml:48ml for a total of 60 ml) by adding HCl slowly to HNO_3 (and not visa versa). Let it be for 5 minutes **Immerse** substrate **in acid solution** and ultrasonicate for 20 minutes at $70°C$ and transfer directly to water (step 6). Clean alumina oven boxes with the acid solution.
6. **Immerse** substrate **in milli-Q water** (or de-ionized water) and sonicate for 30 seconds at RT followed by drying and defect/dirt inspection.

Annealing in tube furnace

1. **Place** tube in furnace with ≈ 13 cm of each tube-end outside the furnace. Check the thermocouple with corresponding plug in rear end reaches 50 cm into the tube.
2. **Place** substrate in alumina boxes and insert the box close to thermocouple **in the center of the furnace.** Set the flowrate of oxygen through the tube to ≈ 10 (arbitrary units) with 5-10 bubbles per second in the bubble-bottle (with 500 ml water).
3. **Bake substrate** by ramping $100°C/h$ to $1000°C$ in tube furnace and hold for 1 h then ramp to $25°C$ at $100°C/h$.

A.2 LED exposure cook book

Chip cleaning:

- Submerge for 2 minutes in 50°C Acetone, blowdry with N_2.
- Submerge for 3 minutes in 80°C NMP (N-Methyl-2-Pyrrolidone), blowdry with N_2.
- Spray IPA (Isopropanol) on the chip for a few seconds, then submerge chip in room temperature IPA for 2 minutes, blow dry with N_2.
- Degass on 185°C heatplate for 2 min.
- Microscope inspection.

A quicker version of the cleaning losses the NMP step (as it is mostly to remove resist) and does everything at room temperature.

LED exposures:

- Spin LOR3B on the chip. I use ≈ 100 μL in a syrringe and set the spin coater to 45 seconds with 4000 RPM.
- Bake chip at 185°C for 2 minutes (4 minutes is another possibility, that would result in a smaller undercut). So timing matters with this layer.
- microscope inspection
- Spin AZ1505 on the chip. Same settings.
- Bake chip for 2 minutes at 115°C. After 2 min. the resist should be done and additional time will change nothing.
- Microscope inspection.
- Load sample in LED writer and follow its instructions to the exposure screen.
- Exposure time is the machines version of power output (which is fixed). I used 18 μs for my exposures along with -2 defocus. Settings varies with machine maintenance.

LED Development:

- 1 minute in ambient AZ developer stirred slowly.
- 1 minute in ambient MQ water stirred slowly.
- Blow dry with N_2.
- Microscope inspection.

PMMA Development:

- 45 seconds in ambient PMMA developer (1:3 MIBK) stirred slowly.
- 5 seconds in ambient IPA stirred slowly.
- 20 seconds in ambient IPA stirred slowly.
- Blow dry with N_2.
- Microscope inspection.

Metal deposition:

At QDev we have two AJA systems electron-beam sputteres that I use.

- Load sample and set it to 0°.
- Optional: If the design only covers up some of the chip it is really helpful to cover the other parts with aluminum foil. It is really easy and makes liftoff so easy (no need for two beakers of NMP).
- Deposit 10 nm of Ti. Aim for ≈ 1 Å/s - ususally around 22.5 nA.
- Deposit 120 nm of Au. Aim for the same rate - usually around 45 nA. You can go higher on this step as it takes a long time to deposite 120 nm with 1 Å/s.

Lift off:

- Submerge in 85°C NMP for 1.5 hours.
- Prepare new beaker with NMP and heat it to 80°C.
- Take a pipette (I use 7.5 ml) and spray some of the hot NMP (dont mix the two beakers!) on the chip while it is still submerged. Do this a couple of times, some of the gold (or all) should be removed and floating around in the NMP.
- Move the chip to the other clean NMP beaker. Let it be for 30 minutes.
- New pipette - same procedure.
- Take a small petri dish. Put in enough IPA that the chip will be covered (If the chip is allowed to dry no more lift off will be possible).
- Move the chip to the petri dish.
- Inspect the chip in the microscope while it is in the IPA.
- If all gold is off - blow dry with N_2. If not more time in the NMP can help, but infinite time in NMP wont produce a perfect lift off. If critical parts of the design is free - blow dry and figure out how to make it work. If critical parts of the design is still covered a possiblity is sonication. Sonication is not good for the sample but it is better to try than having a sample that definitely doesn't work.

A.3 Water Treatment

- Ash the sample for 2 minutes.
- Stir the sample in MQ water for 2 minutes.
- Spray with IPA (Do not clean with acetone if using PMMA hard mask!).
- Submerge for 1 minute in IPA.
- Blow dry.

A.4 LSM etch mixing

- Measure up 74 ml of water.
- Weigh out 2 grams of KI. Mix with water and stir with a magnetic stirring pill.
- Measure up 4 ml of 37% HCl. Pour the acid into the water/KI mix.
- Stir for 15 minutes then pour into labeled bottle.

B Resist devices article

Following is the current progress on an article over the results gathered from the single step PMMA fabrication. The plan is to have a complete manuscript prior to the defense of this thesis.

Resist patterning of LAO/STO oxide device.

Anders Bjorlig,[1] Merlin von Soosten,[1,2] Ricci Falke Erlandsen,[1] Rasmus Tindal Dahm,[1] Yu Zhang,[2] Yulin Gan,[2] Wei Niu,[2] Yunzhong Chen,[2] Nini Pryds,[2] and Thomas S. Jespersen[1,*]

[1] *Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, Universitetsparken 5, 2100 Copenhagen, Denmark.*
[2] *Department of Energy Conversion and Storage, Technical University of Denmark, Risø Campus, 4000 Roskilde, Denmark.*

A new approach is presented for designing complex oxide mesoscopic electronic devices based on the conducting interfaces of room-temperature grown $LaAlO_3/SrTiO_3$ heterostructures. The technique uses only existing techniques from conventional semiconductor processing technology and we demonstrate lateral resolution of $\sim 100\,\mathrm{nm}$. We study the low-temperature properties of nanoscale wires and demonstrate the feasibility of the technique for defining in-plane gates allowing local control of the electrostatic environment in mesoscopic devices.

Since the discovery of a two-dimensional conducting electron system (2DES) at the interface between TiO_2 terminated strontium titanatate (STO) and lanthanum aluminate (LAO)[16] the efforts towards exploring, understanding and utilizing the electronic properties of oxide interfaces have attracted a tremendous amount of attention from all branches of physics and material science. One example is the drive towards the integration of oxide interfaces in mesoscopic devices to complement the semiconductor heterostructures and bottom-up grown nanostructures which have been the material platform for two decades of research in quantum transport. The oxide electron systems share the properties of low dimensionality and electrostatic gatability[5] with the conventional semiconductor systems, but in addition display a wide range of phenomena such as gate-tunable superconductivity, ferroelectricity, magnetism and spin-orbit coupling caused by strong electron-electron and electron-lattice interactions in regimes not accessible in the semiconductors [14, 22]. It turns out, however, that in many cases the oxide 2DES is not compatible with conventional fabrication schemes and the oxide 2DES has been shown to be very sensitive to surface processing[4, 23]. A range of specialized fabrication techniques have been developed for patterning the oxide interfaces ranging from patterned growth of the oxide top layer by hard mask techniques[2, 13, 20, 21, 23], ion irradiation[1], thickness variations of the top layer[19], or the creation of conducting nano-structures using scanning probe lithography[6].

Most studies so far have considered crystalline STO-based heterostructure where the top films are deposited at temperatures above $\sim$ 600 °C. Room temperature deposition such as for the amorhous LAO/STO (a-LAO/STO)[7, 12] system also leads to conducting interfaces where electrons predominately originate from oxygen defects[7, 12] and usually exhibit reduced mobilities[8]. The key properties of gate-tunability, and gate-tunable superconductivity[10, 18], however, remain intact and moreover, the highest transition temperature reported for the STO-based 2DESs was achieved in the a-LAO/STO system[17]. Also, recently some of us studied the transport properties of *negative-U* quantum dots devices which were fabricated from a-LAO/STO heterostructures[9, 18]. Thus, the aLAO/STO system provides an interesting system for mesoscopic oxide devices and here we demonstrate that the reduced deposition temperature allows patterning of the interface conductivity by conventional electron-beam or optical lithography. Thus, with only minor adjustments, the recipes developed for conventional processing of semiconductor heterostructures can be directly transferred to the processing of the aLAO/STO interfaces and we explore the limitations of the technique in terms of lateral resolution and the performance of nanoscale devices at low temperatures.

Our fabrication scheme is schematically illustrated in Fig. 1(a). The starting point is a STO substrate with a TiO_2 terminated surface[11] achieved by first sonicating in acetone at room temperature (RT) for 5 min., then for 20 min. in DI water at 70°C and 20 min. aqua regia 3:1:16 HCl:HNO_3:H_2O at 70°C. Finally, following a brief 30 sec. cleaning in DI water the substrates are annealed for 60 min. at 1000°C in a tube furnace and finally cooled to RT at a ramp rate of 100 C°C/hour. Substrates are then spin-coated with PMMA(??) for e-beam(optical) lithography and baked for 45 sec. (??) at 185°C (?115°C) on a hot plate. The PMMA(??) was exposed using standard parameters and the patterns developed in 3:1 MIBK??(??). Before growing the top-layer the samples are cleaned in an oxygen plasma (power and time), and cleaned in water for (time and temperature). It is crucial that exposed surface does not contain any resist residues and previous attempts not including the last cleaning steps have found to lead to insulating samples[23]. We have successfully tested the patterning technique both for optical lithography and e-beam lithography yielding similar results; in the following we present the results obtained using the latter technique. The final PMMA resist profile is shown in Fig. 1(b) and a representative AFM image of the surface terraces in the exposed channel is shown in Fig. 1(c). No discernible differences to the

* tsand@nbi.ku.dk

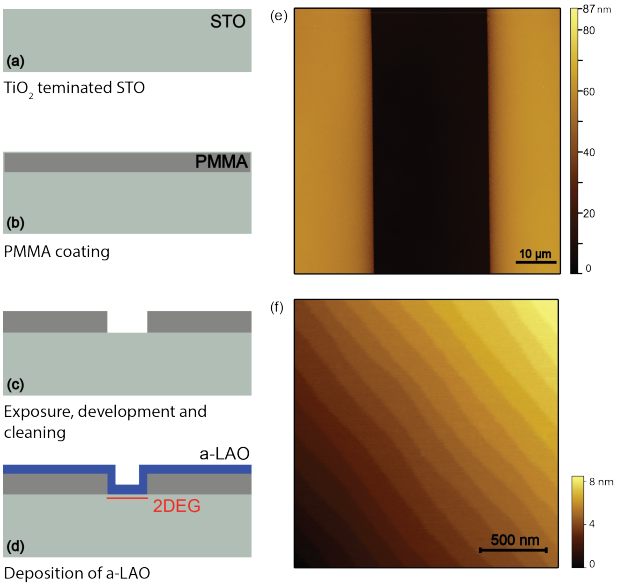

FIG. 1. a) Schematic illustration of the patterning technique. i) An STO substrate is prepared with a TiO_2 surface termination. ii) Surface is spin coated in polymer-based electron or optically sensitive resist and iii) conventional techniques are used for exposure and development, followed by careful clening. iiii) amorphous LAO is deposited on the sample by room-temperature PLD. b) Typical AFM image of a channel after deposition of a-LAO; scale bar is 10μm. c) Typical AFM image of the cannel showing clear STO crystal terraces; scale bar is 500 nm.

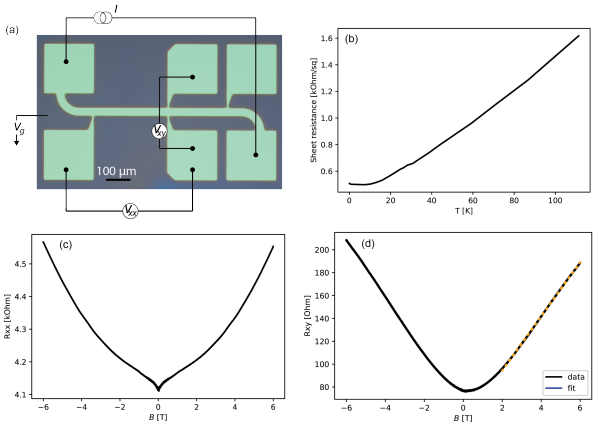

FIG. 2. a) Optical microscope image and schematic measurement setup for a typical sample used for Hall characterization; scale bar is 100 μm. b) Temperature dependence of the sheet resistance showing typical metallic behaviour. c,d) Low temperature Hall characterization yielding a density of $n = 2.45 \cdot 10^{13}/cm^2$ and mobility $\mu = 1180 \frac{cm^2}{V \cdot s}$. d) Gate-stuff coming.

as-treated surface is observed. A top layer of XXX nm a-LAO was grown by room temperature PLD. To investigate the properties of the 2DES induced at the exposed interfaces and the spatial resolution of the lithographical patterning, standard Hall bars samples (Fig. 2) were defined as well as structures allowing four-terminal measurements of leakage currents between parallel wires with varying separations (Fig. 3(a)) and of the conductance of wires of varying width (Fig. 3(c)).

Hall-bar samples were fabricated with width W =? and lengths L = and Fig. 2(a) shows an example of a representative sample after the growth of the top layer. Measurements were performed in a dilution refrigerator with a $\sim$ 20 mK base temperature and standard lock-in techniques using 10 (?) nA current excitation were used to measure the longitudinal V_{xx} and transverse V_{xy} voltage drops as indicated on the figure. The samples were mounted in a using conductive silver epoxy and the overall carrier density was modulated by biasing the conducting back-plane of the sample (V_g). No leakage was measured between neighbouring Hall-samples on chip, and as seen in Fig. 2(b), the sheet resistance $R_S = (W/L)V_{xx}/I$ decreases upon cooling as typically observed for metallic oxide interfaces. The low-temperature dependence of V_{xx} and V_{xy} on a perpendicular magnetic field B_z is shown in Fig. 2(c) and (d), respectively. The positive magnetoresistance in V_{xx} is observed in all(?) samples and has also been reported previously for oxide interfaces and has been attributed to contributions from more than one carrier type

As we find that electrostatic gating irreversibly changes the oxide 2DES[3] the initial measurements (Fig. 2(b-d)) were performed after cool-down and before applying a gate voltage. Figure 2(e) shows the effect of V_g. The sample acts as an n-type semiconductor and resistance drops upon increasing V_g. The V_g-dependence of n nd μ is shown in Fig. 2(?)..

We note, that none of the samples turned superconducting at low temperature. We do not believe that this is a consequence of the patterning technique employed here as also hard-mask devices fabricated at the same time and using the same batches of substrates did not show superconductivity although samples made by this latter technique and measured under the same conditions, have previously exhibited superconductivity[17]. Also, even in unpatterned growth we find variability in when samples exhibit superconductivity. The underlying for this variation remains unknown. Of the XXX? Hall-bars (zzz? patterned using PMMA and the rest by optical lithography) we have measured, ?YYY showed metallic behaviour upon cooling and the resist-based patterning perform similarly to the more involved hard-mask approaches.

The spatial resolution of the patterning technique is crucial for fabrication of nanoscale devices. The pattern can routinely be defined in the PMMA resist with a resolution below 50 nm. The conducting interface is, however, only created upon depositing the LAO top film at

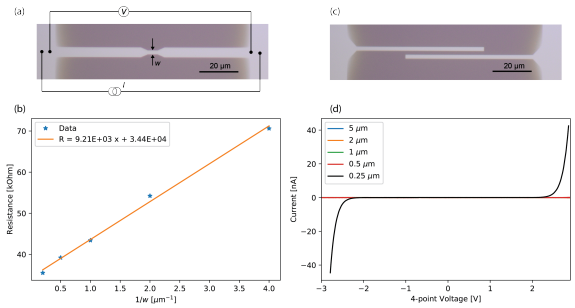

FIG. 3. (a) Optical image of device used to characterize leakage between closely spaced conducting structure. Scale bar is 20 μ m. (b) Corresponding IV characteristics for devices with different separations. No devices shows leakage at low bias and only for the closest spacing of 250 nm is leakage observed for $V_b \sim 2$ V. (c) Optical image of device consisting of a central wire with width W, scale bar is 20 μ m. (d) linear 4-terminal resistance vs W for devices each consisting of 5 identical wires in the geometry of c). The solid lines show fits to simple geometric relations (see text).

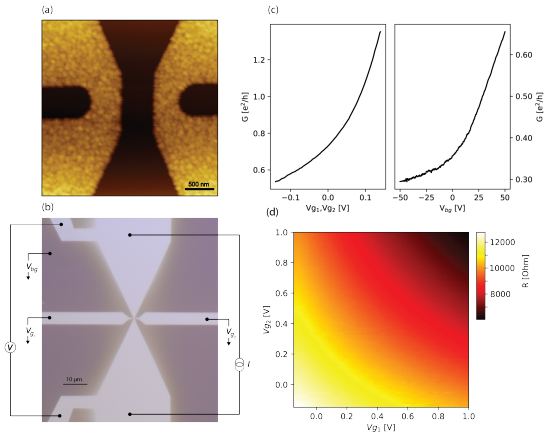

FIG. 4. (a) AFM image of device consisting of a central channels and in-plane side-gates; scale bar is 500 nm. Channel width, sidegate width and spacing between gate and channel was designed to be 500 nm. (b) Optical image of the device showing external circuit; scale bar is 20 μm. (c) *we need to update this caption when we have decided on the content of the figure.* 2D plot displaying the effect of each gate on the resistance of the channel within the maximum range no leak from the side gates. The two side gates show comparable individual effect on the 2DEG with the ability combined to modulate the resistance from 6k Ohm to 12.7 kOhm.

the exposed regions and depending on the ability of the plasma cleaning step and of the plasma of the PLD to enter nano-scale patterns in the ? nm thick mask layer (Fig. 1(b)) the resulting conducting areas may be smaller than the resist openings. On the other hand, since the interface conductivity is presumably a result of oxygen vacancies created when depositing the top layer, and that the oxygen diffusion length may be significant, this could lead to conducting regions extending beyond the resist openings. Thus in the case where either of these mechanism are significant, the actual resolution would not be set by the resolution of the lithography. To investigate this, two types of devices were fabricated allowing four-terminal measurement of 1) the leakage currents between sets of parallel wires with varying separations $5, 2, 1, 0.5, 0.25\,\mu$m between the resist openings (Fig. 3(a)), and 2) the conductance of wires defined with varying widths $4, 2, 1, 0.5, 0.25\,\mu$m (Fig. 3(b)). Considering first the leakage, all wire separations shows negligible leakage currents up to a bias voltage of $|V_{bias}| < 2$ V both at room temperature and low temperature. For the smallest separation of 250 nm clear leakage turn-on is observed for $|V_b| \sim 2$ V. From AFM inspection of the resist profiles, the edges of the openings have a roughness of about XX?, and as measured leakage will be dominated by the points of thinnest separation of the two wires and, we conclude that the conducting region extends at most ? nm beyond the resist openings and presumably much less.

Figure 3(d) shows the resistance of the devices as a function W To reduce errors due to inhomogeneities, each device consists of 5 identical wires in parallel. In the simplest case we expect $R = [L/(W + W_0) + 10]R_{sq}$ where R_{sq} is the sheet resistance of the 2DES and the second term accounts for the resistance of the wide pads (aspect ratio of 10) connecting to central narrow wire. The black line shows one parameter fit fixing $W_0 = 0$ which gives a satisfactory description of the data with $R_{sq} =?$. The red lines shows a fit taking W_0 as a fit parameter yielding $W_0 =??\pm??$. Thus within the experimental accuracy we width of the conducting region is consistent with the width of the resist openings even for the most narrow wires. To summarize, the results of Fig. 3 shows that within an uncertainty of about ... nm (given by the roughness of the resist openings defined by the lithography) the conducting regions in the interface reproduces the lithographically defined openings in the resist mask. Local electrostatic control is an important element in most mesoscopic devices such as quantum dots and quantum point contacts (QPC). Local gates are usually defined by capacitively coupled metallic top electrodes isolated from the electron system by an oxide. Alternatively, to avoid possible damage due to processing on the samples after the growth of the top-layer, metallic gates can either be used as a part of the mask structure[18] or nearby regions of the 2DEG itself can be utilized as a gate[9, 15]. Figure 4 demonstrate the latter approach using the PMMA as patterning mask for defining a 500?? nm wide channel with nearby 2DEG side-gates in a QPC geometry similar to that studied in Ref. [15]. The separation between the gates and the channel was 500? nm. The response as a function

of the applied voltage to the two gates and back-gate is shown in Fig. 4(c)-(d) for a temperature of 20 mK. An interesting regime is that close to pinch-off where only a few channels contribute to the transport and phenomena such as quantized conductance is expected. For all three gates the conductance significantly decreases with lowering gate potential as the channel is depleted of carriers. The gate-efficiency, however, progressively decreases at lower V_g and eventually G saturates. This is attributed to the field dependent dielectric constant of STO[15]. The side gates can be operated at voltages down to $\sim$? V at which point they start to leak to the main channel. Although the device is operated in the regime close to pinch-off no quantization of conductance nor signatures of conductance fluctuation was observed. This is similar to previous reports (cite goswami nano let) and indicates that the current is carried by many weakly transmitting transverse modes. Systematic investigations of device geometries varying the potential steepness around the channel is may shed further light on this.

In conclusion we have presented a new patterning approach for the fabrication of mesoscopic devices from STO-based heterostructures with room-temperature grown top layers. The technique utilizes conventional polymer resists sensitive to either electron or optical exposure and allows for patterning with a resolution of at least 250 nm without affecting the quality of the 2DES. Finally we demonstrated devices implementing local electrostatic gate-control of the carrier density in narrow constrictions. The various aspects of the patterning approach were demonstrated using room-temperature grown amorphous LAO as top-layer of the oxide heterostructure, however, also alternative STO-based conducting room-temperature grown interfaces have been reported[8, 10], and we expect that the techniques reported in this study may be directly applied to such systems as well.

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