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Investigating Majorana Zero Modes in Two Dimensional Electron Gas Based Nanowires with a Multiple Probe Experiment

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Abstract

This thesis reports experimental findings of tunnelling spectroscopy measurements performed in mesoscopic devices formed in a two dimensional electron gas. The devices investigated are quasi one-dimensional indium arsenide nanowires proximitized by aluminium. The wire has multiple segments, each tunable with a separately controlled electrostatic gate. Tunnelling spectroscopy is performed at the middle and at the ends of these segments to infer the density of states in the wire. The aim of the experiment is to investigate Majorana zero modes, which are zero energy states that emerge at boundaries and defects of topological superconductors. Topological superconductivity is induced within the device by tuning the chemical potential and magnetic field.

Contents

List of Figures

vi

Introduction

This thesis is a work in experimental solid state physics, exploring a particular state of matter called topological superconductivity. Fundamental research in this area has rapidly expanded in the past decade with the anticipation of discovering physical phenomena that have theoretically been predicted to enable topological quantum computation [1].

Chapter 2 explains the motivation behind topological quantum computation and introduces the ingredients needed to construct such a computer. Majorana zero modes are introduced as the basic building blocks of a topological qubit and we explain how we attempt to create them. We describe the materials that we use and how we intend to build the devices to be measured. Finally, we elaborate on the experimental goals of this work and emphasize how the measurements performed on these devices contribute to the field.

Chapter 3 describes how the devices are fabricated and how measurements are performed on them. We also introduce the basic operating principles of the equipment used in this experiment and explain how they enable measurements that give us in-

formation regarding device properties that we are interested in.

Chapter 4 reports the main results of this work and demonstrates the improvements and conclusions made, based on the data gathered. We also compare the results to theoretical predictions and previous experimental findings from relevant research performed by others.

Chapter 5 concludes the results and offers suggestions to benefit future experiments that relate to this work.

The devices presented in this work were fabricated by Andreas Pöschl. Measurements were performed and discussions were held in collaboration with Andreas Pöschl, Deividas Sabonis and Alisa Danilenko.

CHAPTER 2

Theoretical background

2.1 Motivation - topological quantum computing

Quantum computing is an area of intense research because it promises more powerful computers that can solve certain problems exponentially faster than classical computers [2]. Such solutions would have widespread application in chemistry [3, 4], cryptography [5], and many other areas [6]. The central idea of quantum computation is to utilize superposition [7]. This is a quantum mechanical phenomenon, which is inaccessible to modern classical computers and incompatible with their basic operating principle.

The logical state of a modern classical computer is encoded in a sequence of binary-valued bits. In a computation, an output is retrieved by decoding the state of the computer after some algorithm has manipulated a given input. Every step of the algorithm is deterministic, in the sense that when we query the state of the computer, the result is uniquely determined by the specific computational step that the query was made at, even if the program is run on a different classical computer. Moreover, if done intelligently, checking the state of the computer does not change that state,

nor does it modify the result of the subsequent computation. This is important, because it allows us to copy the states, compare them for errors and correct for them [8].

In contrast, a quantum computer is in a superposition of logical states, which could be encoded with qubits, that are each in a superposition of two orthogonal quantum states. Quantum algorithms need not be deterministic, meaning that there are situations in which queries regarding the state of the computer return an inherently random answer. The probability distribution of the output can be obtained by repeating the computation multiple times. The power of quantum computing is, that as certain computational problems are scaled, the amount of time needed to sample this distribution becomes much smaller than the time needed for a classical computer to calculate it. This was recently demonstrated by Google [9], although contested by IBM [10]

The error-correcting procedures implemented on classical computers cannot be straightforwardly applied to quantum computers because copying the state of a quantum computer is impossible due to the no-cloning theorem [11, 12]. Nonetheless, quantum error-correcting schemes do exist, but they can only function if the rate of errors made by the quantum computer is below some certain threshold [13, 14, 15]. Errors can arise from either interactions with the environment or from performing quantum operations imprecisely during the computation.

Interactions with the environment are often out of our direct control. For example, it could be a mechanical vibration in the system caused by sound or heat, or an unwanted magnetic field penetrating an accidental loop in our wires or perhaps a cosmic ray [16] originating from another galaxy that coincidentally strikes a qubit during a computation. Any such interaction represents an additional degree of freedom for the quantum mechanical system. As time passes, those interactions take place and the corresponding degrees of freedom will contain an increasingly substantial part of the information that we encoded into our initial quantum state. That information is lost to us because our measurement apparatus is necessarily restricted to only those dimensions that we can control, measure and understand.

Leaving a quantum computer open to the environment will eventually take the probability distribution into the thermal ground state of the system, leaving the information that we hoped to obtain entirely unaccessible to our measurement scheme. This process is known as decoherence and it is a major issue for all of the quantum computers existing today. It represents an upper time limit for a successful computation, which in turn limits the number of total operations that a quantum computation can involve, given that those operations cannot be done arbitrarily quickly without losing precision. As examples, this timescale is currently on the order of microseconds for superconducting qubits [17] and up to hours for ionized donors in silicon [18]. As more qubits are added to a computer, the decoherence time decreases even further, dependent on the particular type of qubit involved. Finding a scalable platform that enables a long decoherence time is a necessary criterion for a universal quantum computer [19].

Even if a quantum computer were perfectly isolated from the environment, the errors stemming from performing imprecise operations remain. The reason why this is a problem for quantum computers is that the coefficients of the qubit states vary continuously, making them dependent on even the smallest variations in operation. For instance, if a qubit is controlled by microwave pulses, then a slight variation in the frequency or duration of the pulse would result in a state that slightly differs from the desired one. This is in contrast with a classical computer, where only a sufficiently large mistake would cause a bit flip. Even if the errors that individual quantum operations make are small, they accumulate with each step of the algorithm and may noticeably distort the final result for a sufficiently long computation [20].

For many quantum computing platforms, it may be possible to alleviate both of these problems with better material systems and clever engineering, however it is too soon to determine which platforms will prove most successful. This thesis is focused on fundamental experimental research in solid-state physics, that hopefully brings us closer to realizing a particular approach called topological quantum computation [21, 22, 23]. No topological quantum computers have been successfully built yet, but the approach is promising and interesting because it attempts to bypass the problems introduced above in a unique and reliable way.

The starting point of topological quantum computation is to consider a configuration of identical particles that reside in a degenerate ground state. Each of these ground states represent a logical state for the computer and can physically be distinguished by some internal quantum number which is somehow encoded amongst the particles. In specific proposals for this type of computer, this internal quantum number is a topological invariant, hence giving the approach the name of topological quantum computing. The user of such a computer can initialize a known ground state by creating those particles in a specific manner. Unitary operations within the manifold of ground states can be performed by exchanging those particles. After some sequence of these exchanges, called braids, the user would perform a measurement on the superposition of ground states by fusing the particles back together in a process that resembles the initialization step in reverse [21].

The power of this approach stems from the property that when performing a braid, the precise paths taken by the particles are not important as long as they can be continuously deformed to each other, as depicted in Figure 2.1. This directly makes small variations of the paths caused by imprecise hardware irrelevant. Additionally, particles could be braided without ever having to be physically close to each other. If they are always located far away from each other, then the probability of the environment accidentally exchanging them is exponentially suppressed.
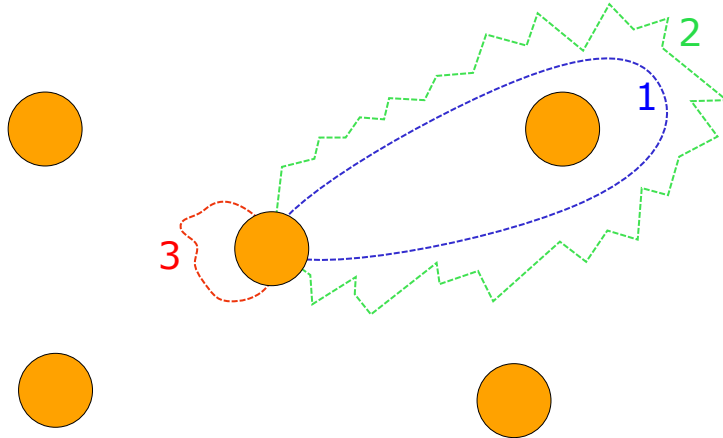
Figure 2.1: A collection of non-Abelian particles, depicted as orange circles on a 2D plane. Three possible closed paths for the central particle have been drawn and labeled 1 (blue), 2 (green) and 3 (red). Moving one particle around another, for instance by traversing paths 1 or 2, changes the quantum state of the system. Since paths 1 and 2 are topologically equivalent, taking either path yields the same quantum state, up to a phase factor of the many-body wavefunction. Traversing path 3 retains the quantum state, because it does not encircle any particles and is therefore topologically equivalent to a null path.

This setup is quite peculiar because bosons and fermions, which are the only possible types of particles in three dimensions, do not possess the properties described above. Namely, when exchanging bosons, the many-body wavefunction does not change at all and when exchanging fermions, it is merely multiplied by a phase factor of π. The particles that have the necessary properties are called Non-Abelian anyons and can only exist in two-dimensional systems [24]. The term anyon means that the phase picked up by the wavefunction during an exchange can have any value, instead of just 0 or π. Anyonic exchange statistics have recently been observed in experiments [25, 26, 27]. The term Non-Abelian means that the order, in which particle exchanges are executed, has significance. Performing the same exchanges in a different order may result in an entirely different many-body wavefunction. This property is what provides the ground state degeneracy and it has not yet been observed in an experiment.

Even though the topological quantum computation approach alleviates the problems introduced before, some sources of decoherence still remain. For instance, thermal energy could add unwanted particles to the system, which may braid or fuse with the anyons. To avoid thermal quasiparticle excitations, it is necessary to use a material system where the ground states are energetically gapped from the excited states, such that the energy gap is larger than the thermal energy at experimentally accessible temperatures. If such a system was built, it could in principle achieve the level of fault-tolerance that is required by the error-correcting procedures necessary for a universal quantum computer.

2.2 Topological superconductivity

Non-Abelian anyons have not been found to exist as elementary particles in nature, but there are proposals for condensed matter systems where they may emerge as quasiparticle excitations [28]. The quasiparticles that this thesis studies are Majorana zero modes, which appear on boundaries of topological superconductors. This section introduces the basics of superconductivity [29], the model of a one-dimensional topological superconductor [30] and the approach taken to realize this model in a semiconductor-superconductor heterostructure [31, 32].

Superconductivity is a state of matter that conducts electricity with no resistance. It was first observed in 1911 by Heike Kamerlingh Onnes [33] and has since been found in a plethora of materials [34]. For many of these materials, superconductivity can be understood through the microscopic theory put forward by Bardeen, Cooper and Schrieffer (BCS theory) [35].

In the BCS theory of superconductivity, charge carriers pair up into Cooper pairs due to electron-phonon interaction. As an electron moves through a lattice of atoms, it attracts the positively charged ions near its path, thereby creating a lattice vibration called a phonon. A different electron with opposite momentum would be attracted to this phonon, meaning that the two electrons essentially attract each other, despite being repelled by regular electrostatics. At a sufficiently low temperature, called

the critical temperature T_c[1], the pairing potential supplied by this attractive mechanism becomes comparable to the thermal energy, meaning it becomes energetically favourable for the electrons to pair up with partners that have opposite momentum. Additionally, this mechanism makes it energetically favourable for the electrons to have opposite spin, such that their spatial overlap does not compete with Pauli's exclusion principle. These pairs of particles are called Cooper pairs.

Cooper pairs can be treated as a type of particle in their own right, carrying a charge of two electrons while having zero kinetic energy, momentum and spin. From these properties it follows, that they all occupy the same ground state, known as the Cooper pair condensate, regardless of how many Cooper pairs are present in the system. A conventional superconductor can be described within this framework with an approximate[2] Hamiltonian

$$H = \sum_{k\sigma} \left[\varepsilon(k) c_{k\sigma}^\dagger c_{k\sigma} - \left(\Delta_k c_{k\sigma}^\dagger c_{k\bar\sigma}^\dagger + \Delta_k^* c_{k\bar\sigma} c_{k\sigma} \right) \right] \tag{2.1}$$

where k is momentum, $\sigma \in \{\uparrow, \downarrow\}$ is spin and $c^\dagger$ and c are the respective creation and annihilation operators of electrons. The first term describes the energy $\varepsilon(k)$ of free electrons, measured with respect to the chemical potential μ. The pairing potential Δ appearing in the second term shows how much energy is gained from combining electrons or holes into Cooper pairs. A superconductor hosts no states within the energy range $\mu - \Delta$ to $\mu + \Delta$, because any such particles will find it energetically favourable to pair up. The width of this energy range 2Δ is called the superconducting gap and for conventional superconductors, its value at zero temperature approaches a limiting value [29]

$$\lim_{T \to 0} \Delta = 1.764 k_B T_c \tag{2.2}$$

where k_B is the Boltzmann constant. The density of states $\rho(E)$ outside the gap is

$$\rho(E) = \frac{E}{\sqrt{E^2 - \Delta^2}} \quad \text{for } |E| > \Delta \tag{2.3}$$

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[1]This threshold depends on the material. In many materials, superconductivity has never been observed.

[2]Mean field approximation $c_{k\uparrow}^\dagger c_{-k\downarrow}^\dagger c_{-k'\downarrow} c_{k'\uparrow} \simeq \langle c_{k\uparrow}^\dagger c_{-k\downarrow}^\dagger \rangle c_{-k'\downarrow} c_{k'\uparrow} + c_{k\uparrow}^\dagger c_{-k\downarrow}^\dagger \langle c_{-k'\downarrow} c_{k'\uparrow} \rangle - \langle c_{k\uparrow}^\dagger c_{-k\downarrow}^\dagger c_{-k'\downarrow} c_{k'\uparrow} \rangle$. The error introduced by this approximation is second order in deviations of $c_{k\uparrow}^\dagger c_{-k\downarrow}^\dagger$ and $c_{-k'\downarrow} c_{k'\uparrow}$ from their averages

For concreteness, the description so far has mostly been formulated with electrons, but it is equally relevant for holes. In fact, there is no meaningful distinction between an electron and a Cooper pair combined with a hole. Curiously, neither electrons nor holes are eigenstates of the Hamiltonian (2.1). Instead, the elementary excitations in a superconductor are Bogoliubons γ, which are a superposition of the two and can be expressed through the electron creation and annihilation operators:

$$\gamma_{k\uparrow} = u_k c_{k\uparrow} - v_k c^{\dagger}_{-k\downarrow} \tag{2.4}$$

$$\gamma_{k\downarrow} = u_k c_{k\downarrow} + v_k c^{\dagger}_{-k\uparrow} \tag{2.5}$$

where the coefficients u and v are called the quasiparticle charges of the electron-like and hole-like components respectively. This can be shown by finding that for certain values of u and v, the Hamiltonian (2.1) is indeed diagonal in the basis of γ operators [29]. For energies above the chemical potential, the Bogoliubons are more electron-like and for energies below, they are more hole-like. A Bogoliubon with zero energy (residing precisely at the chemical potential) is an equal superposition of an electron and a hole.

Now we will consider a simplified version of a superconducting system known as the Kitaev chain [30], which is represented visually in Figure 2.2. This system has three simplifying properties:

1. The superconductor is a one-dimensional chain of discrete sites that can each be occupied by a fermion f. We will denote these sites with an index j. The chain has a finite length, expressed by the total number of sites L.

2. The fermions in this system are spinless. They still obey fermionic statistics, but are just missing a degree of freedom in spin, meaning that each site is limited to one fermion instead of two, following Pauli's exclusion principle.

3. Each fermion only interacts with their nearest neighbouring sites. This interaction can mean pairing up with an adjacent fermion into a Cooper pair. Fermions can also tunnel from one vacant site to another. The strength of these processes are described with a pairing potential Δ and a tunnelling amplitude t respectively.
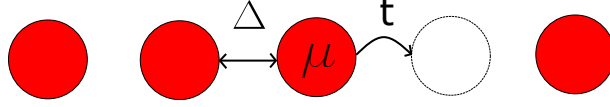
Figure 2.2: A kitaev chain with length $L = 5$. Four occupied sites have been colored red and one unoccupied site has been colored white. The middle site has been marked with the three parameters of the model. The chemical potential μ is the energy required to occupy the site. The tunnelling amplitude t describes the probability for the fermion in the middle to move to the unoccupied site on the right. The pairing potential Δ is the interaction energy between the two neighbouring fermions.

The Hamiltonian for such a system is [36]

$$H = \sum_{j=1}^{L} \left[-t \left(f_j^\dagger f_{j+1} + f_{j+1}^\dagger f_j \right) - \mu \left(f_j^\dagger f_j - \frac{1}{2} \right) + \left(\Delta^* f_{j+1}^\dagger f_j^\dagger + \Delta f_j f_{j+1} \right) \right] \quad (2.6)$$

Generally, the fermionic operators f are complex and can (purely mathematically) be split into real and imaginary parts

$$f_j = \frac{e^{-i\theta/2}}{2} \left(\gamma_{2j-1} + i\gamma_{2j} \right) \quad (2.7)$$

to define operators γ, which are real and therefore Hermitian $\gamma^\dagger = \gamma$ by construction. These are called Majorana operators, because they satisfy the Majorana equation [37], which is the real-valued version of the Dirac equation. The factor $e^{-i\theta/2}$ contains the superconducting phase θ defined by $\Delta = |\Delta|e^{i\theta}$ and is included in this definition purely for convenience, such that the subsequent equations have a simpler form. Rewriting the Hamiltonian (2.6) using the definition (2.7) yields

$$H = \frac{i}{2} \sum_{j=1}^{L} \left[-\mu \gamma_{2j-1}\gamma_{2j} + (t + |\Delta|)\gamma_{2j}\gamma_{2j+1} + (-t + |\Delta|)\gamma_{2j-1}\gamma_{2j+2} \right] \quad (2.8)$$

This Hamiltonian could be interpreted as describing a chain of $2L$ Majorana particles, that interact with their neighbours. The values of the parameters μ, t and Δ determine the relative strengths of precisely which neighbours each mode interacts with. In a limiting case, where t and Δ are equal in magnitude and both much larger than μ, the Hamiltonian approximately becomes

$$H = it \sum_{j=1}^{L} \gamma_{2j}\gamma_{2j+1}, \quad t = |\Delta| \gg \mu \quad (2.9)$$

In this limit, only the Majorana modes indexed by $2j$ and $2j + 1$ interact with each other, forming new fermionic modes defined by

$$\tilde{f}_j = \frac{e^{-i\theta/2}}{2} \left(\gamma_{2j} + i\gamma_{2j+1} \right) \tag{2.10}$$

This type of pairing means that the Majorana modes at the ends of the chain γ_1 and γ_{2L} have been left unpaired. We can formally pair them with each other by constructing a special non-local fermionic operator to describe them:

$$d = \frac{e^{-i\theta/2}}{2} \left(\gamma_1 + i\gamma_{2L} \right) \tag{2.11}$$

The absence of this operator from the Hamiltonian (2.9) means that the corresponding fermionic mode has zero energy, prompting the name Majorana zero modes for γ_1 and γ_{2L}. This property is independent of whether the non-local fermionic mode is occupied $d^\dagger d = 1$ or unoccupied $d^\dagger d = 0$. Therefore, in this regime, the ground state of the system is doubly degenerate. This situation is already reminiscent of the starting point for a topological quantum computer - a degenerate set of ground states that differ by a quantum number (in this case $d^\dagger d = \{0, 1\}$) non-locally encoded amongst the particles in the system. This would imply that the Majorana zero modes are expected to exhibit Non-Abelian exchange statistics [38], but this remains yet to be shown experimentally and is a major milestone towards building a topological quantum computer [39]. The notion of exchanging particles without merging them in a one-dimensional chain seems ill-defined, but it could be performed within a network of such chains [40]. It is even possible to design these networks in a scalable manner [41].

To experimentally investigate Majorana zero modes, we have to engineer a material system in which the Hamiltonian 2.9 is realized. There are obviously many limitations to how closely it is possible to mimic the Kitaev model in an actual device. One of the most important conditions is the second simplification introduced in the model - that the fermions ought to be spinless. Without this property, there can be no unpaired Majorana modes, since every site on the chain could be doubly occupied. One way to achieve this is to create a hybrid semiconductor-superconductor structure, that inherits properties from both of the materials simultaneously. Under the right circumstances, the semiconductor can remove the spin degree of freedom and the superconductor can supply superconductivity and the energy gap that comes

along with it. This approach was proposed theoretically in 2010 [31, 32] and has been studied in numerous experiments since then [42].

The first ingredient in this scheme is a semiconductor that exhibits a strong spin-orbit effect. This effect is a relativistic interaction between the spin of a charge carrier and its motion inside a potential [43]. Namely, as a result of relativistic electrodynamics, an electric field is experienced by a moving object as a magnetic field in the reference frame of that object. Consequently, if that object possesses a magnetic moment, then traversing through an electric field causes that magnetic moment to align with the perceived magnetic field. The magnetic moment of an electron is generated by its charge and spin, which means that the spin-orbit effect ties the spin of an electron to its motion through the material in which it is travelling. The magnitude of this effect is dependent on the material, and is generally larger in crystals composed of heavy elements, such as indium arsenide (InAs). The electric field can be supplied by external electrostatic gates or it could originate from the gradient of the confining potential created by band alignment in a grown heterostructure [44].

The spin-orbit interaction makes it energetically favourable for charge carriers with opposite momenta to have opposite spins. Nonetheless, at any given energy, it is still possible to have the energetically disfavoured orientation of spin at the cost of having lower momentum, so this system is not yet spinless. An additionally applied external magnetic field can modify the energy levels even further, opening up a window of energy within which either direction of momentum allows precisely one possible orientation of spin. Within this region of energy, the spin degree of freedom is effectively removed because it is locked to the momentum degree of freedom. This regime can be accessed by tuning the chemical potential of the semiconductor to be within that region, for instance by using electrostatic gates.

The second ingredient is superconductivity, which can be introduced into the semiconductor near the interface where it connects to a superconductor. This ability of a superconductor to share its properties is called the proximity effect, which is made possible by the electrons near the interface having a wave function that extends into both materials over a finite range. Recently, it has become possible to make epitaxi-

13

ally matched semiconductor-superconductor interfaces with molecular beam epitaxy [45]. The epitaxial match between the two ensures minimal disorder at the interface, which in turn enables the system to possess a hard gap [46] - a feature that was previously unobtainable due to interface inhomogeneity [47].

The properties of the superconductor set some stringent experimental conditions. First, superconductivity only manifests itself at low temperatures, which requires the experiment to be carried out within a cryostat. Second, the magnitude of the superconducting gap decreases with the applied external magnetic field, which means that the topological superconducting phase can only be observed in a particular range of magnetic field strength, bounded from above by the vanishing gap of the superconductor and bounded from below by the requirements set by the spinless regime of the semiconductor. Last, since the aim is to create a nanowire (ideally approximating a 1D wire), the materials and designs of experimental devices need to be compatible with the available methods of nanofabrication.

2.3   The experiment

Performing quantum computation with Majorana zero modes is a complex task and cannot be reliably performed without experimentally establishing how to perform numerous subtasks first. The experiment described in this thesis is designed to investigate the creation, detection and manipulation of a single pair of Majorana zero modes in various segments of a nanowire. The remainder of this section elaborates on how the design of the experiment enables us to do those that.

In this experiment we aim to create topological wire segments in a two dimensional electron gas (2DEG). A 2DEG is a layer of electrons that have been confined in the third dimension within a quantum well. To engineer this confinement, a stack of various materials is grown with molecular beam epitaxy. All of the data presented in this thesis is from devices created from a single wafer of material, grown by the Manfra group at Purdue university. The various layers and their dimensions are shown on Figure 2.3. Near the top of the stack is a thin layer of InAs which is sandwiched by thin sheets of InGaAs. The layers of InGaAs have a higher bandgap than InAs,

14

thereby creating a confining potential well around the InAs [48]. A smaller quantum well results in larger spacings between energy levels within the well. The width of the InAs layer is 7 nm, which is much smaller than the Fermi wavelength within the material, resulting in only one energy level being occupied. This effectively removes the third dimension for the electrons in the well, thereby forming the 2DEG. Beneath the lower layer of InGaAs are multiple layers of InAlAs with various ratios of indium and aluminium. The purpose of these layers is to create a gradually changing lattice spacing that can connect the quantum well with the InP substrate, while providing a large potential barrier to ensure that electrons are unable to tunnel from the quantum well into the substrate. Above the upper InGaAs layer is a layer of aluminium, which is there to provide the superconductivity to the 2DEG via proximity effect. The thickness of that InGaAs layer determines the interface transparency, which regulates the proximity effect [44].
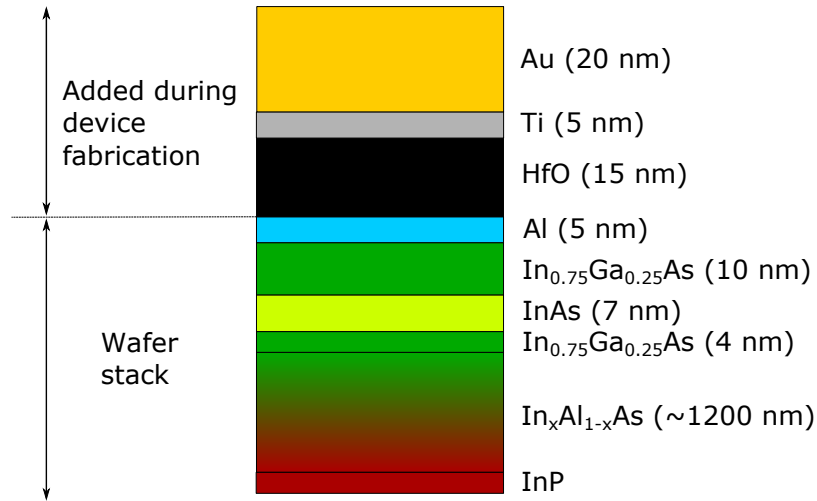
Figure 2.3: The material used for the experiment. The portion labelled wafer stack is entirely grown in a molecular beam epitaxy chamber. During device fabrication, detailed in Chapter 3, some of these layers are removed and others are added for different regions of the devices.

During device fabrication, more thoroughly described in Chapter 3, a narrow wire is patterned out of the aluminium by selective etching. Additionally, gold electrostatic gates called plunger gates are deposited to cover multiple segments of that aluminium

wire and its immediate surroundings. Figure 2.4 shows a false coloured scanning electron micrograph of a complete device, where the placement of these gates can be seen, coloured in red. The gates are separated from the other layers below by an insulating layer of hafnium oxide.
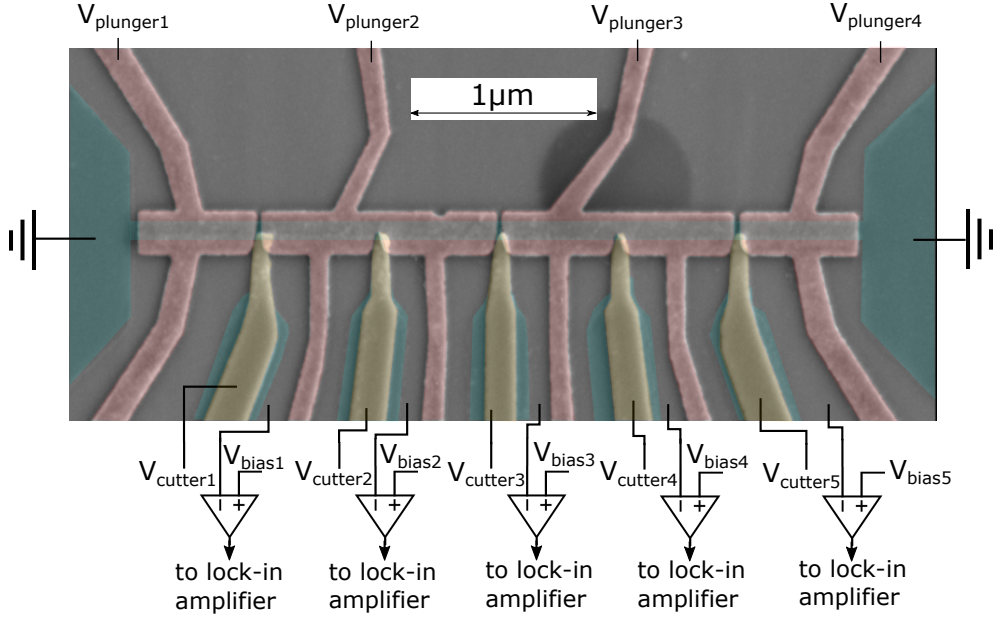
Figure 2.4: Image of a finished device, taken with a scanning electron microscope. Colours have been added for clarity. Coloured in teal are the visible areas of the device where the aluminium has not been etched away. The approximate location of the main wire has also been coloured teal on this image, although it is not visible from the original image. Coloured in gold are cutter gates and coloured in red are plunger gates. The cutter gates were deposited first and are separated from the plunger gates by a layer of dielectric. Slight overlap of the gates is visible at the junctions. Electrical lines have been schematically marked. A more detailed electrical circuit can be seen in Figure 3.4.

The voltages of the plunger gates can be controlled externally and serve three distinct purposes. First, setting a negative voltage for a gate (on the order of -1 V) depletes the 2DEG directly underneath it by field effect. However, the region of 2DEG directly underneath the aluminium wire is protected from this effect, because the electrons in

16

the wire screen the electric field of the gate. This region of 2DEG forms a nanowire - confined vertically by the InGaAs layers and confined horizontally by the electrostatic gate. This nanowire exhibits a strong spin-orbit effect due to the InAs and also inherits superconductivity from the aluminium from above, giving it all the necessary prerequisites for hosting Majorana zero modes [49].

The second function of the plunger gates is to insulate certain regions of the device from each other. The same electrostatic depletion that forms the wire can be used in other areas to make a conducting region of 2DEG insulating instead. The long appendages of the plunger gates that can be seen on Figure 2.4 partition the 2DEG into five probes that approach the nanowire from the side. Each probe can be individually biased with a voltage, which enables us to perform tunnelling spectroscopy. Tunnelling spectroscopy is a method that enables us to infer the density of states in the wire at the points in which the probes are situated and is further elaborated on in Chapter 3. To aid this measurement, there are indentations at the middle and ends of the plunger gates, which allow for a some conductance between the probes and nanowire. For even more precise control, additional gates called cutter gates are also deposited during fabrication. The effect of the cutter gates is screened by the aluminium on the probes with the exception of their tip, where their role is to regulate the electrostatic landscape between the probes and nanowire.

The third function of plunger gates is to tune the chemical potential within the nanowire. Even though the aluminium screens the electric field from above, the wire is still responsive to electrostatic depletion from the sides. This means that the gate is able to tune the chemical potential, while never completely depleting the wire. The tunability of chemical potential is necessary to enable the condition of Equation 2.9 to invoke the transition of the wire into the topological superconducting phase and thereby create Majorana zero modes.

Since Majorana zero modes reside at zero energy, the presence of one is reflected by an increase in the density of states at zero energy. For tunnelling spectroscopy measurements, this translates into an increase in zero bias conductance by $2e^2/h$ [50]. In this experiment, we can individually tune the chemical potential in each segment of

the wire and attempt to detect the presence of Majorana zero modes with the probes situated on the ends of those segments.

Observing a known feature of an object may be enough to detect it, but in many cases can be insufficient to actually conclude the existence of that object. Numerous other effects may produce a zero bias peak, such as Kondo effect [51], weak antilocalization [52], reflectionless tunnelling [53] or the presence of quantum dots and random disorder in the chemical potential [54]. To obtain the capability to distinguish between the different origins for zero energy states, the experiment includes an additional tunnelling probe in the middle of each wire segment. The information supplied by this middle probe is twofold. First, if it does happen to detect zero energy states, then we can have a higher level of confidence that those occurrences are not Majorana modes, because we have deliberately placed that probe in a location where we do not create the conditions for one to appear. This in turn may aid us in analysing the data from the end probes, since it gives a baseline for how many false-positive Majoranas usually occur and what they may look like in terms of shape, magnitude and response to gates in measured differential conductance. Second, even though we expect no Majorana mode to be created in the middle of a segment, the entire segment still undergoes a topological phase transition, which could also be detected by the middle probe. Namely, the excitation gap is expected to momentarily close within the entire wire at the specific values of magnetic field and chemical potential where the transition occurs [55]. If this theoretical prediction holds true for our physical system, then every additional tunnelling probe in the middle of a wire adds a degree of falsifiability to the hypothesis that an observed zero energy state was created in conjunction with a topological phase transition that spans the entire wire. This helps to corroborate observations of Majorana zero modes and to reject effects that coincidentally mimic the signatures at both ends of the wire simultaneously.

Having separate control of chemical potential in each segment allows us to deliberately attempt to join or split two topological segments. Whether or not that actually succeeds could most readily be observed with the probe located directly between the two. If one segment is topological and the other is not, then the probe would observe a Majorana zero mode there. If the segments are both topological and form one large

topological region, then this probe would effectively become a middle probe and it would be able to observe a gap closing and reopening but no Majorana zero mode. If the segments were both topological, but still remained slightly separated, this probe could still observe the Majorana modes, possibly no longer at zero energy - a finite overlap of nearby Majorana wave functions would supply them with an interaction energy [56, 57]. Consequently, observing these differences in the behaviour of this probe would let us infer when these joining or splitting processes occur.

Being able to split and join topological segments would even enable us to perform more complex operations with the Majorana zero modes. For instance, if we create two separate topological segments and later join them through segments situated in between, we could fuse two Majorana zero modes that were not initially created as a pair [40], which is one of the basic capabilities needed to create a topological qubit [21]

CHAPTER 3

Experimental methods

3.1   Fabrication and preparation of devices

Experimental devices are fabricated onto 3x5 mm chips. To obtain a chip, the outline
of the chip is scribed onto the wafer (grown in Purdue) using a diamond tip and subse-
quently cleaved off by applying slight mechanical pressure with tweezers. Devices are
fabricated onto the chip through a scalable fabrication process. Typically, around 12
devices are made on a single chip. All of these devices are made simultaneously, which
means that making more devices or even making devices that have more complex ge-
ometries does not necessarily make the fabrication process longer or more difficult.
The number of devices per chip is instead limited by the total number of bonding
pads on the chip. A bonding pad is a region on the chip that is used to make an
electrical contact from a specific part of a device to our measurement circuits. These
pads are approximately squares with a side length of 0.1 mm and a single device uses
10 to 20 bonds, depending on its design, purpose and complexity.

We successively either remove the upper layers or add new ones on top. By selectively
doing this in some areas of the chip, while not in others, we can define nanostructures

that function as devices that can be measured. To define which areas are processed and which are not, we create a mask on the chip. To do this, we first cover the entire chip with polymethyl methacrylate (PMMA) using a spin coater. Next, we use electron beam lithography to draw a pattern onto the resist. This pattern is designed on a computer in a design program such as Autocad. The electron beam increases the solubility of the resist that is exposed, so when the chip is dipped into a 1:3 solution of methyl isobutyl ketone (MIBK) and isopropanol (IPA) for one minute, the exposed resist is removed whereas the unexposed resist stays intact. Using this method, designs with features as small as 40 nm can be reliably created. This process of creating a mask needs to be done for every layer that is either removed or added. After a layer is processed, the excess resist is dissolved away with 1,3 dioxolane before a new mask is made.

The first fabrication step is a subtractive process called the mesa etch, which defines the outlines of the devices. This step removes the aluminium and semiconducting layers in regions that lie between devices, bonding pads and their appendages. This is done with a wet etch, consisting of transene D for the aluminium and a mixture of hydrogen peroxide, phosphoric acid and citric acid for the semiconducting layers. With current technology, the mesa etch is not precise enough to define fine features (below a micrometer) on devices, so it cannot be used in the inner-most areas of a device. In those regions, we control the conductivity of the semiconductor electrostatically, using plunger gates, as described in the previous chapter.

The second step is similar to the first one, but it is an etch that only removes aluminium. This can create finer features and we use it to define the main aluminium wire of the device and also the aluminium parts of the probes. This step is precarious for several reasons. First, it consists of dipping the chip into hot (50 degree) transene D for just five seconds. For such a short duration, a small deviation in timing can be relatively substantial. If etched too little, the aluminium does not get removed where it should, which can easily short-circuit some parts of the device, especially if they are close to each other. If etched too long, the etchant may start flowing under the resist, removing areas of aluminium outside the pattern defined by the mask. This phenomenum is known as etch run and even with a perfectly performed etch, it is

expected to happen in some places sooner than in others, dependent on the geometry of the design. As a result, aluminium nanostructures fabricated with this method are always thinner than the design would suggest. This also sets a limit to how thin these features can be made. For a 3 μm long wire, the width cannot be made less than 80 nm without having unpredictable discontinuities along the wire.

The next step consists of applying an insulating layer of hafnium oxide onto the chip. For the devices in this experiment, there is no reason to avoid having this layer on any part of the chip, so no mask is made for this step. This layer is grown in an atomic layer deposition chamber to a thickness of 15 nm. This is thick enough to insulate two layers of metal, while being thin enough to allow the electrostatic gates to affect the density of the 2DEG buried underneath.

The final set of steps is gate deposition. A layer of metal is deposited onto the entire chip by putting it into a vacuum chamber where metal is gradually evaporated from a crucible using heat applied by an electron beam. This method covers the entire chip with metal, in both masked and unmasked areas. However, when later dissolving the excess resist away, the metal on top of that resist is also removed, leaving behind only the pattern of gates that we defined with electron beam lithography. The material used for the gates is primarily gold, but the first 5-10 nm of deposited metal is titanium, which acts as an adhesive between gold and hafnium oxide. Gate deposition is done in two separate rounds - one for inner features and one for outer features. The inner features need to be finer and thinner so that they fulfill their function in the device without touching each other. The outer features need to be larger, so that they remain continuous while crossing the somewhat abrupt terrain created by the mesa etch. To make this climbing even more uniform and reliable, the chip is tilted and rotated during the metal evaporation for the outer gates. If needed, additional layers of gates can be added by growing another layer of hafnium oxide and then repeating the process. This can be useful or even unavoidable when designing gates that would be very close to each other or even overlap if left on a single layer. A photograph of a finished device with two layers of gates is shown on Figure 3.1.
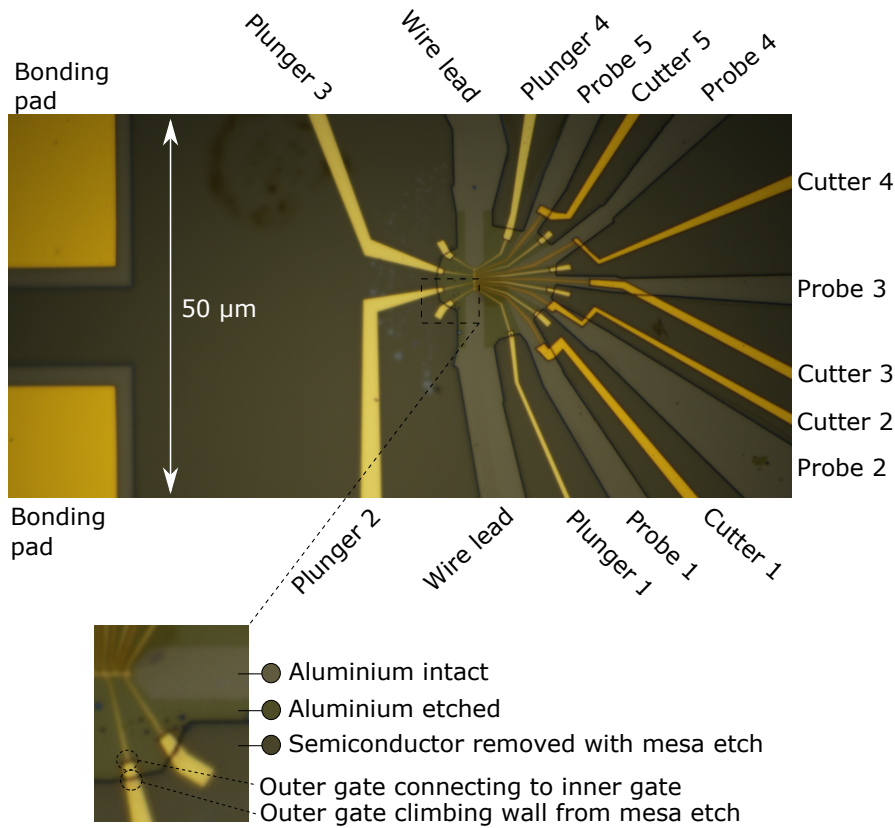
Figure 3.1: A photograph of a finished device, taken under an optical microscope. The device is the same as shown in Figure 2.4 and the labels on the sides have been marked consistently with that. An enlarged and rotated portion of the photo is shown on the bottom, where the borders created by various fabrication steps are visible

When the devices are ready on the chip, they need to be electrically contacted so that we can perform measurements for the experiment. This is done by gluing the chip to a daughterboard and then individually connecting each bonding pad on the chip to a bonding pad on the daughterboard with aluminium wires. This is done using a wedge bonder, which essentially presses the wire into the pad and then fuses them with heat supplied by an ultrasonic vibration. Up to four devices can be bonded up at one time. This limitation comes from the total number of pads on the daughterboard which connect to electrical lines in the cryostat. It also becomes increasingly difficult to make new bonds that do not touch the existing ones. Although the bonding wire is covered with a layer of oxide, it may get removed with friction, potentially causing

23

two neighbouring bonds to make an unwanted electrical connection. A photograph of
a bonded chip is shown in Figure 3.2. New devices can later be bonded up with new
bonds after removing the existing ones.
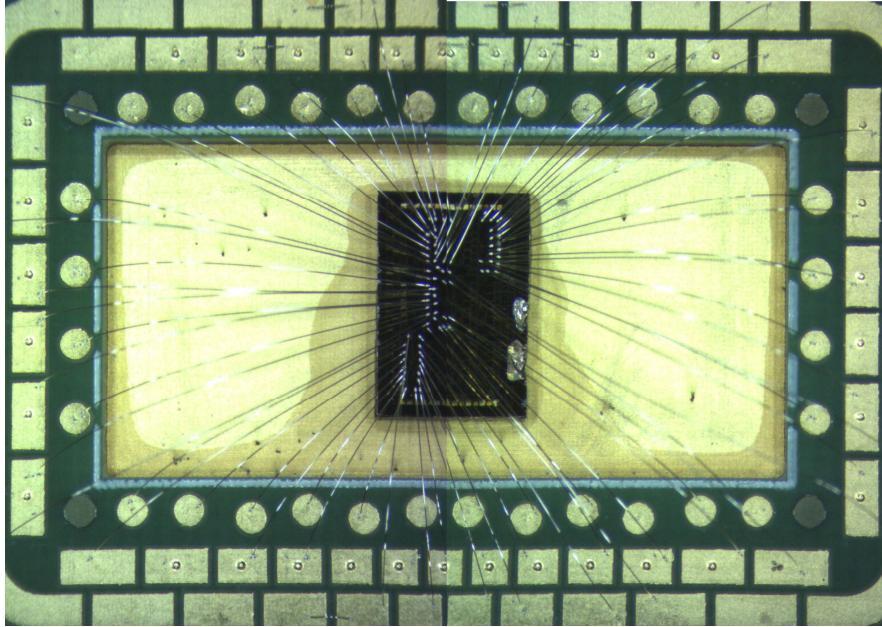
Figure 3.2: Photograph of a 3x5mm chip (black rectangle in the center) glued onto a
daughterboard with PMMA. Four devices are bonded.

The daughterboard is subsequently placed inside a cylindrical frame called a puck,
which is designed to fit into the cryostat. It also provides the connections from the
daugtherboard to the electrical lines that are built into the cryostat, which eventually
lead to a breakout box outside the cryostat, where we are able to connect voltage and
current sources or various measurement instruments. Figure 3.3 shows a photograph
of the puck.

Figure 3.3: Puck with outer casing removed. A daughterboard, currently with no chip, is mounted in the center, with wires connecting it to the electrical lines of the cryostat.

3.2 Cryostat

The cryostat used in this experiment is a dilution refrigerator, manufactured by Oxford Instruments[1]. The puck is in thermal contact with the coldest part of the cryostat, called the mixing chamber, which has a base temperature between 15 to 20 mK. All the measurements presented in this thesis were conducted at this temperature.

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[1] Oxford Instruments Triton 200 Cryofree dilution refrigerator

The primary cooling mechanism of a dilution refrigerator is based on the properties of two helium isotopes, ^{3}He and ^{4}He. When cooled down to slightly below a kelvin, a mixture of these two helium isotopes spontaneously separates into two distinct phases, called the concentrated and the dilute phase [58]. The concentrated phase is almost pure ^{3}He liquid, with a concentration quickly approaching 100% as temperature is further decreased. The dilute phase is ^{4}He superfluid, with a small concentration of ^{3}He atoms sparsely scattered within. Although this small concentration decreases with temperature, it approaches approximately 6,6% instead of zero, as temperature is lowered. The finite presence of ^{3}He is enabled in ^{4}He due to the difference in mass. The larger mass of ^{4}He gives it a lower zero-point motion, meaning that it occupies a smaller volume. Consequently, the atoms in the ^{4}He superfluid are closer together, providing larger Van der Waals forces than the pure ^{3}He liquid. These forces bind atoms and stronger attractive forces result in lower energy quantum states. The ^{3}He atoms can sequentially fill up these states in the dilute phase, following Pauli's exclusion principle. A concentration of 6,6% saturates this mechanism, as the next unoccupied state no longer has smaller energy than a pure ^{3}He liquid.

Whenever ^{3}He atoms migrate from the concentrated phase into the dilute phase, heat is taken from the environment as the ^{3}He expands into a volume with lower partial pressure. To take advantage of this cooling effect, ^{3}He is continuously pumped out of the dilute phase and reinserted into the concentrated phase after precooling and compression. The ^{3}He is extracted from the dilute phase in a separate chamber called the still, which is kept at a temperature of 500-700mK (using heaters), where ^{3}He evaporates preferentially due to its higher partial pressure at this temperature than ^{4}He. The outgoing cold helium is also used to precool the incoming helium by a set of heat exchangers coupling the two lines. The initial cooling is supplied by a pulse tube refrigerator, which cools the mixture down to 4K and subsequent condensation is achieved with a flow impedance that compresses and cools the helium further.

The cryostat is also equipped with a vector magnet, which is also cooled with the pulse tube refrigerator. At the sample, it is possible to apply a magnetic field with a strength of 6T along one axis and 1T along the other two. Changing the strength of the magnetic field dissipates heat, so it is done slowly to avoid heating up the sample.

The temperature of the mixing chamber, still and magnet are all monitored during the experiment to ensure that they remain within acceptable bounds.

3.3 Measurement instruments

In this experiment, the primary method of investigation is the measurement of differential conductance. We perform the measurement with a lock-in amplifier [2], which can measure small signals while minimizing unwanted electrical noise. A lock-in amplifier outputs a small AC voltage with a known frequency (typically below 150 Hz), called the reference frequency f. When this output is connected to a device, it creates a small AC current with the same frequency. We convert this current into a voltage using a low noise I/V converter [3] and feed that voltage back into the lock-in amplifier. The lock-in amplifier digitally multiplies this signal with the reference signal and integrates the result, typically over the range of 30 or 100 milliseconds. This step suppresses any noise or irrelevant signals that do not have the reference frequency (such as the 50 Hz peak), because the integral of the product of two sinusoidal functions approaches zero when the difference in frequencies is greater than the inverse of the integration time. Therefore, the result of this measurement is proportional to the magnitude of the differential current dI in the device at the reference signal frequency. Once this current is calculated, it can be divided by the amplitude of the reference signal dV to yield the differential conductance $G = dI/dV$ of the device. Choosing a longer integration may reduce noise, at the cost of having a measurement that takes longer.

The datasets that we are interested in are measurements of differential conductance as a function of one or more external variables. Among these variables are voltage offsets between different parts of the device. To set voltages, we use a digital-to-analog (DAC) converter [4], which outputs voltages that we set with a computer. The DAC has 48 independent channels, which is more than enough to simultaneously control all necessary voltages with a single instrument. For certain measurements, we also use a

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[2] Stanford Research Systems SR830
[3] Basel Precision Instruments Low Noise/High Stability I to V Converter SP983c [59]
[4] 48 channel QDAC developed at Niels Bohr Institute

Keithley 2400 [5] as a voltage source instead, because it also allows the measurement of the DC current created by that voltage, up to high precision. This functionality is useful for checking whether any parts of the device are shorted, by looking for excess current. Since this instrument only has one or two outputs, we preferentially use the DAC after these excess current detecting tests have been passed.

Often, we measure the differential conductance as a function of voltage bias. To do this, we use a voltage adder to combine the bias supplied by the DAC with the reference signal of the lock-in. Most commonly, we apply these voltages to one or more probes on the device, while keeping the superconducting wire leads grounded. The electrical scheme of this setup is shown in Figure 3.4

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[5]Keithley Series 2400 Source Measure Unit
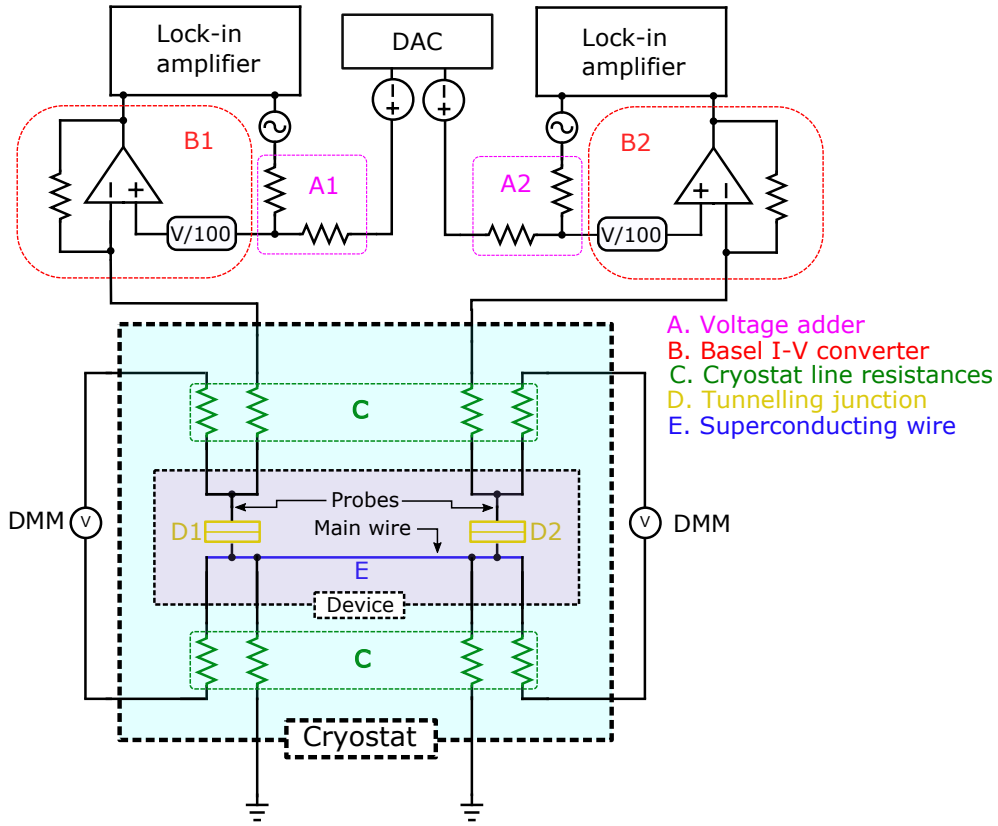
Figure 3.4: Electrical circuit of the measurement setup. This scheme contains two probes, but the actual setup has up to five (not shown on the scheme for readability). Voltages are applied on the probes and the superconducting wire is grounded through cryostat lines which have a finite resistance. Measurements for multiple probes can be performed simultaneously. Additional lines that set voltages on gates are not shown here.

To calibrate the measurement circuit, we disconnect the I-V converter from the cryostat and connect it to a voltmeter instead. By dividing the reading of the voltmeter with the bias applied by the DAC, we obtain the DC voltage division factor originating from the resistances in the voltage adder and internal division by 100 in the I-V converter. We repeat the same process for AC voltage by using the input of the lock-in instead of a voltmeter. These division factors let us calculate what voltages we need our instruments to output to obtain the desirable voltages on the cryostat

lines.

The voltage that we apply on the cryostat lines is already a good approximation for the voltage that is actually applied on the components of the device, but it is not entirely accurate because whenever current passes through the device, there is an accompanying voltage drop across the resistance of the wiring leading to and residing within the cryostat. We can directly measure this difference with a four probe measurement by connecting additional voltmeters or lock-in amplifiers to the same parts of the device using lines that do not pass any current. To have access to these additional lines, extra bonds need to be made to each probe and leads. On a device that had these extra bonds, we performed this measurement and found that the discrepancy was no larger than 10% for tunnelling spectroscopy measurements.

3.4   Tunnelling spectroscopy

By measuring the differential conductance G as a function of the bias V applied between probe and wire, we can map out the density of states at that point in the wire, given that some important conditions are met. The probe and the wire need to be separated by a potential barrier, such that tunnelling is the only mechanism that allows for electrons to pass. The differential conductance is then proportional to the tunnelling rate, which is in turn dependent on the density of states D_wire and D_probe on either side of the barrier

$$G(V) = G_0 \int_{-\infty}^{\infty} \frac{\mathrm{d}f(E - eV)}{\mathrm{d}V} D_\text{wire} D_\text{probe} \mathrm{d}E \tag{3.1}$$

Here $G_0 = \dfrac{2e^2}{h} \sum_n t_n$ is the quantum of conductance for n modes, each with a transmission coefficient t_n, which we assume to be energy independent. The function f is the Fermi function, which depends on the temperature. At low temperatures, the expression approaches

$$\lim_{T \to 0} \frac{\mathrm{d}f(E - eV)}{\mathrm{d}V} = \delta(E - eV) \tag{3.2}$$

which simplifies Equation 3.1 to

$$G(V) = G_0 D_\text{wire}(eV) D_\text{probe}(eV) \tag{3.3}$$

If we know the density of states in the probe, then the density of states in the wire can be calculated:

$$D_{\mathrm{wire}} = \frac{G(V)}{G_0 D_{\mathrm{probe}}(eV)} \tag{3.4}$$

In most designs of this experiment, the probes are superconducting due to the presence of aluminium above, so they have a BCS density of states (Equation 2.3). However, when a magnetic field $B_{\parallel}$ is applied parallel to the main wire, the density of states in the probes becomes constant, similar to a normal metal [60], whereas the main wire remains superconducting. This changes SIS transport into SIN* transport. We observe this transition (Figure 3.5) at 200 mT for the probes, much sooner than the critical field of the wire, which is 3.8 T. These values may vary slightly among devices with different designs, but by no more than 50mT.
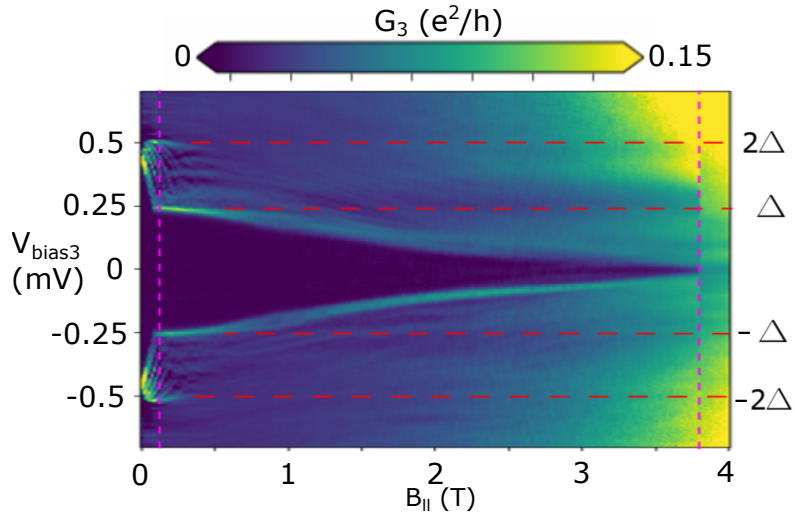

Figure 3.5: Bias spectroscopy as a function of magnetic field parallel to the wire. Marked with magenta: The superconducting gap of the probe vanishes at 200 mT, whereas the critical field of the wire is 3.8 T. Marked with red: the width of the gap seen in spectroscopy is halved as the gap of the probe vanishes. The colourmap has been saturated for increased visibility

3.5 Non-local conductance measurements

Tunnelling spectroscopy can also be performed at one probe with respect to the voltage applied to another probe. This is called non-local spectroscopy and it can be measured simultaneously with the local signal by using an additional lock-in amplifier for each probe. To do this, the additional lock-ins need to measure the current at one probe while slaved to the reference frequency supplied to the other probe. The four different differential conductances obtained from a non-local measurement are commonly arranged in matrix form:

$$
\begin{array}{ccc}
\text{Measured at} & \text{frequency } f_1 & \text{frequency } f_2 \\
\text{probe 1} & G_{11} = \dfrac{\mathrm{d}I_1}{\mathrm{d}V_1} & G_{12} = \dfrac{\mathrm{d}I_1}{\mathrm{d}V_2} \\
\text{probe 2} & G_{21} = \dfrac{\mathrm{d}I_2}{\mathrm{d}V_1} & G_{22} = \dfrac{\mathrm{d}I_2}{\mathrm{d}V_2}
\end{array}
\tag{3.5}
$$

The non-local measurement in our setup is a three-terminal measurement, with two terminals being the two probes that the signals are applied to and the third terminal being the superconducting wire, which is grounded. Such a system has been studied theoretically [61, 62, 63] and experimentally in selective area growth nanowires [64, 65] and it has potential use for aiding the interpretation of data obtained with local bias spectroscopy.

When performing a non-local conductance measurement as a function of bias, we vary V_{bias1} for the left column and V_{bias2} for the right column [66]. Although it would be faster and easier to vary both biases at the same time, it can cause distortions in the data, which are visible in Figure 3.6. It is evident that the data acquires some specularity when the bias on the first probe is outside the value of the gap. This suggests that we ought to vary only one bias at a time, while keeping the other bias fixed at a value within the gap, such as zero.
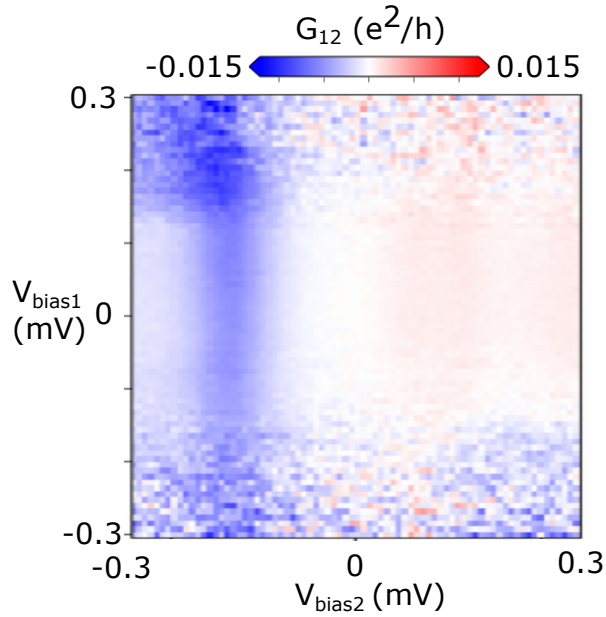
Figure 3.6: A non-local differential conductance measurement with two probes. Current is measured at the first probe at the frequency of the voltage excitation applied to the second probe. This is done as a function of biases on either probe.

Although the superconductor is connected to ground, it is unavoidably grounded through the cryostat electrical lines that have a finite resistance. Again, the effect of this can be checked with an additional voltage measurement if the probes are double bonded, and doing so shows that the correction is below 10 %. As an alternative, we also explored the possibility of using the known values of the resistances to make the correction mathematically. Figure 3.7 displays a schematic of a three terminal device, depicted as a black box, with voltages marked before and after the line resistances. It is possible to derive the general relations between them from the basic electrical laws of Kirchoff and Ohm.

Figure 3.7: A schematic of a three terminal device. The names of resistances, currents and voltages referred to in the main text are defined by the labels indicated here.

The conversion formula is derived in Appendix A and reads

$$
\frac{\partial I_L}{\partial V_L} = D^{-1} \left[\frac{\mathrm{d}I_L}{\mathrm{d}V_1} + (R_2 + R_G) \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right]
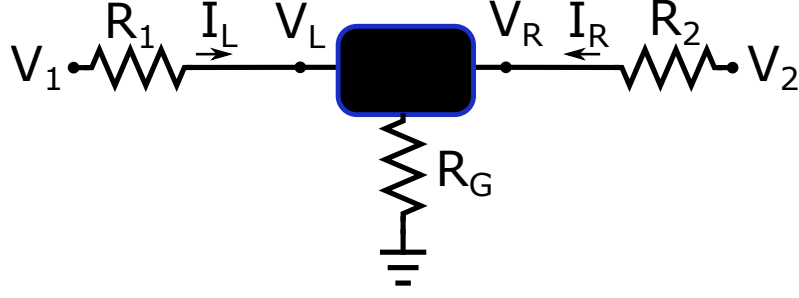$$

$$
\frac{\partial I_L}{\partial V_R} = D^{-1} \left[\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right]
$$

$$
\frac{\partial I_R}{\partial V_L} = D^{-1} \left[\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right]
$$

$$
\frac{\partial I_R}{\partial V_R} = D^{-1} \left[\frac{\mathrm{d}I_R}{\mathrm{d}V_2} + (R_1 + R_G) \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right] \tag{3.6}
$$

where

$$
D = 1 - R_1 \frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_2 \frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_1} + \frac{\mathrm{d}I_L}{\mathrm{d}V_2} + \frac{\mathrm{d}I_R}{\mathrm{d}V_1} + \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right)
$$

$$
- (R_1 R_2 + R_2 R_G + R_1 R_G) \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \tag{3.7}
$$

We performed a test of the validity of this formula by adding various resistances to the lines and benchmarking the results against direct voltage measurements. The result turned out to be unreliable, deviating more from the voltage for higher resistances. The reason this happened is that in general the signals of non-local conductance that we measure are quite small and the noise in these components ends up amplifying the corrections to the point where the theoretically "corrected" plots are less similar to the voltage corrected data than the raw data.

CHAPTER 4

Results and discussion

4.1 Preliminary tests

A prerequisite for any measurement results is to ensure that each component of the device is working as intended. First we check if the connections to the wire and probes are intact. We do this by using the lock-in amplifier to apply a voltage signal to one of the wire leads or probes, while observing what happens when the other lines are connected to ground. When nothing is grounded, then no circuit is formed and the measured resistive component of the differential conductance is zero. With no voltages applied to any of the gates, the 2DEG is conducting everywhere within the device, so when any of the probes or wire leads are connected to ground, we expect the differential conductance to become relatively large (multiple units of e^2/h). If this change does not occur, then that shows that one of the connected lines does not actually reach the device and therefore cannot be used. This could happen if a bond wire came loose or if a mistake was made with the numbering of connected lines.

If we repeat the same test while grounding gates, we expect the differential conductance to remain at zero, as the gates are separated from the rest of the device by

a layer of dielectric. If some differential conductance does appear, then it indicates a defect within the dielectric layer, causing a gate to be shorted to one or more components of the device. In such a situation, the gate simply cannot be used, because the typical voltages that we would apply to them are in the order of volts, which would cause irreversible damage to the entire device. If a cutter gate is unusable, then the experiment could still be performed just with the caveat that the tunnelling barrier at the associated probe cannot be regulated, which may not turn out to be an immediate problem if zero volts happens to provide an optimal tunnelling barrier by chance. A dysfunctional plunger gate makes an entire segment of a device useless because we are unable to form a confined wire without the plunger gates.

Even if the dielectric layer managed to insulate the device, the gates might still be connected to each other due to a misalignment of the chip during fabrication or a microscopic defect within the material. It is important to check this for the entire range of voltage that can be applied to each gate because the gates are frequently operated independently at voltages that differ from each other by many volts, which could potentially result in current leakage between gates given their close proximity. We perform this check by slowly sweeping the DC voltage on each gate while monitoring the current passing through it. If this current begins to exceed 1 nA, then we terminate the sweep to prevent heating and mark up the voltage at which this happened to avoid exceeding it during the experiment. Even for perfectly isolated gates, there are limits to voltage after which we observe leakage current to the entire chip. This typically happens at less than -12 V and at more than 50 mV. These bounds need to be taken into account when designing the gates. Specifically, the upper bound limits the function of the cutter and its ability to open up the potential barrier created by the plungers when operated at very negative voltages.

If two plunger gates happen to be connected to each other, then they can still be used as one big plunger gate, effectively merging two segments together. If two cutter gates are connected to each other, then this may complicate measurements that take place simultaneously on both probes, but does not obstruct using them individually in separate measurements, because they are all far away from each other in the device. This also means that this kind of short-circuit is rare, but could still technically

happen for instance if the bonds on two cutters touched. If a plunger is connected to a cutter, then the spectroscopy with the corresponding probe becomes very limited if not impossible. This is because the voltage required on the plunger gates to form the wire is often more negative than the lower limit of voltage required on the cutter to maintain a tunnelling barrier with a measurably high conductance. To avoid connections between gates, they need to be designed such that they are at least 50 nm apart. Alternatively, gates can be moved closer to each other if they are separated by a layer of dielectric, added with an extra fabrication step.

The next step is to attempt to form the main wire using the plunger gates. To observe this, we apply a negative voltage on each plunger sequentially and measure the differential conductance between the two ends of the wire. Since it would make no difference to a superconducting wire whether or not the surrounding area is depleted, we perform this measurement under a 400 mT magnetic field perpendicular to the chip, which is enough to turn the entire device from superconducting to normal. In that situation, the differential conductance between the two ends decreases sharply at the voltage value where the wire gets depleted. This transition usually happens at around -1.5 to -2.5V. After all plungers cross that threshold, the wire is entirely formed and has a differential conductance of around 10-20 % less than initially. This also indicates that the aluminium is continuous along the entire wire, because a break in the aluminium would cause the differential conductance to drop close to zero, because the 2DEG underneath the break would also be depleted, thereby disconnecting the two wire ends from each other.

Once the voltages on the plungers have been set, it is often necessary to also set a nonzero voltage on the cutters to enable spectroscopy. If the plungers do not automatically pinch the wire junction off from the probe, then the cutter needs to be set to a negative voltage to create a potential barrier in the area between the probe and the wire. We discovered that this might not always be possible. Namely, the first generation of devices that we measured had relatively large junctions, which created a situation where the cutter was unable to cut off a probe entirely, shown in Figure 4.1. In some cases the cutter can be assisted by setting the plungers to an even more negative voltage, but this is not ideal because it further narrows the window of wire

chemical potentials that we can investigate, as that parameter is also regulated by the plungers.
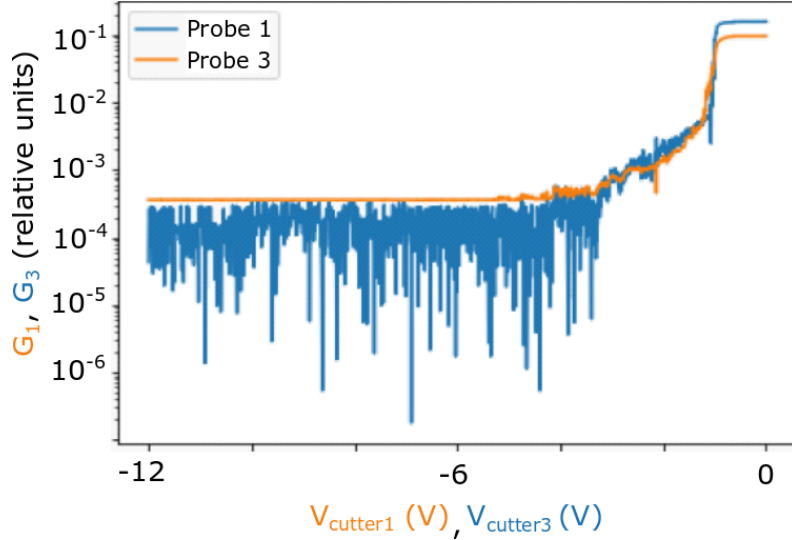

Figure 4.1: Cutter gate effect on differential conductance in two probes of the same device. Probe 3 truly reaches zero conductance shown by the deep dips in the logarithmic scale, which indicate oscillations around zero. The conductance in probe 1 decreases with gate voltage but saturates at a certain value, indicative of residual tunnelling which is not controllable with the cutter.

A fix to this issue was to separate cutters and plungers with a layer of dielectric, which enabled a more compact junction. A comparison can be seen in Figure 4.2, where the device in the bottom picture has cutter gates placed partially underneath plunger gates. With this design, it is very easy to pinch off the junction with the cutter gates, even with no special tuning of the plungers other than having them form the wire. Moreover, with the cutters underneath the plungers, we are almost always capable of preventing the plungers accidentally pinching off the junction - a problem that frequently emerges when the plungers are set to a very negative voltage. This capability is primarily provided by the screening effect that the cutters have simply by virtue of being a piece of metal shielding the junction from the effect of the plungers. We also tested a design variation, where cutters were on top of plungers, which turned out to be less versatile. Namely, in the regime where plunger voltages were highly

38

negative, the cutters were unable to prevent the entire junction from pinching off, partially because they were screened by the plungers but mostly because it required a positive voltage, which we found to cause leakage from around 50 mV, as described earlier.
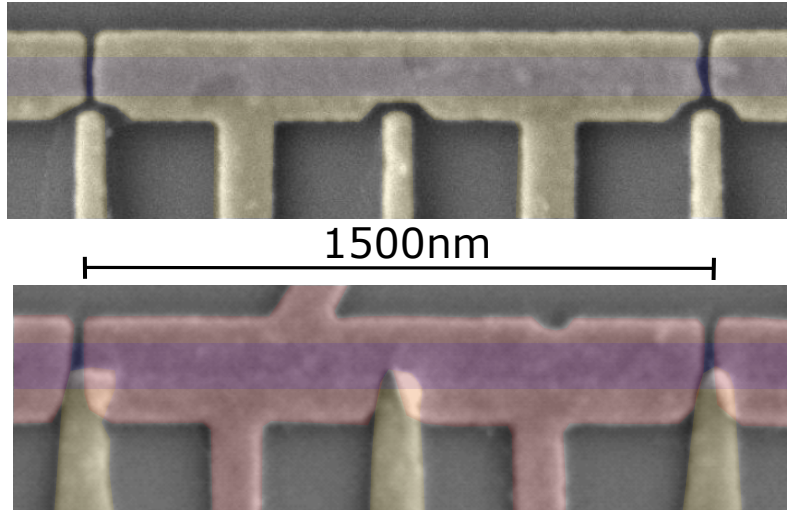
Figure 4.2: False coloured SEM image of a segment in a first generation device (top) and in a later device, also shown in Figure 2.4 (bottom). The first layer of gates is coloured in gold, the second layer is coloured in red. Blue represents the approximate size and location of the main aluminium wire, present underneath the gates and not actually visible in this image.

A properly functioning cutter enables us to access the tunnelling regime in which bias spectroscopy measures the density of states in the wire. Ideally, the tunnelling regime ought to be enabled over a large range voltages so that we are able to make adjustments to identify and/or avoid accidental quantum dots within the device. In Figure 4.3 we observe an empty gap from cutter voltages -30 mV to -70 mV, with above-gap conductance at less than one conductance quantum. At lower than -70 mV, conductance is pinched off entirely and at higher than -30 mV, conductance increases and the gap becomes increasingly difficult to identify.

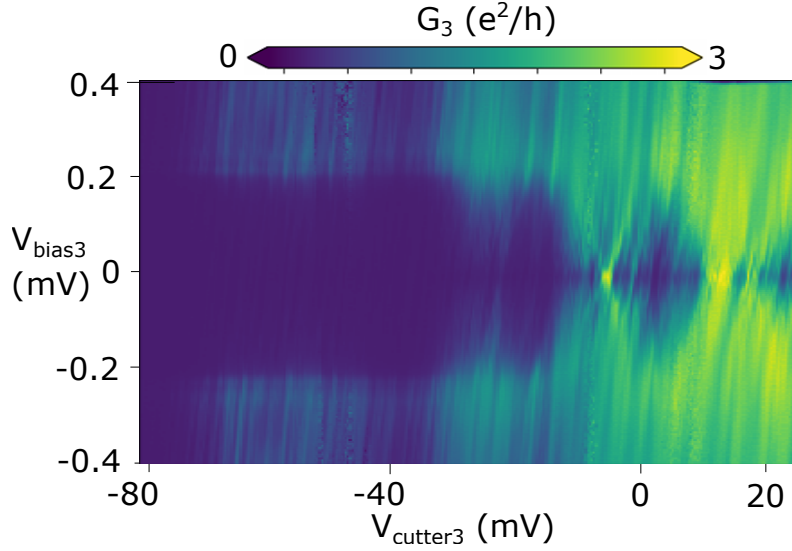Figure 4.3: Bias spectroscopy as a function of cutter gate voltage. The magnetic field is 0.5 T parallel to the wire and the plunger gates are set to -5 V.

This range of voltages is typical for the devices with cutters underneath plungers (as was the case for this measurement). However, this range can vary between cutters quite a lot, even for probes on the same device that have an identical design, which means that we need to perform this type of measurement on each probe to map out its behaviour. The characteristics of a cutter do not change between most measurements so an initial map is sufficiently accurate for selecting suitable cutter voltages where tunnelling spectroscopy is possible. Under some circumstances it is possible that the workable voltage range of a cutter shifts or changes entirely, for instance after large (multiple volts) changes on plunger gates or after warming and recooling the chip in the cryostat.

Figure 4.4 shows the same measurement as Figure 4.3, after warming and recooling the chip. The chip was not removed from the vacuum of the cryostat during this. The conductance is extremely small in comparison, and we are unable to increase it by setting a more positive voltage on the cutter due to the leakage current that starts flowing from the cutter to other parts of the device. All other probes (measurements not shown here) on that device showed similar tendencies, with conductance getting smaller and the suitable voltage range shifting upward.
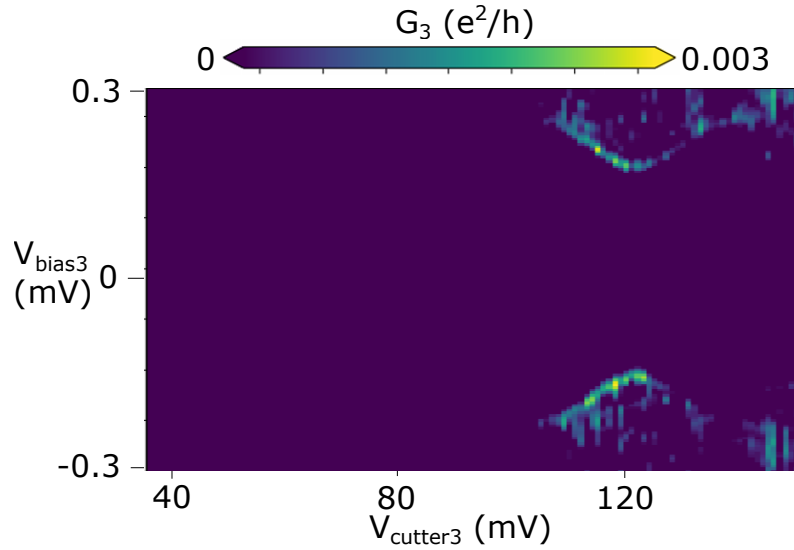
Figure 4.4: Bias spectroscopy as a function of cutter gate voltage. This measurement is performed on the same probe with identical settings as in Figure 4.3, but after thermal cycling.

In conclusion, bias spectroscopy in the tunnelling regime can be performed with these devices, but the range of gate voltages required for it vary among probes and may change after large shifts in temperature. However, once we have access to it we can immediately use it to make a few improvements to the accuracy of subsequent measurements. First, at low magnetic fields, supercurrent is visible at zero bias in most probes. We can use that as a reference to apply a bias offset to our measurements if it appears at a bias voltage slightly different than zero. Second, when we are able to clearly see the quasiparticle gap, we can use it to align the magnetic field with our devices properly. Although the chip is glued flat to the daughterboard, it might still reside at an angle of a few degrees. We can find out what direction of magnetic field is precisely parallel to the wires in the devices by performing a small field rotation - a perpendicular field of the same magnitude results in a smaller gap, so by finding the maximum of the gap as a function of field angle, we can experimentally determine what direction the field is truly parallel to the wires in our devices.

4.2   Searching for zero bias peaks

This experiment has four primary sets of parameters that we can vary - probe biases, cutter voltages, plunger voltages and magnetic field. First, it is important to establish that each probe is only directly affected by the gates that are adjacent to the corresponding junction. We can verify this by measuring on all probes simultaneously while sweeping the voltage on each gate individually and observing no changes on probes that are not in contact with the sweeped gate. Even so, each probe has 2 or 3 gate voltages that it is dependent on. Consequently, the amount of variables is too great for a complete or even dense mapping of parameter space given the constraints on time and resolution provided by the measurement setup. Therefore we are forced to find an efficient recipe for sampling parameter space in order to find features of interest.

The search for Majorana zero modes using tunnelling spectroscopy begins with a search for zero bias peaks. By fixing the bias on the probes to zero, we can specifically look for zero bias peaks within parameter space. Whether or not Majoranas could even exist in the wire, is determined by the chemical potential and magnetic field. Even in theory, the precise range of values in which we expect Majorana modes to be present has a complicated dependence on these two variables [67]. This can originate from multiband occupancy and disorder [68], which are essentially unknown variables that are difficult to quantify in real devices. It would make sense to attempt to map out this dependence, by varying the magnetic field and the plunger voltages.

A set of field-plunger maps can be seen in Figure 4.5, where differential conductance on three probes was measured simultaneously, while varying the plunger that was common to all of them. The regions of higher zero bias conductance appear as almost vertical lines that get dimmer and sparser at more negative gate voltages. The verticality of the lines shows that although states appear and disappear with magnetic field, they remain there at the same gate voltage almost independently of magnetic field. This opens an opportunity for trading resolution in magnetic field in exchange for resolution in some other parameter without losing a significant amount of information, especially in the context of a broad search. For instance, we could

vary two gates instead of one and map out that dependence at perhaps 5-10 magnetic field values to get a more comprehensive idea of device behaviour concerning zero bias conductance.
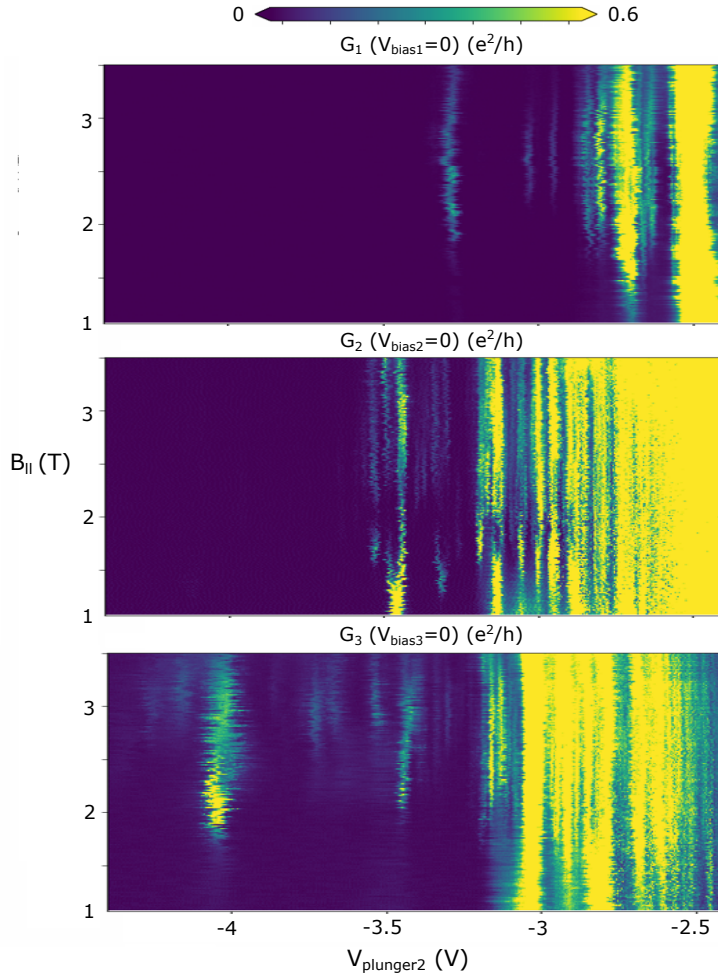
Figure 4.5: Three zero bias conductance maps dependent on magnetic field and plunger voltage. All three maps were measured simultaneously on a single segment, shown in the bottom picture of Figure 4.2

In the most simple picture, we would expect to see a parabolic area of zero bias conductance get added to the outer plots from the presence of Majorana zero modes [69]. Even for a more sophisticated theoretical treatment, we would at least expect to find pockets of conductance [67], again present on the outer plots while absent in the middle plot. None of these features can be found, but it is apparent from these

43

measurements that zero bias conductance in general is not at all rare, regardless of whether it is measured on probes on the end of a segment or in the middle of a segment. This means that there are zero bias signals within our system that have most likely no origin related to topological superconductivity. Additionally, all three probes show a different set of states even though the probes are identical by design. This variance is caused either by inhomogeneities in the material created by the fabrication process or by the complexity of the electrostatic landscape caused by the shape and amount of gates.

The change in zero bias conductance on the horizontal axis is partially caused by change in chemical potential within the wire, but not entirely. One reason why the states get dimmer with more negative voltages is that the plunger gates are also modifying the potential barrier at the probes, causing a change in the transmission coefficients present in Equation 3.4. This effect could in principle be counterbalanced with cutter gates, but the precise action of gate voltages on the barrier and their interdependence is complicated and unknown *a priori*. This further motivates us to measure conductance maps dependent on a plunger and cutter, so that we might begin to untangle the plunger's effect on the chemical potential from its effect on the tunnelling barriers.

An example of a plunger-cutter map at zero bias can be seen in Figure 4.6. The plot contains an abundance of states appearing as lines at various angles. Such an appearance of these plots was generic in our devices and it is reminiscent of the results obtained in Ref [70]. The slope of each line indicates the relative strength of coupling that state to either gate - a mostly horizontal line, such as the two lines near the bottom of the plot, is most likely a resonance of a quantum dot in the junction, formed by the cutter gate. Other features at intermediate angles are harder to straightforwardly interpret and require closer inspection with bias spectroscopy. Although the cutter gate ideally only controls the tunnelling barrier, we cannot rule out that it has the ability to also modify the chemical potential in the wire to some extent, especially given its physical location underneath the plunger. Consequently, the cutter gates have more control over the conductance than they are designed to have - instead of just regulating the value of the conductance, they can also cause states to appear and

disappear at zero bias.
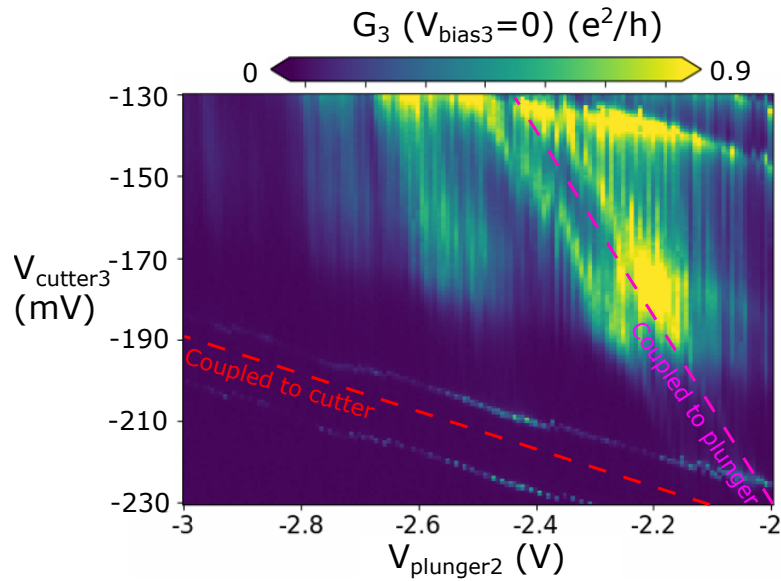
Figure 4.6: Zero-bias conductance as a function of plunger and cutter gate. This measurement is performed at a magnetic field of 2.8 T. Two slopes have been marked to help identify states that couple more to the cutter (red) or to the plunger (magenta).

The field-plunger maps and plunger-cutter maps are our main resource for finding zero bias peaks and can also be readily used to find states that appear simultaneously on different probes. Although they are good for finding which settings of the device may produce interesting physics, they leave out some important information. For instance, they show only zero bias conductance, which could be a peak (as a function of bias), but could just as well be a plateau or even dip. Furthermore, having no measurements at biases other than zero keeps us from tracking how the energy of individual states evolve as a function of other parameters, which could otherwise provide insight into the physical mechanisms that may produce these zero bias signals.

4.3 Testing a Majorana hypothesis on an individual probe

From the field-plunger and plunger-cutter maps, it is clear that there is an abundance of zero-bias signals at many different gate and field settings. We can investigate them in more detail by performing bias spectroscopy to see how they emerge as a function of one of the parameters. We find a variety of different behaviours, each possibly corresponding to a different physical origin. We can compare these different results to theoretical predictions [71, 72, 73, 74, 75] and other experimental works [76, 77].

As the cutter gate only acts locally on one point in the wire, we expect it not to be able to create or destroy topological superconductivity in the rest of the wire, meaning that it would only be able to regulate the visibility of a Majorana zero mode, but not its existence. In contrast, a zero energy state of non-topological origin could plausibly have its energy level modified by the cutter gate to an extent that may be resolvable in bias spectroscopy. Figure 4.7 shows two separate measurements of cutter-bias maps that exemplify these two behaviours. For comparison, a numerical simulation, taken from Ref [71] is included, predicting no splitting for a topological zero bias peak and splitting for a trivial one.
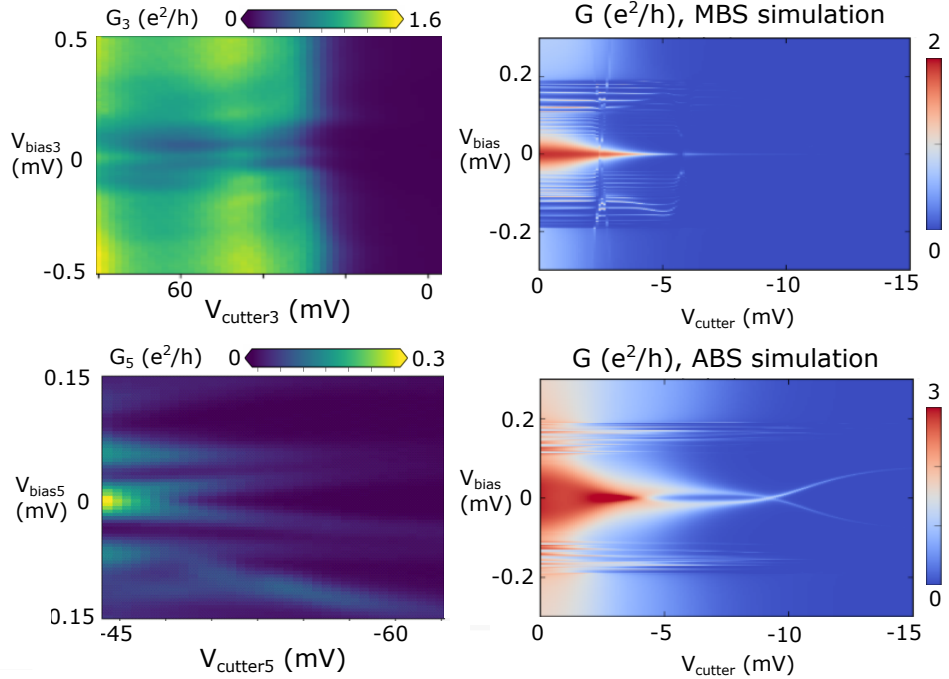
Figure 4.7: Left column: Two separate differential conductance measurements as a function of bias and cutter voltage. The upper one shows a zero bias peak that fades as a function of cutter gate voltage and the lower one shows a zero bias peak that splits. Right column: Plots taken from Ref [71], which simulate the effect of changing the tunnelling barrier with a gate. The upper plot is the expected signal for a Majorana mode, whereas the lower plot is the expected behaviour of a trivial Andreev bound state.

The peak on the upper plot in Figure 4.7 appears to fade rather than split as a function of cutter. This is certainly not generic, as the visibly splitting zero bias peak on the lower plot demonstrates. Although this is the expected behaviour of a Majorana zero mode, it could still be a trivial Andreev bound state [78].

Similarly for plunger gates, there are some states that briefly cross through zero and others that noticeably stick to zero. For a Majorana zero mode, we would expect it to stick to zero for the entire range of voltage values in which the chemical potential of the wire enables topological superconductivity. In all fully functioning devices, we

observed zero energy states of various kinds, some of which could clearly be identified as Andreev levels in quantum dots. The precise location of these dots is unclear, but it is evident that they are often present, unintentionally created by the electrostatic confinement from the gates. Figure 4.8 shows two separate measurements of plunger-bias maps, with the middle plot having a zero bias crossing feature that is very similar to a singlet-doublet-singlet transition of a quantum dot, measured in Ref [76]. These kinds of states that only briefly cross zero bias at two nearby plunger voltages show up on the field-plunger scans as twin peaks, which can for example be seen in the middle plot of Figure 4.5. The lower plot in Figure 4.8 shows noticably different behaviour, with a state sticking to zero bias instead of just crossing. This behaviour is consistent with a Majorana zero mode, but could also be generically produced by an inter-band coupling mechanism theoretically studied in Ref [73].
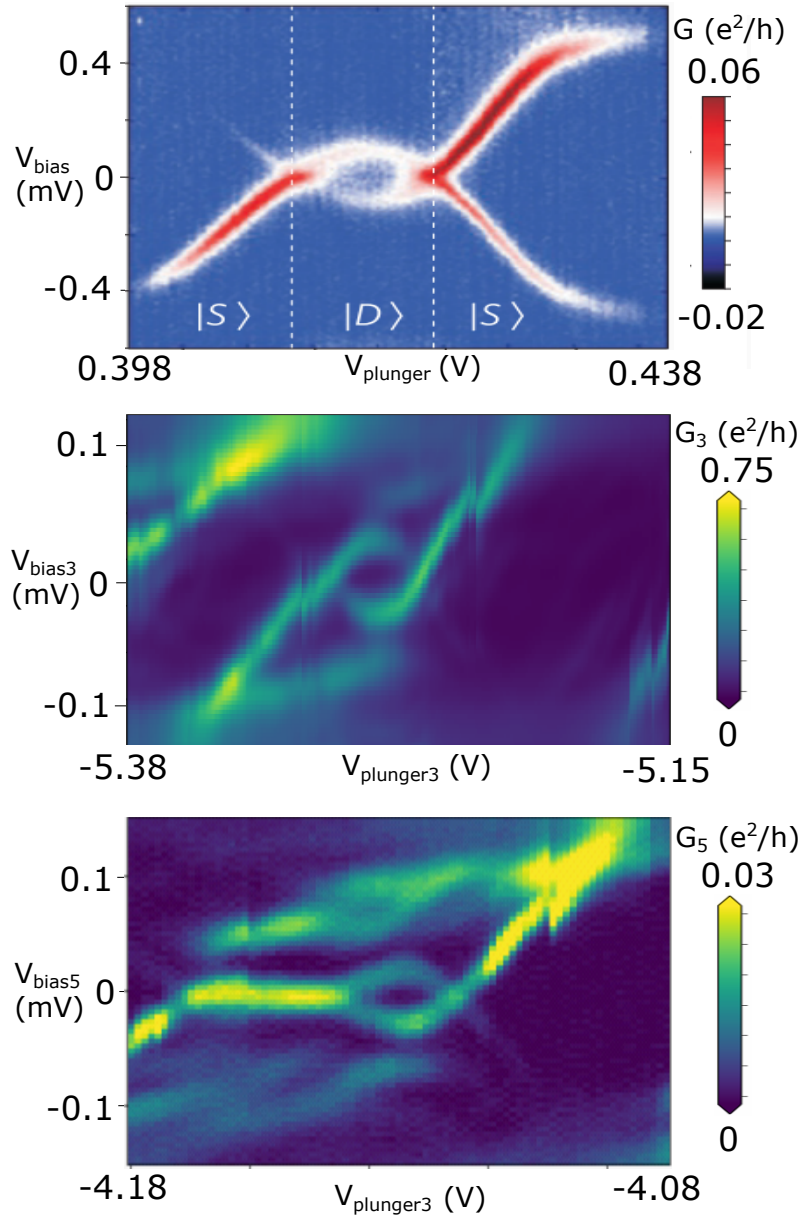
Figure 4.8: Top: Data taken from [76], which shows the singlet-doublet-singlet transition of a quantum dot. Middle: A plunger-bias measurement taken that qualitatively resembles the upper plot, with two states briefly crossing each other twice at zero bias. Bottom: A separate plunger-bias measurement, that shows the presence of a conductance peak that sticks to zero bias for a relatively long range of plunger gate voltage.

Figure 4.9 shows the formation of various kinds of zero bias peaks as a function of magnetic field, also reproducing some of the data previously observed in a shallow 2DEG [77].
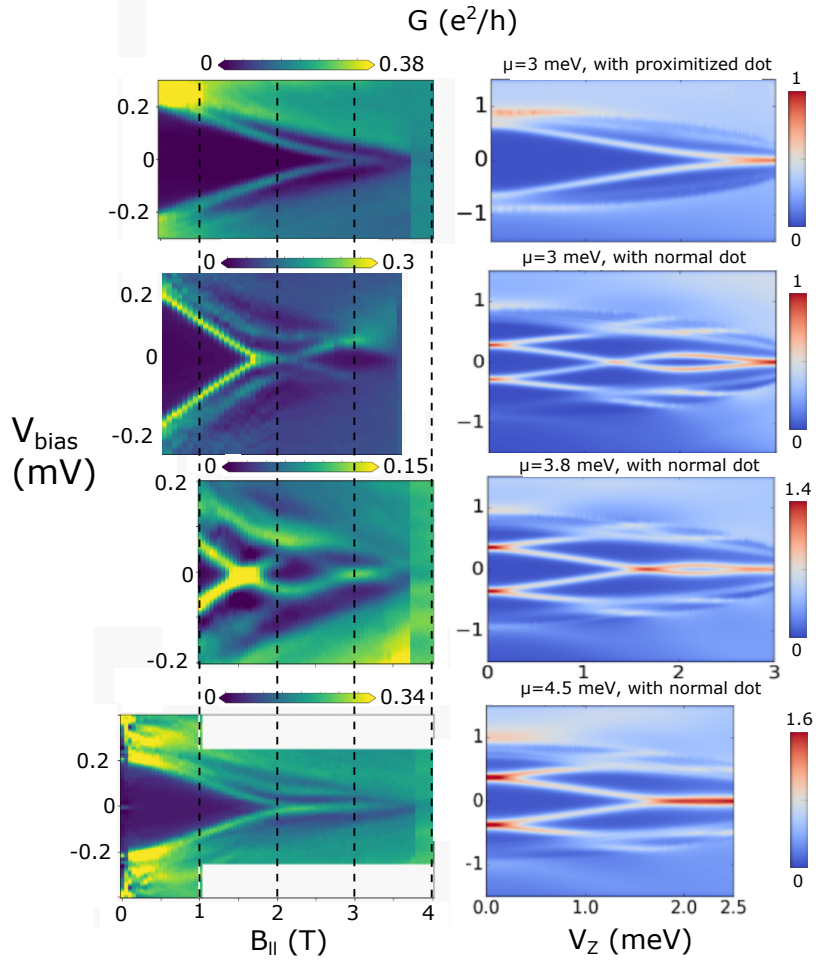
Figure 4.9: Left column: A selection of separate measurements showing different behaviours of states converging to and/or crossing zero bias. Right column: A selection of plots taken from Ref [72], that show qualitatively similar behaviour. All of the simulations shown here include the presence of a quantum dot in the system and have topologically trivial zero bias peaks. The horizontal axis of the simulation plots is the Zeeman splitting energy, which is proportional to magnetic field strength.

For comparison, a selection of theoretical plots from Ref [72], which model the presence of a quantum dot, show qualitatively similar behaviour. Although the simulations in

50

Figure 4.9 all have zero bias peaks of non-topological origin, the expected behaviour of a Majorana zero mode could be very similar, if not indisistinguishable from the trivial ones [72].

All the observed zero bias peaks emerged at a parallel magnetic field larger than ~ 1.2 T. Below that value, the gap was mostly empty, with no signal at zero bias other than supercurrent, which could be faintly seen at low fields and relatively open junctions (also visible in the bottom left plot of Figure 4.9).

Among the various field scans we were unable to find a signature that could definitively be interpreted as a Majorana oscillation [56, 57, 79], although it is plausible that their amplitude could be smaller than our experimental resolution. From a previous experiment in vapour-liquid-solid grown nanowires [80], the amplitude of Majorana oscillations was a few microvolts for a wire length of 1.5 μm, which is the length of our segments in this experiment. The resolution in bias is limited by the magnitude of the reference signal form the lock-in, which we have set between 4 μV and 15 μV for most measurements. Decreasing it further would entail a lower signal to noise ratio, which also requires a longer lock-in integration time to obtain clean data. The time needed to obtain each plot in Figure 4.9 is already on the order of hours.

There was no clearly discernible set of parameters that would more consistently produce a sticking rather than a crossing zero bias signal. Interestingly, we were also unable to recognize any differences between probes situated in the middle of segments versus probes situated at the ends of segments. This likely means that most of the zero bias signals that we observe do not originate from Majorana zero modes because if that were the case, we would expect to see a pronounced absence of these signals on middle probes. It is difficult to quantify how different the probes actually are from each other, because even probes and devices with identical designs have a large variance in behaviour, even when fabricated simultaneously. To make any statistically meaningful statement, tens of devices with identical designs should need to be measured and a more rigorous method to classify behaviours ought to be developed. The measurements shown in this thesis were performed on four generations of devices, each with a slightly different design.

The effect of the different variables described in this section (cutter voltage, plunger voltage and field) can each be used to improve the understanding of the physical origins of the measured zero bias conductance peaks. Although none of these are conclusive by themselves, they can be used in combination with each other, to form a list of tests for any zero energy state with an unknown origin in these devices. Perhaps the tool with the most potential in this regard is the existence of middle probes in this experiment. Finding phenomenology on end probes that is irreproducible on middle probes would give a clear hint in favour of the involvement of Majorana zero modes, but so far such a distinct signature has not been found in these devices.

4.4 Simultaneous measurements on multiple probes

One of the most fundamental features of Majorana zero modes is that they are created in pairs. Since they require such specific circumstances to exist at all, there is not much opportunity for one to go missing in the sense that if we were able to find one in a wire, it is reasonable to believe that the other must also be present in the same wire and in principle not harder to detect than the other. Adhering to this reasoning gives us two guidelines that help us gather evidence for Majorana zero modes.

First, when analyzing data taken simultaneously from different points in the wire, we can use correlations to preselect for simultaneously appearing signals. Given the vast amount of zero bias signals and the relatively long duration of measurements, this technique can speed up the search for Majorana zero modes by eliminating isolated signals with no counterpart present or visible.

Second, when encountering data that is either consistent with Majorana zero modes or has unexplainable behaviour, finding the simultaneous existence of identical behaviour would corroborate the Majorana hypothesis to a degree simply not achievable by single probe measurements. The various ways in which other physical processes may mimic Majorana signatures makes it difficult to know the precise nature of a single probe measurement. Conversely, this richness in phenomenology also makes coincidences of specific behaviours more unlikely to occur on multiple probes at once,

giving the multiple probe setup a stronger capability to detect false-positives.

Ideally we would not only attempt to correlate zero bias peaks, but also their response to gates and magnetic field. Again, the number of parameters makes finding these correlations difficult. Furthermore, characteristics of individual probes could plausibly lead to shifts or distortions in identical features. For instance, if the dielectric grew slightly thicker on one area of the device, then the gates would have a different lever arm and correspondingly a weaker effect on the density of states in the wire and junction. Although correlations in gate space have been observed in shorter devices in other experiments [81], it may be more straightforward to correlate field-bias scans since the magnetic field strength is independent of fabrication variances and bias can be quite reliably calibrated by measuring supercurrent at low field. Additionally, we have a more clear vision of what to expect on probes that are located between the one that display a pair of Majorana induced zero bias peaks [55]. Namely, we would expect the quasiparticle gap to momentarily close and reopen at the same field value for all probes, with zero bias states only emerging at the ends and not in the middle.

The high degree of tunability in our devices enables us to observe such a situation. The top row of plots in Figure 4.10 shows data taken from Ref [82] and the middle and bottom rows show two separate sets measurements in our devices. All three rows represent three consecutively positioned probes that were measured simultaneously. Notably, the outer ones have zero bias states emerging whereas the middle one does not. An important difference between these datasets is that Ref [82] had no gates to regulate the tunnelling barriers. Instead, the barrier was formed by a thin layer of aluminium oxide, left untunable after fabrication. One point of view is that the cutter gates in our experiment allow us to optimize the visibility of whatever is present in the wire, but the other view is that the cutter gates create certain features in tunnelling spectroscopy (for instance by forming dots in the junction) which can easily lead to a case of confirmation bias when trying to find specific shapes or behaviours of states.
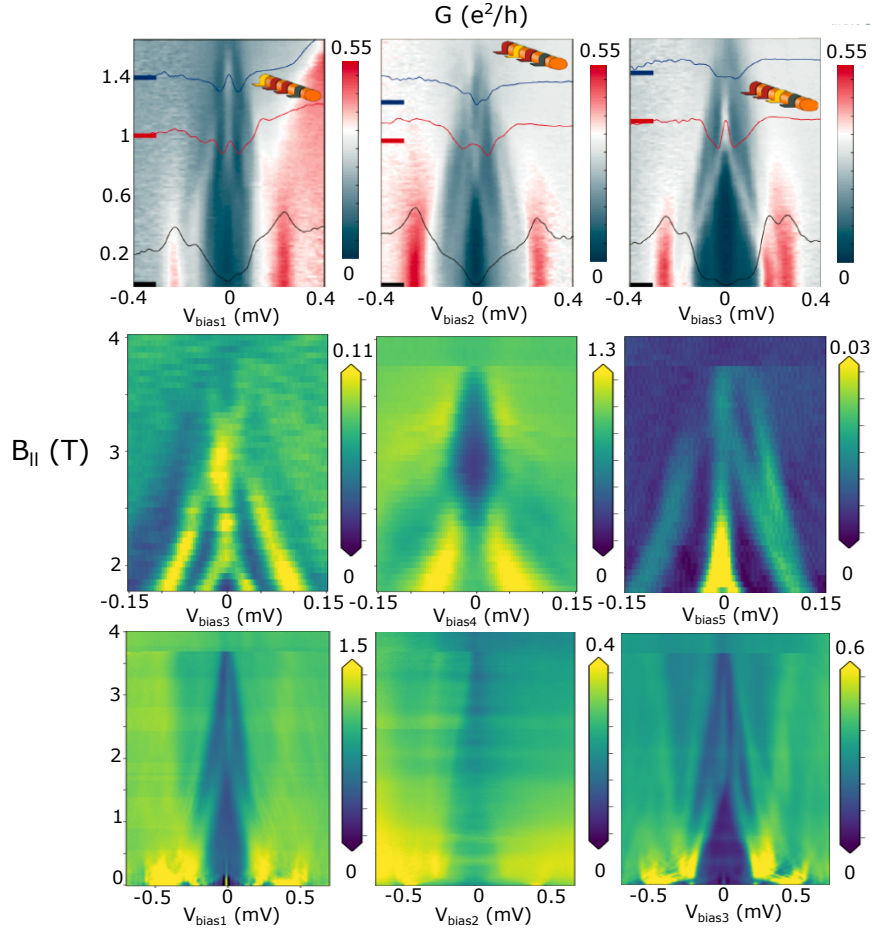
Figure 4.10: Top: Measurements taken from Ref [82] depicting the simultaneous emergence of zero bias peaks on two probes with no peak appearing in between. Middle and bottom: Analogous measurements performed on two separate devices.

Another resource that may augment the data gathered in these devices are non-local conductance measurements. Especially with the superconducting wire grounded, theory provides some methods for extracting various parameters of the system such as the bulk superconducting gap, the induced gap, the induced coherence length [61] and quasiparticle charges [83]. In conjunction with local spectroscopy measurements, these would all be useful in detecting a topological phase transition in a manner more robust to microscopic inhomogeneities in the devices [63]. In other experiments involving shorter nanowire devices, progress has been demonstrated in this area [64, 65].

In our devices, we were able to perform non-local conductance measurements and observe the superconducting gap, shown in Figure 4.11. The magnitude of the signal was weak compared to the local conductance measurements, making individual sub-gap states hard to observe in most measurements. The small magnitude of the non-local conductance may be caused by chemical potential inhomogeneity and random impurity disorder [63]. The measurement shown in Figure 4.11 is taken between two neighbouring probes, with a distance of 750 nm. Whether the small magnitude is a property of the material system or a consequence of the long length needs further study to be clarified, for instance by gathering statistics of these measurements on devices with significantly shorter or longer distances between probes. Again there is a variance in individual probe behaviour making these aspects difficult to generalize.
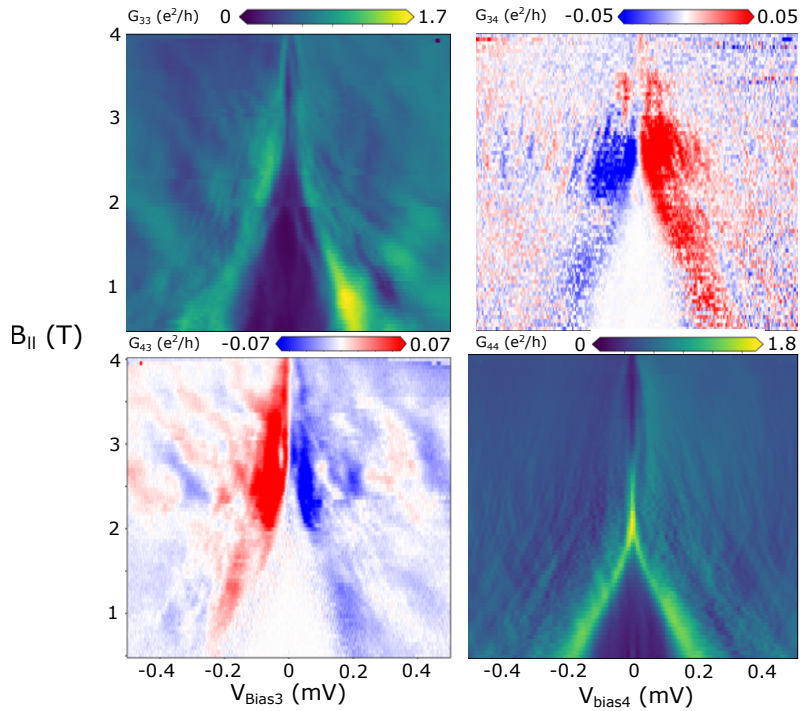
Figure 4.11: Measurement of the non-local conductance matrix between two probes, as a function of bias and magnetic field. The top-left and bottom-right are local tunneling spectroscopy measurements.

An interesting feature of Figure 4.11 is the closing of the gap at 1.8 T on the local measurement on the right probe, which is apparently absent on the other plots. This

could indicate that this particular feature is localized to the right probe, but it could also just be unresolvable on the off-diagonal plots. As a future direction, measurements like this could help distinguish between instances of the gap closing within the bulk of the wire versus the gap closing only at certain points in the wire [84].

Conclusion and outlook

5.1   Conclusion

In conclusion, this work describes the performance of multiprobe devices formed in a 2DEG using top-down fabrication and electrostatic gating. Frequently occurring problems such as current leakage between gates and lack of control of the tunnelling barrier were addressed with an improvement in design. Tunnelling spectroscopy within these devices was characterized and a methodology for efficiently finding zero bias signals was developed and implemented. The formation and physical origin of various zero bias signals were analyzed as a function of gate voltages, magnetic field and bias. Comparisons to other theoretical and experimental works indicate the presence of unintentionally formed quantum dots within the devices, but include signatures consistent with Majorana zero modes. No obvious dependence on probe location was observed, possibly obscured by the inherently large variance of individual probe behaviour. Measurements were performed on multiple probes simultaneously to obtain data with potentially stronger interpretive power compared to single probe measurements. Comparisons with analogous results from nanowires broaden the generality of these measurements and provide a baseline for assessing the results obtained from

future multiprobe experiments.

5.2 Outlook

The experiment could be improved upon in multiple ways. First, plunger gate design could be elaborated by using separate gates for each side of the wire, perhaps asymmetrically, with the intention of creating a narrower and more uniform topological wire [85]. Second, cutter gate design could potentially be improved upon with the aid of numerical electrostatic simulations. Alternatives such as quantum point contacts, possibly formed by appendages of plunger gates could also be tried. Third, a more rigorous statistical analysis of the data could improve the understanding of the rich phenomenology observed thus far. Statistical treatment could be enhanced by exploring segments of different lengths.

The results of this experiment bring us a step closer to being able to control Majorana zero modes. Currently, the emphasis is on identifying their existence in these systems, but once that is achieved, attempting to deliberately create, destroy and move them would be the next step, which can be most readily done with a segmented wire akin to the one studied in this experiment. Understanding of the interplay between multiple gates in more complex devices can be improved by examining the data gathered from the devices investigated in this experiment.
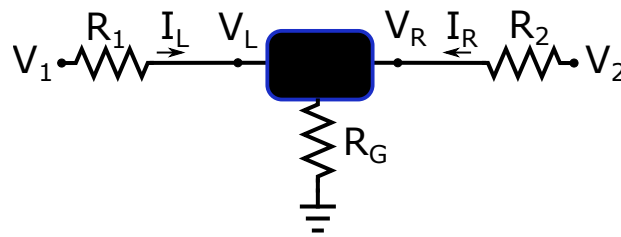
Kirchoff's and Ohm's laws:

$$V_L = V_1 - I_L R_1 - (I_L + I_R) R_G \tag{5.1}$$

$$V_R = V_2 - I_R R_2 - (I_L + I_R) R_G \tag{5.2}$$

Derivatives

$$\frac{\mathrm{d}V_L}{\mathrm{d}V_1} = 1 - (R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_1} \tag{5.3}$$

$$\frac{\mathrm{d}V_L}{\mathrm{d}V_2} = -(R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_2} \tag{5.4}$$

$$\frac{\mathrm{d}V_R}{\mathrm{d}V_1} = -(R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_1} \tag{5.5}$$

$$\frac{\mathrm{d}V_R}{\mathrm{d}V_2} = 1 - (R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \tag{5.6}$$

Conductances

$$\frac{\mathrm{d}I_L}{\mathrm{d}V_1} = \frac{\partial I_L}{\partial V_L}\frac{\mathrm{d}V_L}{\mathrm{d}V_1} + \frac{\partial I_L}{\partial V_R}\frac{\mathrm{d}V_R}{\mathrm{d}V_1} \tag{5.7}$$

$$\frac{\mathrm{d}I_R}{\mathrm{d}V_1} = \frac{\partial I_R}{\partial V_L}\frac{\mathrm{d}V_L}{\mathrm{d}V_1} + \frac{\partial I_R}{\partial V_R}\frac{\mathrm{d}V_R}{\mathrm{d}V_1} \tag{5.8}$$

$$\frac{\mathrm{d}I_L}{\mathrm{d}V_2} = \frac{\partial I_L}{\partial V_L}\frac{\mathrm{d}V_L}{\mathrm{d}V_2} + \frac{\partial I_L}{\partial V_R}\frac{\mathrm{d}V_R}{\mathrm{d}V_2} \tag{5.9}$$

$$\frac{\mathrm{d}I_R}{\mathrm{d}V_2} = \frac{\partial I_R}{\partial V_L}\frac{\mathrm{d}V_L}{\mathrm{d}V_2} + \frac{\partial I_R}{\partial V_R}\frac{\mathrm{d}V_R}{\mathrm{d}V_2} \tag{5.10}$$

Inserting the derivatives yields

$$\frac{\mathrm{d}I_L}{\mathrm{d}V_1} = \frac{\partial I_L}{\partial V_L}\left[1 - (R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_1}\right] + \frac{\partial I_L}{\partial V_R}\left[-(R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_1}\right] \tag{5.11}$$

$$\frac{\mathrm{d}I_R}{\mathrm{d}V_1} = \frac{\partial I_R}{\partial V_L}\left[1 - (R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_1}\right] + \frac{\partial I_R}{\partial V_R}\left[-(R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_1}\right] \tag{5.12}$$

$$\frac{\mathrm{d}I_L}{\mathrm{d}V_2} = \frac{\partial I_L}{\partial V_L}\left[-(R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_2}\right] + \frac{\partial I_L}{\partial V_R}\left[1 - (R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_2}\right] \tag{5.13}$$

$$\frac{\mathrm{d}I_R}{\mathrm{d}V_2} = \frac{\partial I_R}{\partial V_L}\left[-(R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_2}\right] + \frac{\partial I_R}{\partial V_R}\left[1 - (R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_2}\right] \tag{5.14}$$

The first and third equations in matrix form are

$$\begin{pmatrix} 1 - (R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_1} & -(R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_1} \\ -(R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_2} & 1 - (R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \end{pmatrix} \begin{pmatrix} \frac{\partial I_L}{\partial V_L} \\ \frac{\partial I_L}{\partial V_R} \end{pmatrix} = \begin{pmatrix} \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \\ \frac{\mathrm{d}I_L}{\mathrm{d}V_2} \end{pmatrix} \tag{5.15}$$

$$\begin{pmatrix} \frac{\partial I_L}{\partial V_L} \\ \frac{\partial I_L}{\partial V_R} \end{pmatrix} = \begin{pmatrix} 1 - (R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_1} & -(R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_1} \\ -(R_1 + R_G)\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_R}{\mathrm{d}V_2} & 1 - (R_2 + R_G)\frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \end{pmatrix}^{-1} \begin{pmatrix} \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \\ \frac{\mathrm{d}I_L}{\mathrm{d}V_2} \end{pmatrix} \tag{5.16}$$

The result is

$$\frac{\partial I_L}{\partial V_L} = D^{-1} \left[\frac{\mathrm{d}I_L}{\mathrm{d}V_1} + (R_2 + R_G) \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right] \qquad (5.17)$$

$$\frac{\partial I_L}{\partial V_R} = D^{-1} \left[\frac{\mathrm{d}I_L}{\mathrm{d}V_2} - R_G \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right] \qquad (5.18)$$

$$\frac{\partial I_R}{\partial V_L} = D^{-1} \left[\frac{\mathrm{d}I_R}{\mathrm{d}V_1} - R_G \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right] \qquad (5.19)$$

$$\frac{\partial I_R}{\partial V_R} = D^{-1} \left[\frac{\mathrm{d}I_R}{\mathrm{d}V_2} + (R_1 + R_G) \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \right] \qquad (5.20)$$

where

$$D = 1 - R_1 \frac{\mathrm{d}I_L}{\mathrm{d}V_1} - R_2 \frac{\mathrm{d}I_R}{\mathrm{d}V_2} - R_G \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_1} + \frac{\mathrm{d}I_L}{\mathrm{d}V_2} + \frac{\mathrm{d}I_R}{\mathrm{d}V_1} + \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \qquad (5.21)$$

$$- (R_1 R_2 + R_2 R_G + R_1 R_G) \left(\frac{\mathrm{d}I_L}{\mathrm{d}V_2} \frac{\mathrm{d}I_R}{\mathrm{d}V_1} - \frac{\mathrm{d}I_L}{\mathrm{d}V_1} \frac{\mathrm{d}I_R}{\mathrm{d}V_2} \right) \qquad (5.22)$$

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