TOWARDS TANTALUM SUPERCONDUCTING QUBITS WITH SHADOWED JUNCTION NANOWIRES

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Abstract

Superconducting qubits are one of the most promising solutions to realize practical quantum computer. To realize universal gate operations, people develop gatemon to gain control on dynamic couplings among qubits through gate tunable qubit frequency. This thesis mainly investigates the prospect of utilizing tantalum for gatemon qubit. We report the transport properties of tantalum-coated InAs nanowires with shadow S-Sm-S Josephson junction. The tunable critical current is down to 20 nA, and high stability, repeatability is observed. Besides, we report the high-frequency measurement on wet etched sputter tantalum resonator with a million Q factor in single photon regime, which allows a long coherence time ($T_1 > 50\mu s$) qubit. The study provides a promising path to a high T_1 time gatemon.

Preface

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Contents

1 Introduction

1.1 Why we want qunantum computer

Computers are undoubtedly one of the most useful, powerful, and essential tools in the twenty-first century. We can use them to view the latest news in the world, train models on auto-driving cars, and do ab initio calculations for diverse material. Although Gordon Moore correctly predicted that the processors would double the number of transistors per year in the past 60 years, electron tunneling and heat generation due to the growing density of transistors are challenging the known Moore's law.

The Quantum computer is considered a powerful supplement to the classical computer in simulating nature due to its overwhelming advantage in inherent parallel computing capability. Unlike classical bits 0 and 1, quantum bits, namely qubit, can form a superposition of $|0\rangle$ and $|1\rangle$ with phase. This property gives quantum computers extraordinary power to solve challenging questions such as the decomposition of sizeable prime number[1]. Due to the powerful quantum parallelism, people also study the quantum algorithm of ray tracing in rendering images for games[2].

The community now positions superconducting qubits as a platform for noisy intermediate scale quantum (NISQ) computing that performs calculations outside of classical algorithms but with limited logical error-corrected qubits[3]. Nevertheless, quantum computers can still outperform classical computers in specific calculations. Some people call this surpass 'quantum supremacy'[4], or more gently 'quantum advantage'[5]. Scientists and engineers are trying to push the performance of quantum computing forward through, for example, mitigating noise and gate set improvement to the scalable fault-tolerant quantum computer. Until then, we can implement some more heavily-loaded industrial computational tasks and safely say we have reached the quantum computer era.

There are several ways to realize quantum computers. Superconducting qubit is one of the most promising competitors owing to their scalability, fast gate time, and relatively mature fabrication technique. Despite their disadvantages in fast decoherence and the need for a cryogenic environment, superconducting qubits still prosper around the quantum computing community and develop swiftly. A recent paper utilizes a 62-qubit programmable superconducting processor to perform quantum algorithm[6]. Among all the types of superconducting qubits, transmon, namely transmission-line shunted plasma oscillation qubits, is a popular type of charge-insensitive qubit investigated by many labs and companies such as IBM. Based on the idea of transmon, to tune the frequency of the qubit to explore the optimal working regime, people will use superconducting quantum interference device (SQUID) to introduce flux, therefore phase change on the junction. We, in this thesis, use gate-tunable S-Sm-S nanowires to act as the Josephson junction. By defining the gate beneath the junction, we can tune the Fermi energy of the junction, thus the qubits' frequency. In this thesis, we propose a path of using tantalum-coated with shadow in-situ growth S-Sm-S junction InAs nanowire as Josephson junction in gatemon and tantalum as capacitors and control lines as superconducting qubits. We do both DC transport measurements on the tantalum nanowires to prove the possibility of utilizing them as Josephson junction and high-frequency measurement on resonator to show the high quality factor of tantalum.

1.2 Basic quantum computing

Classical bit to qubit

Classically, we use binary representation, 0 and 1, in modern transistor computers and can implement elementary arithmetic by utilizing different gates' combinations. It's worth emphasizing here that each bit is definite, such as 5V in the circuit stands for one and 0V stands for zero. No intermediate bit is allowed like 3V stands for 0.6. Meanwhile, the gate operations like adder can change the number of bits, leading to loss of information during calculations.

When we move to the quantum world, things are very different. Think of a single electron. We learn from Stern–Gerlach experiment that the angular momentum on the z direction can be quantized, and we name it spin with spin up $|\uparrow\rangle$ and down $|\downarrow\rangle$, which represents $|0\rangle$ and $|1\rangle$. However, prior to the measurement, the spin's output can't be written as any function with fixed variables, but only the probabilistic function. It means that quantum mechanics is not local and against the hidden-variable theory. This is the well-known Bell's theorem[7] and has been experimentally proved[8]. The only way to represent such a state is to use complex number α and β like $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ with normalization condition $|\alpha|^2 + |\beta|^2 = 1$. The superposition state $|\psi\rangle$ here, in quantum information, can be called a qubit.

An arbitrary pure state spin's, generally two-level systems, density matrix can be described as:

$$\rho = |\psi\rangle\langle\psi| = \frac{1}{2}(\mathbf{I} + \mathbf{s}\cdot\sigma) \tag{1.1}$$

with Bloch vector $\mathbf{s} = (x, y, z)$ and Pauli matrix σ. For convenience, we use a Bloch sphere to represent the qubit (fig). Let $\mathbf{s} = (\sin\theta\cos\phi, \sin\theta\sin\phi, \cos\theta)$ we now gain a qubit with the wave function:

$$|\psi\rangle = cos\frac{\theta}{2}|0\rangle + e^{i\phi}\sin\frac{\theta}{2}|1\rangle \tag{1.2}$$

The coordinate (θ, ϕ) indicates a pure state point on the surface of the Bloch sphere. If a mixed state, that is $\mathrm{Tr}(\rho^2) \neq 1$, the vector points inside the sphere. For example, the process of qubit decoherence corresponds to a trace from the sphere surface to the inner part. Multi

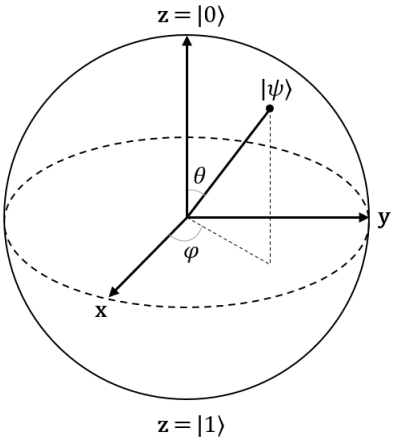


Figure 1.1: The illustration of Bloch sphere. Every point on the surface of the sphere stands for a pure state (for example, the point on the north pole at the end of the z-axis can be $|0\rangle$).

qubits entanglement is another important characteristic different from classical computing. The entanglement as a non-local correlation mathematically means that the many qubits' states can't be written as the direct product of single qubit's state. A two qubits, A and B, system can have a maximally entangled basis, Bell basis:

$$\begin{aligned}
|\Phi^+\rangle &= \frac{1}{\sqrt{2}}(|0\rangle_A \otimes |0\rangle_B + |1\rangle_A \otimes |1\rangle_B) \\
|\Phi^-\rangle &= \frac{1}{\sqrt{2}}(|0\rangle_A \otimes |0\rangle_B - |1\rangle_A \otimes |1\rangle_B) \\
|\Psi^+\rangle &= \frac{1}{\sqrt{2}}(|0\rangle_A \otimes |1\rangle_B + |1\rangle_A \otimes |0\rangle_B) \\
|\Psi^-\rangle &= \frac{1}{\sqrt{2}}(|0\rangle_A \otimes |1\rangle_B - |1\rangle_A \otimes |0\rangle_B)
\end{aligned} \tag{1.3}$$

Take $|\Phi^+\rangle$ as an example. If qubit A collapses to the ground state, we can definitely say that qubit B is also in the ground state theoretically, and vice versa. Therefore the $|\Phi^+\rangle$ state can't be written as any form of $|A\rangle \otimes |B\rangle$.

Superposition and entanglement are the foundation of the quantum technology field, including quantum communication, quantum simulation, and quantum computing, and the reason for fast parallel computation in quantum computers. We can initialise a quantum state $\psi = \sum_{k=1,2..N} p_k|s_0 s_1 ... s_N\rangle$, with s_k the state of qubit k, and compute 2^N state simultaneously in a single step. This property endows exponential acceleration in certain calculations, like Shor's algorithm for integer prime factorization.

Quantum logic gate

Classically, the logic gates include non-reversible operation AND, OR with 2 bits in then 1 bit out. Unlike the classical situation, quantum gates are represented as unitary operators, meaning no information is lost during the calculation. Any single qubit gate operation can be represented as pivot rotation of vector on Bloch sphere:

$$\mathbf{R}(\mathbf{n},\varphi) = \exp(-i\frac{\varphi}{2}\mathbf{n}\cdot\sigma) = \cos(\frac{\varphi}{2})\cdot I - i\sin(\frac{\varphi}{2})\mathbf{n}\cdot\sigma \tag{1.4}$$

where $\mathbf{n} = (\sin\theta\sin\phi, \sin\theta\cos\phi, \cos\theta)$ and φ the rotation angle. For example, we can construct a Hadamard gate:

$$H = \frac{\sqrt{2}}{2}\begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \tag{1.5}$$

This gate operation will bring state $|0\rangle$ to $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$.

To realize entanglement between two qubits, we also need two qubits gate, like Control-NOT (CNOT) gate under $|00\rangle, |01\rangle, |10\rangle, |11\rangle$ basis:

$$CNOT = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \tag{1.6}$$

. This gate maps $|10\rangle$ to $|11\rangle$, and $|11\rangle$ to $|10\rangle$. As shown in Fig.1.2, with the combination of Hadamard gates and CNOT gates, we can prepare a $|\Phi^+\rangle$ state.

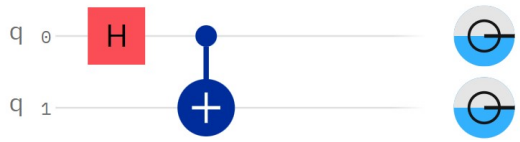


Figure 1.2: The two qubits both start with initial state $|0\rangle$. In the first operation, qubit 0 undergoes a Hadamard gate, and the qubit state becomes $\frac{1}{\sqrt{2}}(|0\rangle + |1\rangle) \otimes |0\rangle$. After the CNOT gate, the state becomes $\frac{1}{\sqrt{2}}(|0\rangle \otimes |0\rangle + |1\rangle \otimes |1\rangle)$, the $|\Phi^+\rangle$state.

Quantum measurement

In quantum mechanics, measurement operation equals to the average of a certain operator of some wave function:

$$\langle \mathbf{F} \rangle = \langle \psi | \mathbf{F} | \psi \rangle \tag{1.7}$$

In qubit, we perform projection measurement, a single shot readout with operator $\mathbf{P}_s = |s\rangle\langle s|$, s is 0 or 1. After thousand times of measurement, the probability of qubit in $|s\rangle$ state, $|\alpha|^2$ or $|\beta|^2$, is obtained. Quantum non-demolition (QND) measurement is another important concept.

With QND, the qubit system remains in the computational subspace and can be repeatedly measured. For example, if we find the qubit is in $|1\rangle$ state, this $|1\rangle$ state can be used as a new initial state for future operations. Dispersive readout, a common QND measurement method for qubits, is performed with far detuning between the resonator and qubit. When the coupling rate of the resonator and qubit g, and the resonator linewidth κ is much lower than the frequency detuning $\Delta g, \kappa$, the readout system is in the dispersive limit and without direct energy exchange to the qubit.

Projection measurement doesn't provide enough information for the density matrix of the whole qubit system. We need to introduce quantum state tomography to get all the elements in the density matrix. In the case of a single qubit, from Eq.1.1 we can see that if we measure $\sigma_x, \sigma_y, \sigma_z$, we can obtain (x,y,z) and then the density matrix. In a multi-qubits system, we can use a neural network to get the density matrix swiftly[9].

Decoherence

The word noise in NISQ indicates decoherence in qubits. The qubit system is unavoidably connected to the environment because we need to read out the information inside the system. Therefore the qubit and environment undergo energy exchange and phase variation. We often consider this event a stochastic process. We usually sort it into two kinds of relaxation. One is energy relaxation, or longitudinal relaxation[10]. In the Bloch sphere, the trace of it indicates a straight line from $|1\rangle$ to $|0\rangle$ through the sphere center. The average time for the evolution is usually written as T_1. We can use the Kraus operator to describe the process quantitatively[11]:

$$\rho(t+\Delta t) = \sum_{i=0,1} K_i \cdot \rho(t) \cdot K_i^\dagger \tag{1.8}$$

where:

$$K_0 = \begin{pmatrix} 1 & 0 \\ 0 & e^{-\Delta t/2T_1} \end{pmatrix}, K_1 = \begin{pmatrix} 0 & \sqrt{1-e^{-\Delta t/T_1}} \\ 0 & 0 \end{pmatrix} \tag{1.9}$$

After evolving Δt time, the density matrix becomes:

$$\rho(t+\Delta t) = \begin{pmatrix} \rho_{00}(t) + (1-e^{-\Delta t/T_1})\rho_{11}(t) & \rho_{01}(t)e^{-\Delta t/2T_1} \\ \rho_{10}(t)e^{-\Delta t/2T_1} & \rho_{11}(t)e^{-\Delta t/2T_1} \end{pmatrix} \tag{1.10}$$

The other relaxation is called dephasing, also pure dephasing time T_2^*. The trace of it is a straight line from a point on the equator on the Bloch sphere to the center. The three Kraus operators to describe the system are:

$$K_0 = e^{\Delta t/2T_2^*}, K_1 = \begin{pmatrix} \sqrt{1-e^{\Delta t/T_2^*}} & 0 \\ 0 & 0 \end{pmatrix}, K_2 = \begin{pmatrix} 0 & 0 \\ 0 & \sqrt{1-e^{\Delta t/T_2^*}} \end{pmatrix} \tag{1.11}$$

, and the density matrix becomes:

$$\rho(t+\Delta t) = \begin{pmatrix} \rho_{00}(t) & \rho_{01}(t)e^{-\Delta t/T_2^*} \\ \rho_{10}(t)e^{-\Delta t/T_2^*} & \rho_{11}(t) \end{pmatrix}. \tag{1.12}$$

Pure dephasing only affects the off-diagonal terms in the density matrix. We shall notice that the energy relaxation also affects the off-diagonal terms, so we define a dephasing or transverse relaxation time T_2:

$$\frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_2^*} \tag{1.13}$$

Quantum information

In classical information, we have Shannon entropy $\mathrm{H} = -\sum_{i=1}^{n} P(x_i)\log P(x_i)$. The quantum analog version is Von Neumann entropy:

$$S(\rho) = -\mathrm{Tr}(\rho \ln \rho). \tag{1.14}$$

This entropy measures the uncertainty of a quantum system and can be potentially used in quantum machine learning[12].

There are several important theorems in quantum information[11]:

no-cloning theorem Any ket state $|\Psi\rangle$ cannot get a duplication.

no-converting theorem No quantum state can be transferred into classical bits.

no-deleting theorem The number of qubits after gate operations are conserved, and no destructive gate exists in the quantum world.

no-broadcast theorem Prevent an arbitrary qubit from delivering to multiple recipients.

no-hiding theorem The information in the qubit never disappears. It may leak into the subspace of the environment but not vanish.

Notice that although there are five theorems, some of them can be mutually agreed upon. For example, from the no-cloning theorem, we can confidently say a no-broadcast theorem because if the latter is wrong, there will be more than one duplication of the qubit, which doesn't make sense. The no-converting theorem is called the no-transportation theorem in some textbooks. Still, since we can actually do quantum teleportation, it is more reasonable to use this name of the theorem instead.

Physical realization of quantum computer

The ultimate question after the theory is if we can realize quantum computers in the physical world. Physicist D.DiVincenzo raised five criteria on quantum computing.[13]

1. The system is scalable and along with well-controlled qubits
2. Qubits can be initialized to a simple state.
3. Much longer coherence time compared to single qubit gate manipulation time.
4. A universal gate set.
5. Decent qubit readout system.

Scientists have used many physical systems to build controllable quantum bits, some of which partly satisfy DiVincenzo's criteria.

Other than quantum computing, quantum technology applications also include quantum key distribution (QKD). In 2017, a Chinese team[14] successfully demonstrated QKD over a distance of 1200 kilometers.

1.3 Layout of the thesis

In **Chapter 2**, we investigate the basic concept of quantum computing, including quantum information and two-level systems. Additionally, we introduce the physics of charge qubit, transmon, and gatemon, then circuit quantum electrodynamics (circuit QED) and its implementation in superconducting qubit systems. **Chapter 3** describes the simulation and fabrication of our devices. Then the setup on both DC transportation measurement on lock-in and high-frequency measurement on VNA. **Chapter 4** involves three DC measurement data of shadow S-Sm-S junction tantalum InAs nanowires in both board station (with $T_{env} \approx 5K$) and in dilution fridge (with $T_{env} \approx 25mK$). **Chapter 5** shows the high-frequency transmission measurement of wet etched sputter tantalum resonator, with different cleaning processes and shielding techniques, in our dilution fridge.

2 Superconducting circuit quantum devices

In this part, we briefly discuss quantum information, then the quantum mechanics used in qubit manipulation and readout. Furthermore, the LC circuit, transmon, and gatemon physics are demonstrated.

I'm going to briefly introduce some quantum mechanics here to offer a better understanding of the later content. Let's begin with the most well-known time-dependent Schrödinger equation:

$$i\hbar\frac{\partial\Psi}{\partial t} = \mathbf{H}\Psi = (-\frac{\hbar^2}{2m}\nabla^2 + \mathbf{V})\Psi \tag{2.1}$$

Where the left part is the Hamiltonian, the right is kinetic energy and potential energy operator. If we only treat the time evolution part, we get:

$$\Psi(t) = exp[-\frac{i}{\hbar}\int \mathbf{H}dt]\Psi(0) = \mathbf{U}(t)\Psi(0) \tag{2.2}$$

Where $\mathbf{U}(t)$ is the time evolution operator. This equation shows that even though our Hamiltonian is time independent, our wave function is still rotating ceaselessly.

Traditionally we use the first-quantized wave function:

$$\Psi[\mathbf{r_i}] = \prod_{i=1}^{N}\psi_{\alpha_i}(\mathbf{r}_i) \equiv \psi_{\alpha_1}\otimes\psi_{\alpha_2}\otimes...\otimes\psi_{\alpha_N} \tag{2.3}$$

that is the direct product of all the individual wave functions in Hilbert space to calculate the total wave function. However, it would be more concise to use second quantization in the future quantum technology study. Instead of asking the state of each particle, we seek the number of particles in each state, which is the Fock state:

$$|\Psi\rangle = |n_1, n_2, ..., n_k, ...\rangle, \sum n_k \equiv N \tag{2.4}$$

N is the total number of particles. We can more easily calculate the hamiltonian of the system in this way. Moreover, it provides an intuitive way for people to understand the composition and evolution of the system.

2.1 Transmon

Quantum harmonic oscillator

Suppose we have a capacitor C and an inductor L that are connected. By Kirchhoff's law, their voltage should be the same:

$$V_C + V_L = 0 \tag{2.5}$$

Therefore, we can write the equation of motion for magnetic flux in the inductor and the charge on the capacitor as

$$\dot{Q} = -\Phi/L, \quad \dot{\Phi} = Q/C \tag{2.6}$$

which endows a frequency $\omega_0 = 1/\sqrt{\mathrm{LC}}$. Note that in normal metal without the superconducting state, this frequency is actually the collective movements of electrons. Still, there are many degrees of freedom for phonon and electron states. Recall that the energy stored in the capacitor and inductor is:

$$T_C = \frac{Q^2}{2C} = \frac{C\dot{\Phi}^2}{2}, \quad V_L = \frac{LI^2}{2} = \frac{\Phi^2}{2L} \tag{2.7}$$

where T_C, U_L corresponds to the kinetic energy and the potential energy. Now the Lagrangian of LC circuit in flux basis is:

$$L = \frac{C\dot{\Phi}^2}{2} - \frac{\Phi^2}{2L} \tag{2.8}$$

and hamiltonian is:

$$H = \frac{Q^2}{2C} + \frac{\Phi^2}{2L} \tag{2.9}$$

end of classical derivation.

To start dealing with the quantum world, we first check if the charge and flux coordinates can be propagated to operators by the Poisson bracket:

$$\{\Phi, Q\} = \frac{\delta\Phi}{\delta\Phi}\frac{\delta Q}{\delta Q} - \frac{\delta Q}{\delta\Phi}\frac{\delta\Phi}{\delta Q} = 1 \tag{2.10}$$

Therefore, we can endow the two canonical variables with the commutator[15]:

$$\begin{aligned} &\Phi \to \hat{\Phi} \\ &Q \to \hat{Q} \\ &[\hat{\Phi}, \hat{Q}] = i\hbar \end{aligned} \tag{2.11}$$

which enables us to quantize the circuit:

$$\mathbf{H} = \hbar\omega(a^\dagger a + \frac{1}{2}) \tag{2.12}$$

by using

$$\begin{aligned} [a, a^\dagger] &= 1, \\ \hat{\Phi} &= \sqrt{\frac{\hbar Z}{2}}(a + a^\dagger), \\ \hat{Q} &= -i\sqrt{\frac{\hbar}{2Z}}(a - a^\dagger) \end{aligned} \tag{2.13}$$

where resonant frequency and impedance are respectively

$$\begin{aligned} \omega &= \sqrt{\frac{1}{LC}}, \\ Z &= \sqrt{\frac{L}{C}} \end{aligned} \tag{2.14}$$

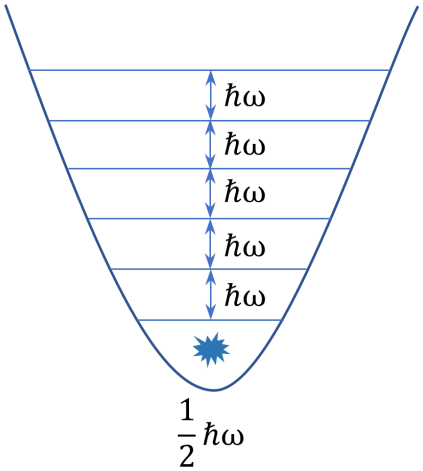


Figure 2.1: The energy levels inside the potential well. The lowest level it can reach is $1/2\hbar\omega$.

So now we get an oscillator with evenly split energy levels. However, to utilize it in quantum computing, the system needs anharmonicity to avoid energizing particles to levels other than the ground and first excited state. Many attempts[16–18] such as charge qubits, phase qubits, and flux qubits are demonstrated. None of them are strictly two-level system, but they all exhibit protections of two-level subspace. We describe these circuits as artificial atoms in the circuit quantum electrodynamics (circuit QED or cQED)[3,10,19]. In the following content, charge qubits, mostly transmon, will be the central part.

Josephson junction

Suppose we are BCS superconductor[20], then we introduce new basis $\hat{n} = \hat{Q}/2e$, $\hat{\phi} = 2\pi\hat{\Phi}/\Phi_0$, where Φ_0 is the magnetic flux quanta. If we sandwiched a thin insulator, like aluminum oxide, between two superconductors, we can get a Josephson junction (JJ). The current phase relation (CPR) of JJ is described as[21]:

$$I = I_0 \sin\phi \tag{2.15}$$

This is known as DC Josephson effect. If we apply a voltage across the junction, the phase difference will evolve:

$$\frac{d\phi}{dt} = \frac{2eU}{\hbar} \tag{2.16}$$

which is AC Josephson effect, with Josephson frequency $f_J = 483.6GHz \cdot U/mV$. These relations give Josephson junctions with non-linear inductance

$$L(\phi) = \frac{\Phi_0}{2\pi I_0 \cos\phi} \tag{2.17}$$

, which is crucial for the anharmonicity in superconducting qubits.

To draw out the current-voltage characteristics of JJs, we consider a simple model called resistively and capacitively shunted junction (RCSJ)[22]. The JJs now transform into a circuit composed of JJ, resistor, capacitor, thermal noise generator, and voltage source. Here through Kirchoff's law, we get:

$$I + I_N(t) = I_0 \sin\delta + \frac{U}{R} + C\dot{U}. \tag{2.18}$$

Replace voltage with AC Josephson effect:

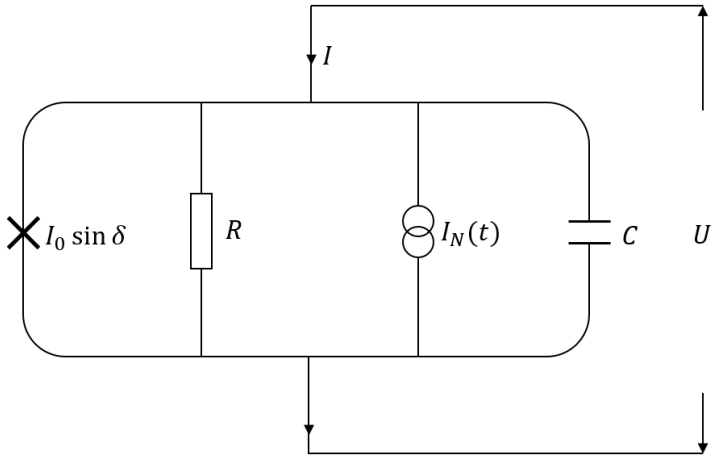


Figure 2.2: The equivalent circuit for RCSJ model. The circuit components from left to right are: Josephson junction, resistor, thermal noise generator and capacitor.

$$I + I_N(t) = I_0 \sin\delta + \frac{\Phi_0}{2\pi R}\dot{\delta} + \frac{\Phi_0 C}{2\pi}\ddot{\delta} \tag{2.19}$$

. Change time t to Josephson time constance $\tau = t\omega_c$ with characteristic frequency $\omega_C = \frac{2\pi}{\Phi_0} I_0 R$, the equation of motion eventually becomes:

$$\beta_C \ddot{\delta} + \dot{\delta} + \sin\delta = \frac{I}{I_0} + \frac{I_N}{I_0} \tag{2.20}$$

with Stewart-McCumber parameter $\beta_C = \frac{2\pi}{\Phi_0} R^2 C$. While the system is overdamped with $\beta_C \ll 1$, the system is not hysteresis. Namely, the critical current and the retrapping current are the

same, and vice versa. The JJs used in our experiment are mostly underdamped then hysteresis with retrapping current $\frac{I_r}{I_0} \approx \frac{4}{\pi}\frac{1}{\sqrt{\beta_c}}$, therefore while searching for the critical current of JJs, we usually scan from superconducting state to normal state.

Charge qubit

In many experiments, the JJs are superconductor-insulator-superconductor (SIS) junctions. We replace the linear inductor term and get the Hamiltonian[23]:

$$\hat{H} = 4E_C(\hat{n} - n_g)^2 - E_J \cos\hat{\phi} \tag{2.21}$$

where

$$E_J = \Phi_0 I_c / 2\pi \tag{2.22}$$

is the Josephson energy, $E_c = e^2/2(C_g + C_J)$ is the charging energy and $n_g = Q_r/2e + C_g V_g/2e$, as Q_r the charge in the environment. In the extreme of $E_C \gg E_J$, we can create a Cooper Pair Box (CPB), namely, charge qubit. After numerically solving, diagonalizing in charge basis, charge qubit can be intuitively imaged by its hamiltonian:

$$\hat{H} = 4E_C \sum_N (\hat{n} - n_g)^2 |N\rangle\langle N| - \frac{1}{2}E_J \sum_N (|N\rangle\langle N+1| + |N+1\rangle\langle N|) \tag{2.23}$$

, where N is the number of Cooper pairs inside the island. The energy band is shown below (Fig 2.3). Notice that when $N_g = 0$, if we have $N = 0$, we are in $|0\rangle$, ground state, and same for 1. When we slowly charge the island to N = 1/2, we can get $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$. Although the mechanics look easy, the realization of it is hard since the environment is perturbing the system all the time, causing decoherence.

Transmon

To reach the goal of mitigating the charge noise, people try to engineer the charge-Josephson energy relationship in the CPB, flattening the potential on each level. Here transmon, that is, transmission line shunted plasma oscillation qubit, comes out and immediately becomes popular in many laboratories.[24,25]

Now, the system is in a different regime, where $E_J \gg E_c$, the charge sensitivity is suppressed, and anharmonicity is still maintained. Neglect the charge offset and do Maclaurin expansion on Eq.2.23, we get transmon Hamiltonian:

$$\mathbf{H} = 4E_C\hat{n}^2 - E_J + \frac{E_J\hat{\phi}^2}{2} - \frac{E_J\hat{\phi}^4}{24} + \mathscr{O}(\hat{\phi}^6). \tag{2.24}$$

with eigenenergies:

$$E_m \simeq -E_J + \sqrt{8E_C E_J}(m + \frac{1}{2}) - \frac{E_C}{12}(6m^2 + 6m + 3). \tag{2.25}$$

Notice that the negative quadratic term offers $\alpha = \omega_q^{1\to2} - \omega_q^{0\to1} = -E_C$, the system's anharmonicity, a negative number around 100 - 300 MHz in transmon. The desirable operating transmon qubit frequency is 3 - 6 GHz.

To tune the frequency of transmon, we can introduce a parallel Josephson junction circuit instead of a single Josephson junction and apply a magnetic field in the loop. This technique is also called superconducting quantum interference device (SQUID) and can be used in detecting an extremely subtle magnetic field. The theory behind the SQUID is the integer number of superconducting flux quanta equals the sum of all the phase components across the Josephson junctions, that is:

$$\phi_1 - \phi_2 + \phi_e = 2\pi k \tag{2.26}$$

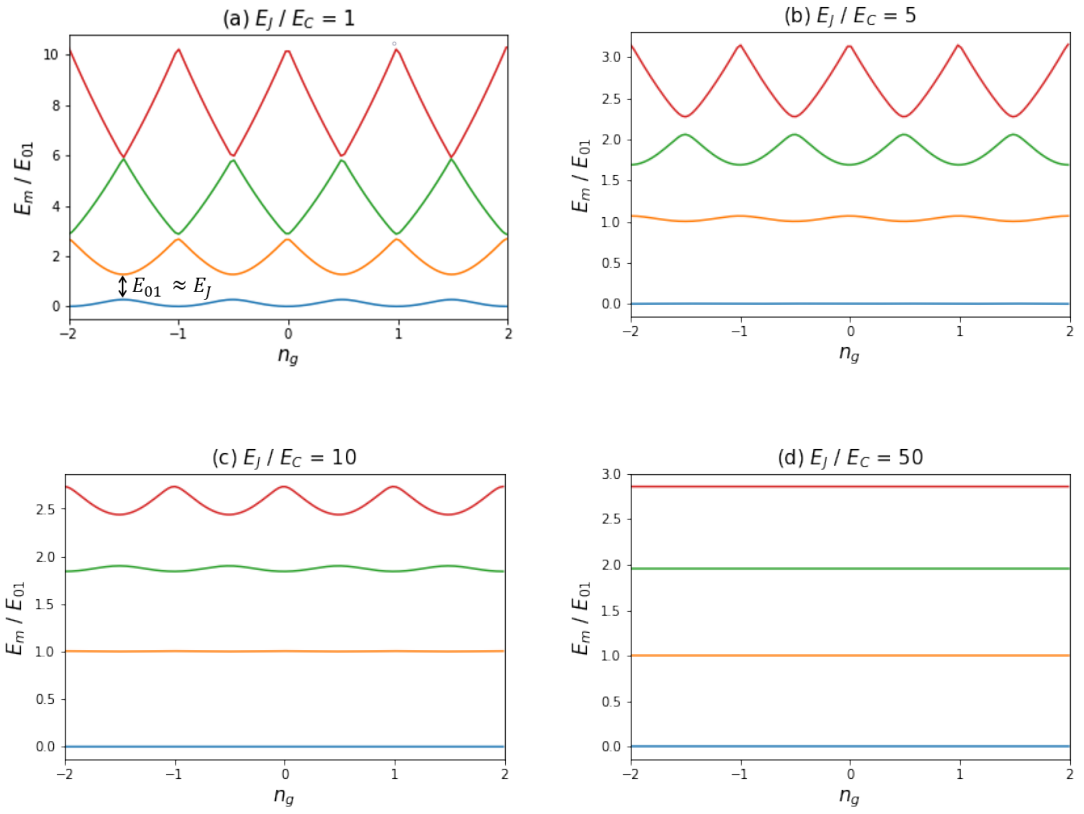


Figure 2.3: The energy level of transmon respect to different E_J/E_C. The x-axis is the total Cooper pairs number in the qubit island. Notice that the energy is less sensitive to charge when E_J/E_C becomes larger

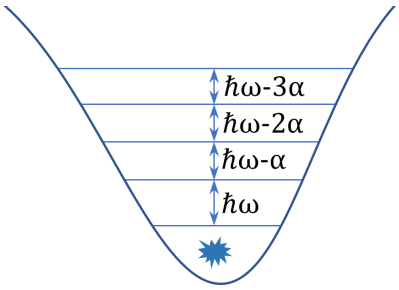


Figure 2.4: The cosine potential well, along with the energy level of transmon. The excitation energy $\hbar\omega_{1\to2}$, $\hbar\omega_{2\to3}$ are calculated according to Eq 2.25. Nonlinearity gives a different transition frequency between levels and therefore protects the qubits in the ground and first excited subspace.

. Rewriting the Hamiltonian of Josephson junction into[24]:

$$\hat{H}_J = -E_{J1}\cos\hat{\phi}_1 - E_{J2}\cos\hat{\phi}_2 \tag{2.27}$$

, and then combine Eq 2.26 and Eq 2.27, we get the Josephson junction Hamiltonian:

$$\hat{H}_J = -E_{J\Sigma}\cos\left(\frac{\pi\Phi}{\Phi_0}\right)\sqrt{1+d^2\tan^2\left(\frac{\pi\Phi}{\Phi_0}\right)}\cos\left(\hat{\varphi}-\varphi_0\right) \tag{2.28}$$

, where $\varphi = (\phi_1+\phi_2)/2$ and $E_{J\Sigma} = E_{J1}+E_{J2}$. The effective Josephson energy can write as:

$$E_{J\text{eff}} = -E_{J\Sigma}\cos\left(\frac{\pi\Phi}{\Phi_0}\right)\sqrt{1+d^2\tan^2\left(\frac{\pi\Phi}{\Phi_0}\right)} \tag{2.29}$$

. Now we get a similar Josephson energy formula to the normal transmon one, and we can utilize this external field to gain more degree of freedoms in qubit.

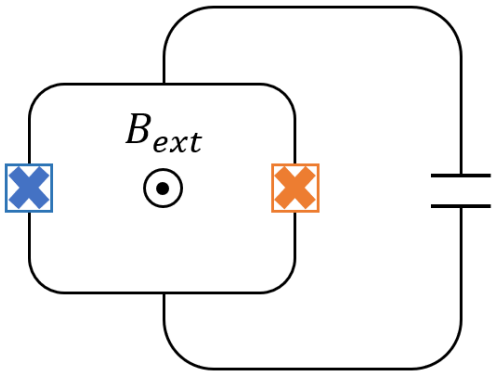


Figure 2.5: A flux tunable transmon with symmetric Josephson junction. The magnetic field is usually generated from a flux line close to the SQUID.

2.2 Gatemon

The previous section introduces frequency tunable transmon through magnetic flux, which idea is crucial in quantum computing since we can use it to do fast gate operations and reduce frequency-dependent noise[26]. However, this system has downsides like heat dissipation from the current flowing through the flux line, the crosstalk among qubits, and flux noises[27]. To eliminate these downsides, we introduce a new system called gatemon, also known as semiconductor gate tunable transmon[28].

Proximitized effect

Imagine a normal metal that is connected by superconductors on both sides. Since it is the cooper pairs that are conducting in the BCS superconductor, when they enter the normal metal, it remains 'pairs' because of the non-locality of particles as long as the characteristic length is longer than the connection[29]. This effect is called proximitized effect, and it is used in nowadays' quantum device[30]. To gain control of this effect, we can use a semiconductor as the connection and implement a nearby gate. By tuning the gate voltage, the bare semiconductor will feel a large electric field and reduce its conductivity channels. In the extreme case, we can completely pinch off the semiconductor, making it act as an infinity resistance component. There are several ways of realizing the tunable connection, such as 2-dimensional electron gas (2DEG), and semiconductor-superconductor hybrid nanowire with S-N-S junction.

Andreev reflection

The detailed mesoscopic explanation of the boundary of the N-S surface for this effect is described by Andreev Reflections. There are two branches of excitations in semiconductor, electron with charge $-e$, momentum $\mathbf{p}$, and group velocity $\mathbf{v_p}$, and holes with charge e and group velocity $\bar{\mathbf{v}}_\mathbf{p} = -\mathbf{v_p}$. In N-I surface, the electron will experience specular reflection, endow the outgoing electron $\mathbf{p}' = \mathbf{p} - 2\hat{\mathbf{n}}(\hat{\mathbf{n}} \cdot \mathbf{p})$. However, for the N-S interface, the electrons undergo the retro reflection, generate holes with opposite momentum and shoot Cooper pairs into the superconductor subgap. Due to the impurities and defects that exist on the interface, there is still a finite probability that the electrons reflect specularly, resulting in an imbalance charge transfer between leads.

N-S interface was theoretically discussed in the 1970s but did not gain attention until decades later[31,32]. One important model for describing metallic to tunneling regime transi-

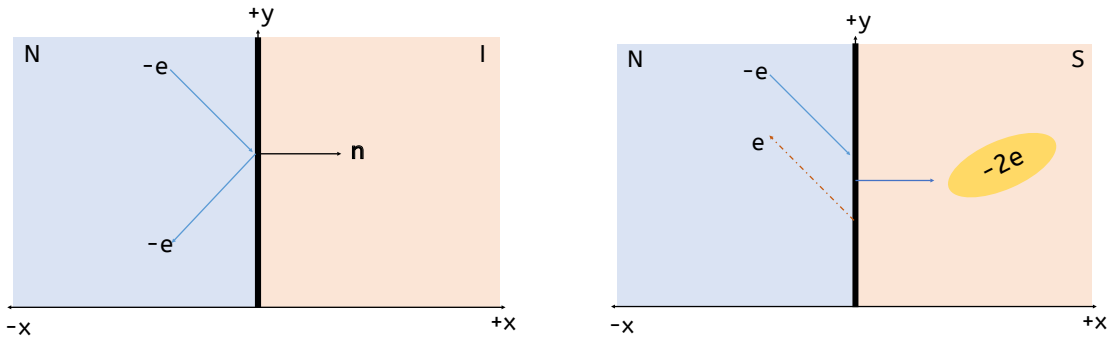


Figure 2.6: (a) Specular reflection with no generation of quasi-particles at the normal metal (semiconductor) -insulator (NI) interface. **n** is the normal vector of the interface (b) Andreev reflection with the generation of Cooper pair inside the superconductor

tion on semiconductor is introduced by Blonder, Tinkham, and Klapwijk (BTK) theory[31], which introduces a barrier strength Z to quantitatively indicate the number of impurities and defects on the boundary. We write the plane wave solution of particle as $|k_0\rangle = \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} e^{ikr}$, as u_0 and v_0 are coherence factors of electrons and holes, and get the propagating wave in the semiconductor:

$$\Psi_N(r) = \begin{pmatrix} 1 \\ 0 \end{pmatrix} e^{ik_n^+ r} + A(E) \begin{pmatrix} 0 \\ 1 \end{pmatrix} e^{ik_n^- r} + B(E) \begin{pmatrix} 1 \\ 0 \end{pmatrix} e^{-ik_n^+ r} \tag{2.30}$$

, where A and B are probability amplitudes of Andreev reflection and specular reflection. Similarly, in the superconductor, we have:

$$\Psi_S(r) = C(E) \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} e^{ik_s^+ r} + D(E) \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} e^{-ik_s^- r} \tag{2.31}$$

, which describes the transmission of electrons without and with branch crossing. By the number conservation of particles, there must be:

$$A(E) + B(E) + C(E) + D(E) = 1 \tag{2.32}$$

and we get the general form of solution:

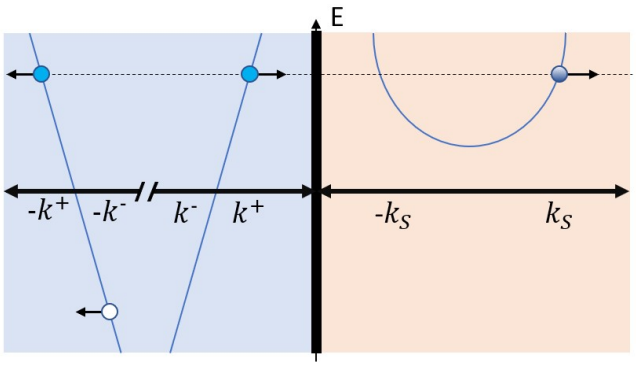


Figure 2.7: The BTK theory model schematic. The normal metal electrons (blue) on the left side undergo Andreev reflections and specular reflections. The quasi-particles (holes and electrons) are formed on the superconductor side. The superscript + and - on k means electrons and holes

$$|A| = \begin{cases} \dfrac{\Delta^2}{E^2 + (\Delta^2 - E^2)(1+2Z^2)^2} & \text{for } E < \Delta \\ \dfrac{u_0^2 v_0^2}{\gamma^2} & \text{for } E > \Delta \end{cases}, |B| = \begin{cases} 1 - |A|^2 & \text{for } E < \Delta \\ \dfrac{(u_0^2 - v_0^2)^2 Z^2 (1+Z^2)}{\gamma^2} & \text{for } E > \Delta \end{cases} \tag{2.33}$$

where $\gamma^2 = [u_0^2 + Z^2(u_0^2 - v_0^2)]^2$, and $u_0^2 = 1 - v_0^2 = \frac{1}{2}\{1 + [(E^2 - \Delta^2)/E^2]^{\frac{1}{2}}\}$. Since the transmission rate at N-S interfaces below the superconducting gap is 0 ($C(E) = D(E) = 0$), we can then utilize these solutions to find current:

$$I_{NS} = \frac{2e}{h}\int [f(E - eV)][1 + A(E) - B(E)]d \tag{2.34}$$

with f the Fermi-Dirac distribution functions and V the bias voltage across the interface. Overall, we can say that Andreev reflections describe the cooper pairs breaking into electron-hole pairs inside the semiconductor, then creating non-conventional superconductivity [33].

Multiple Andreev Reflection

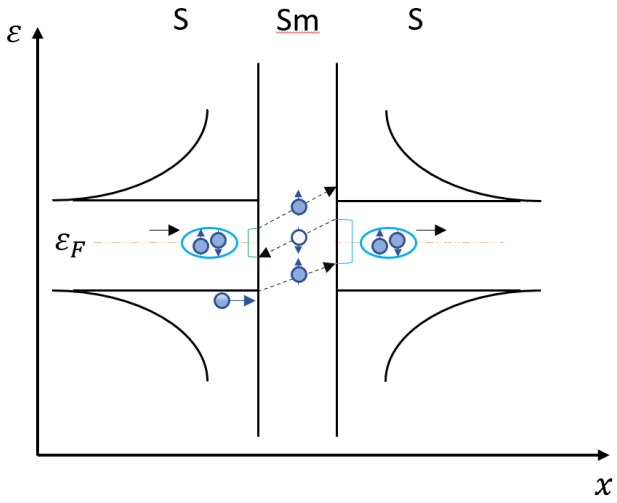


Figure 2.8: The demonstration of multiple Andreev reflections of order 3. The x-axis is spacial distance and y-axis is electron energy.

A phenomenon emerges when two N-S interfaces are encapsulated between two superconducting leads on a small scale. Electrons in semiconductors first hit the N-S interface through Andreev reflection, creating a hole that bounces back. The hole again hits the other N-S interface and bounces back. This process with multiple bounces is called Multiple Andreev Reflection (MAR), with orders $n+1$ where n is the number of AR.

In this scenario, the threshold voltage can be represented as:

$$V_{th} = \frac{2\Delta}{en} \tag{2.35}$$

which can provide conductance peaks in the junctions' I-V characteristic. It's worth noticing that the MAR is observed only when the barrier strength Z is small and the transmission probability is high. Given the phase coherence between the two Andreev reflection processes, a subgap state, Andreev Bound State (ABS), is formed and can be readout through high-frequency measurement [34].

Andreev bound state

Andreev bound state is the essential process that happens inside the semiconductor. The states are characterized by their transmission eigenvalues T_i [35]. We can write the ground and excited state energy of the ABS as:

$$E_{ABS}(T, \delta) = \mp\Delta\sum_i \sqrt{1 - T_i \sin^2\left(\hat{\delta}/2\right)} \tag{2.36}$$

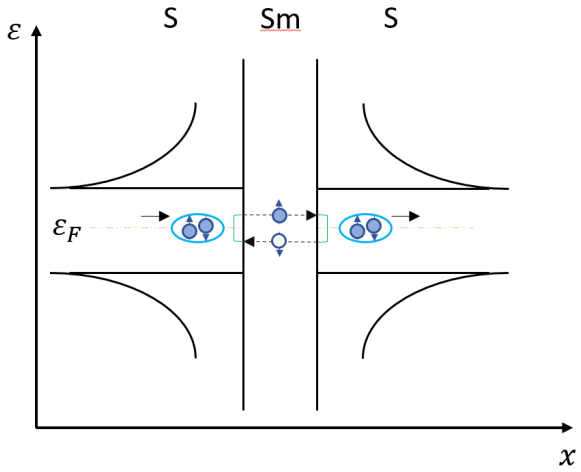


Figure 2.9: The Andreev bound state happens inside the semiconductor.

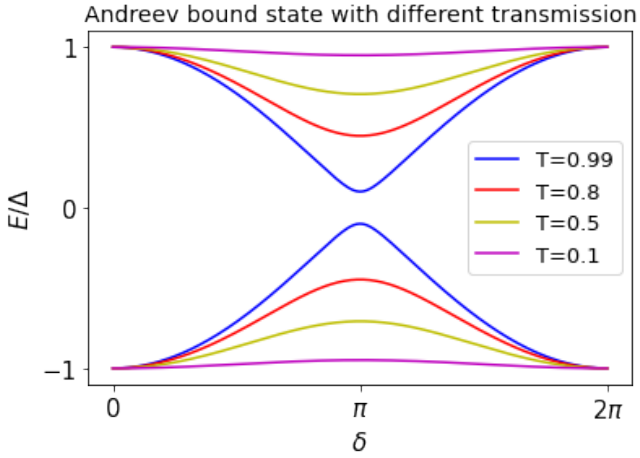


Figure 2.10: The ABS energy in phase space with different transmission rate. When the transmission is 1, the energy gap between the states is closed at $\phi = \pi$.

Then we use Taylor expansion on the ground state energy, substitute the result for the Josephson energy part in Eq 2.21, we can get the energy of each level in gatemon and the anharmonicity of the qubit with respect to the transmission rate (detail calculation is in Anders' PhD thesis[36]):

$$E_{12} - E_{01} = \alpha \approx -E_C \left(1 - \frac{3\sum T_i^2}{4\sum T_i}\right) \tag{2.37}$$

.

Therefore, with the S-Sm-S junction, the anharmonicity changes and it is related to the transparency of the N-S interface and the mean-free path of the electrons inside the junction.

2.3 Circuit QED readout and qubit control

Circuit-QED readout

Superconducting qubits usually need an auxiliary readout solution to obtain the system's state. Several readout strategies exist, like a SQUID as a sensitive magnetic flux detector and a single electron transistor as a sensitive charge detector. The qubit in our system is read out by coupling to a readout resonator, a harmonic oscillator system.

We can write a qubit transverse coupling to a resonator as following[10]:

$$H = \omega_r a^\dagger a - \frac{\omega_q}{2}\sigma_z + g(\sigma^- a^\dagger + \sigma^+ a) \tag{2.38}$$

, with g the coupling strength. The terms in the hamiltonian are resonator energy, qubit energy, and interaction. This formula is the well-known Jaynes-Cumming model, which describes the interaction between an opti0cal field and a two-level system. If the qubit and resonator frequency detune significantly compared to the coupling strength, that is $\lambda = g/\Delta \ll 1$ with $\Delta = \omega_q - \omega_r$, the system is in dispersive regime. We introduce a unitary transformation operator

$$U = \exp[\lambda(\sigma^- a - \sigma^- a^\dagger)] \tag{2.39}$$

and then the hamiltonian:

$$H_D = U_D H_D U_D^\dagger \approx (\omega_r - \chi\sigma_z)a^\dagger a - \frac{\omega_q + \chi}{2}\sigma_z \tag{2.40}$$

, here $\chi = g^2/\Delta$ is the dispersive shift. The hamiltonian tells us the resonator frequency will change by 2χ depending on the qubit state. Rewrite the Hamiltonian with terms in different basis:

$$H_D = \omega_r a^\dagger a - \frac{1}{2}(\omega_q + \frac{g^2}{\Delta} + \frac{2g^2}{\Delta}a^\dagger a)\sigma_z \tag{2.41}$$

. The additional $2g^2/\Delta$ term is called ac-Stark shift. This effect has resulted in photon number fluctuations leading to shifts in qubit frequency, thus dephasing.

We now have a circuit-QED-based gatemon qubit, and we want to read out and manipulate it through the co-planar waveguide, the on-chip circuit. From Eq 2.41 we already know how the readout system generally works. The circuit-QED into the resonator coupled system is described in Hamiltonian[24]:

$$H = 4E_C(\hat{n} - n_g)^2 - E_J\cos\hat{\phi} + \hbar\omega_r a^\dagger a + 2\beta V_{rms}^0 \hat{n}(a + a^\dagger) \tag{2.42}$$

, where $\beta = C_g/C_\Sigma$, with C_Σ the total capacitance to the ground and C_g the resonator qubit coupling capacitance, and $V_{rms}^0 = \sqrt{\hbar\omega_r/2C_r}$ the rms voltage of resonator. The final derivation after second quantization is the same as 2.41, but with $g = 2\beta e V_{rms}^0$.

Qubit control

Now assume we have prepared a two-level system, and our target is to investigate how the system evolves under external control source[37]. Suppose we use a microwave as the external control field:

$$\lambda(t) = E(t)\cos(\omega_d t + \xi(t)) \tag{2.43}$$

, where $\xi(t)$ is an arbitrary time-dependent phase factor for anharmonic oscillation, the Hamiltonian under laboratory (Schrodinger) frame is:

$$\mathbf{H}_L(t) = \sum_{n=0,1} \varepsilon_n |n\rangle\langle n| + \hbar\lambda(t)(|0\rangle\langle 1| + |1\rangle\langle 0|) \tag{2.44}$$

, with the ground state energy $\varepsilon_0 = -\hbar\omega_q/2$ and $\varepsilon_1 = +\hbar\omega_q/2$. We then want the Dirac picture, namely rotation frame hamiltonian $\mathbf{H}_R$. Suppose we have a rotation operator $\mathbf{R}$, with $|\Psi'(t)\rangle = \mathbf{R}|\Psi(t)\rangle$, combined with Eq.2.1:

$$\mathbf{H}'_\mathbf{R} = i\hbar\dot{\mathbf{R}}\mathbf{R}^\dagger + \mathbf{R}\mathbf{H_0}\mathbf{R}^\dagger \tag{2.45}$$

where $\mathbf{H_0}$ is the Hamiltonian of the state $|\Psi(t)\rangle$. The rotation operator can be formalized as:

$$\mathbf{R}(t) = \exp\{-i\sum_{n=0,1}(n - \frac{1}{2})[\omega_d t + \phi(t)]|n\rangle\langle n|\} \tag{2.46}$$

Plug Eq.2.44 and Eq.2.46 into Eq.2.45, and define a phase factor $\varphi(t) = \phi(t) - \xi(t)$, we obtain:

$$\mathbf{H}_R(t) = \frac{\hbar}{2}\mathbf{B}(t)\cdot\sigma \tag{2.47}$$

after rotating wave approximation (RWA). Here $\mathbf{B}(t) = (E(t)\cos\varphi(t), E(t)\sin\varphi(t), \dot{\phi}(t))$ is an effective external field, and σ is the Pauli operator $(\sigma_x, \sigma_y, \sigma_z)$. The driving frequency ω_d is usually tuned to be the same as ω_{01}.

Experimentally, we can treat the superconducting qubit as spin-$\frac{1}{2}$ particle and omit the constant energy term. By choosing the combination we needed in parameter space $(E(t), \phi(t), \varphi(t))$, we can manipulate the qubit freely.

Let's now focus on the qubit control on superconducting qubit. Consider an external drive source with signal V_D, the Lagrangian of the circuit with a harmonic oscillator (like a qubit):

$$\mathscr{L} = \frac{1}{2}C_J\dot{\Phi}^2 + \frac{1}{2}C_d(\dot{\Phi} - V_d)^2 - \frac{\Phi^2}{2L} \tag{2.48}$$

, where C_d is the drive-qubit coupling capacitance. The charges of the system $Q = \frac{\partial\mathscr{L}}{\partial\dot{\Phi}} = (C_J + C_d)\dot{\Phi}$, and the Hamiltonian becomes:

$$H = \frac{Q^2}{2(C + C_d)} + \frac{\Phi^2}{2L} + C_d V_d\dot{\Phi} - \frac{1}{2}C_d V_d^2 \tag{2.49}$$

. Generally, the coupling capacitance C_d is far smaller than C. So omit the last constant term and let $C_\Sigma = C_J + C_d$, we get:

$$H = \hbar\omega(a^\dagger a + \frac{1}{2}) - \frac{C_d V_d}{C_\Sigma}\sqrt{\frac{\hbar}{2Z_r}}\cdot i(\hat{a}^\dagger - a) \tag{2.50}$$

In qubit, the Hamiltonian simplify to two levels:

$$H_d = -\frac{1}{2}\hbar\omega_q\sigma_z + \Omega V_d\sigma_y \tag{2.51}$$

with $\Omega = \frac{C_d V_d}{C_\Sigma}\sqrt{\frac{\hbar}{2Z_r}}$. In rotation frame (Eq.2.45) with the time evolution operator (Eq.2.2), the Hamiltonian becomes:

$$\tilde{H}_d = \Omega V_d(t)(\cos(\omega_q t)\sigma_y - \sin(\omega_q t)\sigma_x) \tag{2.52}$$

Let $V_d(t) = V_0 v(t)$, and with generic electromagnetic wave form:

$$\begin{aligned} v(t) = &\quad s(t)\sin(\omega_d t + \phi) \\ = &\quad s(t)(\cos\phi\sin(\omega_d t) + \sin\phi\cos(\omega_d t)) \end{aligned} \tag{2.53}$$

where $s(t)$ is a dimensionless envelop function. Use the definitions:

$$\begin{aligned} I = &\quad \cos\phi \qquad \text{(In-phase component)} \\ Q = &\quad \sin\phi \quad \text{(Out-of-phase component)} \end{aligned} \tag{2.54}$$

with RWA approximation and set drive frequency $\omega_d = \omega_q$, we get:

$$\tilde{H}_d = -\frac{\Omega}{2}V_0 s(t)(I\sigma_x + Q\sigma_y) \tag{2.55}$$

The formula shows that the in-phase and out-of-phase pulse will rotate the qubit around the x-axis and the y-axis. For example, for an in-phase pulse, the time-evolution operator becomes:

$$U(t) = \exp([\frac{i}{2}\Omega V_0\int_0^t s(t')dt']\sigma_x) \tag{2.56}$$

By choosing the drive time, we can continuously drive the qubit around the x-axis.

2.4 Noise and decoherence

One important factor that limits the coherence time and high fidelity manipulations of qubits is the noise. Since our device is cooled down to around 20 mK (approximately 1.72 μeV in thermal energy), and the qubit transition energy f_{01}/h is 20μeV at 5 GHz, the heat excitation generated by phonons and the 50Ω resistors, namely Johnson noise is one minor source of white noise in the system. At this temperature and high frequency, Nyquist noise has a higher power density than Johnson noise, and it originates from the qubits' spontaneous emission to the environment. Another important noise is called $1/f$ noise with power spectrum density (PSD): $S(f) = 1/f^a$, where a is very close to 1. Shot noise is another major decoherence noise. The photon number fluctuation from the residue photons in the resonator generates a Lorentzian type PSD.

Any electromagnetic wave and phonon fluctuation from the environment, including cosmic rays from outer space[38], mechanical vibration from the vehicles, and excessive noise signal from wave generators will all influence the performance of the qubits. Moreover, the two-level system embedded inside defects and impurities on the metal, random electric and magnetic fields on the surface of the chip, and quasi-particles poisoning inside the Josephson junction are also affecting it.

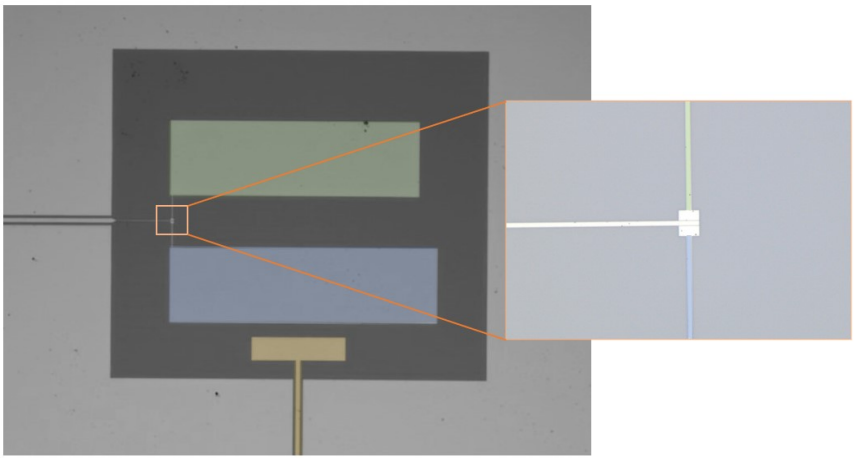
Some sources of noise are easily mitigated by implementing filters. For example, people have developed the suspension system for the dilution fridge to reduce the mechanical vibrations. To mitigate the thermal noise from electrons and photons, we use attenuators and infrared filter on the coaxial lines.

3 Devices fabrication and cryogenic measurement setup

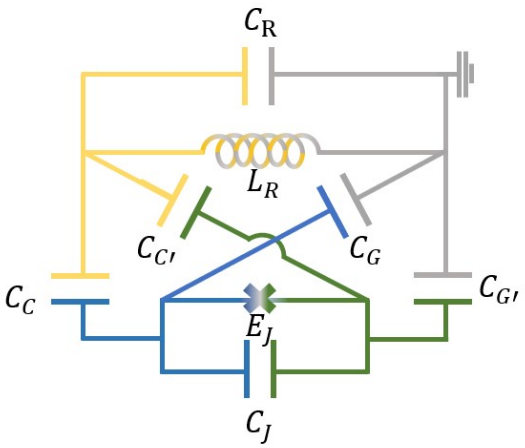
In this section, we will discuss the fabrication and installation of our devices and the circuit setup for the measurement. The overall process in our experiment is firstly fabrication, and then inspect the chip under the microscope and probably SEM, depending on which steps we are in. After that, we bond the chip on the daughter board and load the sample into the measurement and readout circuit in the 4K board station or dilution fridge. We use QCoDes and Labber to collect data and then analyze it in Python. All fabrications were done in the Center of Quantum Device, University of Copenhagen.

3.1 Qubit island design and simulation

Floating design



(a)



(b)

Figure 3.1: (**a**): False color overall floating design of the nanowire-based gatemon, the yellow pad with a downward line is connected to the resonator, and the left no color line is the electric field gate connected to a voltage source. The surrounding metal substrate is connected to the ground. (**b**): Equivalent circuit without the gate.

Our initial design is from A.Gyenis, similar to the floating design transmon circuit (Fig.3.1). The equivalent circuit can be drawn as Fig.3.1(b). The total capacitance in the charging energy

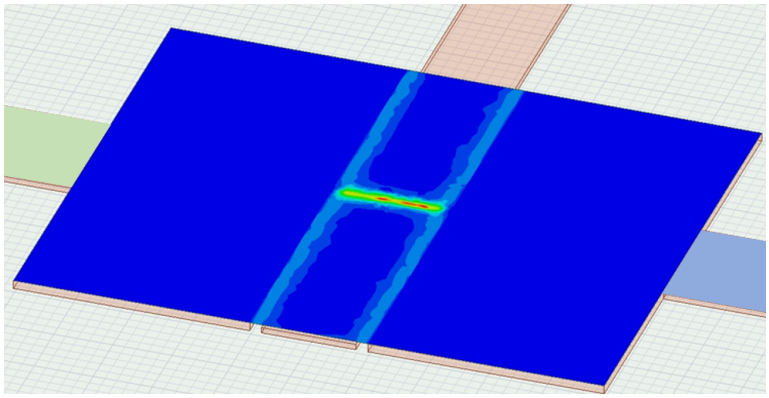


Figure 3.2: The electric field distribution at the bottom cross-section of the nanowire (displayed in blue). The left and right orange pattern is the contact

term is:

$$C_\phi = C_J + \frac{(C_C + C_G)(C_{C'} + C_{G'})}{C_C + C_{C'} + C_G + C_{G'}} \tag{3.1}$$

and coupling capacitance:

$$C_{coup} = \frac{C_{G'}C_C - C_{C'}C_G}{C_C + C_{C'} + C_G + C_{G'}} \tag{3.2}$$

Then we can calculate (All the units in energy is GHz and capacitance in fF):

$$\begin{aligned} E_C &= 19.37/C_\phi \\ \beta &= |\frac{C_\phi}{C_{coup}}| \\ g &= 0.125 \cdot \beta f_R (E_J/32E_C)^{\frac{1}{4}} \\ \hbar\omega_{01} &= \sqrt{8E_C E_J} - E_C \end{aligned} \tag{3.3}$$

where f_R is the resonator frequency that is can be simulated in HFSS and measured through VNA. E_J is the Josephson energy calculated from Ambegaokar-Baratoff relation[39]:

$$I_C R_N = \frac{\pi\Delta}{2e} \tag{3.4}$$

and Eq.2.22. The critical current can be tuned by the gate, and the normal resistance in our SNS junctions varies significantly, ranging from 4-30kΩ before exponentially resistance increase to pinch off. All the capacitance components can be calculated through Ansys Maxwell 3D.

To understand how the gate affects the nanowire, we also simulate the electric field in the design by Maxwell 3D under the distribution.

Impedance matching is also an important consideration while designing the circuit. Almost all the instruments and cables are designed at impedance $Z = 50\Omega$ to minimize the signal reflection in connections.

Grounded design

The floating design is not suitable for gatemon since the gate tunes the Fermi energy of both the lead and the junction simultaneously, making it hard to adjust the ω_{01} of the qubits. Hence grounded design is used to ensure one lead has definite chemical potential.

The calculation now becomes:

$$\begin{aligned} E_C &= e^2/2C_\Sigma \\ \beta &= |\frac{C_\phi}{C_{coup}}| \\ \hbar\omega_{01} &= \sqrt{8E_C E_J} - E_C \end{aligned} \tag{3.5}$$

Figure 3.3: The X-mon grounding design.

3.2 Resonator design and simulation

To measure multiple qubits through a transmission line (feedline) on the same chip, we need to carefully design the characteristic frequency of the resonators to avoid signal overlapping. The resonators are mutually coupled to the feedline and capacitively coupled to qubits, so it is a $\lambda/4$ resonator, and its frequency can be tuned by changing the distance of both ends.

The resonator spectroscopy through VNA is read by S_{21}, defined as V_2^-/V_1^+, the voltage ratio of the reflected wave from port 2 to the incident wave into port 1. One important parameter in determining the goodness of resonators is quality factors[40]:

$$Q = \omega_0 \frac{E_{tot}}{P_{loss}} = \frac{\omega_0}{\kappa} \tag{3.6}$$

with E_{tot} the total energy in the resonator and P_{loss} the dissipated power. κ, the decay rate, namely the inverse of photon lifetime in the resonator, is defined as the full width at the half maximum (FWHM) of the Lorentzian shape response in the S_{21} signal. The quality factor in the resonator can be further decomposed into internal and external (or coupling) quality factors:

$$\begin{array}{ccccc} \frac{1}{Q} & = & \frac{1}{Q_i} & + & \frac{1}{Q_e} \\ \kappa & = & \kappa_i & + & \kappa_e \end{array} \tag{3.7}$$

κ_i denotes the resonator spontaneous decay rate, and κ_e denotes the decay to the environment and the transmission line. In practice, we design the value of Q_e and constrain it in a reasonable interval to make a trade-off in the readout time and T_1 of the qubits.

We use HFSS to simulate the Q external quality factor by varying the distance between the feedline and the resonator. The estimated Q_i is around 1 million, so the corresponding Q_e should be more than 200-300 k. The resonance frequency is determined by the total length and shape of the resonator. To avoid the TWPA working frequency in our dilution fridge, we exclude the frequency at 6.6-6.75 GHz by design. In practice, the resonator's frequency might be shifted due to different materials and over or under-etched.

3.3 Nanowires with shadow junction

Our devices used in this thesis are all using In Situ growth shadow nanowires as SNS junctions to get highly transparent, clean interfaces. The Aluminum coat InAs/Sb nanowires are grown by Sabbir Khan with the series number Qdev 878[41], and Tantalum coat InAs nanowires are

by T.Kanne with the number QDev 1226. We also use the Tantalum nanowires[42] that are grown only for the N-S interface, but we can be lucky to find some nanowires that have S-N-S junctions.

Aluminum coated nanowires with shadow junctions

The Al shadowed nanowires are grown like crosses inside the trenches. Since the Al shadow wires are grown in purpose and the shadow junctions are formed with a high probability, there is no need to do SEM beforehand. We can pick the nanowires from one of the rows and quickly inspect them in SEM or AFM.

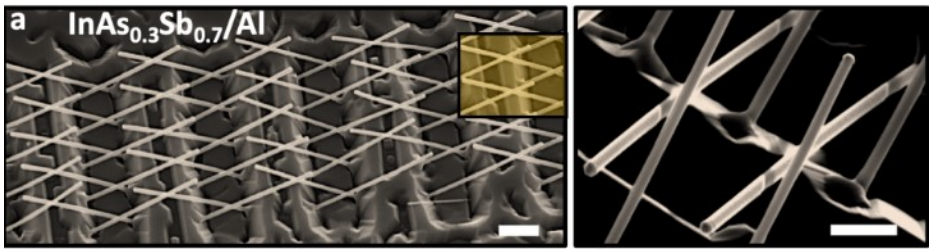
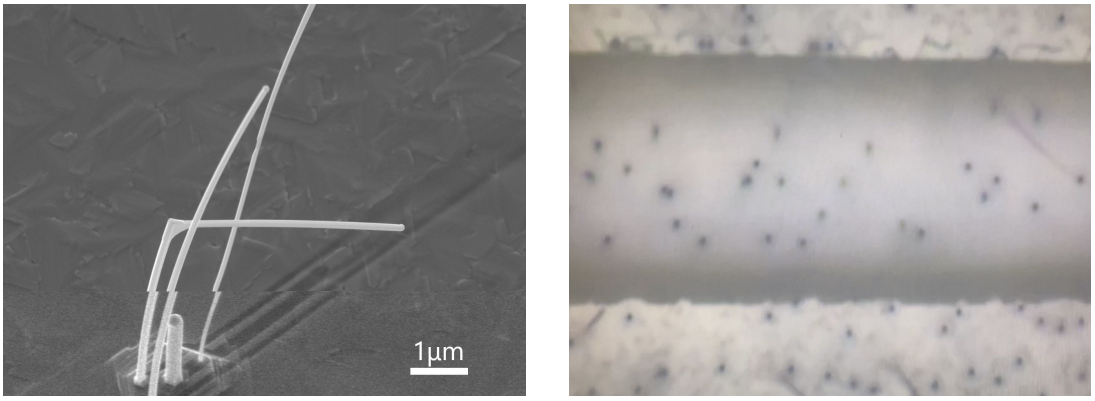


Figure 3.4: The structure of the $InAs_{0.3}Sb_{0.7}$/Al shadow nanowires, picture from Sabbir's paper[41] (scale bar is 500 nm)

This batch of nanowires is investigated heavily. These junctions can be tuned to a reasonably low critical current (10-15 nA) from many orders of MARs that show a low barrier on the S-N-S interface[41].

Tantalum coated nanowires with shadow junctions

However, the two Ta shadow nanowires' chips are in a different situation. Firstly, we need to go into SEM to locate the picking area we want. Then after proper rotation and tilt, we need to spend several hours in SEM to find wires with junctions and note them on paper. Then we move the chip to the micromanipulator and spend hours spotting and transferring the wires.



(a) ***(b)***

Figure 3.5: (a) The nanowires on chip QDev 1226, with shadow junction. (b) In the view in the micromanipulator's microscope (on QDev 551) with 100x magnification, the black dot indicates a nanowire.

Because of the doping problem and potentially carbon contamination[43], it is necessary to reduce the gross time on nanowires and try to lower the applied voltage as low as possible. We occasionally use the SEM system JOEL 7800F, which can rotate the chip in all directions to find the junction better while facing down toward the substrate. An alternative, less charging solution is to use Raith eLine to do SEM. Since it has an alignment mark locating system,

the nanowire can be found and photoed automatically in a short time. The system's downside is that it has no rotation motors, which might cause ambiguity when the junction face down. Besides, it locates in the cleanroom, so it takes us a long time to characterize the wires.

Most of the nanowires' inspections take less than 10 seconds, and gross inspection times less than 20 seconds. Sometimes due to the highly long nanowire and misfortune in the manipulator, the nanowires will be in SEM for a much longer time.

3.4 Aluminum based substrate chip fabrication and bonding

The chips are diced 10x10 mm from Silicon(111) wafer with 100nm aluminum by E-beam evaporation in AJA or molecular beam epitaxy (MBE). The MBE aluminum has fewer impurities and defects than AJA aluminum due to the cleaner environment and finer control of film growth. Thus MBE aluminum has less two-level system (TLS), dangling bonds left on Metal-Air, and Metal-Substrate surface that are accelerating qubits' decoherence. However, AJA aluminum is easier and faster to grow. Therefore, we use AJA aluminum for nanowires transportation property measurement and MBE aluminum for high-frequency measurement in the dilution fridge.

The fabrication is divided into five steps: alignment marks, control line, gate half etch (or deposition), nanowires transfer, and contact deposition.

Alignment mark:

1. Preclean: clean the chip in 1,3-dioxolane for 5 minutes, acetone for 5 minutes in sonication, and isopropyl alcohol (IPA) for 1 minute. Then dry the chip with nitrogen.

2. Spin coat: Coated by PMMA A4 with 4000rpm, 45s spin and baked on 180°C hotplate for 2 minutes. Inspection in the bright field of the microscope that the coat is even except for the edge is recommended.

3. Exposure: Load the chip into E-beam lithography ELS-F125, with dose 1000 μC/cm^2 and correct proximity effect correction (PEC) file.

4. Development: Dip it into MIBK:IPA 1:3 solution for 1 minute to do development, then inspect under the bright and dark field in the microscope. Ash by oxygen for 1 minute to remove (around 8 nm) the remaining resist inside the trenches.

5. Metal deposition: Load it into E-beam evaporation (AJA) to deposit 5nm Ti seed layer and 40nm Au.

6. Liftoff: Soak the chip into acetone for 30 minutes to lift off the resist with metal.

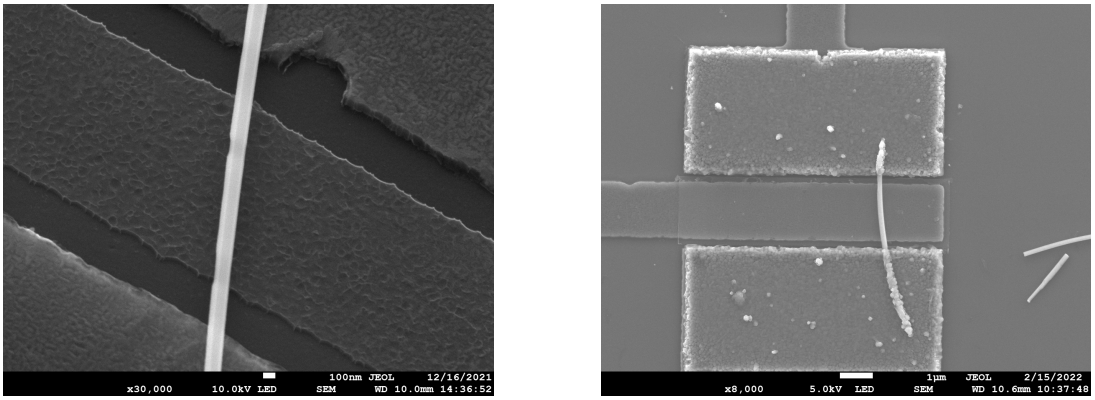
The control line process is similar to the alignment marks process in the first half, but after the development:

1. Postbake: Rest the chip for 2 minutes on the 115°C hot plate in order to harden the resist.

2. Etching: Dip the chip into 50°C of Transene Aluminum Etchant Type-D (TranseneD) for around 23 seconds (AJA aluminum) or 25 seconds (MBE aluminum) with slow agitation, then immediately soak it into 50°C milliQ for 20s and room temperature milliQ for 40s. Check under the microscope to see whether it is under-etched. If yes, redo the etching step but reduce the time in TranseneD to 3-5 seconds.

3. Strip: Soak the chip into acetone for 10 minutes to remove the resist.

Now, if 1. we want a half-etched gate, we can do the same as the control line process except for the around 8s aluminum etch in TranseneD during the etching step. This gate will separate the nanowire physically well from the bottom gate. 2. The other alternative process is depositing a 6nm Hafnium oxide ALD layer on top of the gate without etching. This method is targeted to increase the electric field strength felt by junctions and make them easier to pinch off. We will discuss this later in the result.



(a) ***(b)***

Figure 3.6: Left figure is the gate with half etch and right is the gate with direct deposition of 6nm ALD layer

Then the chip is transferred to the micro-manipulator, and we use 0.1-micrometer Tungsten tips to move the nanowires to the chip. Since the junctions are too small to see in the optical microscope, we usually use SEM to do a quick scan on nanowires and then go back and forth until we make all the junctions located above the gates. However, we discover that SEM will inject impurities and defects into the semiconductor and thus make the junction more conductive, with less probability of pinching off. One way to circumvent this issue is to use AFM to sense the location of the junction. It is experimentally successful sometimes, but it is also very likely to move the nanowire to a random place on the chip through Van der Waals force. Another solution provided is to use an optical surface profilometer to do harmless detection of junctions. We will try this method in our future development.

The final step is contact deposition. Since the nanowires can't withstand temperature at 180°C, we instead use 115°C to bake the resist:

1. Spin coat: First, we do EL9 with 4000rpm / 45 seconds, then 115°C baking on the hotplate. Then one more layer of EL9 and one layer of PMMA A4 with the same procedure. In total, three layers of resist are spun.

2. Exposure: Load the chip into ELS-F125 with dose 1000 μC/cm^2.

3. Development: Soak into MIBK:IPA 1:3 solution for 1 minute, then inspect under the bright and dark field in the microscope. Ash by oxygen for 1 minute.

4. DC milling: Load it into E-beam evaporation (AJA), use Kaufman ion milling (DC milling) with 300 V, 15 SCCM airflow, and 0.41 mbar for 1 minute to bombard the insulating oxidation layer.

5. Metal deposition: Deposit 300-400 nm aluminum with 1Å$/s$.

6. Liftoff: Soak the chip into acetone overnight.

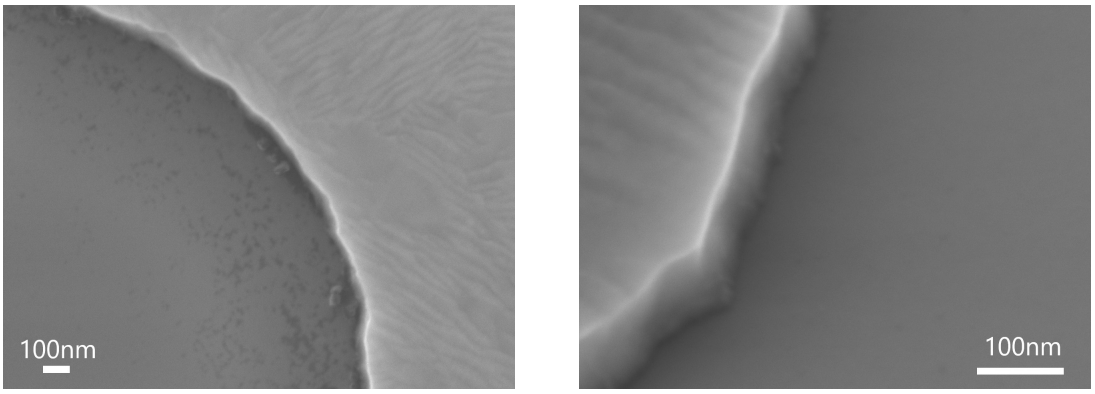
The bonding process depends on which board we are using. If we are using Copenhagen board v7p1 or v8p0 for DC measurement, then use PMMA A4 to glue the chip on the daughterboard and use F/S Bondtec 5630 bonder to connect the port and the chip. Finally, take an

overall picture of the board, and then the daughterboard with the chip is ready to load into the fridge and undergo measurement.

3.5 Tantalum based substrate fabrication

Recent research[44,45] demonstrates supreme performance on tantalum-based transmon, which can reach a 0.5 millisecond lifetime. As a consequence, tantalum probably is a great material for building a gatemon.

We ordered a 100 nanometers thick Tantalum on a 430μmsingle-side polished sapphire wafer from Star Cryoelectronics and diced it to 10x10 mm at Technical University of Denmark (DTU). The etchant we use is Transene 111 ($HF:HNO_3:H_2O$ = 1:1:1). While doing the exposure on sapphire, we need to scratch and fix the metal clamp at the edge of the chip to form direct contact with the metal on top of the substrate. Aside from this detail, the alignment mark process is the same as the aluminum substrate.



(a) ***(b)***

Figure 3.7: (a) The dots on the deep grey part shows that the etchant slightly attacks the substrate. (b) The etching leaves a sharp edge on tantalum.

The etchant containing a high concentration of nitric acid and hydrofluoric acid makes it hard to use E-beam resist on etching (see Appendix B for more detail). Thus, we use photolithography instead of e-beam lithography:

1. Spin coat: Use the pipette to drop AZ 5214E on the chip, and spin it at 4000 rpm / 45 seconds, then bake for 50 seconds on 110°C hotplate. Check the resist under the microscope with the yellow and green light filter to prevent pre-exposure on the resist.

2. Lithography: Load the chip into Heidelberg µPG 501 ultra-violet photolithography system. Set the defocus to 2 and dose to 30 ms.

3. Development: Fill a small size plastic beaker with AZ DEV (1:1). Develop the chip for 45 seconds with slow stirring for 3 seconds, and then rinse it into MilliQ for 30 seconds. Check under the dark-field microscope to see if any resist is left on the trenches (very important). Redo the lithography if there are many unwanted dots in the pattern. Then ash the chip for 2 minutes.

4. Etching: Postbake the chip on 120°C hotplate. Etch tantalum in room temperature Transene111 for 8 seconds with slow stirring (2 seconds per round). Then we rinse the chip into two beakers of MilliQ respectively for 20 seconds and 40 seconds.

5. Strip: Rinse the chip into 1,3-dioxolane for 10 minutes, acetone for 5 minutes, and MilliQ for 1 minute.

It is not recommended to use IPA in the last step since we have several reports on contamination left on the chip after using it, but never for MilliQ.

The ALD layer deposition is similar to the process on the aluminum substrate. However, to form a discharge layer on the floating patterns, we need to deposit a 15 nm aluminum layer on top of the resist before going into lithography. Remember to use the clamp on the discharge layer. After the exposure, we simply soak the chip into MF321 for 60 seconds, rinse it with MilliQ for 60 seconds and dry it. After confirming the disappearance of aluminum, the remaining development and ALD layer forming is the same as the previous one.

Contacts deposition also needs an extra discharge layer on top of the chip:

1. Spin coat: Two layers of EL9 and one layer of PMMA A4 with 4000rpm / 45 seconds and 115°C baking on the hotplate.

2. Discharge layer: Deposit 15 nm of aluminum on the resist in the AJA system.

3. Exposure: Load the chip into ELS-F125 with dose 1000 μC/cm^2 with a clamp on the discharge layer.

4. Etch discharge layer: Immerse the chip into MF321 for 60 seconds to fully etch out the aluminum, then rinse it with MilliQ for 60 seconds.

5. Development: Soak into MIBK:IPA 1:3 solution for 1 minute, then inspect under bright and dark field in the microscope. Ash by oxygen for 1 minute.

6. DC milling: Load it into the AJA system, use Kaufman ion milling with 300 V, 15 SCCM air flow, and 0.41 mbar for 1 minute to bombard the insulating oxidation layer.

7. Metal deposition: Deposit 300 nm aluminum with 1Å$/s$.

8. Liftoff: Soak the chip in acetone for more than 3 hours. Dry it after dipping into IPA for 30 seconds.

The edge on the tantalum pattern looks sharp, and the sapphire substrate is slightly attacked.

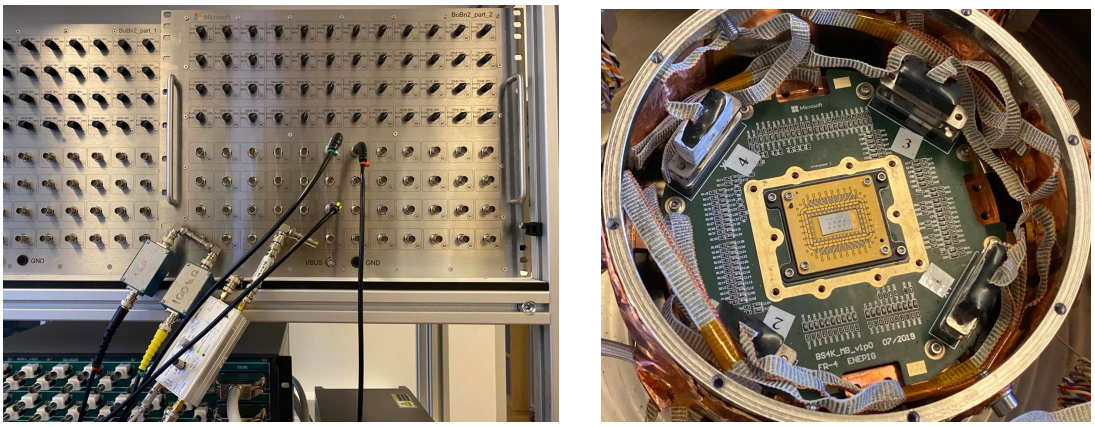
3.6 Board station setup

The board station is one cryogenic environment that we used mainly for testing the gate function on the chips. The model is CRX-4K Cryogenic Probe Station from Lake Shore, and the base temperature goes down to around 5 K on the temperature gauge.

The port on the daughterboard is connected to the breakout box. The fully cool down time of this station is less than 3 hours. Therefore it is truly convenient to test connectivity, gate functionality, and leakage in this system.

3.7 Dilution refrigerator setup

The dilution refrigerator is one of the most significant systems in our measurement. Its core physics process is the change of concentration of the Fermi gas like ^{3}He from dilute phase Bose statistics ^{4}He (More details in Pobell's textbook[46]). The cool-down operation has two stages: the first stage is called precooling, which takes the gas state of ^{3}He-^{4}He mixture into a pulse tube cooler and circulates in the mixing chamber, the final coldest part in the fridge. When the mixing chamber reaches 10 K, condensing process starts. The ^{3}He is continuously pumping into the mixing chamber, maintaining the 6.4% ^{3}He in ^{4}He rich phase inside. The still pump then keeps pumping the ^{3}He out from ^{4}He in the distiller (still) due to the lower latent heat, thus a higher vapor pressure of ^{3}He. Different concentration leads to an osmotic pressure $\Delta\pi$ between the mixing chamber and still, which 'sucks' ^{3}He to the still. The heat



(a) *(b)*

Figure 3.8: (a) The breakout box used to connect to the instruments for measurement. (b)The chip is loaded into the board station. The probe arms are all removed to lower the base temperature of the apparatus.

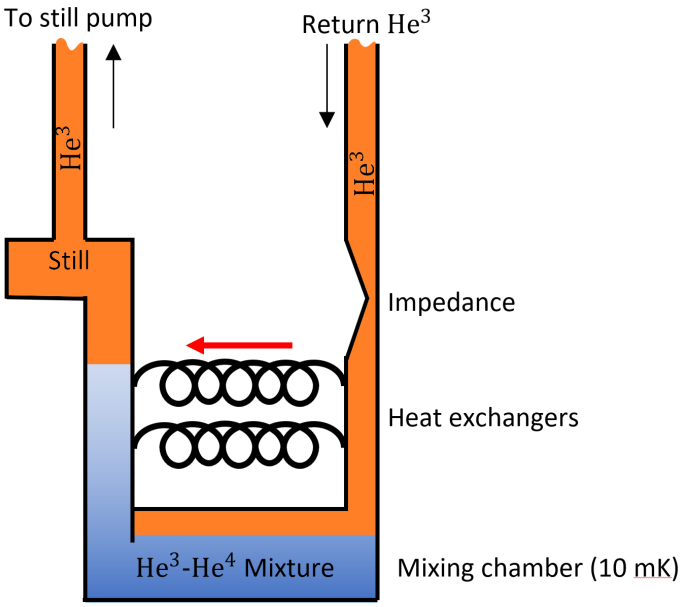


Figure 3.9: The mixing chamber and the distiller (still) in the dilution fridge. The impedance is used to condense the returning ^{3}He by Joule-Thompson expansion combined with the heat exchangers.

exchanger in between them is cooling down the returning ^{3}He. Theoretically, the mixing chamber can reach 10 mK by using this method.

The cryogenic environment in the fridge can enable the superconducting state of aluminum and tantalum on the chip, maintaining a high vacuum and suppressing the circuit's thermal excitation. Moreover, it is also responsible for filtering the external mechanical vibration and shielding the exterior electromagnetic wave.

The fridge we use is Triton 200 from Oxford Instrument, with a base temperature of 23 mK with our samples loaded. The wiring is shown in Fig 3.10. Besides the DC gate line connected to the bias-tee, there is a 24 ports DC loom with nano-D connectors linking directly to the motherboard for transportation measurement purposes. The DC lines are connected to the breakout box (BoB), the integrated board with the ground, float, and bus function on each port. The apparatuses are connected to the BoB through BNC cables for DC and SMA connector coaxial lines for high-frequency measurements. The in-going readout signal experiences 60 dB attenuation (more in the experiment. See Chapter 5) and a high-frequency filter. The out-going readout signal is subsequently amplified by superconducting traveling wave

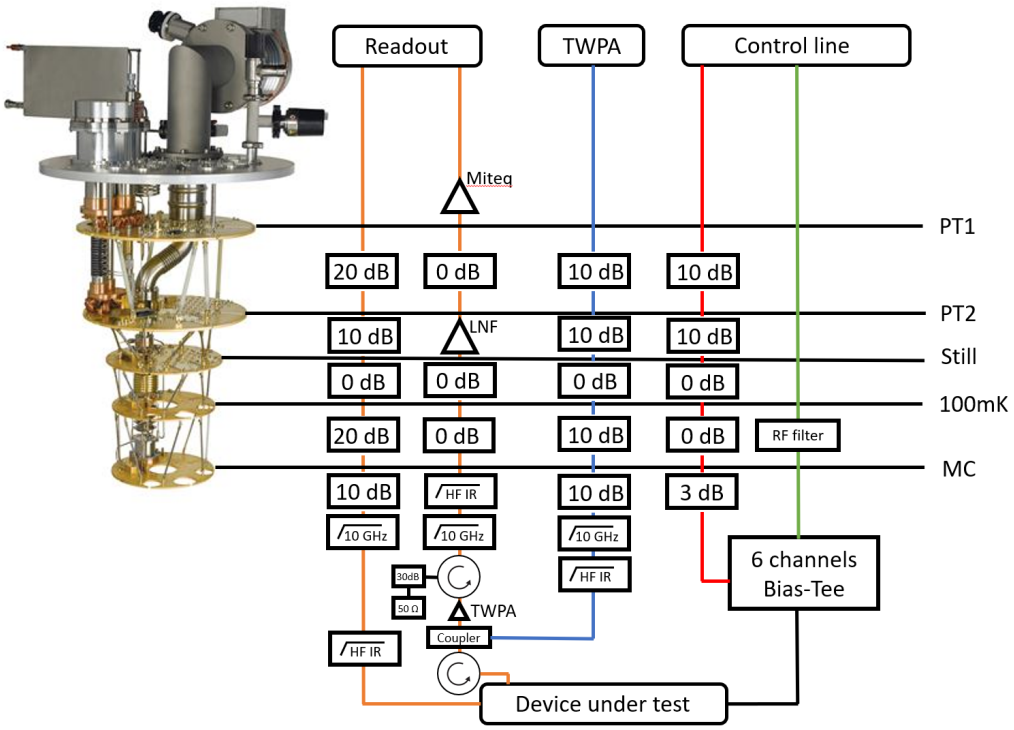
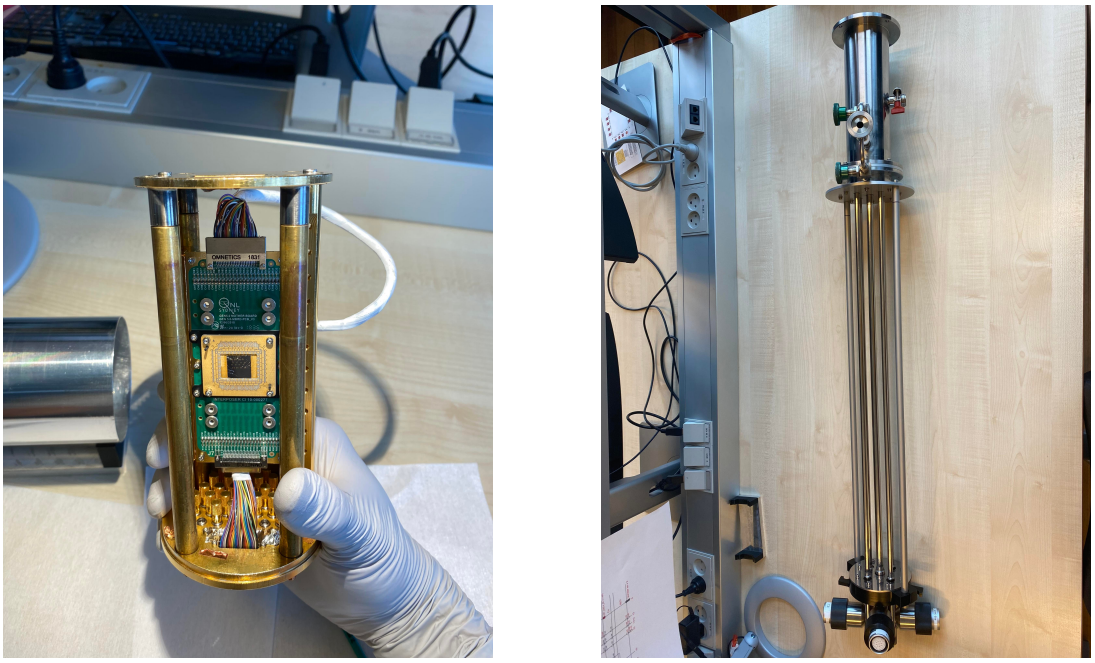


Figure 3.10: Wiring of T2 dilution fridge in QDev. The orange line is the readout line (the left goes into the device, and the right goes out). The red line is the high-frequency drive line for qubit control, and the green one is the DC line for gating.

parametric amplifier (TWPA)[47], high-electron-mobility transistor (HEMT) from Low Noise Factory (LNF) LNC4_8C616Z and room temperature amplifier Miteq. All the readout lines are mounted with a high-frequency infrared filter to absorb the unwanted 20 GHz to hundreds of THz light, excluding the extract heat source along the coaxial cable.



(a) ***(b)***

Figure 3.11: (a) The puck with Copenhagen board v8p0 on and a nano-D wire connected. (b) The loading rod is hanging on the arm.

We need to assemble the motherboard with the puck through 4 rods to load in the sample. Grounding yourself is required during the assembly process. Then we use a loading rod to push them together into the fridge. Grounding the rod during loading is also essential to protect TWPA and nanowires.

3.8 DC transport measurement setup

Figure 3.12: The picture contains two SR865 Lock-in amplifiers (bottom two), one YOKOGAWA as voltage source (upper left), one SR830 as a differential voltage amplifier, and one digital multimeter (DMM, the upper right one). All the low frequency (f <100 Hz) and DC signals are linked to the breakout box through low noise BNC cable. The Keithley 2600 (not shown) is used to apply gate voltage.

With four bonds directly on the capacitor pads, we can do four-terminal measurements on the nanowires. There are two types of cryogenic environments to do the transportation measurement, the board station with a base temperature of 5 K and a dilution fridge, but the measurement circuit is the same. We here use the double lock-ins technique, a high accuracy ac signal to do the measurement. Lock-in amplifiers use phase-sensitive detection [48] to single out the specific frequency we set and reject the other noisy signals in different frequencies. The output AC signal can describe as the mixture of reference and measurement signal of lock-in:

$$\begin{aligned} V_{psd} &= V_{sig}V_L \sin(\omega_{sig}t+\theta_{sig})\sin(\omega_L t+\theta_{ref}) \\ &= \frac{1}{2}V_{sig}V_L \cos([\omega_{sig}-\omega_L]t+\theta_{sig}-\theta_{ref}) \\ &\quad -\frac{1}{2}V_{sig}V_L \cos([\omega_{sig}+\omega_L]t+\theta_{sig}+\theta_{ref}) \end{aligned} \tag{3.8}$$

where V_{sig} is the output voltage from the measurement circuit, V_L is the lock-in amplifier's internal reference signal voltage. While $\omega_{sig} = \omega_L$, we will see that the difference frequency term is what we need as a very nice DC signal. The frequency is usually set as a prime number far from 50 or 100 Hz, such as 17.177Hz. There are two measurement types, current bias (I bias) and voltage bias (Vbias). The current bias is used when the junction is in the metallic regime to measure the critical current of the qubit system (including bulk aluminum or tantalum). We usually set the AC current to 1nA (corresponding to 1V output from Lock-in on 1GΩ resistor) and apply bias current up to 30nA. As the gate voltage tunes down, the normal resistance of

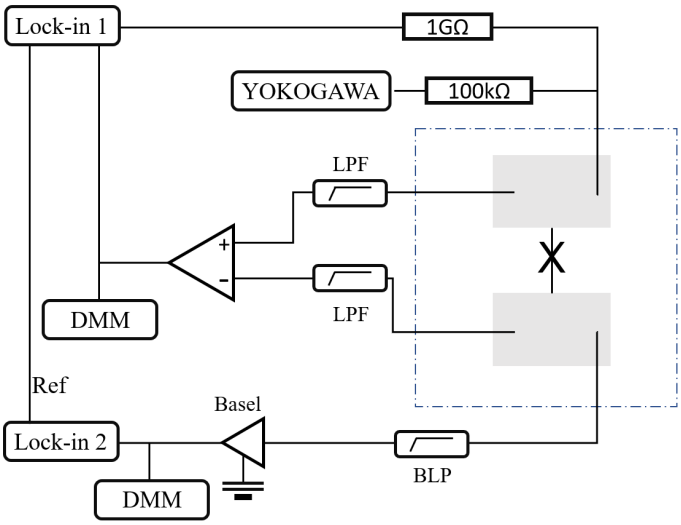


Figure 3.13: The two lock-ins' current bias measurement circuit. We use Lock-in amplifiers, SR830 or SR865 from Stanford Research System, as AC signal detectors. YOKOGAWA GS200 serves as a DC voltage bias source, then converts to current bias through the resistor. DMM is a digital multi meter as the monitor for gross voltage signal. Basel is the current-voltage converter, which turns the current signal to voltage and amplifies it. BLP and LPF are both low-pass filters.

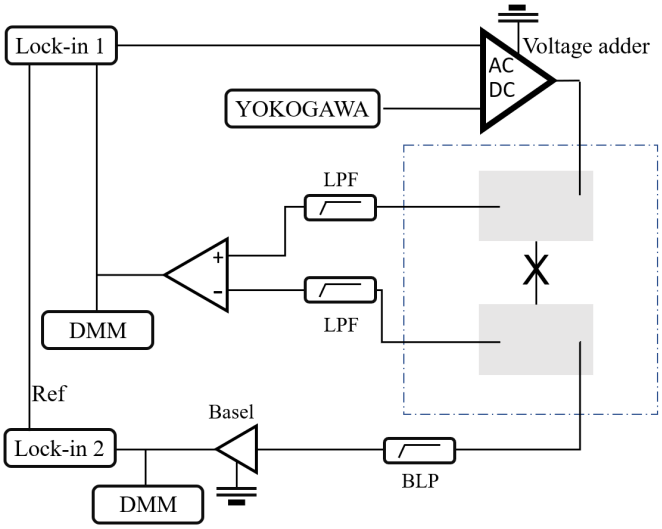


Figure 3.14: The voltage bias measurement is the similar configuration as the current bias measurement, but replace the resistors with a voltage adder.

the nanowire goes up and approaches over $10^7\Omega$ magnitude. We define this regime as the tunneling regime. The I bias measurement is risky now because the voltage output voltage from YOKOGAWA and lock-in is mostly applied on nanowires and thus potentially blows them up. Vbias measurement in this regime is used to precisely control the voltage applied to the nanowires. We use a voltage adder, which combines the AC and DC voltage and outputs an attenuated voltage. Meanwhile, we can observe different properties like the superconducting gap of the system, MAR. The output AC bias voltage on the nanowire is now around 10 μeV (which is 100 mV output from the Lock-in). The voltage bias measurement is only used in the dilution fridge since the nanowire and the bulk aluminum, tantalum, are both not becoming superconducting in the board station (the base temperature at around 5 K).

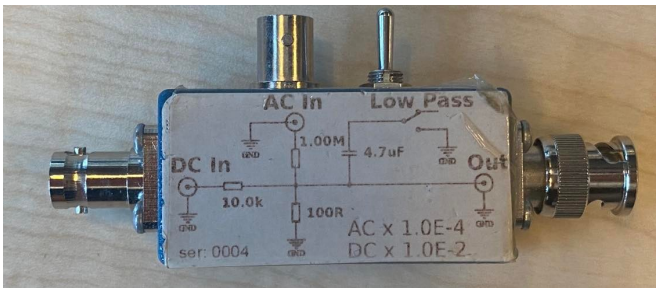


Figure 3.15: The voltage adder we are using for voltage bias measurement.

3.9 High frequency spectroscopy measurement setup

The high-frequency measurement comes after we understand the transportation property, such as the nanowires' critical current and superconducting gap. The measurement is done in the dilution fridge. We use two types of setups, one is the vector network analyzer (VNA) in frequency domain measurement to find the resonance peak for readout and qubit manipulation frequency, and the ALAZAR digitizer in both frequency and time domain measurement.

Resonator spectroscopy

VNA is a powerful tool to sweep a wide range of frequencies and return a **S**-parameter matrix. Experimentally, we mainly focus on S21 since it tells us the transmission signal through the device under test (DUT). When a mutually or capacitively coupled resonator is in resonance with the input signal, we will clearly see a dip in the S21 signal. Usually, we will sweep the frequency in high power, for example, 0 dB output on VNA and -80dB on line attenuation, to spot the bare cavity resonance frequency. We then do a power sweep on the TWPA to find the best pump power with a high signal-noise ratio (SNR). After that, we do a power sweep on the resonator and find the lowest power with a visible resonator shape. More details are at **Chapter 6**

4 DC measurement of nanowires with shadowed junction

This chapter will mainly focus on the DC measurement of in-situ growth MBE tantalum nanowires. Besides, it includes some DC measurements from Aluminum nanowires (Qdev 878).

4.1 Gate leakage through Silicon substrate

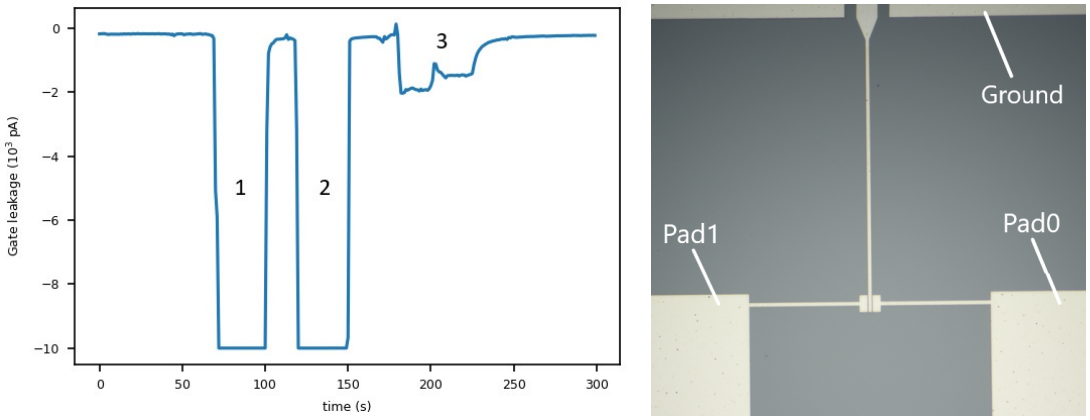
To reduce the fabrication steps after putting the nanowires on the chip, we first use the half-etched bottom gate to tune the Fermi level inside the junction. The advantages of this technique are: 1. Maintain a cleaner surface on the nanowires. 2. Better quality of material on the gate. However, we find that we can't pinch off the nanowires before exponential leakage happens($I_{leak} > 1nA$) in the experiment. We suspect SEM on the Silicon substrate will dope it and change the conductivity.

We fabricate a chip with four identical designs to determine whether the current flows through the substrate. Two of the devices undergo SEM heavily, and two are not. Then we load the chip into the 4K board station for a gate leakage test. In this experiment, only the gate is connected to a voltage source.

First, we apply a gate voltage to all the devices with contact pads open. None show exponential leakage before 20V, the largest voltage output from Keithley 2600.

After that, we connect one of the pads to the ground and find all of them start to leak when the voltage goes down to around -6V.

We realize the device has a breakable voltage channel for leakage to the contact pads through the Silicon. Nevertheless, we find in the experiment that the floating design also has leakage below -10V despite both contact pads being disconnected from the ground. There must exist another channel for the current directly flowing to the ground. So we apply -10V to the gate and subsequently ground both contact pads and the grounding surrounding. The leakage current will flow directly to the ground at high gate voltage. One solution to this



(a) *(b)*

Figure 4.1: The gate leakage measurement on the chip. The dip 1 and 2 indicate the grounding of contact pads 0 and 1, and 3 indicate the grounding ground.

issue is adding an ALD layer (HfO_2) on top of the bottom gate to reduce the distance between the source of the electric field and the Josephson junction. In this case, the junctions can be pinched off more frequently. The limitation is that the superconductor coated on the nanowire will directly touch the ALD layer, which might introduce extra noise channels, such as a two-level system on the ALD surface, to the qubit. Also, the nanowires are not guaranteed to be pinched off before leakage.

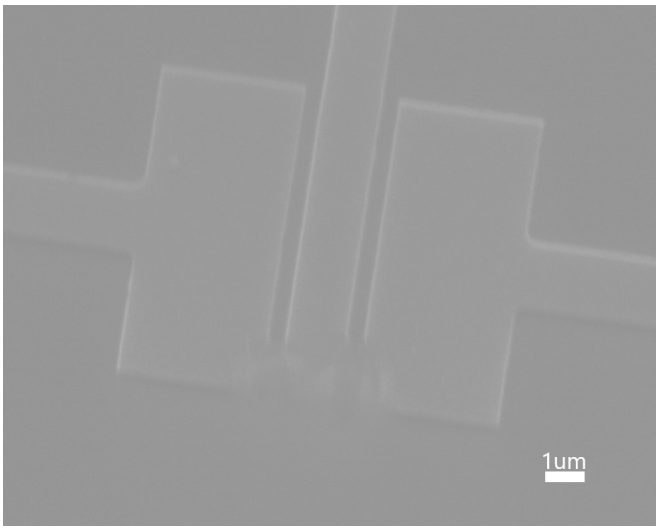


Figure 4.2: The 'explosion' happens after a huge leakage through the substrate. The SEM image tells us that the electric field is concentrated at the end of the gate line.

Changing Silicon to a Sapphire substrate is another solution to solve this problem by slightly adjusting the design of the qubit to have impedance matching. Sapphire has a lower dielectric constant, which can endure higher gate voltage before leakage.

Experimentally we find that Sapphire indeed increases the leakage tolerance. Thus we can pinch off the nanowires more frequently. However, the leakage will occasionally happen at around -5V, possibly because of the short distance between the gate and the nanowire when there is an ALD layer. This is easily solved if we use the half-etched gate on an Aluminum-based chip but is hard to solve with a Tantalum-based chip due to the aggressive wet-etch recipe. Nonetheless, the dry-etch technique can possibly solve this issue and endows higher resolution, more uniform edges to the control line. We will consider doing dry-etch in the future.

4.2 Four-terminal measurement on Tantalum nanowires

The VLS shadowed Aluminum nanowires have been investigated thoroughly on DC measurement[41]. Therefore our main focus in this thesis is to measure the transport properties of the new growth InAs-Ta shadow nanowires QDev 1226. The nanowires' junctions are shadowed by the nanowires with diverse shapes in front of them. Therefore the junctions behave differently due to the distribution of tantalum on semiconductors.

DC measurement on straight Tantalum nanowire

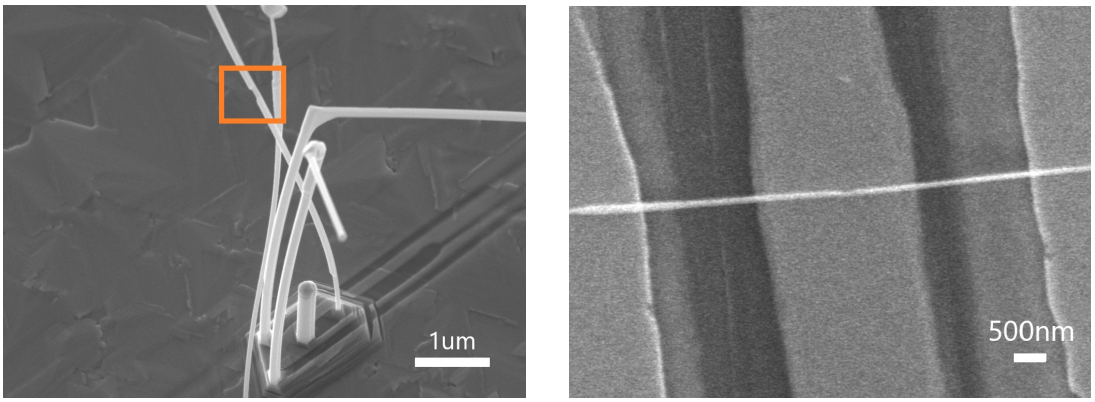
In current bias measurement, we seek the critical current I_C of the Josephson junction. It is a crucial parameter in calculating the Josephson energy, then the approximate operating frequency of qubit. The applied gate voltage should tune the critical current. Combining Eq 2.22 and with the equation:

$$f_{01} \approx (\sqrt{8E_C E_J})/h \tag{4.1}$$

, we can know that to modulate the qubit frequency in 4-6 GHz, we need to tune down the gate so that the I_C can reach down to 20-45 nA.

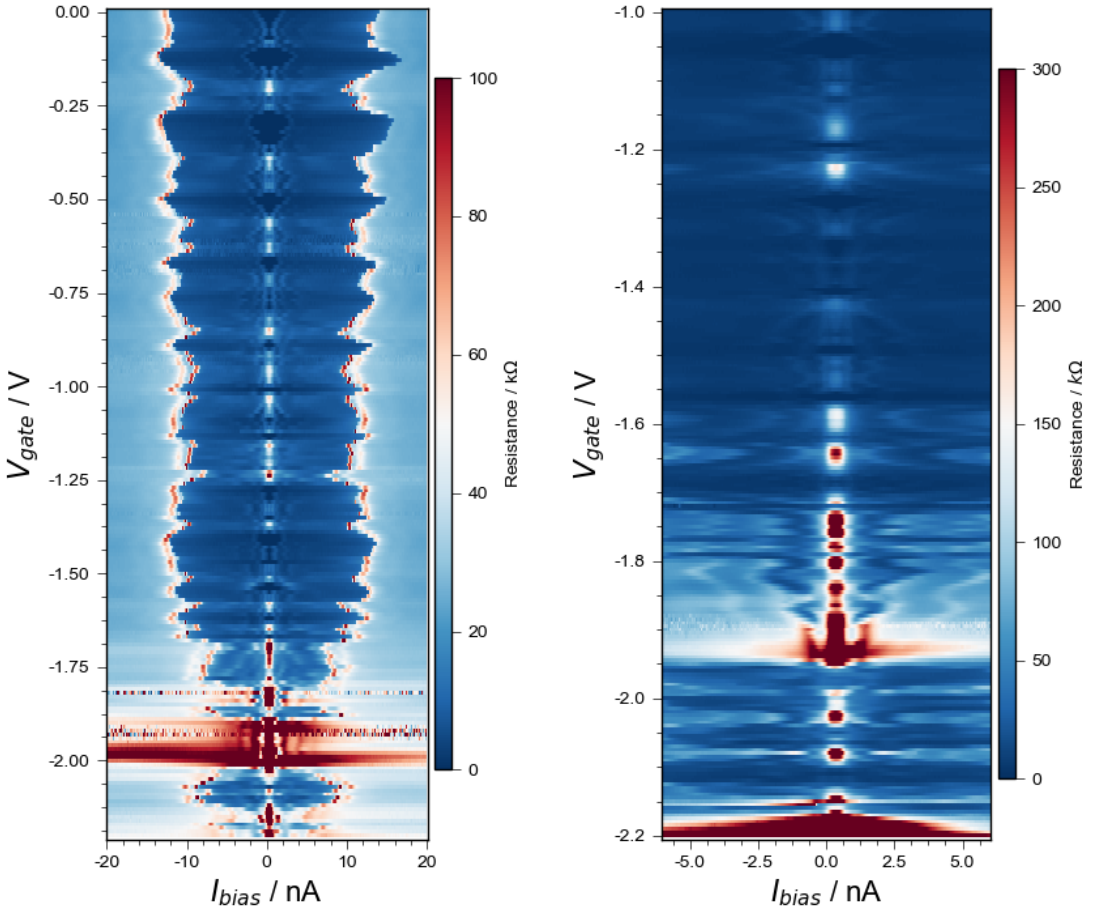
This nanowire has a Josephson junction of 150 - 200 nm in length. We do a quick SEM check before contact deposition to ensure the junction is on top of the gate, but we can't precisely measure the length of the junction since we only get a low-resolution image.

From the figure, we can clearly see the critical current is tuned by applying a gate voltage, and its value varies around 20-45 nA. There are complicated conductance fluctuations inside the critical current regime, indicating that Andreev reflections are perturbed by some states



(a) *(b)*

Figure 4.3: The SEM pictures (a) before transferring onto the chip. The junction is highlighted in the box. (b) After transferring but before the contacts deposition and measurement. The resolution is very low because we want to reduce the SEM time, thus the charge poisoning on the junction.



(a) *(b)*

Figure 4.4: Current bias measurement of Tantalum nanowire in dilution fridge, with differential resistance dV/dI. The DC bias current sweeps from left to right. (a) The overall current bias measurement until the nanowires are saturated. (b) Zoom in scan inside the supercurrent regime.

that occur inside the Josephson junction. The junction becomes highly resistive when $V_{gate} < -2.3V$, indicating it can enter a tunneling regime with only a few conducting channels inside the junction that provide electrons and holes.

In order to further understand the transportation property of the junction, we use voltage

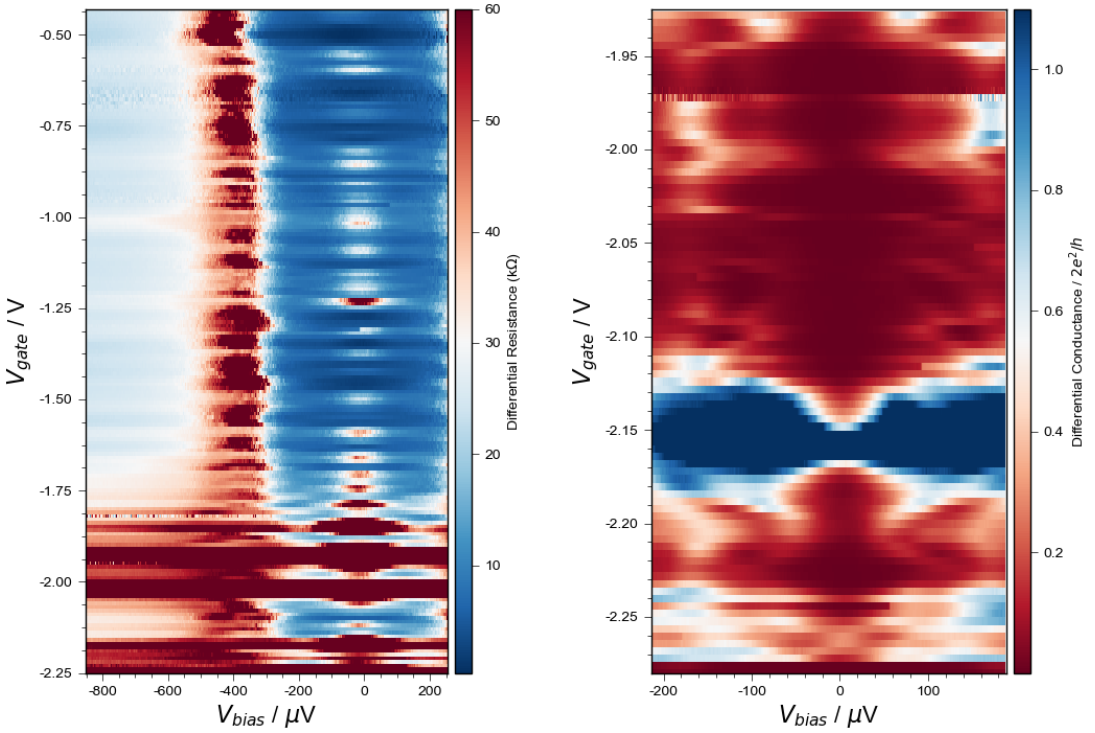


Figure 4.5: The voltage bias measurement plotted in differential resistance and conductance respectively on the straight nanowire. (a) The overall voltage bias scan until normal resistance shows up on the device. We can see a lot of recurring resistance fluctuation and dot-like events inside the superconducting gap. The measurement is asymmetric due to the large offset while doing the voltage bias measurement. (b) The zoom-in voltage bias scan inside the superconducting gap at high gate voltage near pinch off. No supercurrent occurs, and the dot-like oscillation fills the subgap.

bias measurement to find out the situation inside the superconducting gap after the resistance of the junction is higher than several thousand Ohms. Otherwise, we measure in an equivalent current bias (explain later). The voltage bias data shows the approximate induced superconducting gap Δ^* of this nanowire is around 150 μeV (estimate at $V_{gate} = 2.10V$). The measurement data still looks noisy even if the junction is close to pinch-off.

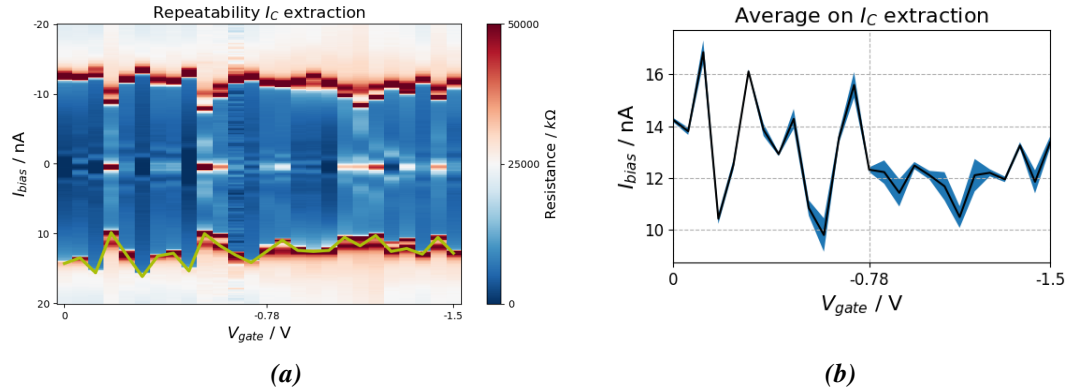


Figure 4.6: (a) One of the ten repeat current bias measurement data. The critical current is extracted from the plot, with the bias current sweeping from negative to positive. (b) The critical current average plot for ten repetitions.

Two other important factors for making a good transmon qubit are the repeatability and stability of a nanowire. The former indicates the accuracy of recurrence of the critical current,

hence qubit frequency, in certain gate voltage. The more accurate we can repeat the critical current, the easier we can improve our qubit gate manipulation in the future. The lateral one tells us the variation of the qubit frequency at fixed gate voltage in the unit of time. In the implementation of any time domain measurement, including gate operation and time domain measurement in a qubit, we want the qubit frequency to be stable forever.

The repeatability of the nanowire is relatively high, with almost the same change in amplitude regarding the gate voltage ten times. Moreover, the stability measurement in 3 hours demonstrates a robust Josephson junction against charge jump for a reasonably long time.

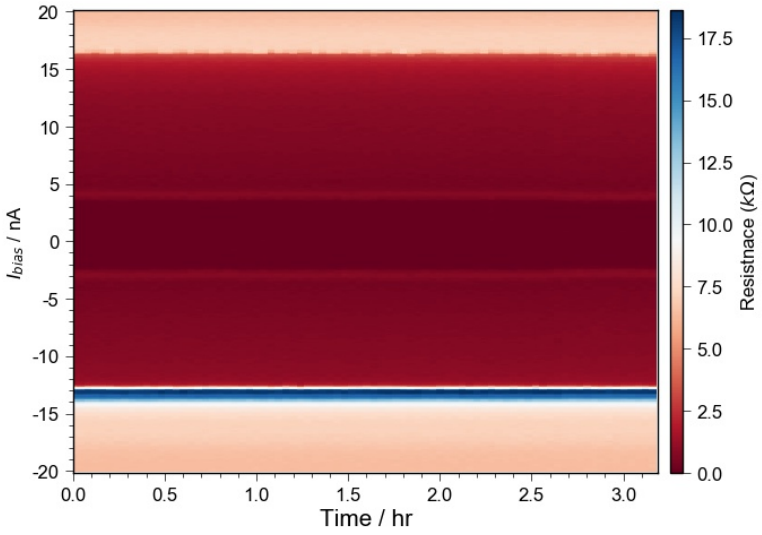


Figure 4.7: Stability measurement on the tantalum nanowires. The current sweep is from negative to positive.

This nanowire is promising since both stability and repeatability show good robustness on the shadow Josephson junction. Nevertheless, the quantum dot-like behavior makes the wires unsuitable for gate-tunable Josephson junction in the qubit island on gatemon. It provides additional states that will break the coherence of particles inside the junction. The emergence

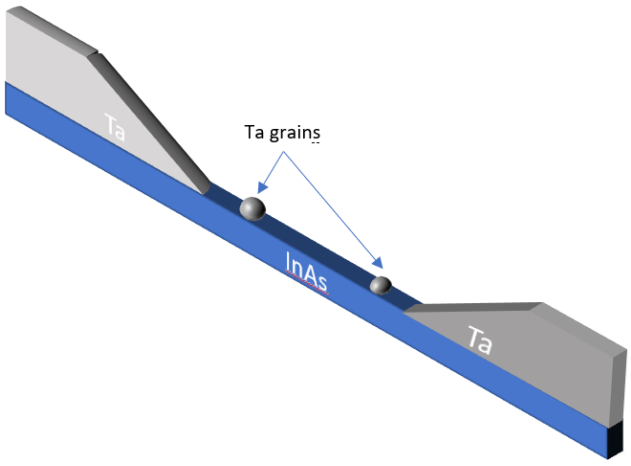


Figure 4.8: The formation of grain on the junction can potentially provide extra states inside the superconducting gap.

of this behavior has many potential hypotheses. One possible reason for this phenomenon's formation is the unintentional tantalum grain growth on the junction. While depositing the metal on the nanowire, the atoms will diffuse into the junction and start to form grains on it. Intuitively we can imagine that the grains break the coherence of electrons and holes that participated in Andreev reflections and also reduce the mean free path of them. From an energy

level perspective, these grains will provide extra energy levels inside the superconducting gap, interrupt Andreev reflections and thus introduce resistance when there is a small amount of conducting channels inside the junction.

Further proof of whether the Tantalum nanowires have actual sub-gap states that prevent clean Andreev Reflections, hence supercurrent, from appearing, we need to find more wires to measure.

DC measurement on straight nanowire 2

According to the SEM image, the second nanowire has a 200 nm Josephson junction (Fig 4.9).

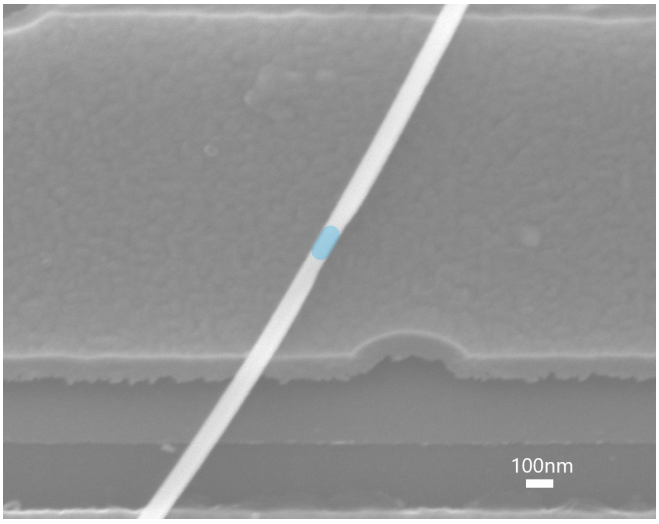


Figure 4.9: The nanowire overview in the SEM after transferring. The blue strip indicates the location of the junction, but not the length of it, since the tantalum-InAs interface has a large slope.

After cooling down to the base temperature (25 mK) in the dilution fridge, we first try to sweep the gate without bias current.

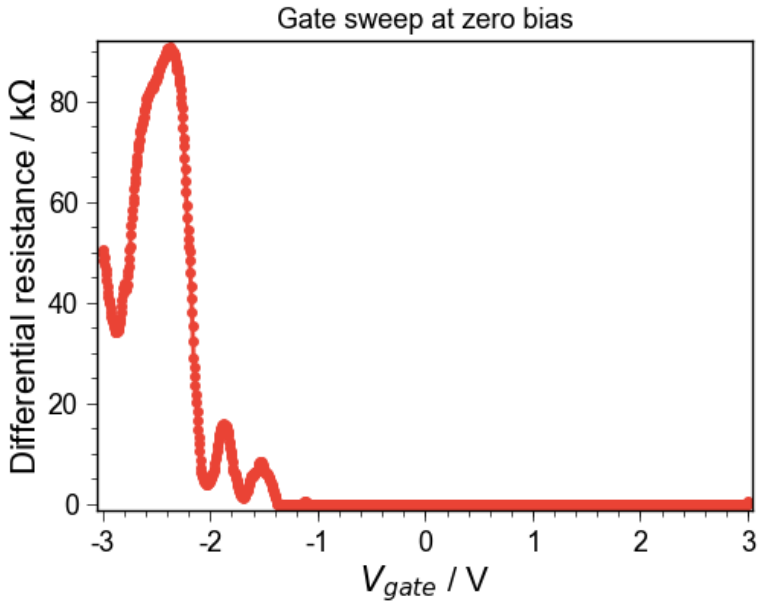


Figure 4.10: The gate sweep on the nanowire at zero DC bias current, with AC current 5 nA.

It is clear that the supercurrent exists and no dot-like behaviors before -1.4 V. The resistance increases when the gate voltage is more significant, and it shows some oscillations as

the voltage changes.

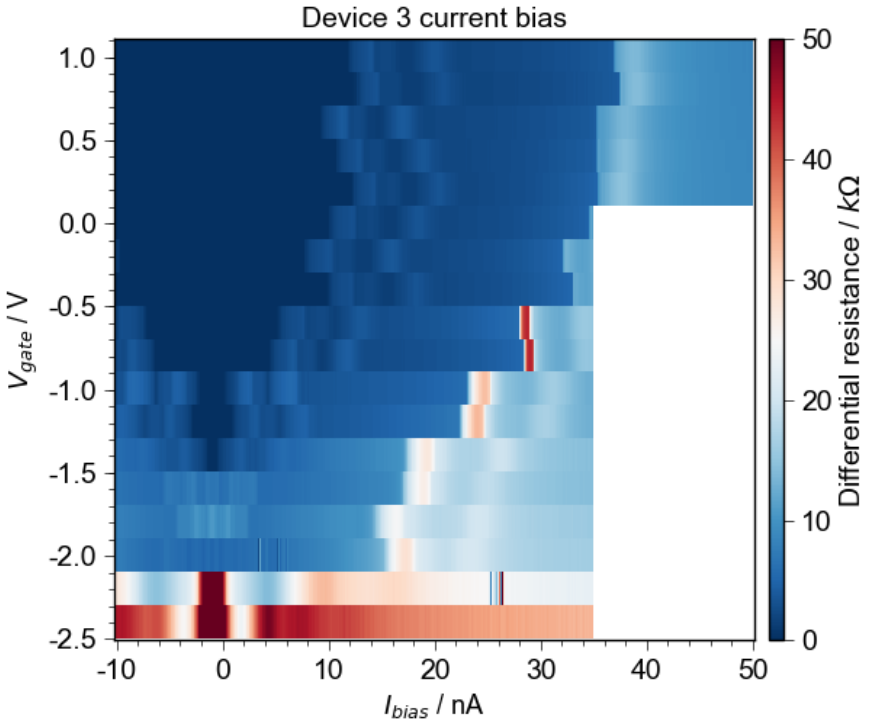
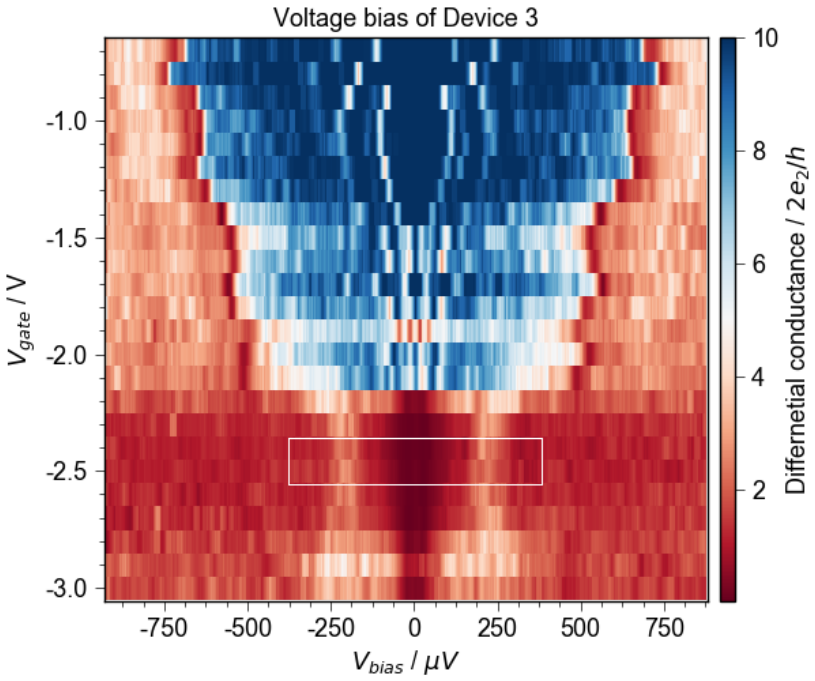


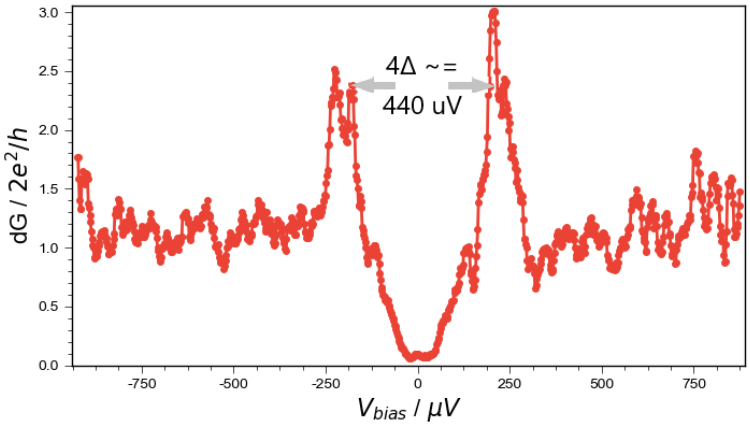
Figure 4.11: The current bias measurement in the unit of kOhm. The junction is partly superconducting inside the critical current regime, except for the finite resistance at the 'sleeve'.

The current bias sweeps from -10 nA to 50 nA. We can observe some resistance at a relatively large bias current before reaching the critical current, which is tuned along with the critical current. An explanation for this is the existence of different transmission rates in conductance channels. The Andreev reflections contain multiple channels, and their combination forms the supercurrent. Hence, if there are three types of Andreev reflections with different transmission rates and critical currents, the current bias map might show three boundaries (As shown in Figure 4.11), and all are gate tunable. The blank part is due to the reduction of the sweeping range to 35 nA.

In voltage bias measurement, we can tune the junction into a tunneling regime, which almost eliminates Andreev reflections and leaves many specular reflections at the interface. We now get a highly resistive junction, and the voltage output from the DC source is mostly dropped on the junction. Therefore, we can estimate the induced superconducting gap from the measured $4\Delta^*$ of the junction. In Fig 4.12, the line cut at $V_g = -2.4V$ shows that the induced superconducting gap $\Delta^* \approx 110\mu eV$, which is lower than the superconducting gap of bulk tantalum (crystalline) $\alpha-$phase tantalum $\Delta_\alpha \approx 1.4meV$ and amorphous $\beta-$phase tantalum $\Delta_\alpha \approx 300\mu eV$.



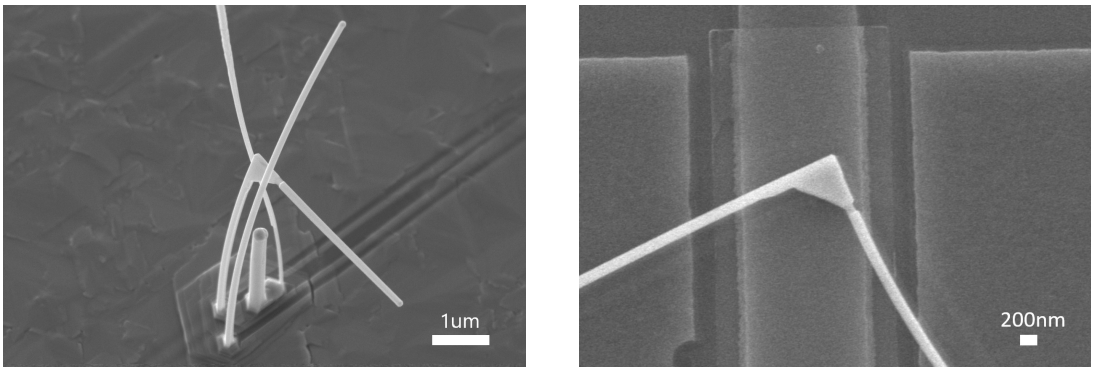
(a)



(b)

Figure 4.12: (a) The voltage bias measurement on the nanowire. The wire can enter the tunneling regime, but the signal is pretty noisy. (b) The line cut is at gate voltage -2.4 V. The measured superconducting gap is about 110 μV, comparable to Damon's tantalum wire[42].

DC measurement on kinky shadow nanowire



(a) *(b)*

Figure 4.13: The kinky wire and its SEM picture on the ALD gate. Notice that the junction is around 100-150 nm.

The Kinky wire with shadow junction is found with luck, and its tantalum coat looks homogeneous. The S-N interfaces are spotless and clear, which may give us cleaner data than previous nanowires. Therefore it is worth to try measuring it and knowing how it behaves.

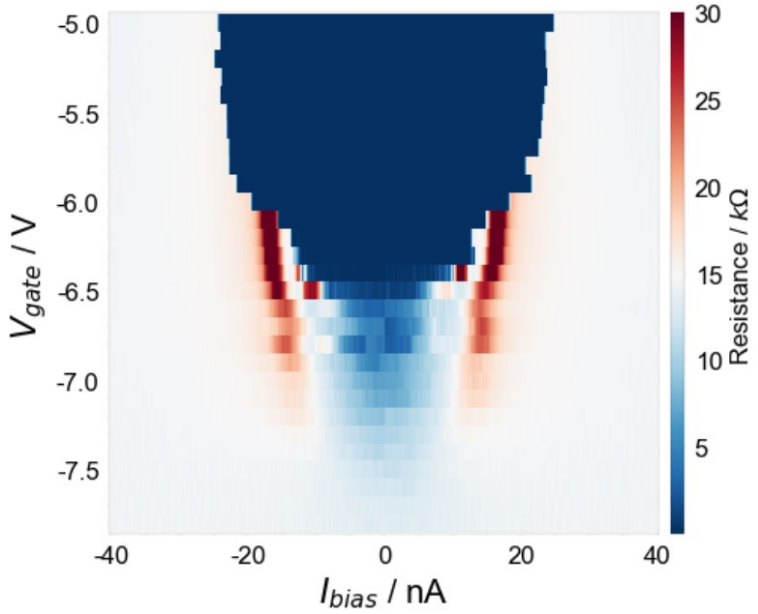


Figure 4.14: Current bias measurement of kinky wire. The sweeping is from 0 to both sides to get a critical current. The superconducting regime starts to be vague after -6.5V due to the gate leakage.

In current bias measurement, the superconducting regime of the nanowire is clean and genuinely superconducting (for the random measured phase on voltage drop to prove further that this is true supercurrent). Meanwhile, the critical current is easily turned down to 20 nA without gate leakage. This is already the optimal operating regime for gatemon. The lack of features inside the critical current area also is a good sign for having a flawless junction. However, the gate starts to leak when the gate voltage is at -6.5 V, which injects more than 1 nA current through the junction. This causes vagueness in the data and eventually vanishing of the supercurrent. The problem prevents the nanowire from entering the tunneling regime, and thus we can't measure the induced superconducting gap of this nanowire.

Since we can't tune the nanowire into the tunneling regime, and the resistance of the nanowire at zero bias is still low, the voltage bias measurement is now equivalent current bias measurement. This is because the line resistance of the fridge along the DC loom is around

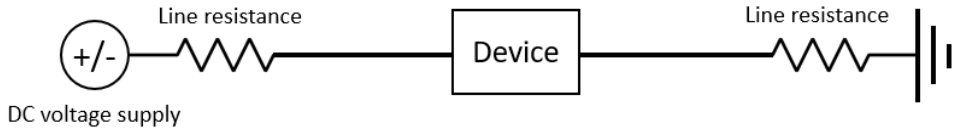
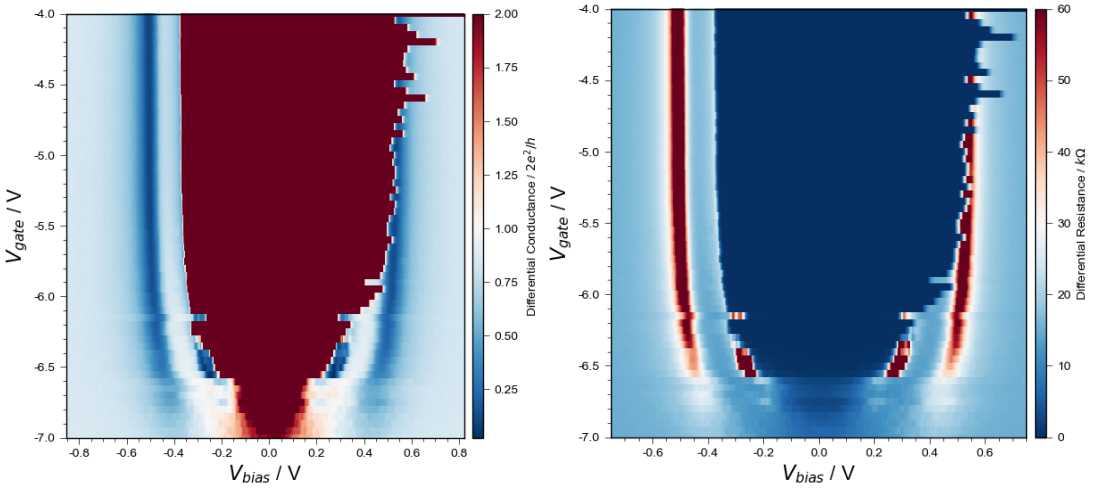


Figure 4.15: The illustration of the line resistance in the fridge. While in voltage bias measurement, we need to tune the device to high resistance. Otherwise, it is an equivalent current bias measurement.

3000 Ω. Unless we can tune the resistance of the nanowire at zero DC bias to higher, the significant voltage drop will still be on the coaxial line, and no valid superconducting gap is shown.

There is yet no MARs sign in the measurements in both current and voltage, probably because we are not close to the tunneling regime of the nanowire.



(a) ***(b)***

Figure 4.16: The voltage bias measurement plotted in (a) differential conductance and (b) differential resistance. Since the resistance is still low at zero bias, the voltage bias measurement is not valid because the voltage will drop on the coaxial line

5 High frequency measurement on Tantalum Resonator

In this section, the Tantalum resonator is made and measured. We fabricate 12 Tantalum resonators with a common feedline on the sapphire substrate. Then we load it into the dilution refrigerator, extract the forward transmission signal and fit the data with the resonator model. The measurement is all done in QDev's Triton 2 dilution fridge.

5.1 Calibration on readout input line's attenuation before loading

The high-frequency measurement is sensitive to the wiring in the fridge and shielding. To accurately calculate the photon number loaded into the resonator, we have to know the exact attenuation on the readout input line. The calibration is done by shorting the drive line and an unattenuated line, then measuring the transmission rate S21 on VNA. The drive line has in total of 60 dB attenuators and approximately 20 dB attenuation on others when calibrating at 7GHz at the base temperature in the dilution fridge.

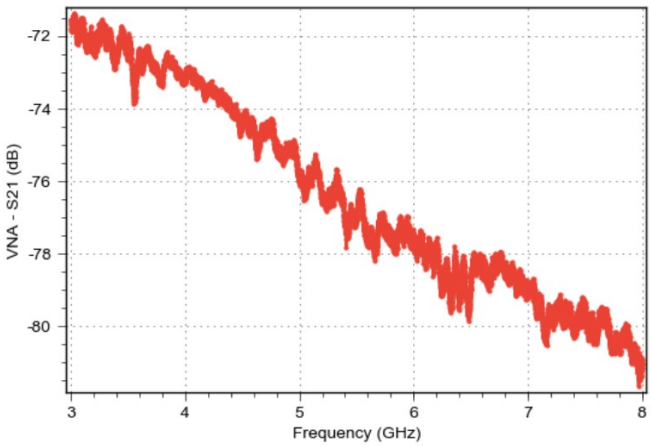


Figure 5.1: The transmission on the T2 fridge was measured on VNA. The resonators are lying between 6-7 GHz, so the total attenuation on line is around 80 dB.

5.2 Fitting function for extracting Q factor

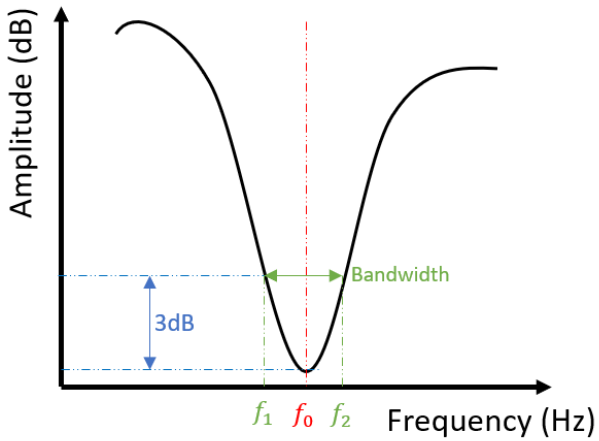


Figure 5.2: The diagram shows the components we need to estimate the loaded quality factor.

Quantum fitter, the package we make for data fitting, is perfect for routine usage on fitting high-frequency measurement data and plotting them. The resonator fitting formula, consider-

ing non-ideal elements such as impedance mismatch, can be described as[49,50]:

$$S_{21} = A\left(1+\alpha\frac{f-f_r}{f_r}\right)\left(1-\frac{\frac{Q_L}{|Q_e|}e^{i\theta}}{1+2iQ_L\frac{f-f_r}{f_r}}\right)e^{i(\phi_v f+\phi_0)} \tag{5.1}$$

Here the quality factor Q_L is the important parameter with relation $1/Q_L = 1/Q_i + 1/Q_c$, where $1/Q_i$ is the internal quality factor that tells us the intrinsic decay rate of the resonator, and Q_e indicates the coupling between resonator and the feedline with $Q_e = |Q_e|e^{i\theta}$ (asymmetry in the resonator line shape) and $1/Q_c = \mathrm{Re}(1/Q_e)$. The higher Q_i is in low readout power, the better resonator we get. To obtain a trustworthy internal quality factor, we need to modulate the external quality factor to the same order. Therefore we have 12 resonators with different coupling strengths to the feedline.

The loaded quality factor is simply estimated by measuring the 3 dB cut-off frequency at the resonance peak (Fig.5.2). The definition of loaded quality factor in power is $Q_L = f_r/\Delta f$, where f_r is the resonance frequency, and Δf is the full width at half maximum (FWHM) frequency. The definition of dB is:

$$L = 10\log_{10}\frac{P}{P_0}(dB) \tag{5.2}$$

Consequently, 3 dB is equivalent to a half drop of power $P/P_0 = 0.5$, which is the FWHM we need. With the formula:

$$Q_L = f_0/(f_2 - f_1) \tag{5.3}$$

we can calculate the rough quality factor of the system and use it to check if the fitting is valid.

5.3 Measurement on bare resonators

After fabrication of the Tantalum resonators on the chip, we immediately bond and load the resonator into T2. The first task is to find the 12 resonance dips on the overall resonator scan.

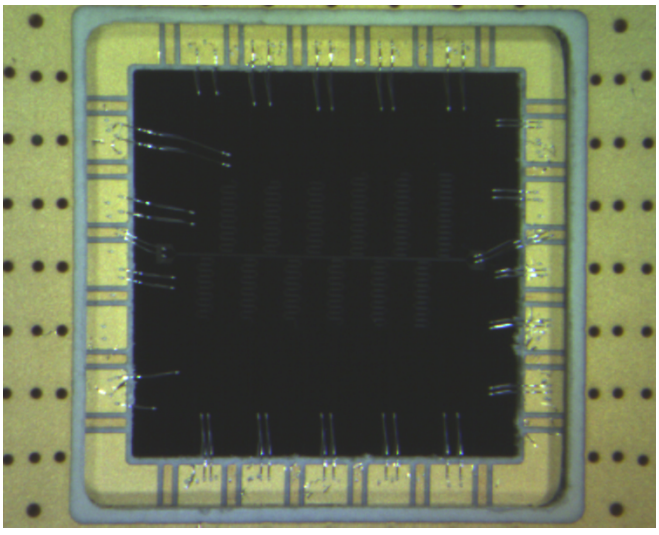


Figure 5.3: The chip with bare resonators after bonding on the QCage board.

The VNA is set to have no average with large bandwidth and scan over the 4 GHz range to find the resonance peak on the S_{21} spectrum. After that, we do a finer scan on each resonator in high power to locate precisely the center frequency of all the resonators. Then we set a scan on the center frequency, with a small frequency span and low bandwidth, to measure the S21 on each resonator and fit it with the resonator model.

The resonator has a decent internal Q while in high power but decreases dramatically while we approach the single photon regime. The figure shows the highest Q internal factor

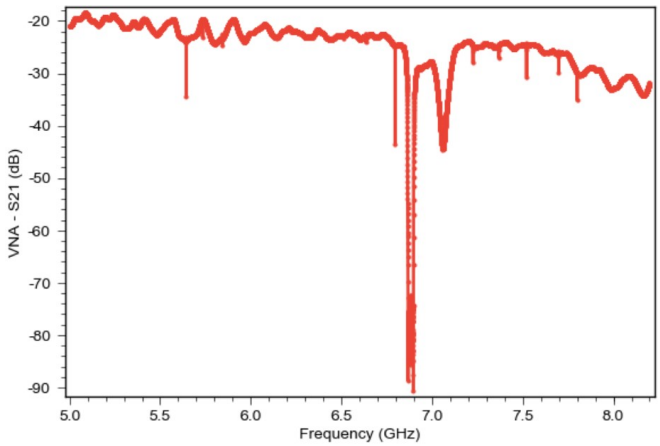


Figure 5.4: Overall scan of the resonator. The resonance peak at around 6.9 GHz is the TWPA's eigenfrequency. Our design of the resonator has avoided the frequency around this peak.

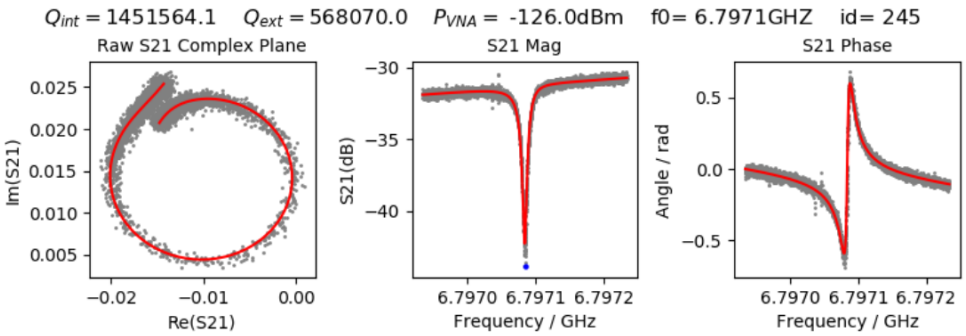


Figure 5.5: The fitting data with -46 dBm output from VNA. The total readout power to the resonators is -126 dBm.

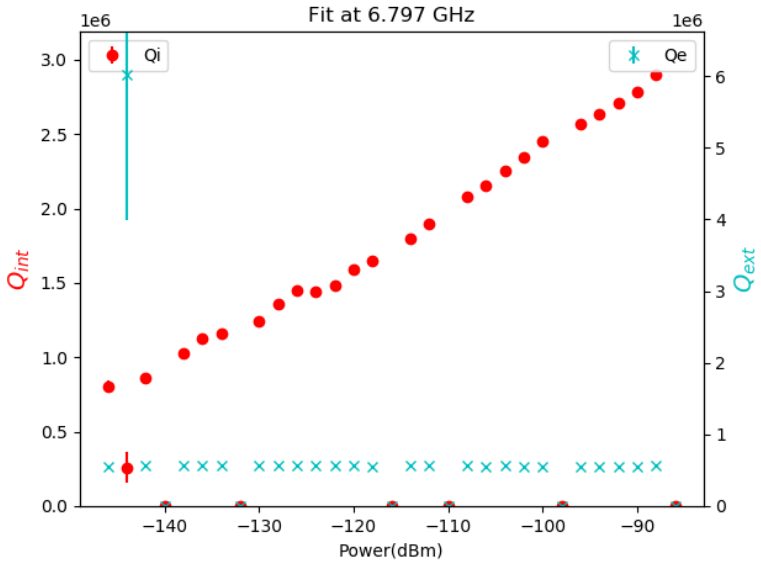


Figure 5.6: The fit down to -146 dBm. Now the VNA is attached with a 36dBm attenuator to reach a lower drive power.

resonator on-chip, and the signal becomes too weak to measure below -146 dBm, roughly equal to 5 photons inside the resonator.

To get a higher Q internal factor, we unload the chip and do surgery on the chip and wiring.

5.4 Measurement on post-cleaned resonators

The high-frequency measurements, including resonator and qubit spectroscopy, are sensitive to environmental noise like Johnson–Nyquist noise, and TLS embedded in the material[26]. Therefore, several strategies to reduce the noise on the chip are deployed. The chip is cleaned with Piranha solution for 20 minutes to reduce the quantity of reactivity metal like zinc and chemical compound residue from the fabrication process on the surface.[45]. We then bonded the chip with on-chip bonds on both the feedline and the resonator. This technique helps to balance the voltage difference between two ground planes. Beyond these, we add the 50Ω terminator at the end of the SMP connector coaxial line to stop signal reflection to the chip and prevent noise from getting into the ground plane.

(a) ***(b)***

Figure 5.7: (a) The on-chip bonding. Every resonator is cross-bonded with 2 to 3 bonding wires, and the feedline is cross-bonded with five bonding wires. (b) The 50Ω terminators at the end of the SMP connector.

With this cleaning combination, the resonators gain a higher SNR and can measure down to a single photon regime. At -146 dBm, the Q_i is nearly 1 million but around 800 thousand without the combination.

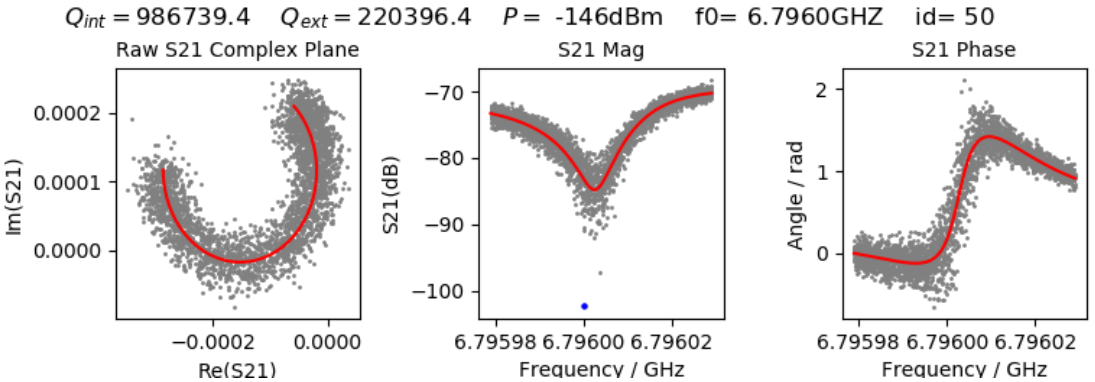


Figure 5.8: The resonator fit in the post-clean resonator, which is better than the internal quality factor we showed on Fig 5.6. At this power, the photon number inside the resonator is around 2.

Now the best resonator on the chip is around 7.8 GHz and still has over a million Q factors in the single photon regime (in this case, at -150 dBm).

The loaded quality factor is related to the relaxation time of qubit in the form $Q_L = 2\pi f_{01} T_1$. With this tantalum resonator, A qubit, with $f_{01} = 3.5GHz$, has relaxation time T_1 limited by the resonator in single photon regime over 50 μs.

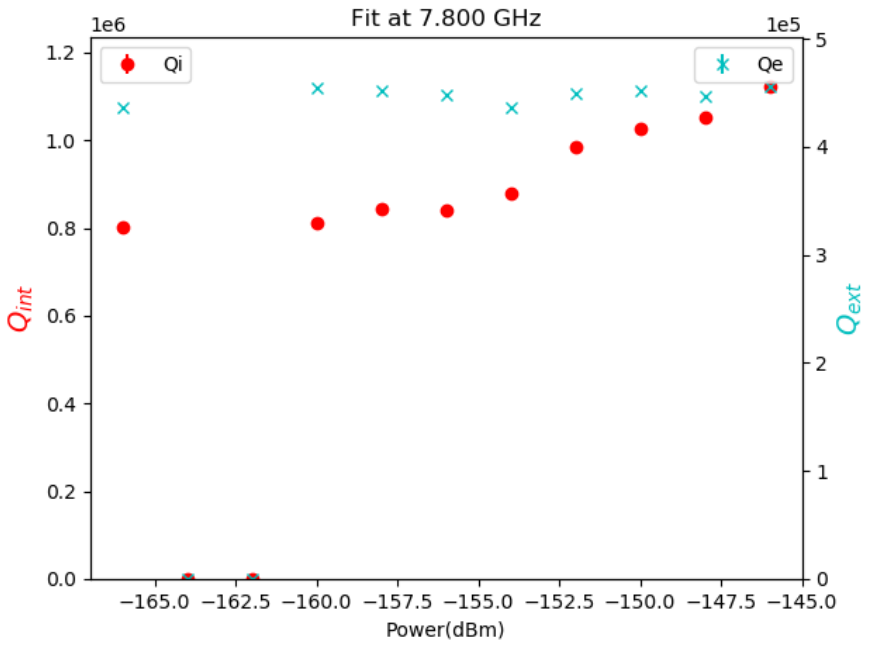


Figure 5.9: The fitting of the best resonator we find on chip. At -150 dBm, the resonator reaches the single photon regime and still has over a million internal quality factor.

6 Conclusion

In this thesis, we investigate the transport properties of the first batch of tantalum nanowires with shadowed junctions worldwide. The nanowires' critical current is gatable and can be adjusted down to 15-20 nA, which endows the future working tantalum gatemon qubits with $\approx$ 5 GHz frequency, an optimal number for high-frequency measurement setup and device. The measured induced superconducting gap of the wires is around 110 μeV, which is lower than the aluminum shadowed $InAs_{0.3}Sb_{0.7}$ nanowires. Also, we develop a wet etch recipe on tantalum with up to $1\mu m$ resolution. With the recipe, we successfully fabricate a twelve resonators' chip and get over two million Q internal factors in several thousand photons regime. With proper cleaning, terminators, and on-chip bonding, we can get over a million Q internal factors in the single photon regime. Additionally, we successfully fabricate a tantalum based substrate with tantalum shadowed nanowires chip and show supercurrent when measuring in the dilution fridge. Therefore, we have already accomplished the preparation works for fabricating a gatemon qubit chip.

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Appendices

APPENDIX A

Shadow nanowires supplement data

1 Milling test on the tantalum nanowires and tantalum

The usual way to form contacts on nanowires is using RF milling on the nanowires and then depositing metal on gold and the terminals of nanowires, and this works for both tantalum and aluminum shadow nanowires. However, since our contacts are aluminum or tantalum along with oxidation layer, we are recommended to use Kaufman milling on the nanowires. We, from previous DC experiment data, know that the aluminum shadow nanowire can withstand 1 minute Kaufman milling and form a good connection to the contact pad. We still need to test whether the tantalum nanowire survived after 1 minute Kaufman milling. The SEM shows

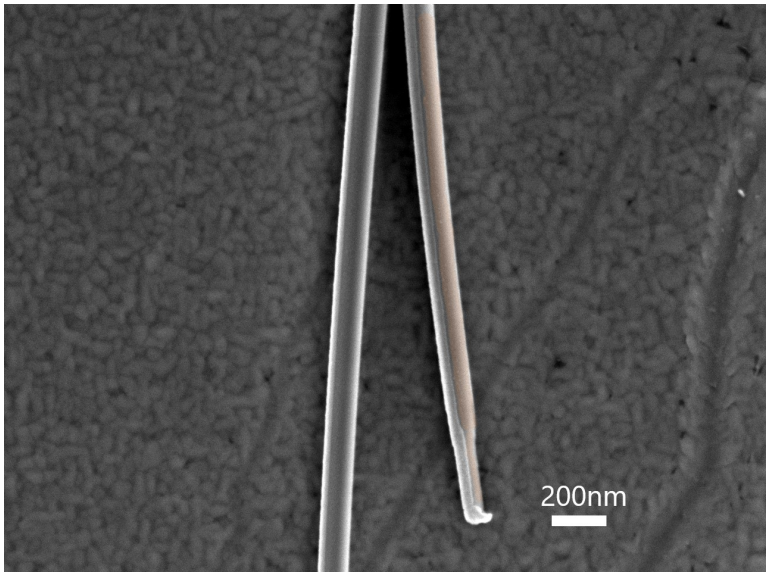
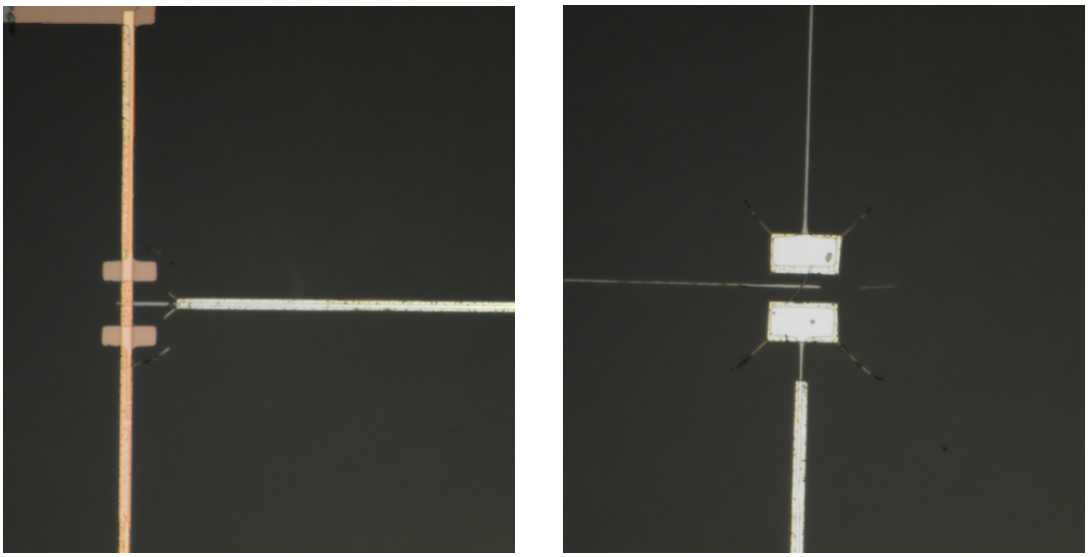


Figure A.1: The nanowires after milling. The orange part is the tantalum.

that the tantalum nanowires remains visually intact after Kaufman milling.

The next step is to test whether this milling recipe works for bulk tantalum. We fabricate a chip with deposition metal between the contacts and measure the differential resistance by four terminal measurement of this 'fake' wire in board station (higher than the T_C of α-phase tantalum. The chip has in total 3 'fake' aluminum wires. All of them shows tens of Ohm resistance, which means the milling works well on tantalum.

The real nanowires with (1 of 3) and without (2 of 3) junctions, however, all have a resistance to around 10 $k\Omega$. This is higher than what we are expected because the nanowires without junction is merely acting as a piece of metal. Nevertheless, the measurement data in dilution fridge shows the supercurrent across the junction, which means the line resistance can be eliminated when the metal is under critical temperature. So this high resistance issue remains unsolved and we might test it once again to find out the issue.

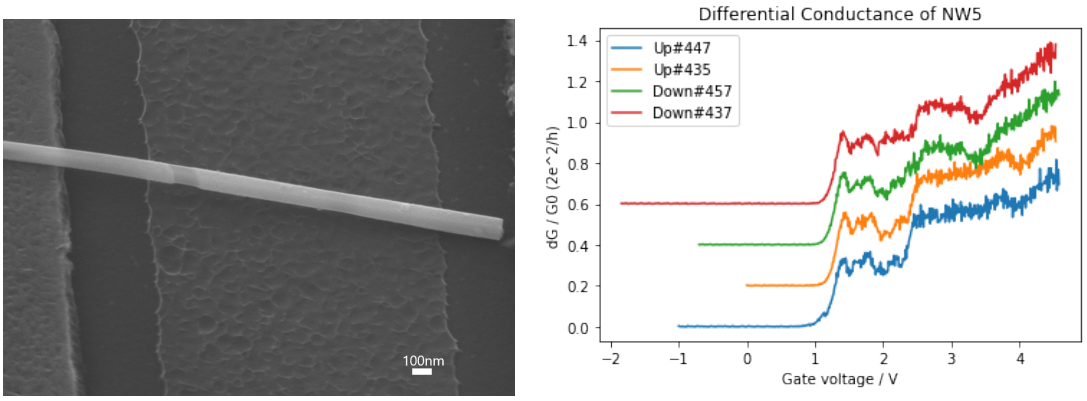


(a) *(b)*

Figure A.2: (a) The 'fake' aluminum nanowire (in orange color) deposited by AJA with bulk Tantalum underneath it. The right metal strip is the gate line, which remains floating when measuring the resistance. (b) The nanowire is linked to the bulk tantalum with aluminum contacts. The crack like aluminum strips around the contacts are because of the exposure problem. We don't use the discharge layer on top for this chip, thus the resist breaks and leaves the strips.

2 Gate tunability test on tantalum nanowires

Another important thing to demonstrate is to find out where the junction is gate tunable. This tantalum nanowire is loaded into board station and go through a current bias sweep. The



(a) *(b)*

Figure A.1: (a) The nanowire and the half-etched bottom gate on the chip. (b) The measured differential resistance with respect to the gate. The line is offset by 0.2 conductance quantum for each.

nanowire is pinch off when no gate voltage is applied, but gradually open after applying positive gate voltage. We conclude in this experiment that the InAs/Ta nanowire is gate tunable and we can use it for DC measurement in dilution fridge.

3 Tantalum nanowires supplement data and images

The measurement are all done through four-terminal connection in dilution fridge **Device 1** (Kinky wire shown in the main text): This device is from DC Chip 2 NW7

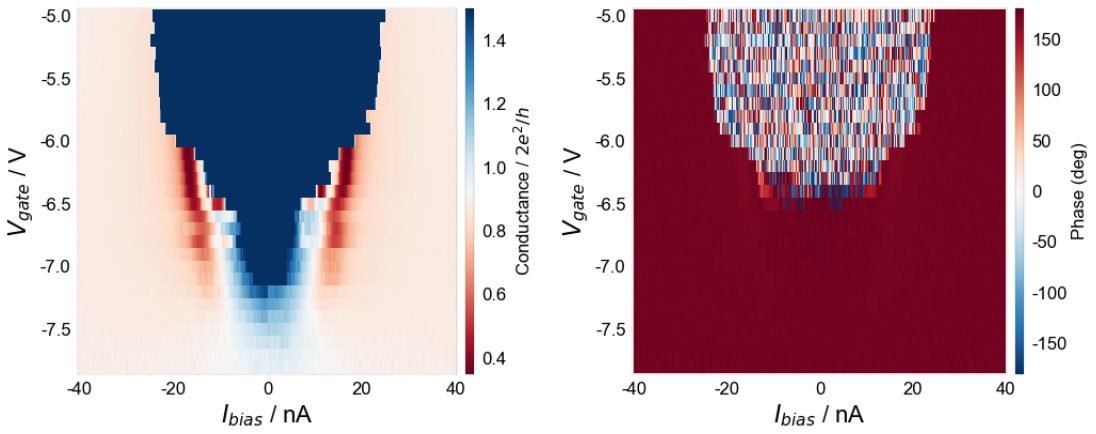


Figure A.1: (a) The measured conductance of the kinky wire. (b) The measured phase while biasing with current. This shows that the inner is truly superconducting.

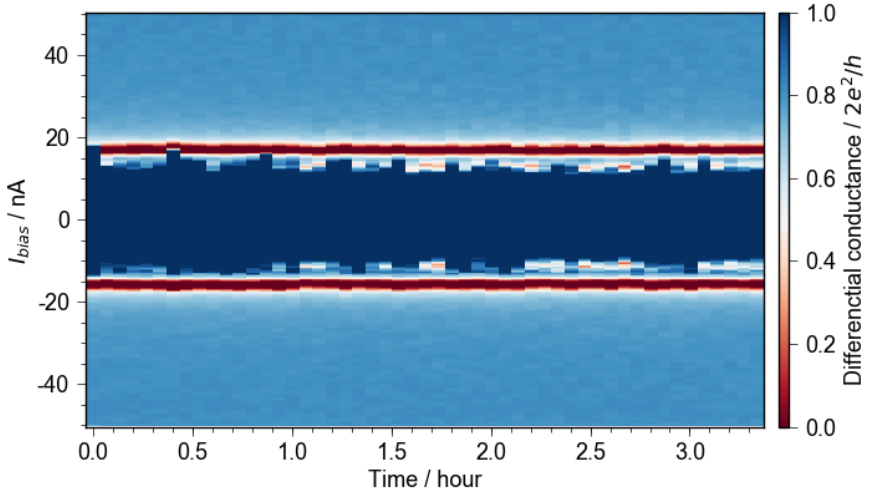


Figure A.2: The stability measurement on the kinky wire for over 3 hours

Device 2 (straight wire shown in the main text): This device is from DC Chip 6 NW2

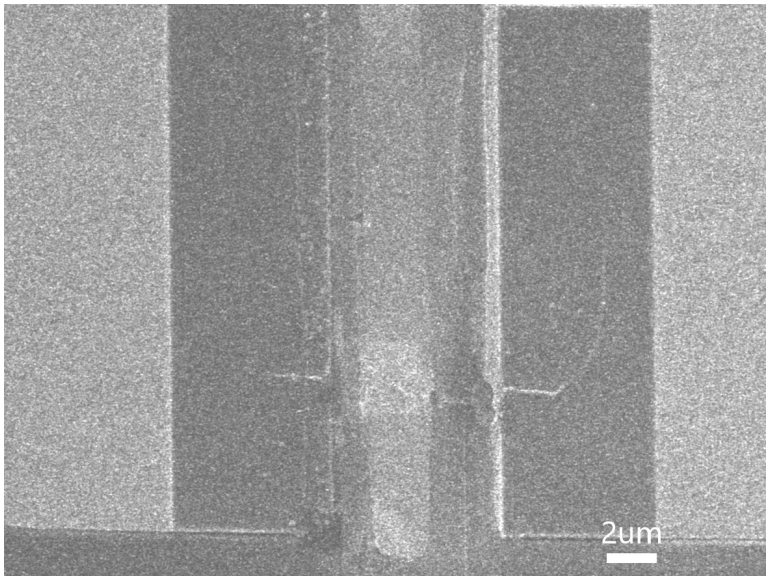


Figure A.3: The nanowire explodes after approximately 2 minutes scan in post-measurement SEM.

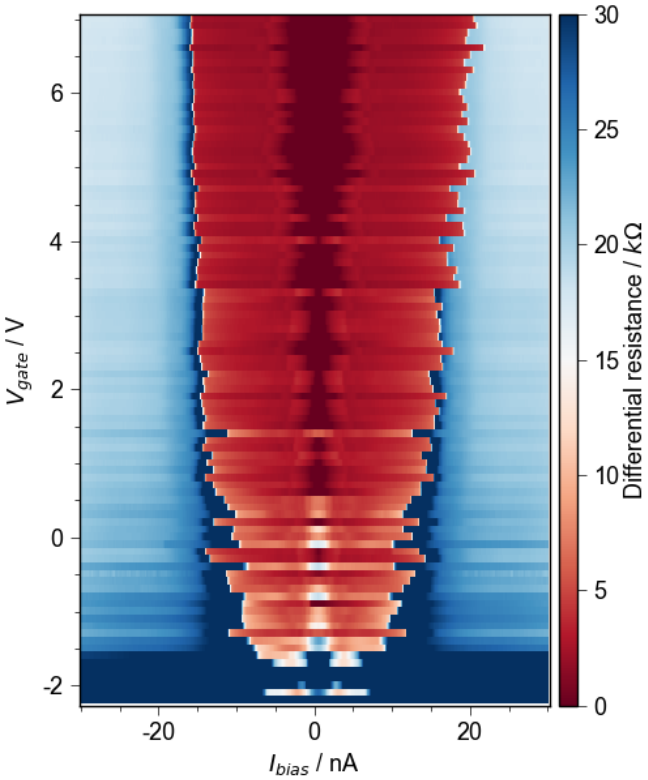


Figure A.4: The trial to fully open up the junction and get rid of the dot-like behaviour in the junction. The finite resistance still exist inside the critical current regime even the gate voltage goes to 7 V.

Device 3: This device is from DC Chip 2 NW4 (the straight wire 2 in the context)

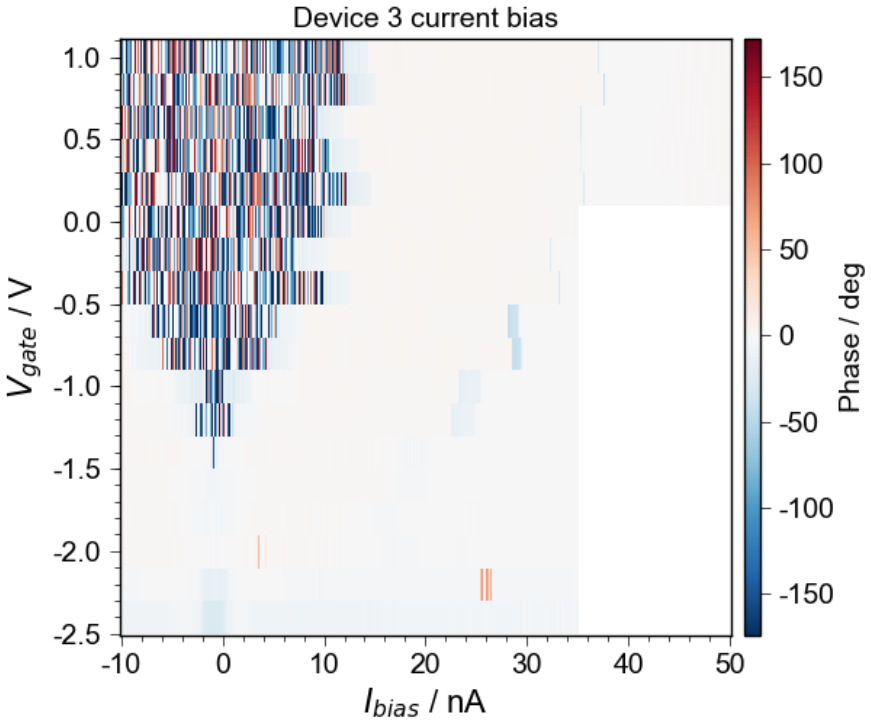


Figure A.5: Support diagram for Fig 4.11 to show that it is truly superconducting inside the critical current regime

Device 4: This device is from DC Chip 2 NW3

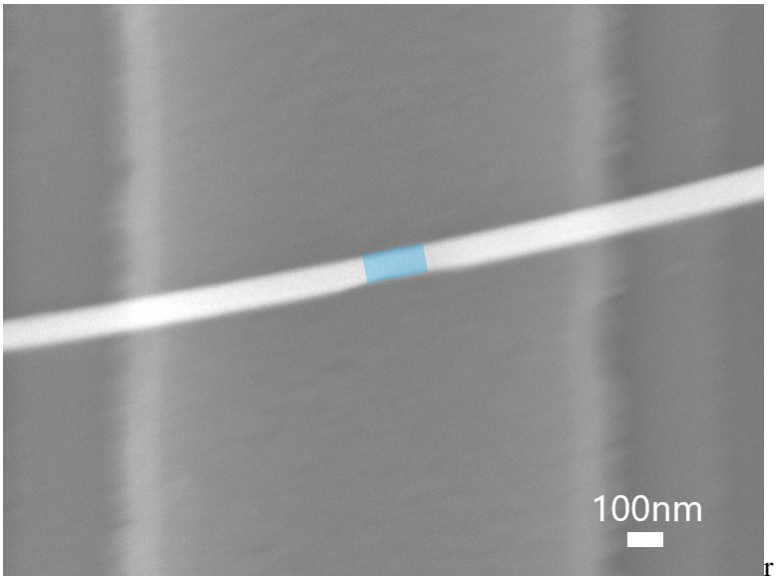


Figure A.6: The nanowire overview in the SEM after transferring

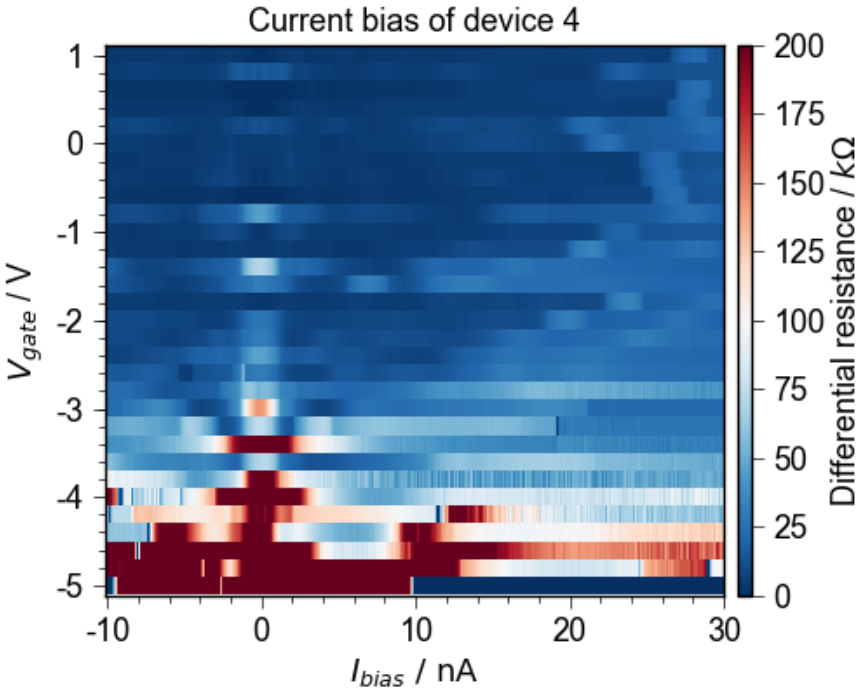


Figure A.7: Current bias measurement of device 4. The device's differential resistance inside the critical current regime seems very noisy and mostly has no supercurrent flowing through while applying small current bias.

APPENDIX B

Tantalum etch test on Electron beam lithography

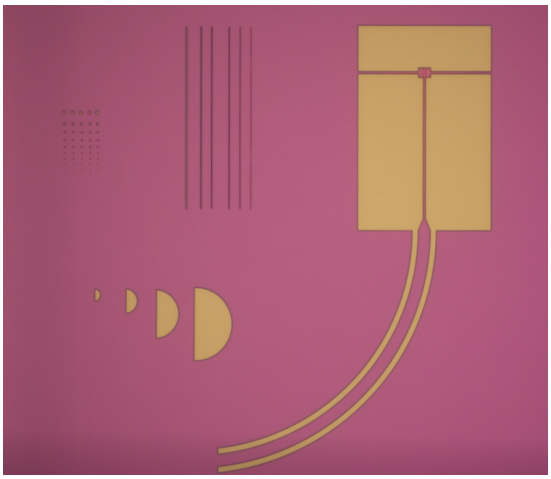
One major difficulty on the nano-scale Tantalum wet etch by EBL is the e-beam resist are on data sheet, less compatible to hydrofluoric acid and nitric acid. Success on etching in buffered HF (1:10) by using Csar 62 (https://www.allresist.com/resist-wiki-boe-etching-of-sio2-with-csar-62-mask/) and cold buffered HF (1:20) by PMMA A2 is reported and although the resist wiki on Allresist shows concentrated oxidation acid like nitric acid acts as a remover on E-beam resist already at room temperature (https://www.allresist.com/resist-wiki-how-high-is-the-etch-resistance-of-e-beam-resists-in-the-presence-of-strong-acids), we want to try if the resist can survive until the Tantalum is fully etched.

1 Trail on Csar 13

The first trial recipe we use is Csar 13:

1. Pre-clean the chip 10 minutes in 1,3-dioxolane, 3 minutes in acetone with sonication, and 1 min IPA. Dry it with nitrogen.
2. Spin Csar 13 on the chip with 4000 rpm / 45 seconds, then bake it with 150 degree for 1 minute.
3. Lithography on ELS-F125 ebeam system with $430\mu C/cm^2$. Develop in oxylene for 1 minute, MIBK:IPA (1:3) for 30 seconds, IPA for 30 seconds and dry.
4. Ash in Diener plasma asher for 1 minute, and bake it for 4 minutes, 150 degree.
5. Etch the chip in Transene 111 for 8 seconds with slow stirring (0.5Hz) and then dip it into the first MilliQ for 20 seconds, and the second MilliQ for 30 seconds.
6. Strip it with 50 degree acetone for 10 minutes and the IPA for 1 minute.

The resist looks intact and clear after the development, but falls off after etching.

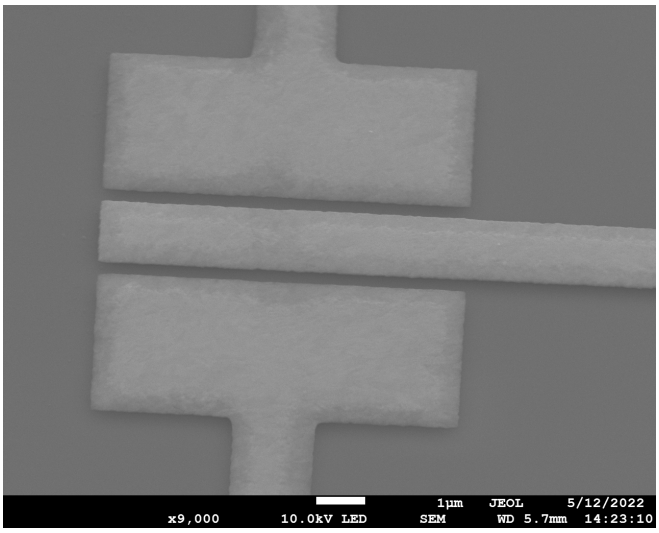


(a)

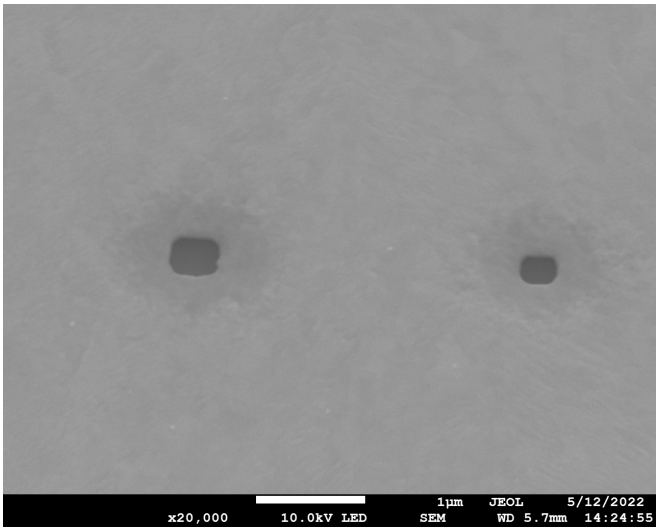
(b)

Figure B.1: (a) The resist remains intact after the development. (b) And it falls off during the etching process after merely 8 seconds inside the acid.

Optical microscope can't provide enough information on how the etch looks like. We then put the chip into SEM, which shows a bad etch on the Tantalum pattern.



(a)



(b)

Figure B.2: The etch

In the SEM photos, we can clearly see the Transene 111 is attacking the Tantalum pattern surface during the etch. These evidences show that Csar 13 is not a good candidate in Tantalum wet etch with Transene 111. However, The pattern on the chip appears with sharp edge and without distortion. Therefore, one possible solution is to use Csar 62 with low spin rate, which has more than 1 μm thickness, to do EBL.

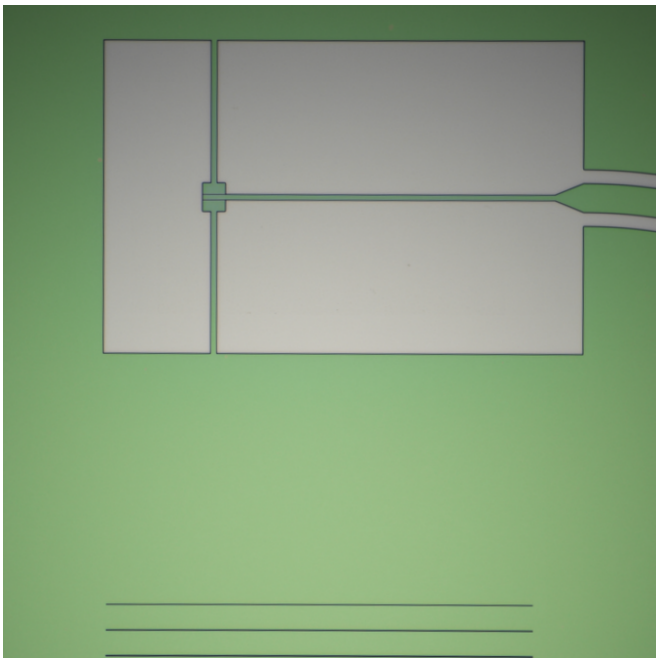
2 Trail on PMMA layers

PMMA series is another possible resist that we can try. We try several different combinations of PMMA recipes to thicken the resist layer:

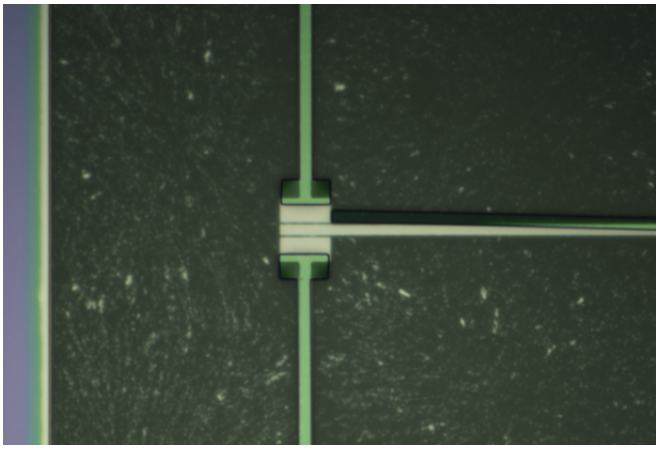
1. Pre-clean the chip 10 minutes in 1,3-dioxolane, 3 minutes in acetone with sonication, and 1 min IPA. Dry it with nitrogen.

2. Spin PMMA A6 on the chip with 4000 rpm / 45 seconds, then bake it with 185 degree for 1 minute.

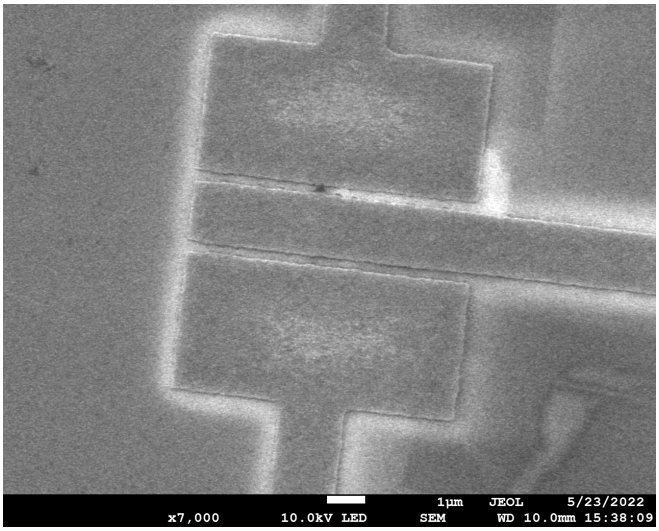
3. Spin PMMA A6 on the chip with 4000 rpm / 45 seconds, then bake it with 185 degree for 1 minute. (Optional)



(a)



(b)



(c)

Figure B.1: (a) After development on the PMMA. (b) The etch on the PMMA

4. Spin PMMA A2 on the chip with 4000 rpm / 45 seconds, then bake it with 185 degree for 1 minute.

5. Lithography on ELS-F125 ebeam system with $1000\mu C/cm^2$. Develop in MIBK:IPA (1:3) for 60 seconds, IPA for 30 seconds and dry.

6. Ash in Diener plasma asher for 1 minute, and post-bake it for 2 minutes, 115 degree.

7. Etch the chip in Transene 111 for 9 seconds with slow stirring (0.5Hz) and then dip it into the first MilliQ for 20 seconds, and the second MilliQ for 30 seconds.

8. Strip it with 50 degree acetone for 10 minutes and the IPA for 1 minute.

The total thickness of the resist is up to 800 nm if two layers of PMMA A6 and one layer of PMMA A2 is spun on. This recipe has a similar resist falling off and distortion issue to the Csar one. Moreover, the etching always leaves some leftover Tantalum on the sapphire, even if we extend the etching time. Beyond 15 seconds, the pattern will all disappear. SEM pictures show that the surface are attacked severely, which is not ideal for the qubit devices since it might generate extra TLS coupled to the transmon system.