UNIVERSITY OF COPENHAGEN

Master's thesis

Coulomb blockade and Little-Parks effect in hybrid double nanowire systems

Author:
Sara Lorić

Supervisors:
Jesper Nygård
Kasper Grove-Rasmussen

Center for Quantum Devices
Niels Bohr Institute

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Abstract

This thesis investigated double nanowire (DNW) heterostructres that combine two parallel InAs nanowires with the in-situ deposited Al layer that serves to couple the wires. Two types of geometries were in the focus of this study. The first was parallel quantum dot geometry with common superconducting and normal leads (N-pDQD-S), while the second was the full-shell geometry (Al layer all around the nanowires) studied in the context of the Little-Parks effect.

It was first demonstrated that gate tunable parallel quantum dots can be realized in this heterostructure. Optimization of the fabrication procedure lead to the device performance improvement and the induced superconducting gap was observed. Furthermore, there were signatures of Yu-Shiba-Rusinov bound states within the superconducting gap. Ground state studies for different quantum dot occupations revealed spin singlet to doublet transition, as the quantum dot goes from having even to odd occupation. Increase in the coupling of quantum dots to the superconducting lead resulted in the screening of a spin doublet ground state to a Yu-Shiba-Rusinov (YSR) type of singlet.

The investigation of full-shell double nanowires revealed phase diagrams characteristic of the Little-Parks effect. Theoretical model was used to extract the parameters such as coherence length, nanowire diameter, and superconducting shell thickness. With the exception of coherence length, the parameters were in the agreement with the expectations based on the independent measurements.

The above mentioned investigations in double nanowire heterostructures provide a first step towards exploring their full potential as a promising experimental platform.

Acknowledgements

I would like to start by extending my gratitude to Jesper Nygård for accepting me into his research group and making me feel like I belong. Thank you for granting me this extraordinary experience in the most stimulating environment. Special and biggest "TAK" goes to Kasper Grove-Rasmussen for his vigilant supervision, invaluable guidance and encouragement to face all challenges without fear. His patience with me was limitless and I was lucky to have him as a supervisor on this journey.

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I especially want to say "thank you" in all of the world's languages to my QDev friends Denise Puglia, Miķelis Marnauza, Dāgs Olšteins and Anna Wulff Christensen for all the times we laughed, discussed science and science-fiction, shared a meal, made dinners, or just had fun. Further, special thanks to my smithie, Emma Rocco, a brilliant scientific mind that constantly humbles me with her compliments. Few people that I can count on for emotional support and true advice, big thanks to them, my girls Mirta, Naida, Vladanka and Senija.

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Contents

1 INTRODUCTION (AND MOTIVATION)

1.1 INTRODUCTION AND MOTIVATION

Research community that uses single nanowire semiconductor-superconductor hybrids as experimental platform spans over a number of fields. Quantum devices are particularly interesting for the fundamental studies and currently also for the realization of qubits, as the research into quantum computing is steaming up. Hybrid devices that result from the combination of the semiconducting nanowires with a superconductor attracted a lot of attention in recent years. This kind of experimental platform proved to be a great playground to investigate various interesting phenomena, including subgap states as Majorana [1], [2] and Yu-Shiba-Rusinov states [3], [4].

The fast-paced technological advancements witnessed over the last decades reflected on the nanofabrication and material science. At first, quantum devices were studied in single nanowire hybrids, with ex-situ evaporated superconductor, which more often than not resulted in soft superconducting gap. Now, it is possible to have the nanowire hybrids with in-situ deposited superconductor resulting in high level epitaxial match between the semiconductor and superconductor [5].

The superconductor can be deposited on few selected nanowire facets, or on all of them, resulting in the so called full-shell superconductor-semiconductor nanowires. The experimental potential of such nanowires in the context of Majorana [6] and Little-Parks effect [7] related research has been demonstrated recently.

Now, what if we add another wire to this heterostructure? There is no need to wonder because such structure has already been successfully grown. Prior to this, scientific investigations that required two nanowires closely placed and parallel to one another, coupled to a superconductor required careful manipulation of separate wires and ex-situ deposition of superconductor [8], [9]. Now there is a parallel nanowire heterostructure that is ready for device fabrication. Theoretical proposals to investigate Topological Kondo effect [10], parafermions [11], Andreev molecule [12] require such double nanowire geometry, making these novel heterostructures quite promising.

The work presented in this thesis is concerned with understanding these double nanowire heterostructures from the quantum transport point of view, with the goal of establishing their potential utility as experimental platform. Half-shell nanowires were investigated in parallel double quantum dot (pDQD) geometry, with common normal and superconducting lead. Full-shell version of double nanowires was investigated through the Little-Parks type of the experiment. The results showed a great experimental potential of this exciting heterostructures.

1.2 THESIS OUTLINE

Chapter 2 introduces general theoretical background and concepts necessary to understand the work presented in this thesis. It begins with an introduction to semiconductor nanowires and hybrid structures that combine semiconducting nanowires. Chapter continues with a discussion of the quantum dot origins and physics, including double quantum dot geometry. Next, the phenomenon of superconductivity is briefly introduced, followed by an introduction to the bound states with a focus on Yu-Shiba-Rusinov bound states. Finally, the physics of Little-Parks effect is explained with a special consideration of the two possible regimes.

Chapter 3 starts with a brief overview of the nanowire-based heterostructure used for device fabrication and continues with a discussion of the fabrication techniques and processing steps. Description of certain fabrication challenges

is also included. The chapter concludes with the presentation of the two- and four-terminal measurement setups.

Chapters 4 and 5 present the main results from the transport measurements of parallel quantum dot systems in double nanowires. The first chapter analyses the results when both contacts are in the normal state. Building upon this, the following chapter examines the situation when one of two contacts is in superconducting state. These two chapters demonstrate

Chapter 6 is dedicated to the experimental investigation of the Little-Parks effect in the new full-shell double nanowire (DNW) systems. It includes a discussion on resulting phase diagrams for destructive and non-destructive regime. Qualitative observations are supplemented by theoretical modeling and fitting of the experimental data.

Chapter 7 provides the conclusion to the experimental findings and the outlook regarding the future work based on these particular double nanowire heterostructures.

2 THEORY

To comprehend the work presented in this thesis it is necessary to get familiar with the general physical concepts that underlay it. This chapter is written with this purpose in mind and it serves to provide.

2.1 SEMICONDUCTOR-SUPERCONDUCTOR NANOWIRES

Semiconductor nanowires provide an excellent platform for studying variety of low-dimensional quantum phenomena. Due to their large aspect ratio (width much smaller than length), nanowires are essentially a 1-D material. As such, they are used as quasi 1-D channels in quantum transport experiments. Electrons are already radially confined in nanowires, making is easier to confine them in all three dimensions via gating and to form quantum dots. Due to electronic quantum confinement, nanowires feature a number of interesting properties not observable in bulk (3-D) materials (e.g. quantization of conductance).

Nanowires are fabricated from a full range of materials, making them one of the most diverse (versatile) nanostructures available. Most commonly, they are made out of group III-V and II-VI compound semiconductors, as well as group IV semiconductors. Variability among them is large, so their morphology, composition, dimensions, crystallographic orientation among other parameters are used to classify and distinguish between them [13].

There are several advantages to InAs nanowires, compared to other types of

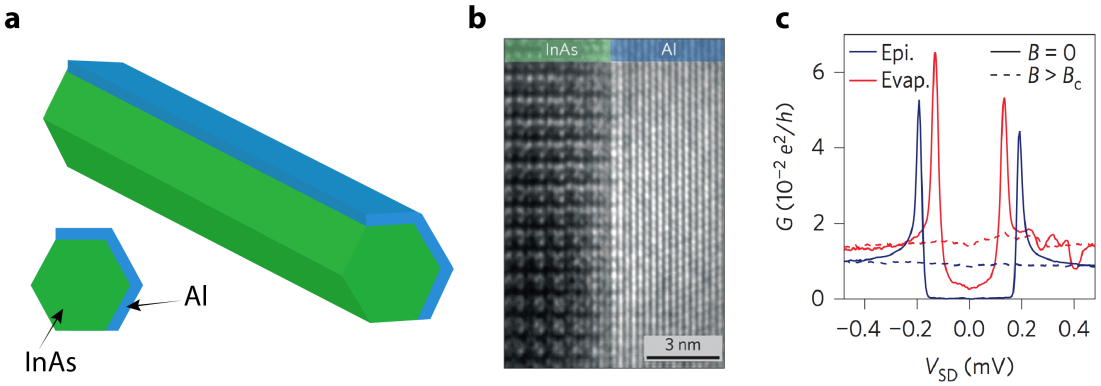

Figure 2.1: *Semiconductor-superconductor hybrid nanowire.* **a)** Illustration of morphology and composition of an InAs/Al nanowire. This nanowire has six facets, three of which are covered with epitaxial Al. **b)** High resolution transmission electron micrograph of the interface between InAs and Al. It highlights an excellent lattice match and uniform interface between the two materials. (adapted from [5]). **c)** A comparison of resulting differential conductance as a function of source-drain bias for a nanowire with epitaxial Al (blue line) and a nanowire with evaporated Al (red line). (adapted from [14]).

nanomaterials and those include [15]:

- Low effective electron mass m^* which leads to increased level spacing.
- Narrow energy bandgap (V_g= 0.36 eV) that allows for charge carrier manipulation with small gate voltages applied.
- High electron mobility due to low level of lattice defects.
- Small work function which results in easier fabrication of Ohmic contacts to the wire.

Coupling semiconducting nanowires with a superconductor results in a very exciting class of new hybrid materials. In 2015, Krogstrup et al. [5] presented a brand new hybrid material consisting of InAs nanowire with epitaxial Al shell grown by the means of Molecular Beam Epitaxy (MBE). Figure 2.1a) shows an example of such a nanowire. This material features defect-free, atomically uniform semiconductor-metal interface, as shown in Fig. 2.1b). Krogstrup et al. reported a lattice mismatch of 0.3 percent, promising highly ordered interfaces. Cheng et al. [14] demonstrated the existence of proximity-induced hard superconducting gap in this hybrid material. It essentially means that there

is no density of states within the superconducting gap, compared to soft gaps, as shown in Fig. 2.1c). This behaviour is a direct result of high interface quality. Hybrid nanowires allow for easy fabrication of devices with superconducting contacts. Semiconductor-superconductor nanowires can be used to explore most exciting phenomena, such as supercurrent [16] and majorana zero modes [2].

2.2 QUANTUM DOTS

To get an idea of what a quantum dot (QD) is, lets first consider bulk crystalline structures. "Free" electron (Sommerfield) theory tells us that valence electrons in solids move freely in all directions (much like electrons in vacuum). However, these electrons are going to be affected by the periodic potential landscape created by the crystal lattice. This interaction is taken into account through the "effective" electron mass m^* that replaces free electron mass m_e. An intriguing result (of the free electron model) is the formation of energy bands in momentum (k) space.[17] This means that there is a continuum of energy states that electrons are allowed to occupy.

Now, lets imagine that all three dimensions of this crystalline structure are decreased to the order of de Broglie wavelength of its electrons. The result of spatially confining electrons in all three dimensions is a 0D structure, popularly known as quantum dot. Unlike in bulk crystals where energy spectrum is continuous, QDs have discrete energy spectrum due to reduced dimensionality(confinement). Quantum dots remarkably resemble a system that appears naturally in the universe - atoms. Therefore, they are often referred to as "artificial atoms" [18]. Typically, QDs are tens of nanometers in size [18] and consist of 10^3 - 10^9 atoms [19].

While in real atoms electrons are confined by the positively charged nucleus, in nanowire-based "artificial atoms" electrons are most commonly confined by the combination of intrinsic nanowire dimensions and electrostatic gating. A nanowire is considered to be a quasi-1D structure since its radius size is on the order of 100 nm, hence it intrinsically confines electrons in radial direction.

The fact that electrons are confined in two dimensions to begin with makes nanowires an excellent choice of material for top-down realization of QDs. Local electrostatic gates are widely used to induce potential barriers and prevent electron movement in axial direction, thus completing confinement in all three spatial dimensions and making QDs [20]. This scenario is illustrated in Fig. 2.3 a). However, there are other ways to achieve zero-dimensionality in nanowires. For example, is possible to engineer a polytypic superlatice within a single nanowire (homostructure) [21][22] such that thin wurtzite (WZ) segments can be controllably embedded along the zinc-blende (ZB) nanowire to form crystal phase-defined QDs [23]. Similarly, heterostructure nanowire growth allows for InP barriers to be introduced in InAs nanowires, which results in formation of QDs between the closely spaced InP sections [24], as illustrated in Fig. 2.3 b).

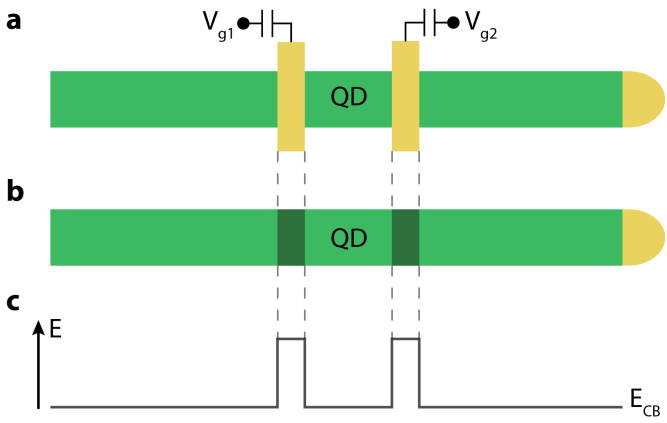

Figure 2.2: *Quantum dot formation in nanowires.* **a)** gating (example top or bottom gates). **b)** crystal phase-defined dot or embedded InP barriers. **c)** edge of conduction band showing the tunnel barriers.

2.2.1 Single Quantum Dots

Quantum dots are the type of nanostructures where Coulomb interactions (electron-electron interactions) play a crucial role in the electron transport. Being weakly coupled to their environment (i.e. to source and drain contacts) is another characteristic of QDs. Important energy scale in connection to QD is charging energy U, defined as $U=\frac{e^2}{C}$ (C is the self-capacitance of a dot). It is

essentially the energy that is required in order to place an extra electron to the QD.

Coulomb blockade effect is an important phenomenon to consider when talking about QDs. It manifest itself by a series of separated peaks in conductance when measured as a function of a plunger gate voltage. In the regions between the peaks, transport is blocked and conductance falls to zero. There are specific conditions to observe this effect. First, $U > k_B T$ in order to prevent transport triggered by thermal excitations. Next, the tunneling resistance R_t of QD has to satisfy the following $R_t > h/e^2$, where h/e^2 is the resistance quantum. This simply means that the QD system needs to be deep into the tunneling regime for Coulomb blockade to happen. Third, it is necessary that the charging energy is larger than the source-drain voltage $U > eV_{SD}$. Figure 2.3 b) illustrates the situation when QD is said to be in the Coulomb blockade regime, hence the transport through the system is blocked.

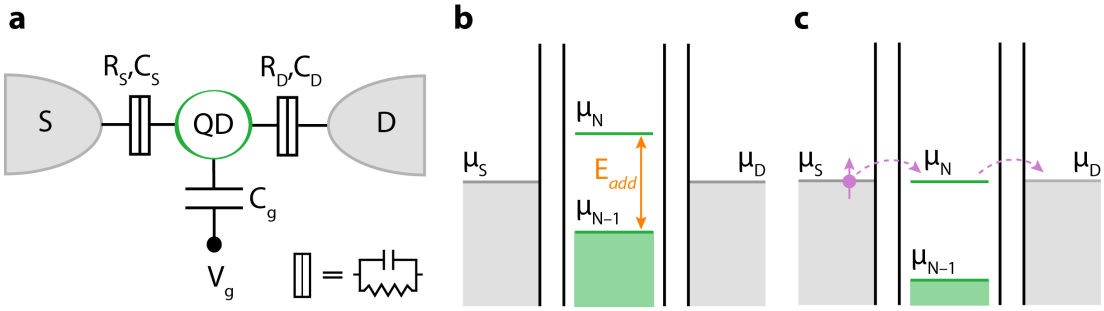

Figure 2.3: *Single quantum dot.* **a)** Schematic illustration of a quantum dot (QD) circuit. QD is tunnel coupled to source (S) and drain (D) contacts, and capacitively coupled to plunger gate (V_g). Tunnel junction is modeled as a resistor in parallel with a capacitor. **b)** Energy diagram of the system in plot a) illustrating the case when QD is in Coulomb blockade (CB) regime. QD is occupied by N-1 electrons and all levels below μ_{N-1} are filled. μ_S and μ_D are the electrochemical potentials of the source and drain. E_{add} is the addition energy, defined as a sum of charging energy and single-particle level spacing. **c)** Electrochemical potential μ_N of the QD is tuned by the gate voltage (V_g) and brought in resonance with source and drain, lifting the blockade and allowing transport through the QD.

In order to get out of the Coulomb blockade regime, one can either apply

finite source-drain bias, or tune the chemical potential of the QD via electrostatic gating to bring it in resonance with μ_S and μ_D. The second option is illustrated in Fig. 2.3 c). QD is out of the Coulomb blockade and sequential tunneling through the dot is enabled, provided that the system is in the low coupling regime ($U \ll \Gamma$). The parameter Γ describes the coupling between the QD and its leads.

2.2.2 Double Quantum Dots

To take a step further, let's consider a system where additional quantum dot (QD) is introduced. There are two ways to do this; second QD can be added in series or in parallel with the first one. By decreasing the separation between the individual QDs they get mutually coupled. There are two components to this coupling to consider: capacitive coupling U_{12} and tunnel coupling t_d. Capacitive coupling arises due to the electrostatic interaction between the electrons residing on the two QDs. This interaction results in the two dots influencing each others energy spectra. Tunnel coupling, on the other hand, requires the wave-functions of the two quantum dots to have a degree of overlap and it leads to splitting of resonant energy levels.[25]

2.3 SUPERCONDUCTIVITY

Since its discovery in 1911 by H. Kamerlingh Onnes [26], the phenomenon of superconductivity has captivated scientific community. To complete astonishment, Onnes observed that electrical resistance of some metals (e.g. mercury, lead) dropped from finite value to zero when material is cooled down below a characteristic critical temperature T_C, as shown in Fig. 2.4 a). Later it was found that not only certain metals but also other types of materials (e.g. ceramics) undergo this phase transition to superconducting state.

Dissipationless transport, or in other words perfect conductivity, is the first characteristic of superconductivity observed on macroscopic level. The second characteristic, discovered by Meissner and Ochsenfeld[27] in 1933, is perfect diamagnetism. As long as the applied magnetic field is below the critical field H_C, it will be both excluded from entering a superconductor and expelled from originally normal sample as it transitions to superconducting state. This phenomenon is known as Meissner effect. Above H_C the superconductivity will break down and sample will transition into normal state. Note that both T_C and H_C are material-dependent properties.

Now, what is the mechanism behind the superconducting phase transition? The main ingredient is the so-called Cooper pair of two electrons. In their pioneering (game-changing) work, Bardeen, Cooper, and Schrieffer[28] showed that two electrons with opposite momentum and spin can form a bound pair when a net attractive interaction exists between them. This positive (second order) interaction is mediated by electron-phonon interaction. The conceptual idea is that negatively charged electron attracts positive ions and causes medium polarization as it is moving through the lattice, illustrated in Fig. 2.4 c)1. Second electron experiences attraction by these positive ions, resulting in an attractive interaction between the two electrons, shown in Fig. 2.4 c)2. Superconductivity arises in case when this effective attraction dominates over the Coulomb repulsive interaction (repulsion)[29].

The resulting Cooper pairs are zero spin particles (bosons) and do not obey Pauli exclusion principle. As such, they can all condense on a single quantum

mechanical ground state (E_{Fermi} in Fig. 2.4 d), opening up a gap in the energy spectrum of the electronic DOS between the ground state and exited states (Fig. 2.4 d). The magnitude of energy gap with no available states, called superconducting gap Δ, is on the order of $k_B T_C$. When $T < T_C$, it is energetically favorable for electrons within $E_{Fermi} \pm \Delta$ to condensate in the form of Cooper pairs, leaving the energy gap behind.

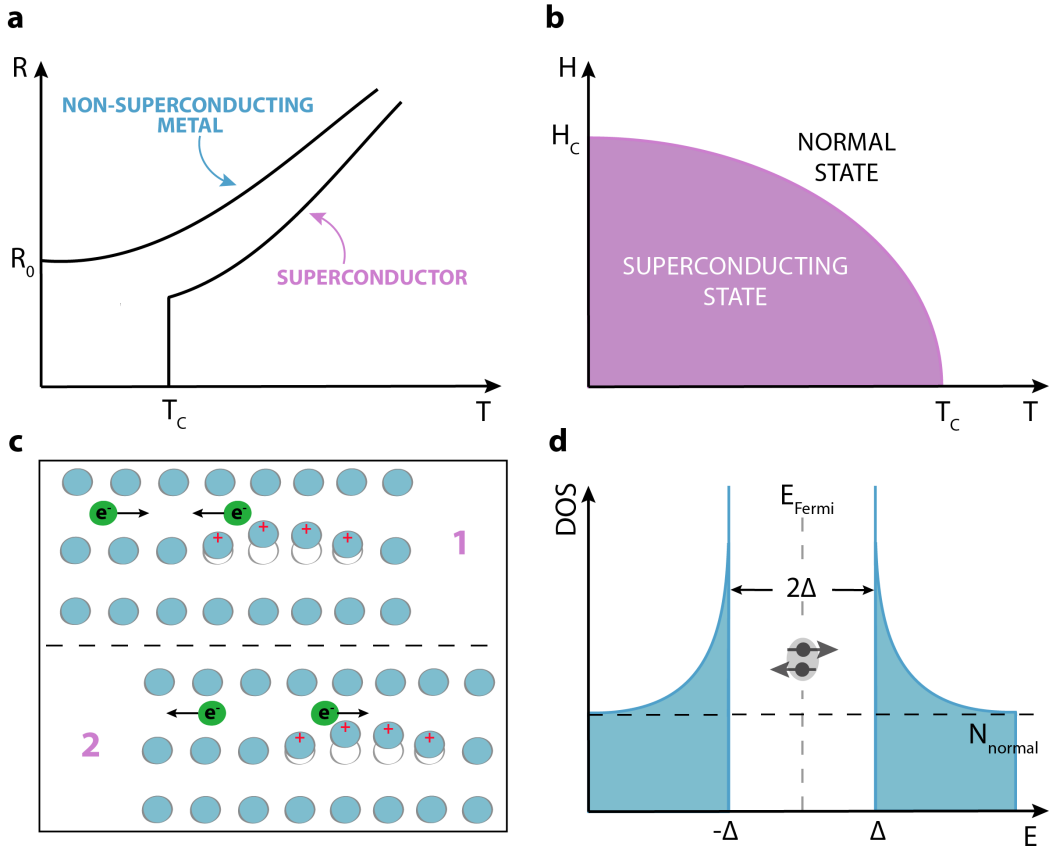

Figure 2.4: *Characteristics of superconducting state.* **a)** Temperature dependence of resistance for superconducting and non-superconducting material. **b)** Temperature dependence of the critical field for type I superconductors. **c)** Illustrative depiction of mechanism that guides the formation of Cooper pairs. **d)** Density of states for a superconductor at $T = 0$. N_{normal} marks the density of states for a material in normal state.

BCS theory predicts that minimum energy required to break a Cooper pair and create two quasi-particles is $2\Delta(T)$ (gap is a function of temperature). In

fact, Δ reaches its maximum value at $T = 0$ and its magnitude is given as:

$$\Delta = 1.764 k_B T_C$$

Above critical temperature Cooper pairs break due to thermal fluctuations and superconducting gap in electron density of states closes/vanishes.

Besides temperature dependence, BCS theory predicts dependence of the superconducting gap Δ on the applied magnetic field B. Hence, there is a critical magnetic field H_C above which a sample transitions from superconducting to normal phase. Applied magnetic field <1 T can break down the the superconductivity in bulk superconductors. Spatially confining the material can increase its critical magnetic field. [reference] For example, if magnetic field is applied parallel to the thin superconducting plane or wire, H_C will be larger as less magnetic field lines are screened out, compared to bulk.

Critical magnetic field H_C is related to the condensation energy of the superconducting phase, or in other words to the difference in free-energy of normal and superconducting states in zero field. Empirically, H_C is approximated by [29]:

$$H_C(T) \approx H_C(0) \left[1 - \left(\frac{T}{T_C} \right)^2 \right]$$

The phase diagram depicting this quadratic relation between applied magnetic field and temperature is shown in Fig. 2.4 b.

Superconductors are classified into two types, type I and type II, depending on how the superconductivity breaks down when finite magnetic field is applied. Type I superconductors expel all magnetic flux and behave as perfect diamagnets (Meissner effect) until sample turns normal at H_C.

Type II superconductors are characterised by two critical magnetic fields, H_{C1} and H_{C2}. Starting at H_{C1}, flux starts to penetrate the sample and it continuously increases until H_{C2} is reached, at which point superconductivity breaks down. The flux penetrates the sample in the form of vortices, each vortex carrying a flux quantum $\phi_0 = hc/2e$. Between H_{C1} and H_{C2} the superconducting sample is in the so-called mixed state or Schubnikov phase [tinkham].

When discussing superconductivity, it is important to consider two characteristic length scales, coherence length ξ_0 and London penetration depth λ. Coherence length determines the spatial extent of the Cooper pair. This length scale characterizes the distance to which a phase coherence can travel into a non-superconducting region before it decoheres. Assuming that only electrons in the range of $E_F \pm k_B T_C$ are relevant, one can estimate the coherence length using the Heisenberg uncertainty relation. Momentum uncertainty Δp of these electrons is $\Delta p = k_B T_C / \upsilon_F$. From here, one finds that:

$$\Delta x \geq \frac{\hbar}{\Delta p} \approx \frac{\hbar \upsilon_F}{k_B T_C}$$

Estimating the coherence length by the position uncertainty δx, one finds that:

$$\xi_0 = \alpha \frac{\hbar \upsilon_F}{k_B T_C} \sim \frac{\hbar \upsilon_F}{\Delta}$$

where α is a constant close to unity, υ_F is Fermi velocity, and T_C is the critical temperature of the superconductor. Note the inverse proportionality between ξ_0 and Δ suggesting that superconducting materials with higher T_C have lower ξ_0. Coherence length ξ_0 is smaller than (the electron) mean free path l_e is indicative of a system that is in "dirty regime" since phase decoherence can occur due to scattering. Accounting for this fact, an effective coherence length has to be considered and is given as[29]:

$$\xi_{eff} = \sqrt{\frac{\pi \hbar \upsilon_F l_e}{24 k_B T_C}}$$

2.3.1 Bound States

Bound states or sub-gap states are excitations that exist within the superconducting band gap where otherwise density of states is zero. In fact, one is concerned with understanding the physics of superconductors in close proximity to quantum dots, as it is the interaction between them that gives rise to bound states. They will arise when the system meets a set of specific conditions, which are

discussed in this section. When Andreev reflections [1] become resonant, which is often the case in small systems, then sub-gap structures, known as Andreev Bound States (ABS), get formed [30]. Andreev bound states come in pairs and make up a two level system that is symmetrical around E_{Fermi}[31]. This thesis is concerned with ABS that get formed in hybrid systems where QDs (acting as magnetic impurities) are coupled to superconducting lead (QD-S setup).

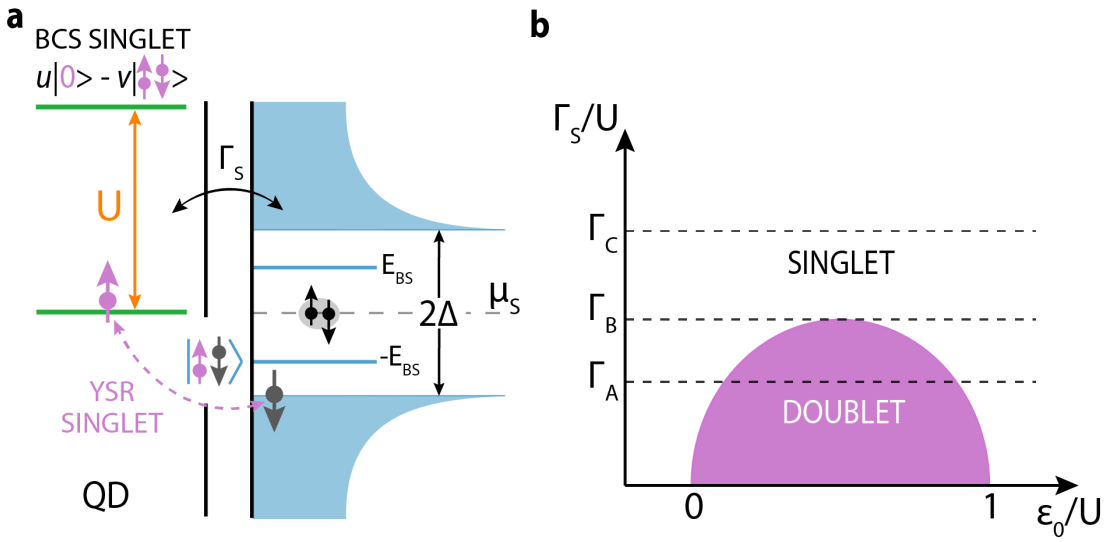

Figure 2.5: *Yu-Shiba-Rusinov bound states.* **a)** The energy diagram illustrating the the singlet correlation between a single electron on the QD and a quasiparticle in superconductor that result in the formation of YSR bound state. U is the charging energy, Δ is the superconducting gap, μ_S is the chemical potential of superconductor, $\pm E_{BS}$ is the energy of bound states, Γ_S describes the coupling between the QD and superconductor. **b)** Phase diagram in the plane of coupling to the superconductor versus QD occupation, both normalized by the charging energy. Within the pink dome-shaped region it is the spin doublet $|D\rangle$ that is stabilized, while spin singlet $|S\rangle$ is stable outside of it. (adapted from Lee2013 and Zitko2015)

Based on the underlying mechanism that leads to the formation of ABS in the QD-S setup, they can be divided in two types: Yu-Shiba-Rusinov (YSR)[32]–[34] bound states (or simply Shiba states) and bound states that arise in superconducting atomic limit[31] (proximity induced states [30]). The condition for YSR states is that $U \gg \Delta$, while the opposite, $U \ll \Delta$, is necessary for proximity

[1] explain in 2 sentances

induced states. This section focuses on YSR bound states as they are observed in the given type of systems since QD can be tuned in such a way that is acts like a magnetic impurity.

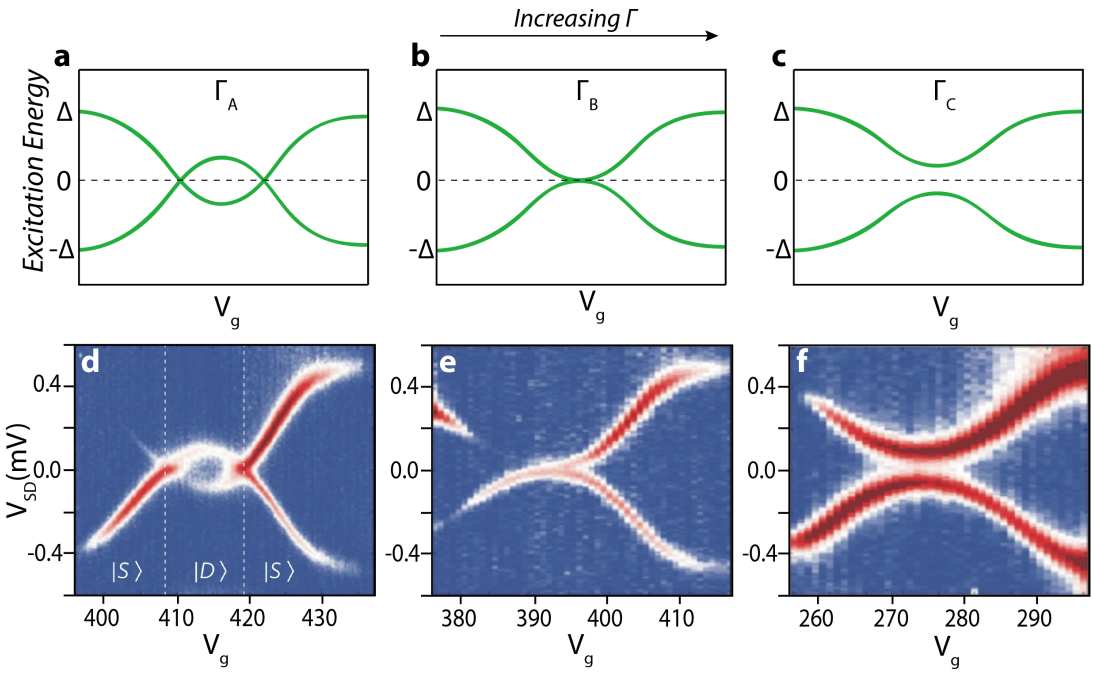

Figure 2.6: *Coupling strength dependence of YSR bound states.* Plots **a-c)** show illustration of predicted behaviour for YSR bound states as the coupling to the superconductor increases. The loop-like feature seen in a) disappears signaling the quantum phase transition from doublet to YSR singlet ground state. $\Gamma_{A/B/C}$ corresponds to the positions marked on the Fig. 2.5 b). Plots **d-e)** show the bias spectroscopy of subgap states for different coupling strengths. The observed behaviour agrees with the plots above. [adapted from Lee2015]

Figure 2.5 a) illustrates the energy diagram and the process that results in the YSR bound states. Namely, magnetic impurity (QD with odd occupation) Phase diagram in Fig. 2.5 b) shows the regions where spin doublet $|D\rangle$ and singlet $|S\rangle$ are stabilized. Note that the region that favours doublet shrinks as the coupling to the superconducting lead is increased. Eventually, for large enough coupling, singlet ground state will prevail regardless of the occupation of the QD.

2.4 LITTLE-PARKS EFFECT

In 1962, W. A. Little and R. D. Parks published a paper that investigated the effect of applying axial magnetic field to the thin-walled, hollow superconducting cylinder [35]. By measuring the modulation of resistance as a function of magnetic field, they demonstrated that superconducting critical temperature T_C of such a cylinder periodically oscillates [or varies] as a function of axially applied magnetic field B, i.e. parallel to the cylinder. Instructive theoretical overviews of what is known as the Little-Parks effect can be found in Ref. [36] and [37], while this section focuses on introducing the key ideas and concepts.

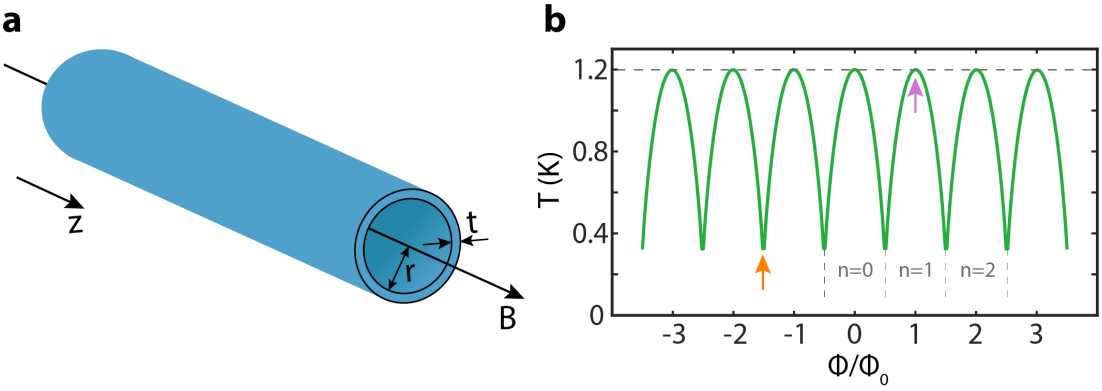

Figure 2.7: *Little-Parks experiment in the limit* $t \ll r$ *(idealized case).* **a)** An illustration of thin-walled, hollow superconducting cylinder with thickness t and radius r in axially applied magnetic field. **b)** Modulation of critical temperature as a function of the applied flux Φ, normalized by flux quantum Φ_0, for a cylinder with vanishing thickness. Orange arrow indicates just one example where the critical temperature T_C shows maximum reduction, while pink arrow points to an example where the reduction of T_C is zero. n is the winding number (energetically favorable number of fluxoids piercing through the cylinder).

In their experiment, Little and Parks investigated a hollow cylinder (see Fig. 2.7 a) with the radius much larger than the London penetration depth ($r \ll \lambda_L$), and wall thickness much smaller than the London penetration depth ($t \ll \lambda_L$). In the limit $t \ll \lambda_L$, screening currents induced by the applied magnetic field cannot expel the field lines from the superconductor which results in the uniform magnetic field inside and outside the cylinder wall. In

this case, flux piercing through the cylinder ($\phi = \pi r^2 B$) is not strictly quantized [38]. In contrast, it is the fluxoid that is always quantized as $n(h/2e)$ [29].

Ginzburg-Landau mean-field theory provides a good framework to understand the key ideas behind the Little-Parks effect. This section only briefly presents the main results and conclusions derived from them. One of those results is the expression that relates the variation of the critical temperature to the magnetic flux:

$$\frac{\Delta T_C}{T_C^0} = -\frac{\hbar^2}{4mr^2\alpha}\left(n - \frac{\Phi}{\Phi_0}\right)^2$$

where T_C^0 is zero-field superconducting critical temperature and Φ is the applied flux. Detailed analytical derivation, as done by Abrikosov, can be found in [38]. From this expression follows that variation of the critical temperature as a function of flux is defined in the form of periodic array of parabolas (see Fig. 2.7 b), where each parabola corresponds to an interval designated by integer n. These parabolas are centered around the corresponding integer values of $\frac{\Phi}{\Phi_0}$. Maximum reduction of the critical temperature T_C occurs when $\frac{\Phi}{\Phi_0}$ takes odd half-integer value (see orange arrow in Fig. 2.7 b). Oppositely, this reduction is 0 when $\frac{\Phi}{\Phi_0}$ equals to an integer and one obtains the highest T_C possible (T_C=T_C^0) (see pink arrow in Fig. 2.7 b). This is in agreement with the phase diagram presented in the paper by Little and Parks [35].

The maximum solution $T_C(\alpha)$ to the implicit equation

$$\ln\left(\frac{T_C(\alpha)}{T_C^0}\right) = \Psi\left(\frac{1}{2}\right) - \Psi\left(\frac{1}{2} + \frac{\alpha}{2\pi T_C(\alpha)}\right) \tag{2.1}$$

is the corrected superconducting transition temperature at finite magnetic field ($B \neq 0$)[references for this equation]. Here, digamma function $\Psi(x) = \frac{\Gamma'(x)}{\Gamma(x)}$ and α is the pair-breaking parameter. When magnetic field is applied parallel to the superconducting cylinder, the pair-braking parameter is given by [references]

$$\alpha_{\parallel} = \frac{4\xi_0^2 T_C^0}{A}\left[\left(n - \frac{\phi}{\phi_0}\right)^2 + \frac{t_S^2}{d_F^2}\left(\frac{\phi^2}{\phi_0^2} + \frac{n^2}{3}\right)\right] \tag{2.2}$$

where ξ_0 is superconducting coherence length at $B = 0$, A is the area of the cylinder cross-section, n is the winding number, t_S is the thickness of the cylinder wall, and d_F is the diameter of the cylinder. In dirty-limit ($l_e << \xi_0$), $\xi_0 = \sqrt{\pi\hbar v_F l_e / 24 k_B T_C^0}$ is the expression for coherence length, with l_e being the mean free path and v_F the Fermi velocity [29]. The pair-breaking parameter α essentially controls the critical temperature T_C. Note that through α, the finite-field T_C is strongly dependant on the sample parameters.

The pair-breaking parameter $\alpha_{\parallel}$ consists of two terms - first one is periodic and the second one is non-periodic in flux. In case when $\frac{t_S}{d_F} < 1$, $\alpha_{\parallel}$ is dominated by the first term for $n = 0$. This term takes maximum value at odd half-integer $\frac{\Phi}{\Phi_0}$ and minimum value (zero) at integer $\frac{\Phi}{\Phi_0}$. For $n > 0$, it is the second (thickness-dependent) term that gets significant and takes over in $\alpha_{\parallel}$. This can result in large values of pair-breaking parameter even when $\frac{\Phi}{\Phi_0}$ is an integer, causing finite depression of critical temperature at those points [39]. The second term, contributes to the continuous increase of $\alpha_{\parallel}$ and destruction of superconductivity above critical B-field. It is introduced as a correction to the pair-braking parameter in the case of finite thickness of superconducting cylinder [40]. This trend of quadratic increase of $\alpha_{\parallel}$ superimposed on its periodic component is visible in fig. X. In the limit of $t_s \ll d_F$, this thickness-dependent quadratic component vanishes [41].

An applied current bias can also drive the superconducting cylinder to the normal state. The relationship between the critical current $I_C(\alpha)$ and the corresponding critical temperature $T_C(\alpha)$ is given by the expression

$$I_C(\alpha) = I_C^0 \left(\frac{T_C(\alpha)}{T_C^0} \right)^{3/2} \tag{2.3}$$

as presented in [7]. Here, I_C^0 is the critical current at $B = 0$. Note that $I_C(\alpha)$, just like $T_C(\alpha)$, is dependent on the applied magnetic field.

The above outlined theory can be used to fit the Little-Parks type of the experimental data as demonstrated in [7]. First, α should be calculated for all values of Φ using the equation (2.2). All the necessary parameters are known or can be deduced from the independent measurements. Next, equation

(2.1) should be numerically solved for $T_C(\alpha)$ for all α values calculated in the previous step. Finally, the critical current $I_C(\alpha)$ can be extracted by plugging solutions for $T_C(\alpha)$ into the equation (2.3).

Magnetic field applied perpendicularly to the superconducting cylinder induces additional screening currents which contribute to Cooper pair breaking. A second pair-breaking parameter

$$\alpha_\perp = \frac{4\xi_0^2 T_C^0}{A_\perp}\frac{\phi_\perp^2}{\phi_0^2}$$

is introduced to take into account the effects of applied $B_\perp$ [7], [29], [42]. Here, $\Phi_\perp$ is the magnetic flux created by $B_\perp$. Note that $\alpha_\perp$ is non-periodic. Finally, the total pair-breaking parameter is simply the sum of the two terms $\alpha = \alpha_\parallel + \alpha_\perp$ [29], [43] and it accounts for the combined effects of $B_\perp$ and $B_\parallel$. Vaitiekenas et al. [7] showed that an applied transverse magnetic field can be used to transition a device from non-destructive to destructive Little-Parks regime.

2.4.1 Destructive vs. Non-destructive Regime

An analysis done by de Gennes in 1981 [44] using the Ginzburg-Landau framework yielded an interesting result. It predicted that that the infinitesimally thin superconducting ring, placed in magnetic field perpendicular to its plane, can be in two different regimes: destructive and non-destructive. For the non-destructive regime the critical temperature T_C is periodically reduced but remains finite for all values of the applied magnetic field lower than the critical field B_C. Hence, the superconductive phase prevails at low temperatures. In the case of the destructive regime, the regions of normal state emerge in finite magnetic field intervals, even at $T = 0$ K. The reason for this is that maximum reduction of T_C is so large around the B-field values that correspond to the odd half-integers of the magnetic flux quantum Φ_0, so that T_C is quenched to zero while the system assumes a finite resistance. This effectively results in the flux-tuned quantum phase transition. Further, in the case where the length of the cylinder (see Fig. 2.7 a) is zero, the relation of r and the zero-

temperature superconducting coherence length $\xi(0)$ determines the criterion for seeing destructive regime. More precisely, when $2r < \xi(0)$ the normal phase will occur around odd half-integer values of Φ_0, even at T=0, thus the system is in destructive regime. The opposite is true for $2r > \xi(0)$, where non-destructive Little-Parks oscillations are observed.

In 2010, Schwiete and Oreg [40] reported that the maximum reduction of T_C, and therefore the emergence of destructive regime, depends on the ratio $2r/\xi(0)$. When $2r/\xi(0)$<1.2, the normal phase is expected to appear around the odd half-integer multiples of Φ_0, enabling the recurring destruction of superconductivity.

The effect of finite cylinder wall thickness, among other things, was investigated by Dao and Chibotaru in 2009 [41]. They showed that a cylinder initially in non-destructive regime (satisfying the above mentioned $2r/\xi(0)$ condition) can be transitioned into destructive regime if its wall thickness is increased enough. This is a consequence of thickness-dependent term in equation (2.2) which continuously increases the pair-breaking parameter, making the T_C reduction larger. Hence, destructive regions around odd half-integer of Φ_0 can appear for certain wall thickness.

3 FABRICATION AND MEASUREMENT SETUP

First sections of the following chapter are dedicated to the discussion of nanowire-based device fabrication. The objective was to fabricate double quantum dot system in parallel nanowire geometry (one quantum dot per wire), with normal and superconducting contacts (N-S device). All the processing steps are outlined, while the most important and challenging parts are discussed in more details. Fabrication efforts described in this chapter yielded devices that were measured and results reported in subsequent chapters. The second part of this chapter is concerned with measurement techniques and experimental setup (including dilution refrigerator) used for data collection. More detailed account of fabrication recipes (protocols) can be found in Appendix B.

I have personally contributed to the development and optimization of the entire device fabrication process. Moreover, I participated as a member of three people in most of the chip bondings, loadings as well as the measurement of devices.

3.1 MATERIAL OF CHOICE: PARALLEL NANOWIRES

A new and exciting type of nanowire-based heterostructure, grown by Thomas Kanne Nordqvist and his team, is used for the fabrication of devices that are being reported in this work. This heterostructure is comprised of two InAs nanowires that are being merged by the superconducting layer, in this case Al. The nanowires are being grown by the means of Molecular Beam Epitaxy (MBE) and Al layer is deposited in-situ without breaking the vacuum (the so-called

epitaxial Al, due to the perfect epitaxial match between Al and InAs). All details concerning the growth of these structures can be found in [45].

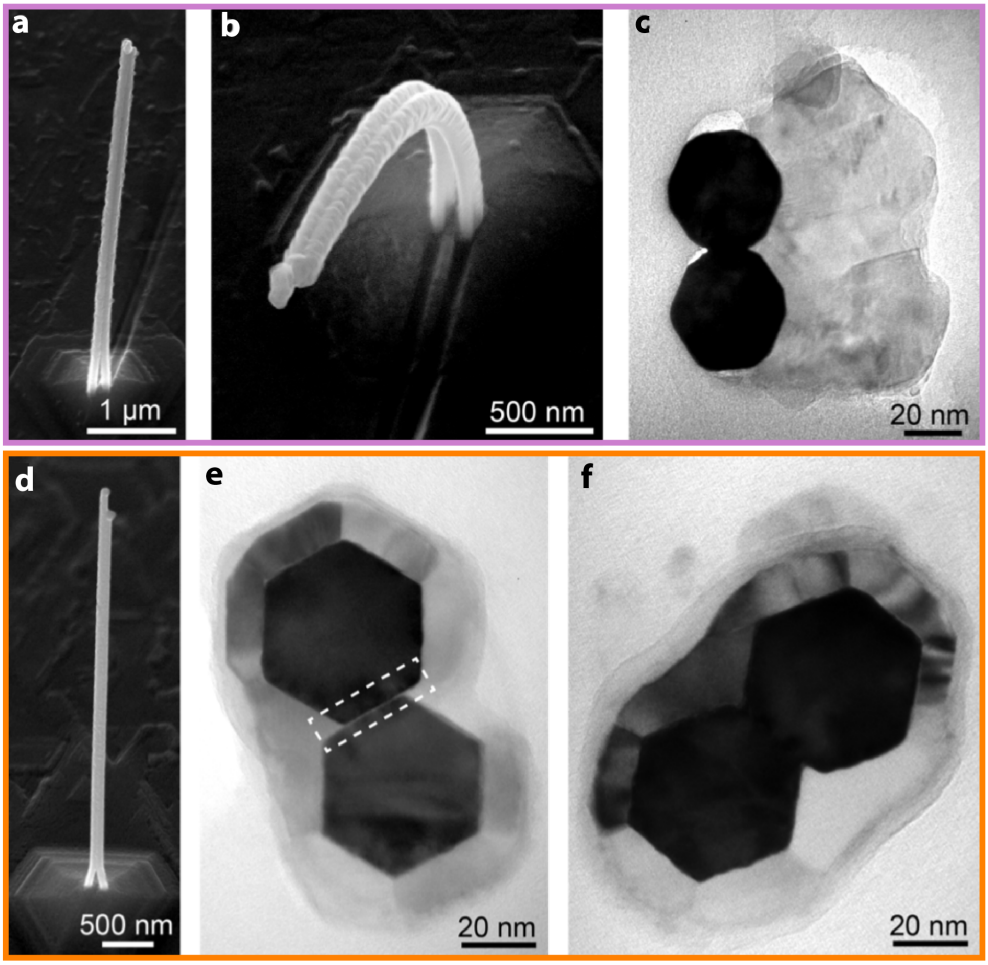

Figure 3.1: *Half-shell and full-shell InAs/Al double nanowire heterostructure.* **a-c)** Half-shell double nanowires (DNW) with the SEM micrograph showing an example of structure bending in **b)** and TEM image showing the example of a cross-section in **c)**. **d-f)** Full-shell DNW with TEM image in **e)** showing small gap between the two wires and another TEM image in **f)** showing an example . Adapted from [45].

Figure 3.1 gives an overview of the types of heterostructures used for the experiments reported in this thesis. Enclosed in pink box (Fig. 3.1 (a-c)) are the images of half-shell InAs/Al double nanowires (DNW). Bending of the nanowires away from Al is seen in Fig. 3.1 b). There are two possible causes to this: different thermal expansion coefficients in InAs and Al, or the strain at

the interface between the two materials [45]. Regardless of the cause, nanowire bending introduced problems during fabrication. For thick connecting Al layer (in combination with large nanowire diameter) it was observed that the wires would not relax during the nanowire transfer (see sec. 3.2.3 for more). As a consequence of this, it was impossible to get both wires to sit flat on the substrate. They would rather sit on top of each other, with only one wire in contact with the substrate. Figure 3.1 c) shows an example of how aluminum half-shell is connecting the wires. In this particular case, the separation between the wires is small, that they merged together during the growth process. Half-shell InAs/Al DNW were used to make devices with parallel quantum dots (Chapter 4 and 5).

Wafer Code	Al thickness	Wire diameter	Stem pitch	CC	FF
QDev 822	100 nm	60 - 105 nm	50 - 290 nm		✓
QDev 872	100 nm	46 - 91 nm	50 - 160 nm	✓	✓
QDev 898	12-15 nm	50-100 nm	50 - 160 nm	✓	✓
QDev 903	17 nm	40 - 50 nm	70 - 150 nm	✓	✓

Table 3.1: *Parameters summary of nanowire batches used for device fabrication.* CC stands for corner-to-corner, while FF stands for facet-to-facet wire orientation (configuration) in respect to each other. Check mark in either column indicates that particular growth includes given orientation. Reported values for wire diameter are average values based on post-growth measurements. Wafer QDev 898 coontains wires with full-shell Al. All the others have double nanowires with half-shell aluminum.

The same heterostructure but this time with the full shell of Al is shown in Fig. 3.1 (d-e). The important thing to note is that the very small (e) or non-existent (f) distance between the two wires. Ideally, there would be a separation between the wires to avoid the danger two wires behaving as one. The Al shell seems nonuniform in certain domains, varying in thickness, but of much better morphological properties compared to the example thicker Al film. These wires did not have a problem with being bent, possibly due to decreased thickness of Al shell[45]. Once transferred to the substrate they would be flexible and relatively easy to work with.

Over the time, and as a part of the optimization process, nanowires from multiple growth batches were used for device fabrication. The most relevant properties of the used nanowire batches are summarized in Table 3.1. The advantage of changing batches is that nanowire properties were improving with every new batch. However, the disadvantage was that for every new wafer the fabrication protocol had to be revised. Most challenges turned out during nanowire transfer (see sec. 3.2.3).

A number of different device geometries can be realized using InAs/Al DNW including parallel QDs in N-S junction, Josephson Junction geometry, and superconducting island based geometries.

3.2 NANOFABRICATION OF DEVICES

Over the past few decades, advances in nanofabrication allowed scientists to design, fabricate and study ever decreasing, submicron systems. Following subsections are dedicated to presenting concepts, techniques and fabrication steps which proved to be paramount in realizing parallel double quantum dot systems.

3.2.1 Electron Beam Lithography

Nanodevice fabrication would not be possible without modern lithographic techniques. Electron beam lithography (EBL) was used to fabricate nanometer scale features and it will be briefly discussed. This technique uses a highly focused electron beam to transfer/imprint a computer generated pattern onto the electron-sensitive material. These materials are called resists and they are composed of long-chain polymers. Most commonly used resist for EBL is called Poly(methyl methacrylate) or PMMA. It gets deposited on top of the sample by spin-coating (Fig. 3.2 b) to form as uniform resist layer as possible. Blow drying the sample before spinning the resist is crucial to avoiding dust-induced irregularities. When exposed with electron beam (Fig. 3.2 c), polymer chains break upon the energy absorption and become more soluble. Overexposure due to backscattered electrons is accounted for and corrected by software during the

pattern design stage. Nevertheless, the side profile of the exposed pattern tends to be undercut. Broken polymer chains from the exposed areas are removed with a developer solution (Fig. 3.2 d), at which point the exposed pattern is said to be developed. Development is followed either by etching (Sec. 3.2.4) or metallization (Sec. 3.2.5), as illustrated by Fig. 3.2 e) and f). Upon the completion of desired process, the excess resist is removed by a stronger solvent.

In the case of devices we studied, EBL is used to define all sub-micron elements, those being alignment marks on the blank chips, etch windows, contacts and gates.

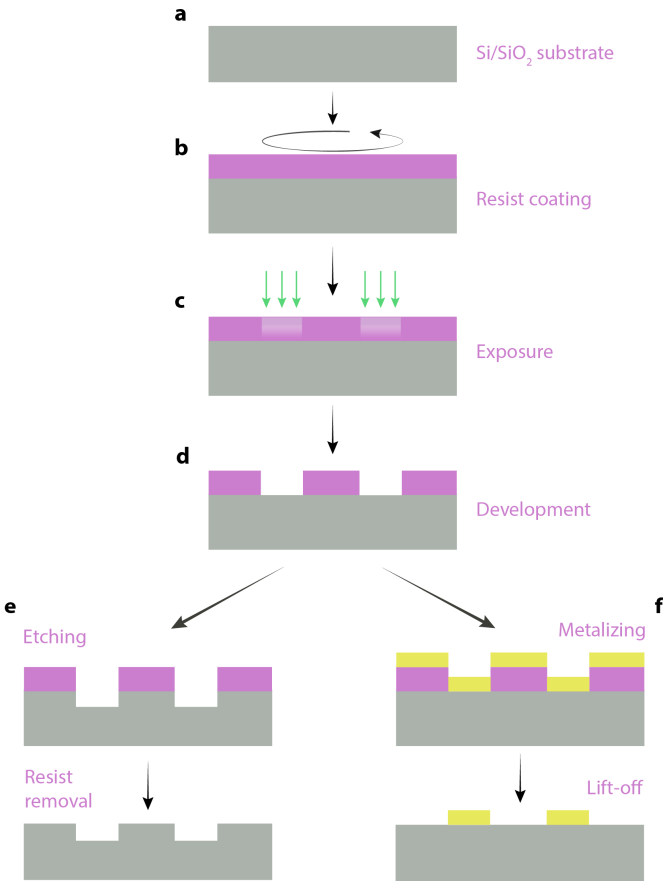

Figure 3.2: *Steps in lithography.* **a)** Preparing the substrate by cleaning it with IPA and acetone. **b)** Spin-coating the sample with chosen resist, followed by soft baking. **c)** E-beam or UV exposure of the pattern. **d)** Removal of the resist from the exposed area. **e)** Dry or wet sample etching. **f)** Metal deposition on the sample.

3.2.2 "Blank Chip" Fabrication

The fabrication of blank chips is a two step procedure where bonding pads are defined by the means of photolithography, whereas alignment marks are defined by electron beam lithography (EBL). Fabrication starts with a full 2-inch Si wafer. The exact wafer type used is a highly doped Si substrate with a 200 nm thick layer of SiO_2 on top. Out of 2-inch wafer, a smaller piece measuring 2.1 cm x 2.1 cm was cut with the help of a diamond pen or manual scriber and cleaved. After processing is finalized, such piece of wafer yields 16 blank chips in total, of approximate size 5 mm x 5 mm. Depending on the cleaving, the exact size of each individual chip can slightly vary. It has been seen that cutting with diamond pen and afterwards cleaving can introduce damage (substrate chipping and scratching) along the edges and the surface of the chip. As a consequence, the oxide layer could get damaged, which could cause leakage during measurements. To prevent this, it is useful to spin a thin layer of resist on the sample before cutting and cleaving. Additionally, it is advised to use manual scriber for finer, more precise cut lines. The procedure itself becomes more involved, but it reduces the possibility of damage.

Figure 3.3 shows a single chip design created in KLayout (CAD software). All large features, coloured in purple, were exposed using Heidelberg μPG501 ultraviolet (UV) lithography system. UV lithography is perfectly adequate for exposing features larger then 1 μm. Greatest advantage of using UV lithography in this step comes from the decrease in total fabrication time, as it is faster then EBL. However, to expose fine features coloured in red in Fig. 3.3, it was necessary to resort to EBL. The reason for this comes from diffraction limit of light, making UV lithography inadequate for accurately exposing submicron features. Figure 3.3 a) shows the position of four global alignment marks, one at the each chip corner. These alignment marks are very important as they are used to align all subsequent exposure designs. The EBL system used allows for both manual and automatic mark registration. Automatic alignment eliminates the possibility of human induced error at this step, thus it is the preferable choice. Thickness of alignment marks needs to be at least 100 nm for successful

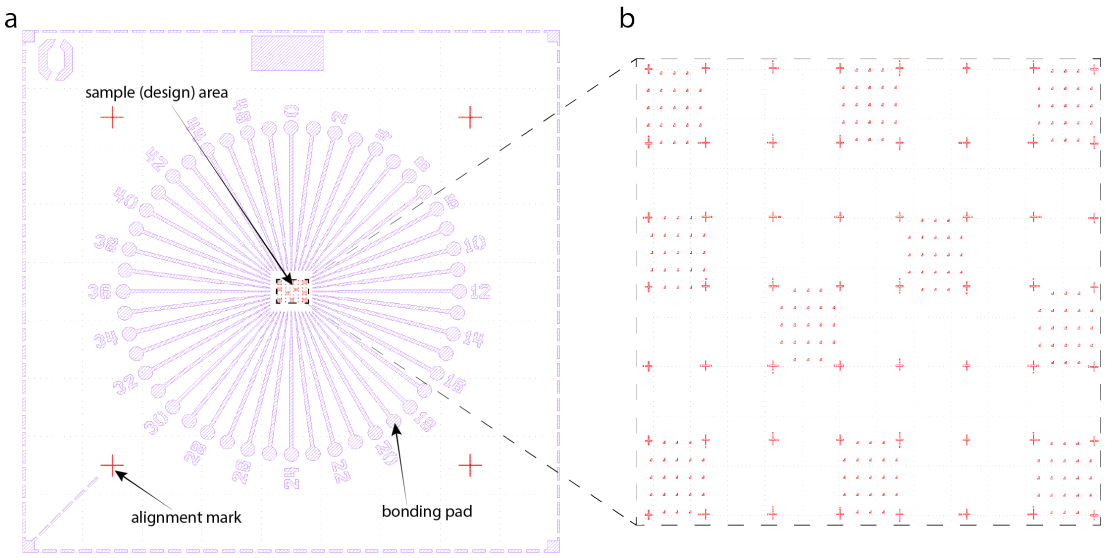

Figure 3.3: *CAD design of a "blank chip".* **a)** Main features in this design include alignment marks, bonding pads and sample area. There are in total four alignment marks which are used during EBL exposure. Distance between two neighbouring marks is 3 mm. Bonding pads (including the leads connected to them) are numbered and circularly distributed for easier bonding. Besides these, each chip has a rectangle distinguishing the top of the chip and a number in the upper left corner for reference. **b)** Close-up of the sample area. This is where the nanowires are deposited for further processing. Crosses and smaller marks are used for device design and alignment of contacts and gates.

automatic alignment using Elionix ELS-7000 EBL system.

Fine alignment marks shown in Fig. 3.3 b) are located in the sample area where nanowires get deposited. To be able to accurately design contacts, gates, and any other circuit element around the wire, it is necessary to match actual location of the wire on the chip and on the CAD design as accurately as possible. Good alignment is of greatest importance and this step requires special attention. Let's suppose that the position of the wire on the sample design area (shown in Fig. 3.3 b) is not matching well to the physical position of the wire on the chip. Any contact or gate subsequently designed is not going to be successfully fabricated. There is going to be a discrepancy between designed device and realized device. This discrepancy can be anywhere from negligible to severe. In the most severe case, contacts and gates are not going to be in the desired

places at all; hence sample will not be usable. To avoid such scenario, ten sets of superfine alignment marks are added to the blank chip design. This small, but significant alteration, resulted in the improved accuracy and resolution when translating wire's physical position into the CAD design, as well as designing the device elements. Full fabrication recipe for blank chips, including all steps and details, can be found in Appendix B.

3.2.3 Nanowire Transfer

Once the blank chip is ready, next step would be to place some nanowires on it. To do this, an *eppendorf TransferMan 4r* instrument for micromanipulation was used. The idea behind the operation of such instrument is that one can use an optical microscope and a 3D joystick-controlled probe needle to break the wire from the growth wafer, pick it up and deposit it on the target substrate. A wire, or a pair of wires, gets attached to the needle tip via Van der Waals forces. Smooth and gentle wire deposition is necessary to prevent puncturing through the substrate oxide.

Unlike the cases where growth wafers are manipulated post-growth resulting in nanowires laying on the substrate, detached from it, our nanowires were standing upwards, attached to the growth substrate. Hence, detaching wires from the substrate was the first obstacle in nanowire transfer. The efforts to overcome this issue resulted in two solutions:

1. *Method One*
   (a) Adjust optical microscope such that the focus is on the very tip of the wire.
   (b) Slowly approach the wire tip with the probe needle, gently touching it.
   (c) Simultaneously move the needle slowly down the wire and adjust the focus, until the wire breaks off the substrate and ends up laying on it.
2. *Method Two*
   (a) Adjust optical microscope such that the focus is at the nanowire stem.

(b) Gently approach the wire stem with the needle and push to break it off.

Both approaches proved to be useful in the case of parallel nanowires, with the first method being more successful. It was observed that nanowire pair tends to break off harder when attempted to break it directly at the stem. Often, wire would end up attaching inadequately to the needle upon the breakage, making it hard or even impossible to deposit. This was not experienced so often when the first method was used.

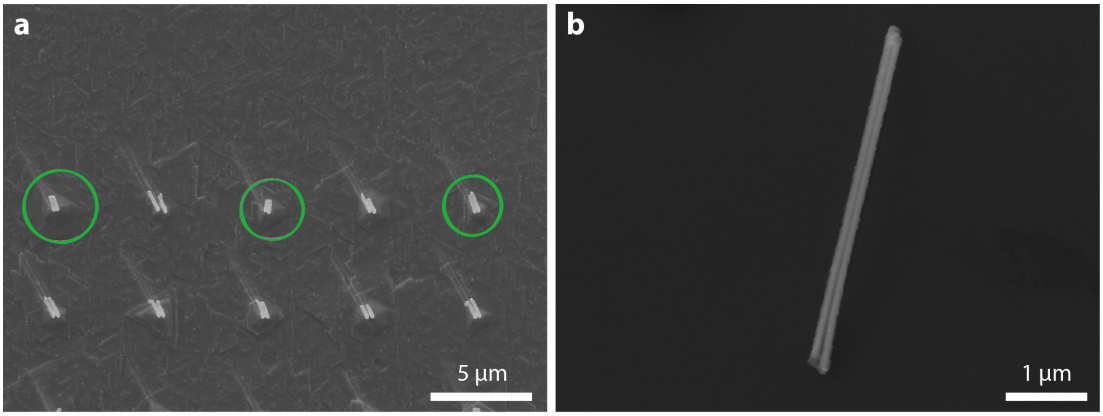

Figure 3.4: *Nanowire transfer.* **a)** An SEM image of growth wafer showing nanowires after growth. Encircled pairs of nanowires are selected to be transferred. **b)** An SEM image of a nanowire after being picked up from the growth substrate and deposited on the chip.

Nanowire transfer can be either straightforward or quite time-consuming and involved fabrication step. When working with uniform, high-yield growth substrates (as often are those carrying single wires), the process is as simple as randomly picking up wires and placing them on the chip. However, this was not the case with our material of choice. Although it was quite impressive growth, wafers featuring parallel nanowires came with very low yield. This made the random transferring approach inadequate and called for a new strategy. To overcome this challenge, an alternative, systematic wire transfer method was devised. This method includes:

1. SEM imaging the growth wafer to locate and mark the position (row and

column) of desired pairs of wires.

2. Finding those pairs using the optical microscope at the micromanipulator setup.
3. Picking up and placing wire pairs on the chip.
4. SEM imaging the chip to evaluate the nanowire deposition.
5. *(optional)* Re-positioning the wires on the chip to get them to desired orientation.

Figure 3.4 shows the results of steps 1 and 4. From Fig. 3.4 a) one can reason why random transfer method would not work well in this case. The yield is quite low, meaning there are many nanowire pairs that are not successfully connected by superconductor. Hence, one would likely be transferring single wires instead. To prevent this, it is necessary to image and select wires before micromanipulation step. Although it is time consuming procedure, there are some advantages to doing so.

Firstly, one can have a control over properties (wire diameter and stem pitch) of nanowires that are being transferred on the chip. The growth wafer is accompanied with design layout, specifying wire diameter and stem pitch. Hence, it is possible to keep track of wires that are being transferred in a very systematic and organized way. This ultimately provides a better understanding of the system that is being experimented on.

Secondly, imaging the wires after the transfer (step 4) reveals the orientation of the wire in respect to the chip surface. An illustration of the three possible orientations is shown in Fig. 3.5. This information is particularly important to know, as it determines the way metallic contacts to the device are fabricated. If the situation is as shown in Fig. 3.5 a), then both normal and superconducting contact can be created in the same step, simplifying the fabrication. This is due to the fact that superconductor is below the nanowires... However, if the wire sits on the chip as shown in Fig. 3.5 b), then normal and superconducting contacts are fabricated in two separate steps, adding to the device processing time.

The least favoured case is shown in Fig. 3.5 c). It is still possible to make

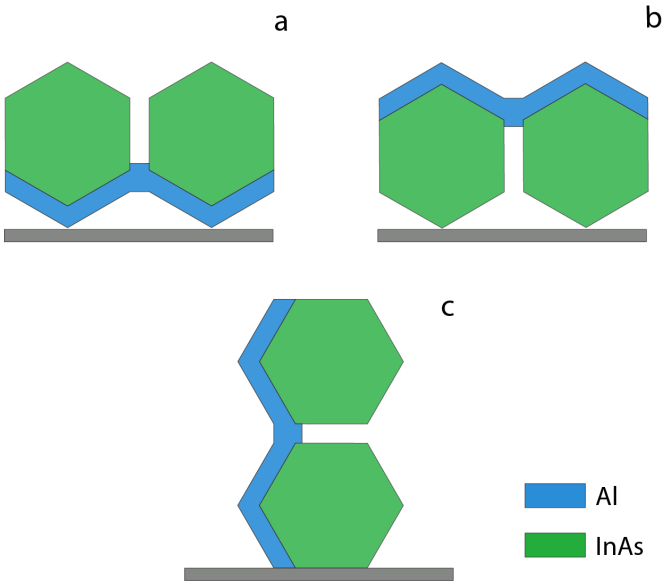

Figure 3.5: *Nanowire orentation on the substrate.* **a)** Al half shell is facing the substrate (gray). **b)** Nanowire is sitting on the substrate with Al half shell on top. **c)** Nanowire is sitting with the Al shell on the side, perpendicular to the substrate.

a device, but only one wire can be effectively gated. When most wires are oriented in this way it is necessary to go back to micromanipulator and try to gently push and flip the wire into either orientation a) or b). It is observed that the attempts of orientation correction are not always successful; whether the nanowire flips or not is mostly a random event.

A useful trick was discovered that helps minimize, and sometimes avoid the orientation correction step altogether. Depending on the thickness of the Al half-shell, it is possible to see under the optical microscope when the wire is sitting on the side (as illustrated in 3.5 c). When that is the case, a subtle purple-coloured shadow, indicating Al half-shell, is observed only on one side of the deposited wire. This "trick" is most useful when the thickness of the Al half-shell is comparable to the thickness of the wire, as then the Al is most clearly observed. When this is the case, one can try and correct the orientation right away at the micromanipulator. For very thin Al films (<10 nm), this method is not appropriate.

Practise showed that there is not a clear minimum energy orientation for the investigated pairs of wires, with one exception. Nanowires that got bent

during growth, but showed no relaxation upon being picked up, would tend to choose the orientation seen in Fig. 3.5 c). In all other cases (i.e. straight wires, slightly bent wires, flexible wires), they would randomly pick an orientation on the substrate, which might depend on the starting position when attached to the probe needle, or similar conditions. No significant difference regarding this matter has been observed between facet-to-facet and corner-to-corner type of nanowire pairs.

3.2.4 Aluminium Etching

Aluminium etching is an important and delicate device fabrication step. Poor etching can result in the lack of superconductivity in a given device. Often, it is the interface between the superconductor and semiconductor that gets destroyed as a consequence of etching process. Thus, the goal is to optimize etching and minimize the damage at the interface.

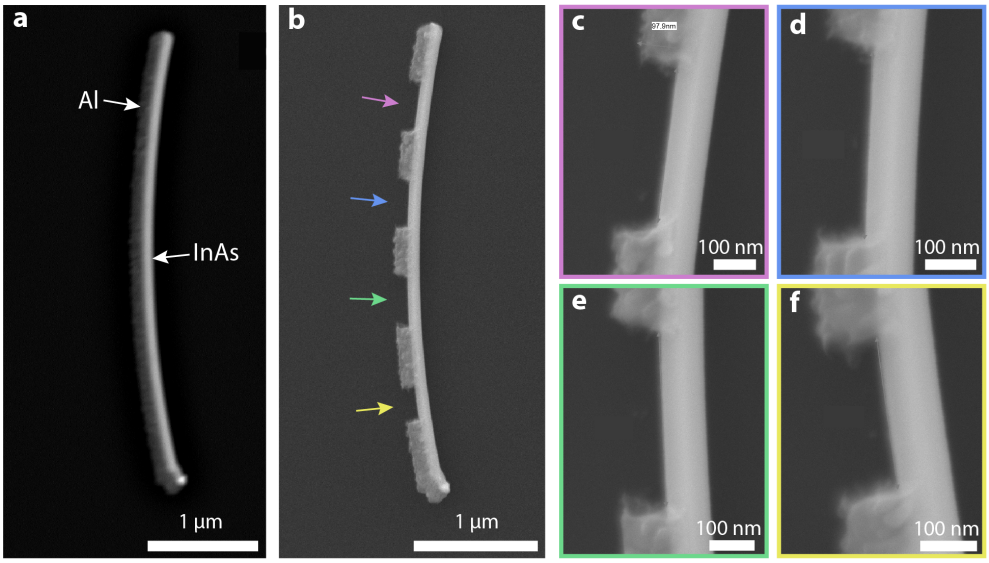

Figure 3.6: *Aluminum Etching.* **a)** SEM micrograph of a single InAs/Al DNW before etching. **b)** SEM micrograph of the same wire after etching. Arrows are pointing towards etched Al areas. The etching window was designed to be 100 nm wide. **c-f)** SEM images zoomed in on the etched nanowire regions.

To illustrate why the quality of the semiconducting-superconducting interface is vital, consider the following. In an N-S device, as investigated in this

work, only the very tip of the superconducting film, the region that is closest to the junction will play a role in transport. If the interface between the Al and InAs is poor at that very spot due to etching, then one has a very bad superconducting probe. Hence, there will not be any observable superconducting features (i.e. gap, bound states) in transport data.

The difficulty with Al etching came from the fact that Al layer is 100 nm thick. Thus, a lot of effort is put into the etching optimization for the 100 nm thick Al layer since the etching is isotropic. It means that etching is not happening in a single direction, but in multiple directions (including horizontal). Therefore, it is impossible to etch 100 nm wide window when Al layer is 100 nm thick. Aluminum etching can also be difficult to optimize because of the fact that Al oxidizes. When a growth wafer containing nanowires is taken out of the ultra-high vacuum and into the oxygen environment, a layer of native oxide (usually few nm) gets formed. The oxide is etched slower than the Al, so once the oxide is gone aluminum is quickly etched away. This process is so quick that even one second longer can lead to significant overetching. The tests are done on the single wires coming from the same growth wafer. An example of etching results with the mentioned time are shown in Fig. 3.6. Final etch time for 100 nm of Al using Transene D (highly selective etchant) was 14+1s (where +1s account fot the time that it takes to transfer the chip from the etchant to stop the reaction). Total overetching was estimated to be between 202-222 nm, which is about the minimum that can be reached.

3.2.5 Metal Deposition: Contacts and Gates

The last fabrication step is to create contacts and gates through the process of metallization. As most of the others, this step is not without its challenges. Poor lift-off or broken contacts can be the doom to the entire chip. Contacts are necessary for device biasing and measurement, while gates are needed to control a device. Gates are often understood as control nobs; the more nobs you have to turn, the more options one has while tuning a device. To fabricate contacts and gates we first expose the patterns by EBL and develop them. Then, we do the e-beam metal evaporation and lift-off. See B.2 for a detailed account.

Device Contacts

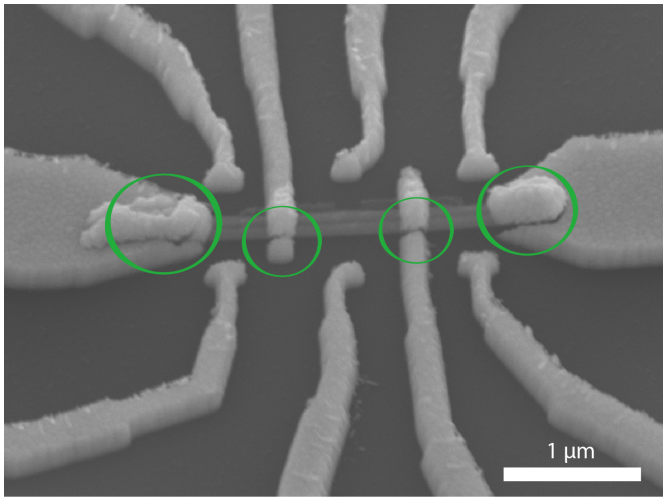

Figure 3.7: *Faulty device contacts.* An SEM image showing different examples of bad connections between the nanowire and metallic leads. Discontinuities of metallic leads are visible as gaps in encircled areas. As a consequence, it is impossible to bias the device and make measurements.

Poor quality or broken contacts were major challenges that we faced during contact fabrication. More precisely, the attempt to connect metallic leads and nanowire failed. There was a discontinuity at the interface between the metallic lead and the nanowire as shown in Fig. 3.7. It turns out that the cause of broken leads is insufficient thickness of Au that is being evaporated. Au contacts were simply not high enough to climb over the wire and withhold the tension forces and stress, without breaking. Increasing the thickness of evaporated Au to 350 nm on top off 5 nm of Ti proved to be enough to assure reliable contacts in the case of our devices. Note that 5 nm of Ti serve as a sticking layer for better adhesion and stability of Au.

Additional to this encountered issue, InAs wires oxidize when in contact with air. Hence, a layer of native oxide needs to removed before placing contacts. This oxide layer causes a barrier between InAs wire and deposited Ti/Au contact, preventing the formation of Ohmic contact. Instead, a kind of tunnel junction forms - an interface not suitable for making source and drain. RF milling is used to circumvent this problem. Metal evaporation chamber,

featuring ultra high vacuum, is equipped with an argon milling system so that undesired oxide layer can be removed immediately prior to the metal deposition.

Side and Top Gates

Studied devices were made with two types of gates: side gates and top gates. Side gates are typically fabricated ~200 nm from the wires and their effective gate area is ~100 nm. Figure 3.8 shows few examples of side gates. Although they offer a great starting point, top gates come with certain advantages. First, there is the question of numbers. Having only one side gate per dot (plunger gate) often means that one can tune the levels of each dot, but not so much their coupling to the leads (at least not independently). Switching to top gates resulted in more gates per dot available for tuning, making it possible to better control the coupling between the dots and the leads. Further, it has been observed that top gates are more effective than side gates. These are the reasons why we ultimately resorted to utilizing top gates.

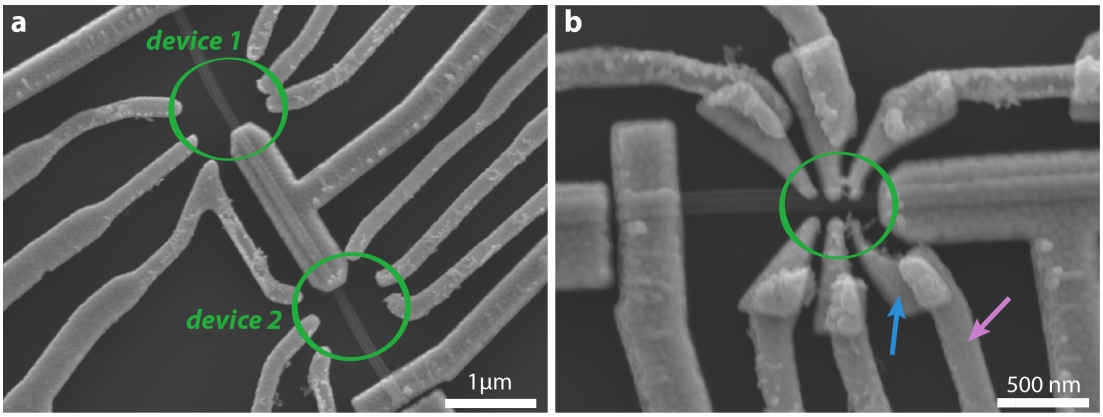

Figure 3.8: *Top gates.* **a)** An SEM image of two parallel QD devices, with partially fabricated gates. Encircled areas are indicating where top gates are partially missing. **b)** An SEM image of the device number 2 after patching the top gates. Fine features are present and encircled. Blue arrow is pointing to an original part of top gates, also visible in a). Green arrow is indicating a patch made subsequently to complete that top gate.

While side gates are fairly easy to fabricate, top gates fabrication is more

challenging. Full step-by-step recipe for both types can be found in Appendix B.2. Fabricating top gates includes a deposition of oxide layer (HfO_2 in our case) to ensure that nanowire and top gates are capacitively coupled. First fabrication trial resulted in top gates being incomplete. After lift-off, the finest features (designed width of 60 nm) were missing from all of devices. The example of this is shown in Fig.3.8 a).

After careful analysis and consideration, three fabrication adjustments were made to circumvent this obstacle. First, it was made sure that the right parameters for proximity effect correction (PEC) were chosen during the creation of design files ("Si substrate, 100V system, 400 nm PMMA"). It was speculated that picking a wrong PMMA height setting could have played a role in top gates fabrication issues. Next, O_2 plasma ashing time got increased from 30 to 45 seconds to make sure that all resist leftovers after development are removed. Resist leftovers, which would end up under the evaporated metal, could have lifted the fine features during lift-off step. Lastly, we increased the area dose for e-beam exposure from 900 to 1000 C/cm^2. Ultimately, 5 nm of Ti + 180 nm of Au were deposited during the top gates patching to ensure that new gate parts can climb the originally deposited 150 nm parts, as shown in Fig. 3.8 b). Top gates lifted off properly after making these changes.

3.2.6 Nanowire Clamping

Device fabrication using nanowires from QDev 872 batch (see sec. 3.1 for details) was only partially successful because a number of nanowires went missing from the chip during the processing. Having in mind how intricate and time consuming the nanowire transfer is (see sec. 3.2.3), losing wires was far from acceptable/optimal. To prevent nanowires from flying off the chip we resorted to clamping. It simply means that nanowires had to be fixed to the chip substrate by evaporating small metal patches at their ends. Results of clamping are shown in Fig. 3.9 where metal clamps are encircled in green. Introducing clamping as the first fabrication step added one more lithography to the process which in turn increased the total fabrication time. Detailed fabrication protocol can be found in Appendix B.2. Clamping nanowires at both ends or just at one

end showed no difference.

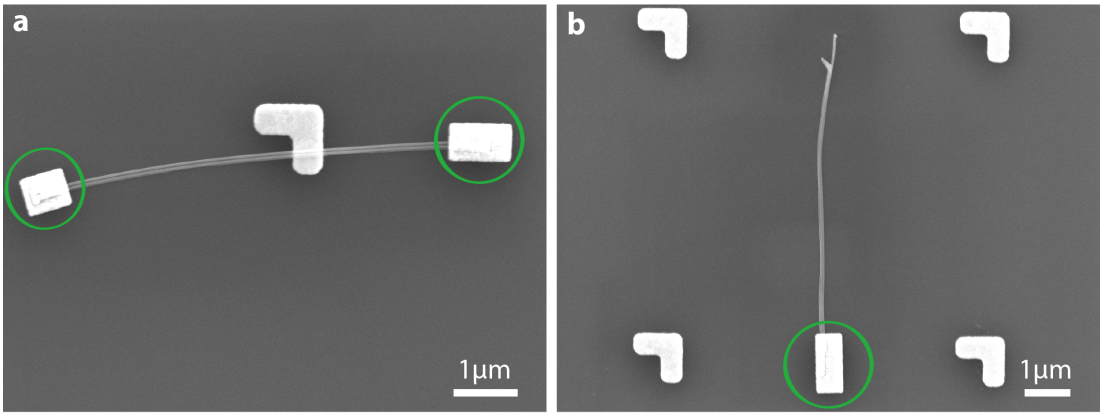

Figure 3.9: *Nanowire Clamping.* SEM images showing nanowire pairs clamped on both ends in **a)** and on one end in **b)**.

The exact reason for wires moving from the chip remained largely unknown. However, it was established that the wires detached from the substrate after the etching was done and the excess resist stripped off. It could only be speculated that after Al was etched some nanowires were left with very little contact area between them and the substrate, making it easier for them to be stripped away or moved around. There is a possibility that the observed issue was a random occurrence, but we decided not to take any unnecessary risks and clamped down the NW on the next set of devices. It is important to note that the issue of wires detaching from substrate or moving around was not encountered when fabricating with nanowires from other batches listed in Table 3.1. Nanowires from QDev 903 were clamped for the first set of devices, but it was discovered shortly after that it was not necessary.

3.3 MEASUREMENT SETUP

Two types of measurement circuits/techniques were used to acquire the data. Four-terminal measurement was used for Little-Parks experiment (discussed in Chapter 6), where sample resistance is expected to be low and it is preferred to current bias the device. On the other side, two-terminal measurement was used to measure hybrid devices involving quantum dots (discussed in Chapters 4

and 5) where voltage bias is more suitable due to the larger resistances of the sample. The advantage of having a 4-terminal measurement is that voltage drop across the sample is measured directly, without the need to subtract the contribution coming from the resistance in the measurement lines. This line contribution has to be considered in the case of 2-terminal measurement.

Two-terminal measurement setup

The setup for voltage biased 2-terminal measurement is shown in Fig. 3.10 b). Here, instead of applying I_{SD} we are applying V_{SD} to the source contact. The applied signal is a combination of AC component sourced from the lock-in 1 (0.02 V, excitation frequency of ~77 Hz) and DC component sourced from a DAC. Both signals are passed through a voltage divider (division factor 1:10^4 for AC and 1:10^3 for DC signal) and combined to have the final AC excitation of 2μV (smaller than k_BT). This combined signal passes through the breakout-box and gets applied at the source electrode. The signal on the other end of the device (drain electrode) is passed through a current amplifier and into a lock-in 2 to measure AC current as well as DMM to measure DC current. In 2-terminal measurement line resistance R_{line} (mostly coming from the filter) has to be considered and subtracted from the measured values. Differential conductance $\frac{dI}{dV}$ is found by the measured AC current divided by the AC voltage excitation at the sample. DC voltage applied at every gate is supplied by a 16bit DAC with a resolution of 300 μV. The aim is always to have the resolution as large as possible for the purposes of fine-tuning quantum dots.

Four-terminal measurement setup

Figure 3.10 a) shows a circuit schematic for 4-terminal measurement where the sample is current biased. Upon loading, the sample is connected to the breakout-box via measurement lines. To reduce the high-frequency noise, measurement lines are equipped with a set of low-pass RC filters and have a series resistance of R_{line} = 4.12 kΩ. The signal applied at the source contact is created by sourcing 0.1 V (with excitation frequency of ~68.08 Hz) from the lock-in amplifier (AC

component) and combining it with a DC voltage component sourced from a digital-to-analog converter (DAC). Both AC and DC signals pass through voltage dividers (DC: $\times 10^{-1}$, AC: $\times 10^{-3}$) and finally, to apply current bias I_{SD}, the signal is connected in series with a large (1 MΩ) resistor giving the value of 0.1 nA for AC current component [double check this]. On the other end, the current transferred through the device passes through the drain contact and into a low noise current-to-voltage converted where signal gets amplified by 10^6 V/A. Amplification of the signal helps to distinguish originally very faint signal from the noise. Next, the signal arrives to the lock-in 3 where it gets multiplied by the reference frequency provided by the lock-in 1. This signal multiplication and filtering results in the removal of all signals with frequencies that do not match the reference, leaving us with the filtered AC signal component. A digital multimeter (DMM) was used to measure the DC component. The two inner contacts measure the voltage drop across the device. This is done by first amplifying the signal (gain of x100) and then measuring the resulting AC component by lock-in 2 and DC component by DMM. The two BNC cables coming from the breakout-box into the voltage amplifier are wrapped around each other to cancel any magnetic fields. The differential resistance $\frac{dV}{dI}$ is found by the measured AC voltage divided by the applied current, given by the bias resistor and lock-in excitation.

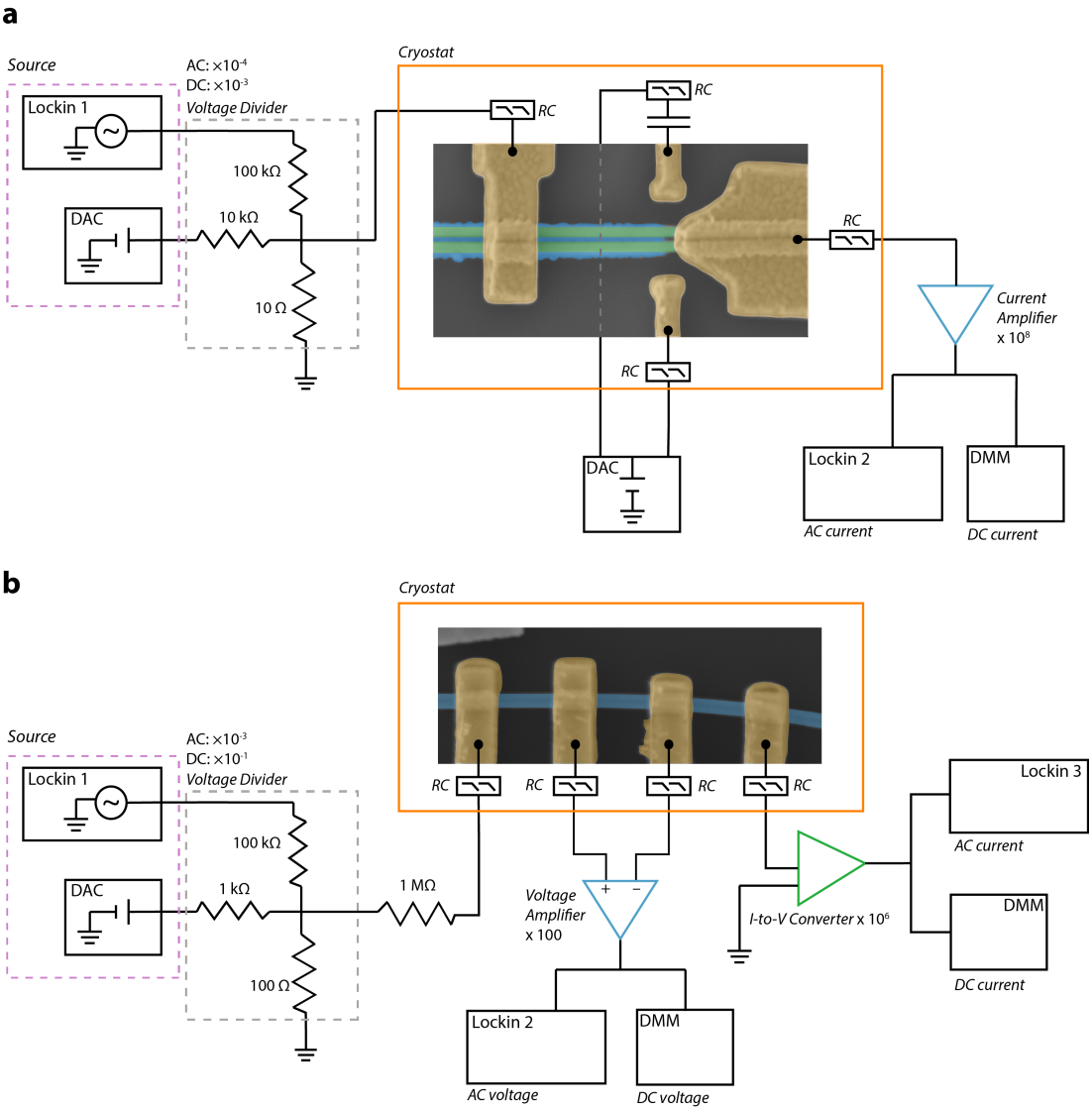

Figure 3.10: *Measurement setups.* **a)** Circuit schematic of 2-terminal measurement. The model of current amplifier is LSK389A Physics Basel. The capacitivly coupled gates are controlled by a 16bit DAC. **b)** Circuit schematic of 4-terminal measurement. This setup is used for measuring the differential resistance of Al shell. AC signal sourced from lock-in 1 amplifier (model SE830 Stanford Research Systems) is mixed with DC signal sourced from DAC (16bit) and applied to the source lead. Lock-in 2, together with DMM (Agilent 34401A), is measuring amplified voltage drop across the device. Lock-in 3 and another DMM are measuring the current at the drain lead.

4 PARALLEL DOUBLE QUANTUM DOTS: FORMATION AND TUNABILITY

Provided with such an exiting heterostructure where nanowires are arranged in parallel and coupled by epitaxial superconductor, it is only natural to start by exploring devices where quantum dots are in parallel configuration. Parallel QDs in nanowires have been investigated before, but in slightly different platforms. In 2017 and 2018, Baba et al.[46][8] reported gate tunable parallel QDs in systems where two individual InAs NWs (no Al shell/half-shell) are transferred and placed parallel to each other on the substrate. Aluminum is therefore deposited later during the fabrication process. Also, parallel quantum dots defined by the combination of crystal-phase engineering and gating were investigated in single InAs nanowires [47].

To examine the suitability of this novel heterostructure for hybrid quantum dot experiments, it was first necessary to verify that a parallel quantum dots (pDQD) system can be formed in this platform and demonstrate the independent control and tunability of those quantum dots. The expectation was to see two well defined QDs with $U \sim \Delta E$, which would enable shell-filling and the observation of even/odd occupancy pattern as the number of electrons on the dots changes. Additional expectations included the observation of induced superconductivity, as well as tunnel coupling between the dots.

This chapter reports the first realization of parallel double quantum dot system in double nanowire platform with in-situ grown Al half-shell. The work discussed throughout this chapter provided invaluable insights that served as stepping stones on the path of optimizing the given nanowire platform for

future/subsequent transport experiments.

My personal contribution to the work presented here was device fabrication, as described in the previous chapter. As a member of three people team, I handled the sample loading and performed the transport measurements.

4.1 DEVICE OF INTEREST

Scanning electron micrograph of the studied device in Fig. 4.1 a) reveals the N-pDQD-S device geometry. The nanowires used to fabricate this device came from QDev 822 nanowire batch. Their diameter is between 80-105 nm and they feature 100 nm of in-situ grown Al half-shell. The fabrication steps are described in Chapter 3, while the detailed fabrication recipe is located Appendix B.

The nanowire pair (green colour) is oriented such that Al half-shell (blue colour) is facing the substrate, as illustrated in Fig. 4.1 b). Two quantum dots parallel to each other are formed in the etched section of the wires, seen between the two contact leads (i.e. the upper AuTi lead and less visible Al on the NW) in Fig. 4.1 a). The length of the etched wire section is L$\approx$ 380 nm. QDs are tunnel coupled to the common leads, as well as mutually coupled to each other due to being in close proximity. Figure 4.1 c) shows the system at hand (rotated by 90° counterclockwise compared to the SEM image) and the couplings involved. In the etched area, nanowires are physically separated and native oxide is formed upon completion of Al etching. Two plunger gates (g_1 and g_2) are capacitively coupled to quantum dots, one gate per each dot. Gates are introduced in order to establish a degree of control over the device. Their role is to shift (tune) the energy levels of the dots and pinch-off nanowires. By applying high enough negative voltage to one gate, it is possible in principle to pinch-off the corresponding wire and have transport occur only through the other one. Side gates like these are typically fabricated at about 200 nm from the nanowires. Additionally, this sample incorporates a global back gate which is capable to simultaneously tune the energy levels on the QDs as well as the strength of tunnel couplings (by lowering or increasing the tunnel barriers). The back gate can be effectively used to tune the system into different working regimes

by controlling the charge carrier density and coupling strength of QDs to the leads. Although it was designed to be N-pDQD-S type of device, measurements revealed transport signatures that are consistent with N-pDQD-N device type. The intended superconducting lead behaved as a normal lead.

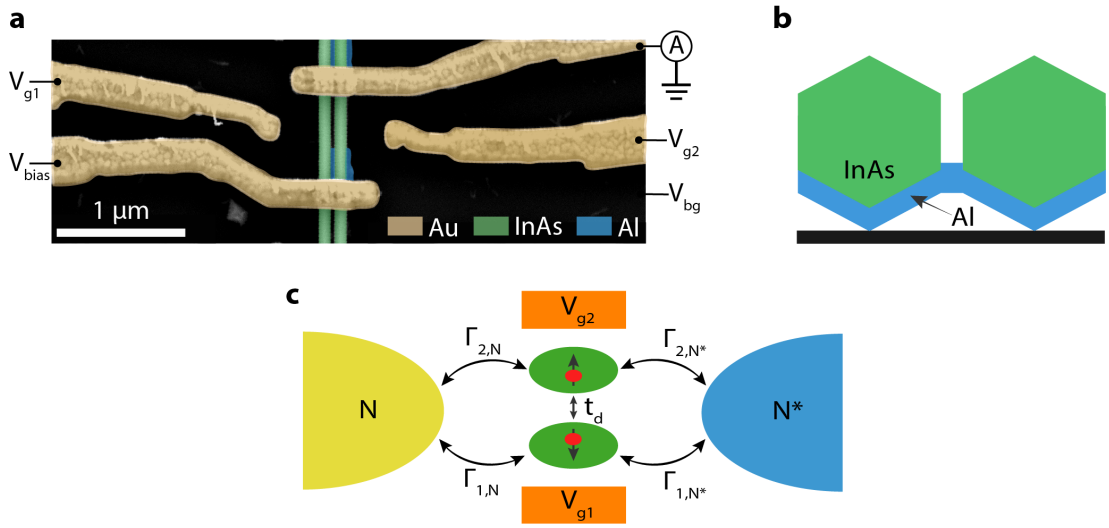

Figure 4.1: *Device of interest.* **a)** Scanning electron micrograph of the measured device. The image is false coloured for easier interpretation. Device sits on a substrate consisting of highly doped Si, topped with a layer of SiO_2. Bare nanowire segment where QDs are formed is approximately 380 nm long. It features two spatially confined parallel quantum dots, two common contacts and two plunger gates (one per each QD). The backgate is also connected and available for device tuning. **b)** Illustration of axial cross section of the nanowire pair. It indicates the position of the 100 nm thick epitaxial Al half-shell (blue) in respect to the chip substrate (gray). Nanowires are in so called facet-to-facet orientation in respect to each other. **c)** Schematics of two quantum dots in parallel with common source and drain contacts. Tunnel couplings of QDs to both leads are shown, as well as inter-dot coupling. Energy levels on QDs are tuned by applying the voltage on plunger gates V_{g1} and V_{g2}. N* indicates the metallic lead that was designed to be superconducting, but behaived as a normal contact.

4.2 UNDERSTANDING THE DEVICE

To verify that two parallel quantum dots are indeed formed, one should investigate the charge stability diagram of the device. Figure 4.2 a) shows a measurement of linear conductance in the plane of two plunger gates V_{g1} and

V_{g2}, for the device showed in Fig. 4.1. The hexagonal regions with stable charge in the parameter plane are enclosed by conductance lines, as schematically shown in in Fig. 4.2 b). There are two sets of conductance resonances, each having a characteristic negative slope. The fact that there are only two characteristic slopes indicates that there are only two quantum dots in this system. Finite slope values suggest that there is a cross-capacitance between the gates and QDs, as expected in case of capacitively coupled QDs. Otherwise, if the dots were decoupled, one would observe sets of parallel and vertical charge degeneracy lines.[19] Following from the diagram in Fig. 4.2 a), voltage on gate 1 mainly affects QD1, while voltage on gate 2 mainly affects QD2. Hence, there are two tunable quantum dots in this system but they are not fully independently controllable due to the mutual capacitive coupling of the two dots, as expected.

Figures 4.2 c) and d) show high bias spectroscopy measurements for QD1 and QD2 along dashed lines marked in Fig. 4.2 a), respectively. These measurements reveal Coulomb diamonds pattern, including excited state lines, for both quantum dots. This suggests that the system is tuned into the Coulomb blockade regime. Differential conductance is going to zero within Coulomb diamonds, while it takes a finite value outside the diamonds. Note that QDs in this system, defined/confined by the tunnel barriers and the inherent NW potential landscape. Compared to the state of the art QDs which are very well defined by the means of the crystal phase engineering[23][47][48], it seems that the quality of investigated QDs is not on the highest level.

Characteristic energy scales, like addition energy E_{add} and single-particle level spacing ΔE, can be directly extracted from bias spectroscopy measurements. The height of the diamond from the zero applied source-drain voltage provides the value for addition energy $E_{add(1,2)}$, while the distance from the zero bias line to the excited state line gives $\Delta E_{1,2}$. Addition energy E_{add} is just the sum of charging energy U and level spacing ΔE, where charging energy often dominates. If QD has odd occupation, E_{add} equals U since additional electron is placed on the same energy level. For QD with even occupation, the cost of adding extra electron E_{add} increases to $U + \Delta E$, as that additional electron has

to go to the next available energy level.

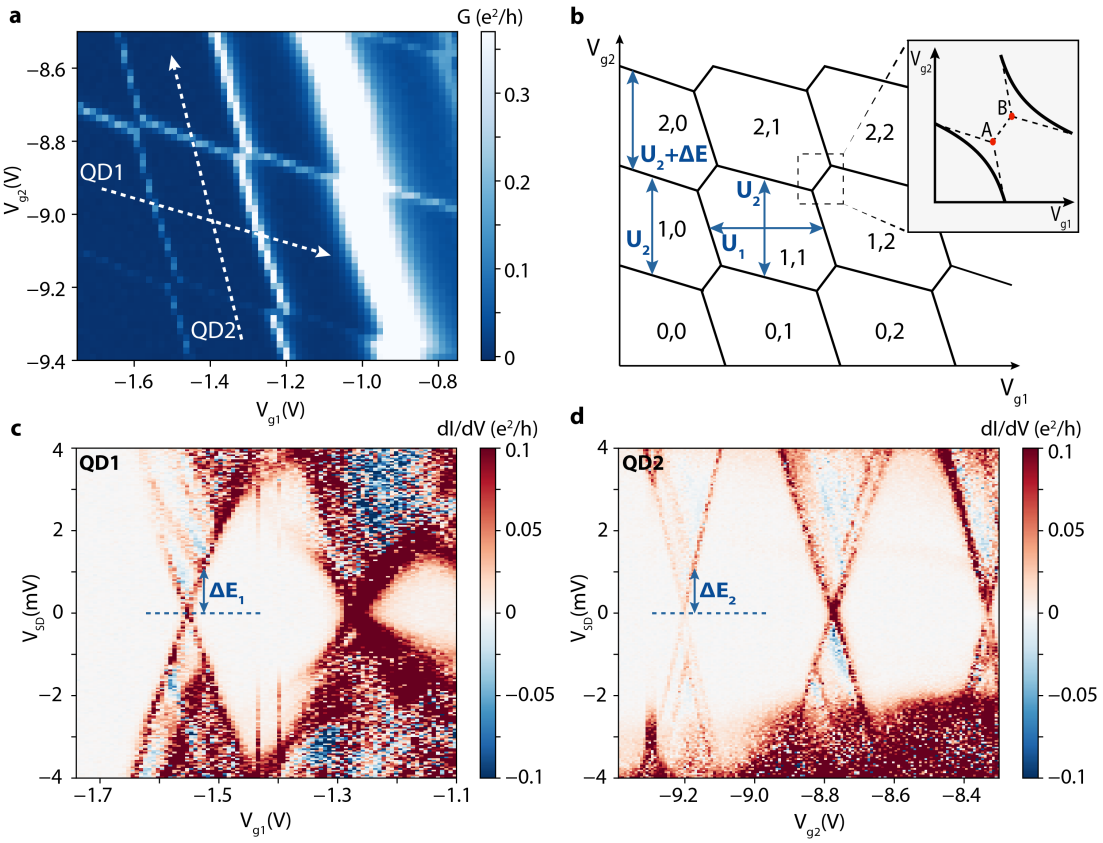

Figure 4.2: *Charge stability diagram and bias spectroscopy.* **a)** Plot of linear (zero bias) conductance taken at the backgate value of V_{bg}=-9.84V. The x and y axis show the modulation of two plunger gates. White arrowhead lines show the cut directions for bias spectroscopy corresponding to (seen in) panels c and d. **b)** Schematic representation of honeycomb pattern for double quantum dot system with no inter-dot tunnel coupling. Arrows show a set of characteristic energy scales in the system. Pairs of numbers n,m=0,1,2 show the occupancy of QD1 and QD2. Inset zooms in to degeneracy lines near a pair of triple points, indicated by red dots. Dotted lines represent the case when QDs are only capacitively coupled, while features indicated by full lines appear when there is some degree of inter-dot tunnel coupling, in addition to electrostatic coupling. **c)** Bias spectroscopy of QD1 revealing Coulomb diamonds. The height of the diamond corresponds to the addition energy E_{add} of the dot. Within the diamond, QD is in the Coulomb blockade. There are lines corresponding to excited states within the area where the current is allowed to flow. The lever arm parameter is found to be $\alpha_1 \approx 0.02$. **d)** Bias spectroscopy of QD2. The lever arm parameter is found to be $\alpha_2 \approx 0.08$

From the set of data presented in Fig. 4.2 c) and d) it is found that $E_{add,1} \approx$ 5.5 meV and $\Delta E_1 \approx 1.2$ meV for QD1, while $E_{add,2} \approx 6.5$ meV and $\Delta E_2 \approx 1.1$ meV for QD2. These values are valid only for specific Coulomb diamonds (charge stable sectors) that are being examined. Knowing the aspect ratio of diamonds (addition energies and distance between adjacent Coulomb peaks at zero bias) makes it possible to calculate the lever arms for both QDs. Lever arm is a factor relating the plunger gate voltage to the applied bias. For QD1, it is found that $\alpha_1 \approx 0.019$, while for QD2 $\alpha_2 \approx 0.015$. For convenience, results are summarized in Table 5.1. These results indicate that U and ΔE are on the same order of magnitude, which in turn suggest that features corresponding to shell filling should be observable.[49] However, the plots in Fig. 4.2 offer no clear evidence of shell structure (that could back up the single-level transport simplification in this pDQD system. In turn, the investigated pDQD system cannot be simplified to two parallel single levels.[double check Ihn p349] Based on the small difference in values for addition energy and level spacing for two QDs, it can be argued that the dots are of similar size.

	E_{add} [meV]	ΔE [meV]	α	U_d [meV]
QD1	5.5±0.2	1.1±0.1	0.019±0.001	1.1±0.1
QD2	6.5±0.1	1.1±0.2	0.015±0.0002	

Table 4.1: *Characteristic energy scales for parallel DQD system.* This summary comprises of values for addition energies, exited state (single-particle) level spacing and lever arm extracted from bias spectroscopy data. In addition, inter-dot charging energy is also included. Uncertainties are estimated graphically for all measured values. Rules of error propagation are used to estimate error on α.

Charge stability diagram in Fig. 4.2 a) reveals a curious development of resonance peaks. Even though QDs have common source and drain leads, their tunnel couplings do not appear to behave the same (within the given gate ranges). Conductance lines of QD1 are increasing in intensity and broadness for more positive values of gate 1. On the other hand, the broadness of the peaks of QD2, although not entirely constant, does not exhibit such a dramatic change within the given gate range. Broadening of the conductance peaks can

be attributed to three main causes: T, Γ and V_{AC} (applied AC excitation)[48]. It is unlikely that temperature would change so much during one measurement in order to cause this change in peak broadness. Width limit of the line shape that can be extracted is determined by V_{AC} and it should be set so that $eV_{AC} \ll k_BT$, Γ (2μV in our case). To better understand the main cause of the peak broadening, a short analysis is done and the results are in Appendix A.2. It turns out that $k_BT \ll E_{FWHM}$ (for $T = T_{base} = 30mK$, where E_{FWHM} is extracted from the full-width half maximum (FWHM) of a peak. From here we conclude that device is in the regime where tunnel coupling is the dominant factor in peak broadening ($k_BT \ll \Gamma$), making thermal broadening insignificant. In this limit, $E_{FWHM} = \Gamma$ [48]. By increasing the plunger gate voltage as in Fig. 4.2 a), the strength of total tunnel coupling to the leads, given by $\Gamma_i = \Gamma_{i,N} + \Gamma_{i,N^*}$ (i=1,2), gets larger and peaks consequently get broader.

From the details of device geometry described in Section 4.1, an approximation that t_d=0 can be made. Upon closer inspection, the charge stability diagram in Fig.4.2 a) shows the kinks created by parity change (conduction) lines. A zoom in to one set of those kinks is seen in Fig. 4.3 a). Based on their apparent shape (sharp, cornered kinks) it can be deduced that the two dots are electrostatically coupled, with no or very weak probability for interdot tunnel coupling.[19] The consequence of interdot capacitance is discrete shift of the energy spectrum of QD1 when additional electron is added to QD2 (and vice versa).[25] If t_d was not negligible, the observed sharp kinks would become rounded and the triple point separation would increase to reflect the strength of tunnel coupling. The inset in Fig.4.2 b) illustrates this situation. Hence, the approximation for t_d holds, meaning that QDs do not form a "quantum dot molecule", electrons are localized on separate QDs, and charge states of two dots are degenerate at the vicinity of triple point.[19],[25]

The distance between the two triple points reflects the sum of interdot charging energy U_d and tunnel coupling $2t_d$, for zero detuning[25]. This energy measures the amount of conductance peak splitting that results from the mutual interdot coupling[50]. Bias spectroscopy measurements across the two triple points can be used to extract the value for U_d, as interdot tunnel coupling can

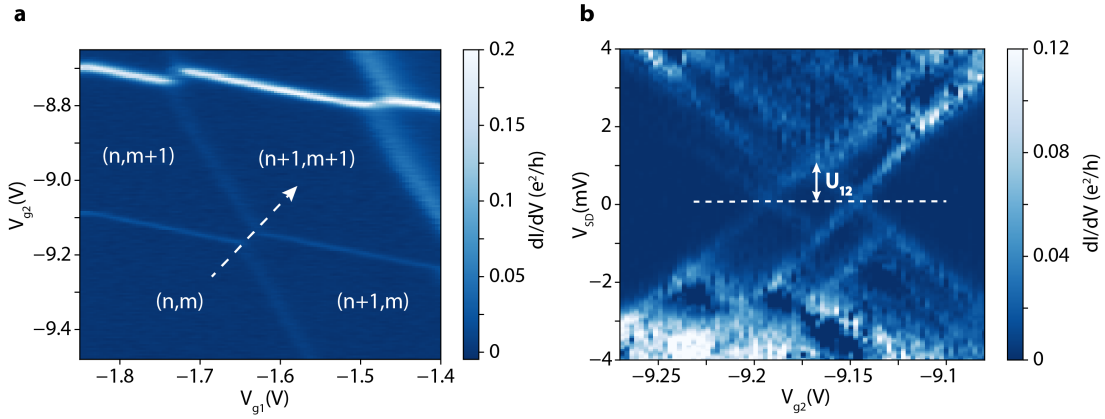

Figure 4.3: *Triple point (cut) bias spectroscopy.* **a)** Charge stability diagram, zoomed in on one pair of triple points. Around triple points, conduction lines make kinks. Dashed line is showing the direction along which a cut for bias spectroscopy is made. Integers (n,m) represent arbitrary charge states of QD1 and QD2, respectively. **b)** Bias spectroscopy measured across the dashed line in a). The height of the resulting diamond, indicated by white arrow, gives the capacitive coupling energy $U_{1,2}$ between the two QDs.

be neglected in this system. In this case, U_d determines the distance between the two triple points. Figure 4.3 shows the results of such measurement. The height of the diamond in Fig. 4.3 b) yields the interdot charging energy to be $U_d \approx$1.2 meV. The value of U_d is on the same order of magnitude as the energy scales investigated earlier, E_{add} and ΔE.

What happened with superconductivity?

As to why the superconductivity was not observed in this device, there is no definite explanation. It it most likely a combination of factors that are rooted in poor Al etching, such as: reduced superconductor quality and insufficient semiconductor-superconductor interface (contact) area. Both troubling factors stem from a common source, overetching of superconductor. First, overetching left the nanowires with less superconductor on them than intended (<500 nm), thus reducing the chances for inducing the superconductivity in nanowires due to reverse proximity effect. Second, it is speculated that overetching degrades the interface between superconductor and semiconductor, further deteriorating

(minimizing) the chances of proximitizing the nanowire.

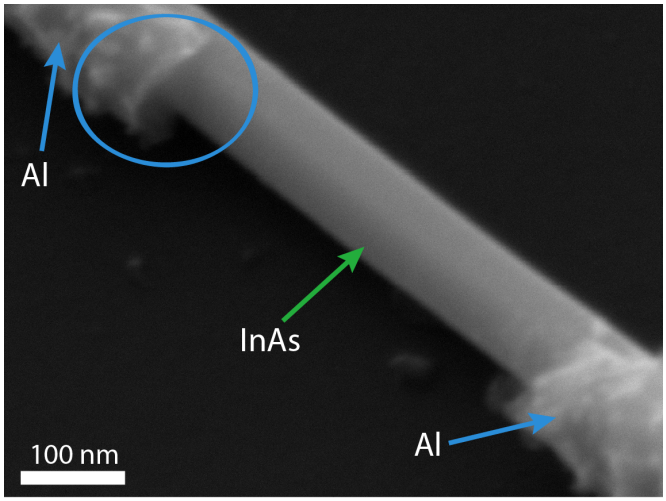

Figure 4.4: *Post-etching SEM images.* **a)** The image is showing an etched section of a nanowire. Leftover Al layer can be seen at the each wire corner, as indicated with blue arrows. Encircled portion of the wire shows a distinct tunnel-like structure (hollow shell) in Al layer that is created during etching process.

Figure 4.4 shows just how unanticipated etching results can be. The resulting etch profile seen in SEM image resembles a hollow Al shell, where Al layer moves further away in respect to the shell entrance. The problem with tunnel-like etch profile is twofold and in line with the factors mentioned above. Semiconductor-superconductor interface is non-ideal, making it hard to obtain a good superconducting probe. Further, tunnel-like structure, which is simply a hollow Al shell, can be quite deceiving as it conceals the fact that superconductor is actually etched away inside it. Hence, the contact area between the two materials is reduced, even though it might not appear so after doing a rapid SEM imaging. This misleads the observer to believe that there is a larger contact area between superconductor and semiconductor than there actually is.

With potentially damaged interface and insufficient superconductor left, it gets hard to proximitize the nanowire and superconductivity is unlikely to be observed.

4.3 CONCLUSION

In summary, we successfully demonstrated gate tunable parallel quantum dots in a pair of InAs nanowires with in-situ deposited Al half-shell. However, there was no evidence of shell-filling nor superconductivity. The size of QDs should be decreased by larger confinement (e.g. decrease the nanowire diameter) to improve the chances of observing shell-filling. For superconductivity, special attention needs to be payed to the etching in terms of optimizing the etching time for the given superconducting layer height.

Measurements revealed that in the case of physically separated wires (plus the native oxide), tunnel coupling between the dots t_d is negligible. This is not an ideal scenario if one would like to study phenomena that require non-zero tunnel coupling (e.g. YSR spin screening in parallel QDs). However, no interdot tunnel coupling scenario could be beneficial in case that these wires are used in island geometry to investigate Topological Kondo Effect[10].

5 PARALLEL DOUBLE QUANTUM DOTS: SUPERCONDUCTIVITY

Having demonstrated that parallel quantum dot system can be formed and controlled in the given double nanowire platform, the next step was to achieve and investigate proximitized superconductivity. Superconductor-semiconductor hybrids are an important platform for the investigation of exciting phenomena, such as Majorana bound states [1], [2], Yu-Shiba-Rusinov bound states [3], [4], topological superconductivity [6], Little-Parks effect [7]. Parallel nanowire hybrids, such as those used in this thesis, are ideal platform for exciting theoretical proposals such as topological Kondo effect [10], Andreev molecule [12], and parafermions [11].

The work presented here represents the first step towards those experiments. Thus, it was necessary to better understand this platform and to optimize it for the future investigations. The first objective was to confirm the presence of the induced superconducting gap Δ^* and estimate its nature and value. Ideally, we would expect to see a hard gap, similar to that reported by Chang et al. in 2015 [14]. Additionally, we looked for the signatures of sub-gap states.

My personal contribution to the work presented here was to fabricate devices. Furthermore, I was a member of three people team that handled the sample loading and performed the transport measurements.

5.1 DEVICE OF INTEREST: N-PDQD-S GEOMETRY

Figure 5.1 a) shows a false coloured micrograph of the investigated N-pDQD-S device. The device features common normal (right yellow) and superconduct-

ing (left blue) leads and a global bottom gate (capable of tuning the levels on the QDs and the strength of tunnel couplings at the same time). Two parallel QDs are formed in the ≈ 110 nm long etched section of the nanowire pair, where Al is removed. The etched NW section here is much smaller compared to the device discussed in Chapter 4 where it measured about 380 nm. The electrochemical levels of QDs are electrostatically tuned by applying the voltages, V_{g1} and V_{g2}, at the plunger (side) gates. This device was fabricated using the nanowires from QDev 872 batch, featuring 100 nm of epitaxial Al half-shell (covering 3 facets of each NW). Fabrication steps and recipes are laid out in Chapter 3 and Appendix B, respectively. Figure 5.1 b) illustrates a variety of couplings that play a role in the given N-pDQD-S system. Besides the fact that each QD is tunnel coupled to the N and S contacts, they are also mutually coupled to one another. However, NWs in this device are physically separated which allowed for the native oxide to get formed between them. Due to this geometry restriction, the inter dot tunnel coupling is predicted to be effectively zero, as was the case for device presented in Chapter 4. Nevertheless, the two QDs are still expected to be capacitively coupled.

5.2 UNDERSTANDING THE DEVICE

Figure 5.1 c) shows the linear conductance G measured as a function of two plunger gate voltages V_{g1} and V_{g2}. This plot is also known as a charge stability diagram, a common tool in characterising QD systems. Two sets of conductance resonances indicate that there are two QDs in the system, as intended. In a system like this, the exact location of the quantum dots cannot be known as they they tend to get formed around some lattice defects. Hence, they are not necessarily perfectly parallel to each other. However, it is clear from Fig. 5.1 c) that plunger gates affect the QDs well as they can change the charge state of their respective QD. This suggests that both QDs are most likely situated between the contacts and not under them. Else, the metal contact would screen the plunger gate and there would be no observable effect as the voltage on the gate changes.

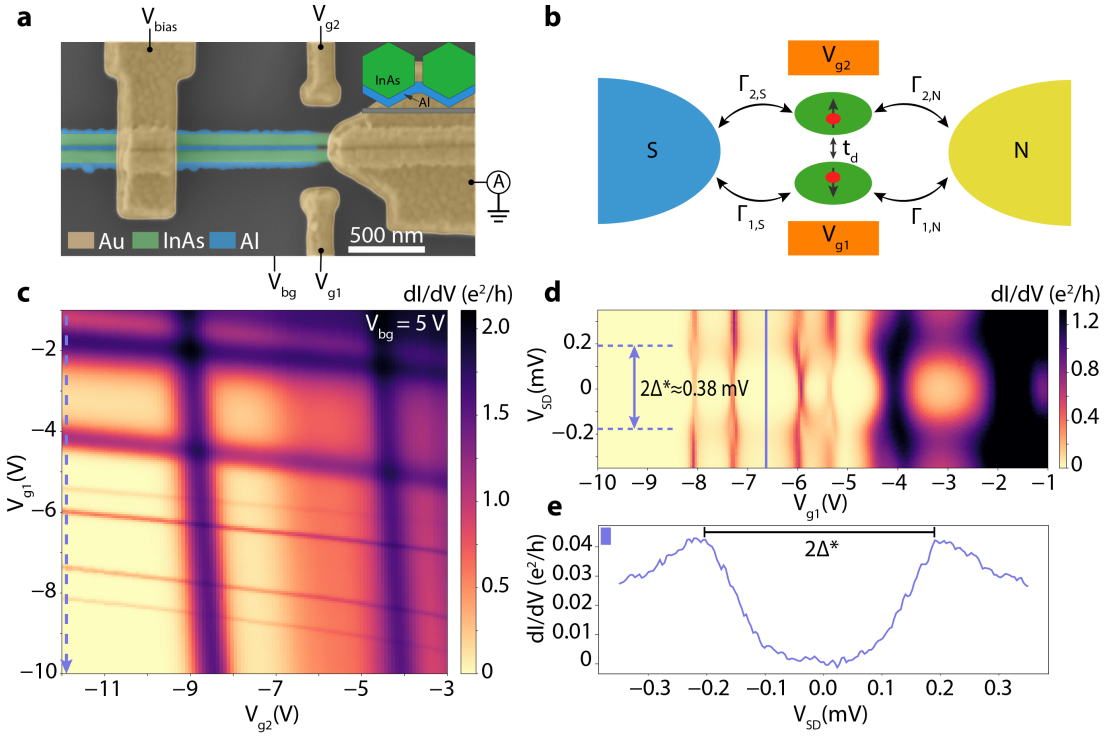

Figure 5.1: *Device of interest.* **a)** False coulloured scanning electron micrograph of N-pDQD-S device. Device sits on a Si++/SiO_2 substrate with Al half-shell pointing towards the substrate. Two QDs are confined in the etched segments of nanowires, measuring approximately 110 nm. The device includes two plunger gates (one per each QD), common normal and superconducting contacts, as well as a global backgate. Inset shows that Al half-shell is pointing towards the substrate. **b)** Illustration of tunnel couplings in parallel quantum dot system with common leads. Γ_d represents inter dot tunnel coupling, while $\Gamma_{1(2),N(S)}$ stands for tunnel coupling between the QDs and normal/superconducting leads. V_{g1} and V_{g2} tune the electrochemical potential of the QD1 and QD2, respectively. **c)** Examplary charge stability diagram of the studied device. Data was measured at the backgate V_{bg}= 5 V. Purple arrowhead line at the very left shows the direction along which a bias spectroscopy cut for QD1, seen in panel d, was taken. **d)** Differential conductance measured as a function of source-drain bias V_{SD} and gate 1 V_{g1}. The plot reveals the existence of the induced superconducting gap and indicates the signatures of potential sub-gap bound states. The value of the induced gap is estimated to be $\Delta^* \approx 0.19$ meV. **e)** Line cut taken at V_{g1} as indicated by solid purple line the panel d. The soft nature of the effective superconducting gap is revealed.

An observation from Fig. 5.1 c) that stands out is that conductance peaks of QD2 are much broader than the ones related to QD1, for about the same range of V_{g1} and V_{g2}. This broadening can happen when the dot is strongly coupled to the normal lead. Since we cannot individually control the couplings to normal and superconducting lead $\Gamma_{1(2),N(S)}$, one can assume that perhaps QD2 is positioned closer to the normal lead, compared to QD1.

Upon further examining the plot in Fig. 5.1 c) it appears that the conductance lines of the two QDs cross in a way that forms square instead of hexagonal shapes of the charge stable regions. The expected honeycomb pattern of the charge stability diagram is not observed in Fig. 5.1 c) and consequently the triple point region (where vertices of the square domains split and possibly curve due to the interdot coupling) is neither. This impedes any attempts to determine the nature of the interdot coupling. The lack of clear hexagonal charge stable domains and the fact that there are no observable discontinuities in conductance lines at the crossing points suggest that the two QDs in this system are fairly decoupled [19], [25]. Even for the thinnest resonance line in QD2, no shift is observed upon adding an electron in QD1 indicating a small U_{12}. However, geometry of the device (see Fig. 5.1 a), mainly the small distance between the wires, would suggest that the wires are capacitively coupled (in which case the square vertices would split into two triple points). Alternatively, not seeing triple points could be a resolution problem where the line width is dominating over the mutual charging U_{12} and tunnel coupling t_d, making it impossible to examine them.

Low bias spectroscopy cut of QD1 is shown in Fig. 5.1 d). There are two new features to consider on this plot. First, suppression of conductance in the regions around V_{SD}= 0V provides the evidence of the induced superconducting gap Δ^*. This suppression of conductance and the size of the gap are seen in the line cut shown in Fig. 5.1 e). The magnitude of the induced gap of $\Delta^* \approx$ 0.19 meV is found by taking the half of the peak-to-peak distance in Fig. 5.1 e). This gap value is consistent with the one reported for the similar InAs/Al heterostructure in Ref.[14]. From the BCS ratio $T_c=\Delta^*_{Al}/1.764k_B$ it follows that $T_c \approx 1.2$ K. Often the quality or hardness of the gap is characterized by the ratio

$G_{V_{SD}>\Delta^*}/G_{V_{SD}=0}$, where $G_{V_{SD}>\Delta^*}$ is the out-of-gap conductance and $G_{V_{SD}} = 0$ is the zero-bias conductance [14]. In this case it is found that the subgap conductance is suppressed by a factor of 136.

Second thing to notice on Fig. 5.1 d) is the increase in feature broadness as V_{g1} gets more positive. This is attributed to the increase in tunnel coupling between the QD and the leads. Device geometry shown in Fig. 5.1 a) and b) does not allow for independent tuning of $\Gamma_{1(2),N(S)}$.

Figure 5.2 a) shows differential conductance as a function of V_{g1} and V_{g2} and focuses on a narrow plunger gate region. V_{bg} is decreased to -35 V with the intention to sharpen the conductance peaks as well as the sub-gap features seen in bias spectroscopy. Figures 5.2 c) and d) show high bias spectroscopy cuts for two quantum dots in the system (QD1 and QD2) taken along the arrowhead lines indicated in plot a). Simple qualitative examination indicates the presence of superconducting gap that manifests itself as a region of zero conductance around $V_{SD} = 0$ for both quantum dots. While for QD1 it is possible to observe Coulomb blockade diamonds (Fig. 5.2 c), it is not possible for QD2 within the given plunger gate range (Fig. 5.2 d). Additionally, data for QD1 reveals that $U \gg \Delta^*$.

Since QDs, which for odd filling behave as magnetic impurities, are coupled to the superconductor, discrete subgap (bound) states are expected to appear within the gap Δ^*. In the limit $U \gg \Delta^*$, these states are in fact Yu-Shiba-Rusinov bound states (see Sec. 2.3.1) and they actually lead to the zero-bias features seen in Fig. 5.2 a). Figure 5.2 d) shows low bias spectroscopy of QD1 with more focus on the gap region. The subgap loop-like features (consequence of subgap states crossing the zero-bias) strongly indicate that the QD1 undergoes the ground state transition. In fact, it transitions from spin-singlet (QD has even occupation, spinless) to spin-doublet (QD has odd occupation, spinful) back to spin-singlet ground state, i.e. $|S\rangle \rightarrow |D\rangle \rightarrow |S\rangle$. The fact that spinful QD is in doublet ground state indicates the low coupling between the QD and the superconductor. In contrast, Figure 5.2 f) shows no signs of loop-like behaviour, rather that the the subgap states might be anticrossing. This could be interpreted as the YSR singlet ground state $|S_{YSR}\rangle$, which results from the

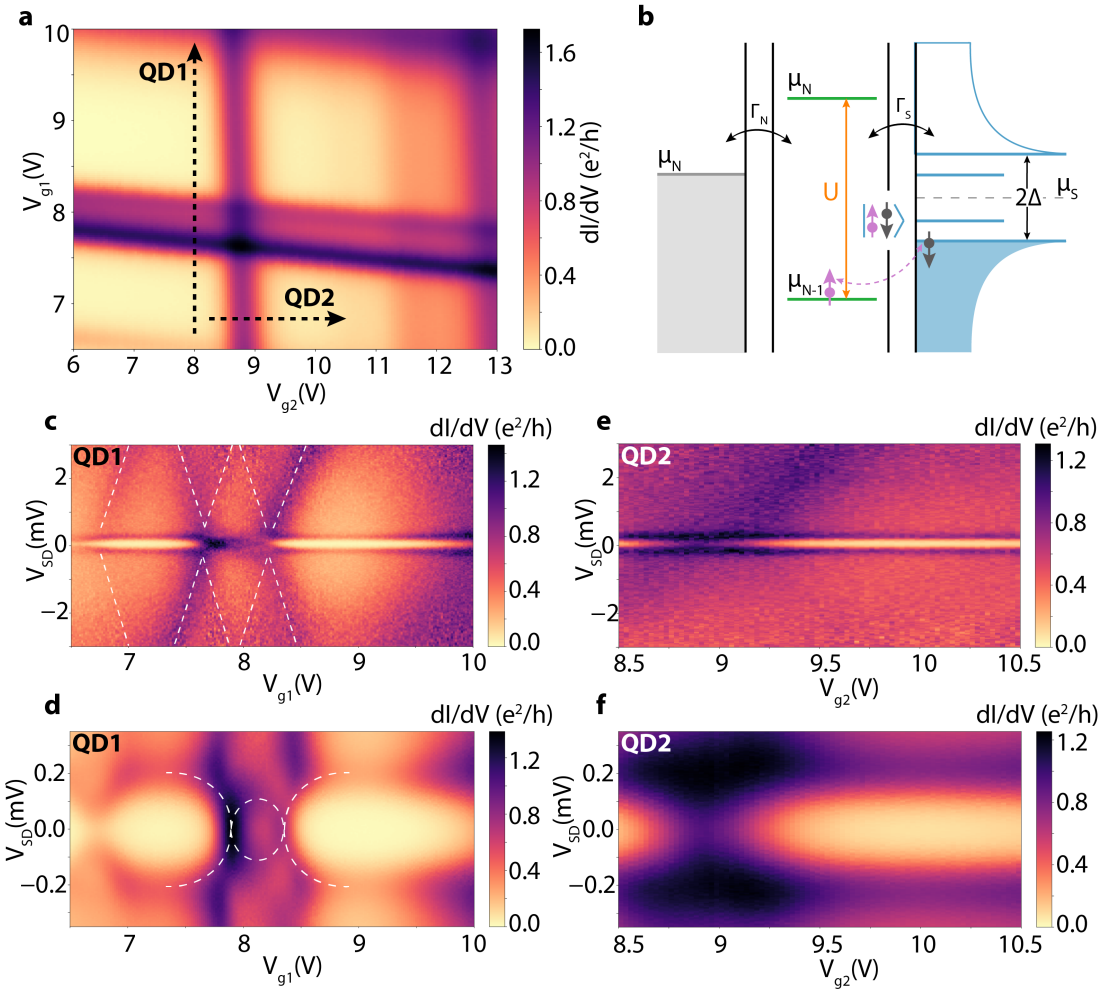

Figure 5.2: *High bias and low bias spectroscopy [of parallel quantum dot system].* **a)** Plot of linear conductance as a function of two plunger gates. Arrowhead lines show the place and directions where bias spectroscopy cuts were taken for the two QDs. All data shown in this figure was taken at V_{bg}= -35 V. **b)** Schematic energy diagram of the system in cotunneling regime. **c)** High bias spectroscopy plot taken for QD1. There are visible signatures of Coulomb diamonds and induced superconducting gap. Addition energy is estimated to be $E_{add} \approx 5$ meV, while lever arm $\alpha \approx 0.005$. **d)** Low bias spectroscopy of QD1. The induced gap is clearly present. The broad features near the edges of the superconducting gap suggest the presence of bound states. However, the broadness of the features prevents any definite conclusion. **e)** High bias spectroscopy of QD2. **f)** Low bias spectroscopy of QD2. Plot shows superconducting gap and broad features at the gap edges.

spin screening by the quasiparticles in superconductor as the tunnel coupling

between the QD and the superconductor is increased. Hence, a ground state transition $|D\rangle \rightarrow |S_{YSR}\rangle$ takes place for spinful QD. The condition to observe the spin-screening is that system is tuned in the intermediate regime $\Gamma \sim U$. Now, the singlet ground state is maintained within the given plunger gate range (8.5 V$\leq V_{g2} \leq$10.5 V), regardless of the QD occupation. Sharper, better resolved subgap features are needed to remove any doubts regarding this interpretation. To resolve sub-gap states well Γ_S needs to be larger then Γ_N [3]. The broadness of the features seen in Fig. 5.2 d) and f) suggests that this is not the case and this is likely due to the significant tunnel coupling to the normal lead.

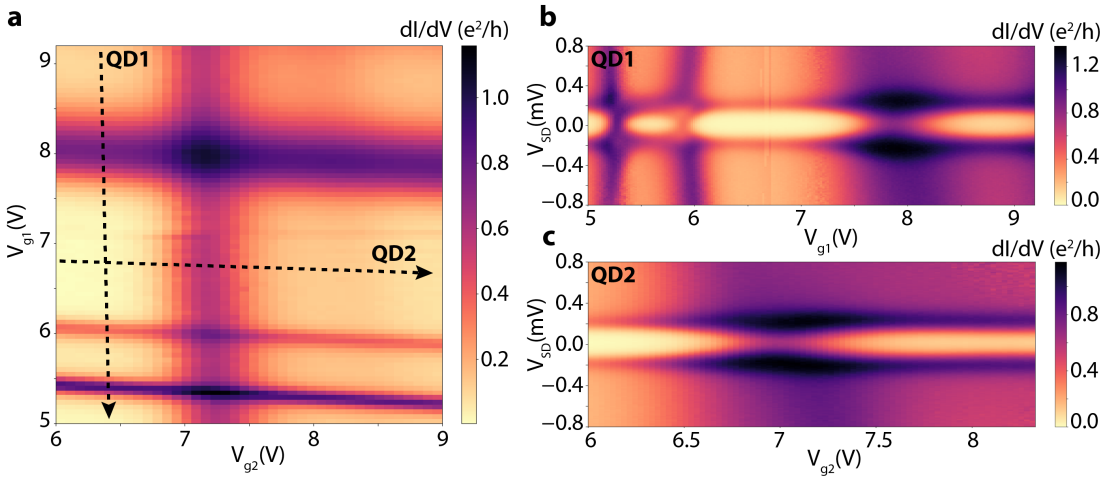

Figure 5.3: *Charge stability diagram and bias spectroscopy.* **a)** Differential conductance plotted in the plane of two plunger gate voltages, V_{g1} and V_{g2}. Data was measured at the back gate voltage of V_{bg} = -16.45 V. Black arrowhead lines mark the place and direction where two bias spectroscopy cuts were taken. **b)** Plot of differential conductance as a function of source-drain bias and plunger gate 1. The induced superconducting gap is visible in addition to broad features close to the gap edges. **c)** Same type of plot as in b), but taken for QD2 along the QD2 arrowhead line shown in a).

To further support the conclusions made above regarding the bound states, another set of data is presented and examined. Figure 5.3 a) shows the charge stability diagram for the two QDs system, taken at $V_{bg} = -16.45$ V. It encompasses a total of three conductance lines for QD1 within the V_{g1} modulation range. The spacing between the two thin conductance lines is small relative

to the larger spacing that follows before the next line appears around $V_{g1} = 8$ V. This behavior resembles the shell-filling pattern [16], [49] where smaller and larger charge stable regions indicate odd and even occupation of QD1, respectively. The behaviour of conductance lines at their crossing and resulting shape of the charge stable regions are the same as in Fig. 5.2 a).

Figure 5.3 b) shows a low bias spectroscopy of QD1 where two interesting features stand out. First, a loop-like feature appears within the gap between approximately 5 V $\leq V_{g1} \leq$ 6 V. From the previous discussion, it follows that the system is in the spin-doublet $|D\rangle$ ground state. This also agrees with the prediction based on the shell-filling pattern, that QD is spinful within this region. Next conductance line, appearing around V_{g1} =8 V in Fig. 5.3 a), is much broader and within the YSR bound states framework it could signal $|D\rangle \rightarrow |S_{YSR}\rangle$ quantum phase transition. This is justified by the fact that increase in V_{g1} leads to the increase of tunnel coupling between the QD1 and the superconducting lead, necessary to stabilize $|S_{YSR}\rangle$ as the ground state for the spinful QD. Hence, one could argue that the feature appearing in Fig. 5.3 b) around V_{g1} =8 V is showing the bound states closely anticrossing, as expected for $|S_{YSR}\rangle$.

Figure 5.3 c) shows a low bias spectroscopy cut for QD2, taken along the horizontal arrowhead line shown in Fig. 5.3 a). Following the same reasoning, the broad conductance line in a) indicates the existence of $|S_{YSR}\rangle$ ground state and the system is in spin-singlet ground state throughout the given V_{g2} range.

5.3 DEVICE OF INTEREST: N-PDQD-ISLAND-S

Moving on, lets look into a device with a slightly different geometry. Coloured SEM image of this device, shown in Fig. 5.4 a), reveals the details of a N-pDQD-Island-S geometry. Unlike the previous devices, Al half-shell is oriented upwards (away from the substrate), as illustrated in Fig. 5.4 b).

The length of the superconducting island is about 2 μm. Two parallel quantum dots are formed in the etched section of InAs nanowires between the normal contact and the superconducting island, seen on the left hand side of the device in Fig. 5.4 a). On the right hand side of the device, the superconducting

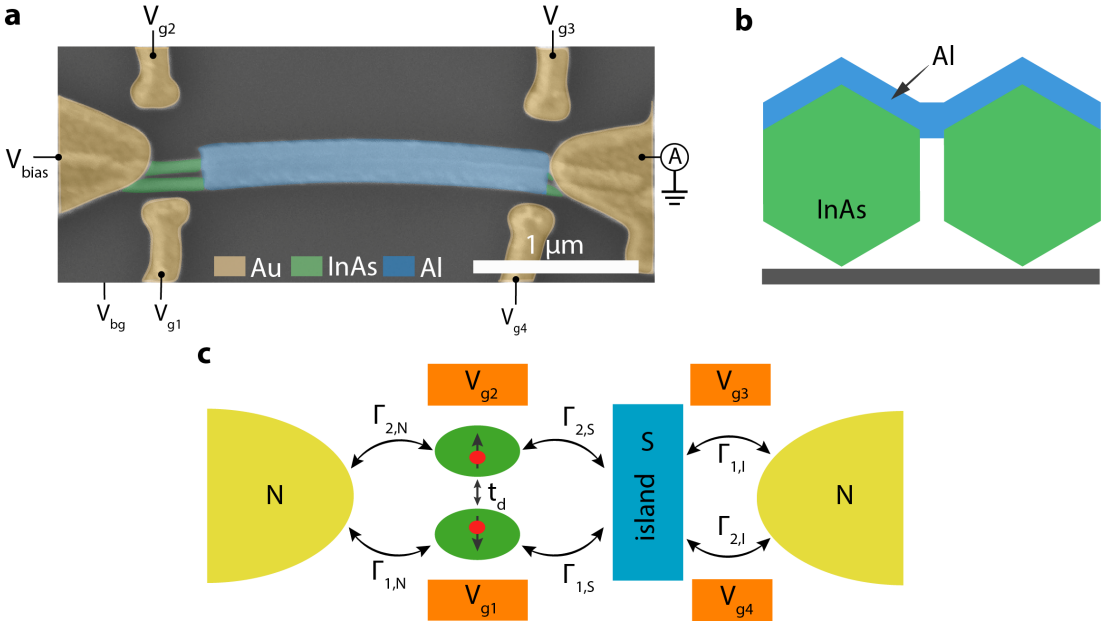

Figure 5.4: *Device of interest with S island.* **a)** Scanning electron micrograph of the investigated device, false coloured. Device is fabricated on S++/SiO_2 substrate and it features two normal contacts, four plunger gates and a global back gate. **b)** Illustration shows that Al half-shell (blue) is sitting in top of the nanowire pair (green), pointing away from the substrate (gray). Al half-shell is 100 nm thick. NWs are in FF orientation. **c)** Schematic diagram of the investigated system. Two parallel QDs are tunnel coupled to common normal lead on the left and a superconducting island to the right. Besides being tunnel coupled to QDs, the island is also tunnel coupled to the normal lead to the right ($\Gamma_{1,I}$, $\Gamma_{2,I}$). t_d represents the inter dot tunnel coupling. Plunger gates 1 and 2 (V_{g1} and V_{g2}) are tuning the chemical potential of the two QDs, while gates 3 and 4 (V_{g3} and V_{g4}) are controlling the coupling of the island to the normal lead.

island is tunnel coupled to another normal contact due to the existence of a small gap between them where Al half-shell is etched away. Note that plunger gates are asymmetrically positioned in respect to the nanowire pair as a result of EBL misalignment. Simplified break down of different device components and couplings involved is illustrated in Fig. 5.4 c). Note that plunger gates shown in orange are capacitively coupled to the device. By applying voltages V_{g1} and V_{g2} it is possible to shift the electrochemical levels of QD1 and QD2, respectively. The nanowires used to fabricate this device come from QDev 872 batch. They measure $\approx$ 69 nm in diameter each, and have $\approx$ 100 nm thick Al

half-shell.

5.4 UNDERSTANDING THE DEVICE

The device is tuned into the low coupling regime $\Gamma \ll U$ and the resulting measurements are presented in Fig. 5.5. This work is not concerned with investigating the island features, but rather focuses on quantum dots. Thus, a region of charge stability diagram with suppressed signal coming from the island was identified and shown in Fig. 5.5 a). Two sets of conductance lines confirm that the system is consisting of two QDs that are being tuned by V_{g1} and V_{g2}. Figure 5.5 b) and c) show bias spectroscopy measurements of each QD revealing Coulomb blockade diamonds as expected. Note how the Coulomb diamond vertices (corresponding to conductance peaks at V_{SD} =0 V in normal state) are split and shifted in $V_{g1(g2)}$. This separation happens due to the emergence of induced superconducting gap Δ^* when device transitions into the superconducting state [51]. The Coulomb diamond vertices become split in energy by $2\Delta^*$ and shifted in gate voltage by $\Delta V_{g1(g2)}=2\Delta^*/\alpha_{1(2)}e$, where α is the lever arm of the plunger gate [51], [52]. The shift in gate voltage is caused by the capacitive coupling between the contacts and QDs [52], [53].

Bias spectroscopy of QD2, shown in Fig. 5.5 c), seem to reveal a feature that manifests itself as kinks in the straight line (marked by dashed black line) that comes from a cotunneling line in QD1 (marked by black arrow in 5.5 b)). This happens due to the interdot charging (adding charge to one dot affects the levels on the other).

Figure 5.5 d) focuses on a narrow plunger gate region of the plot in a). This zoomed in version shows splitting of triple points due to significant interdot charging energy U_{12}. However, there seem to be no curvature of the kinks which implies that tunnel coupling $t_d = 0$. Looking back at the geometry of the device and the separation between the wires (see Fig. 5.4 a)) this seems to be plausible.

Moving on, Fig. 5.5 e) is the result of taking a bias spectroscopy cut across the triple points, as indicated by black arrow in plot d). There is a clearly seen

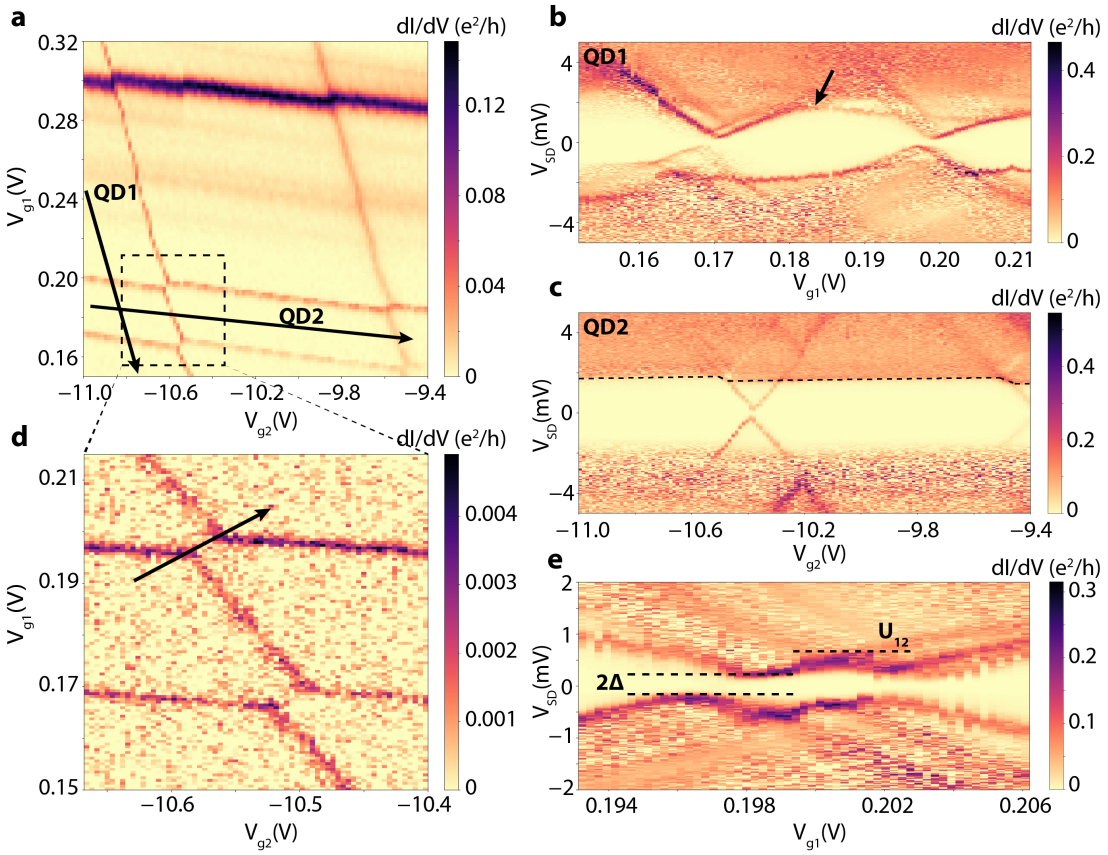

Figure 5.5: *Charge stability diagram and bias spectroscopy plots.* **a)** Measurement of differential conductance in respect to V_{g1} and V_{g2}. Voltages of other gates are fixed during measurement at values V_{g3} = 4 V, V_{g4} = 0 V, V_{bg} = -0.5 V. **b)** Bias spectroscopy cut taken along the black arrowhead line named QD1 in panel a). There are characteristic features indicating the presence of Coulomb diamonds and superconducting gap. **c)** Similar to plot in b). **d)** Zoom in on a portion of the charge stability shown in a). The black arrowhead line shows where the cut corresponding to panel e) was made. **e)** Resulting plot of a bias spectroscopy across the two triple points, as seen in panel d). From this data, superconducting gap $2\Delta^*$ and inter dot charging energy U_{12} are estimated to be 0.37 meV and 0.3 meV, respectively. They are also indicated by the black dashed lines.

suppression of transport at the bias range where $e\,|V_{SD}| < \Delta^*$. Due to very weak coupling to the S lead ($\Gamma_S \ll U$) we do not observe any bound states, evidenced by a very clear superconducting gap. However, it was possible to extract the values for characteristic energies of the two QDs from the plots in 5.5 b) and c). The results are summarized in Table 5.1. QD1 has addition energy E_{add}= 2.9 meV, while E_{add}= 7.4 meV for QD2. This suggests that QD2 is likely to be larger

than QD1.

	$\mathbf{E}_{add}$ [meV]	α [eV/V]	$\mathbf{U}_{12}$ [meV]	$\mathbf{2\Delta^*}$ [meV]
QD1	2.9	0.05	0.3	0.37
QD2	7.4	0.008		

Table 5.1: *Characteristic energy scales for parallel DQD system in superconducting regime.* The summary of estimated values for addition energies, exited state (single-particle) level spacing and lever arm extracted from bias spectroscopy data shown in Fig. 5.5. In addition, the estimates for the induced superconducting gap Δ^* and inter-dot charging energy U_{12} are provided.

5.5 SUMMARY

To summarize, the parallel quantum dot system coupled to the superconducting lead was successfully demonstrated in superconductor-semiconductor double nanowires. Independent control of the QD levels as well as the coupling to the leads has been shown. Through the measurements of differential conductance it was possible to observe and estimate the size of the the superconducting gap Δ^* induced by the Al half-shell in the InAs nanowire core below the transition temperature T_C. Despite the fact that the suppression factor value suggests the presence of hard gap, it is clear from the measurements that the conductance is not completely suppressed when moved closer the BCS peaks. Hence, the superconducting gap can be characterized as soft and suppression factor is not the most reliable descriptor in this case. Next, no signs of interdot coupling, capacitive nor tunnel coupling, have been observed for device in the intermediate coupling regime ($\Gamma \sim U$). On the other hand, there were clear signs of capacitive coupling between the two QDs for the device in low coupling regime ($\Gamma \ll U$). Finally, the bias spectroscopy cuts of QDs revealed subgap features that are most likely YSR bound states. There have been some indication of ground state quantum phase transition $|D\rangle \rightarrow |S_{YSR}\rangle$ for spinful QD, as its coupling to the superconductor was increased. Bound states demonstration is important as it shows potential to study YSR molecule using parallel double nanowires.

6 FULL-SHELL PARALLEL NANOWIRES: LITTLE-PARKS EFFECT

Besides having parallel nanowires with half-shell of Al, it is possible to grow them with full Al shell as seen in Sec. 3.1. These kind of structures are the result of recent technological advancements and provide the opportunity to investigate the Little-Parks effect [35] in the system of two closely placed ultrathin superconducting cylinders. Little-Parks effect was investigated earlier using single InAs nanowires with Al shell and both destructive and non-destructive regimes were observed [7], [39], [54]. However, this is the first time to try to study this effect in double nanowires. This experiment is motivated by the abundant curiosity to investigate the behaviour of such a system. Upon expanding the knowledge of these particular nanowires through transport experiments, they could be ultimately used for the experimental demonstration of Topological Kondo effect [10].

My personal contribution to the work presented here includes performing measurements in a team of three people, writing the code for the L-P model with the assistance of another team member and assisting with the device fabrication.

6.1 DEVICE OF INTEREST

Figure 6.1 a) shows the false coloured micrograph of the investigated device. This device has four contacts, two outer ones to apply the current bias and two inner ones to measure the voltage. Aluminum oxide was removed before Au contacts were deposited. The nanowires used to fabricate this device come from

QDev 898 (see sec. 3.1), featuring Al shell with thickness between 12-15 nm and InAs core with diameter of about 50-60 nm. An illustration of nanowire cross-section (Fig. 6.1 b) shows two nanowires in facet-to-facet (FF) orientation having a uniform Al shell and distance d_{NW} between them. Note that the nanowires can be in an alternative corner-to-corner (CC) orientation, not depicted here. However, TEM images of cross-sections (see sec. 3.1) reveal that Al shell is not quite uniform and in fact varies in thickness around the perimeter of the studied cross-section. Also, nanowires seem to be clamped together (d_{NW}=0) or having a very small separation between them. Results from three different devices are reported in this chapter. They all have the same geometry as shown in Fig. 6.1 a), but different length L of the device and nanowire orientation.

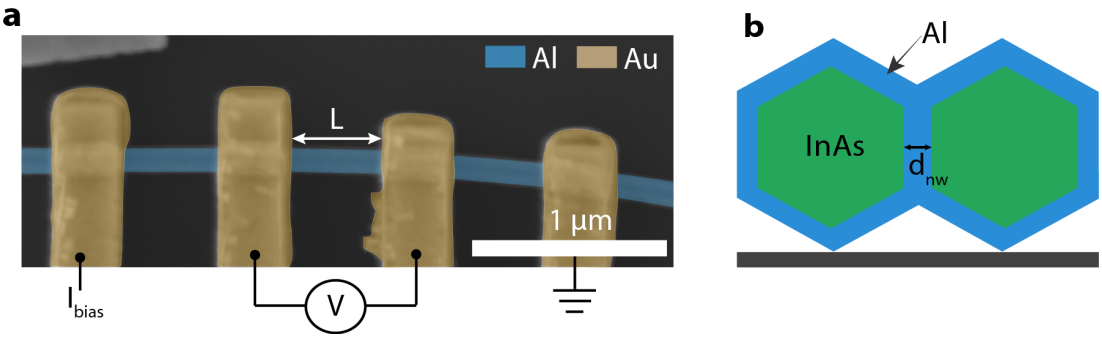

Figure 6.1: *Device of interest with full-shell Al.* **a)** False coloured SEM micrograph showing a device geometry and four-probe measurement setup. Device is fabricated on highly doped S++/SiO_2 substrate. L is the length of the measured device. **b)** An illustration of cross-section of full Al shell (blue) InAs core (green) nanowires used for fabricating device in a). d_{NW} stands for the distance between the wires. Thickness of Al shell is estimated to be between 12-15 nm. Here, nanowires are shown in facet-to-facet (FF) configuration, but they can also be in the alternative corner-to-corner (CC) configuration.

6.2 UNDERSTANDING THE DEVICE

The results of measuring differential resistance of the superconducting shell $\frac{dV}{dI}$ with respect to the applied current bias I_{bias} and the applied magnetic field B_r for the two different devices are shown in Fig. 6.2. Plot in a) shows a series of superconducting lobes (yellow regions $\frac{dV}{dI}$ being zero) separated by the regions

where superconductivity is destroyed ($\frac{dV}{dI}$ assumes a finite normal-state value). This is a characteristic pattern of superconducting lobes that emerges in the destructive regime. This device has maximum switching current I_{sw} ≈22 μA at B=0 T (zeroth lobe, $n = 0$). First ($n = 1$), second ($n = 2$) and third ($n = 3$) lobe have reduced maximum I_{sw} in comparison to the zeroth lobe. This is a consequence of the magnetic field applied to a cylinder of finite thickness, which ultimately destroys superconductivity when the critical field B_C is reached.

Between the superconducting lobes at I_{bias}= 0, the differential resistance assumes a finite value hinting that the device has transitioned into normal state. These normal state regions appear around odd half-integer values of $\frac{\phi}{\phi_0}$ as expected from theory (see sec. 2.4). However, the resistance around zero bias for $\frac{\phi}{\phi_0}=\frac{1}{2}$ takes a value that is only a fraction of the normal state resistance (R_N=10.94 Ω). This points towards the existence of an anomalous, intermediate phase where $0 < R < R_N$. This is not the case between the first and second, as well as the second and third lobe where $\frac{dV}{dI}=R_N$. A possible explanation is that this deviation from expected resistance value could be due to the inhomogeneities (e.g in coherence length ξ_0, cylinder thickness t_S) along the Al shell (see sec. 3.1)[41] which would cause variations in local I_{sw}. In such a case the phase transition would be gradual and incomplete for the whole cylinder since some regions of Al shell would turn normal before the others as current bias is modulated. The same reasoning can be used to explain the lobe replicas (i.e. regions of lobes that have finite resistance) as well as the non-zero resistance within the third lobe. Note how the separation between the lobes increases with the increasing magnetic field. This is the result of non-periodic term of the pair-breaking parameter (see sec. 2.4) which grows quadratically with increasing magnetic field.

Figure 6.2 b) shows the same type of measurement as in a) but for a different device. In this case, there is no separation between superconducting lobes around zero bias (i.e. no phase transition), except between the second and third lobe. The superconducting lobe pattern observed at lower magnetic field is an example of non-destructive regime phase diagram. Here, the pair-breaking parameter is not large enough to completely quench superconductivity but only

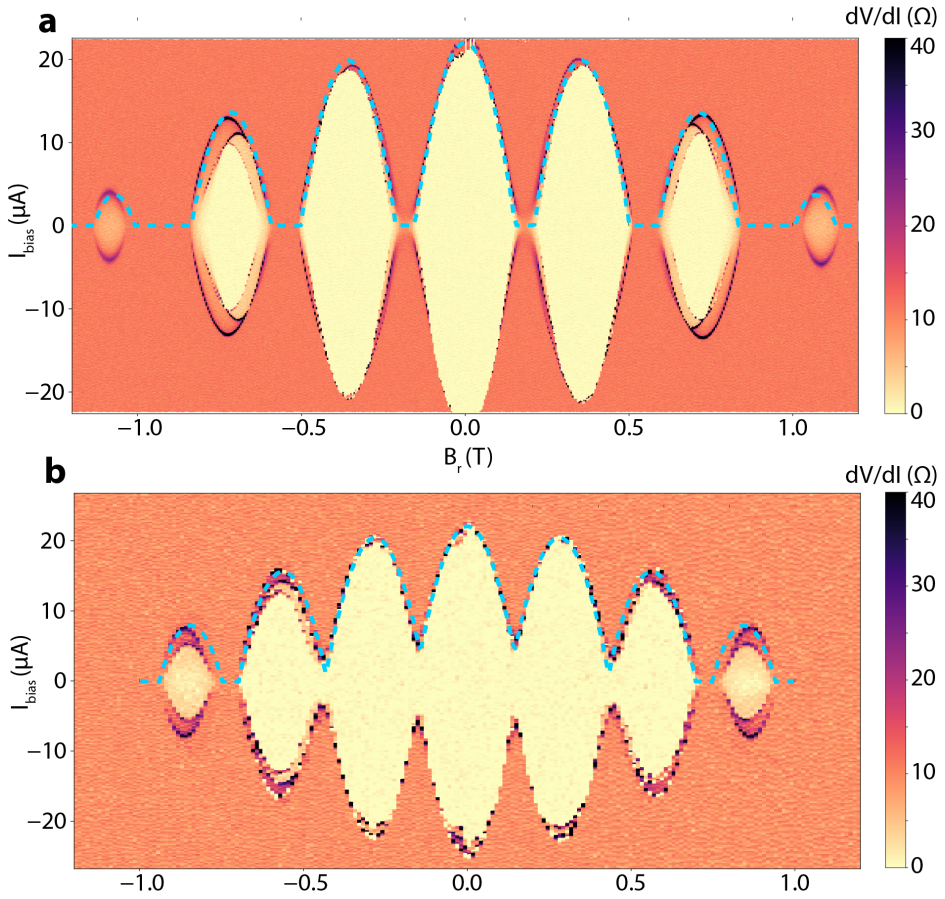

Figure 6.2: *Destructive vs. non-destructive Little-Parks regime.* **a)** Differential resistance $\frac{dV}{dI}$ measured as a function of applied magnetic field B_r and current bias I_{bias}, at base temperature of $\sim$ 30 mK. Superconducting lobes are separated by the resistive, normal regions of phase diagram. Switching current I_{sw} periodically oscillates with decreasing amplitude from $B_r = 0$ up to $B_{r,C} = \pm 1.1$ T, at which point the superconductivity is destroyed. **b)** Same as a) but for a different device. Non-destructive Little-Parks oscillations are present in the range of $B_r = \pm 0.7$ T. For larger B_r, there is only one occasion of re-entrant superconductivity (one more lobe for $n = 3$) after which the superconductivity vanishes at $B_{r,C} = \pm 0.9$ T.

to reduce the switching current I_{sw}. Maximum I_{sw} for this device is found to be 22 μA at B=0 T and R_N=9.1 Ω. Vanishing superconductivity between the second and third lobe is a result of ever increasing pair-breaking parameter α which gets large enough to destroy superconductivity around $\frac{\Phi}{\Phi_0} = \frac{5}{2}$.

The model based on theory described in Sec. 2.4 was used to fit the experimental data. It was developed for cylinders with circular cross-section, which

is not the case with the system under the investigation here. In fact, it consists of two closely placed hexagonal nanowires, making the cross-section more oval shaped rather than circular. Therefore, to make the use of this model, some assumptions had to be made. It was assumed that the cross-sectional area of the the two hexagonal nanowires can be mapped into the circular cross-section with the equal area. This means that the diameter that goes into the model calculations is the diameter of that circle. By equating the two areas it is easy to find that the diameter of the corresponding circle is larger than the diameter of a single hexagonal nanowire that is in the system by a factor of ≈ 1.28. The matlab code used to calculate the fitting curves can be found in Appendix C.

There are three fitting parameters in this model: coherence length ξ, thickness of the aluminum shell t_s and the diameter of the circle d_{circ}. Best fits for two different devices are shown as blue dashed lines in Fig. 6.2. Qualitative analysis of these lines suggests that the model at hand explains the observed features and the effect quite well. Interestingly, whether the cross-section is circular or oval shaped does not seem to affect the underlying physics (see Sec. 2.4). However, the theory curve fails to account for the third lobe with the same accuracy as for the others. A potential cause of this might be the fact that the model used in this thesis does not account for the presence of the perpendicular field. If the applied magnetic field, that is thought to be parallel to the nanowires, is in fact under an angle, a contribution of the resulting perpendicular component could lead to a modulated lobe patterns where the last lobe would be most affected. A thorough examination of this is under way by another group member.

For the device in Fig. 6.2 a) it was found from the fitting that $\xi = 82$ nm, $t_s = 13.7$ nm, and $d_{nw} = 92$ nm, where d_{nw} is the diameter of the nanowire. The best fit parameters for the device in Fig. 6.2 b) give $\xi = 70$ nm, $t_s = 13.7$ nm, and $d_{nw} = 80$ nm. An independent measurement of Al thickness, done by nanowire growers using SEM and TEM imaging, estimates the thickness of the Al shell to be between 12-15 nm. Hence, the thickness extracted from the data fitting agrees well with the expected value. The same is true for the nanowire diameter.

Coherence length ξ_S can be calculated by using the expression for dirty-limit shell coherence length $\xi_S = \sqrt{\pi\hbar v_F l_e/24 k_B T_C}$ [29], [54]. Critical temperature T_C=1.2 K (at B=0), Fermi velocity of Al $v_F = 2x10^6 m/s$ [55], and Drude mean free path l_e=6.7 nm (calculated using R_N=10.94 Ω) yield ξ_S=106.4 nm for the device in destructive regime (Fig. 6.2 a). For the device in non-destructive regime (Fig. 6.2 b) the same approach (using $R_N = 9.1$ Ω) yielded $\xi_S = 111$ nm. Dirty limit coherence length values do not seem to agree with the values extracted from the data fitting. This approximation might not be valid for the system in hand.

Figure 6.3 shows a selection of measurement results for the third device. The measurement of differential resistance $\frac{dV}{dI}$ as a function of temperature T and applied magnetic field B (Fig. 6.3 a) reveals a T-B phase diagram. It shows the re-entrant nature of superconductivity, typical for devices in destructive regime. Hence, the superconducting regions (yellow) are split by the normal-state regions (purple). This is further illustrated by the horizontal cut shown in Fig. 6.3 b). Within the superconducting regions, $\frac{dV}{dI}$ is suppressed and drops to zero, while for normal regions $\frac{dV}{dI}$ abruptly takes a constant finite value around odd half-integer values of $\frac{\phi}{\phi_0}$ even at the lowest measured temperature. The normal states resistance for this particular device is measured to be $R_N \approx 14.2$ Ω. Vertical line cuts from Fig. 6.3 c) are taken at three positions marked in Fig. 6.3 a). All three lines converge towards the R_N value past the zero-field transition temperature. Note how the superconducting critical temperature decreases from $T_C \approx 1.2$ K at $\frac{\phi}{\phi_0} = 0$ to $T_C \approx 0.8$ K at $\frac{\phi}{\phi_0} = \pm 1$, as expected for a cylinder with finite thickness (see sec. 2.4). As with two previous devices, one identifies an intermediate resistive phase emerging around the superconducting-to-normal phase transition boundary line.

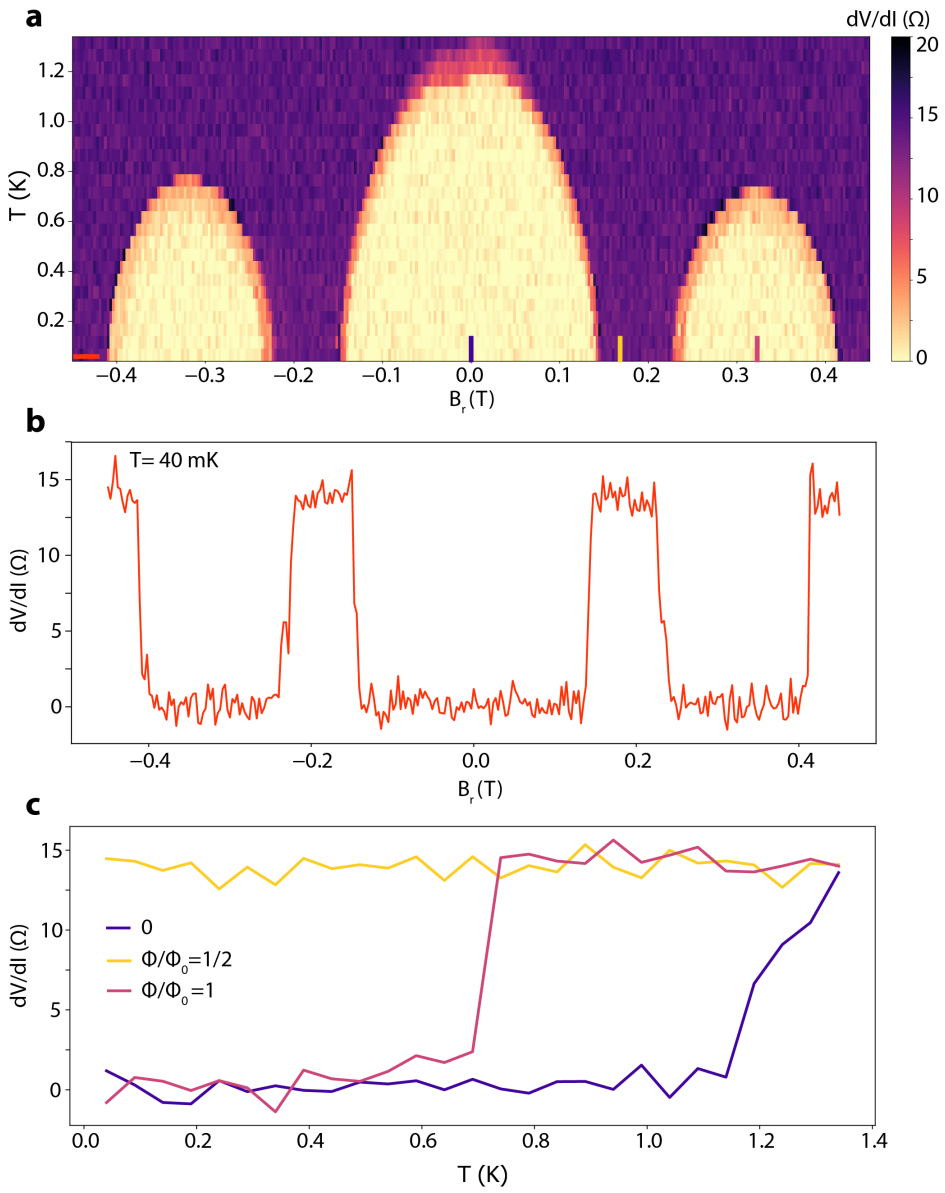

Figure 6.3: *Shell resistance in the T-B plane.* **a)** Periodic modulation of the superconducting critical temperature T_c as a function of applied magnetic field B_r, through the measurement of differential resistance $\frac{dV}{dI}$. **b)** A horizontal line cut at T = 40 mK taken from a). The alteration of normal and superconducting phase is shown as the magnetic field is modulated. **c)** Vertical line cuts taken at three different values of magnetic field that correspond to $\frac{\phi}{\phi_0} = 0, \frac{1}{2}, 1$. At odd half-integer values of $\frac{\phi}{\phi_0}$, differential resistance $\frac{dV}{dI}$ of the Al shell maintains the normal state resistance through the lowest measured temperature.

7 CONCLUSION AND OUTLOOK

Constant technological advancements in the field of material science offer new and exciting nanomaterials that could open a window to the experimental study of new phenomena. The work presented in this thesis progressively investigated the potential of one such nanomaterial, which is in fact a heterostructure consisting of two InAs nanowires grown parallel to each other and connected by epitaxial superconductor. Device fabrication procedure was successfully developed, despite many challenges particularly in regards to the nanowire transfer and etching of the aluminum half-shell. Coulomb blockade measurements for the first batch of devices showed that gate tunable parallel quantum dots (one in each wire) can be formed in this material by the combination of selective etching, normal lead positioning, and capacitive gating. Furthermore, it was observed that the tunnel coupling t_d between the QDs is negligible in case of finite separation between the nanowires.

After optimizing the fabrication procedure, devices from the second batch showed signatures of superconductivity in the form of induced superconducting gap Δ^* and features that resemble the Yu-Shiba-Rusinov bound states within the gap. It was also found that the tunnel coupling between the nanowires was negligible, most likely due to the oxide formation between the wires.

Measurements of the full-shell heterostructures showed a behaviour that agrees with the one expected for the Little-Parks experiment. Data fitting showed that the results can be well explained by the theory that describes the Little-Parks effect. Parameters extracted from data fitting were in good

agreement with the expected values, apart from the coherence length.

Perspectives

In the future experiments with the half-shell double nanowires, it would be beneficial to include the single wire from the same growth batch in order to have a control case for the superconductivity. Furthermore, decreasing the nanowire diameter would lead to larger confinement and access to the shell-filling pattern in zero-bias conductance measurements. Additional improvement include independent control of the coupling to the leads, which can be achieved via top gates. If this was implemented, future experiment could have improved resolution of the bound states.

For the double InAs nanowires with full-shell Al, as investigated in Chapter 6, there are two promising avenues to pursue in the future. Due to the negligible separation between the nanowires, the flux seemed to pierce through the two nanowires as if they were one, resulting in classical Little-Parks effect. In this context, a next step would be to ensure a double nanowire heterostructure with a finite spacing between the wires. Repeating the experiment with this condition satisfied could potentially lead to the observation of some new physics.

Building up on this, a potential solution could be to simply use a different superconductor, ideally a high T_C one like Pb. The concern with aluminum is that the the shell thickness needs to be quite small to ensure large critical field B_C. This thickness requirement might in turn hinder the attempts to have two wires separated with enough aluminum between them to make it significant. Using a high T_C superconductor like Pb instead circumvents this thickness requirement, since it allows for a thicker superconducting shell without paying the price of lowering B_C.

A ADDITIONAL CALCULATIONS

A.1 ERROR PROPAGATION

Assuming that variables are not correlated.

For addition and substraction:

$\delta X = \sqrt{(\delta a)^2 + (\delta b)^2 + (\delta c)^2}$

For multiplication and division:

$\delta X = X\sqrt{(\frac{a}{a})^2 + (\frac{\delta b}{b})^2 + (\frac{\delta c}{c})^2}$

A.2 BROADENING OF CONDUCTANCE PEAKS IN NDQD DEVICE

Here is a brief description of how conductance peak broadening was investigated. It was observed that for QD1 more than for QD2 conductance peaks broaden significantly as the voltage on gate 1 gets increased. In the case that $k_B T >> \Gamma$, conductance peaks will be thermally broadened. In the opposite case where $\Gamma >> k_B T$, it is tunnel coupling that broadens the conductance peaks.[25]

At bath temperature T=30 mK, it is estimated that $E_{thermal} \approx 9.1 \mu eV$ using $E_{thermal} \approx 3.53 k_B T$. A cut showing resonance peaks for QD1 at fixed gate 2 voltage was taken and shown in the Fig. A.1. FWHM (full width half maximum) of the peak is extracted and converted to energy E_{FWHM} with the help of lever arm α=0.002 (extracted from data). For the three peaks shown in the plot $E_{FWHM} = 0.4meV, 0.6meV$ and $2meV$, from smallest to largest peak respectively. These values are much larger than the value found for $E_{thermal}$. $E_{thermal}$ seems

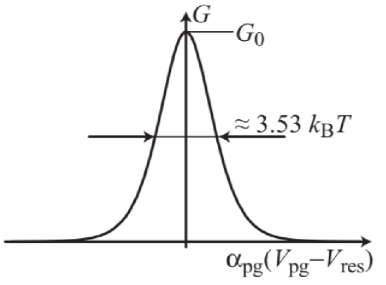

Fig. 18.34 Shape of a conductance resonance according to eq. (18.57) in the single-level tunneling regime, if the tunneling coupling is much smaller than temperature.

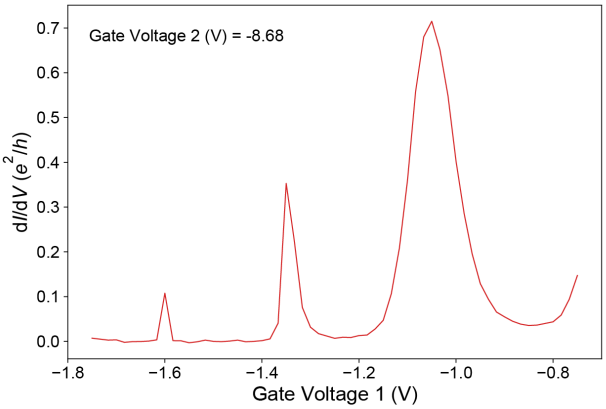

Figure A.1: *Conductance peaks.* **a)** From Ihn. **b)** Cut from the data.

to be only a very small part of E_{FWHM}. From this it follows that the broadness of the peaks cannot be explained by thermal broadening.

B FABRICATION PROTOCOLS

B.1 BLANK CHIP RECIPE

OVERVIEW:

1. **Alignment Marks**
2. **Bonding Pads**

Note:
* To protect sample (chip, wafer) while cleaving, one can spin A4.5 and bake it for 2 minutes at 185°C before scribing and cleaving.
** Start with 2 inch Si/SiO_2 wafer with 300 nm thick oxide. Cut the wafer to desired dimensions.
*** Cleaning is a very important step, as it ensures that there are no debris left from previous wafer cleaving, nor any other kind of dirt that can later hurt device fabrication.

1. ALIGNMENT MARKS

Cleaning:

- Rinse wafer in H2O, IPA and acetone.
- Sonicate in acetone for 2 min. At frequency 80 kHz, power 100.
- Rinse wafer in H2O, IPA and acetone.
- Blow dry with N_2 gun.

- O_2 plasma ash for 2 mins.

Resist:

- Ash for 2 min.
- Bake wafer for 2 min at 285°C.
- Spin EL9 resist in low acceleration mode (4000 rpm, 45 s).
- Bake for 3 mins at 185°C.
- Spin CSAR4 resist in low acceleration mode (4000 rpm, 45 s).
- Baking for 3 mins at 185°C.

Lithography (*parameters*):

- Area dose: 400 $\mu C/cm^2$
- Current: 500 pA
- Field size and no. of dots: 20 000 dots, 150 μm field size.

Development:

- Submerse sample in O-xylene for 30 sec.
- Submerse sample in MIBK:IPA 1:3 developer for 40 sec.
- Submerse sample in IPA for 30s.
- O_2 plasma ashing for 1 mins.

Metal evaporation:

** Chip was tilted by 15° (from 0) in the beginning of the evaporation and by 15° in the other direction from 0° in the middle of evaporation.*
*** 100 nm of metal is necessary for successful automatic alignnmet in EBL system.*

- Evaporate 5 nm of Ti.
- Evaporate 100 nm of Au.

Lift-off:

- Submerse chip in NMP (N-Methyl-2-Pyrrolidone).
- Sonicate for 1 min at 37 kHz, power 100.
- Submerse chip in NMP (N-Methyl-2-Pyrrolidone) at 85°C for 60 min, **facing down**.
- Flush the chip with a pipette to accelerate lift-off (avoid scratching). Use tweezers to hold the chip in place while flushing.
- Rinse with IPA.
- Dry with N_2 gun.

2. BONDING PADS

Resist:

- Rinse wafer in IPA and accetone.
- Bake wafer for 4 min at 115°C.
- Spin LOR3B resist in low acceleration mode (4000 rpm, 45 s).
- Baking for 4 mins at 185°C.
- Spin AZ1505 resist in low acceleration mode (4000 rpm, 45 s).
- Bake for 2 mins at 115°C.

* *Used LOR3B resist (lift-off) in order to create an undercut during development process, which results in smoother lift-off. Photolithography is used to expose bonding pads features as they are relatively large and EBL is not necessary in that case.*

Lithography(*parameters*):

- Exposure time 20 ms.
- Defocus -2.

Development:

- Submerse sample in MF321 for 30 sec.
- Submerse sample in Millipore (MQ) water for 30 sec.
- Dry with N_2 gun.
- O_2 plasma ash for 2 mins.

Metal evaporation:

* *Chip was tilted by 15° (from 0°) in the beginning of the evaporation and by 15° in the other direction from 0° in the middle of evaporation.*

- Evaporate 5 nm of Ti.
- Evaporate 100 nm of Au.

Lift-off:

- Submerse chip in NMP (N-Methyl-2-Pyrrolidone).
- Sonicate for 1 min at 37 kHz, power 100.
- Submerse chip in NMP (N-Methyl-2-Pyrrolidone) at 85°C for 60 min, **facing down**.
- Flush the chip with a pipette to accelerate lift-off (avoid scratching). Use tweezers to hold the chip in place while flushing.
- Rinse with IPA.
- Dry with N_2 gun.

B.2 DEVICE RECIPE

OVERVIEW:

1. **Metallisation (Clamping)**
2. **Aluminum Etching**
3. **Metallisation (Contacts and Gates)**
4. **Oxide Deposition**
5. **Metallisation (Top Gates)**

1. METALLISATION (Clamping)

Resist:

- O_2 plasma ashing for 1 min.
- Spin 50K resist in low acceleration mode (4000 rpm, 45 s).
- Bake for 2 mins at 115°C.
- Spin 50K resist in low acceleration mode (4000 rpm, 45 s).
- Baking for 2 mins at 115°C.

* *To remove resist legs (which can cause tilt during lithography) clean the bottom of the chip BEFORE baking.*

Lithography (*parameters*):

- Area dose: 850 $\mu C/cm^2$
- Current: 500 pA
- Field size and no. dots: 60 000 dots 300 μm field size.

Development:

- Submerse sample in MBIK:IPA 1:3 developer for 75 sec.
- Rinse in IPA for 30 sec.
- Dry with N_2 gun.
- O_2 plasma ashing for 2 mins.

Metal evaporation:

- Evaporate 5 nm of Ti.
- Evaporate 350 nm of Au.

* *Used Al foil to cover most of the chip, evaporating metal only on the area of interest. This prevents metal to stick to alignment marks and bonding pads.*

Lift-off:

- Submerse chip in NMP (N-Methyl-2-Pyrrolidone) at 85°C for 60 min, facing down.
- Flush the chip with a pipette to accelerate lift-off (avoid scratching).
- Rinse with IPA.
- Dry with N_2 gun.

* *To check under the optical microscope if the lift-off was successful, one can pour some IPA on a curved microscope glass and transfer sample from beaker to glass, quickly to avoid drying. Fine features might not be observable under optical microscope, but it should be enough to make a decision whether the process was successful or needs more time/flushing.*

2. ALUMINUM ETCHING

Resist:

- O_2 plasma ashing for 2 mins.
- Spin EL9 resist in **low acceleration mode** (4000 rpm, 45 s) - prevents NW from flying off.
- Bake chip at 185°C for 2 mins.

Lithography (*parameters*):

- Area dose: 400 $\mu C/cm^2$

- Current: 500 pA
- Field size and no. of dots: 60 000 dots 300 μm field size.

Development:

* *Before starting with development, it is good to prepare the etching agent. Set warm bath to 55°C and place one beaker with MBIK:IPA and one beaker with MQ. Make sure that the amount of liquid is the same in both beakers. Place the lid on both beakers and leave them to get warmed up while developing. For 30 ml of liquid, it should take between 15-20 mins to reach the desired temperature.*

- Submerse sample in MBIK:IPA 1:3 developer for 40 sec.
- Dry with N_2 gun.
- Bake chip at 115°C for 1 min.

* *After development is done, take the lids off of both beakers and check the temperature of MQ at the bottom of the beaker. Wait until the temperature is 50°C +/- 0.5. When desired temperature is reached, start with etching process.*

Etching:

- Submerse the sample in Transene D at 50°C for 14 + 1 sec for ~100 nm Al, or 8 + 1 sec for ~17 nm Al.
- Rinse in beaker with warm MQ for 30 sec.
- Rinse in breaker with room T MQ for 30 sec.
- Dry with N_2 gun.

* *+1 second accounts for the time it takes to transfer the sample from Transene D beaker to MQ beaker where etching process is effectively stopped.*

Resist stripping:

- Submerse the sample in NMP at 55°C for 7 mins.
- Rinse with IPA (to remove NMP).
- Dry with N_2 gun.

3. METALLISATION (Contacts and Side Gates)

** The same procedure as metallisation for clamping. EXCEPT there is **RF milling step** before metal evaporation!

Resist: See Metalisation (Clamping)

Lithography: See Metalisation (Clamping)

Development: See Metalisation (Clamping)

RF milling (gentle):

- Settings: 7 W, 18 mTorr, 7 min. (*It is necessary to remove the native oxide from wires in order to make an Ohmic contact to InAs*).

Metal evaporation: See Metalisation (Clamping)

Lift-off: See Metalisation (Clamping)

* *If we are making **side gates**, which are usually deposited in the same step as the contacts, then the recipe is the same.*

4. OXIDE DEPOSITION

* *Dialectric, in this case HfOx, is used to isolate top gates from the rest of the device (nanowires, contacts) and achieve capacitive coupling between the top gates and the nanowires. ALD was used to deposite oxide.*

Resist:

- O2 plasma ashing for 1 min.
- Spin El6 resist in low acceleration mode (4000 rpm, 45 s).
- Bake for 2 mins at 115°C.
- Spin A2 resist in low acceleration mode (4000 rpm, 45 s).
- Bake for 2 mins at 115°C.

Lithography (*parameters*):

- Area dose: 900 $\mu C/cm^2$
- Current: 2 nA
- Field size and no. dots: 20 000 dots 300 μm field size.

Development:

- Submerse sample in MBIK:IPA 1:3 developer for 60 sec.
- Rinse in IPA for 30 sec.
- Dry with N_2 gun.
- O_2 plasma ashing for 2 mins.

Oxide Deposition:

- 10 h degassing.
- Deposite 15 nm of HfOx.

Lift-off:

- Scratch the corners of the chip gently with tweezers to remove the resist and deposited oxide from these areas. It is done to accelerate the lift-off. After scratching, the colour difference should be visible under the optical microscope.
- Submerse chip in NMP (N-Methyl-2-Pyrrolidone) at 85°C for 60 min, **facing down**.
- Flush the chip with a pipette to accelerate lift-off (avoid scratching).
- Rinse with IPA.
- Dry with N_2 gun.

5. METALLISATION (Top Gates)

Resist:

- O_2 plasma ashing for 2 mins.
- Spin A6 resist in low acceleration mode (4000 rpm, 45 s).
- Bake 15 mins at 185°C.

Lithography (*parameters*):

- Area dose: 1000 $\mu C/cm^2$
- Current: 500 pA
- Field size and no. dots: 240 000 dots 600 μm field size.
- PEC parameters (Si substrate, 400 nm PMMA).

Development:

- Submerse sample in MBIK:IPA 1:3 developer for 30 sec.
- Rinse in IPA for 30 sec.
- Dry with N_2 gun.
- O_2 plasma ashing for 45 s.

Metal evaporation:

- Evaporating 5 nm of Ti.
- Evaporating 150 nm of Au.

* *Used Al foil to cover most of the chip, evaporating metal only on the area of interest. This prevents metal to stick to alignment marks and bonding pads.*

Lift-off:

- Submerse chip in NMP (N-Methyl-2-Pyrrolidone) at 85°C for 75 min, **facing down**.
- Flush the chip with a pipette to accelerate lift-off (avoid scratching).
- Rinse with IPA.
- Drying with N_2 gun.

** **The sample is ready to be bonded and loaded**. **

After lift off we usually SEM the sample to confirm that the lift-off went as planned. SEM is done very fast, at low acceleration voltage, to minimise the carbon deposition.
Ash with O2 plasma for 1 min after SEM imaging the sample, to remove any carbon that gets deposited while imaging, before proceeding.
Glue the chip to daughterboard with silver paste and let it dry for 10-15 mins before starting with bonding.
After bonding is completed, double check that all bonds are correct and successful.

C CODE FOR LITTLE-PARKS MODEL

The MatLab code listed below was used for the fitting of the Little-Parks oscillations in Chapter 6.

```
%% LP Model
% Sara Loric
% Jan, 2021
clc
clearvars

%% Parameters

df_nw=82.*10.^(-9); %diameter of one hexagonal nanowire
ts=13.*10.^(-9);  %Al thickness - speculation that the
    aluminum is
%X nm - 2nm of Al ox

% Here we equate the area of a double hexagon to a circle
     and get the
%circle's diameter
df=df_nw.*sqrt(3.*sqrt(3)./pi); %final diameter for model
    ; df=1.286(df_nw)

```

```
17 % calculation based on the area which is derived from the
       normal state
18 %resistance and the length of the device
19 xi=83*10^(-9);  %coherence length
20 Tc=1.2; %critical temperature
21 Area=2.*3.*sqrt(3)./2 .* (df_nw/2).^2;
22 Area_circle=pi.*(df./2).^2;
23 Area_calc=7.252*10^(-15); % area calculated from the
      oscillation period
24 %% Additional setups
25
26  n = [3,2,1,0,1,2,3];
27  size = [-3.5:1:3.5];
28
29  F_tot = linspace(-3.5,3.5,280); % phi/phi_0 axis
30
31  B=(F_tot.*(2.067*10^(-15)))./Area_calc; % B axis
32
33 %% Alpha Parallel
34
35  alpha_par=[];
36  for k=1:length(n)
37      F=linspace(size(k),size(k+1),40);
38      alpha = [];
39      for i=1:length(F)
40      alpha(i)=(4*xi^2*Tc)/Area_circle * (((n(k)-abs(F(i))
           )^2 +(ts/df)^2 *(F(i)^2 ...
41      + n(k)^2 /3)));
42      end
43      alpha_par=[alpha_par,alpha];
44  end
45
```

```
46 figure(1)
47 plot(F_tot,alpha_par)
48
49 %% Alpha Perpendicular
50
51 %alpha_perp=4*xi^2*Tc*B_perp^2 *Area/Flux^2
52
53 %% Calculation for Tc_0
54 %eqnleft = T*exp(psi(1/2 +a/(2*pi*T)));
55 %eqnright = exp(psi(1/2)) * Tc;
56 %alpha_par_pos=alpha_par(9000:18000);
57 Tc_a=zeros(1,length(alpha_par));
58 syms T
59 for i=1:length(alpha_par)
60     try
61     a=alpha_par(i);
62     %x0=1;
63     %s = fsolve(@x*exp(psi((1/2) +(a/(2*pi*x)))) - exp(
          psi(1/2)) * 1.2,x0);
64     x=vpasolve(T*exp(psi((1/2) +(a/(2*pi*T)))) - exp(psi
          (1/2)) * 1.2==0,T,0.1);
65     Tc_a(i)=x;
66     catch ME
67         % move on, keep 0
68     end
69 end
70
71 figure(2)
72 plot(F_tot,Tc_a)
73 %ylim([0 1.3])
74
75 %%
```

```
76 I_c0=22;
77 I_sw=[];
78 for i=1:length(Tc_a)
79     I=I_c0 * (Tc_a(i)/Tc)^(3/2);
80     I_sw=[I_sw,I];
81 end
82
83 figure(3)
84 %set(gcf,'units','centimeters','InnerPosition
       ',[0,0,13.4614,6.4346])
85 plot(B,I_sw)
```

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