Electrical characterization of selective-area-grown InAs buffered nanowires with a $In_xGa_{1-x}As$ top barrier

Nikhil Niranjan Maka

Supervisors:
Peter Jeppesen Krogstrup
Daria Beznasyuk

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ABSTRACT

Semiconductor nanostructures are great building blocks for realizing topological quantum computation. The need for scalability of nanowire networks makes selective-area grown nanowires a promising candidate. Indium Arsenide nanowires are know for their charge accumulation surface states, which makes them ideal for implementation as Ohmic contacts. However due to poor interfacial qualities, roughness scattering and charge trapping phenomena prove to be detrimental towards the performance of InAs NWFETs.

In this thesis, electrical characterization is done on selective-area grown InAs buffered nanowires, consisting of double buffer layers of $GaAs(Sb)$ and $In_xGa_{1-x}As$. A further modification in the form of a thin 10nm $In_xGa_{1-x}As$ top-barrier is also grown on top of the InAs transport channel. This is known to improve the interfacial properties of the channel and promote a less abrupt decay or overlap of the charge density into the barrier region, leading to higher carrier mobilities. Although this has been investigated before in 2DEG platforms, it is yet to be implemented with selective-area grown heterostructures. Transport measurements and Schrodinger-Poisson simulations were utilized in tandem for exploring the implications of including the thin barrier layer.

ACKNOWLEDGEMENTS

I heartfully convey a big thanks to Peter Krogstrup for taking me under his wing and integrating me into the research group. There have been numerous issues and hurdles I have dealt with the past year, but his constant support and motivation was one of the main reasons I was able to make it this far. I would also like to thank some people who have made my daily thesis journey meaningful during its duration, starting from my office-room mates Harris, Sabbir, Yu, and Yan. The atmosphere in the room was never void of wisdom, advice, laughter, and stress food. I then thank Jordan and Daria for always lending a helping hand during my thesis work without fail, night or day. It also wouldn't complete without thanking Karolis and Sangeeth, the cleanroom gurus whom were always ready to jump on my fabrication mistakes made in the lab, without which I wouldn't have fabricated as many devices as I did during the Covid induced mayhem. I would also like to thank the whole Qdev and Micrsoft Lyngby team.

Finally I would love to thank my loving family who have always provided ample love and support during this journey. Till next time..

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Part I

PART I

1

MOTIVATION

We currently live in the information age, triggered by seismic digital transformation that started with the invention of the transistor and the integrated circuit [1, 2]. Intel co-founder Gordon Moore proposed a law of exponential dependence, stating that the amount of transistors that could be fitted onto an integrated circuit would roughly double every two years - formally known as Moore's Law [3]. However a realization is that the semiconductor industry can no longer keep pace with this increasing demand in shrinking electronics due to a lower limit set by the Bohr's radius and the characteristic size of atoms and molecules. Moreover, a parallel issue is the lack of computational power for carrying out highly complex simulations. In 1985, Richard P. Feynman hypothesized about an alternate form of computation, quantum in nature. This was to be done by reducing computer bits to the size of atoms. Some of the first framework for its physical implementation was laid out by David P. DiVincenzo [4, 5]

Enter: A Quantum Computer.

An important feature of a quantum computer is in the encoding or storage of information in the form of quantum bits (Qubits). Such a system would involve the representation of these qubits as two distinct states (0 or 1); and in a quantum superposition of both, thus allowing both states to exist at once. This would enable us to exploit its quantum nature, resulting in computational capabilities which surpass that of conventional computing systems [6]. To manipulate these qubits demands the development of new algorithms [7, 8], but to effectively realize this, there are major obstacles present such as the unstable evolution of a qubit's state due to decoherence. This is a result of unwanted interactions between the qubit and the environment or host material which would compromise the accuracy of the computation being made. Hence, a considerable amount of qubits would have to be devoted for the correction of errors that arise [6]. With this in consideration, numerous platforms have been investigated: ion traps [9], spin qubits [10], superconducting qubits [11], and qubit implementation in topological materials [12].

A promising area of research encompassing material sciences and quantum mechanics, is that of Topological materials. One of the first proposals for realizing topological qubits was brought forward by Kitaev in 2003 [13]. Recently a wave of studies on Majorana zero modes (MZM), named after physicist Ettore Majorana, has emerged. These neutral excitations corresponding to bound zero-energy ground states, only depend on the exchange characteristics of the quasiparticles, and not on the method or details of execution. In other words they are topologically protected, and therefor provide ample protection from decoherence and errors which may arise when being used for quantum computation [12, 14].

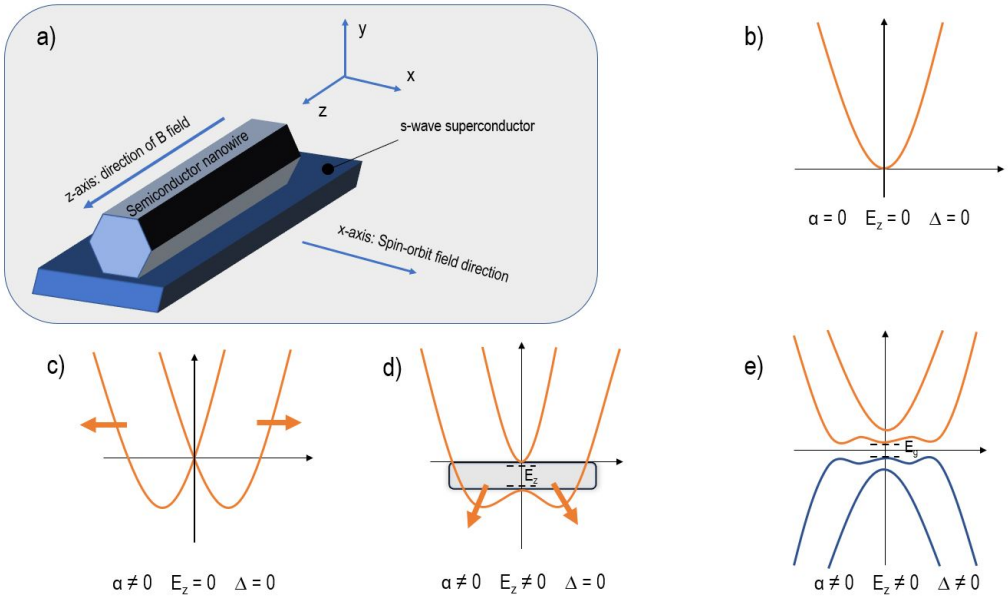


Figure 1: Ingredients for finding Majorna Zero Modes: (a) Shows a 1D NW with a proximitized superconductor with a magnetic field B applied in perpendicular to the spin-orbit axis (b) shows an E-k parabola without spin-orbit interaction (c) we now see horizontal splitting of the spin-orbit bands cause due to strong spin-orbit coupling (characterized by a finite Rashba spin orbit coefficient $\alpha \neq 0$) (d) A helical gap opens with the application of a magnetic field B perendicular to the spin-orbit field direction (e) finally we can tune in and out of a topological gap after proximitizing the nanowire with a s-wave superconductor.

The search for MZMs has been performed on a number of occasions [15, 16, 17]. Using a one-dimensional (1D) semiconductor nanowire with strong spin-orbit coupling allows energy-momentum $E - k$ parabolas seen in Figure 1 to split horizontally. On application of a magnetic field B (i.e Zeeman field) along the nanowire axis and perpendicular to the spin-orbit field as seen in Figure 1a, a Zeeman splitting of the spin orbit bands and opening of a helical gap at $k = 0$ occurs. Pairing this setup in proximity to a s-wave superconductor (i.e Aluminum or Niobium) leads to an induction of a superconducting gap Δ due to the coupling between semiconductor and superconductor. The system can now be driven in and out of a topological phase transition with careful tuning of the electrochemical potential μ and magnetic field (magnitude and angle to nanowire axis). The choice of materials plays a large part in creating a non-trivial topological phase transition (opening of topological gap). Materials with high spin orbit coupling strength α and Lande g-factor are desired such as in Indium Arsenide (InAs) or Indium Antimonide (InSb) - this corresponds to high spin-orbit interaction and sets the critical magnetic field needed to drive the system through the topological phase transition. Furthermore, 1D nanowires are preferred as we hope to find single localized MZMs at the ends of a nanowire, and not a continuum of modes. The quality of the induced superconducting gap depends on the effective tuning of properties at the semiconductor-superconductor (SU) interface. A proven method for preserving a high SU interfacial quality is through in-situ epitaxial growth of semi-super nanowires [18]. Also, a significant requirement for the opening of a topological bulk gap is the need for pristine, disorder free crystalline materials.

Topological materials research took a significant turn with the retraction of a high profile 2018 Nature article [19]. It was finally concluded that any signs of MZMs investigated over the past decade are mainly trivial

zero-bias conductance peaks, most likely caused due to the presence of disorder or impurities in the material. Much of the present emphasis lies with the improvement of the quality of materials being used [20].

This is where the motivation for this thesis lies - in investigating and characterizing electronic quantum transport in semiconductor materials. This thesis will focus solely on one of the key ingredients needed for the development of topological quantum computation, namely epitaxially grown 1D semiconductor nanowires.

Nanowires are cylindrical or elongated shaped structures with radial dimensions of around 100 nm and in the range of a few in the longitudinal direction, thus being quasi one-dimensional in nature [21]. One of the main benefits nanowires possess is their unlimited material design freedom in terms of composition, stacking, and geometry. With its small dimensions, strain can be relieved at the surface, and also there is flexibility in being able to fabricate devices with local metallic or superconducting contacts and electrostatic gates on top, beneath or next to the wires [22]. Group III-V semiconductor nanowires (i.e InAs, InSb) are the main focus of interest, due to their high electron mobility and excellent electrical tunability of charge transport [23].

There are two methods for nanowire growth via: (i) Vapour Liquid Solid growth (VLS) and (ii) Selective Area Growth (SAG). Both are grown in the Molecular Beam Epitaxy (MBE) system which is great for achieving pure, epitaxial layered growth [24]. Various studies have been carried out previously with VLS or free-standing nanowires[25, 26]. Although they allow for delicate engineering and growth of complex heterostructures for studying electron transport, there is difficulty in scaling up to multiple networks of nanowires. Therefore, SAG nanowires have attracted alot of interest due to its compatibility with various growth techniques. Also the top-down processing methods used for defining structures for SAG nanowires allows for ease in scaling up [24]. Several studies have also been carried out for SAG nanowires [27, 28, 29], and will be one of the main topic of discussion. This thesis will focus on the investigation of fundamental electronic properties Indium Arsenide Selective area grown buffered nanowires. Much detail of what comprises the term ”buffered” in these nanowires will be discussed in the later sections. The other main emphasis in the experimental work for this thesis, is in the inclusion of a thin top-barrier layer for a set of samples for the SAG nanowires. These are meant to serve as comparisons with the samples grown without the barrier. This structural modification holds a promising premise within the transport measurements of past literature []. This will also be discussed in further sections and will be a primary topic of discussion through the support of experimental results.

The thesis outline is as follows:

Part I: Theory - Firstly, important and relevant concepts in quantum transport will be covered. This will be followed with a necessary overview of MOSFET terminology in connection with the Field-effect transistor (FET) measurements performed at QDev, Neils Bohr Institutet, will be discussed. The theoretical discussion then moves to a brief discussion on SAG growth/morphology and the addition/purpose of a top-barrier layer.

Finally the theory will focus on the relevant concepts and terms needed to understand the Schrodinger-Poisson simulations to support the electronic characterization of the SAG models with/without the top-barrier.

Part II: Fabrication and Measurement methodology - The step-to-step methods and processes involved in the clean room fabrication at Qdev, Neils Bohr Institute and measurement at Microsoft Lyngby campus will be the focus of this section.

Part III: Results and Discussion - Scanning transmission electron microscopy (STEM) and Electron energy loss spectroscopy (EELS) profiles provided by Qdev and Catalan Institute groups will be used in accordance with the FET measurement and Comsol results for a final discussion on the electrical characterization of fabricated devices for the SAG NWs.

Part IV: Conclusion and Future Outlook

2

THEORY

2.0.1 *Quantum Transport*

One of the basic principles in electronics revolves around obtaining a certain output (current I or voltage V) for a measurement on a device can be obtained by through by applying a signal (voltage or current respectively). These quantities of V and I and its dependence on one another can be described by $\frac{V}{I}$ known as resistance (R). Re-arranging the equation to $V = RI$, is popularly known as Ohm's law [30]. It's proportionality can be further extended to a device length (ℓ) divided by its cross-sectional A and given as: $R \propto \frac{\ell}{A}$. It holds a proportionality to the parameter resistivity (ρ) which depends on the electronic properties of the material or device in question. With Drude's model, it can be defined as the inverse of the product of the charge, carrier density and, mobility ($\rho = \frac{1}{n|e|\mu}$). These quantities are highly important in the context of performing electrical measurements on devices.

Electrical measurements depend entirely on the qualities of a device or material's inherent carrier density n, which is defined as the product of the density of states (DOS) with the Fermi function $f(E)$. DOS is the number of states available in a system for conduction. The $f(E)$ describes the probability of these states to be occupied. Both of these terms strongly depend on the Fermi energy E_F which is the energy below which electronic states are filled and available to conduct. These terms together ultimately describe carrier transport in a material. The carrier density may vary with respect to the nature of dimensions of the material. the thermal broadening the Fermi level with respect to the band structure. This project focuses on a one-dimensional case because of the diameter/width of the nanowires being smaller than the mean free path l_e. Moreover, the base temperature of the cooling system is $1.7K$, giving a thermal broadening of $0.15meV$. The equation for the carrier density along with the previously introduced terms is given by Eq 1.

$$n = f(E) \cdot DOS = \frac{1}{1 + e^{\frac{E - E_F}{KT}}} \cdot \begin{cases} \delta(E) & \text{0 D} \\ \frac{1}{\sqrt{E^{-1/2}}} & \text{1D} \\ const & \text{2D} \\ \sqrt{E^{1/2}} & \text{3D} \end{cases} \tag{1}$$

Nanowires and their one-dimensional properties, along with various configuration of band structures, density of states, and operation temperatures leads to different electrical transport regimes. Diffusive and Ballistic transport are two types of transport an electron could experience as it traverses through a transport channel in a material. The former is a result of propagation in a 1D system where the length before a scattering event occurs know as mean free path l_e, is lesser than the channel length L. The latter type of transport namely, Ballistic transport where l_e is greater than the channel length is of particular interest. Sometimes l_e is near the order of L, which is known as quasi-ballistic transport [31].

Ballistic transport was reported in 2DEGs since 1988, and up till now, has been a primary method to characterize transport in 1D or quasi-1D nanostructures and its applications. Its observation has also expanded to other nano-platforms such as quantum point contacts (QPC) and in NWs. Using ballistic mode of transport as a type of transport-quality certification for structures has allowed researchers to develop higher quality materials and complex heterostructures by fine tuning its properties as it pertains to high mobility and dislocation-free crystals [32].

Ballistic transport is best introduced through a QPC case, where a narrow constriction is made between two wide electrically conducting regions with a width comparable to the wavelength of the electron. This can be further applied to other one-dimensional systems, which is the main focus of this thesis. Two main requirements are needed to obtain pronounced $N\frac{e^2}{h}$ steps in a curve where conductance G is measured with the tuning of voltage (gate-voltage), in a constricted channel. Firstly the electron mean free path l_e needs to be longer than the transport channel length L, and additionally, the Fermi wavelength should be comparable to the transport channel (i.e nanowire) width. An ideal QPC in a finite low temperature and under an applied potential between the two reservoirs or source/drain contacts (R for the right and L for the left) the current is given by the expression $I_{tot} = -g_s\frac{|e|}{h}\sum_n\int_{E_n}^{\infty} dE[f_L(E) - f_R(E)]$, where g_S is the spin degeneracy factor of an electron which is equal to 2 and $f_i = (\exp\left(\frac{E-\mu_i}{K_BT}\right)+1)^{-1}$ is the Fermi - Dirac distribution for each reservoir (i is an index standing for each reservoir). The conductance from the small applied source-drain voltage $V_{SD} = \frac{\mu_L - \mu_R}{|e|}$ where μ_L being the electrochemical potential for the left reservoir, and μ_R the electrochemical potential for the right reservoir, is given by:

$$
\begin{aligned}
G =& \frac{I_{tot}}{V_{SD}} = \frac{g_s|e|}{hV_{SD}}\sum_n\int_{E_n}^{\infty} dE[f_L(E) - f_R(E)] \overset{\mu_L - \mu_R \ll K_BT}{=} \frac{g_s|e|}{hV_{SD}}\sum_n f_L(E_n)V_{SD} \implies \\
G =& \frac{2|e|}{h}\sum_n f_L(E_n)
\end{aligned}
\tag{2}
$$

The above formalism validates the tuning of the Fermi level for effective control of the occupied modes in the channel. In the case of field-effect transistors, the most straightforward way to shift the energy potential is by gate modulation. Moreover, the number of modes existing in an ideal quantum wire is limited by its width giving an estimate of $N \approx 2\frac{W}{\lambda_F}$, where λ_F is the Fermi wavelength [32]. We then implement this for

the NWs which to draw a good estimate for subband mode plots seen later in the thesis. These are the $[1\bar{1}0]$ and $[010]$/$[100]$ orientated SAG NWs. The diameter (or width as seen in Figure 6) for both $[010]$ and $[100]$ NWs are approximately $235nm$, and for $[1\bar{1}0]$ NWs it is $265nm$. The Fermi wavelength in InAs is $24nm$, that approximately equals to $N = 2 \times \frac{230}{24} = 20$ modes being occupied for $[010]$/$[100]$, and 23 modes for $[1\bar{1}0]$ NWs in theory. Because of resonance effects however and subsequent thermal broadening at the temperature 1.7K (temperature used for FET experiments); there is a smearing of the conductance steps or plateaus.

The above approximation is an empirical explanation of the quantized conductance in accordance with the Fermi function. We now open a discussion for a more realistic description for mesoscopic systems. The reservoirs have finite size and break translational invariance within the wire. We now define a 1D effective potential along the NW axis through which the electron wavefunction is considered to propagate. This introduces a tunnelling probability through the nth channel with an energy E and thus, we define the transmission function $T_n(E) = |t_n(E)|^2$ which is energy-dependent. The total current is now given by $I_{tot} = \frac{|g_s|e||}{2\pi} \int_0^\infty dE \sum_n T_n(E)[f_L(E) - f_R(E)]$. Then the conductance for a finite temperature $T \ll 0$ is described by the Landauer - Büttiker expression [32]:

$$G = g_s \frac{|e^2|}{h} \int_{-\infty}^{\infty} dE \sum_n T_n(E)(\frac{\partial f_L(e)}{\partial E}) \tag{3}$$

The above equation describes the transmission of electrons between two reservoirs (i.e source and drain) as seen in *Figure*. The resulting sub-band occupation is an important concept as it helps envision the transverse motion of electrons through the nanowire in discrete quantized modes, that are the conducting channels used for transmission between reservoirs. The step-like units of $2\frac{e^2}{h}$ of conductance G as seen in *Figure*.., corresponds to the (de-)population of individual 1D subbands with each step. Previous studies have noted a dependence of subband spacing with the width of the channel. A reduction in width has shown to increase spacing between occupied sub-bands, resulting in the subbands being more pronounced or distinct due to greater quantum confinement. Conversely, a larger channel width has reduced confinement with smaller subband spacing because of more subbands being occupied. Correlation has also been made between large channel width and disorder due to reduced electron scattering in between subbands. Ideally, controlling fewer conducting channels with ballistic transport can be preferable in obtaining disorder free materials for the creation of topological states [33, 34].

2.0.2 *MOSFET concepts*

Metal oxide semiconductor field effect transistors are at the heart of principles which the devices fabricated and investigated in this thesis rely on. The MOSFET structure consists of a source and drain which are the metallic leads, a thin oxide dielectric layer (i.e HfOx, AlOx, etc) and a metallic gate on top of the oxide layer. An n-type or p-type semiconductor channel lies below the aforementioned layers. The transport channel can be filled or depleted with tuning of the chemical potential or Fermi level through the metal gate.

a) Metal-Semiconductor junctions and MOSFET regimes

It is first important to note the nature of the junction formed at the metal-semiconductor interface. Band diagrams are a necessary method of visualizing changes in energy (with respect to vacuum) in a semiconductor when the bias is modulated through the metal gate. Depending on whether our transport channel in the semiconductor is n-type or p-type, the location of the Fermi level is either close to the conduction or valence energy band respectively. If we consider the axis through the gate/oxide/semiconductor to be along the z-axis. The semiconductor work function W_S and metal work function W_M is the minimum energy required to excite an electron in the respective regions from its Fermi level to the vacuum.

W_S is not a accurate value to use for a semiconductor as it may change due to doping. The more widely used term is the electron affinity χ_{SM} which represents the energy needed to excite an electron from the conduction band edge to vacuum. In our SAG nanowire used in the FET measurements and Comsol modelling, InAs is the choice of transport channel due to a desirable feature it possesses in forming an accumulation layer of electrons at its surface. These surface states are therefore responsible for n-channel characteristics in InAs field effect transistor devices. Band bending at the surface occurs due to charge transfer, leading to a change in the values of work function and electron-affinity at the material surfaces. This becomes an issue, hence the values we obtain for these terms from literature should only be taken as rough values. Semiconductor-metal junctions can be two types: either Schottky barriers or Ohmic contacts. An important note in forming these junctions is that, for an n-type semiconductor - we require the electron-affinity of the semiconductor to be larger than the work function of the metal, thus obtaining a Ohmic contact; opposite holds true for a Schottky barrier. These junction forming roles are fully reversed for a p-type semiconductor where an Ohmic contact is formed with a smaller electron-affinity and vice-versa. For more information on Schottky barrier please see [30]

We are more interested in Ohmic junctions as they allow for ease of electron flow between the metal and semiconductor. In Figure 2 we see a metal-semiconductor ohmic junction before and after contact. On contacting, electrons which are filled up to the Fermi level spill into empty conduction band states of the

semiconductor and hybridize. As a result, an electrostatic potential builds up in the semiconductor which opposes the flow of charge by band bending.

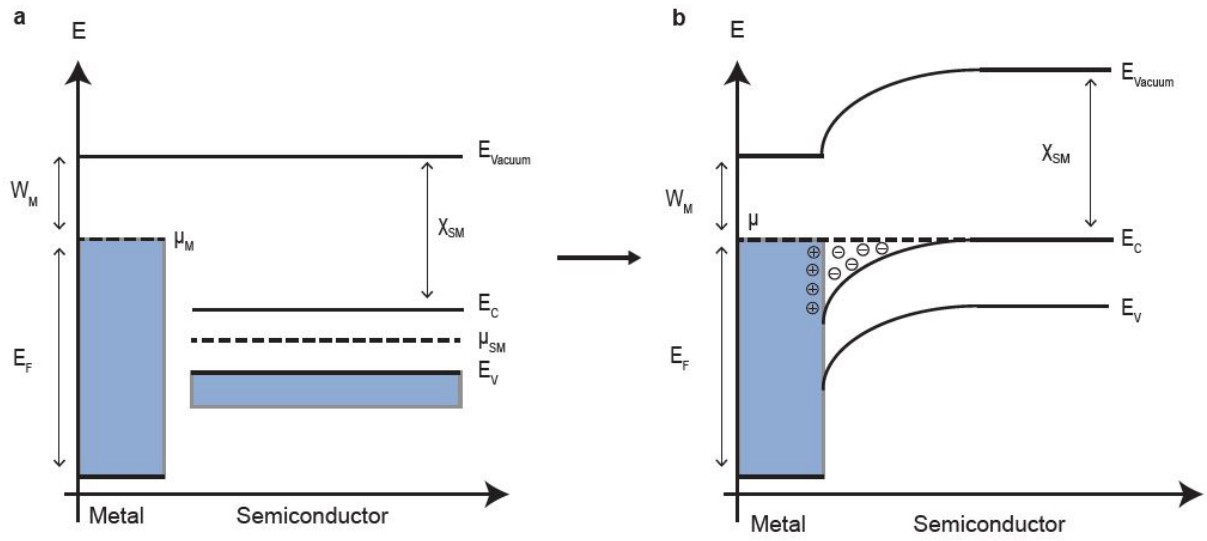


Figure 2: Diagram describing a metal-semiconductor junction where (a) shows the band diagram for before contact between metal and semiconductor. Here W_M is the work function of the metal and χ_{SM} the electron affinity of the semiconductor. Band bending characteristic to a Ohmic junction occurs when χ_{SM} ¿ W_M before contact (b) After contact electrons freely move from the metal to the empty conduction band states in the semiconductor. This leads to a downwards band bending. Positive charges in the metal screen the surrounding charges to keep the electric field constant within the metal. Adopted from [35]

Now, moving back to a full picture of a MOSFET potrayed by the schematic below Figure 3 We have a MOSFET device with gate length or channel length L between metal contacts (soure and drain), and width or diameter d of the conducting channel (i.e nanowire). A finite source-drain voltage V_{sd} when applied controls the flow of electrons between the source and drain. Now once a positive voltage V_g is applied to the gate, electrons are attracted to the interface between the gate dielectric and semiconductor. These electrons form a conducting channel known as the inversion layer. No gate current is required to maintain this inversion layer at the interface since the gate oxide blocks the carrier flow. The net result is the control of current between source and drain through the applied V_g. Various n-channel (i.e InAs NW) MOSFET regimes can be visited such as when a threshold voltage V_t limit of the applied V_g once exceeded, it leads to the accumulation of electrons at semiconductor/oxide interface. Further application of V_g with constant $V_s d$ leads to a saturation current regime. Conversely if negative V_g is applied at the metal gate, a depletion region is formed where where the electrons are pushed away from the semiconductor/oxide interface [30]. These regimes are important in assessing a FET's performance and the quality of the semiconductor material. For example, the depletion regime is very important in investigating whether a pinch-off effect can be achieved with a semiconductor transistor. This allows us to determine if the semiconductor NW grown contains few disorders, and whether the FET device fabrication process has been successful.

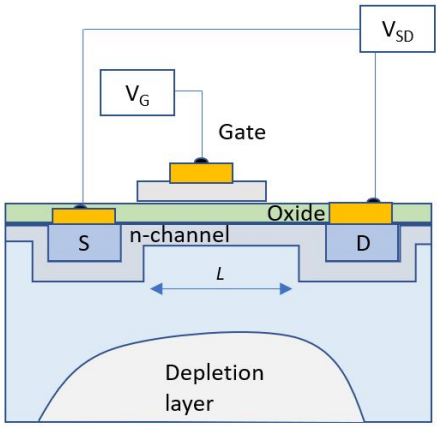


Figure 3: An illustration of a MOSFET as described

b) Field-Effect Mobility and Scattering phenomena

Semiconductor nanowires are versatile building blocks for electronic systems due to the unique possibilities they provide with control over properties such as dimension, composition, and doping during growth. Before their implementation with various applications, improved methods are needed to electrically characterize them. Nanowire field-effect transistors (NWFETs) which rely on the basic MOSFET principles as stated prior, have been a common choice for investigating basic carrier transport behavior and as potential high speed electronic devices with III-V semiconductor materials. InAs is favoured for use with NWFETs due to its natural inclination (without doping) to form a accumulation layer of surface states as a result of its Fermi level pinning above the conduction band. These interface trap or surface states possess donor like characteristics and are charge neutral when occupied by a electron and positively charged otherwise. Once the surface state density increases, localized states begin to overlap. As a result, a ”surface band” forms through which conduction occurs. This becomes ideal for forming low-resistance ohmic contacts. Surface states can also have unwanted effects on FETs such as the reduction in gate capacitance, cause hysteresis in FET measurements, and result in inaccuracies in field-effect mobility and carrier concentration estimation. Further challenges for realizing NWFETs is due to the lack of simple, reliable methods for determining carrier concentration and mobility. This is due to the requirement of extensive fabrication, and the exposure of the NWs to numerous process chemistries which provides a channel instead of bulk moblility. [36, 37].

Carrier mobility correlates drift velocity of charge carriers as they traverse through a material when an electric field is applied [**35**]. As discussed before, disorder has a detrimental effect for opening a topological gap. Therefore to further assess the degree of disorder in a material, carrier mobility is an important term of merit for a material. It is needed to weigh a NW’s potential for use in transport experiments and is important for the development for nanowire-based quantum devices.

In light of Matthiessen rule, which states that a number of scattering mechanisms determines the the net mobility by the following relation

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + ... \tag{4}$$

The net mobility μ is a result of all the scattering mechanisms that occur, which each lead to a separate mobility μ_n [38]. This shows that scattering events have a significant impact on the resulting net mobility. Hence it is important to try and identify the possibility of the type of scattering events involved and to reduce them.

Various scattering phenomena can be a hindrance for electron transport in FETs. The accumulation of surface states as observed with InAs NWs, results in surface roughness which induces changes in the local electronic band structures. This leads to scattering potentials that can scatter electrons whilst they are traversing through the NW. This is one of the main causes for mobility degradation in InAs NWFETS. Past studies have also found a strong correlation with the aforementioned surface-roughess scattering and the diameter d of a NW. Larger d provides more cross-sectional area for an electron to move through and reduces the roughness scattering potential, hence a smaller roughness effect is experienced by the electron with the mobility being enhanced. More negative threshold voltages and higher on-currents have been associated with larger d NWs in order to fully deplete its transport channel. Conversely, smaller cross-sectional areas have exhibited reduced field-effect mobility values, potentially due to higher frequency of scattering events [39, 40, 41]. It is difficult to accurately characterize the nature of scattering events that occur in FET devices. However, types of scattering events can be further differentiated according to the temperature T being used for a transport experiment. Higher temperatures of over $77K$ have display signs of scattering due to phonons or the presence of surface/interface traps. Lower temperatures on the other hand can be associated with neutral impurity scattering which is a result of formation of scattering potentials due to a neutral shallow-level impurity centers which becomes a dominant scattering source after carriers freeze out at low T. Just to name a few more - charged impurity (result of doping) and inter-subband scattering events can also take place within a NW under the presence of an electric field. It is important to understand the effect that certain dimensional and experimental parameters can have on the carrier mobility [41, 42].

Bulk InAs mobility of over $33000 cm^2 V^{-1} s^{-1}$ has been reported previously. This however isn't representative of InAs NWs due to its inherent surface states and the consequent surface scattering. Field-effect Mobility values for InAs NWs have been reported previously at $6850 cm^2 V^{-1} s^{-1}$ [36] and upwards to $16000 cm^2 V^{-1} s^{-1}$ with surface passivation [43]. For the InAs surface, lower mobility values of around $2000 - 3000 cm^2 V^{-1} s^{-1}$ have been exhibited where the states behave as a accumulated free-electron gas [36].

Conventional methods for measuring mobility have been through Hall Effect and Field-effect transport measurements. The focus will be on the latter which was incorporated for experimental work described in this thesis. Typical FET measurements are carried out through the measurement of current flow as a function of gate voltage and fixed voltage bias through a transport channel of a nanowire, connected by two electrodes (i.e source and drain). The conductance G of the channel can then be related by the linear region of the accumulation regime of the FET device. This is given by the following equation [38]:

$$G(V_g) = \left(R_S + \frac{L^2}{\mu C (V_g - V_{th})} \right)^{-1} \tag{5}$$

where V_g is gate voltage, μ the mobility, capacitance C, channel length L, threshold voltage being V_{th}, and the interface resistance R_S.

Here typically, the capacitance and channel length are known quantities and the FET mobility is usually determined by from transconductance, given by $g_m = \frac{dG}{dV_g}$ where $dG = dI_{SD}/dV_{SD}$ with dI_{SD} being the output current and dV_{SD} being the input bias-voltage. The interface resistances are to be neglected in the above equation due to the surface accumulation layer that InAs nanowires inherently have. Also, both mobility and field effect transport is described with the Drude model, where carrier transport display both classical and diffusive behaviour.

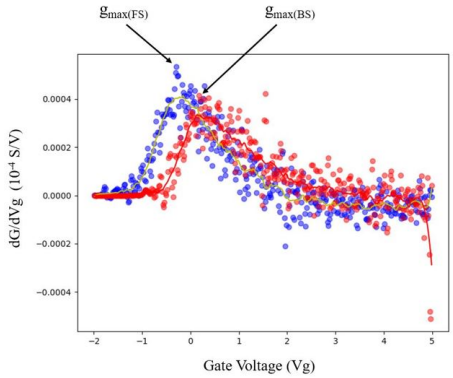
One of the methods for extracting mobility is by using maximum(peak) transconductance. The method used for this thesis work however, uses an equation fitting method for measured $G(V_g)$ as done in 2015, *Gül et.al*. Mobility μ, interface resistances R_S, and threshold voltage V_{th} are free-fit parameters in the above equation. The capacitance value is obtained from finite element modelling due to the complexity of the geometry for the selective-area grown (SAG) model. As a final note on the equation-fitting method, is that it benefits from the consideration of a wider gate voltage range by fitting a larger section of $G(V_g)$. Hence, the mobility extracted is insensitive to small conductance fluctuations, which is in contrast to the peak-transconductance method.

Low-temperature FET measurements have numerous challenges where electronic transport in undoped III-V nanowires are potentially hindered by stacking faults, point defects and surface effects due to surface roughness. In order to make progress in topological materials research, the extraction of mobility is an important step in electrically characterizing the material [38].

Mobility Extraction method for results analysis

This method is important to be mentioned as it was used in extracting the mobilities that are discussed later in the Results section. It is carried out by adopting the equation fitting method mentioned before. A Python code is utilized to average all the transconductance $g_m = \frac{dI_{SD}}{dV_{SD}dV_g}$ values for N points for the full V_g sweep range. From this averaging plots, a suitable max transconductance value g_{max} can be chosen from the respective front (FS) and back-sweep (BS) range of V_g. These values are then useful to separate the high-slope mobility region from the low-tail/sub-threshold mobility region as seen in Figure below. Then for both regions, a curve

can be fitted separately for Eq 5 to determine the mobilities in the two regions of the FS and BS plots. It might be first useful to start reading the Results section before reverting back to this method for reference. In Eq 5 the values for Capacitance C (as seen in table below) are difficult to determine for a SAG NW due to its complex geometry. Therefore they were obtained from a previous finite element SAG modelling [28] done by a past Qdev PhD student at Copenhagen. University.



	Capacitance (F)		
NW orientation	**L: 500 nm**	**L: 1 µm**	**L: 2 µm**
[100] / [010]	0.9 x 10^{-15} F	1.8 x 10^{-15} F	3.6 x 10^{-15} F
[1-10]	1.1 x 10^{-15} F	2.2 x 10^{-15} F	4.3 x 10^{-15} F

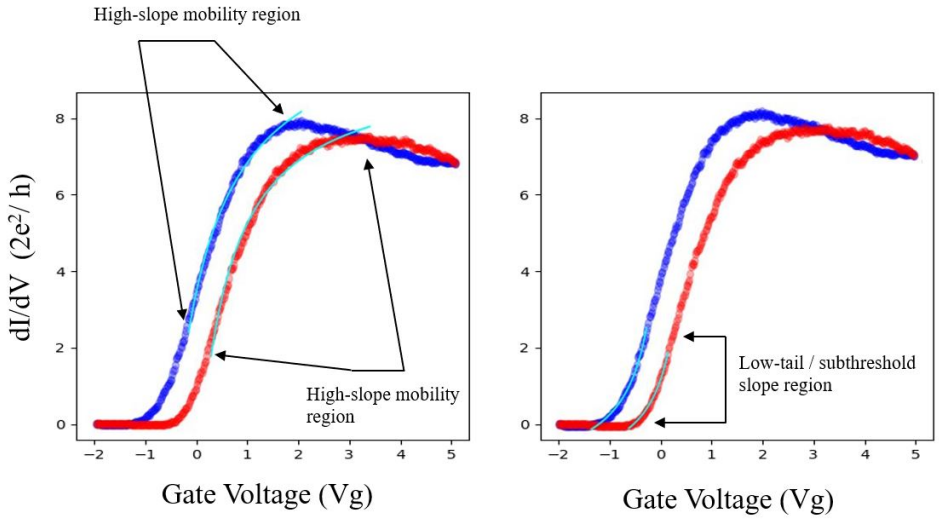


Figure 4: The top most plot displays the averaging distribution for g_m, from which the values for g_{max} from the peaks are chosen for FS (blue) and BS (red). The two plots in the bottom row consists of the G vs V_g hysteresis curves with the labelling for where the high-slope mobility and low-tail/sub-threshold mobility region lies. Also the capacitance C values used for the mobility extraction is given in the table (top-right).

c) Oxides and charge traps

A MOSFET's gate capacitance C has a strong dependence on the presence of a dielectric layer. A higher capacitance is obtained if the area A of the capacitor and dielectric constant κ is increased. Also, the thickness of the dielectric or gate oxide layer d between the metal gate and semiconductor should be minimal. These terms are dependent on one another through the following equation $C = A\frac{\kappa}{d}$. Further motivation for using high-k (also termed as κ) dielectrics/gate oxides is to ensure excellent gate control and to lower power consumption for preserving high speed operation of field effect devices. Also as discussed in the previous sub-section InAs nanowires face a reduction in mobility as a result of scattering due to surface roughness. This along with the formation of native oxides at the InAs/oxide interface degrades the semiconductor surface properties. Therefore, choosing an ideal gate oxide with high-k is a necessity [44]. A major issue that arises with alternative (non Silicon based) dielectrics is high leakage currents and defects which can trap electrons or holes.

A characteristic feature of NWFETs is the formation of charge traps at the interface or in the oxide layer. The presence of such traps can be unveiled when performing gate voltage V_g sweeps. These charge traps are known to capture and emit electrons, and are highly dependent on the rate at which V_g is swept. Ultimately, this gives rise to the hysteretic behaviour observed in conductance G-V_g measurements as seen in $Figure$. Slow V_g sweep rates allows ample time for the traps to capture or emit charge (larger hysteresis), and faster sweep rates doesn't leave enough time for emission or capture processes to occur (lower hysteresis). An increase in the number of positively charged oxide traps results in an increase in net positive charge, and thus would cause a negative shift in threshold voltage V_t. Otherwise a net negative charge increase caused by additional negatively-charged interface traps or electron trapping in oxide, results in a positive shift in V_t. It was further concluded that a cooling down process along with gate potential modulation could effectively deactivate these surface traps. An inducing of high emission/capture barrier heights, significantly larger than kT would help freeze these trap states[45]. Certain processes are also adopted during the NW growth or fabrication process to remove native oxides and the consequent manifesting of trap states. For example, thermal annealing or atomic hydrogen (a-H) treatment was incorporated during the SAG NW growth [29], and processes such as RF-milling were utilized during the fabrication procedure.

No extensive treatment will be given to the investigation of charge trapping phenomena in this thesis. However, it is important to note the origin of the dynamic hysteretic behavior observed in FET measurements which arise as a response to the electric potential, as it could potentially have a detrimental impact on the performance of transistor devices. Another possibility for improving the InAs-oxide layer interfacial quality would be with the inclusion of a protective barrier layer for the InAs channel. This will be explored in the next sub-section.

2.0.3 *SAG morphology with a thin-top barrier*

In order to inch closer towards the development of topological quantum computation, certain framework for nanowire (NW) networks and manipulation of braiding statistics is needed [46]. In light of this, much emphasis lies on the scalability of NW networks.

In-plane selective area growth (SAG) technique has proven to be a promising scalable approach for achieving NW growth. It employs parallel growth to the substrate which depends on a template or mask to selectively grow one or more semiconductor materials on top of another. The benefits from this technique is that it allows for better flexibility of the NW network designs that can be achieved, with the preferred design being written and etched directly onto a mask. As a result, complex structures can be grown and scaled. Furthermore, the growth is confined within the mask, thus maintaining a (quasi) one-dimensional structure along the nanowire axis and constant cross-sectional size [47].

The focus is the growth of InAs NWs on $[100]$ Gallium Arsenide (GaAs) susbtrates. If the NW is grown directly onto the substrate, a network of dislocations form at the interface due to the lattice mismatch that is present between the InAs NWs and GaAs substrate. The mismatch is close to 7.2%. This can ultimately have detrimental effects on the carrier properties in the InAs transport channel. To circumvent this problem, one or more buffer layers can be grown in between the channel and the substrate to reduce the lattice mismatch and improve interfacial quality. This enhancement of interface quality occurs through partial elastic strain relaxation. The SAG heterostructure of the InAs NWs used for the experimental work in this thesis follows closely to that of the recent paper 2021 paper by $D.Beznasyuk, et.al$. This consists first of a primary GaAs(Sb) buffer layer growth within the predefined trench in the mask opening on the GaAs substrate. The Sb acts as a surfuctant by promoting favorable growth kinetics for smooth buffer growth. Subsequently, a second buffer layer of $In_xGa_{1-x}As$ is grown on top of the GaAs(Sb) layer. This layer reduces the lattice mismatch between the InAs channel and GaAs(Sb) layer. This layer holds alot of importance within this SAG structure as it effeciently traps misfit dislocations at the InGaAs/GaAs(Sb) interface, leaving the InAs mainly dislocation free. Also the $In_xGa_{1-x}As$ buffer layer should strike a fine line with its composition. Very high In composition could result in the buffer layer conducting too much (loses insulation properties), and too less of In would mean the layer loses its ability to reduce the lattice mismatch between the transport channel and GaAs(Sb) primary buffer layer. Finally, the InAs channel is capped onto the InGaAs buffer layer as seen in (a) of Figure 5. The uniformity of the growth largely depends on the selectivity window for the growth of InAs and GaAs in the molecular beam epitaxy (MBE) system, where the upper and lower bounds are set depending on the temperatures and critical growth fluxes used. More information on this can be found in [48]. (c) and (d) of Figure 5 show EELS and GPA rotational maps adopted from [29] to give an example of how the In and Ga relative composition in the

NW is displayed, and how misfit dislocations formed at the InGaAs(buffer) and GaAs(Sb) buffer interface, are observed.

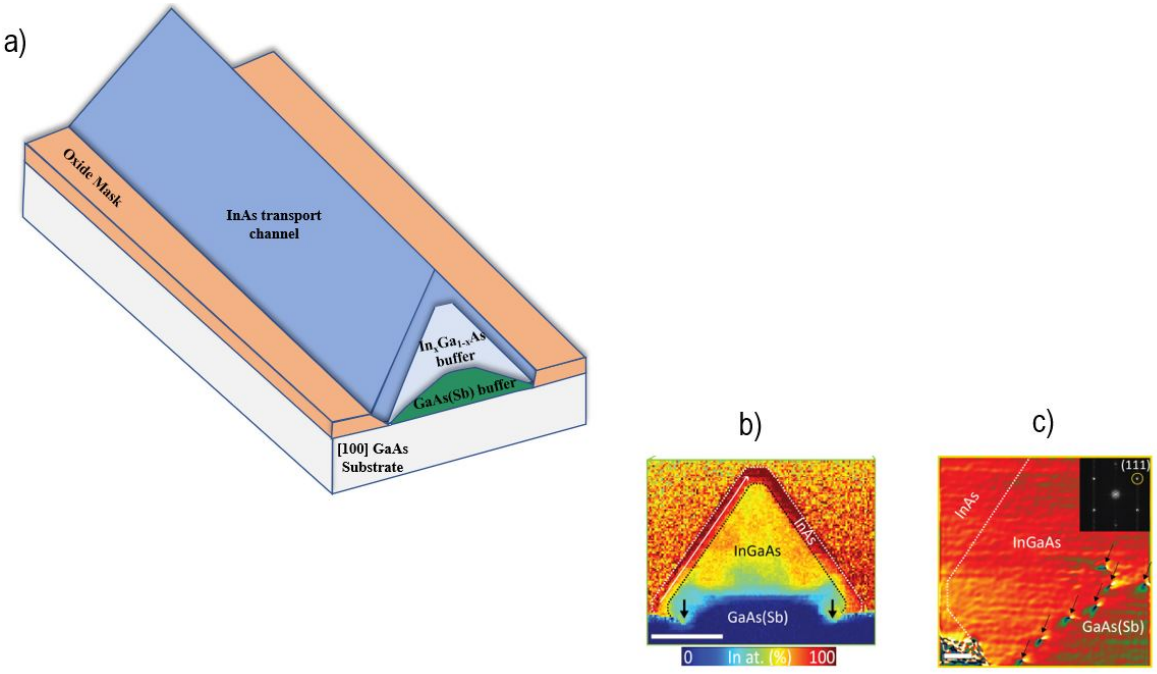


Figure 5: (a) Shows the SAG NW as described with the two buffer layers and transport channel. Images (b) and (c) have been taken from [29]. (b) shows the EELS map displaying the In composition in the NW relative to Ga with a percentage scale bar (c) consists of a GPA map where arrows point out the misfit dislocations that form at the InGaAs (buffer) and GaAs(Sb) buffer region interface

One of the main purposes of this Thesis was to add a modification to the SAG heterostructure just described. So for this thesis work, a few samples had an additional thin (10 nm) $In_xGa_{1-x}As$ layer grown on top of the InAs channel. The reason for this is due to the surface states that the InAs nanowire and poor interfacial quality. The wavefunctions of the electrons residing near the surface could potentially be drawn partly into the barrier layer and away from regions of interface scattering (i.e surface roughness). The motivation and premise for incorporating a $In_xGa_{1-x}As$ top-barrier layer for this research was taken from 2016 *Shabani, et.al* [49]. In that study, researchers incorporated a InGaAs-InAs-InGaAs quantum well for a 2-dimensional electron gas (2DEG) heterostructure. They discovered that for a critical thickness t of the InGaAs layer (barrier) the wavefunction decay of the electrons in the active InAs region was less abrupt, and overlapped to an extent into the barrier region. By moving the charge distribution away from the surface, there would be less chances for the electrons to encounter scattering potentials. However one has to investigate further the impact the thickness of the barrier has on the charge density near the interface. High t could cause too large of a wavefunction overlap into the barrier region (low mobility region because of less In composition), and could lead to a reduction in mobility. This approach of using a thin layer of InGaAs or InAlAs as a barrier, has been investigated in the past with numerous 2DEG systems [50, 51], but not yet with SAG heterostructures.

2.0.4 *Schrodinger-Poisson Comsol model*

An important method used for a better understanding of the FET measurement results obtained at the Qdev/Microsoft Lyngby labs is with the assistance of computer simulations. Hence, Schrodinger-Poisson (S-P) equations for the SAG model were solved self-consistently to reveal the conduction band energy E_c profile, electron densities n, and subband occupation. The simulations were performed by using the semiconductor and electrostatics modules provided by the finite-element modelling software, COMSOL [52].

Few things to note is that the Comsol models were devised to represent $[1\bar{1}0]$ NWs with diameter $d = 265nm$, and $[100]/[010]$ NWs of $d = 235nm$. For simplicity, the orientation dependent crystal lattice is not taken into consideration here. The only focus is on the dimensions, angle of top facets with substrate, and the GaAs(Sb)-$In_xGa_{1-x}As$-InAs-$In_xGa_{1-x}As$ layers with their respective compositions. More information with how these compositions were chosen is discussed in the initial part of the Results section. Figure 6 shows the models for $d = 235nm$ and $d = 265nm$ with variations: no barrier and with the top-barrier. The model labelling in the figure will be used throughout the thesis:

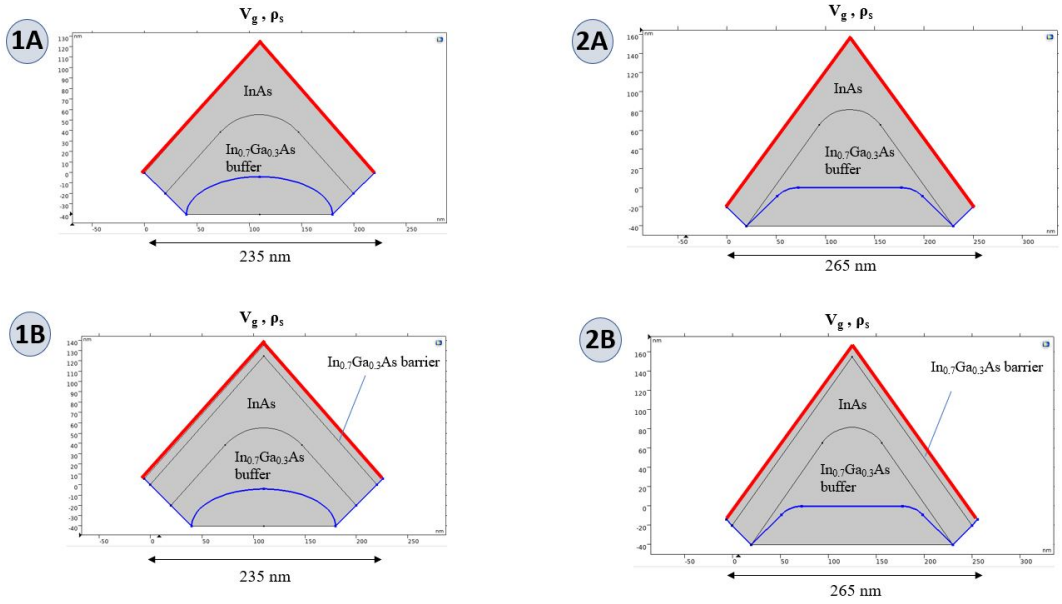


Figure 6: Simulation models are labelled as following: 1A ($d = 235nm$, no barrier), 1B ($d = 235nm$, with barrier), 2A ($d = 265nm$, no barrier), 2B ($d = 265nm$, with barrier). The boundaries marked red are the regions where V_g and ρ_s are applied, and the blue marked boundaries are the insulated boundaries. To note: The region below the insulated boundaries is GaAs(Sb) first buffer layer which isn't included in the simulations as it is assumed to be acting as a insulator.

NW models 1A and 1B have top facets (marked red) have a 45^o angle with the substrate, and 2A and 2B with to 54^o angle facets. The geometry V_g sets a Dirichlet boundary condition on the top facets of the models. This is to match the top-gate which was fabricated for the FET experiments. Comsol provides an external node within the modelling interface to simulate the metal-gate (Titanium-Ti) and a thin dielectric oxide (Hafnium oxide-HFO_2) without having to externally build it into the geometry. This can be done by further

inputting important parameters: metal-gate work-function: ϕ_m, and dielectric permittivity ϵ, the dielectric layer thickness t. The rest of the boundaries Also the effects of a surface-charge density ρ_s will be investigated where its assigned to as a dirichlet condition at the same facets where V_g is assigned. ρ_s was taken to be $3 \times 10^{12} cm^{-2} eV^{-1}$ [53] from recent literature for InAs nanowires. This surface charge was kept constant for all models unless stated otherwise.

The S-P simulations were performed for temperature $T = 7K$ and with respective layer compositions as show in the figure. The bottom-most buffer layer $GaAs(Sb)$ was not simulated for simplicity as it acts mostly as an insulator with the sole purpose of providing lattice match between channel and substrate. All the material parameters used for the simulations are displayed in the table in Figure 7.

Material Parameters	InAs	$In_{0.7}Ga_{0.3}As$ (buffer)	$In_{0.7}Ga_{0.3}As$ (barrier)	Dielectric (HFO_2)	Metal gate (Ti)
Relative permittivity ε	15.15	14.3	14.3	24	-
Electron affinity χ	4.9 eV	4.65 eV	4.65 eV	-	Work function (Φ): 4.33 eV
Effective density of states in conduction band N_C	3.11 x 10^{14} [1/cm^3]	5.68 x 10^{14} [1/cm^3]	5.68 x 10^{14} [1/cm^3]	-	
Effective mass m_{eff}^*	0.023 m_e	0.03437 m_e	0.03437 m_e	-	

Figure 7: Table with the material parameters used which were adopted from [54, 55]. The parameters $\epsilon, \chi, m_{eff}^*$ are composition dependent parameters. N_C is composition and temperature dependent.

The simulations were carried out in two steps:

(I). Using the semiconductor module, the Poisson equation is first solved for all the models

$$\nabla \cdot (\epsilon \nabla V) = -q(p - n + N_{D^+} - N_{A^-}) = \rho \tag{6}$$

where ϵ is the permittivity, V the total electrostatic potential of system, q the elementary charge, n and p the electron and hole densities respectively, N_{D^+} and N_{A^-} being the ionized donor and acceptor densities respectively. Also the total charge $\rho = \rho_n + \rho_s$ where ρ_n is the local space charge density of the system. We assume that only the conduction band electrons contribute to the band bending in the semiconductor at low temperature, in light of the nature of charge transport at the metal gate/InAs surface. Hence the simulations were only done for the majority charge carriers. The carrier densities in Eq(6) are related to the quasi-Fermi energy levels with the following equation

$$n = N_C F_{1/2}\left(\frac{E_{F_n} - E_c}{k_B T}\right) \tag{7}$$

where N_C (T dependent parameters from literature) is the density of states in the conduction band, $F_{1/2}(\eta)$ the Fermi-integral of order $1/2$ and approaches e^{η} when $\eta \to -\infty$, E_c being the conduction band edge, E_{F_n} the electron quasi-fermi level, k_B as Boltzmann constant, and T being the temperature. The conduction band energy in Eq(7) is related to the electrostatic potential V as follows:

$$E_c = -\chi - qV \tag{8}$$

where χ is the electron-affinity for the material. An assumption is also made in the Comsol semiconductor module that any donors will be fully ionized as there is no doping included in the model. These equations are then self-consistently solved over a finite mesh to estimate n and V.

A simulation convergence issue (ability for simulation to arrive at an answer below error tolerance) emerges due to the exponential dependence of the carrier densities on the temperature. For sufficiently low temperatures and large electric fields, the electron densities vary sharply with position. For example, the electron density varies by 2 orders of magnitude per nm [56]. As this effects the convergence of the system, a suitable low T of $7K$ was chosen where the simulations for the system converges correctly. In comparison to the temperature used in the actual FET experiments of $1.7K$, this accounts to an energy difference of about $0.5meV$. For simulation purposes this is acceptable and suffices. First the electron density is computed for $T = 300K$, after which multiple steps need to added in the Comsol interface where each step acts as an initial condition for n for a lower temperature step such that it self-consistently arrives at a solution for $T = 7K$. From here, a V_g sweep was done where the total charge density at different V_g values provides an initial charge density for the Schrodinger-Poisson self-consistent solver.

(II). We enter the second part of the simulation which utilizes the Schrodinger-Poisson equation multiphysics interface in Comsol. Within this interface there is a coupling between the electrostatics interface and the Schrodinger equation interface to model charge carriers in confined systems. The conduction band energy E_c profile from the previous part of the simulation contributes towards the potential energy term in the Schrodinger equation. Then the weighted sum of the probability densities of the energy eigenvalues of the Schrodinger equation contributes towards the space charge density in the electrostatics.

We now solve Poisson's equation again with an initial estimate from the first part of the simulation for ρ. The electric potential V here takes into account the V_g boundary conditions that imposes Fermi level pinning E_{fn} from the previous simulation. Thus we have V which must contribute towards the potential energy term in the Schrodinger equation as $-e\phi(x,y,T)$. (x,y) as we are only considering a 2D model with translational symmetry along the z-axis. So the following is the Poisson's equation

$$\nabla^2\phi(x,y,T) = -\frac{1}{\epsilon_0\epsilon_r}\rho(x,y,T) \tag{9}$$

where ρ is the charge density initial condition from the prior simulation, ϵ_r the relative permittivity of the the various layers in the SAG Comsol model, and ϵ_0 being the vacuum permittivity. Now the electrons are to be confined within the 2D model, therefore a boundary condition is provided for the wavefunction such that $\Psi = 0$ on all the outmost boundaries of the SAG model. The Schrodinger equation which describes the electrons confined within the model reads

$$-\frac{\hbar^2}{2m^*}\nabla^2\Psi(\vec{r}) + (V - e\phi(x,y,T))\Psi(\vec{r}) = E\Psi(\vec{r}) \tag{10}$$

where V is the confinement potential of the structure. Once again, we consider the NW to run an infinite length along the z-axis. Hence the wave function can be written as

$$\Psi(\vec{r}) = e^{ik_z z}\psi(x,y) \tag{11}$$

Equation 11 into 10, we get the following 2D differential equation

$$-\frac{\hbar^2}{2m^*}\nabla^2\psi(x,y) + (V - e\phi(x,y,T))\psi(x,y) = E_0\psi(x,y) \tag{12}$$

with $E = \dfrac{\hbar^2 k_z^2}{2m^*} + E_0$. By solving the last equation we obtain a first set of self-functions ψ_i and self-energies $E_{0,i}$ for the system. Another thing to note is that the $L.H.S$ of equation 12 receives potential energy contributions from the respective conduction band energy profile of the previous simulation. Also a total contribution to the potential energy is also taken with the respective effective masses m^* of the various layers (buffer/channel/barrier) in the model.

Now that we have all the needed elements, the electron density associated with the occupation of each of the states can be computed:

$$\eta(x,y,T) = \sum_{i=1} N_i F_{-1/2}\left(\frac{E_F - E_{0,i}}{k_B T}\right)|\psi_i(x,y)|^2 \tag{13}$$

where $N_i = g_i\sqrt[3]{4N_C}$, and E_F the Fermi energy, and g_i the degeneracy factor which is a factor of 2. This equation describes the density of electron gas at a point (x,y) at the temperature $T = 1.7K$. η corresponds to the electron probability density or the summation of probability of finding the electron in the coordinates (x,y) inside the 2D quantum wire model in each determined state ψ_i with energy $E_{0,i}$. Now once the probability density is calculated from Eq 13, a new profile for the total charge density of the system is obtained given by

$$\rho_{new}(x,y,T) = e[N_d - \eta(x,y,T)] \tag{14}$$

Now by solving Poisson's equation 9 and with the corresponding charge density profile, a new potential $\phi_{new}(x, y, T)$ is obtained, which again contributes to the potential term in the Schrodinger equation. Then the solution for Eq 12 provides the system with a new set of eigenfunctions and eigenvalues ψ_i^{new}, E_i^{new}. This set is associated with a new electron density profile η_{new} relative to each state of the system's occupation. Thus this self-consistent method is repeated iteratively until the absolute value of the difference between the potential terms of two successive self-consistent steps falls below a certain threshold/tolerance $|U - U_{old}| < 10^{-6}$ eV, where $U = V - e\phi(x, y, T)$. Hence, the system obtains self-consistency in order to determine the eigenstates/eigenvalues, electron probability densities, and subband occupation [57].

The finite element model simulations for the models were performed with 30 maximum iterations of the self-consistent method and 10^{-6} as the absolute tolerance. The mesh elements for the various models are as follows: **1A** (*1208510 triangular shaped mesh elements, 7863 edge elements, and 10 vertice elements*), **1B** (*1378512 triangular shaped mesh elements, 11307 edge elements, and 13 vertice elements*), **2A** (*1133875 triangular shaped mesh elements, 8993 edge elements, and 11 vertice elements*), **2B** (*1332852 triangular shaped mesh elements, 12899 edge elements, and 14 vertice elements*).

Part II

PART II

3

SAMPLE PREPARATION & DEVICE FABRICATION

3.0.1 *Sample preparation*

The SAG NWs are grown in a MBE system and consist of a Zinc-Blende face centred cubic (FCC) crystal structure. An advantage of using the MBE is the growth process purity and the prevention of unwanted precursor chemicals from being attained into the process. Also the materials are epitaxially grown directly onto the substrate without the need for complex chemical reactions. Lastly the whole procedure finally allows for in-situ growth monitoring with processes such as reflection high-energy electron diffraction (RHEED) which enables great control over growth rates and composition with a slow layer-by-layer growth. The MBE growth process for buffered SAG nanowires will not be a focus of this thesis. It can be found in [24].

The general synthesis process for a SAG NW is as following. In brief: (1) A semi-insulating substrate of a chosen substrate is prepared (2) An oxide (SiO_x) layer is deposited (3) A mask is then fabricated through a standard electron beam lithography (EBL) process (4) Prepared mask is etched into the oxide layer (5) Substrate is fully cleaned of impurities entered in through the fabrication process (6) Selective-area growth of first buffer layer GaAs(Sb) is done (7) Second buffer layer (InGaAs) is grown (8) Buffer layer is capped with the transport channel: InAs. The growth of the top-barrier which is not seen in the Figure is also grown, but for a few samples.

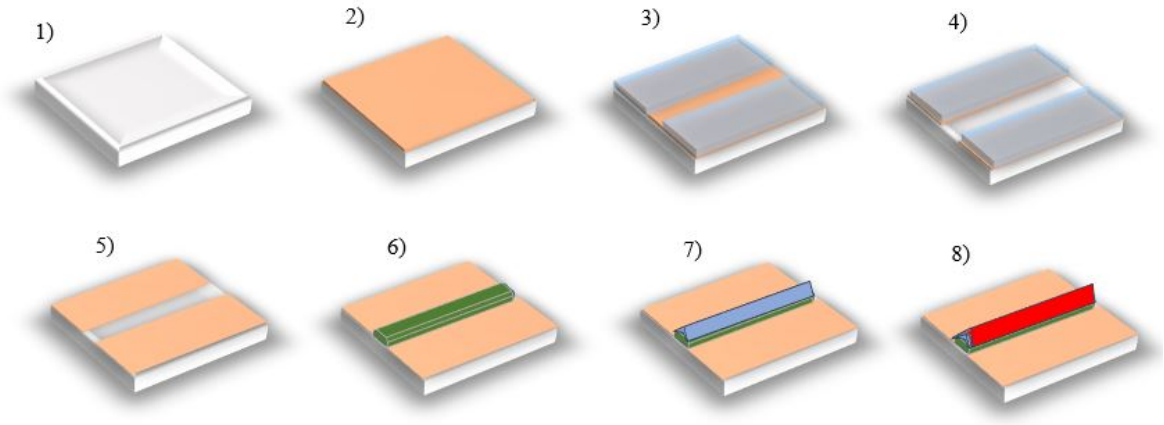


Figure 8: SAG nanowire synthesis steps schematic (1-8).

NW growth for the samples used for this thesis were grown by *Daria Beznasyuk* from the Qdev/Microsoft growth group at the University of Copenhagen. The exact growth process for the SAG NWs in this thesis can be found in [29]. Only differences to note are the different growth temperatures used in the paper which leads to ambiguity. To be clear the following are the growth temperatures that were used in the MBE system - GaAs(Sb): 670^oC, InGaAs (buffer): 580^oC, InAs channel: 535^oC, InGaAs (top-barrier): 535^oC. Once the NW growth is complete, the sample is then prepped for device fabrication.

3.0.2 *Device Fabrication*

3.0.2.1 *Electron Beam Lithography*

Electron beam lithography is an important technique in nanofabrication that allows for patterning arbitrary submicron scaled features. It basically consists of a scanning electron microscope (SEM) that is equipped with a pattern generator and beam blanker [53].

A design is first prepared through a software, whilst a thin layer of polymer material known as the resist is spin-coated onto the chip (containing NW sample) in a clean-room. The positive resist usually consists of polymers (long chain of molecules) which are monomerized upon exposure to high-energy electrons. For obtaining high-resolution features, electron scattering is taken into consideration. Once the electrons come into contact with the resist, they break up the polymer chains leading to broadening of the beam after every contact. The forward scattering can be reduced by increasing the incident electron energy and decreasing thickness of the spin resist. The high-energy electrons easily pass through the resist and penetrate deeply into the substrate, after which they reflect and reemerge from the surface, hence exposing the resist. The backscattering of electrons can be compensated by software simulation.

With post-exposure, the chip is taken into the clean-room for development by placing it in a solvent. The irradiated bits of the polymer film are dissolved and removed after being placed in solution, while the rest is left intact. The chip is rinsed in a neutral solution for stopping further development. Care is taken to carefully monitor the duration that the chip is developed in the solvent as it may lead to over-development of the electron-beam exposed pattern, which could lead to further problems in later stages. Also, the choice of polymer resist and chemical developer is important.

After the chip wafer is cleaned, it is placed into a thin film deposition chamber. Here the chip is covered by a thin layer of metal or other material. There are multiple options by which the thin film can be deposited such as through magnetron sputtering, electron beam evaporation or thermal evaporation. The material film is deposited onto the previously exposed/developed areas of the substrate, whereas everywhere else contact is prevented with presence of the resist. Tilt and rotation can be provided for the sample which allows the forming of various shadowed patterns, soft edges and more. Lastly, the final step is known was lift-off where the polymer film and

unwanted metal is dissolved/removed by following a set of small steps (acetone bath, sonication, etc). In other words, the material is lifted-off the substrate, leaving the metal on only the previously exposed regions. Another note: Choosing different resists and particular layering leads to better undercut design with different sensities to the electron beam whilst the resolution is preserved. These are the steps for fabricating metal electrodes for the NWs in order to realize FET devices. The fabrication steps are briefly depicted in Figure 9 below.

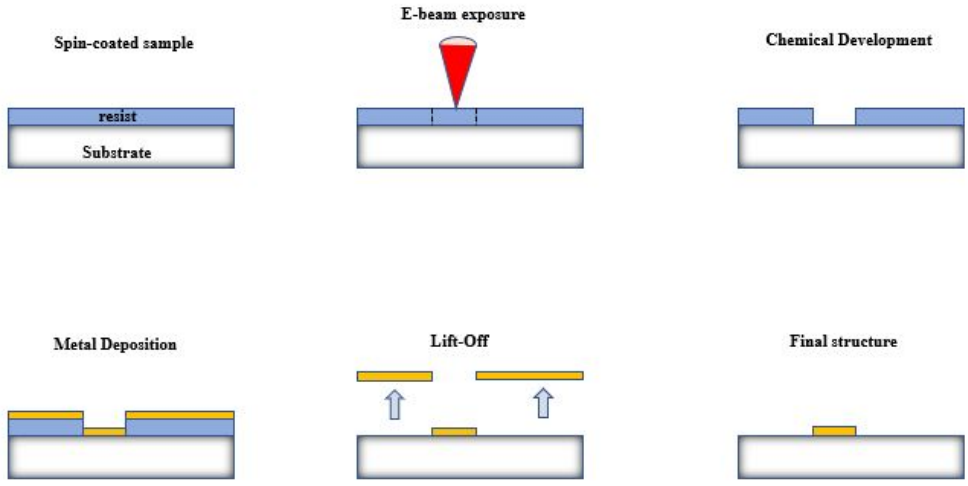


Figure 9: Device fabrication process from resist spin-coating to lift-off

3.0.2.2 *Fabrication Recipe*

The last discussion was a brief overview for how a typical device fabrication procedure is followed. The following is the particular fabrication recipe with specifications which were followed repeatedly for fabricating the devices:

- 5×5mm chip sample with SAG NWs grown is received. $[1\bar{1}0]$, $[010]$, and $[100]$ orientation NWs are chosen after checking under microscope.
- Contacts, alignment markers, & gates are designed for three NW channel lengths (L: 500nm, $1\mu m$, $2\mu m$) with a autoCAD software. These lengths were chosen due to previous promising results and difficulties in fabricating devices for lower L. Once done with design, the design files are then compiled to job files for EBL system
- Sample is cleaned [Acetone 5min / Isopropanol (IPA) 5min / Deionized water (DI)]
- Spin resist PMMA (400nm) is spin coated at 4000 rpm for 45sec and successively baked at 115^oC for 1.5min

- Exposure of Contacts and alignment markers with EBL is then done with *Elionix ELS-7000* EBL system. Inner features are exposed at $1000\mu C/cm^2$, $40\mu m$ write fields, 24000 dots, 500pA beam current, and outer features at $700\mu C/cm^2$, $250\mu m$, 20nA beam current.

- Exposed pattern is developed for 1min with 1:3 methyl isobutyl ketone (MIBK):IPA and then rinsed for 15sec in pure IPA. Then blown dry with nitrogen gun. Quality of development is checked under microscope. If any issues are present, sample is cleaned again and resist is spin-coated again. Last few steps are repeated again. If everything looks ok after checking with microscope, then next step.

- Sample placed in plasma asher for 1min (removes unwanted organic residue).

- Sample is then placed in the AJA Orion metal deposition system. First the sample is RF milled (15W, 18mTorr) with Argon for 2min (**samples without top-barrier**) or for 4min (**samples with top-barrier**). RF milling helps remove any native oxide formation at the NW surface. Once milling is done, the metal (Ti 5nm/Au 250nm) is deposited onto the sample substrate.

- The lift-off process is then initiated by placing the sample with deposited metal in acetone overnight for efficient removal. Using a pipette, the sample is gently flushed to remove some of the metal. Then it is placed in new/clean acetone solution and into a 15sec sonication process (80W), after which it is rinsed in IPA and DI. The sample is then checked with a optical microscope. If extra metal is still left (besides on the contacts), the lift-off process barring the overnight step is repeated.

- Sample is then plasma ashed for 2min

- Atomic layered deposition (ALD) method is used for depositing 10nm of Hafnium Oxide (HFO_2) onto the sample. (ALD methods for depositing the HFO has been known to reduce some of the native oxides of InAs, thus leading to improved electronic properties such as increased/decreased on-state/off-state current respectively, increased electron mobility, and increased transconductance [58]).

- (***Processes are repeated now for the metal top-gates***): Spin resist PMMA (400nm) is spin coated at 4000 rpm for 45sec and successively baked at 115^oC for 1.5min

- Top-gates are now exposed with EBL. Inner features are exposed at $1000\mu C/cm^2$, $40\mu m$ write fields, 24000 dots, 500pA beam current, and outer features at $700\mu C/cm^2$, $250\mu m$, 20nA beam current.

- Exposed pattern is developed for 1min with 1:3 methyl isobutyl ketone (MIBK):IPA and then rinsed for 15sec in pure IPA. Then blown dry with nitrogen gun. Quality of development is checked under microscope. If any issues, prior steps are repeated. Otherwise, go to the next step.

- Sample placed in plasma asher for 1min

- Metallization for top gates (Ti 5nm / Au 250nm) done (**without RF milling step**)

- Lift-off processes are repeated as previously enlisted, then checked with microscope.
- Plasma ashed for 2min.
- **Sample is now ready for wire-bonding**

3.0.2.3 *Wire-Bonding*

This is the middle step which is needed to prepare a wiring system for our chip sample in order for us to be able to tune the Fermi level within the NW, and for the sample to have a suitable platform to hold it safely in place.

An FS Autobonder with Aluminum wire is used for this purpose. The sample is lightly glued onto a daughterboard with silverpaint. Then the daughterboard is screwed onto the pad of a grounded gate platform on the FS Autobonder. Using a remote-stickpad system the wires can be bonded between the bonds of the daughterboard and the metallized bond bads on the outer boundaries of the sample chip (these are designed along with the contacts and gates). Finally as seen in Figure 10, once this process is done, the devices for the NWs on the chip have been fully fabricated.

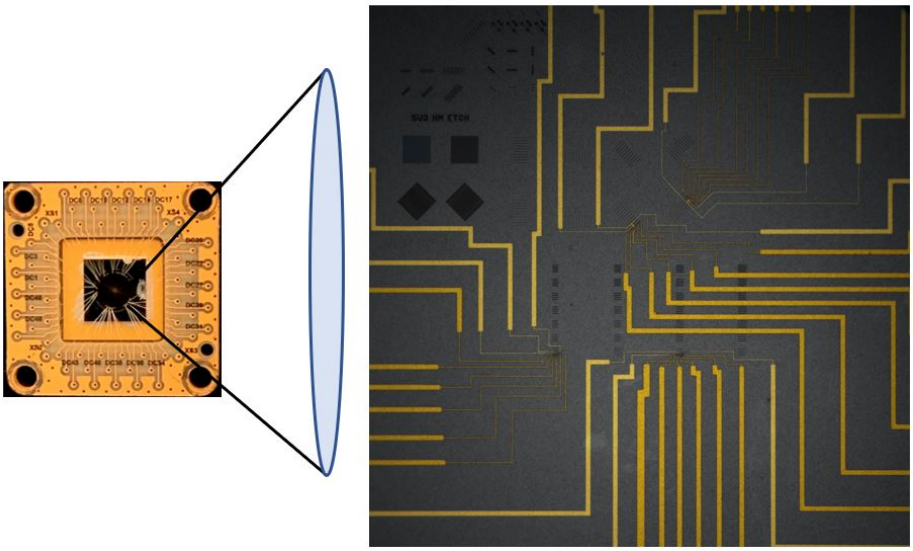


Figure 10: The daughterboard with chip sample post-wirebonding can be seen in the left image. It contains the fully fabricated NW FET devices as seen in the right image, which was taken with an optical microscope.

3.0.3 *Measurement Procedure*

3.0.3.1 *PPMS Dynacool system*

The wirebonded chip is now placed in a cryo-cooling system named as the Dynacool^{TM} Physical Property Measurement System (PPMS). It has a base-temperature of 1.7K, and additionally, magnetic fields can be

applied with a maximum limit of $9T$ with an atmosphere control system with minimum pressure of $10^{-4}Torr$ (high-vacuum).

A general schematic for the PPMS is displayed in Figure 11. The system configuration operates with a single two-stage pulse tube cooler. It relies on two plates at temperatures 45K and 4.2K respectively. The cooler stages as seen in the figure below are enclosed within a tank of Helium (He) gas and liquid environment called the ”bucket”. The cooler state operating at 45K is connected to the radiation (main) shield by conduction. Room temperature components (along with annulus shield) is connected to the main shield with solid contact. Now for the second cooler stage, it is contained in $150cm^3$ of LHe, to achieve a 4.2K temperature. A connection exists between the bottom of the liquid surrounded bucket and the 4K plate by solid contact. The 4K plate connects directly to the superconducting magnet. The heat transfer from the plate occurs through evaporation of the liquid from the bucket, which condensates onto the second stage. Thus, an equilibrium of such is achieved of the two phases. Achieving a 1.7K for the FET measurements is important. A capillary arriving from the bottom of the aforementioned bucket allows the flow of gaseous He into the sample chamber. The lowering of T below 4.2K is made possible due to the enthalpy difference between the two ends of the capillary and gas pumping from the annulus. For circulating the low-pressure He gas, an inter-connection of the annulus and bucket is present. This transfer results in the liquid/gas He mixture at 1.7K.

The Dynacool PPMS system contains three enclosures: the cryostat, cryopump/magnet cabinet, and the CAN module bay. The loading of the sample for performing the experiments is done within the cryostat, which further consists of a cryocooler, a superconducting magnet and sample chamber where the stick-like removable loading tool called the puck is attached as seen in Figure 12. A constant maintenance of He flow and temperature is done by the cryostat which is placed together within a cabinet that has an additional temperature control server and superconducting magnet power supply. Lastly, an external controller is present called the ”CAN module bay” which is accessible via ethernet in order to set conditions for the experiments.

Finally the wirebonded daughterboard (containing chip) is carefully loaded onto the puck and into the PPMS. Care must be taken so that the appropriate temperature and high-vacuum conditions are immediately set before experiments can commence. The sample is first degassed for 10 hours, usually over night. After degassing, BNC cables can be appropriately connected to the connections hub for the FET measurements to begin.

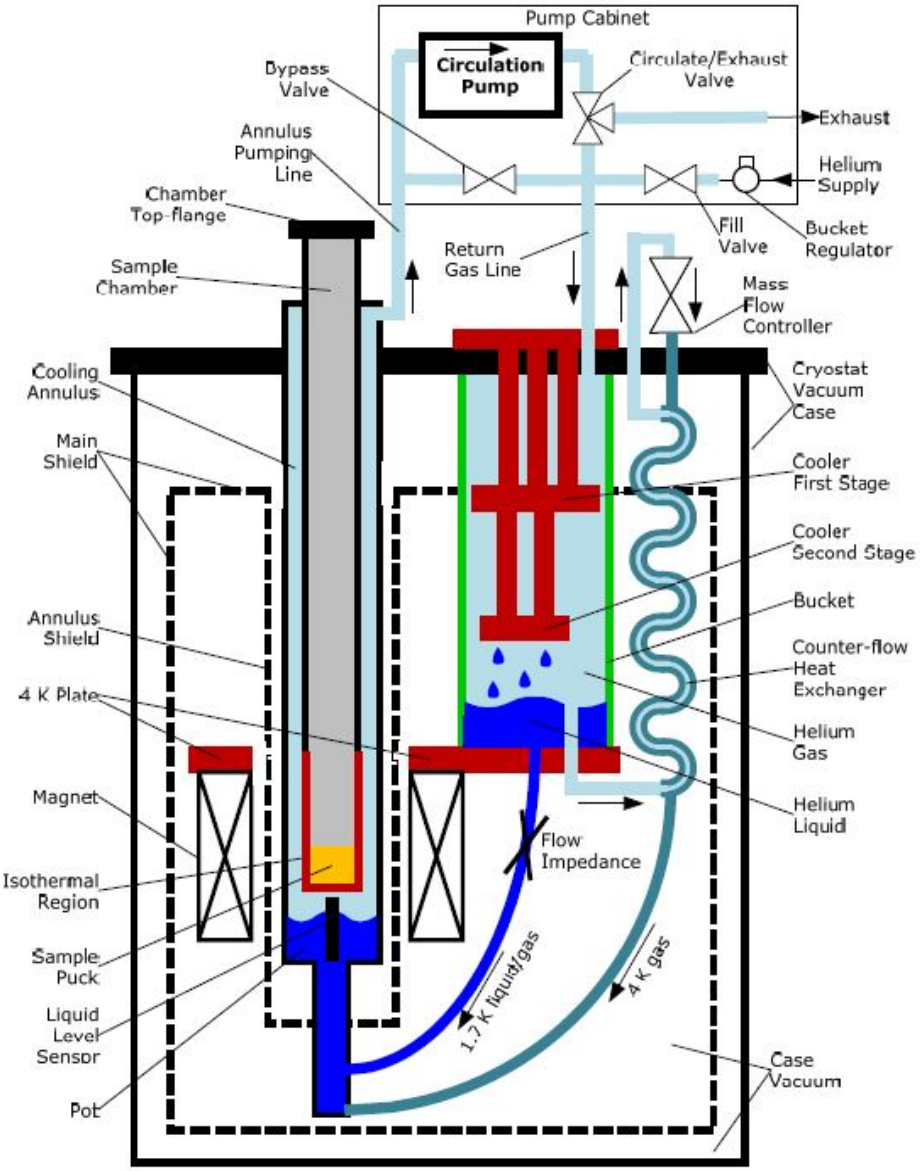


Figure 11: Schematic of the Dynacool PPMS system. Note the two dark-red labelled plates and the ”puck” where the sample is loaded and unloaded. Image is taken from [58]

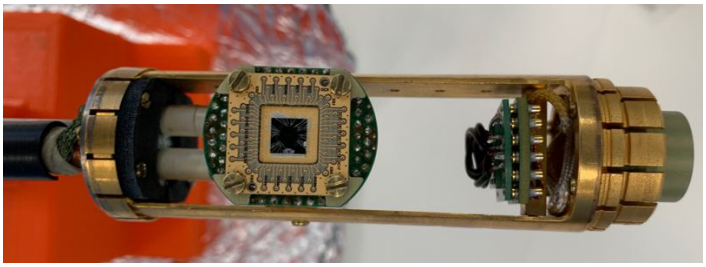


Figure 12: Daughterboard is screwed onto the ”puck” as seen in this image, before being loaded into the PPMS

4

MEASUREMENT METHODS

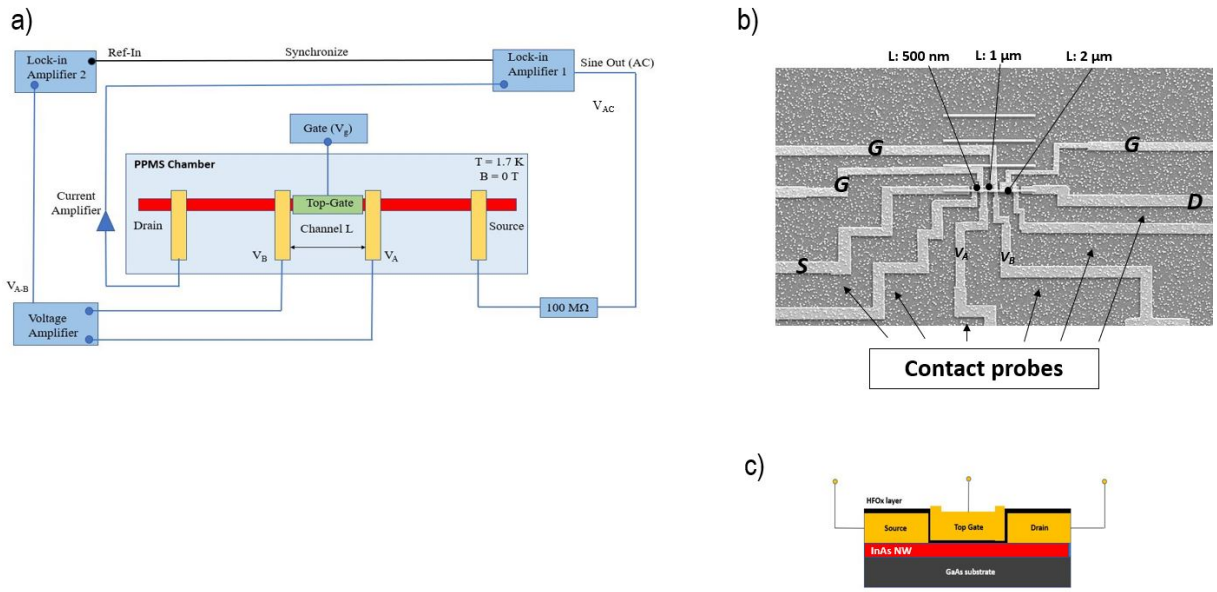


Figure 13: (a) 4-probe NW device in the PPMS chamber with connections made. (b) Originally a 9-terminal NW device from which 4 probes are chosen at a single time to perform a measurement. Here S/D is the source and drain, labelled G are the top gates. V_A and V_B can be interchanged depending on where which L is chosen to measure the potential difference between. (c) Side view of the fabricated NW device as it lies on top of the substrate.

Once the sample has been loaded into the PPMS and successfully degassed, BNC cables are appropriately connected to a MFP control box in correspondence with the wire-bonding scheme. The mode of measurement is a four-terminal/probe measurement which is preferable over a two-probe measurement due to negligible contact resistance being incorporated. The NW device as seen in Figure 13 (b) is originally a nine terminal device. However four probes are chosen to perform a measurement accordance with the channel length L used. Special packages, namely *qcodes* obtained from the institute are used in tandem with Python for the controlling the measurement equipment from the local computer located next to the PPMS. The measurement is performed at 1.7K with a standard lockin-in technique using a *SR830* lock-in amplifier. An AC amplitude signal of 1V is applied at a frequency of 120Hz from Lock-in 1. With another BNC cable, this signal is synchronized with Lock-in 2. The signal from Lock-in 1 is current biased through a $100M\Omega$ resistor and sent to the Source contact of the sample. Thus, the Source contact would be receiving an excitation signal of 1mV which is the source-drain voltage V_{sd}. The current (I) signal from the Drain is then sent through a *SP 1004* current amplifier which is used in order to amplify the signal for for readout of the final current I_f. The current amplification

I_{amp} used is 1×10^6. Using a *Keithly 2614B* instrument, the chemical potential or fermi-level E_f of the NW is tuned by modulating V_g of the top-gate located on the length of the NW channel L. Subsequently, the potential difference V_{A-B} (depending on which L was chosen) is fed to a voltage amplifier, where a V_{amp} of 500 is used. The final signal V_f can be read through Lock-in amplifier 2. This measurement sequence corresponds to the schematic in Figure 13 (a). Hence the conductance G can be calculated by $G = I_f / V_f$. The table in Figure 14 shows the parameters used for the experiment.

Experiment Parameters	Values
Source-Drain Voltage (V_{sd})	1 mV
Gate-Voltage min (V_g min)	-2 V
Gate -Voltage max (V_g max)	5V
Time delay (t)	0.4 or 1 sec
Frequency (f)	120 Hz
No. of data points	401
No. of iterations for Vg sweep (N)	3
Current amplification	1 x 10^6
Voltage amplification	500
Temperature (T)	1.7 K

Figure 14: Parameters used for measurement

For the four-probe measurement the V_g sweep was done by performing a front sweep (FS) from -2V to 5V and a back sweep (BS) from 5V to -2V. $N = 3$ iterations were used for the gate sweep, and for a range of 401 data points. These parameters were picked accordingly due to prior results for SAG NWs showing good results. Two V_g sweep rates where used by applying a time delay of $1sec$ or $0.4sec$. Time delay of $1sec$ corresponds to a slower sweep rate and $0.4sec$ for a faster sweep rate. The former was used for the NW devices which have a top-barrier, and the latter for the NW devices without the barrier. Finally for the G vs V_g curves, only the last of the three gate-sweep iterations were used as this allows the G profile to stabilize and provide a more accurate plot.

A total of four sets of four devices (in each set two devices for $[1\bar{1}0]$ NWs and one device each for $[100]$ and $[010]$ NWS) were fabricated at QDev, Copenhagen university and subsequently measured at the Microsoft lab in Lyngby. However only a few devices worked, and in random assortment. Therefore the measurement data for each orientation has been presented in the best possible way in the ”FET measurement results” sub-section.

Part III

PART III

5

RESULTS AND DISCUSSION

5.0.1 *Nanowire STEM and EELS mapping*

It was stated in the methodology section that $[1\bar{1}0]$, $[100]$, and $[010]$ NWs were chosen for fabricating FET devices with channel lengths L of 500nm, $1\mu m$, and $2\mu m$. Three samples were grown with a top-barrier on top of the InAs channel, and three were grown without to act as control samples for comparison purposes. HAADF-STEM images for $[1\bar{1}0]$ and $[010]$ NWs with a barrier can be seen in Figure 15. Its to be noted that the crystal morphology is the same for $[010]$ and $[100]$ NWs, hence both the orientations will be portrayed together. Also there are angle differences between the $[1\bar{1}0]$ and $[010]/[100]$ NWs such that the former has around a 54^o angle of its top two facets with respect to the substrate and the latter have 45^o angled facets.

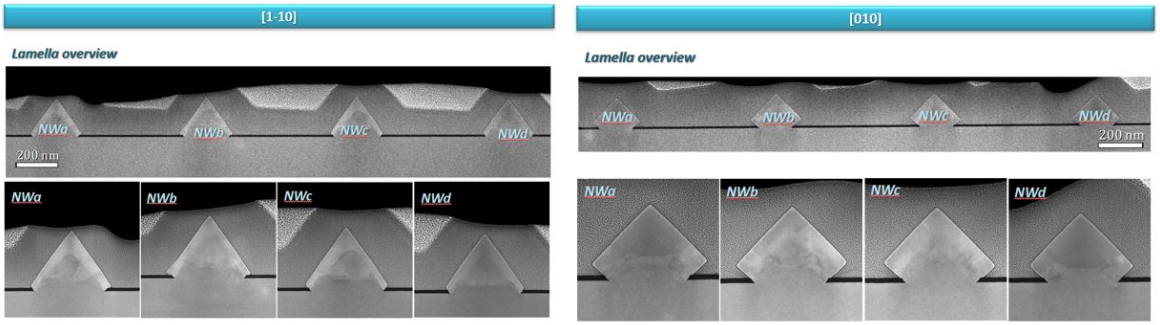


Figure 15: HAADF-STEM images provided by the nanoscience group at Catalan institute. A lamella (cross-sectional) cut was taken from the SAG NWS for the imaging.

The scale seen in the STEM images was used to estimate an approximate average diameter d for the NWs. As also mentioned in the Comsol modelling sub-section, the estimates for d are 235nm for $[010]/[100]$, and 265nm for $[1\bar{1}0]$ NWs. One can slightly discern shades within the STEM images which depict the buffer layers. To correctly obtain a composition map vs distance along certain axial cuts through the NW, Electron energy-loss spectroscopy (EELS) maps were incorporated. These can be seen in Figure 16 of the next page.

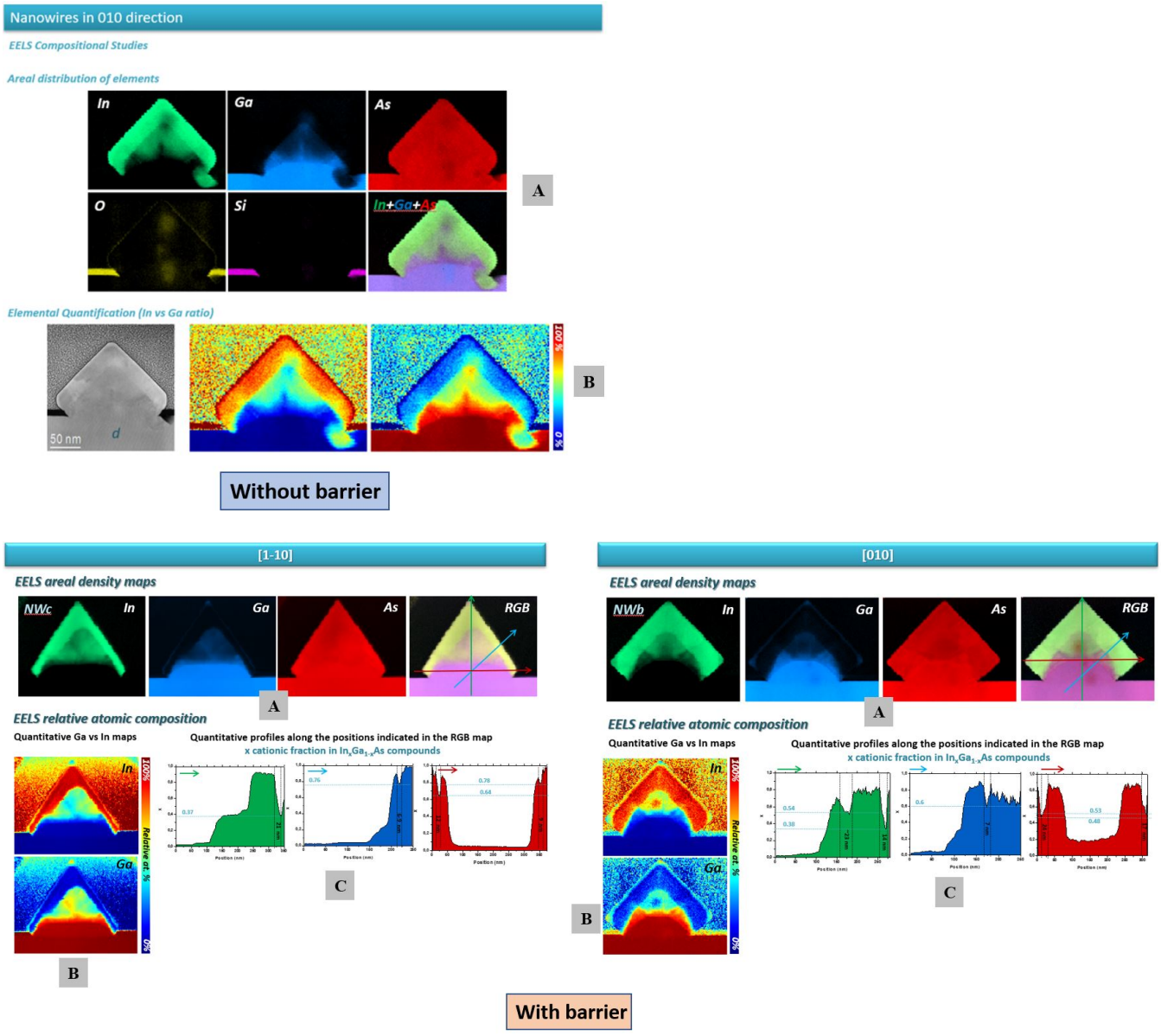


Figure 16: Top-most shows EELS composition maps for [010] NWs without barrier (maps for $[1\bar{1}0]$ were lost in the process). In the bottom row, the EELS maps for the two orientations with a top-barrier are shown. Maps consist of areal density (A), relative In vs Ga atomic composition (B) and maps showing the In composition as a function of position along the three coloured line cuts, labelled (C)

The maps portrayed in the EELS maps above show the composition of In, Ga, and As in the SAG NWs after growth. (Note: The top row for NWs without barrier is missing the $[1\bar{1}0]$ maps as they were lost in the process of obtaining the maps). The maps with the A labels represent the respective element material and its growth composition areal density map in the NW. The B labelled maps show a colour scale which displays the quantitative In relative to Ga ratio for one of them, and a Ga relative to In ratio map for its bottom counterpart. Hence in the maps, In composition is present more in abundance in the transport channel and for Ga, its presence lies mainly in the buffer regions (especially in the GaAs(Sb) buffer). In the second row (with-barrier NW EELS maps) the last of the A maps display three lines running through the cross-sectional area of the NW. These lines describe the quantitative In composition profile along the path of the lines. Just to be clear, x cationic fraction

in $In_xGa_{1-x}As$ is for the In composition, hence for Ga it would be $(1-x)$. This rule for material mixtures is described by Vergard's Law.

Now let's take an example and take a look at map *C* in the bottom-left for $[1\bar{1}0]$ oriented NWs with a barrier. For this particular example we shall focus only on the green In vs position chart in accordance with the green line seen in the RGB cross-section in the *A* areal density map (which shows the three lines cutting through NW). By tracking the green line from bottom to top, it displays negligible In composition in the first buffer region: GaAs(Sb) (as expected), then about a 0.37-0.4 In content in the second buffer region (InGaAs), which then continues till it reaches a peak in In composition (0.9) when the line reaches the position range in the InAs channel. As one can see, the transport channel region isn't a pure InAs channel but has about a 0.1 Ga composition present (therefore not pure InAs). It then shows a dip in the last region at the end which portrays the top-barrier region. Here it exhibits some Ga content at the top of the NW. This same method of reading the maps can be used for the other coloured line cuts. Using the EELS maps, a good approximation for $[1\bar{1}0]$ NWs (with barrier) would be a $In(0.75)Ga(0.25)$ in the barrier, $In(0.9)Ga(0.1)$ or close to pure InAs in the transport channel, and $In(0.4)Ga(0.6)$ in the 2nd buffer (InGaAs) region. As for [010]/[100] NWs in the bottom-right of the figure- $In(0.65)Ga(0.35)$ in the barrier region, $In(0.8)Ga(0.2)$ or close to pure InAs in the channel, and around a $In(0.65)Ga(0.35)$ in the 2nd buffer region. Now these are just estimates taken from the maps so that we can make assumptions on the impact it could possibly be having on the FET measurement results later in this section.

Its important to note, these maps only show composition changes at one particular cross-section along the whole axis of the NW. Although we would like to believe these changes remain constant throughout the NW's longitudinal axis, it is far from the case. If a different cross-sectional cut was taken from the NW, we would be left with a slightly different looking composition map. Perhaps the InAs channel would be more or less constant, but the buffer/barrier regions could show changes. Leaving this upto speculation and having uncertainty, makes it difficult to investigate the effect the various compositions have on the transport physics in the NW.

5.0.2 *Comsol Schrodinger-Poisson results*

Due to the difficulty in arriving at a good estimate for the In and Ga compositions in subsequent layers of the SAG heterostructure and to avoid complexity, the compositions were kept constant throughout the simulations for the models. So the buffer layer was set with a $In(0.7)/Ga(0.3)$ composition, the transport channel as pure InAs, and the top-barrier (when present), with the same composition as the buffer with $In(0.7)/Ga(0.3)$. This is for both the models of *d*, 235nm and 265nm. The influence of surface charge density is incorporated into all models except one, for comparison.

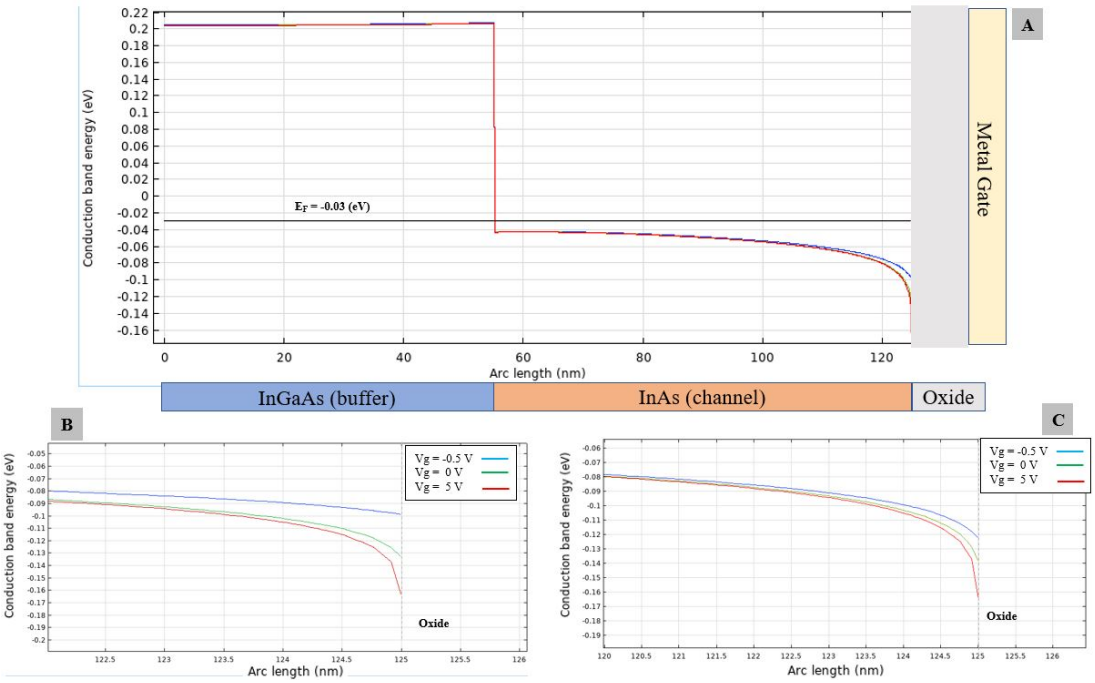


Figure 17: Plot A displays the E_c profile for 1A model (without barrier). Plot B is a zoomed in plot of the E_c edge at the oxide interface for $\rho_s = 0$ and plot C shows the same for $\rho_s \neq 0$

Simulations were first performed for model 1A (refer to modelling theory sub-section for labelling) at $7K$ without the top-barrier and surface charge density ρ_s set to zero. The conduction band profile E_c was generated for the 1A model system as seen in Figure 17. Plot A in the figure shows a vertical cut of the model where the InGaAs buffer extends from 0 to 55nm, followed by the InAs channel (thickness extending from 55nm to 125nm) which has a greater electron affinity χ than the buffer layer. The Fermi level E_f is approximately -0.03 eV. Two finite gate voltages V_g were used for the simulation $V_g = -0.5V, 5V$, and for when $V_g = 0$. As known, InAs exhibits a fermi level pinning above the conduction band minimum as reported in past literature. Band bending can be observed at the InAs/oxide interface which is determined by the offset between the conduction band edge and Fermi level set by the workfunction of the metal-gate (Ti).

The triangular well at the channel-oxide interface is an intrinsic feature of InAs NWs where a charge accumulation region would form at the surface due to the presence of donor like surface states. Plot B displays the conduction band edge for $\rho_s = 0$. Here, without any gate voltage applied ($V_g = 0$), the E_c edge lies approximately 0.1 eV below the E_f pinning as reported in various past literature for undoped InAs NWs. For $V_g = 5V$ and $V_g = -0.5V$, it is approximately 0.13 eV and 0.07 eV below the E_f respectively. Plot C is with the inclusion of a surface charge density where $\rho_s = 3 \times 10^{12} cm^{-2} eV^{-1}$ is used. This doesn't seem to have much of an effect on the degree of potential already formed for V_g of 5V, but pulls E_c further below by 5 meV when $V_g = 0$ and 20 meV for $V_g = -0.5V$. The presence of surface charge clearly manifests itself when negative voltages are applied, which decreases the potential and reverses the depletion effect that was previously present when $\rho_s = 0$. To get a clearer picture, a self-consistent Schrodinger-Poisson solver was

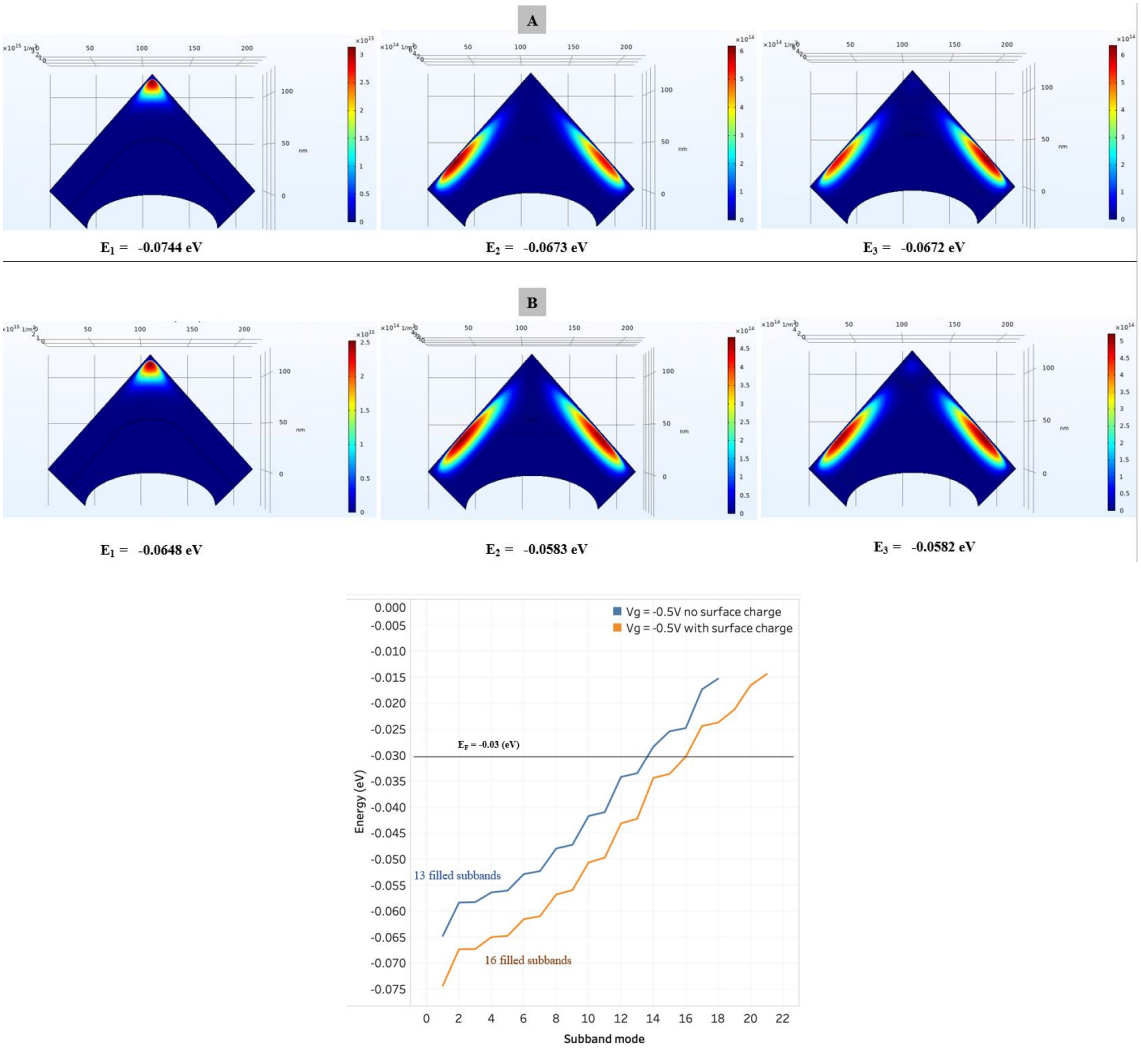


Figure 18: The first row (A) displays the probability density maps of the first three electron subbands being occupied for $\rho_s \neq 0$, and the same in (B) but for $\rho_s = 0$. XY dimensions in nm are show on the grid. The respective energy eigenvalues are provided under each map. The bottom-most graph plot shows the Energy vs subband occupation at $V_g = -0.5$ for NW model without (blue) and with surface charge (yellow). E_f being the Fermi level.

used to generate subband occupation for V_g of -0.5V at a fermi level of $E_f = -0.03eV$. We ideally want to investigate the low subband regime.

Figure 18 displays a map for the first there occupied modes and the respective probability densities for subband occupation within the 2D NW model. Only the confinement of electrons in the xy (vertical) axis is important due to the NW having translational symmetry along its length. It can be seen that the subband modes are mainly confined in the low effective mass InAs region (high χ) and not in the $In_{0.7}Ga_{0.3}As$ buffer region due to the large band offset. Row A probability density map in the figure is with surface charge and row B being without. Few things which can be observed here is the strong dependence on symmetry that the subband modes possess which exists along the centre of the NW cross-section. The first excited state E_1 exhibits s-type orbital character and with second E_2 and third E_3 excited states displaying p-type orbital character. 2-fold degeneracy is also present for modes E_2 and E_3 which are more or less equal in energies. Small differences between these energies would be due to presence of thermal energy provided by the $7K$ on the system. Also due to the increase

in interface potential in the presence of surface charge, the energies for the modes in row A are shifted to more negative values than for row B. Closely inspecting the subband maps in accordance with the colour scale for row A unveils a higher probability density for electrons being occupied in the three subbands in comparison to row B where $\rho_s = 0$. To be specific, approximately $0.5 \times 10^{15}/m^2$ more for E_1, $1.5 \times 10^{14}/m^2$ more for E_2, $1 \times 10^{14}/m^2$ more for E_3. This is a result of the positive surface charge attracting more electrons at the accumulation region formed at the InAs-oxide interface. Finally the bottom-most plot in Figure 18 shows the subband occupation at $V_g = -0.5V$ where 16 electron subbands are filled with $\rho_s \neq 0$ and 13 filled subbands for $\rho_s = 0$. This is evident by the plot's step-like features below E_f. The 2-fold degeneracy also partly exists for modes E_2E_3, E_4E_5, after which the thermal energy starts to smear the step pattern by introducing energy differences. It is thus sensible to state that more negative gate voltages would be needed to deplete the system of subbands filled by the electrons. With certain negative V_g values, a conducting channel could also perhaps be opened for hole majority carriers. This however was not investigated in this thesis and will be a a future topic to perform simulations for.

We have now so far briefly investigated how the presence of a finite surface charge density has impacted the 2D NW model. Now in the context of FET experiments, it is evident that the presence of surface donor states play an important part in characterizing the transport properties in a NW. Particularly, the presence of these fixed charges makes it more difficult to deplete or effectively turn-off the transport channel, as it would require overcoming these positively charged states.

The prior NW model 1A corresponds to the $[010]/[100]$ NWs with its same diameter of $235nm$. Now for comparison the larger diameter $265nm$ model 2A (without barrier) was included into the investigation. This will be in correspondence with the $[1\bar{1}0]$ oriented NWs. From here onwards all models will be simulated with

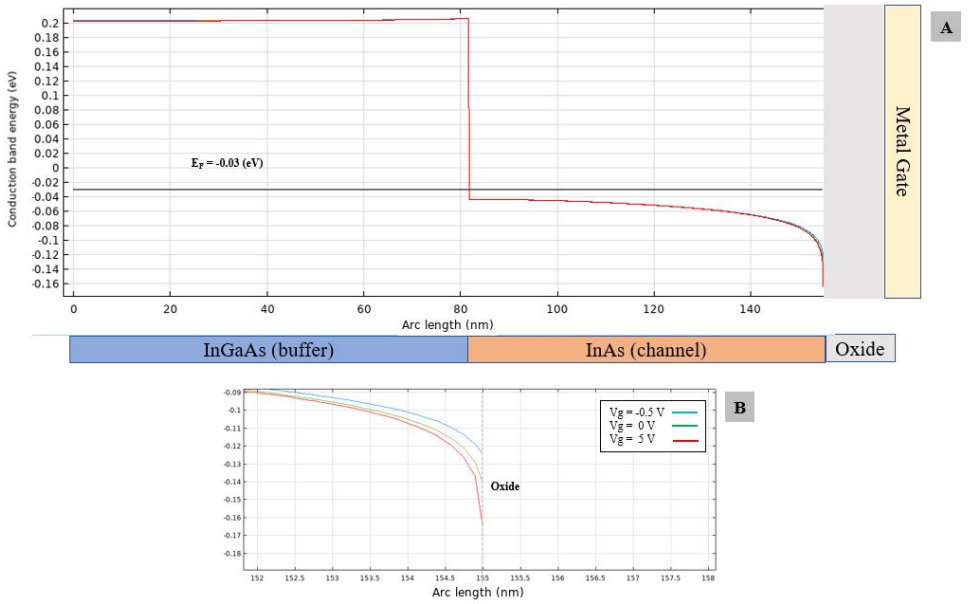


Figure 19: Plot A displays the E_c profile for 2A model of $d = 265nm$ (without barrier). Plot B is a zoomed in plot of the E_c edge at the oxide interface with finite surface charge density $\rho_s \neq 0$.

a finite surface charge at its top facets. Figure 19 shows an E_c plot for NW model with $d = 265nm$. The features of the plot doesn't change much and only consists of miniscule changes with the E_c edge relative to the E_f pinning. As a reminder, the In and Ga compositions are always kept constant (same). There are however some changes in the width of the quantum well (QW) present. This small difference in QWs formed can be observed when closely compared with model 1A's E_c plot in Figure 17. With NW 2A in figure above, the QW is approximately 73nm in width, as compared to NW 1A's width of 70nm. This is the case when taking a vertical cross-sectional cut through the centre of the NW. If a cut through the side facets is taken, the symmetrical QWs on the sides are a width of 27nm for NW 2A and a width of 30nm for NW 1A as seen in Figure 29 given in the Appendix.

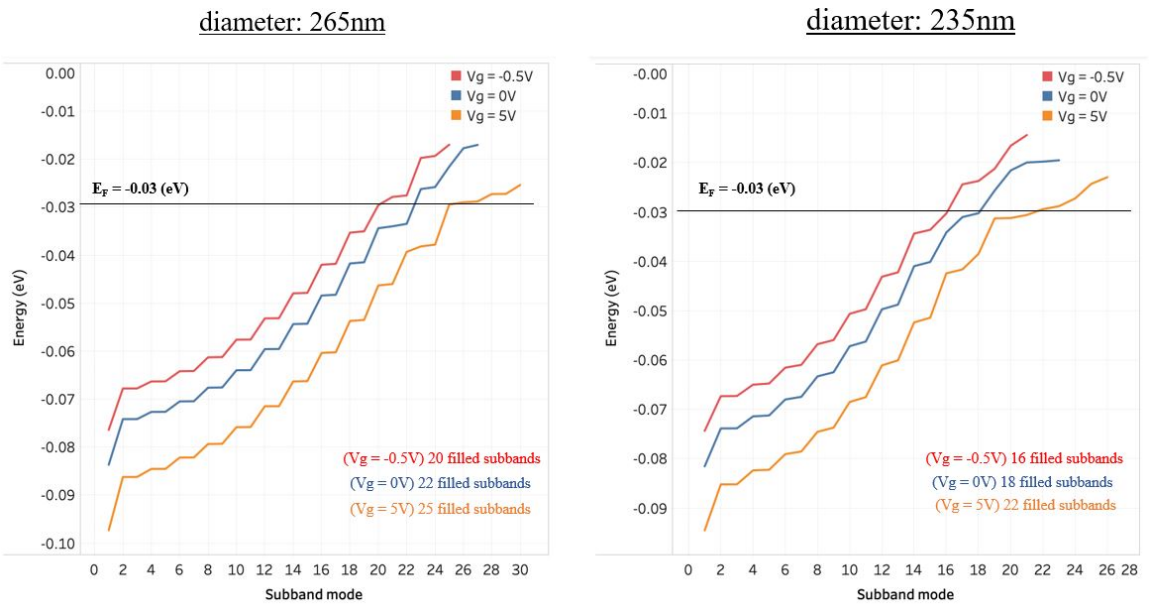


Figure 20: The graph on the left shows Subband occupation vs Energy in the $d = 265nm$ NW model 2A for $V_g = -0.5V, 0V, 5V$. The plot on the right shows the same for the NW model 1A of $d = 235nm$.

Subband occupation plots in Figure 20 above clearly shows direct proportionality between the number of subbands occupied with the diameter of the NW [59]. NW 2A with larger d exhibits higher subband occupation below E_f for every each of the three gate-voltage values of ($V_g = -0.5V, 0V, 5V$). NW 2A (larger d) also has its first subband filled at a slightly more negative energy in comparison to NW 1A (smaller diameter). 2-fold degeneracy can once again be observed for subband modes E_2E_3, E_4E_5, and so on. However the step-like pattern seems more distinguishable for 2A than 1A. This goes slightly in contrary to past reports of NWs with larger d exhibiting a reduced quantum confinement [34, 59], hence leading to more closely spaced subbands with less distinct step-patterns. The geometry used for the SAG NWs in this thesis however consist of a more complicated geometry. There could be a possibility that given the strong dependence of the triangular NWs on its symmetry, the reduced width of the QWs on the sides for NW model 2A could be having a stronger impact. Greater confinement in the sided QWs for NW 2A could be of more significance, than the confinement for

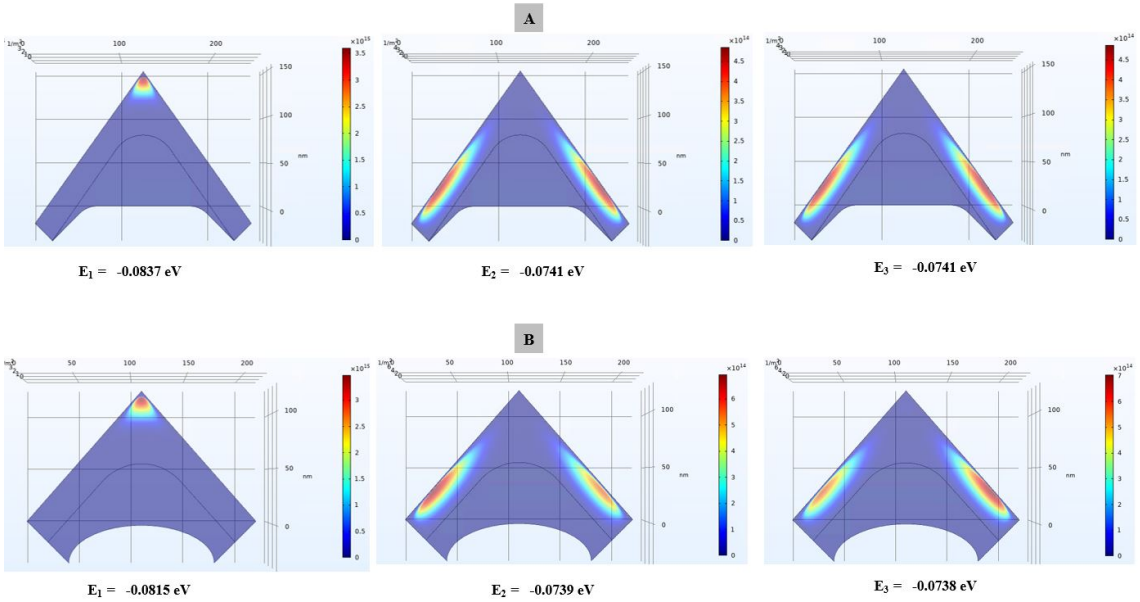


Figure 21: Probability density$1/m^2$ maps for electrons $V_g = 0$ is shown above for the first three subband modes with their respective energies. Here A represents the maps for NW with $d = 265nm$ and B represents NW with $d = 235nm$

the 1A NW in the vertical QWs. This explanation is only a speculation, and is further supported with the help of the subband probability density maps provided in Figure 21. Within these maps for E_2 and E_3 a reduced electron density can be discerned in the side QWs for the larger d NW. This along with the fact that the QWs on the side are thinner, could lead to a greater confinement. In the appendix, the maps for higher subband modes show that most of the electron probability density is localized in the side QWs for these triangular geometry NWs. Also, in the subband occupation plots in Figure 20 the energy differences between the non-degenerate subbands (E_1E_2), (E_3E_4), (E_5E_6) onwards, appear to be more closely spaced for NW 2A in comparison to NW 1A. This has been reported in past literature that NWs greater in diameters display closer spacing between occupied subbands. A resulting effect in FET experiments could mean the possibility of scattering effects between subbands which could ultimately decrease electron mobility, but there are also advantages as a larger d could mean less scattering events due to surface/interface roughness [40].

We finally move onto to the addition of a thin 10nm $In_{0.7}Ga_{0.3}As$ barrier layer on top of the InAs layer for the NW model. This was simulated for both the $d = 235nm$ (1B) and $d = 265nm$ (2B) NW models. However only 1B will be discussed for the large remainder of this subsection. The sole purpose now is to make a comparison with NW 1A which did not have the barrier. A finite ρ_s will still be included but this time on the top facets of the barrier region. The E_c profile was then simulated for NW 1B with the three gate-voltages once again. This is shown in Figure 22 in the next page.

Plot A in the figure portrays the same E_c minimum up until the barrier region where the separate profiles for the various gate-voltages can be distinguished. In this region the close presence of the metal-gate seems to have a great effect, where a positive V_g creates a large potential at the oxide interface. This could be the result of simulating a very thin layer next to the oxide/gate with a finite ρ_s. The E_c edge at the InAs/barrier interface

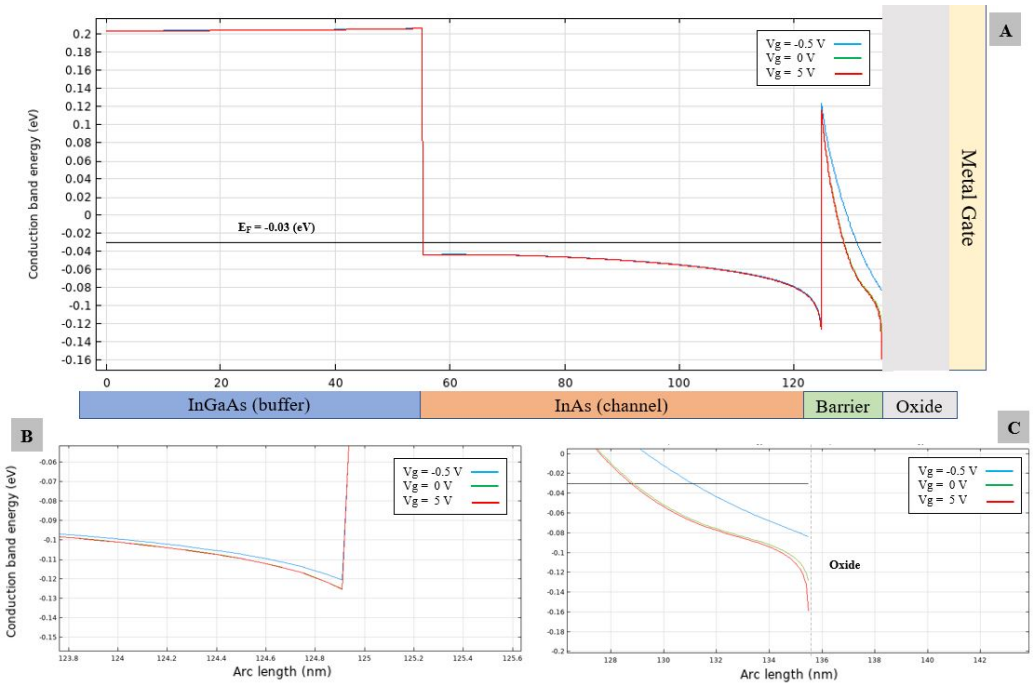


Figure 22: Plot A displays the E_c profile for NW 1B (with barrier). B is a zoomed in plot of the E_c edge at the InAs/barrier interface, and C shows a zoomed plot for the E_c edges at the barrier/oxide interface. In each plot there are three E_c profiles which correspond to the three values for $V_g = -0.5V, 0V, 5V$

however, lies close to -0.12 eV (0.09 eV below E_f pinning) without much change for the three V_g values. This is very different from the case without the presence of the barrier, where the potential which formed at the oxide interface displayed distinct changes with change in V_g. The barrier appears to have a stabilizing effect on the electric potential at the InAs interface.

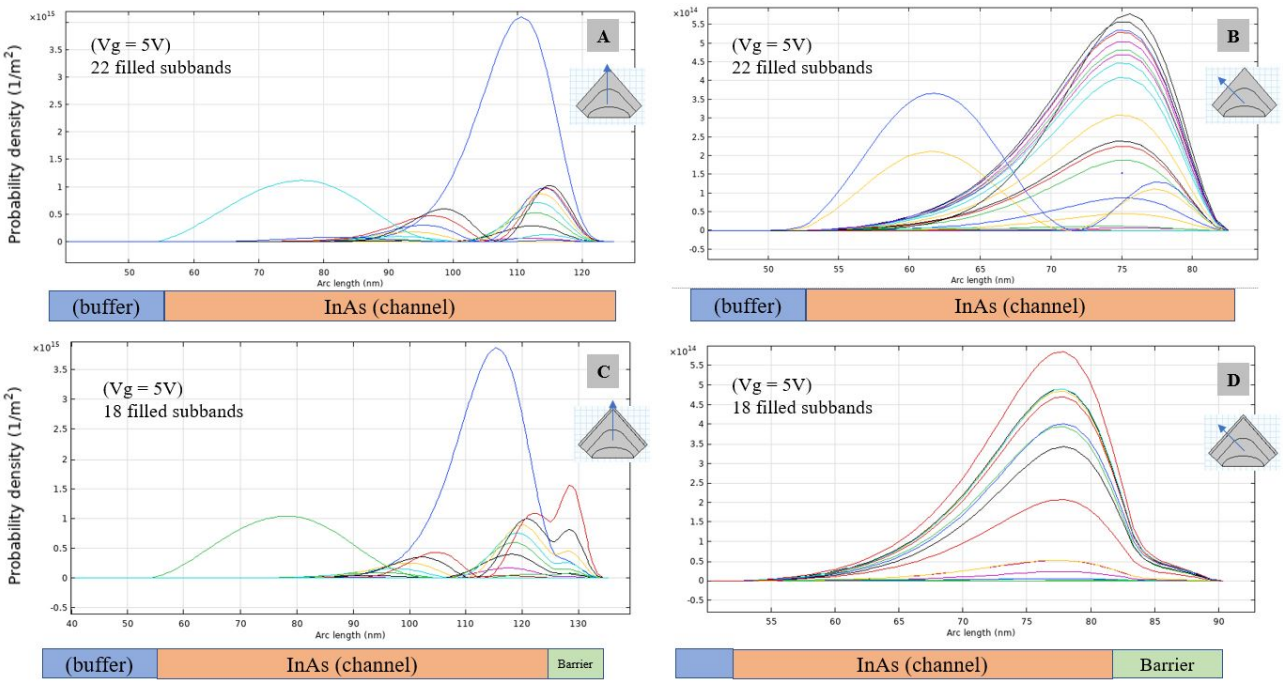


Figure 23: The above image consists of probability density plots where *A* and *B* consists of the vertical and side QWs for NW 1A (without barrier). *B* and *C* portray the same but for NW 1B which consists of a top-barrier. The barrier positioning is between 125nm to 135nm in *C*, and 82nm to 90.5nm in *D*. The small model diagram insets (with and without barrier) display a arrow in the direction of QW being portrayed.

We are now mainly curious about $V_g = 5V$, because for this case the the electron wavefunctions would be pulled closer to the gate due to the positive potential. Figure 23 shows the probability density plots where the top row plots *A* and *B* represent the QWs formed with the vertical and side cross-section (facet) regions respectively for NW 1A (without barrier). For all plots the number of occupied subbands is stated. This cannot be easily noticed from the Figure 23 as some of the electron densities vary between orders of 10^7 to 10^{13}. It is important to observe the nature with which the electron wavefunctions decay with and without the presence of the barrier. In plots *A* and *B* the wavefunctions decays near the would-be oxide region. This in reality would bring the charge density in close contact to interface scattering mechanisms or traps in the oxide or at the surface. But in plots *C* and *D*, the wavefunctions have a delayed decay response or overlap into the barrier region. This could have a positive effect on the transport properties of electrons at the InAs NW's surface. What is still left to investigate in the future is the critical thickness for the barrier, and the effects it has on the nature of wavefunction decay when it is changed.

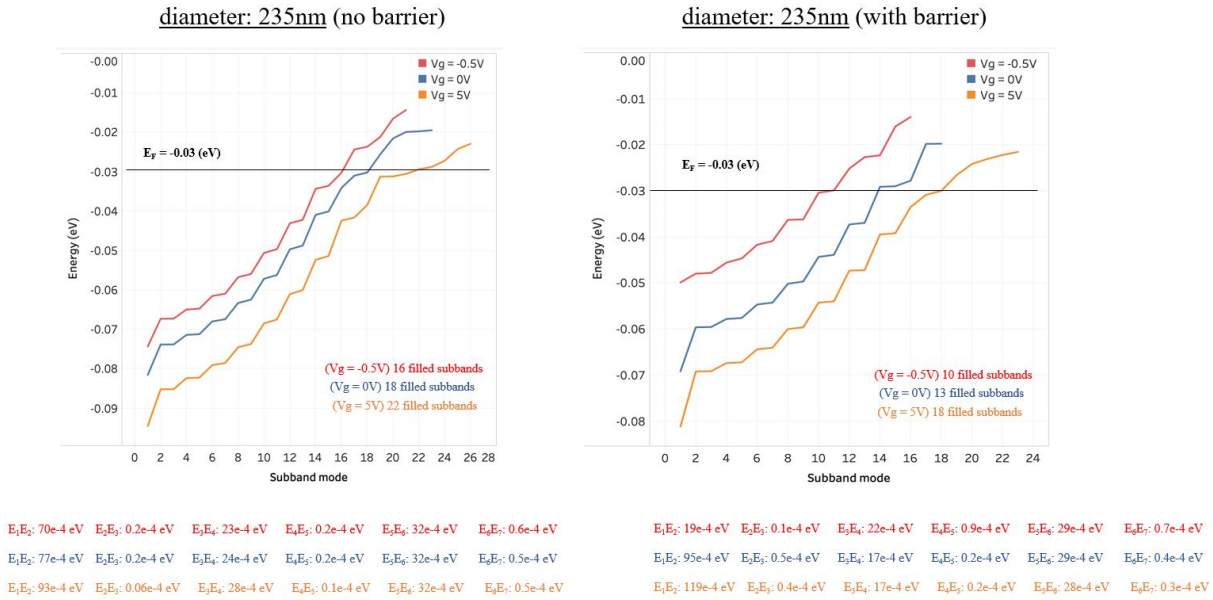


Figure 24: Energy vs subband occupation plots for NW 1A (no barrier) shown in left plot and for NW 1B (with barrier) shown in the right plot at $V_g = -0.5V, 0V, 5V$. Energy differences for first seven subbands shown underneath the respective plots.

Finally for this subsection we make a comparison for the NW models 1A and 1B in Figure 24. The energy vs subband occupation step plots were used to inspect the differences. Here as a result of including a top-barrier, the plot on the right shows lesser subband occupation in NW 1B and greater confinement than 1A. This shows we could ideally stay in the low subband regime within the same range of V_g as in 1A, when the barrier is present. Also lesser negative V_g would effectively deplete the NW when with the barrier inclusion. One could also slightly discern a more flat step-like plateaus for the plot on the right representing for the subband occupation with barrier. This is further supported by the energy differences provided at the bottom of the Figure. It shows a gradual presence of lower energy differences for the right plot in comparison with the left. A conclusion can be made that including a barrier for the model would more likely result in fewer subband occupation and better confinement, and with the added protection of preventing the charge distribution to lie too close to the NW surface. However, the overall geometry still plays a part and would have to be investigated properly as a whole. In the appendix, the energy vs subband occupation comparison plots were also provided between NW models 2A and 2B in Figure 30. Here also there's a lower subband occupation for NW 2B at the three gate-voltages, in comparison to NW 2A.

5.0.3 *Field-Effect Transistor Measurement results*

Finally for this thesis, FET measurements were performed on the three different NW orientations: $[1\bar{1}0]$, $[010]$, and $[100]$. The measurements were performed at low temperature as that largely helps to eliminate charge trapping and scattering phenomena that act with thermal activation. The devices which were fabricated for the NWs are shown in the Scanning Electron Microscope (SEM) images below.

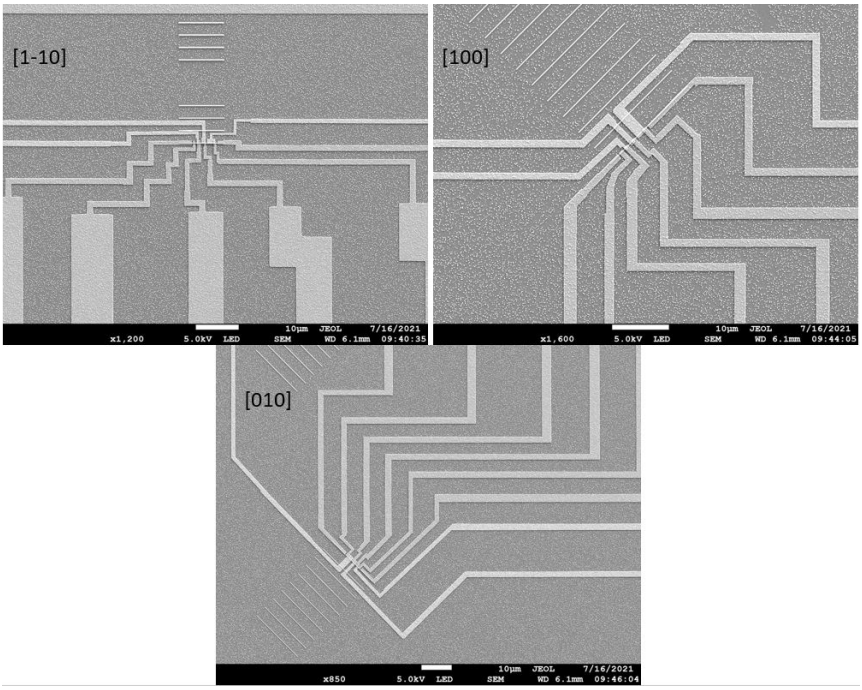
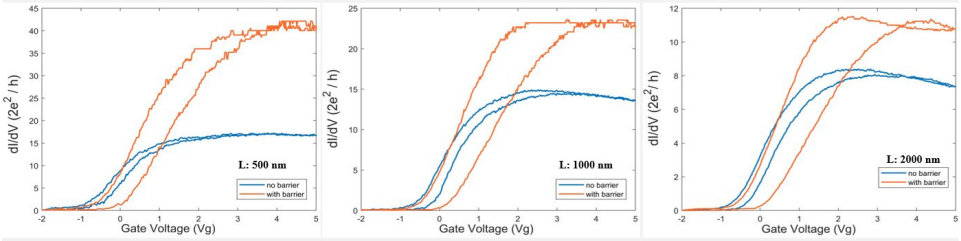


Figure 25: SEM images represent the 9-terminal FET devices where 4 probes were used at a single time for a measurement. Top-left is a device for a $[1\bar{1}0]$ NW, top-right for $[100]$, and bottom for $[010]$ NWs.

Four-terminal measurements were performed with three channel lengths (L: 500nm, $1\mu m$, and $2\mu m$) for the NWs with no-barrier and with the inclusion of a top-barrier. The measurements were performed at a base temperature of 1.7K. Please revisit the "Measurement methods" section for the procedure followed. The terms calculated are the front (μ_{FS}) and back (μ_{FS}) sweep field-effect mobilities which pertains to the electron accumulation region of the curve; additionally the low-tail or subthreshold region front/back sweep field-effect mobilities $\mu_{FS(L-tail)}/\mu_{BS(L-tail)}$ were determined which gives us an insight into the electron depletion or "tail" region of the curve, furthest away from the metal-gate tuning influence. Lastly the max transconductance for front/back sweep $g_{max(FS)}/g_{max(BS)}$ was calculated. The four devices which weren't included and were working are included in the thesis in Figure 31 and Figure 32.

[1-10]

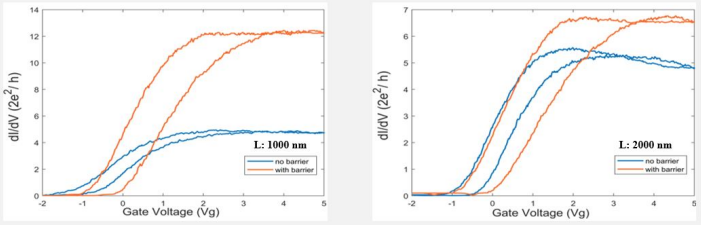


no barrier	with barrier
L = 500 nm	**L = 500 nm**
$\mu_{FS(H)}$ = 6900 cm²/V.s	$\mu_{FS(H)}$ = 10800 cm²/V.s
$\mu_{BS(H)}$ = 5550 cm²/V.s	$\mu_{BS(H)}$ = 6020 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 90 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 350 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 190 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 400 cm²/V.s
$g_{max(FS)}$ = 2.1 µS	$g_{max(FS)}$ = 2.49 µS
$g_{max(BS)}$ = 1.5 µS	$g_{max(BS)}$ = 2.12 µS

no barrier	with barrier
L = 1000 nm	**L = 1000 nm**
$\mu_{FS(H)}$ = 8460 cm²/V.s	$\mu_{FS(H)}$ = 14870 cm²/V.s
$\mu_{BS(H)}$ = 9770 cm²/V.s	$\mu_{BS(H)}$ = 8770 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 260 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 910 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 440 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 1320 cm²/V.s
$g_{max(FS)}$ = 1.2 µS	$g_{max(FS)}$ = 1.75 µS
$g_{max(BS)}$ = 1.3 µS	$g_{max(BS)}$ = 1.23 µS

no barrier	with barrier
L = 2000 nm	**L = 2000 nm**
$\mu_{FS(H)}$ = 11300 cm²/V.s	$\mu_{FS(H)}$ = 15300 cm²/V.s
$\mu_{BS(H)}$ = 9800 cm²/V.s	$\mu_{BS(H)}$ = 7600 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 300 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 420 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 520 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 430 cm²/V.s
$g_{max(FS)}$ = 0.52 µS	$g_{max(FS)}$ = 0.65 µS
$g_{max(BS)}$ = 0.5 µS	$g_{max(BS)}$ = 0.57 µS

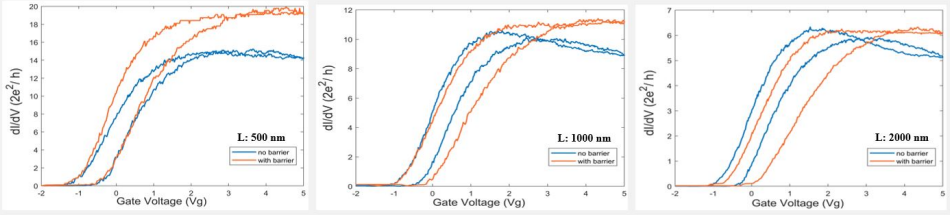
[100]



no barrier	with barrier
L = 1000 nm	**L = 1000 nm**
$\mu_{FS(H)}$ = 3550 cm²/V.s	$\mu_{FS(H)}$ = 9700 cm²/V.s
$\mu_{BS(H)}$ = 3760 cm²/V.s	$\mu_{BS(H)}$ = 5100 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 250 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 420 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 80 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 510 cm²/V.s
$g_{max(FS)}$ = 0.46 µS	$g_{max(FS)}$ = 0.85 µS
$g_{max(BS)}$ = 0.53 µS	$g_{max(BS)}$ = 0.79 µS

no barrier	with barrier
L = 2000 nm	**L = 2000 nm**
$\mu_{FS(H)}$ = 7980 cm²/V.s	$\mu_{FS(H)}$ = 7090 cm²/V.s
$\mu_{BS(H)}$ = 8330 cm²/V.s	$\mu_{BS(H)}$ = 5610 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 530 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 580 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 660 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 750 cm²/V.s
$g_{max(FS)}$ = 0.36 µS	$g_{max(FS)}$ = 0.39 µS
$g_{max(BS)}$ = 0.42 µS	$g_{max(BS)}$ = 0.36 µS

[010]



no barrier	with barrier
L = 500 nm	**L = 500 nm**
$\mu_{FS(H)}$ = 5680 cm²/V.s	$\mu_{FS(H)}$ = 9390 cm²/V.s
$\mu_{BS(H)}$ = 5730 or cm²/V.s	$\mu_{BS(H)}$ = 5500 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 460 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 680 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 450 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 890 cm²/V.s
$g_{max(FS)}$ = 1.42 µS	$g_{max(FS)}$ = 1.72 µS
$g_{max(BS)}$ = 2.01 µS	$g_{max(BS)}$ = 1.54 µS

no barrier	with barrier
L = 1000 nm	**L = 1000 nm**
$\mu_{FS(H)}$ = 10060 cm²/V.s	$\mu_{FS(H)}$ = 8000 cm²/V.s
$\mu_{BS(H)}$ = 7070 cm²/V.s	$\mu_{BS(H)}$ = 5500 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 660 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 990 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 560 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 1120 cm²/V.s
$g_{max(FS)}$ = 0.98 µS	$g_{max(FS)}$ = 0.91 µS
$g_{max(BS)}$ = 0.79 µS	$g_{max(BS)}$ = 0.81 µS

no barrier	with barrier
L = 2000 nm	**L = 2000 nm**
$\mu_{FS(H)}$ = 10500 cm²/V.s	$\mu_{FS(H)}$ = 8280 cm²/V.s
$\mu_{BS(H)}$ = 9620 cm²/V.s	$\mu_{BS(H)}$ = 5640 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 800 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 870 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 1050 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 640 cm²/V.s
$g_{max(FS)}$ = 0.65 µS	$g_{max(FS)}$ = 0.44 µS
$g_{max(BS)}$ = 0.57 µS	$g_{max(BS)}$ = 0.34 µS

Figure 26: The plots above display conductance G vs gate voltage V_g hysteresis plots for $[1\bar{1}0]$, [100], and [010] NWs. There are presented such that there is a direct comparison between the NWs with/without a barrier for each channel length L. Additionally the relevant FET measurement terms mentioned prior were calculated and are displayed in tables.

At first inspection of the G vs V_g curves, the plots for $[1\bar{1}0]$ with-barrier seem to exhibit the highest saturation conductance of all plots displayed, with around 40 ($2e^2/h$), 23 ($2e^2/h$), 11 ($2e^2/h$) for L of 500nm, 1μ, and $2\mu m$ respectively. Also the FET mobilities for the high-slope regions, which were calculated through the equation fitting method (*mentioned in FET mobility sub-section of Theory*) using equation 5, show a clear increase with the increase in channel length L for the $[1\bar{1}0]$ NWs (with and without barrier), and for other orientations without barrier. So why not the orientations without the top barrier? A reference can be made to the EELS maps in Figure 16 where the map for $[010]/[100]$ NWs displays about a $In(0.65)Ga(0.35)$ composition in the top-barrier. This reasonably high Ga composition could enhance surface roughness at the interface between the InAs channel and the top-barrier because of the increased lattice mismatch. This, coupled with the fact that the $[010]/[100]$ NWs possess a smaller diameter of 235nm, could also be resulting in enhanced surface scattering and subsequent mobility reduction [40]. Also the purpose of including a top-barrier seems to have only worked in increasing the field-effect mobilities for the $[1\bar{1}0]$ NWs than their other orientation counterparts. The aforementioned reasoning could perhaps be used to explain this by adopting the EELS maps once again for $[1\bar{1}0]$ NWs which seem to exhibit $In(0.75)Ga(0.25)$ composition in the barrier region. Firstly, this would be providing a better quality InAs/InGaAs(barrier) interface because of an increased lattice match. Also the Schrodinger-Poisson simulations incorporated in this thesis displayed wavefunction decay or overlap of the electron densities into the barrier region as reported in past literature [49, 50]. A barrier region composed of $In(0.75)Ga(0.25)$ would result in an effective electron mass of $0.03244m_e$ for $[1\bar{1}0]$ NWs and the barrier region $In(0.65)Ga(0.35)$ of $0.03631m_e$ for $[010]/[100]$ NWs. Thus, the charge density distribution overlapping into the latter would more likely result in a decrease in mobility. This is due to the inverse dependence of the mobility on the electron effective mass in a material. Also there is a good case for the high saturation conductance observed for the $[1\bar{1}0]$ NWs to be a result of high In content in the top barrier where a charge density overlap into that region could be leading to additional conduction. Now to move the focus to the low-tail or subthreshold mobilities $\mu_{L-tail(FS/BS)}$ for the front and back V_g sweeps. These values correspond to the efficacy of the channel depleting action of the gate. This means that the interface which the InAs channel has with the InGaAs buffer layer is of concern now. It could be said that the top-barrier inclusion doesn't have much of an effect on this tail region of the G plot anymore. All the devices seem to have pinched-off (effectively deplete the channel of electrons) except for the $[1\bar{1}0]$ NWs (with and without barrier) with L=500nm, the $[100]$ NW without barrier, and $[100]$ NWs (with and without barrier) for L=$2\mu m$. Also the general average of subthreshold region mobilites (FS and BS) is slightly higher for the $[010]/[100]$ NWs than the $[1\bar{1}0]$ NWs. This could be the result of a better lattice match between the InAs and InGaAs buffer layer interface for the $[010]/[100]$ NWs which have a $In(0.65)Ga(0.35)$ composition in the buffer. The $[1\bar{1}0]$ NWs exhibit a $In(0.4)Ga(0.6)$ composition in the buffer region. This would degrade the quality of the interface. These assumptions made so far are hard to fully support without devising a method to get a better picture

of the average composition through the longitudinal axis of the NW. Also the larger diameter d NWs in the Comsol simulations displayed larger subband occupation. This could possibly lead to inter-subband scattering, which also has to be take into consideration. However, it is known that the reduction in mobility due to surface scattering phenomena plays a stronger part in hindering carrier transport, which is increasingly observed in smaller d NWs. The highest front-sweep (FS) mobilities (high-slope region) can be noted as $14870 cm^2/Vs$ and $15300 cm^2/Vs$ for L of $1\mu m$ and $2\mu m$ respectively. These pertain to the $[1\bar{1}0]$ NWs. These mobilities are higher than the previously reported [28, 29]. The highest back-sweep (BS) mobilities also belong to the $[1\bar{1}0]$ NWs amongst all three orientations. The table in the figure below shows the average mobilities

Orientations	Average μ_{FE} (no barrier)	Average μ_{FE} (with barrier)
[1-10]	8630 cm^2/Vs	10560 cm^2/Vs
[100]	5905 cm^2/Vs	6875 cm^2/Vs
[010]	8110 cm^2/Vs	7050 cm^2/Vs

Orientations	Average $\mu_{L\text{-}tail}$ (no barrier)	Average $\mu_{L\text{-}tail}$ (with barrier)
[1-10]	300 cm^2/Vs	640 cm^2/Vs
[100]	380 cm^2/Vs	565 cm^2/Vs
[010]	660 cm^2/Vs	865 cm^2/Vs

Figure 27: The top table shows the average FET mobilities for the high-slope region and the bottom table the FET mobilities for the subthreshold slope region.

The max transconductance g_{max} is an important term in FET measurements which is an expression of the performance of the FET. It describes the ratio of the change in drain current with the change in gate voltage, whilst a constant source-drain voltage is maintained. g_{max} was determined as shown in the FET mobility theory subsection. The value for the determined g_{max} is the highest at $2.49\mu S$ for $[1\bar{1}0]$ NWs. Also, for all NW orientations, g_{max} decreases as L is increased. Additionally, the V_g sweeps (FS or BS) displaying a greater mobility (high-slope) exhibits the larger g_{max}.

We finally arrive at the glaring disparity of the G curves between the front and back V_g sweeps. This behaviour is the result of the modulation of charge traps FET channel when the sweep in V_g is performed. When V_g is swept up to positive values, just before the down sweep, the positive gate voltage causes the filling of traps with electrons that contribute towards an increased negative potential. Thus to cancel out this potential, a shifting in conductance occurs which is the form of the curve appearing at a more positive V_g value during the sweep down. This is the underlying reason behind the difference in G curves that appear in the plots. The hysteresis arises due to time lags between the capture and emission of interface states. Furthermore, the magnitude of the relative gate voltage shift (hysteresis) between the up and down sweep curves δV_g is an

indicator of the density of charge traps present at the NW surface/interface or in the oxide. From Figure 26, two observations can be made from the nature of hysteresis that has manifested in the G curves. Firstly, the hysteresis curves coincide for the plots without barrier (blue) and with barrier (orange) at certain regions for a particular V_g. This means that the trapping or de-trapping of electrons from the charge traps are occurring at the same rate and for the same magnitude of potential set by V_g. So the smaller hysteresis is inherent to all the plots for NW devices without-barrier (blue) is a result of a faster V_g sweep rate (time delay: 0.4sec) being used. The trap states are unable to respond to the quick varying potential. However the NW devices with-barrier (orange), a slower sweep rate was used (time delay: 1sec). Here the slow varying potential allows ample time for trapping or de-trapping of electrons to occur, hence the larger hysteresis, because new charge traps are activated which were otherwise frozen during the faster sweep rate. Also in the plots, a keen observation can be made of the general increase (even if slight) in hysteresis with increase in channel length L. This makes sense as there are more possibility of charge traps of various forms being encountered by the electrons along its path through the longer travel distance to the drain contact.

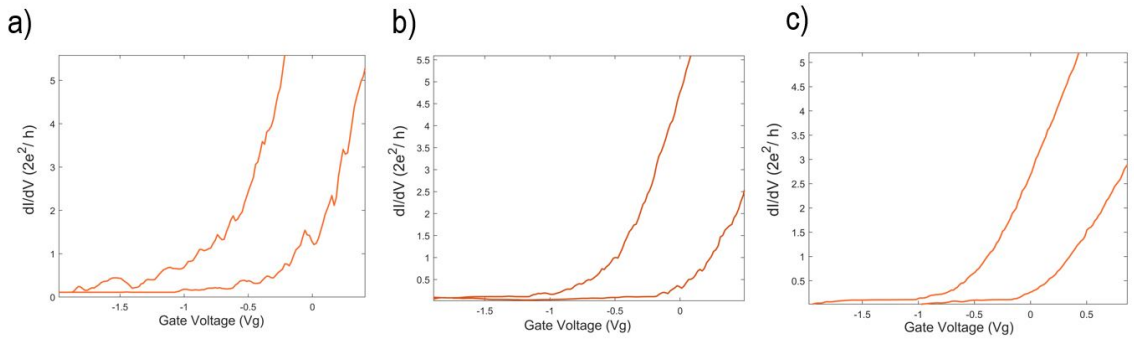


Figure 28: Zoomed in images of the plots for $[1\bar{1}0]$ NWs with top-barrier for L: 500nm, $1\mu m$, and $2\mu m$.

A final note can be made on the probable mode of transport occurring in the SAG NWs. As an example, we inspect Figure 28 above which is also characteristic of the other plots obtained through the FET measurements. If quantized conductance step plateaus appear, they do so for the lowest values for G which signalizes the filling of the first few subbands, after which the steps smear out. In the zoomed plots above, for $L = 500nm$, small singularities or oscillatory steps can be distinguished which quickly fade out. It could be due to the filling of subbands, but they are not distinct nor prevalent. In plots (b) and (c), there are no signs of these oscillations due to the longer channel lengths. It can be said that the diffusive mode of electron transport is most likely occurring in these NWs where the mean free path l_e is smaller than the channel lengths used. This is possibly due to a combination of disorder, scattering phenomena, and thermal broadening. Investigating smaller channel lengths for future SAG devices could be promising.

Finally this sub-section can be concluded by proposing that the FET mobilities (high-slope region) and the values for g_{max} for the SAG heterostructures displayed a maximum for the $[1\bar{1}0]$ NWs having the top-barrier layer present. The FET mobilites (low subthreshold region) exhibited average higher values for the $[010]/[100]$

NWs. Due to the discrepancy in choosing the right V_g sweep rates, accurate comparisons of the hysteresis between the plots with and without-barrier NWs devices couldn't be made. However the hysteresis curves as they appear can be explained to a degree. For future research, thoroughly characterizing the surface state induced scattering/charge trapping dynamics, and obtaining a method for determining the average compositions in the InGaAs buffer and barrier regions is crucial as these have a direct impact on the carrier mobility and hysteresis in FET measurements.

Part IV

CONCLUSION AND FUTURE WORK

6

CONCLUSION AND FUTURE WORK

To further the development in topological quantum computation, methods must be realized to grow disorder free materials. Selective area-grown NWs are a promising candidate due to their (quasi) 1D dimensionality and scalability factor. An investigation into the carrier transport in a SAG NW, with the inclusion of a thin top-barrier layer, was done in this thesis. The barrier layer essentially allows for the creation of a quantum well amongst the semiconductor heterojunctions, but most importantly assists in improving the surface and interfacial properties of the InAs transport channel.

Four-probe FET measurements were carried out for the SAG NWs to be able to characterize the carrier transport. To further support theis investigation, COMSOL finite element modelling simulations were utilized, namely a Schrodinger-Poisson self-consistent solver.

Given that the FET transport measurements were performed for three NW orientations of $[1\bar{1}0]$, $[100]$, and $[010]$, the Comsol models were devised accordingly to match the NWs with its diameter/width d. Schrodinger-Poisson simulations were then performed at $7K$ (not lower T couldn't be reached due to convergence problems) for two models (with and without barrer) for a NWs of $d = 235nm$ and another two models for NWs of $d = 265nm$. Additionally a finite surface charge density ρ_s was included for the NW top facets within the modelling. Due to inaccuracies in obtaining definite compositions of In and Ga for the InGaAs buffer/barrier layers, the compositions were kept constant for the models.

The Comsol modelling showed that the inclusion of ρ_s results in the formation of a deeper accumulation region or potential. With the help of the Schrodinger-Poisson solver exhibited a higher subband occupation than the model without ρ_s. Then, whilst keeping ρ_s constant for the rest of the models, the next set of simulations showed a proportionality between the NW diameter and number of subband occupation. Here the $d = 265$ NW model showed a higher subband occupation for the three gate voltages used $V_g = -0.5V, 0V, 5V$ than the $d = 235nm$ NW model. It was also noted that the NW subband modes have a strong dependence on symmetry in a triangular NW. Hence the electron probability densities tend to reside in the side QWs, more than the central/vertical QWs in the NW geometry. Finally the inclusion of a top-barrier showed better quantum confinement and decreased subband occupation numbers within the NW when compared to a NW of same d

but without barrier. The inclusion of the barrier also displayed a degree of overlap of the charge density into the barrier region. This could be beneficial in preventing a reduction in carrier mobility by pulling the electron wavefunctions into the barrier region, and away from the interface where trap states or scattering centers might reside.

The four-probe FET measurements showed some of the highest reported FET mobilities for SAG NWs. These are, $14870 cm^2/Vs$ and $15300 cm^2/Vs$ for $L = 1\mu m, 2\mu m$ with the $[1\bar{1}0]$ NWs. The resulting high mobilities were most likely due to the presence of the protective top barrier. Also the larger diameter of $[1\bar{1}0]$ NWs could have led to a less chance of scattering phenomena which is more predominant in NWs with smaller d. EELS maps also hinted at different In and Ga compositions in the buffer and barrier regions. This could have led to varying degrees of lattice mismatch at the interfaces and changes in the electron effective mass in the respective regions. Furthermore, large tranconductances were also attributed to the $[1\bar{1}0]$ NWs. However higher mobility values for subthreshold-slope region was more characteristic of $[100]/[010]$ NWs. Finally, diffusive transport was likely the type of carrier transport occurring within the NWFETS.

For the current research in this thesis to continue, an important step is to be able to devise a method for obtaining the average In and Ga compositions in the subsequent layers of the SAG NWs. The simulation and electrical characterization methods would then provide us with more accurate results. Determining the critical thickness of the top-barrier is also a necessity to optimize the charge density overlapping into the region. The Schrodinger-Poisson simulations hinted at quantum confinement effects within the side quantum wells of the SAG triangular geometry. Investigating this by changing the overall diameter or width of the NW whilst preserving the small width of the quantum wells would be worth pursuing.

Part V

APPENDIX

7

APPENDIX

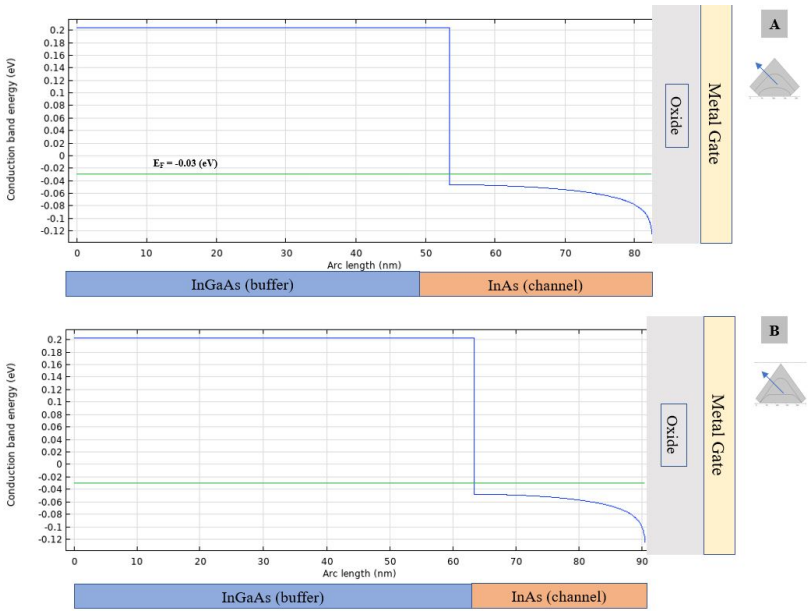


Figure 29: Plot A above is the E_c profile which portrays the side QW of 30 nm characteristic of the 1A NW and plot B shows the side QW of 27nm for NW 2A

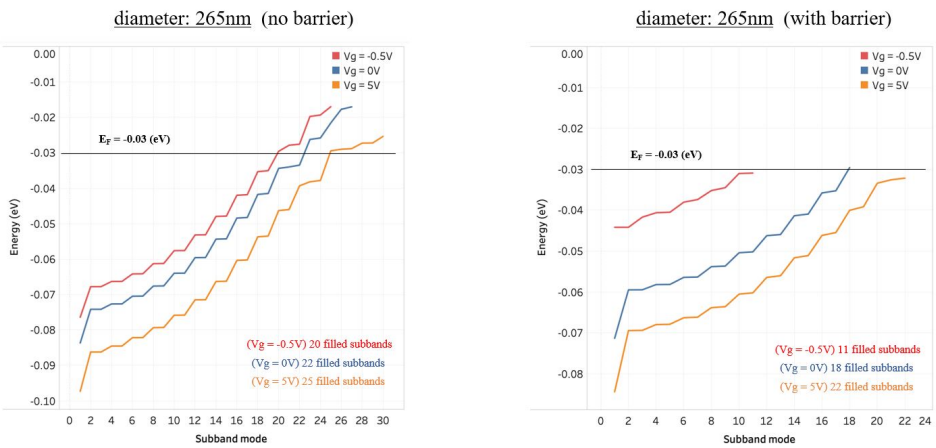
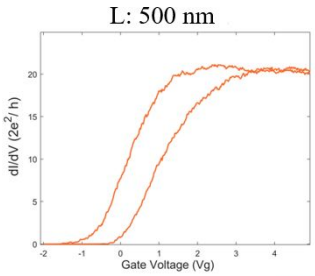
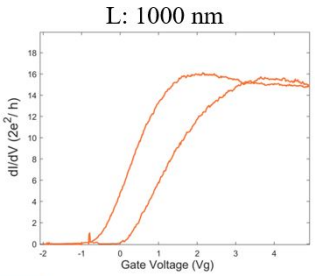


Figure 30: Subband occupation for NW 2A (no barrier) and the same for NW 2B (with barrier). Plot for NW 2B has been plotted only up till E_f



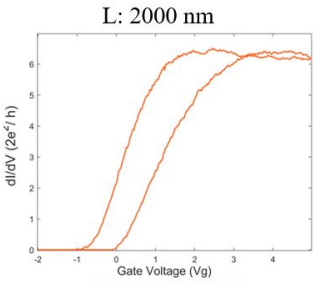


[1-10]

L = 500 nm	L = 1000 nm
$V_{Hys}(G_{Hys})$ = 0.95 V	$V_{Hys}(G_{Hys})$ = 0.93 V
$\mu_{FS(H)}$ = 9500 cm²/V.s	$\mu_{FS(H)}$ = 11000 cm²/V.s
$\mu_{BS(H)}$ = 5550 cm²/V.s	$\mu_{BS(H)}$ = 5500 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 410 cm²/V.s	$\mu_{FS(L\text{-}tail)}$ = 970 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 690 cm²/V.s	$\mu_{BS(L\text{-}tail)}$ = 1360 cm²/V.s
$g_{max(FS)}$ = 2.1 µS	$g_{max(FS)}$ = 1.2 µS
$g_{max(BS)}$ = 1.6 µS	$g_{max(BS)}$ = 0.9 µS

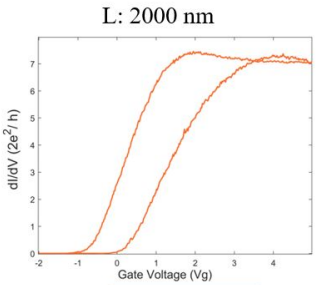
[1-10]

Figure 31: Devices for [1-10] which were still working



[1-10]

L = 2000 nm
$V_{Hys}(G_{Hys})$ = 0.95 V
$\mu_{FS(H)}$ = 12100 cm²/V.s
$\mu_{BS(H)}$ = 8000 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 1040 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 1330 cm²/V.s
$g_{max(FS)}$ = 0.51 µS
$g_{max(BS)}$ = 0.43 µS



[010]

L = 2000 nm
$V_{Hys}(G_{Hys})$ = 0.95 V or 1.96
$\mu_{FS(H)}$ = 10400 cm²/V.s
$\mu_{BS(H)}$ = 6900 cm²/V.s
$\mu_{FS(L\text{-}tail)}$ = 830 cm²/V.s
$\mu_{BS(L\text{-}tail)}$ = 1040 cm²/V.s
$g_{max(FS)}$ = 0.39 µS
$g_{max(BS)}$ = 0.29 µS

Figure 32: Devices for [1-10] (left) and [010] (right) which were still working

BIBLIOGRAPHY

[1] W Shockley. “Transistor technology evokes new physics”. In: *Nobel Lecture* (1956), pp. 344–374.

[2] J. S. Kilby. “Miniaturized Electronic Circuits (U. S. Patent No. 3,138, 743)”. In: *IEEE Solid-State Circuits Newsletter* 12.2 (2009), pp. 44–54. ISSN: 1098-4232. DOI: 10.1109/n-ssc.2007.4785580.

[3] Gordon E. Moore. “Cramming more components onto integrated circuits”. In: *Proceedings of the IEEE* 86.1 (1998), pp. 82–85. ISSN: 00189219. DOI: 10.1109/JPROC.1998.658762.

[4] Richard P. Feynman. “Simulating physics with computers”. In: *International Journal of Theoretical Physics* 21.6-7 (1982), pp. 467–488. ISSN: 00207748. DOI: 10.1007/BF02650179.

[5] D. P. Divincenzo. “Topics in Quantum Computers”. In: *Mesoscopic Electron Transport* (1997), pp. 657–677. DOI: 10.1007/978-94-015-8839-3_18. arXiv: 9612126 [cond-mat].

[6] R. J. Schoelkopf and S. M. Girvin. “Wiring up quantum systems”. In: *Nature* 451.7179 (2008), pp. 664–669. ISSN: 14764687. DOI: 10.1038/451664a.

[7] Thomas Monz et al. “Realization of a scalable Shor algorithm”. In: *Science* 351.6277 (2016), pp. 1068–1070. ISSN: 10959203. DOI: 10.1126/science.aad9480. arXiv: 1507.08852.

[8] C. Figgatt et al. “Complete 3-Qubit Grover search on a programmable quantum computer”. In: *Nature Communications* 8.1 (2017), pp. 1–9. ISSN: 20411723. DOI: 10.1038/s41467-017-01904-7. arXiv: 1703.10535. URL: http://dx.doi.org/10.1038/s41467-017-01904-7.

[9] T. P. Harty et al. “High-fidelity preparation, gates, memory, and readout of a trapped-ion quantum bit”. In: *Physical Review Letters* 113.22 (2014), pp. 2–6. ISSN: 10797114. DOI: 10.1103/PhysRevLett.113.220501. arXiv: 1403.1524.

[10] T. F. Watson et al. “A programmable two-qubit quantum processor in silicon”. In: *Nature* 555.7698 (2018), pp. 633–637. ISSN: 14764687. DOI: 10.1038/nature25766. arXiv: 1708.04214.

[11] R. Barends et al. “Coherent josephson qubit suitable for scalable quantum integrated circuits”. In: *Physical Review Letters* 111.8 (2013), pp. 1–5. ISSN: 00319007. DOI: 10.1103/PhysRevLett.111.080502. arXiv: 1304.2322.

[12] R. M. Lutchyn et al. “Majorana zero modes in superconductor-semiconductor heterostructures”. In: *Nature Reviews Materials* 3.5 (2018), pp. 52–68. ISSN: 20588437. DOI: 10.1038/s41578-018-0003-1. URL: http://dx.doi.org/10.1038/s41578-018-0003-1.

[13] A.Yu. Kitaev. “Fault-tolerant quantum computation by anyons”. In: *Annals of Physics* 303 (2002), pp. 2–30.

[14] Kristjan Ottar Klausen et al. “Majorana zero modes in nanowires with combined triangular and hexagonal geometry”. In: *Nanotechnology* 31.35 (2020). ISSN: 13616528. DOI: 10.1088/1361-6528/ab932e. arXiv: 2004.14991.

[15] V. Mourik et al. “Signatures of majorana fermions in hybrid superconductor-semiconductor nanowire devices”. In: *Science* 336.6084 (2012), pp. 1003–1007. ISSN: 10959203. DOI: 10.1126/science.1222360.

[16] M. T. Deng et al. “Majorana bound state in a coupled quantum-dot hybrid-nanowire system”. In: *Science* 354.6319 (2016), pp. 1557–1562. ISSN: 10959203. DOI: 10.1126/science.aaf3961. arXiv: 1612.07989.

[17] J. Kammhuber et al. “Conductance through a helical state in an Indium antimonide nanowire”. In: *Nature Communications* 8.1 (2017), pp. 1–6. ISSN: 20411723. DOI: 10.1038/s41467-017-00315-y. URL: http://dx.doi.org/10.1038/s41467-017-00315-y.

[18] P Krogstrup, C M Marcus, and T S Jespersen. “Epitaxy of semiconductor–superconductor nanowires”. In: 14.January (2015). DOI: 10.1038/NMAT4176.

[19] Hao Zhang et al. “Quantized Majorana conductance”. In: *Nature* 556.7699 (2018), pp. 74–79. ISSN: 14764687. DOI: 10.1038/nature26142. arXiv: 1710.10701.

[20] Sankar Das Sarma and Haining Pan. "Disorder-induced zero-bias peaks in Majorana nanowires". In: *Physical Review B* 103.19 (2021), pp. 1–10. ISSN: 24699969. DOI: 10.1103/PhysRevB.103.195158. arXiv: 2103.05628.

[21] Kwok K Sze, S.M and . NG. *Physics of Semiconductor Devices*. Third Edit. John Wiley sons, 2006. ISBN: 0471143235.

[22] Sergey M Frolov et al. "Quantum computing based on semiconductor nanowires". In: 38.October (2013), pp. 809–815. DOI: 10.1557/mrs.2013.205.

[23] S Heedt, W Prost, and J Schubert. "Ballistic Transport and Exchange Interaction in InAs Nanowire Quantum Point Contacts". In: 111 (2016). DOI: 10.1021/acs.nanolett.6b00414.

[24] "Semiconductor Nanowire Networks Grown by Molecular Beam Epitaxy (PhD Thesis) by Filip Krizek". In: (2018).

[25] Filip Krizek et al. "Growth of InAs Wurtzite Nanocrosses from Hexagonal and Cubic Basis". In: (2017). DOI: 10.1021/acs.nanolett.7b02604.

[26] Sabbir A Khan et al. "Highly Transparent Gatable Superconducting Shadow Junctions". In: (2020). DOI: 10.1021/acsnano.0c02979.

[27] L Desplanque et al. "In-plane InSb nanowires grown by selective area molecular beam epitaxy on semi-insulating substrate". In: *Nanotechnology* 29.30 (), p. 305705. ISSN: 1361-6528. DOI: 10.1088/1361-6528/aac321. URL: http://dx.doi.org/10.1088/1361-6528/aac321.

[28] Filip Krizek et al. "Field effect enhancement in buffered quantum nanowire networks". In: 093401 (2018), pp. 1–8. DOI: 10.1103/PhysRevMaterials.2.093401.

[29] Daria V Beznasyuk et al. "The role of growth temperature on the electron mobility of InAs/In". In: (), pp. 1–7. arXiv: arXiv:2103.15971v1.

[30] D. A. Neamen. *Semiconductor Physics and Devices: Basic Principles*. Fourth Edi. McGraw Hill, 2012.

[31] Chuancheng Jia et al. "Nanowire Electronics : From Nanoscale to Macroscale". In: (2019). DOI: 10.1021/acs.chemrev.9b00164.

[32] Supriyo Datta. *Electronic transport in mesoscopic systems*. 1995.

[33] Appl Phys. "Ballistic one-dimensional transport in InAs nanowires monolithically integrated on silicon". In: 083105.January (2017). DOI: 10.1063/1.4977031. URL: http://dx.doi.org/10.1063/1.4977031.

[34] Benjamin D Woods, Sankar Das Sarma, and Tudor D Stanescu. "PHYSICAL REVIEW B 101 , 045405 (2020) Subband occupation in semiconductor-superconductor nanowires". In: *Physical Review B* 101.4 (2020), p. 45405. ISSN: 0031-899X. DOI: 10.1103/PhysRevB.101.045405. URL: https://doi.org/10.1103/PhysRevB.101.045405.

[35] Author August and Edwards Guldberg. "Master's Thesis Schrodinger-Poisson Calculations for Majorana Devices". In: (2017).

[36] Shadi A. Dayeh et al. "High electron mobility InAs nanowire field-effect transistors". In: *Small* 3.2 (2007), pp. 326–332. ISSN: 16136810. DOI: 10.1002/smll.200600379.

[37] "Transport characterization in nanowires using an electrical nanoprobe". In: *Semiconductor Science and Technology* 25.2 (2010). ISSN: 02681242. DOI: 10.1088/0268-1242/25/2/024015.

[38] Önder Gül et al. "Towards high mobility InSb nanowire devices". In: *Nanotechnology* 26.21 (2015), pp. 1–7. ISSN: 13616528. DOI: 10.1088/0957-4484/26/21/215202. arXiv: 1411.7285. URL: http://dx.doi.org/10.1088/0957-4484/26/21/215202.

[39] "Surface roughness induced electron mobility degradation in InAs nanowires". In: *Nanotechnology* 24.37 (2013). ISSN: 13616528. DOI: 10.1088/0957-4484/24/37/375202.

[40] Alexandra C Ford et al. "Supporting Information: Diameter-dependent electron mobility of InAs nanowires". In: *Nano Letters* 9.1 (2009), pp. 360–365.

[41] "Diameter dependence of electron mobility in InGaAs nanowires". In: *Applied Physics Letters* 102.9 (2013). ISSN: 00036951. DOI: 10.1063/1.4794414. URL: http://dx.doi.org/10.1063/1.4794414.

[42] Sheng S. Li. "Scattering Mechanisms and Carrier Mobilities in Semiconductors". In: *Semiconductor Physical Electronics* (1993), pp. 183–211. DOI: 10.1007/978-1-4613-0489-0_8.

[43] Shadi A. Dayeh et al. “Transport properties of InAs nanowire field effect transistors: The effects of surface states”. In: *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures* 25.4 (2007), p. 1432. ISSN: 10711023. DOI: 10.1116/1.2748410.

[44] Lee Stauffer and Keithley Instruments. “Fundamentals of Semiconductor C-V Measurements”. In: February (2009), pp. 1–4.

[45] Marina Blumin and Harry E Ruda. “Surface State Dynamics Dictating Transport in InAs Nanowires”. In: (2018). DOI: 10.1021/acs.nanolett.7b05106.

[46] Jason Alicea et al. “Non-Abelian statistics and topological quantum information processing in 1D wire networks”. In: *Nature Physics* 7.5 (2011), pp. 412–417. ISSN: 17452481. DOI: 10.1038/nphys1915. arXiv: 1006.4395.

[47] Roy L.M. Op het Veld et al. “In-plane selective area InSb–Al nanowire quantum networks”. In: *Communications Physics* 3.1 (2020), pp. 1–7. ISSN: 23993650. DOI: 10.1038/s42005-020-0324-4.

[48] Pavel Aseev et al. “Selectivity Map for Molecular Beam Epitaxy of Advanced III V Quantum Nanowire Networks”. In: (2019). DOI: 10.1021/acs.nanolett.8b03733.

[49] Javad Shabani, Morten Kjaergaard, and Henri Suominen. “Two-dimensional epitaxial superconductor-semiconductor heterostructures: A platform for topological superconducting networks”. In: September 2016 (2015). DOI: 10.1103/PhysRevB.93.155402. arXiv: arXiv:1511.01127v2.

[50] T Tschirky et al. “Scattering mechanisms of highest-mobility InAs / Al x Ga 1 x Sb quantum wells”. In: 115304 (2017), pp. 1–8. DOI: 10.1103/PhysRevB.95.115304.

[51] Joon Sue Lee et al. “PHYSICAL REVIEW MATERIALS 3 , 014603 (2019) Contribution of top barrier materials to high mobility in near-surface InAs quantum wells grown on GaSb (001)”. In: 014603 (2019), pp. 1–7. DOI: 10.1103/PhysRevMaterials.3.014603.

[52] *COMSOL Multiphysics® v. 5.6. www.comsol.com. COMSOL AB*. Stockholm, Sweden.

[53] Sebastian Heedt et al. “Resolving ambiguities in nanowire field-effect transistor characterization”. In: *Nanoscale* 7.43 (2015), pp. 18188–18197. ISSN: 20403372. DOI: 10.1039/c5nr03608a. URL: http://dx.doi.org/10.1039/c5nr03608a.

[54] M. Levinshtein, S. Rumyantsev, and M. Shur. *Handbook series on Semiconductor Parameters. Volume 1*. 1996.

[55] M. Levinshtein, S. Rumyantsev, and M. Shur. *Handbook series on semiconductor parameters. Volume 2*. World Scientific, 1999.

[56] Fahd A. Mohiyaddin et al. “Simulation of Silicon Nanodevices at Cryogenic Temperatures for Quantum Computing”. In: *Nanotechnology* 27 (2016), p. 42. URL: https://www.comsol.com/paper/download/437352/mohiyaddin_paper.pdf.

[57] John A. Gil-Corrales et al. “Self-consistent schrödinger-poisson study of electronic properties of gaas quantum well wires with various cross-sectional shapes”. In: *Nanomaterials* 11.5 (2021). ISSN: 20794991. DOI: 10.3390/nano11051219.

[58] Tong Li et al. “Improving the electrical properties of InAs nanowire field effect transistors by covering them with Y2O3/HfO2 layers”. In: *Nanoscale* 10.39 (2018), pp. 18492–18501. ISSN: 20403372. DOI: 10.1039/c8nr05680c.

[59] Alexandra C. Ford et al. “Observation of degenerate one-dimensional sub-bands in cylindrical InAs nanowires”. In: *Nano Letters* 12.3 (2012), pp. 1340–1343. ISSN: 15306984. DOI: 10.1021/nl203895x.