UNIVERSITY OF COPENHAGEN

Barrier Properties and Electron Transport of Quantum Dots in InAs-InAsSb Nanowire

University of Copenhagen

Xiangyu Lin
Supervisor: Jesper Nygård
Kasper Grove-Rasmussen

August 15, 2022

Abstract

This thesis addresses electron transport and the physical properties of InAs/InAsSb nanowires. By incorporation of Sb in the Molecular-Beam Epitaxy (MBE) growth of InAs, the $InAs_{1-x}Sb_x$ would have different crystal phase and energy band gap from InAs. Thus alternating InAs and $InAs_{1-x}Sb_x$ segments can be used to simulate the operating principle of quantum dots, which are always used in research on quantum effects in finite low-dimensional systems. Moreover, different growth parameters, for example, the growth temperature, catalyst particle diameter, and growth time of each segment forming the quantum dots can change the properties of these quantum dots to influence their conditions of electron transport. By characterization with different kinds of microscopes and fabricating devices for electron transport measurement of InAs/InAsSb with different growth parameters, it is possible to show the effect of each parameter and then try to find the best conditions for growing quantum dots with stable Coulomb resonances.

Acknowledgements

First of all, I would like to thank Jesper Nygard for taking me into the nanophysics world, and offer me lots of guidence and patience. And also Kasper Grove-Rasmussen and Thomas Kanne Nordqvist, who also supervise my thesis and offer me the specific topics to study.

I feel very lucky that lots of people taught me to be a skillful experimenter: the cleanroom experts Karolis Parfeniukas, Nader Payami, Zhe Liu, and Martin Bjergfelt, who taught me to use many fantastic instruments in the laboratories. I would also present my appreciation to every members in our group: Alexandros Vekris, who offers me the substrates used in all my fabrications and shares much helpful lab experience with me; Kasper Grove-Rasmussen (thank you so much again) and Joachim Sestoft, who taught me each detail of the setup and process for measurement; James Xu, who often asks me to shadow his fabrication to bring my initial realization of each instrument in our lab, and always shares great researching experience with us; Rasmus Schlosser, who often solves my programming trouble as once; Oskar Perstølen and Daniel Kjær, who have been my partner in measurement for a long time; and finally: Jesper Nygard, who is our boss and also supply us instruments for measurement.

Outside the lab, I would like to thank my friends I meet in Copenhagen: James Xu, who is not only my good experiment partner, but also a good friend in my life; Buyuan Luo, my roomate for nearly two years; Yangming Wang and Lingxiao Li, two great friends bring me lots of pleasant memries. And last but not least, every of my family members, especially my parents, grandparents, and my fiancee, Siying Ren, who always accompany me to remit my emotional disturbance.

My best respect to you all!

Contents

List of Abbreviations

QD - Quantum dot
CB - Coulomb blockade
SEM - Scanning electron microscope
EBL - Electron beam lithography
MBE - Molecular beam epitaxy
ZB - Zincblende
WZ - Wurtzite
AC - Alternating current
DC - Direct current
DMM - Digital multimeter

Chapter 1

Introduction

1.1 Research Background

In recent years, continuous downscaling of critical dimensions of nanomaterials for high-performance logic applications is one of the main directs of the nanoelectronics region [3]. Nanowires are one kind of one-dimensional semiconductor device with a coaxial gate-dielectric channel geometry to achieve great electrostatic control [39].

Nanowires based on group III-V materials, which are tailored to high-quality axial/radial heterostructures and electron transport properties [21] [10], are particularly considered in this project. Within III-V materials, binary semiconductor InAs and ternary semiconductor $InAs_{1-x}Sb_x$ are chosen to fabricate the quantum dots and nanowires because of their different crystal phases and energy band gap caused by different strengths of spin–orbit interaction [26] [42]. One another important reason is that during the growth in MBE, it is excellent operability to switch between these two materials. There are clear borders between these two materials on fabricated nanowires, meaning fewer impurities are produced when switching to another material.

In this project, quantum dots formed by these two III-V semiconductors with different growth conditions on nanowires are the main object to be researched.

1.2 Thesis Outline

In chapter 2, theories regarding the InAs/InAsSb QD and nanowire containing InAs/InAsSb QDs grown under different conditions are presented, including how these two kinds of materials work as QD under different gate voltages, several variables of growth influenced the working condition of QD, and structure, design methods, and steps for the growth of InAs/InAsSb nanowires.

Chapter 3 describes the experimental techniques of the whole research progress on InAs/InAsSb nanowires, including characterizing nanowires before fabrication, depositing nanowires from the growth substrate to the bonding chip, designing and depositing contacts for measurement according to design, loading the bonding chip with fabricated designs on the fridge, and preparing a circuit for measurement. The result and analysis of measured data are discussed in chapter 4.

In chapter 5, according to researching and comparing the analyzed data of nanowires grown under different conditions, the most suitable parameter for growing InAs/InAsSb QD working like ideal QD would be found for future research. Some outlook on how to improve this research is also noticed.

Chapter 2

Theory

This chapter presents some of the theoretical background required for understanding the experiments. First, there is an introduction about the research objects, initially the materials and production of nanowires, and then general QDs and the specific QDs in the nanowires researched in this project. After that, the fundamental properties of theoretical QDs and some additional phenomena are introduced, so we can explain the different electron transport regimes for a quantum dot.

2.1 Nanowires

This section introduces the nanowires used in this project. All devices based on each nanowire are formed from the same materials, but with different growth conditions. This section focuses on the materials and the process of growing nanowires on substrates.

2.1.1 Materials of Nanowires

This project is based on experiments with nanowires made from group III-V materials which mainly crystallize in cubic zinc-blende (ZB) structure in bulk to bring high electron mobilities and strong confined energies. Then by being integrated with Si-based microelectronics to tailored III-V materials into unique axial and radial heterostructures, the samples can behave as one-dimensional device [11] [33] [21] [22]. At the same time, by adding another material into such a binary system (for example, Sb), the materials can exhibit hexagonal wurtzite (WZ) structure, which has higher electron mobility and smaller bandgap energy. Therefore, the nanowires with combinations of switching between segments of these two structures could form quantum dots (QDs) that control the electron transport, as mentioned in the next section.

Within the III-V materials, InAs and InSb have higher electron mobilities than others, and InAs can form low-resistance ohmic contacts as the Fermi level of InAs is pinning in its conduction band, leading to the formation of an electron surface accumulation layer [7] [31]. Thus in this thesis, the growth of nanowires uses InAs and adds Sb to form a WZ structure.

2.1.2 Nanowire Growth

All the InAs/InAsSb nanowires researched in this project are produced by the vapor-liquid-solid (VSL) growth method with metal catalysts in MBE by Thomas Kanne (express my highest appreciation again).

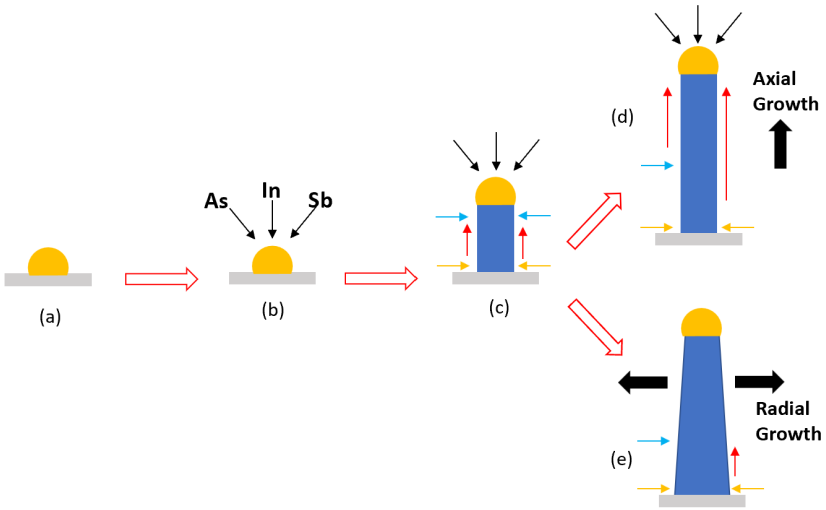


Figure 2.1: Schematics of nanowire growth. (a) Defining the position and diameter of the growing nanowire via the Au droplet by depositing different sizes of Au droplets on the substrate. (b) Supplying vapor phase reactants with different fluxes from the beam until supersaturation. (c) Nucleation takes place at the interface between the nanoparticle and substrate, and then the nanowire grows upward layer after layer. At the same time, besides the adatom directly impinging on the Au droplets (marked by black arrow), there are three other adatom contributions: atoms absorbed by substrate (in orange), impinging toward the sides of the nanowire (in blue), and diffusing along the concentration gradient toward the top of the nanowire. Under different ratios of each adatom contribution, two different directions of growth are defined: (d) Axial growth and (e) Radial growth.

The whole process of the VSL mechanism is started by depositing Au droplets in the designated positions. The Au droplets determine the position of the nanowire growing upward, and they also work as catalysts during the growth [32] [22]. Then

the precursor materials in the vapor phase are supplied as the reactants forming the nanowire [22]. Under a suitable temperature, the Au particles would alloy with precursor materials to form a liquid eutectic, and then as these materials are continuously supplied, the alloy particle becomes supersaturated. At this condition, the materials nucleate and crystallize at the liquid-solid interface. The formation of this crystal layer causes a decrease in the concentration of precursor materials in the alloy particle, so it is not supersaturated with them. Then the previous process is repeated to nucleate and crystallize new layers periodically to form a rod-shaped solid phase upward [21]. These steps are shown in Figure 2.1a-c.

As the nanowire grows, some other adatom contributions besides precursor materials directly impinging on the Au droplets set in, as shown in Figure 2.1c. Before the length of the nanowire reaches the adatom diffusion length, which explains the distance that the surface diffused adatoms can get, both directed impinging and surface diffusing adatoms join the upward growth. It is axial growth shown in Fig 2.1d. However, as the distance between the Au droplet and these adatom fluxes (e.g., from collection on the substrate) becomes farther than the diffusion length, only adatoms within the diffusion length from the Au droplet can join the axial growth, others are unable to reach the droplet to join the axial growth. Instead, they will deposit on the sidewalls of the nanowire to make the nanowire grows along the lateral direction [12]. Reflected in the grown nanowires used in this project, generally, they are fabricated by axial growth, but it is clear that their diameter is decreasing from the bottom to the top. It is not caused by radial growth because the diffusion length of InAs and InAsSb is much higher than the length of the grown nanowires (all below 10 μm) [38] [27]. Therefore, for each nanowire on both two substrates used in this thesis, the whole sample was only grown under axial growth. The decrease in diameter as growing upward is caused by the increase in distance from the substrate to the Au droplet. As the distance goes higher, the diffused adatoms require longer time to reach the droplet, so within the same growth time, for higher positions, there are fewer adatoms joining the nucleation to make the diameter become smaller.

Reflected in InAsSb and InAs, which are the materials of nanowires used in this thesis, during the growth of InAsSb/InAs nanowires, under As-rich conditions, both the vertical growth of nanowires and the parasitic layers deposited on the surface of the substrate are limited by the In supply, and the material balance of In is positive related to the radius of growing nanowire [13]. Therefore, for nanowires with a larger diameter, the growth speed is lower because of the finite amount of In. From the schematic of the growth process shown in Fig 2.5b, the length of each segment of nanowires is decided by the growth time, so within the same growth time, thicker nanowires would be shorter than thinner. The comparison of Fig 2.2 d and f proves this property.

The crystallization of precursor materials is confined within the liquid-solid

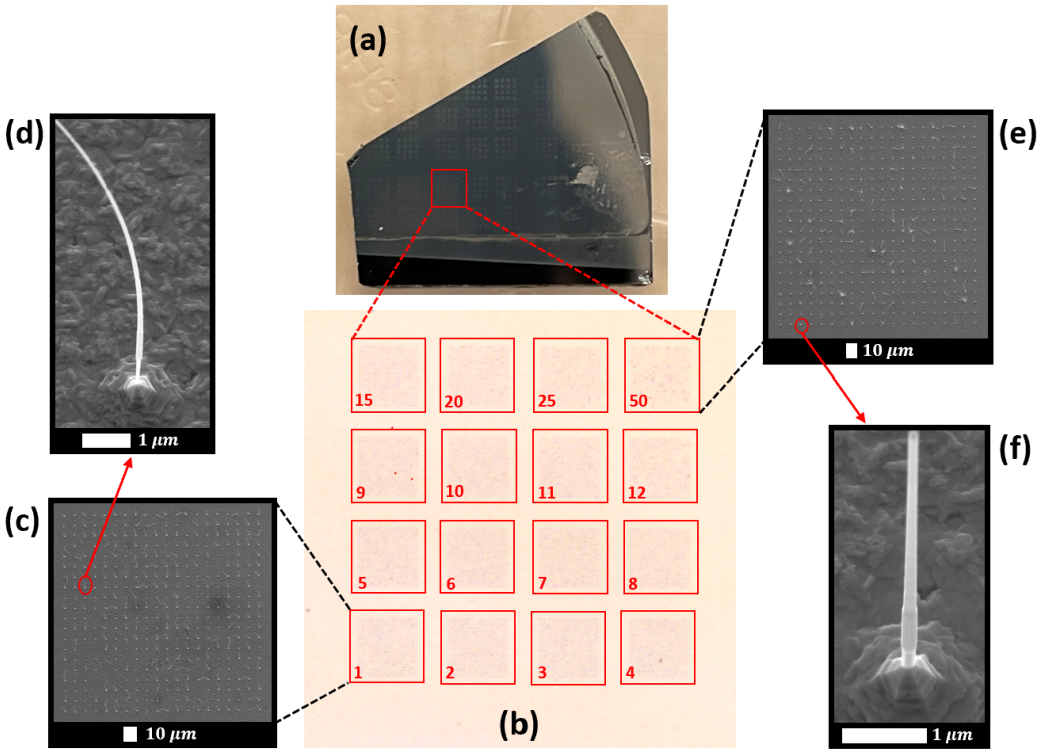


Figure 2.2: (a) Picture of one piece of vertical InAs/InAsSb nanowires growth. Repeated and even-distributed 4×4 matrix regions with sixteen different Au particle sizes are observable in this figure. (b) Zoom into one matrix to display the arrangement of all sixteen regions. Each region's 'shot number' of nanowires is labeled at each left bottom. This figure is obtained by an optical microscope with a magnification of 2.5. (c-d) and (e-f) separately zooms in on one nanowire of the 1 shot region and 50 shot regions. The diameters and lengths of these two nanowires are significantly different. The diameter of the widest position of this 1 shot nanowire is around 123 nm, and the 50 shot one is around 191 nm. These four figures are imaged by SEM.

interface. Therefore, the diameter of the Au droplet also determines the diameter of the grown nanowires. To study the influence on electron transport of the diameters of nanowires, for all devices used in this project, several different diameters decided by different Au droplet sizes are considered. To deposit Au droplets onto the surface of the substrate, it requires the electron beam lithography (EBL) technique, which is introduced in section 3.2.2. When irradiated more by electron beams, more space is created to hold Au droplets with larger diameters. To control this variable, when the size of an Au droplet needs to be increased, the position expected to deposit Au to grow nanowires would be irradiated more times by an electron beam with the same intensity and dose time. The exposure times are recorded and labeled as 'shot numbers' to determine the size of Au droplets and the diameter of grown nanowires. Nanowires with sixteen different 'shot numbers' are grown on the substrate shown in Fig2.2.

2.2 InAs/InAsSb Quantum Dots

This section introduces the quantum dot system, the electron transport, and then how to use heterostructures to achieve such systems on nanowires for further research.

2.2.1 Quantum Dots

Quantum dots (QDs) are 'artificial atoms' that are very weakly coupled to their environment to confine electrons or holes within very small regions [22]. Therefore, the electronic motion within QDs is restricted in all three dimensions, and QDs can be referred to as a zero-dimensional system. However, even though the size of the QD system is very small, the electron's phase is preserved over a large distance, and the energy spectrum is discrete. Therefore, QDs can be used to investigate quantum effects in finite low-dimensional systems [19] [36] [22] [2] [32].

The weak coupling to the environment enforces electrons to tunnel to be transported into or out of the QDs. The transport properties of a QD can be measured by coupling it with source and drain leads and then applying a bias voltage between the source and drain to make a current pass through the QD, as shown in Fig 2.3a [22] [32]. Fig 2.3b shows the condition of one QD system without any voltage applied. Electrons with lower energy than the height of barriers between the leads and QD can possibly tunnel through the barrier to enter or exit the island when there is an empty state with the same or lower energy on the other side of the barrier. Therefore, in the condition of Fig 2.3b, there are no available states on the QD to allow electrons to cross the QD to produce current flowing through.

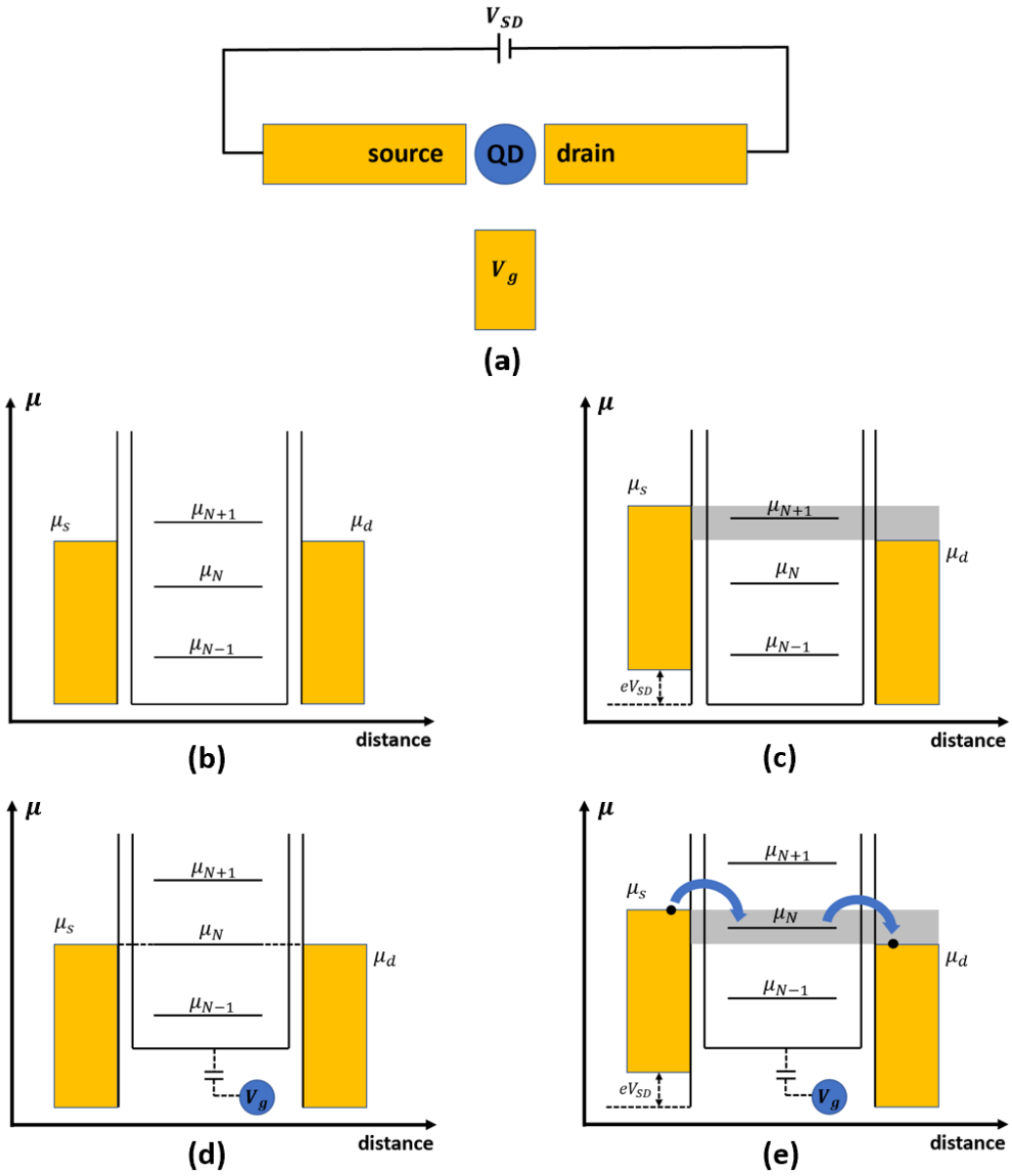


Figure 2.3: Schematic of single QD system. (a) Schematic representation of a QD system with source and drain contacts and one plunger gate. (b) Energy schematic diagram of the QD system shown on (a) with zero voltage of all leads or gates. The chemical potential of the source, drain, and islands in the dot are represented as μ_s, μ_d, and μ_N. (c-d) The effect of the chemical potential of the source and drain and energy levels on the QD by applying a bias voltage (V_{SD}) across the QD or gate voltage V_g with another voltage at 0. (e) The electron transfer tunneling through the DQ by moving V_{SD} with a constant value of V_g. When a dot level (or island) on the QD is in the bias window, the Coulomb blockades (CBs) would be relieved to allow electron transfer through.

There are two ways to make electrons able to transfer through the QD shown in Fig 2.3c and Fig 2.3d. In Fig 2.3c, There is a bias voltage (V_{SD}) applied across the island to lift the chemical potential and open a bias window (displayed in gray in the Figure) with the width of $\mu_s - \mu_d = eV_{sd}$. If there is an unoccupied energy level within the bias window as $\mu_s > \mu_N > \mu_d$, electrons could transfer through the QD from the source to the drain [22] [17] [4] [8]. If there are no quantum energy levels within the bias window, this condition of electron transport cannot be fulfilled, and there will be no current flowing. This system is called Coulomb blockade (CB), which will be introduced in the following sections. Another way without producing bias windows is applying gate voltage(s) to change the chemical potential of energy levels within the QD relative to μ_s or μ_d. If the chemical potential of one electron quantum state moves to the same height as its source and drain, like Fig 2.3d, the CB would be ceased, and an electron can tunnel through the system. When staying at zero bias and sweeping one gate voltage (V_g), there will be Coulomb resonances as periodically one electron tunneled through the QD, as shown in Fig 2.4.

Therefore, the Coulomb blockade can be ceased by switching V_{SD} and one V_g. By measuring the differential conductance $G = dI/dV$ respected to both V_{SD} and V_g, a charge stability diagram displayed as a diamond-shaped pattern would be plotted, called Coulomb blockade diamond, which will be introduced in later sections.

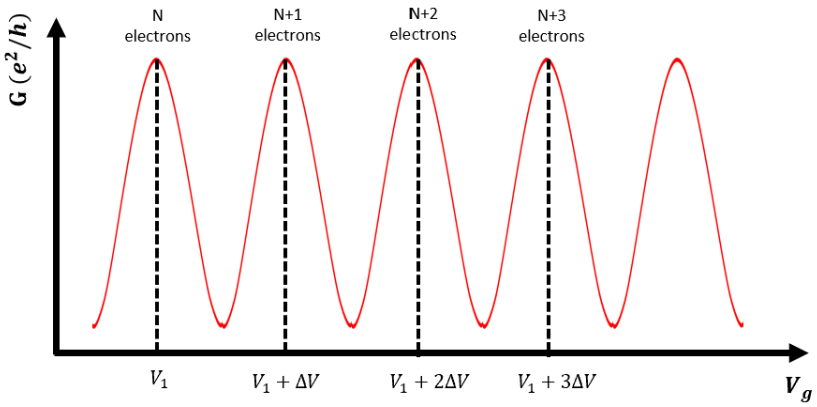
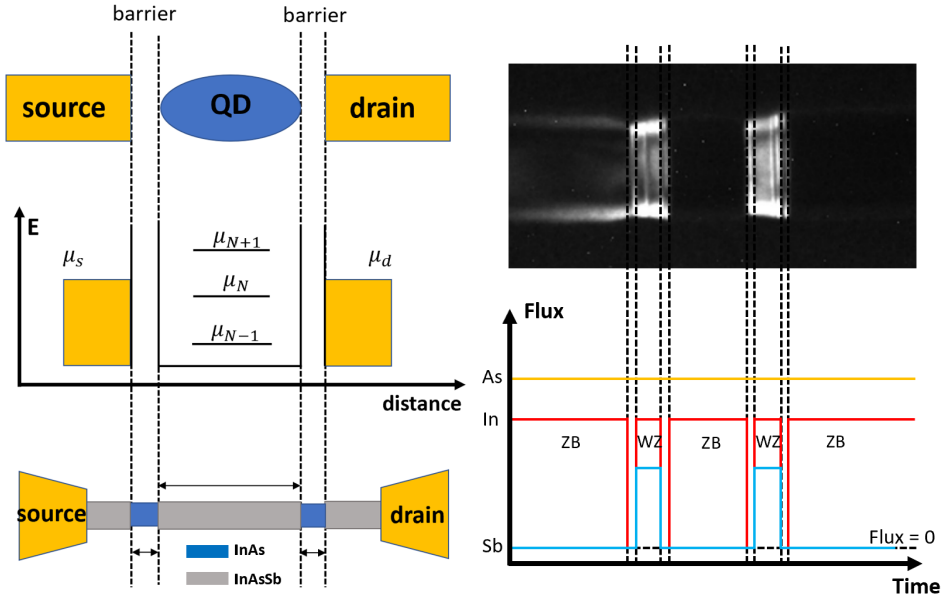


Figure 2.4: Schematic of electronic conductance resonance. Sweeping one V_g with zero bias, by every increase of ΔV toward the V_g, one electron is transferred through the QD. This behavior would be detected as each immediate excitement of electronic conductance.

2.2.2 Principle of InAs/InAsSb QDs

In order to effectively gate the devices, initially, it requires a low enough charge carrier density. Therefore, semiconductors are one of the ideal materials for building QD systems. Several different semiconductor QDs have been achieved, for example, two-dimensional electron gases, carbon nanotubes, and also semiconducting nanowires [19], which are studied in this project.



(a) (b)

Figure 2.5: Schematic of one InAs/InAsSb QD on a nanowire. (a) The correspondence between the QD system shown in Fig 2.3 and the schematic of InAs/InAsSb QD. The two regions between dash lines are the barriers to block the QD from the environment and control electron tunneling. The length of both QD and barriers are pointed out as factors for researching in this project. (b) The process of controlling the flux of each material to grow each segment of one InAs/InAsSb QD corresponding to the image of one fabricated InAs/InAsSb QD taken by transmission electron microscopy (TEM) by Oskar Perstølen.

InAs and InAsSb are chosen to form the QD system because of the difference in energy bandgap of these two kinds of phases. Both InAs and InSb are in the wurtzite (WZ) crystal phase, but for $InAs_{1-x}Sb_x$, which is using x molar composition of Sb to replace the same fraction of As by changing the flux ratio of each component during the molecular beam epitaxy (MBE) growth. $InAs_{1-x}Sb_x$ has a different crystal phase from ZB, and its energy band gap relates to the molar ratio of Sb (the gap reaches the minimum value at $x \sim 0.6$).

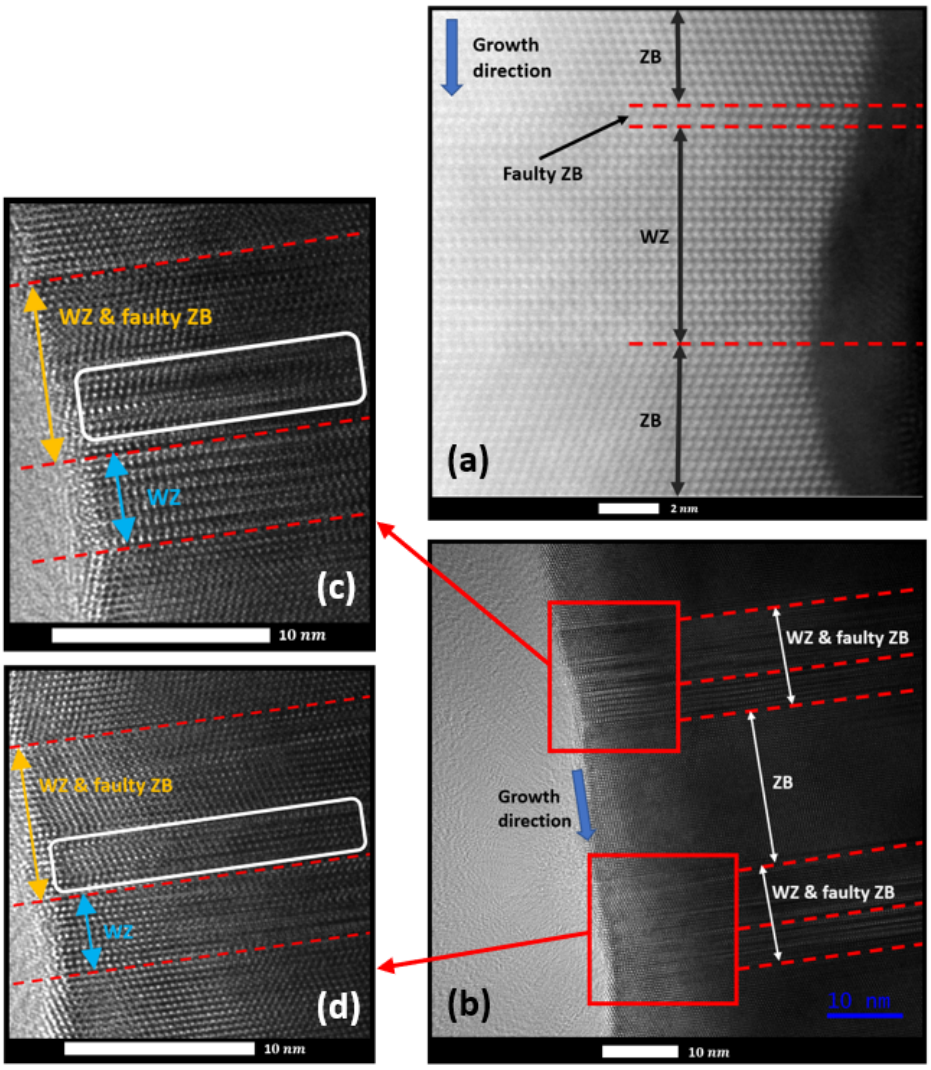


Figure 2.6: TEM images focusing on interfaces (highlighted by red dash lines) between segments with different structures of InAs/InAsSb QDs on QDev1248 and QDev1255 substrates. (a) Image of one barrier of one QD at a 3 shot nanowire on QDev1248. When switching from ZB to WZ by turning off the flux of Sb, there are a few layers of faulty ZB before the nucleation of WZ layers. Then when switching to ZB again, it changes immediately without growing other unexpected layers. (b) Focusing on one QD of one nanowire on QDev1155. For both barriers of this QD, the thickness of faulty ZB is much higher than QDs in QDev1248 shown in (a), but the switching back to ZB also happens immediately. The thickness of both barriers (including pure WZ and faulty ZB segments) are very similar, which is expected. (c-d) Zoom in to each barrier of the QD at (b). For both of them, between clear faulty ZB and WZ layers, which are circled by the white box, it is still faulty ZB but seems not even distributed like two nearby segments. All these images are taken by Martin Bjergfelt.

To achieve the InAs/InAsSb (also WZ/ZB) structure behaving as a QD, where electrons on InAsSb (with lower energy band gap) tunnel through InAs (with higher energy band gap), there should be a proper conduction band offset as enough height difference of barrier between these two materials. This offset can be adjusted by using different x of $InAs_{1-x}Sb_x$, which is controlled by using different ratios of fluxes of As and Sb during the growth. From the experiment mentioned in reference [33], it is reported that at around x = 0.3, the conduction-band offset is 95 meV, and there will be significant barriers to making electron transport as QD.

Adopting the ratio of the fluxes of As and Sb resulting in reference [33] can result in InAs/InAsSb QDs on nanowires by switching the flux of each element in MBE. The whole process has been shown in Fig 2.5b. During the growth, the flux of Ar is constant. When switching between ZB and WZ, both In and Sb would be paused for 30 s to deplete these atoms and maintain the purity of each component. However, in Fig 2.6, it shows that when switching from ZB to WZ by turning off the flux of Sb, there are still some undepleted Sb atoms joining nucleation to form faulty ZB layers, whose crystal structure is similar to pure ZB but crystalize toward a different direction. After depleting Sb atoms, pure WZ layers start to be nucleated. Then turning on Sb flux to switch to grow ZB layers. This switch takes place immediately without growing other unexpected materials first. Therefore, it required some extra work to deplete Sb before starting to grow WZ layers (for example, increasing the pause time or stopping the flux of Sb first and then leaving the other two fluxes for a little longer to grow extra ZB layers to deplete the left Sb atoms). On nanowires of QDev1255, which is not researched in this thesis but also contains InAs/InAsSb QDs, even though nanowires on both two substrates are grown under the same conditions except the growth time of barriers and ZB segments between, the thickness of faulty ZB segments on nanowires of QDev1255 is much higher than QDev1248. What caused the different sizes of faulty ZB and how the faulty ZB influences electron transport through the QD might require further research.

The size of each pair of barriers on both sides of each QD should be the same in order to make electrons tunnel through the same barrier height, and it has been proved by the TEM images taken by Oskar Perstølen and Martin Bjergfelt. The growth time of both ZB and WZ determines the length of QDs and barriers.

2.3 Coulomb Diamond

By measuring the differential conductance dI/dV with sweeping V_{SD} respected to one V_g on a QD, there will be a charge stability diagram with a diamond-shaped pattern, which is called Coulomb diamond and is available to display the addition

energy (E_{add}) and addition voltage (ΔV_g) to emit one more electron. Within this project, there are three kinds of conductance behaviors displaying differently in Coulomb diamonds: classical CB, multi-electron system, and Kondo regime [16].

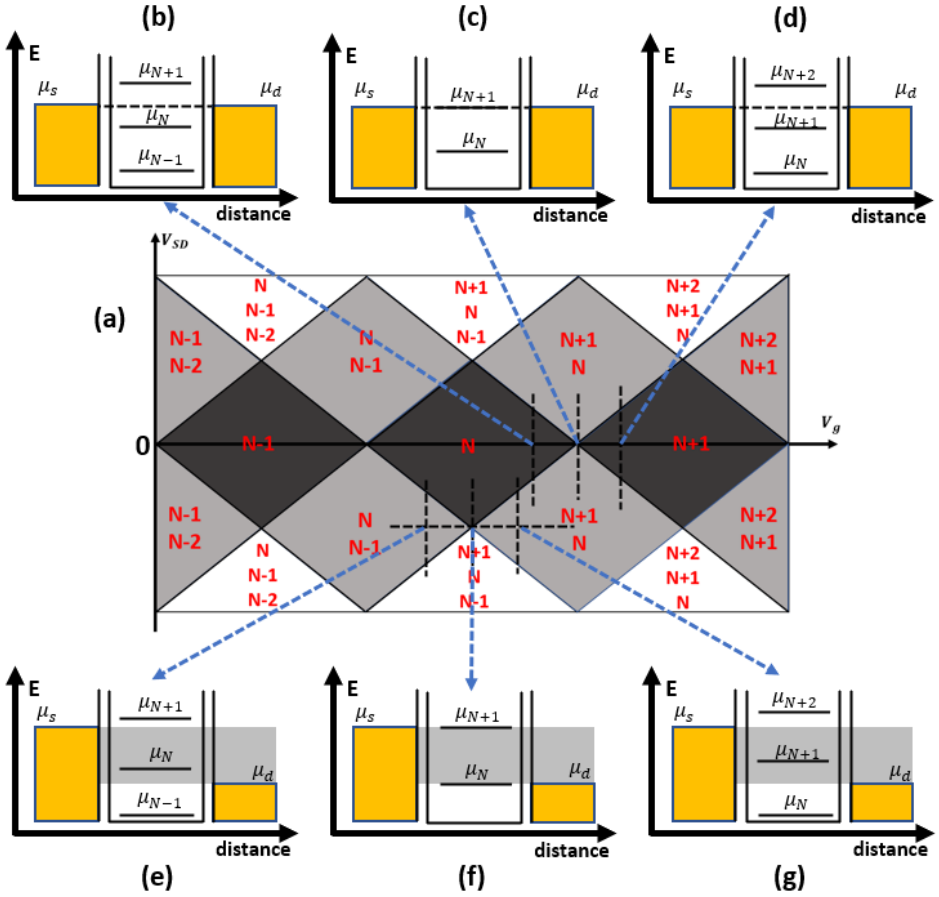


Figure 2.7: Schematic of single electron CB diamond and energy schematic diagrams of several positions on the CB diamond patterns to show the dependence of V_{SD} and V_g. (a) CB diamond of one single electron QD system. Red Labels in each inset diamond refer to the number of electrons on the dot fluctuating within the range of V_{SD} and V_g. Lighter shades indicate higher conductance. (b-d) show how electrons transfer through the QD by variation of V_g at zero bias, and (e-g) show the electron transport under a constant value of V_{SD}.

2.3.1 Classical Coulomb Diamonds

It starts from the classical Coulomb diamond, which exists in a single electron model. In this model, each dot level only admits one more electron. Fig 2.7

shows a schematic of single-electron tunneling (SET).

The comparison of the upper three and bottom three figures of Fig 2.7 show that for a higher range of V_{SD}, the width of the bias window could be increased to cover more split dot levels. Thus the further CB diamonds at higher V_{SD} appear to dot charge fluctuation between more electrons, and the conductance of these diamonds goes higher. Only the diamonds at zero bias with confining the bias window to accommodate only one channel can achieve almost full conductance blockade; therefore, these CBs are the main objects to research. Within Fig 2.7 (b) to (d) or (e) to (g), it shows the process that as increasing the plunger gate voltage, the SET could reach the charge degeneracy point (displayed in Fig 2.7 c and f) to lift the CB and then start fluctuating between higher dot levels.

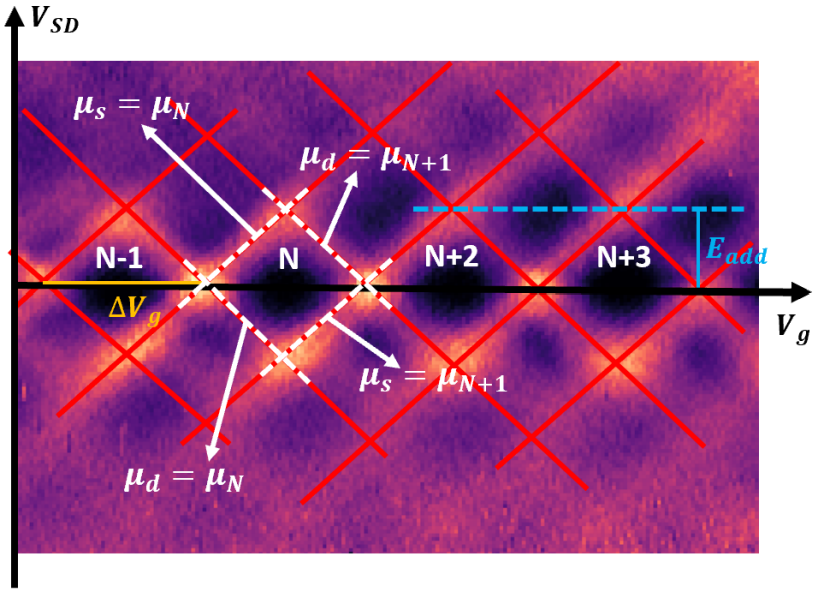


Figure 2.8: Using real measurement result to show the transport of single electrons at zero bias with displaying E_{add} and ΔV_g. The red full lines highlight the edges of CB diamonds at the lowest level, which refers to the alignment of chemical potential between the QD levels and the leads (source or drain). The white dash lines are one example to explain the coreference of four edges of one CB diamond.

Being different from multiple electrons structure, on the SET system, for one electron enters the QD to occupy one site on a dot level, it does not need extra energy to overcome the single particle level spacing ΔE with another electron that resides on the same dot level in the QD. Therefore, to add one extra electron, it only needs to overcome the electrostatic repulsion E_c from other levels or islands of the QD. The additional energy (E_{add}) and voltage (ΔV_g) are displayed on CB diamonds, which is shown in Fig 2.8.

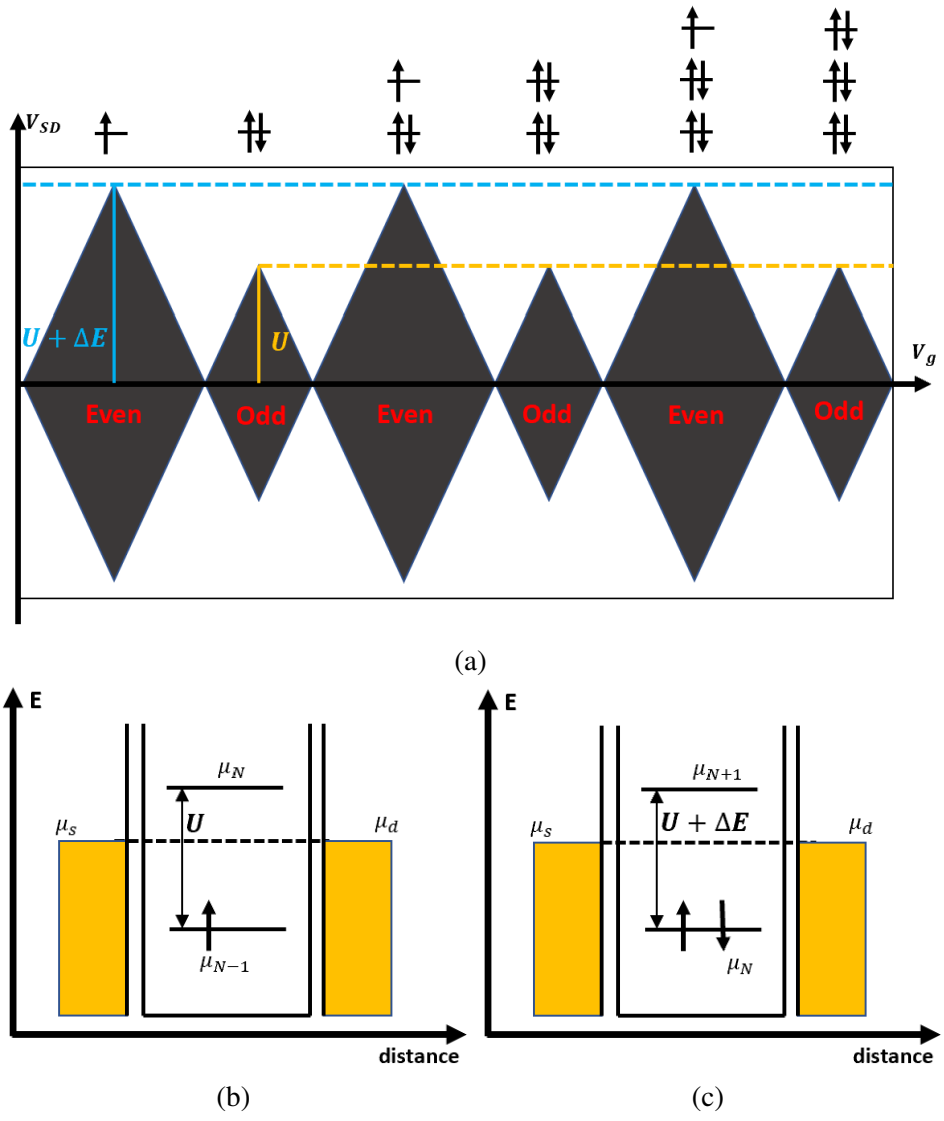


Figure 2.9: (a) Schematic of Coulomb blockade diamonds of multi-electron system with periodically switching two diamonds with different sizes. From the bigger diamond to the smaller one, the dot level has been fulfilled, and then the newly entered electron occupies the next level. The arrows at the top show how the levels are filled with spins. (b) Energy schematic diagram of an oddly loaded QD achieved by improving gate voltage ΔV_{odd} to overcome E_c only. (c) Energy schematic diagram of an evenly loaded QD by improving gate voltage ΔV_{even} to overcome both E_c and ΔE.

2.3.2 Coulomb Diamonds of Multi-electron System

When considering the spin of electrons, each dot level would be fulfilled by two electrons with different spins (spin up or spin down). Therefore, the electron transport has two conditions recorded as oddly and evenly loaded QD shown in Fig 2.9.

When the entered electron occupies a site on an empty level, it only needs to overcome the charging energy E_c brought by the electrostatic repulsion from other internal dot levels of the QD, which is similar to SET and labeled as 'odd diamonds' with smaller size shown in Fig 2.9. For the next entered electron, as mostly E_c is much bigger than ΔE on the same dot level, this electron would overcome $E_c + \Delta E$ by improving larger ΔV_g to occupy the same dot level with flipped spin instead of moving to a higher level. The greater E_{add} and ΔV_g bring a bigger size of Coulomb diamond labeled as 'even diamond' shown in Fig 2.9. As the previous level has been fulfilled, the following entered electrons would repeat this process to bring the periodic switch of these two different sizes of diamonds [16] [22].

However, this system would be visible when the ΔE is prominent, or it will behave similarly to classical CB diamonds as the size of odd and even diamonds becomes almost the same. There are two main factors to control it: the first one is the size of the QD. For a smaller QD, the quantum confinement would spread to single particle levels within each island; hence the quantization energy would be dominant to make ΔE clear enough. In contrast, E_c is dominant on QDs with bigger sizes. Another factor is the temperature during the measurement. Under higher temperatures that satisfy $\Delta E \ll k_B T$, as the energy spacing is much smaller than the thermal energy, the energy spectrum may be treated as a continuum. At the same time, the thermal energy is also much greater than the finite width $h(\Gamma_l + \Gamma_r)$ (Γ_l and Γ_r are the tunneling rate from the same level to the left or right reservoirs) of transmission resonance through the QD, thus this finite width can be disregarded, and each island of the QD can be treated as one energy level without single particle level spacing [18]. Therefore, this QD would behave like classical CB diamonds.

2.3.3 Kondo regime

Kondo regime of Coulomb blockade is one kind of specific condition of multi-electron structures. Kondo effect explains that for pure metals, typically, their electrical resistance goes lower with decreasing temperature as lower temperature restrains more on their atomic vibrations to make electrons easier to travel through. However, when the temperature drops to the Kondo temperature, the resistance saturates due to static defects in these materials. Then the scattering from

magnetic ions interacting with the spins of conducting electrons would increase the resistance logarithmically with decreasing temperature. But when the temperature is well below the Kondo temperature, the magnetic moment of the impurity ion will be screened entirely by the spins of electrons in the metal. After that, the electrical resistance of the metal would return to the saturated resistance. On semiconductor QDs, sometimes the conductance respected to V_g behaves the same as the resistance respected to the temperature of Kondo effect in metals, which is also caused by impurities [24] [35] [16].

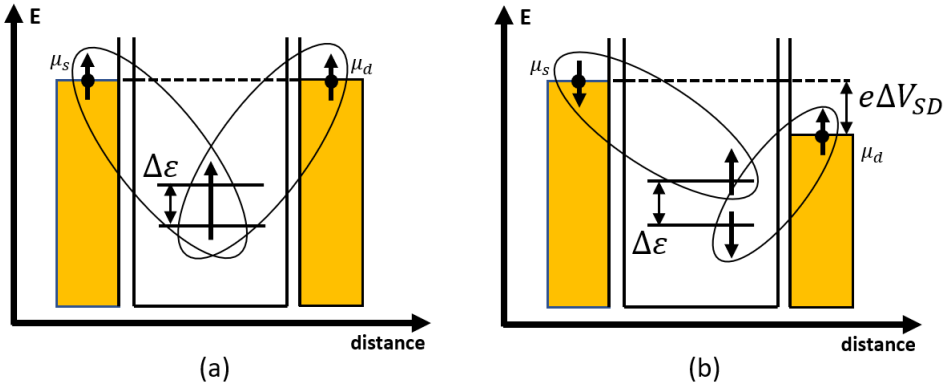


Figure 2.10: Schematic of Kondo resonances by forming Kondo singlets (pointed out by ellipses) between spin levels and reservoir electrons under (a) Zero bias (or conditions with spin degenerate spins when $\Delta\varepsilon = 0$) and (b) finite V_{SD}.

On the QD system, the Kondo effect is given rise to the strong coupling between the quantum dot and its leads. Considering only for a spin-degenerate level, electrons trapped at magnetic impurities with also two spins and large Coulomb energy compared to all other relevant energy scales of the QD system tunnel into the QD and occupy one site on a dot level. Because of the large Coulomb energy of impurities, one extra electron with flipped spin will be brought onto the occupied site through a normal channel instead of magnetic impurities. This coupling is achieved by the spin effect; therefore, for the multi-electron system, the Kondo effect would only take place on oddly loaded QDs as trapped electrons need to occupy an empty site first, and the evenly loaded QDs will not be influenced. The impurity spin in the QD would be screened by the electron spin, which is similar to the Kondo effect of metals. Then the coupled electron can tunnel out of the QD even though the impurity level ε may not be aligned with two leads.

For QDs with non-degenerate spin levels, it is also available to observe Kondo resonances. Under zero bias, the Kondo resonances are inhibited by the energy difference $\Delta\varepsilon$ between non-degenerate spin levels. However, this splitting can be compensated by supplying finite V_{SD}, and at that time, the lifted degenerate levels

separately couple with source and drain, which is shown in Fig 2.10b. During this process, an electron with the opposite spin of the electron trapped at the magnetic impurity tunnels into the QD to form a virtual intermediate state (as the higher level shown in 2.10b) with both electrons on the impurity site. However, as all accessible states up to the Fermi level have already been occupied, this condition should not exist. Therefore, it decays into the impurity being occupied by electrons with opposite spins at the Fermi level, and at that time, the spin on the impurity site has flipped. $\Delta\varepsilon$ can be controlled by adjusting the supplied magnetic field, but this project does not cover the research on magnetic fields, which requires further research in the future.

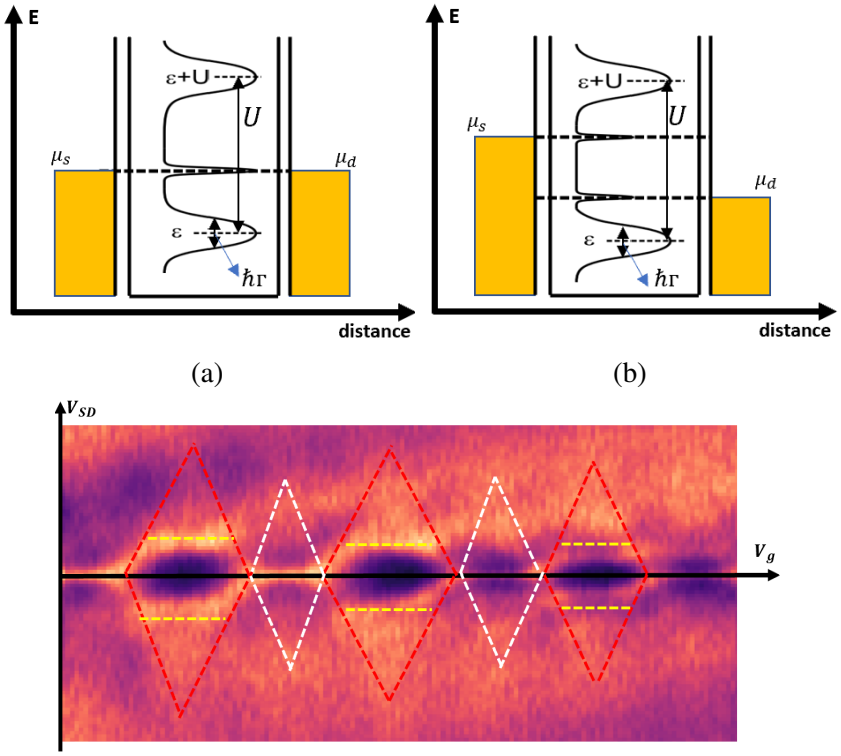


Figure 2.11: Schematic diagrams of a QD in the Kondo regime. Initially the Coulomb and Kondo resonances (a) at zero bias and (b) at finite V_{SD}. (c) One example of Coulomb diamonds displaying the Kondo effect. Red dash lines highlined the edges of even Coulomb diamonds, and white dash lines outline the vanished odd Coulomb diamonds replaced by some zero bias anomaly.

In order to observe the Kondo effect on one QD, two main conditions should be satisfied: the first one is that the measurement work should be done below the Kondo temperature of the materials forming the QD, and the other one is

supplying suitable ranges of V_g to achieve the 'strong coupling' between the QD and its leads [22] [16] [23].

Fig 2.11a and Fig 2.11b show the differential conductance for a QD with non-degenerate spin levels within a Kondo regime under zero bias and finite V_{SD}. These two wide peaks are the Coulomb resonances of the QD by electron transport and the sharp peak(s) between is the Kondo resonance(s) pinned at the Fermi levels of the reservoirs. Because of the split spin levels under finite V_{SD}, there will be two Kondo resonances at $\pm V_{SD}$ positions. Respected on its Coulomb diamonds shown in Fig 2.11c, even diamonds within Kondo regimes are similar to the standard multi-electron system explained in the previous section except for the co-tunneling process, which is highlighted by yellow dash lines (described in next section). But the odd diamonds almost vanished and are replaced by some zero bias anomaly (ZBA), which represents the Kondo regime [17] [35] [23].

The Reference [23] offers a zoom-in measurement of one ZBA region to explain its formation. As displayed in Fig 2.12, the ZBA part behaves as two consecutive diamonds with much smaller sizes on both V_{SD} and V_g, which are characteristics of few-electron quantum dots. And these two diamonds could represent the Kondo resonances at $\pm V_{SD}$ displayed in Fig 2.11b.

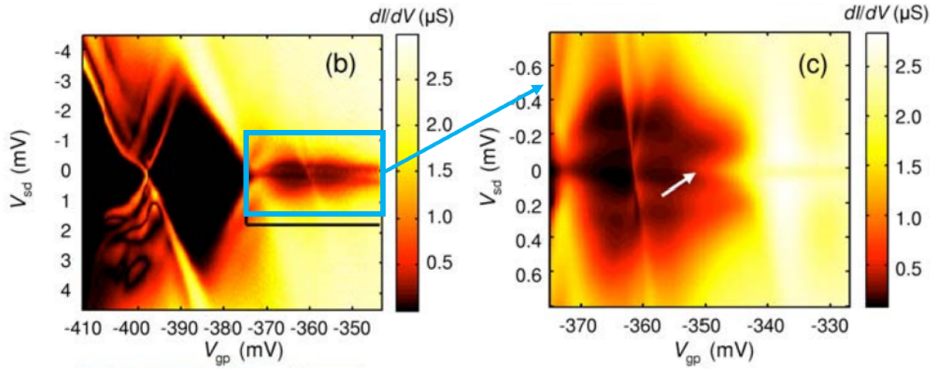


Figure 2.12: Zoom-in to one ZBA region of CB diagrams of one multi-electron system from Reference [23]. The white arrow on the right figure points to the position of the Kondo resonance

2.3.4 Excitation Spectroscopy

Sometimes there are extra transport channels running parallel to the edges of Coulomb diamonds. On this condition, electrons tunnel to the excited states in the QD instead of dot levels. These additional channels and excited states are shown in Fig 2.13.

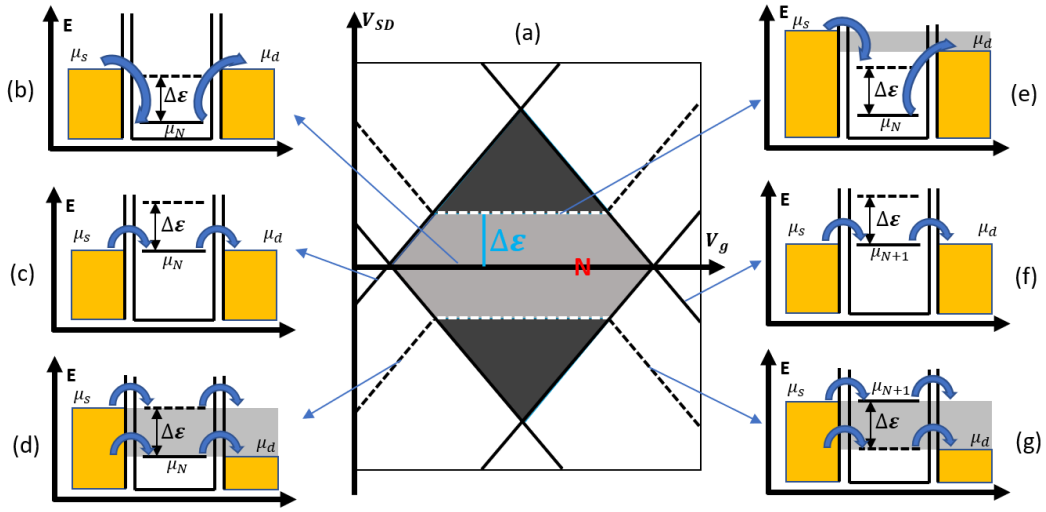


Figure 2.13: (a) Schematic of excitation spectroscopy and Coulomb diamond with excited states of one QD. Lighter shades indicate higher conductance, and the elastic (lighter) and inelastic cotunnelling (darker) regions are divided by excited states (white dash line). (b-g) Energy schematic diagrams and electron transports through several channels to the QD's ground state or excited state.

This phenomenon takes place by extra quantizations of dot levels in the QD, and two main reasons are causing it. First, the level spacing $\Delta\varepsilon$ between two electrons on one island becomes comparable to the charging energy U or even larger. Thus, the periodic oscillation which happens under $U \gg \Delta E$ would not be satisfied. Another reason is that sometimes more than one electron tunnels into the QD, but the bias window might not be big enough to overcome another charging energy. Therefore, another channel exists to let extra electrons tunnel out when it happens [15] [16] [32].

The electron transport through the excited states or even the ground states of QDs is called co-tunneling. The Coulomb diamond shows that this transport only needs to overcome $\Delta\varepsilon$ to transport electrons. On this condition, this value would be treated as the additional energy instead of either U or ΔE.

Chapter 3

Experiments

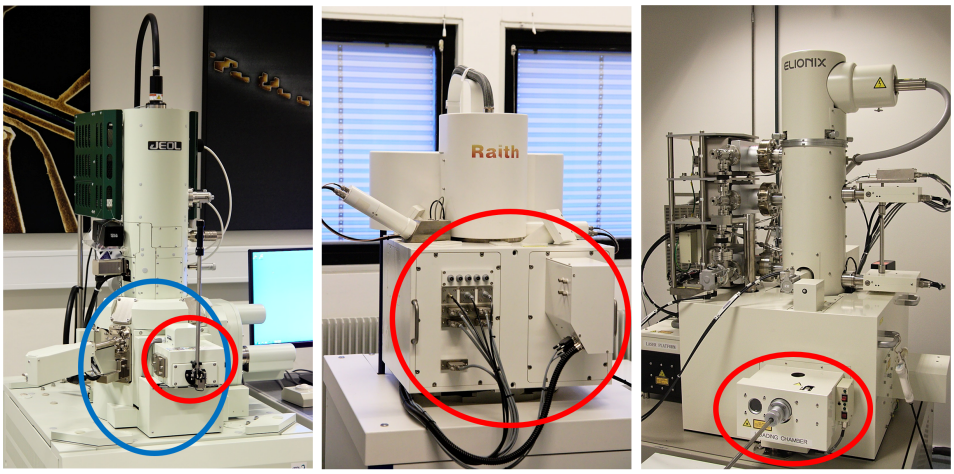
This chapter introduces the experimental techniques used during the fabrication, including how they function in the samples and each step to process devices using different equipment. After fabrication, the whole samples are available for measurement, and the setup for measurement in fridges is introduced at the end of this chapter.

3.1 Characterization

Before fabrication, it is essential to check whether the nanowires on substrates are clean and intact to be used and observe the structures of the alternative nanowires for fabricating. After finishing each process in apparatuses, it often requires checking whether the results are according to expected. After measurement, the samples are also needed to check if they were damaged during the measurement and analyze whether these damages influence the measurement results. As each device on the sample is in scales of nanometers, the observation requires techniques to enlarge the images more than 1000 times. Therefore, microscopes that can enlarge objects within hundreds of nanometers to be visible are necessary for this project.

3.1.1 Scanning Electron Microscope

Scanning electron microscope (SEM) is the most often used technique used for characteristics. The wavelength of electrons is much shorter than photons, so the resolution of SEM using electrons to generate images is much better than optical microscopes imaging by photons [37]. In order to avoid interacting and scattering of electrons along their path to distort the images, the environment within the main chamber holding the samples and electron beams for scanning



(a) (b) (c)

Figure 3.1: Three instruments using SEM technique. (a) JOEL 7800F, which is used the most for characteristics. The low lock marked in red circle is the position for loading or unloading samples. After loading the sample inside the low lock and pumping it down until the pressure within is close to 10^{-4} Torr, the sample is available to be loaded into the main chamber for measurement. (b) Raith eLine, which is mainly used when going to scan a large number of positions on the loaded sample in defaulting sequences. The inner space of this instrument is one whole without divided into the low lock and main chamber, so it requires a much longer time for pumping when loading and uploading samples through the gate marked by the red circle. (c) Elionix 7000, which is used for exposure and has SEM for observing. The structure between the low lock and the main chamber resembles JOEL 7800F. All these pictures are taken from the NBI cleanroom wiki.

should stay in a high vacuum (below 10^{-4} Torr). However, as images collected by SEM display different brightness by detecting the signal intensities of different positions, the imaged pictures by SEM are only monochrome [14].

SEM technique is adopted by several instruments used in this project. The first one is JOEL 7800F (shown in Fig 3.1a), which is the main equipment used for characteristics. Most figures of zoom-in segments on nanowires and fabricated devices displayed in the next chapter are taken by JOEL 7800F as this instrument is more convenient for adjusting focusing, stigmatizing, and aligning with the aperture, and it is available to scan and analyze the image of the current position observed on at once. Another advantage of JOEL 7800F is that the inside space is divided into the low lock, a small space for loading and unloading the samples, and the main chamber, which is the working area for characteristics and always at high vacuum. There is a gate between these two regions. When loading or

unloading samples, it just needs 2 to 3 mins to depressurize or pressurize the low lock, then turn on the gate between the low lock and main chamber to transfer samples between these two areas when their pressure difference is detected as low enough. Therefore, JOEL 7800F is a good choice for a quick look after each step of fabrication, meticulous searching on huge and complex devices, and detailed observation for realizing unfamiliar samples.

Another instrument having SEM is Raith eLine (shown in Fig 3.1b). Being different from JOEL 7800F, the inner space of eLine is in a whole chamber without being divided into two areas (low lock and main chamber). Therefore, when loading or unloading, the pumping work aims at the entire inner space instead of only the low lock compared with JOEL 7800F, and it takes a much longer time (around 15 to 20 mins) to depressurize or pressurize. The SEM of eLine is mainly used for scanning and imaging lots of positions on loaded samples in defaulted sequences without often manual switch. Before scanning, the primary process is to set up all interested positions on the sample to scan and collect images in a prearranged sequence, which is shown in Fig 3.3b. In order to align the real sample and the design file to make every action on the design file can act on the same positions on the real sample, there are alignment marks having precise points to record their coordinate values on both to correspond them into the same coordinate system with a tiny error (mostly within 20 nm). On the real-time image feedback by SEM, choose three clearly visible and complete alignment marks not on the same line, and find the corresponding alignment marks on the design file. Then by well matching the coordinate values of each group of alignment marks, all positions on both real samples and design files are at the same coordinate, when selecting one position on the design file, the SEM can move to the corresponding position on the real sample immediately. Then it is possible to prearrange many positions for long-time measurements without manual switches all the time.

When doing exposure by using Elionix 7000 (Fig 3.1c), which will be introduced in Section 3.2.2, it also requires aligning the real samples to the design files, whose methods and operations are similar to eLine. And the same as JOEL 7800F, Elionix 7000 also has a low lock for loading and unloading. Thus it does not take a long time to prepare.

3.2 Fabrication

This section introduces each step of fabrication, including transferring nanowires from the substrates with all grown nanowires to the base chip, designing patterns according to the layout of deposited nanowires shown in collected SEM images to build the devices for researching these selected nanowires, and then depositing metals on positions of designed patterns to get a complete quantum circuit for

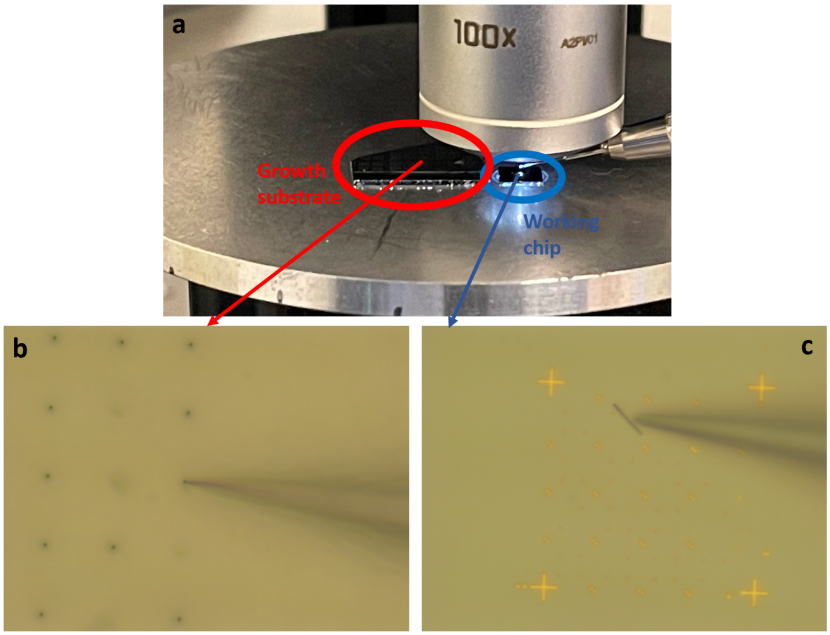


Figure 3.2: Images displaying the process of transferring 25 shot nanowires on QDev1197 by using a micromanipulator. (a) Stage of micromanipulator with both two substrates. Changing the vision of the optical microscope by moving the stage. (b) One region with 25 shot nanowires on growth substrate labeled as QDev1197. By adjusting the focus, the micromanipulator can zoom in to segments with different heights on the nanowire. Most users prefer to find out the Au droplet on the top of the nanowires, which is the most cognizable. (c) After breaking off and absorbing a nanowire by using a thin needle, raise the needle in order not to touch stuff on the substrate, and then move to the work chip to deposit this nanowire on a region circled by alignment marks.

measurement.

3.2.1 Nanowire Deposition

The first step of fabrication is transferring nanowires from the substrate with all grown nanowires to the base chip with coordinates for the following processes built by alignment marks. The image of the area accommodating deposited nanowires and metals on the base chip is shown in Fig 3.3b. It was initially placing both the substrate with grown nanowires and the cleaned base chip on the stage of the micromanipulator under an optical microscope. Then adjust the focus of the microscope and the height of the stage to make the Au droplet on top of the nanowires on the substrate and alignment marks on the base chip visible enough,

shown in Fig 3.2.

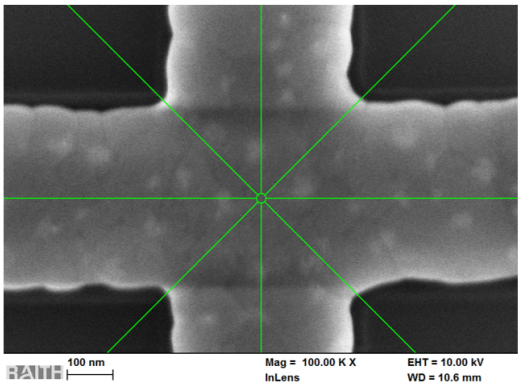
After adjusting the focus of the microscope and recording the coordinates of aimed positions (including the current heights of the stage) on both substrates, move down the stage to bring a large space for loading a needle with a tip radius of 100 nm for breaking off and transferring nanowires. After adjusting the focus and height of the needle to make its image taken by the microscope clear enough, record two positions of the needle: a transfer position, which is high enough from each surface of both substrates to transfer the needle between them without touching any stuff onside them even when carrying nanowires, and the engaging position, which is adapted for taking or putting nanowires.

The transfer of nanowires can start after the preparation above. In order to maintain all QDs on the collected nanowires for fabrication, the truncation position of these nanowires should be as close to their roots as possible. Therefore, the optical microscope is better to zoom in on the surface of the growth substrate and move down the needle to be close to this surface, then press the stand nanowire to make it bent until it breaks. Use the tip of the needle to absorb the broken nanowires, move the stage to the position of the work chip right up against the needle and the optical microscope, and then put the nanowire within an area surrounded by alignment marks. As the resolution and the maximum magnification of the optical microscope are limited, it is hard to check whether the transferred nanowires have high enough qualities (for example, whether all required QDs on the nanowires are intact) while using a micromanipulator. Therefore, it is necessary to transfer more than the needed number of nanowires (at most 16 as each working area has one nanowire, shown in Fig 3.3).

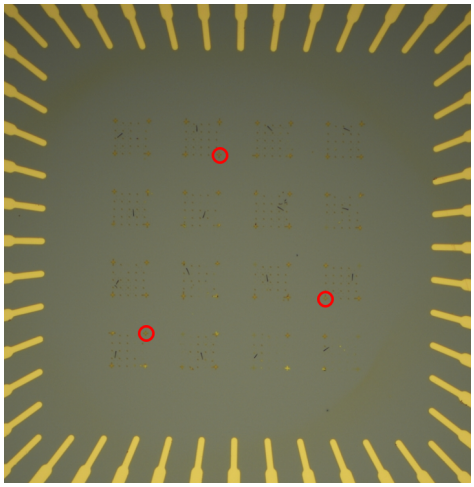
3.2.2 Electron Beam Lithography

With the help of inner alignment marks of each working area on the base chip, it is convenient to put images taken by SEM in the same positions of the design file. By adjusting the position of images to make the alignment marks on them almost overlap with their corresponding alignment marks on the design file, which has been shown in Fig 3.4b. As the number of terminals on the daughter board to plug in voltages and surrounding bonding pads separately connecting one terminal on the daughter board and one metal contact placed on the nanowires are limited, it cannot accommodate all nanowires to be fabricated for measurement. Therefore, only some nanowires with the best quantities of all can be chosen for the following processes.

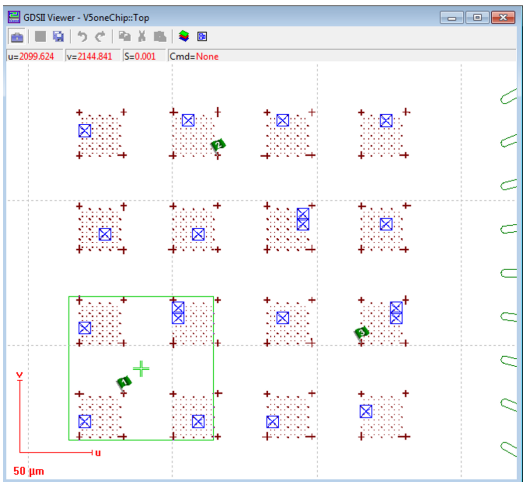
Each selected nanowire needs to deposit metal to produce contacts climbing over the segments of the nanowire at both sides of QDs, sidegates separately pointing to each QD with the same distance, and paths connecting contacts or sidegates with surrounding bonding pads. The arrangement of their positions will



(a)



(b)



(c)

Figure 3.3: Taking images of each deposited nanowire used to design devices for measurement by SEM on Raith eLine. (a) The real-time image collected by SEM zooming in on one alignment mark under magnification of 100,000 times. Green auxiliary lines make it easy to locate the center of cross markers. This position is recorded to correspond to the same position on the design file. (b) The deposited nanowires by using a micromanipulator taken under its optical microscope. Gold alignment marks build a coordinate to record the specific positions of each nanowire. The alignment marks used for aligning with corresponding markers on the design file are marked in red circles. (c) The setting of eLine to take detailed images of each deposited nanowire. Three alignment marks marked by green flags are chosen for building the one coordinate with corresponding alignment marks on the real chip, and the bottom left one corresponds to the alignment mark shown in figure (a). Lots of small regions circled by small purple squares are the scan regions of each deposited nanowire, which are selected according to figure (b) with the help of alignment marks. The sequence of imaging toward each region and the positions of all taken images on the design file are also recorded by the eLine system.

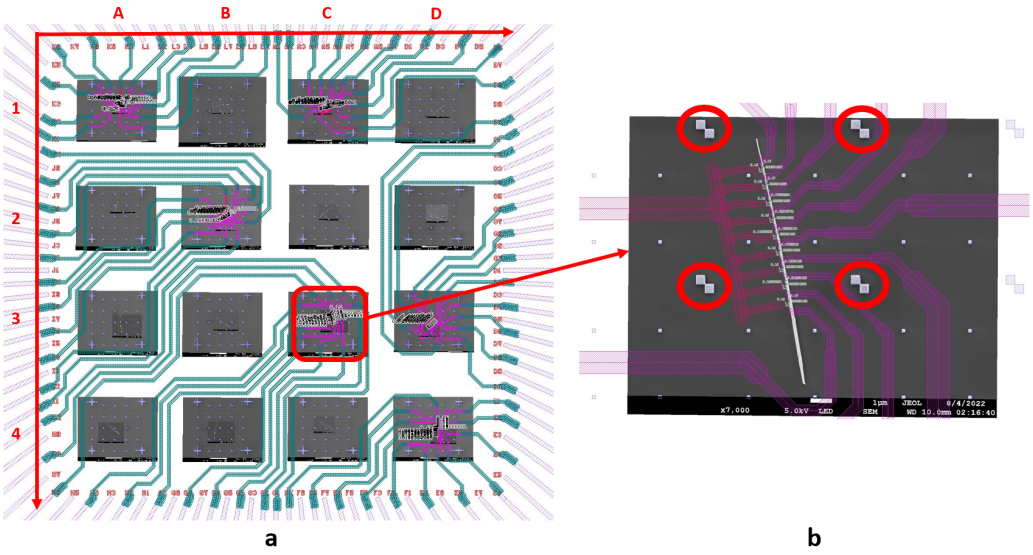


Figure 3.4: Using Klayout to design the circuit and devices on the selected 6 shot nanowires on QDev1248 to be fabricated for measurement. (a) The whole circuit designed for fabricating. All transferred nanowires have been imaged by SEM and put onto this design file by overlapping each group of corresponding alignment marks. All working areas are numbered according to the shown coordinate, and in the latter part of this thesis, each nanowire and its device will be represented as 'number-letter' (e.g., 2B and 3C) as its verticle and horizontal coordinates. By checking the quality of each deposited nanowire from its SEM image, six of them are chosen for designing devices. The methods of designing nanowires from different substrates are explained in the next Chapter. (b) Zoom in to the 3C device, which is numbered according to the coordinate system in Figure (a). All alignment marks on the SEM images and the design file are highly overlapped, marked by red circles.

be introduced in the next Chapter. As shown in Fig 3.4, the positions where metals are expected to be deposited are covered by patterns on the design system named Klayout. Then Fig 3.5 displays how to fabricate devices according to these designed patterns.

Step I. to step VI. on Fig 3.5 show the process of exposure with the electron beam lithography (EBL) technique in Elionix 7000, which is shown in Fig 3.1c. First of all, the surface of the base chip with deposited nanowires should be dispensed by Polymethyl methacrylate (PMMA) solution, then spin to make the covered PMMA uniformly distributed over the whole surface of the substrate. After baking, the PMMA over the surface will coagulate into Methyl methacrylate (MMA), which has a better resistance against dissolvent, for example, Isopropanol

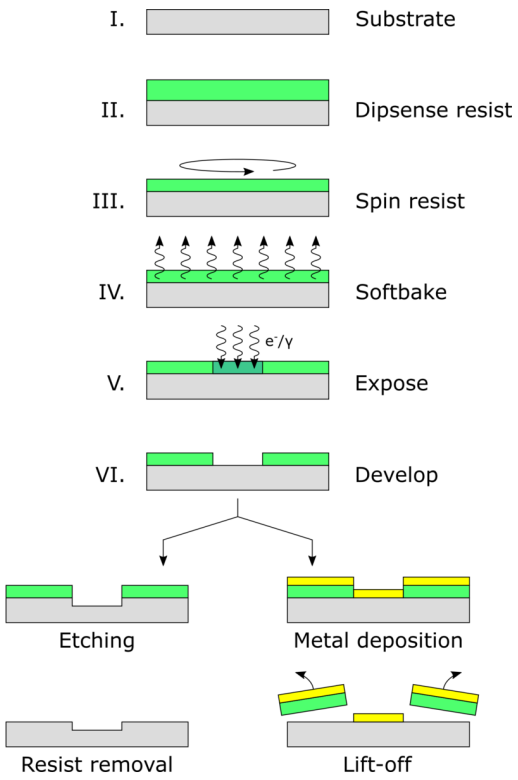


Figure 3.5: The whole progress of fabricating devices according to the designed patterns. Step I. to step VI. introduce the process of exposure within this section, and the rest steps are explained in the next section. This schematic is taken from the NBI cleanroom wiki.

(IPA) and Methyl isobutyl ketone (MIBK).

After MMA covers the surface of the base chip, the sample would be ready for exposure by using Elionix 7000. Loading or unloading samples of Elionix 7000 is similar to JOEL 7800F, then align each pair of corresponding alignment marks on the sample and its design file into the same coordinate, which is similar to the work on eLine. The exposure toward the sample is using the electron beam to break the chemical bonds between MMA molecules at the positions on the sample corresponding to the designed patterns on the design file. The exposed MMA is much more solvable as the chemical bonds are broken, so after exposure and then putting the sample into the solution of MIBK: IPA with a ratio of 1:3 for about 45 s, the weakened polymer placed on the positions of designed patterns would be dissolved, and because the rest MMA placed out of the patterns has not been exposed, it will not be influenced a lot as MMA has high resistance against this kind of dissolvent. Now the exposed positions are bare without being covered

by anything, with is shown in step VI. of Fig 3.5.

The thickness of deposited metal is mainly expected to be 150 nm, so to avoid the metal deposited on the exposed positions and expected to stay at the surface of the base chip connecting with the metal placed on nearby MMA, which should be removed after depositing metals, the thickness of MMA after baking should be high enough. This thesis adopts the value of around 300 nm, and it can be achieved by using A6 resist with a spin speed of 4000 rpm and baked for 2 mins under 185 $^{\circ}C$ [1].

Before exposure, the patterns on the design file should be divided into small constant pixels using the program Beamer. During the exposure, the electron beams remain on each pixel for the height and dose time on set values. Decreasing the size of each pixel or the current of electron beams effectively restrains the overexposure of the outermost pixels to maintain the exposed patterns having a closer size to expect. But relatively, it may take a much longer time, and the low current might be unable to radiate the resists at the very bottom closing to the surface of the base chip to make some residual MMA still stay at the exposed patterns after development. In this project, for all samples, the current uses 500 pA, and the area dose is always 1000 $\mu C/cm^2$.

Both SEM and EBL use accelerated electron beams toward samples for working. Therefore, substrates covered by polymer should not be characterized by SEM, or some undesirable positions might be exposed to influence the following process. During the alignment in SEM before exposure on Elionix 7000, it is necessary to choose alignment marks far away from the work regions with lots of patterns and avoid focusing on the substrate for a long time.

3.2.3 Metal Evaporation

After each process putting on polymer (e.g., exposure, develop, and lift-off displayed in Fig 3.5), it is necessary to use oxygen plasma to clean the epibiotic polymer or some other organic chemicals to improve the quality of fabrication. After exposure and plasma cleaning, it is available to deposit metal on the samples' surface using AJA.

In this project, the only metals used for fabrication are Gold and Titanium. Their melting points are not too high, so melting these two kinds of metal does not require a high current, which may harm the instrument and substrates. Therefore, electron beam vaporization (EBV) is adopted to deposit metal on the substrates.

After loading the sample, rotate the stage to make the sample face the crucible liners, where release atoms into the chamber. Before depositing metal, the exposed segments of nanowires where metal is expected to climb over should be cleaned by accelerated Argon atoms to remove the oxidation parts on the surfaces of these nanowires to make a better connection between the metal leads and

nanowires. After milling using Argon, switch to the high voltage power (10 kV) of EBV to acculturate electron beams to make the target metal evaporate and move up to deposit on the sample surface, which is shown on the 'Metal deposition' step of Fig 3.5. There is one sensor to detect the thickness of deposited metal, so it is easy and convenient to know when to stop depositing metal. For most samples, it requires depositing 5 nm Titanium as 'glue' and then depositing 150 nm Gold as leads for plug-in voltages.

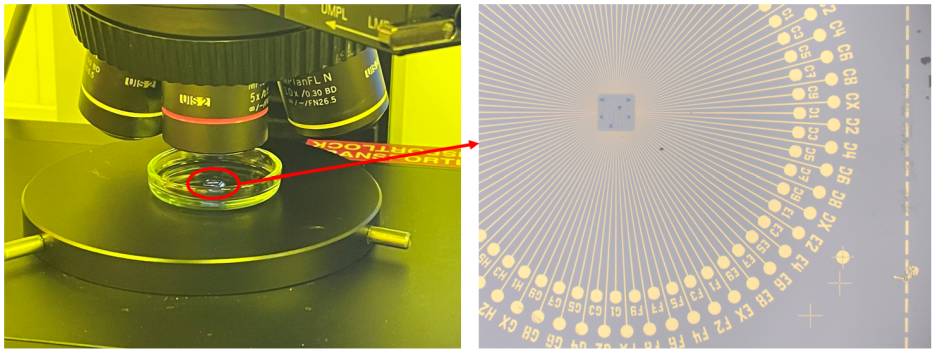


Figure 3.6: The left figure shows a sample covered by Acetone to check the result of liftoff. The right figure is the real-time image taken by the optical microscope to check the result of liftoff. For this sample, even though there are still some pieces of metal that have not been removed, the inner region covering bonding pads and working regions does not have large pieces to break the design for measurement.

After depositing metal on the samples, the next step is liftoff, which is dissolving the remaining MMA by putting the sample into more than 60 $^{\circ}C$ N-Methyl-2-pyrrolidone (NMP) or Acetone for more than half an hour. This step also takes away metal placed on MMA and only leaves metal leads that straightly contact the substrate or nanowires as expected. To check whether the liftoff is perfectly clean, the samples can be transferred to glass plats and covered by Acetone, which is shown in Fig 3.6, then check by using an optical microscope. If the surfaces of the samples become dry, it is hard to restart the liftoff process. If there are still extra pieces of metal that are not expected, try to blow them by using a pipette or Nitrogen gun, and even ultrasonication (but not recommended as it is easy to damage devices). If the results of liftoff seem clean enough under an optical microscope, move to SEM for more detailed checking of each device to make sure whether the fabrication mostly fits the design.

3.3 Measurement

After fabrication, the sample would be ready for measurement after bonding with the daughter board. Each contact of QDs, sidegates, and backgates of the base chip on the daughter has its own contact channel extending to the breakout box displayed in Fig 3.7b and c for plugging in external voltages, then loaded into the fridge for supplying low enough temperature for measurement.

3.3.1 Bonding on Fridge

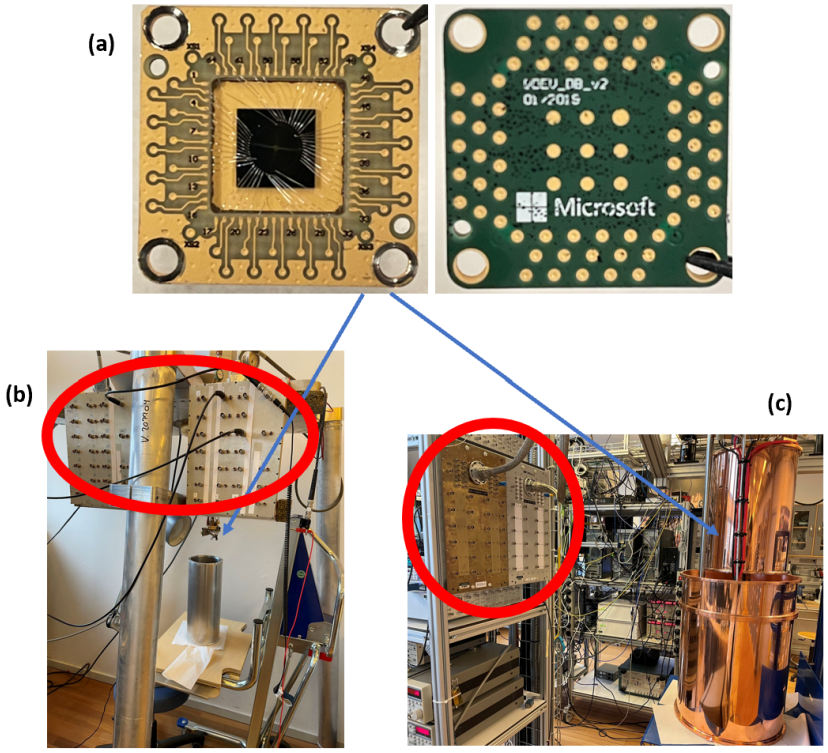


Figure 3.7: The preparation for measuring the samples under low temperature. (a) Both two sides of the daughter board. One substrate is bonded to it. On the front side, each loading pad of the daughter board is connected with one bonding pad on the substrate by an aluminum wire. The reverse side displays the pins to connect with the motherboard of two fridges: (b) Heliox and (c) Triton. Both breakout boxes supplying external voltages are marked in a red circle, and the blue arrow points to the positions holding the samples for measurement.

As each bonding pad on the base chip cannot straightly connect to the plug-in terminals on the breakout boxes shown in Fig 3.7b and c, on the front side of the

daughter board which carries the bonded base chip, each loading pad connects to one bonding pad on the base chip by an Aluminum wire, and the back side has pins which contact each loading pad on the front side to one specific port on the breakout box along the internal wiring of the fridge. Then it is available to supply external voltages to pointed devices on the samples.

Bonder can use one aluminum wire to connect two points by melting two nodes of the wire and pressing to improve the interface area between the bonding pad and the wire. After the condensation of melted metal, the two nodes cohere with these two bonding pads. The pressing force and melting power should not be too high in order to avoid breaking down the pads, which may bring huge leakages. Before bonding each pair of loading pads on the daughter board and bonding pads on the base chip, the base chip should be stuck in the center part of the daughter board via conductive glue (Leitsilber 200 Silver Paint) because all devices on the sample require supplying a backgate voltage.

3.3.2 Setup for Measurement

After loading the sample into the fridge, the measurement can start under the electrical setup as Fig 3.8. Both measurements using Heliox and Triton have used almost the same setup with the only difference in the temperature during the work.

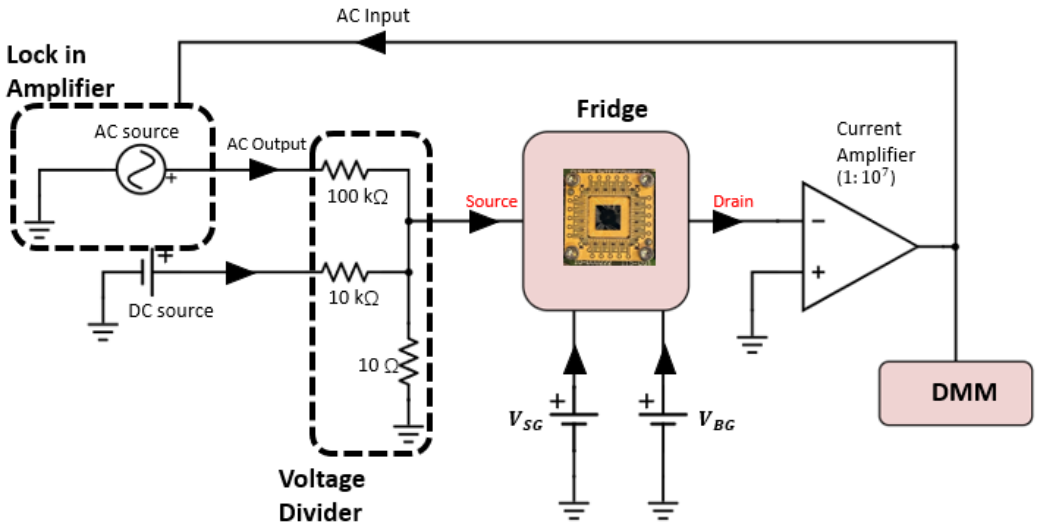


Figure 3.8: The measurement setup for both Heliox and Triton.

There are three direct currents (DC) sources generated by digital to analog converter (DAC) or Keithley and one alternating current (AC) source generated by the lock-in amplifier used in this project. Two DC sources are straightly connected

to the backgate and sidegate to supply gate voltages within ± 20 V. The other DC source and the AC source would meet up at a voltage divider, and the output from this divider is the device's source. After crossing the whole device, a DC current would flow out from the drain contacting to one port on the breakout box and then be measured by the DMM.

The insert of the AC source is mainly used to measure the differential conductance. This AC current generated by the lock-in amplifier would create a dV from the source, and then the signal with the same frequency flows out from the drain would be locked by the lock-in amplifier, which is recorded as dI. By using $G = dI/dV$, the differential conductance of the current device would be calculated. There are two extra external gate voltages (V_g) straightly act on the devices without joining the circuit above: the sidegate voltage (V_{SG}) and backgate voltage (V_{BG}).

For both Heliox and Triton, there are 48 contact channels with their own switches to float or ground their contacts which are shown in Fig 3.7b and c. When changing the connection to move to another device for measurement, ground the channels connected to all contacts of the nanowire holding the on-measuring device, then float all channels above to let current flow through that device for measurement.

Chapter 4

Results and Discussion

This Chapter contains research on two different kinds of nanowires with InAs/InAsSb heterostructures. The first growth of nanowires labeled as QDev1197 mainly focuses on finding the ideal parameters for growing gateable InAs/InAsSb QDs. Then following up on the results from QDev1197, a new growth recorded as QDev1248 was produced to study how the length of the QD and the barriers influence the formation of QDs.

4.1 QDev1197

At the beginning of the study on InAs/InAsSb heterostructure nanowires, the cure problem is how to fabricate well-defined QDs which are able to transport electrons in quantized. Three parameters are considered to research in this section: the temperature in MBE during the growth of nanowires, the width of QDs, which can be represented as the diameter of nanowires containing these QDs (controlled by the 'shot number' when growing these nanowires), and the thickness of InAs barriers forming QDs.

4.1.1 Structure of Nanowires

The growth of QDev1197 contains nanowires with a 'shot number' from 1 to 50, representing potential diameters from around 80 nm to 170 nm (at the position of each first QD). All nanowires contain nine QDs grown under three different temperatures: from bottom to top, for every three QDs, the growth temperature was switched from 447 $^{\circ}C$ to 440 $^{\circ}C$ to 433 $^{\circ}C$, and according to the difference of growth temperature, these nine QDs (denoted as QD1 to QD9 from down to top) are divided into three groups labeled as group A (QD1 to QD3), group B (QD4 to QD6), and group C (QD7 to QD9), which is shown in Fig 4.1.

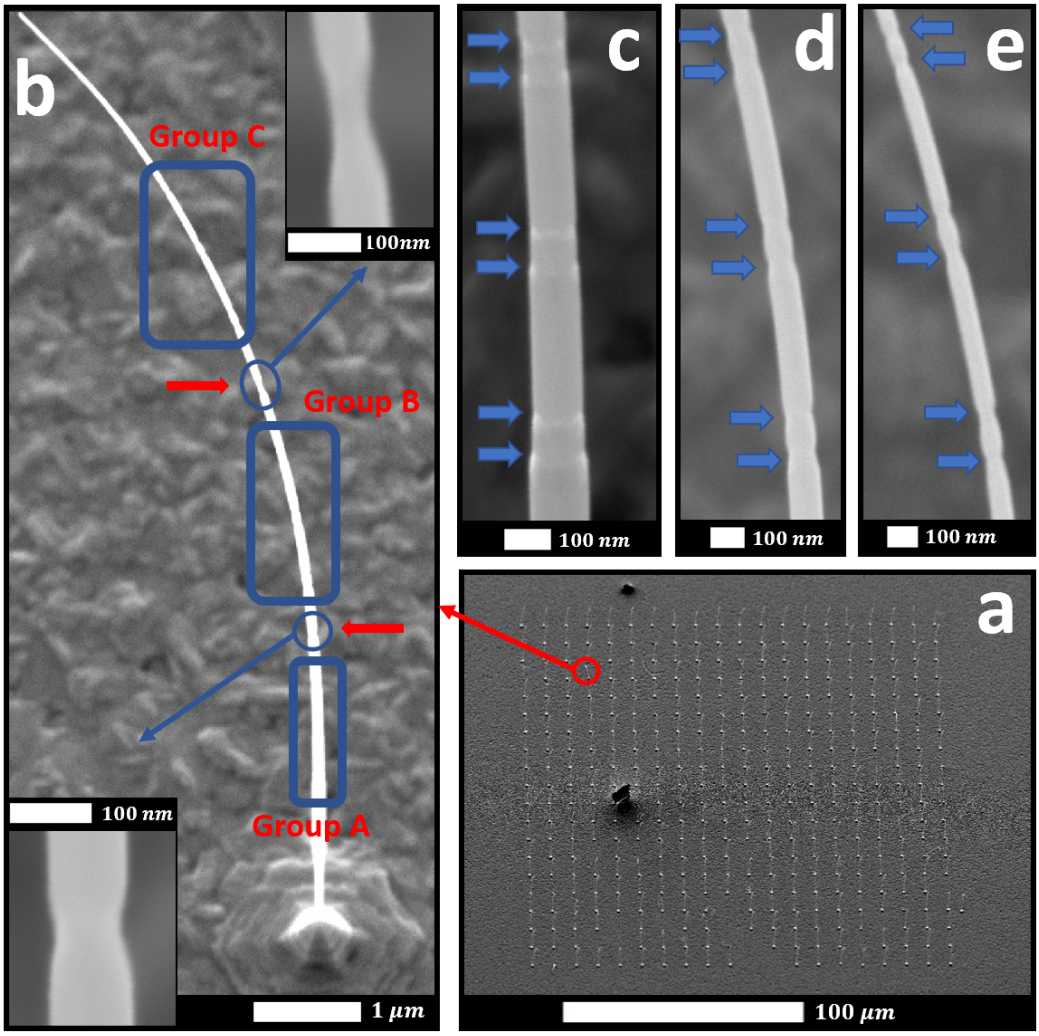


Figure 4.1: Observation of 1 shot nanowires on QDev1197 substrate in SEM. (a) One sample region of 1 shot nanowire on the substrate. The circled nanowire is selected to show the structure of this kind of nanowire. (b) Zoom in on the selected nanowire shown in (a). There are totally nine QDs on one nanowire. These QDs are divided into three groups (denoted as Group A to C) according to their different growth temperature. Between every two groups, one marker is designed and fabricated for identification. Two markers are indicated by red arrows and enlarged into two inset figures. (c-e) Zoom in on the QDs of groups A to C separately. Each group contains three QDs with a growth time of barriers as 15 s, 10 s, and 5 s (from bottom to top) when the grwoth time of segments between barrriers of all QDs is 20 s. All barriers are pointed out by blue arrows.

Fig 4.1 uses 1 shot nanowires as the example to show the structure of nanowires on QDev1197 substrate because barriers on this kind of nanowires are the most visible. During the growth, when switching to another temperature, a marker was fabricated by stopping the evaporations of all materials briefly. The markers are helpful in recognizing each group, and it is convenient for fabrication when depositing contacts as markers are designed at the midpoints between the last QD of the previous group and the first QD of the next groups.

Within each group, there are three QDs with a barrier growth time of 15 s, 10 s, and 5 s from bottom to top, and the growth time for the nanowire segments between each pair of barriers is kept the same at 20 s. The growth time for the nanowire segments between every two neighboring QDs (or QD and marker) is 2 mins to offer enough space to accommodate at least 200 nm contacts without touching QDs on both sides.

4.1.2 Fabrication for Measurement

After depositing nanowires on working areas surrounded by alignment marks through a micro-manipulator, as explained in Section 3.2.1, several of the most intact nanowires are selected to be employed in devices for fabrication by characterizing them in SEM. There are 48 bonding pads encircling the region for depositing nanowires. For each bonding pad, the inner end pointing to the center region with working areas accommodates one sidegate or contact touching one nanowire, and the outer end extends to external voltages through the internal wiring of instruments as explained in Section 3.3.1. Each nanowire used for measurement requires at least 11 bonding pads for connecting to supply voltages (one for sidegates and ten for QDs), so there are only three or four nanowires of all could be selected for fabrication. Fig 4.2a displays the sample of 8 shot nanowires as an example to show how to fabricate samples with QDev1197 nanowires.

All sixteen working areas on this sample have been numbered in the 'number-letter' form according to the coordinate displayed in Fig 3.4a. Fig 4.2b zooms in on the devices of the nanowire on position 1D shown in Fig 4.2a. Between every two neighboring QDs, one contact with a width of around 300 nm is designed and deposited at the midpoint of these QDs. If there is one marker at the midpoint of two QDs, the width of the contact was enlarged to maintain the distance from QD to the closer edges of contacts on both sides almost the same in order to exclude the influence from the different lengths of nanowires crossed by electrons before transport through QDs. Each QD has one sidegate pointing to it with a distance around 160 nm to 180 nm, which is close enough to make its supplied voltage affect the movement of electrons transported through the QD to make this QD gateable.

Another important aspect of nanowires on this substrate is the diameter of

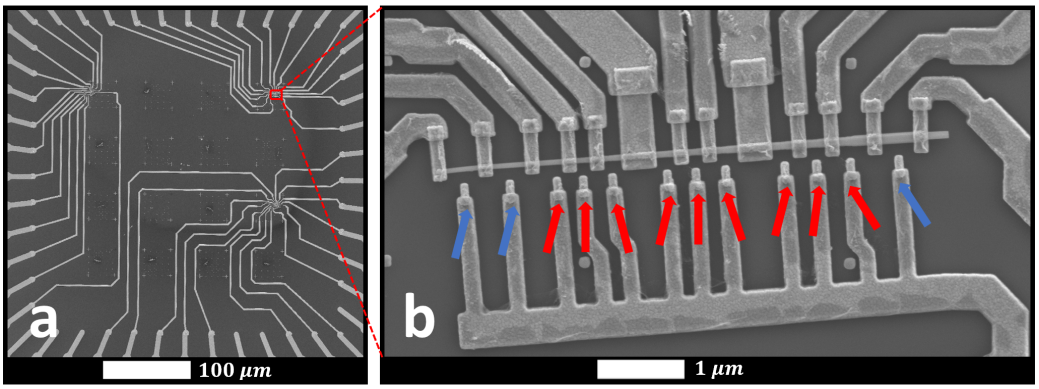


Figure 4.2: The sample with 8 shot QDev1197 nanowires, which is ready for measurements after depositing nanowires and evaporating metal contacts. (a) The whole fabricated device on the substrate. Three nanowires without damage and well deposited are chosen for fabrication. Sidegates and contacts are designed, deposited, and connected with encircling bonding pads. (b) Zoom in on the nanowire marked in figure (a) as an example to show the devices of each nanowire. Red arrows are put on sidegates which point to a QD, and sidegates with blue arrows point to some bare sections without QDs used as references. The distances from each sidegate to the nanowire are the same.

Au droplets which catalyze the growth of nanowires and are placed at the top of nanowires. For a larger Au droplet which is reflected in a higher 'shot number', the diameter of the nanowire becomes larger and the length of each nanowire segment grown under the same growth time becomes much lower, which has been explained in Section 2.1.2. Therefore, for nanowires with larger 'shot numbers', it is important to adjust the width and thickness of contacts in order not to touch their bilateral QDs and make the contacts able to climb the surface of the nanowire without breaking.

Besides QDs marked by red arrows in Fig 4.2b, there are several bare sections without QDs used as references for comparison. These references are regarded as devices with a barrier width of 0 and fabricated according to the same design as QDs (with sidegates, and the same length of nanowires between contacts and devices). But it is important to notice that the number of surrounding bonding pads is limited; therefore, there are not enough free bonding pads left for lots of references after bonding all contacts and sidegates of QDs.

The other ends of all sidegates are connected to a much wider metal strip. At first, it can save a large number of bonding pads whose numbers is limited, thus more nanowires on this base chip could be available for measurement; Second, as very thin sidegates with a width lower than 100 nm merge into a wide strip

with a width of around 500 nm, the risk of the very thin paths' breaking during exposure and evaporation would be decreased a lot; for the last, as all sidegates are connected, when moving to another QD or reference, it does not need to switch the connection of sidegates, thus the risk of damaging from electrostatic when attaching or detaching the voltage supply would be decreased a lot. Therefore, combining all sidegates and connecting them to one bonding pad is adopted.

4.1.3 Overview of Measurement

In order to find out the ranges of growth temperature and 'shot numbers' with more well-defined QDs, several samples with different 'shot numbers' are fabricated, and all devices on each sample are measured under the same conditions. The whole work started with nanowires of 1 shot. After that, skipped to 4 shot and 8 shot for fabrication and measurement as the difference in diameter between nanowires with adjacent 'shot numbers' is not prominent observed in SEM. According to the measurement results above, overall, fewer QDs of 8 shot and 1 shot samples behave as well-defined QDs than 4 shot. To test whether the decreasing number of well-defined QDs would continue along the improvement of 'shot number', 25 shot and 50 shot were chosen and adopted the same fabrication and measurement as previous samples, and the results fit the inference of diameter. Then moved to the 6 shot nanowires, which are surmised as having the highest percentage of QDs displaying clear resonances and CBs. The measurement on the fabricated 6 shot sample verified this mind.

Therefore, the research on nanowires on the QDev1197 substrate contains six samples (with 'shot number' of 1, 4, 6, 8, 25, and 50), and on each sample, devices numbered as QD1 to QD9 on three to four nanowires are measured. Unfortunately, during the measurement, a large number of devices were unable to conduct electricity. Some of them had too huge resistance and when supplying huge V_g, stable currents could be detected. But for most unworkable devices, they might have been damaged before supplying voltages to them, which was determined by characteristics after measurement in SEM.

All the measurements above are achieved in Heliox, which offers temperatures between 300 mK to 2.6 K for measurement. By comparing the plots of dI/dV conductance with sweeping gate voltages under different temperatures between 300 mK and 2.6 K on the same devices, the behavior of conductance with respect to gate voltages mostly seems not very similar. But at lower temperatures, the electric noise seems insufficient as low temperatures restrain the electron scattering [7].

The results of measurement on all devices of all six samples above are divided into four different groups except devices that cannot conduct electricity. All these four different behaviors are explained and show examples in Fig 4.3. Fig 4.4

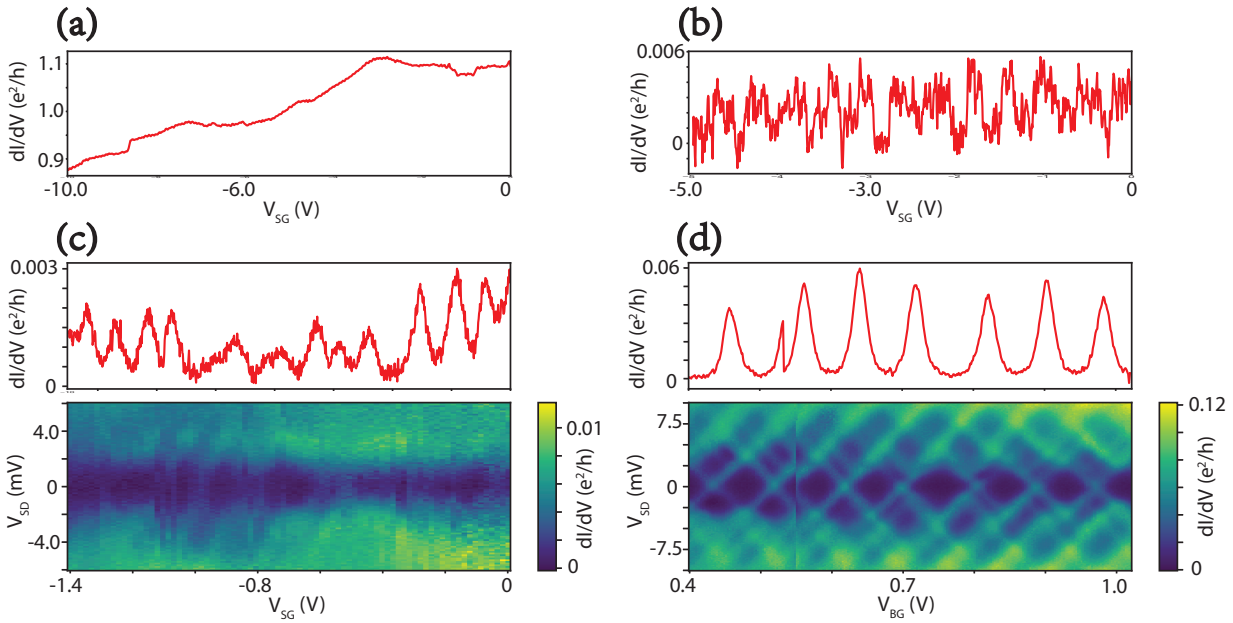


Figure 4.3: Models of gate characteristics and corresponding conductance dI/dV as a function of V_{SD} and V_g, which has been introduced in Chapter 2, to group the measurement results of all devices fabricated by nanowires on QDev1197 into four different types shown in Figure 4.4(a) The sample of **'Very open'** in Fig 4.4, which is measured on one QD1 of the 50 shot sample under V_{BG} = -5 V. The plot of conductance is a flat curve and always stays at high values without pinch-off. It means that most electron channels are very hard to close and always keep open. (b) The model of **'Too closed'**, which is measured on one QD7 of the 8 shot sample under V_{BG} = -5 V. It always stays at very low conductance, which means that electron channels are mostly closed. Coulomb blockades do not exist in both two models above. (c) Using one QD3 of the 4 shot sample under V_{BG} = 0.3 V as example of **'Noisy periodic spikes'**. There are periodic spikes of conductance, but the magnitudes, widths, and positions of the valley of these spikes are very different, so they may not have conductance resonances. (d) Measured on one QD8 of the 6 shot samples V_{SG} = 10 V, which has **'Clear resonances'** and classical CBs with the same diamonds periodically.

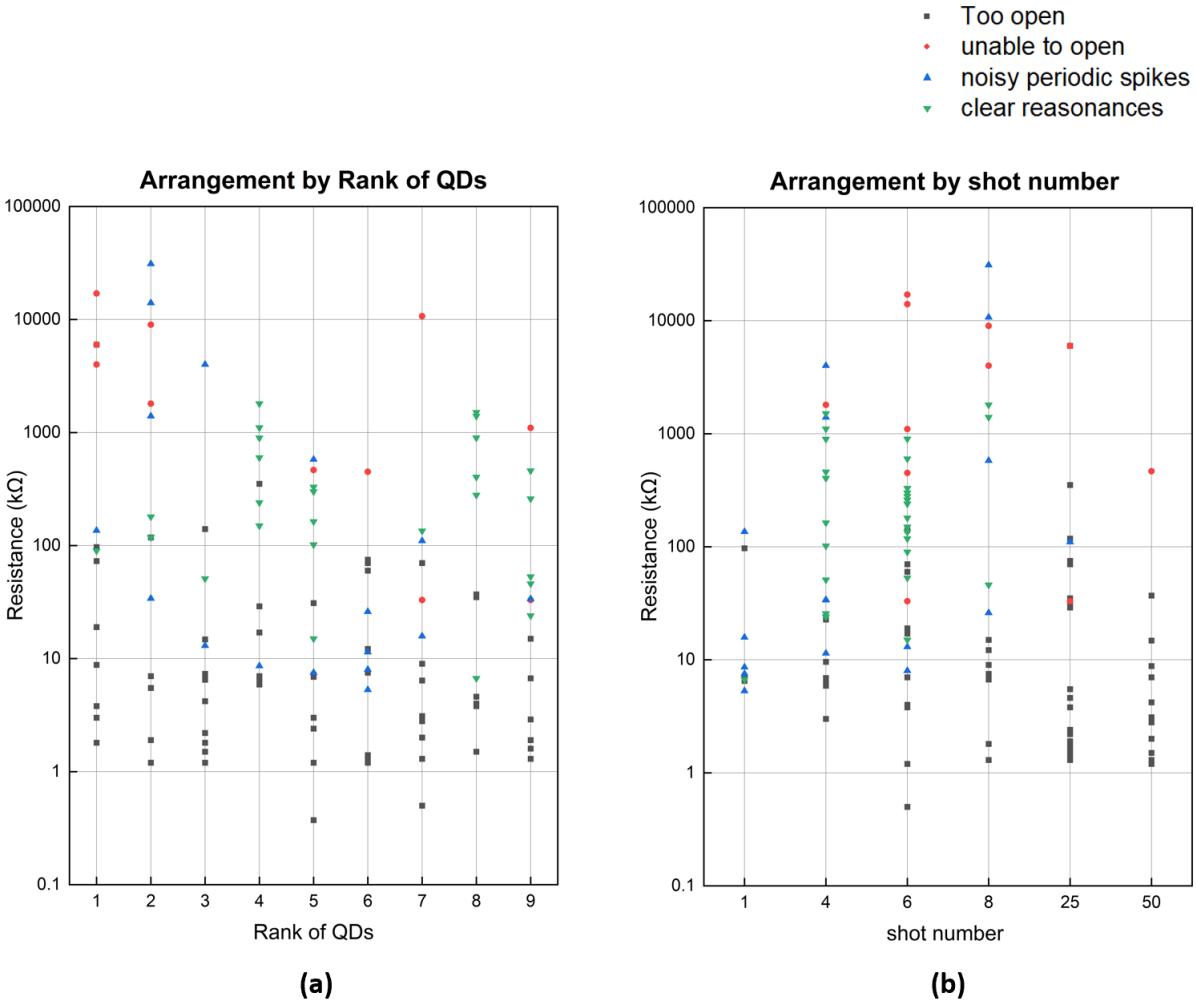


Figure 4.4: The resistance distributions of all devices on QDev1197 samples without supplying gate voltages or bias. The data are arranged according to (a) the rank of devices on nanowires (QD1 to QD9) in order to research different growth temperatures and (b) different 'shot numbers' of nanowires to research the width of QDs.

shows the resistance distribution of all devices without supplying gate voltages at zero bias, and each device belongs to which group shown in Fig 4.3.

Fig 4.3a and Fig 4.3b show two examples of ungateable devices. Devices in the first group labeled as 'very open' on Fig 4.4 always have high conductance and low resistance. Therefore, it is hard to turn off electron channels to pinch off even though supplying gate voltages to the highest rated values. Devices in another group labeled as 'too closed' go to another extreme: their conductance keeps at low values close to 0, and even though supplying positive gate voltages, most electron channels still cannot be opened. This kind of devices mostly have a huge resistance which limits the transport of electrons. Devices working along Fig 4.3c or Fig 4.3d are available to display continuous conductance spikes. Devices behaving as displayed in Fig 4.3d have clear resonances and CBs, and this kind of devices might be well-defined QDs, whose growth parameters are expected to be adopted for further production. Devices working along Fig 4.3c seem to behave closely to QDs, but each conductance spike is very different from others, including the conductance amplitude and the width of each spike. This phenomenon cannot be interpreted as quantized electrons transport through. Instead, it might be that some other particles are emitted or caused by some other reasons. The conductance as a function of bias voltage and gate voltages also does not display clear CBs. Therefore, this kind of devices cannot be identified as well-defined QDs.

The results of measurement on all devices on the 1, 4, 6, 8, 25, and 50 shot samples are listed in Fig 4.4 grouped into four different kinds according to the previous introduction. Fig 4.4a arranges all results by the rank of devices on each nanowire from QD1 to QD9, and Fig 4.4b arranges by different 'shot numbers', which mainly indicates the diameters of nanowires. Both figures show that well-defined QDs are gathered within resistance between 100 to 1000 $k\Omega$. Below that range, the conductance would be too high to pinch off, and above this range, the conductance is mostly too low to have channels for electron transport.

Fig 4.4a arranges all results according to the rank of QDs. It displays at which ranges of temperature have more well-defined QDs. Under different temperatures, the deposition rate of each element is different. For lower temperatures, the grown layers become broader [25] [28], and these properties might influence the transport of electrons within. On statistics, QD7 to QD9, grown under 433 $^{\circ}C$, behave the best as a larger percentage of well-defined QDs gathered in this group within all three selected temperatures. Therefore, for the following growths of InAs/InAsSb nanowires, 433 $^{\circ}C$ was chosen for fabrication. However, within these three selected thicknesses of barriers (with growth time for 20 s, 10 s, and 5 s), their conductance and ability to be gated do not have differences with some regularity. It might be that when the ratio between the axial length of the barriers and QD reaches a high enough value to constrain the conductance to be able

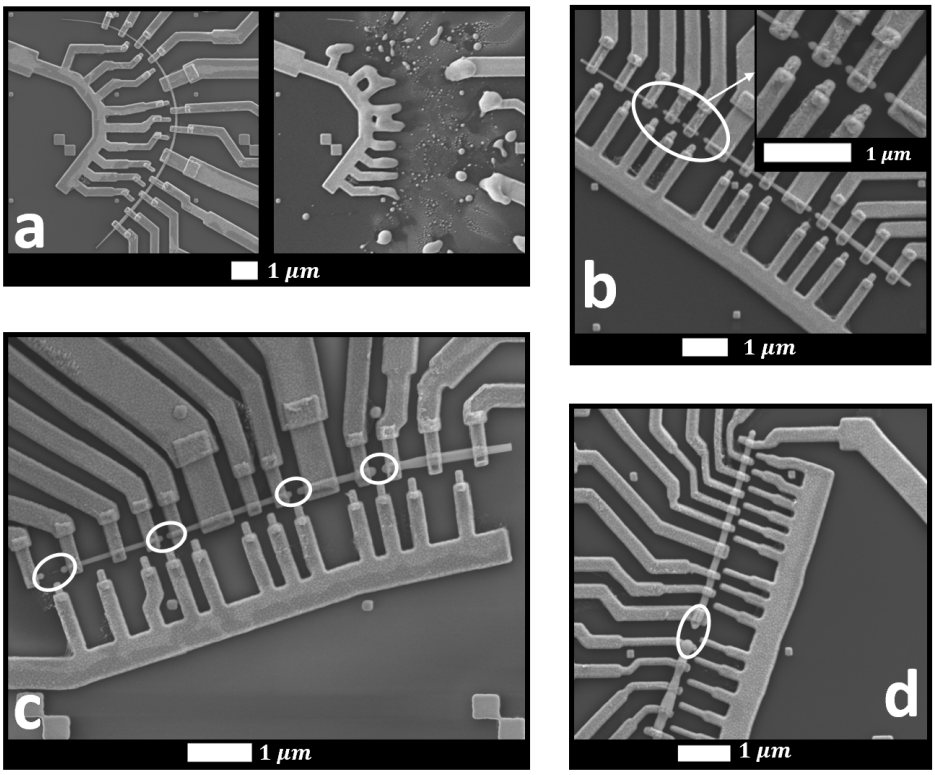


Figure 4.5: Some damages of samples after measurement in Heliox imaged in SEM. (a) The comparison of the nanowire at the 3A position of the 1 shot sample before and after measurement. (b) The nanowire at the 2C position of the 4 shot sample after measurement. Inset figure zooms in on the continued damaged devices. (c) The nanowire at the 3D position of the 8 shot sample. (d) 1D of the 50 shot sample. Damaged positions are marked in white circles.

to pinch off, it may exist a range of this ratio where the increasing of the barrier length does not effect the behavior of the QD. Further research on barriers will be continued on the work of QDev1248 samples, which will be explained in the next section.

Fig 4.4b arranges all results according to the 'shot numbers' of the on-testing nanowires, which represents the influence of different diameters of nanowires. It shows that nanowires on the 6 shot sample have a higher percentage of well-defined QDs. For higher 'shot numbers' (8, 25, 50), as the diameters of the nanowire (and also the width of QDs) improves a lot, the area of the cross-section becomes much larger to accommodate more electrons transport per unit of time, and the effectiveness of gate voltages applied to QDs becomes worse. For lower 'shot numbers', as the diameters are too low, supplied gate voltages might be also

hard to control the QDs as their conductance stays at a lower level and it is easy to damage the QDs as these nanowires are too narrow to oppose static electricity.

The different appearances imaged in SEM of the samples with different 'shot numbers' after measurement may explain how different diameters of nanowires influence the control effect of supplied voltages toward the devices. The measurement of QDev1197 by Heliox contains a large number of nonconducting devices and damages when measuring. After each measurement, the sample is characterized in SEM to check the condition of each device. Fig 4.5 shows several figures of nanowires on the 1, 4, 8, and 50 shot samples after measurement. After not so long of starting to measure devices on the 1 shot sample, the whole sample lost conducting, and by checking in SEM, it showed that all nanowires fabricated for measurement are exploded, shown in Fig 4.5a. A similar thing happened in the measurement of the 4 shot sample, but the explosion only took place on half of one nanowire. There are still a large number of broken on gated positions (including QDs and references) shown in Fig 4.5b. Then as the 'shot number' becomes higher, the break of nanowires becomes less, but instead, there is still some damage on devices, which is obtained by comparing the measurement of the image with them before measuring. On the whole, the deposited sidegates with widths of around 100 nm and laying 200 nm away from the devices are hard to control devices with larger diameters effectively; however, they over-forced on devices with lower diameters to make them easy to be damaged.

The 'shot numbers' do not only determine the diameters of grown nanowires, as explained in Section 2.1.2, for nanowires with bigger sizes of Au droplets, the nucleation of each layer would spend much longer time because of the finite supplyment of In under As-rich conditions and the large area of the layers, so for segments at the same positions on nanowires with differen 'shot number', the higher 'shot number' brings bigger diameter and smaller length under the same growth time. Therefore, the comparison of the same devices on nanowires with different 'shot number' in direct is hard to be reflected in the sizes of the grown QDs. Instead, as the growth time of segments are determined, the ratio of the lengths of barriers to segments between their barriers of QDs at the same positions of nanowires with different sizes of Au droplets contains the same, and the variable can be ascribed to the ratio between the barrier's axial thickness and its QD's radial length.

Unfortunately, due to the high defect rate of devices and the very low number each kind of samples, it is hard to zoom in on the same QDs with differences between the barrier's axial thickness and its QD's radial length (for example, researching on all QD7s at nanowires with different 'shot numbers', which was grown under 433 $^{\circ}C$ with the ratio of their axial lengths between barriers and QD determined by their growth time is 15 s : 20 s). For the overall resistance of all devices which shown in Fig 4.4b, the main range of the resistances of most de-

vices are moving down as the increase of 'shot numbers', and at the same time, the devices become harder to be gated as ths conductance becomes too high to pinch it off. Therefore, for QDs on the QDev1197 substrate, the ratio between the barrier thickness and the radial width of the QD is more effective on determine the QD than the ratio between the axial length of the barriers and the QD, and the latter factor will be researched on devices of the QDev1248 substrate shown in the following section.

More skillful operations on measurement may play an important role in decreasing terrible damages. However, even till the last measurement on the 50 shot sample, visible damages to the devices are still inevitable. Measuring under a much lower temperature might be helpful in restraining the scattering of electrons and decreasing the static electricity to receive more stable results and protect the devices [41] [7]. In the following work, it is a critical reason for using Triton, which offers a much lower temperature for measurement.

4.2 QDev1248

This section researched how the length of barriers and the length of QD influence the work of QDs, including the ability to quantize the transportation of electrons, the formations of their CBs, and the change of their conductance (G), addition energies (E_{add}), and addition voltage to emit one more electron (ΔV_g).

4.2.1 Structure of Nanowires

From the research of nanowires on the QDev1197 substrate, nanowires grown under the temperature of 433 $^{\circ}C$ would be more beneficial to get more gratebale QDs, so 433 $^{\circ}C$ is the only adopted temperature for growing nanowires on QDev1248 substrate.

The research on QDev1248 nanowires mainly focuses on the 3 shot nanowires whose QDs have several different typical conductance behaviors under gate voltages, for example, clear conductance resonances in several regimes, smoothly plotted conductance with high magnitudes, and pinched-off of almost all charge carrier channels. Fig. 4.6 shows a 3 shot nanowire of the QDev1248 substrate deposited on a base chip for fabrication.

Each nanowire on the QDev1248 substrate has seven markers and six DQs. Markers are clear depressions on the surface of the which are the same as the markers on nanowires on the QDev1197 substrate. They are easily visible in SEM, and the distances between every two neighboring markers are mostly the same. These markers are designed to deposit metal contacts for plugging in bias voltages, and they also assist in locating the positions of each QD as all QDs are located

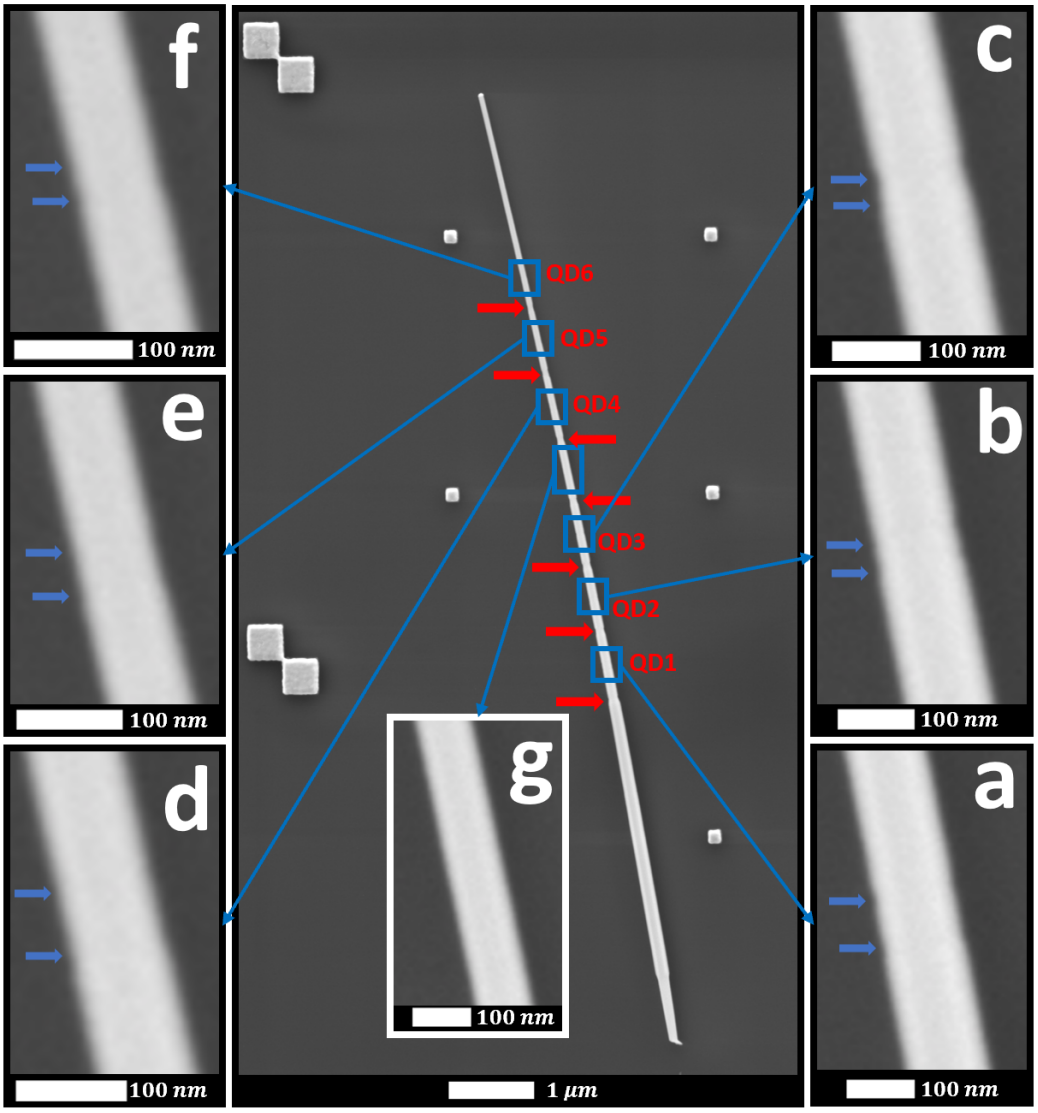


Figure 4.6: The deposited 3 shot nanowire at the 3C position on the base chip. Red arrows point to the markers which are easy to be visible in SEM and designed as the positions to deposit Au contacts. (a-f) Zoom in on each grown InAs/InAsSb QDs. Blue arrows point to the barriers of QDs whose diameters are obviously smaller than their nearby segments. (g) Zoom in on the nanowire segment between the middle two markers. There are no barriers, and this region is treated as a reference for comparing with QDs.

close to the midpoints of two markers except QD6. Each QD is formed by two WZ (InAs) barriers and one ZB (InAsSb) segment between barriers. The positions of these barriers are clearly shown in Fig. 4.6 (a) to (f), so it is easy to distinguish where these QDs are, and it is clear that between the middle two markers, there is no QD in this region. Be true this region is designed as one reference without barriers to comparing with QDs. The differences between QDs on the nanowire and the selection of each reference will be introduced in the next section.

4.2.2 Fabrication for Measurement

Besides the six QDs and one reference introduced in the previous section, two more references are designed for measurement together. Fig. 4.7 shows the sequences and structures of all these six QDs and three references after fabrication. As nanowires go narrower from the root to the top, the widths of these three references are very different as each of them is far away from the others. Thus, the influence of the nanowire's diameter toward conductance would be prominent within these references. Several devices are not covered by markers, but the positions of the deposited contacts can be calculated from the distances between every other two neighboring marks. Each segment between every two contacts should be almost the same to guarantee that the current flows through the same length of the nanowire. For these six QDs, the growth time of barriers is 5s for the first three QDs (categorized as group 1) and 2s for the second three QDs (categorized as group 2. Three references are categorized as group 3). Within each group of QDs with the same growth time of barriers, the growth time of the ZB segment between barriers is respectively 20s, 10s, and 5s from bottom to top. The distance between every two neighboring QDs in the same group is not as large as the reference, so the influence of QD behaviors from the difference in diameter is negligible. Therefore, the different behaviors of QDs in the same group can be attributed to the difference in the length of QD (also the length of the InAsSb segment between two barriers). It is hard to directly compare QDs with the same growth time of ZB segments between barriers (e.g. QD1 and QD4) in different groups because of the difference in their widths caused by their long distances.

As the positions of each device on these deposited nanowires are visible and clear in the images taken by SEM, it is easy to decide the positions of sidegates whose midpoints are expected to point to the center of QDs. Each sidegate should cover the whole directed side of the QD (both WZ barriers and ZB segment). Initially, there were always inevitable misalignments on most devices during the exposure. After a series of misalignment tests, it was detected that there was an inevitable misalignment with around 20 to 40 nm on both vertical and horizontal directions on this batch of base chips. Therefore, the width of sidegates is designed as 100 nm longer than the average length of QDs in order to guarantee

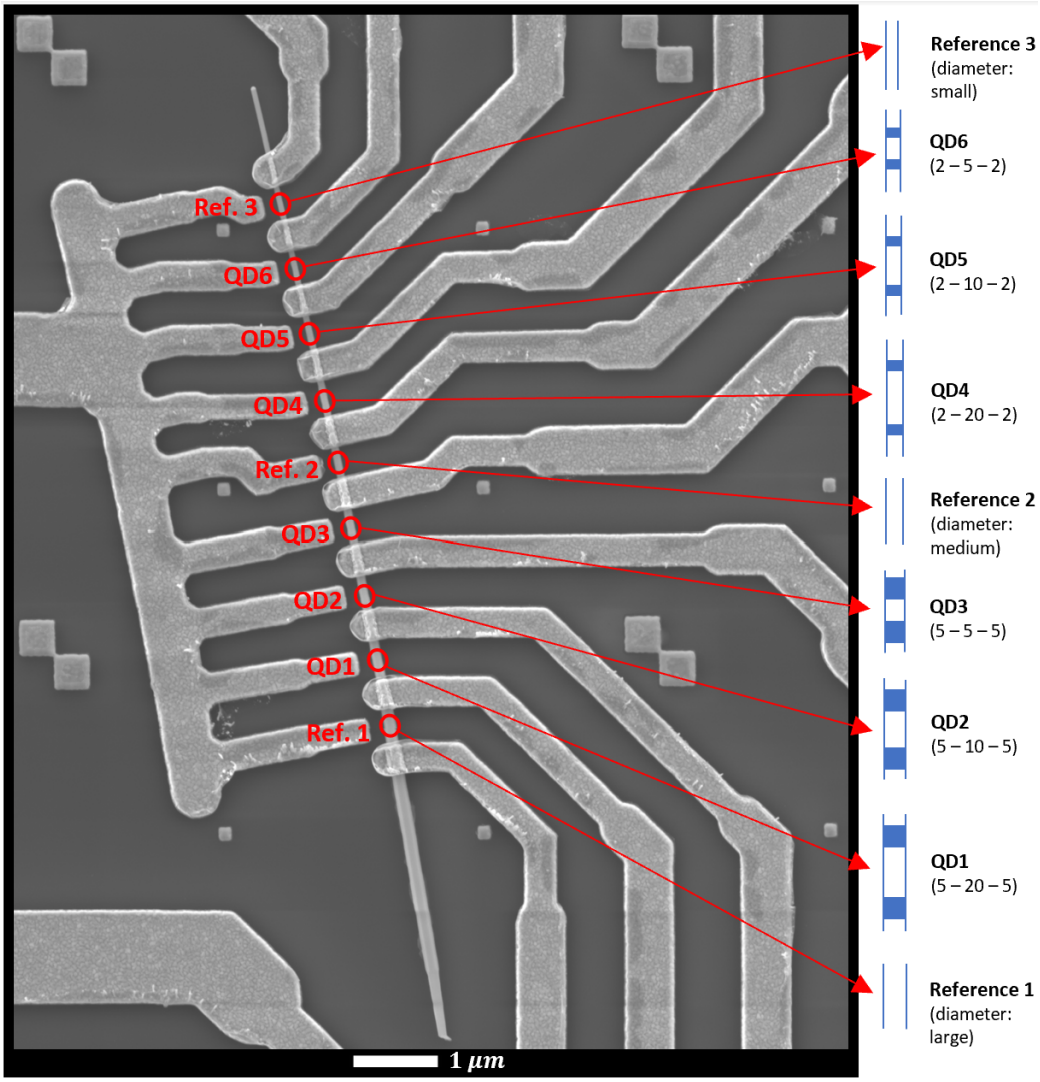


Figure 4.7: The nanowire at the 3C position of the fabricated 3 shot sample of QDev1248 substrate. This figure displays all devices for measurement. The positions of all devices (six QDs and three references) are marked, and the inset figures display the differences in each device's structure. For QDs, it shows the growth time of each segment (in the form of barrier-dot-barrier).

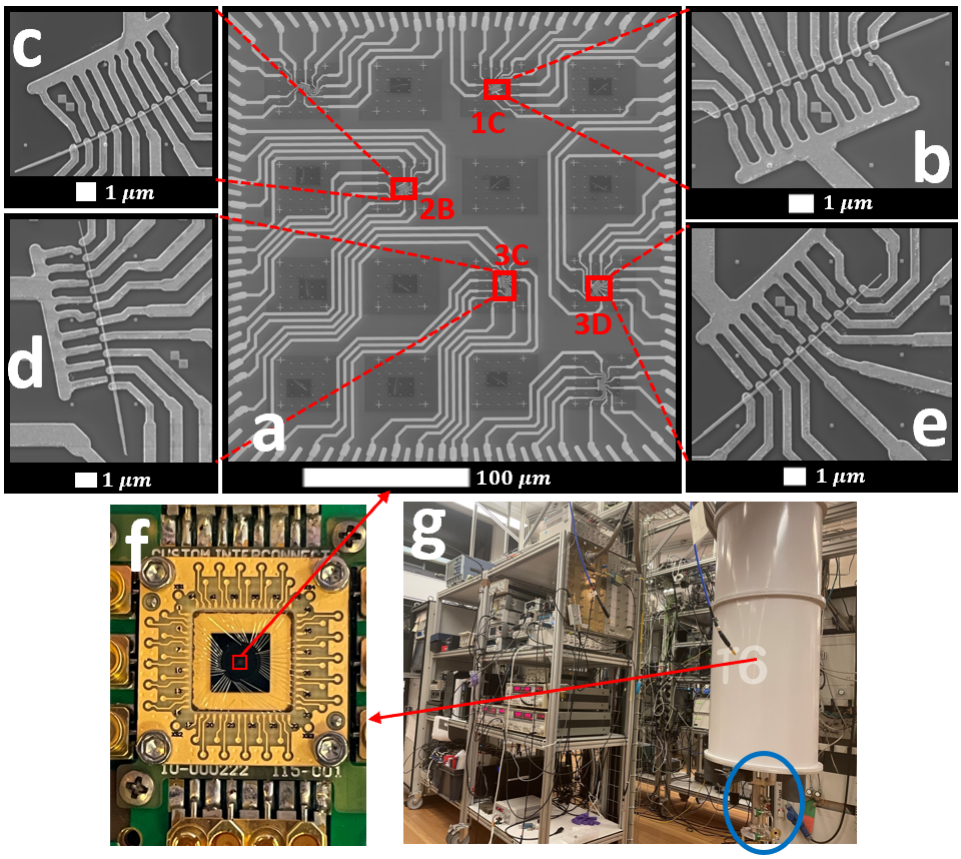


Figure 4.8: (a) All fabricated devices connected with bonding pads. Four of them, labeled as 1C, 2B, 3C, and 3D according to the the coordinate shown in Fig. 3.4a, are selected to bond with the daughterboard for measurement. (b-e) Zoom in on each selected nanowire. The contacts and the sidegate is bonded with their individual loading pads on the daughterboard through the encircled bonding pads on the base chip. (f) Silicon substrate with all samples sticks to the daughter board using silver glue. All bonding pads are linked to the loading pads on the daughterboard by aluminum wires. The marked-out area is the region for fabrication which is shown in Figure (a). The daughter board is held on the motherboard of cold-finger SMP bullet receptacles, which carries the sample and links it with the Triton. (g) Triton 6, the Dilution fridge cools down the sample to 27 mK for measurement. The handle marked in a blue circle is used to load the sample into the fridge and transfer it between different chambers.

that all QDs can be covered by their sidegates even though the fabricated device shifted a lot comparing with the pointed patterns on their design files. The distances between sidegates and the devices each sidegate points to are set as 150 nm to maintain the fabricated distances staying at the range of 100 to 200 nm, which is the most suitable distance for gating QDs by supplying V_{SG}.

Fig. 4.8 shows the four devices whose contacts and sidegates coincide well with their expected positions, and there are also no damages to the devices on these nanowires during the fabrication. These four devices are labeled as 1C, 2B, 3C, and 3D according to their positions on the base chip by using the same coordinate as Fig. 3.4a. This sample with all devices would be affixed to the daughter board and bonded each pair of bonding pads on the base chip and loading pads on the daughter board as explained in Section 3.3.1. After finished bonding, the sample would be held on the motherboard of the cold-finger SMP bullet receptacle and then sent to the main chamber of the fridge for measurement.

4.2.3 Overview of Measurement result

After cooling down the temperature to 26 mK, the measurement in Triton can be started. Before starting the measurement of each device, it is necessary to check the leakage of both sidegates and backgates by tracking the change of leaking current when increasing each V_g slowly. If the leaking current rapidly increases, stop the increase of V_g immediately to avoid further damages from high leakages. If the leaking current keeps at low and stable values, the device will be safe to try much higher gate voltages. By testing each instrument, both the sidegates and backgates of all these four nanowires can safely work within -10 V to 10 V with a leaking current lower than two $\times 10^{-9}$ A, which is low enough to guarantee their security.

Table 4.1 shows the results of the measurement of all four devices. In this table, each device (reference or QD) on each nanowire contains three factors: The first one is whether these devices can pinch-off under different gate voltages, and their background color shows the rough range of V_g to start pinch-off according to the color bar in Fig 4.9. For a gateable QD where well-defined CBs are able to be observed by adjusting the supplied V_g. Initially, it is open transport without charging effects on a high conductance background; then, as the gate voltages increase, the conductance goes lower and gradually yields Coulomb oscillations, and when pinch-off, record the current V_g on Table 4.1. At this condition, well-isolated CB peaks would be observed [5].

The second factor is the description of electron transport and its CB formations if the device is gateable. Fig 4.10 shows some sample plots of different electron transports observed during the measurement of this sample which is explained by their conductance with respect to gate voltages and their corresponding

Table 4.1: Overall Display of Measurement

	1C			2B			3C			3D		
Rank of QD	Pinchoff	Comment	R [kΩ]	Pinchoff	Comment	R [kΩ]	Pinchoff	Comment	R [kΩ]	Pinchoff	Comment	R [kΩ]
Ref 1	No	Very open	9.5	No	Very open	9.5	No	Very open	9.5	No	Very open but noisy	9.5
1	Easy	Resonance with Kondo	151	No	Very open with low G	15.7	Easy	Resonances with Kondo	21	Hard	Resonances with Kondo	40
2	No	Too open to see resonances	18	Easy	Very open with even lower G	37	Very easy	Resonances but less Kondo	75	Easier	Resonances but less Kondo	15
3	Very easy	Very open and easy to be closed	48	Always	Very closed, but can open at +V	220	Very easy	Very open and easy to be closed	18	Very easy	Very open, closed with high bias	19
Ref 2	No	Very open	9.8	No	Very open	10	No	Very open	10	No	Very open	10
4	No	Very open, but able to gate a little	10	Always	Very closed, but can open at +V	220	Hard	Very open, more gated at high bias	12.7	No	Very open with very low G	16
5	Very hard	Very open	14	Hard	Very open, but roughly resonances	11.4	Easier	More open, more closed at high bias	14.5			
6	Hard	Very open, closed with high bias	20	Very easy	A little clearer, but soon closed	47	Very easy	Even more open and closed	28	Easy	Very open, easier to pinch off	15
Ref 3	Very hard	Very open, may gated at high bias	12	Easy	Very open and easy to be closed	12.3	Hard	Very open, seems a little gated	12	No	Very open	12

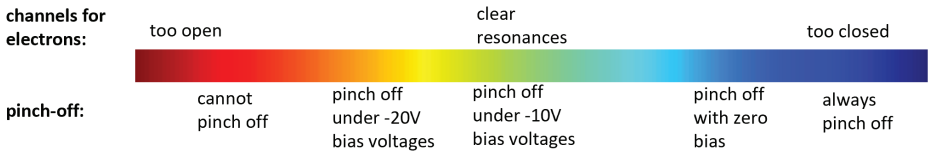


Figure 4.9: Color bar corresponding to different conditions on Table 4.1. The upper coordinate displays the properties of electron transport applying to the list of 'channels for electrons': the more to the left, the device is more open and harder to be pinched off, and the more to the right, the device is more often to be pinched off with almost zero conductance; The bottom coordinate shows the difficulties of pinch-off of this device acting on the row of 'pinch-off': the more to the left, it requires more negative gate voltages to pinch off this device, and the more to the right, the supplies gate voltages are required more positive.

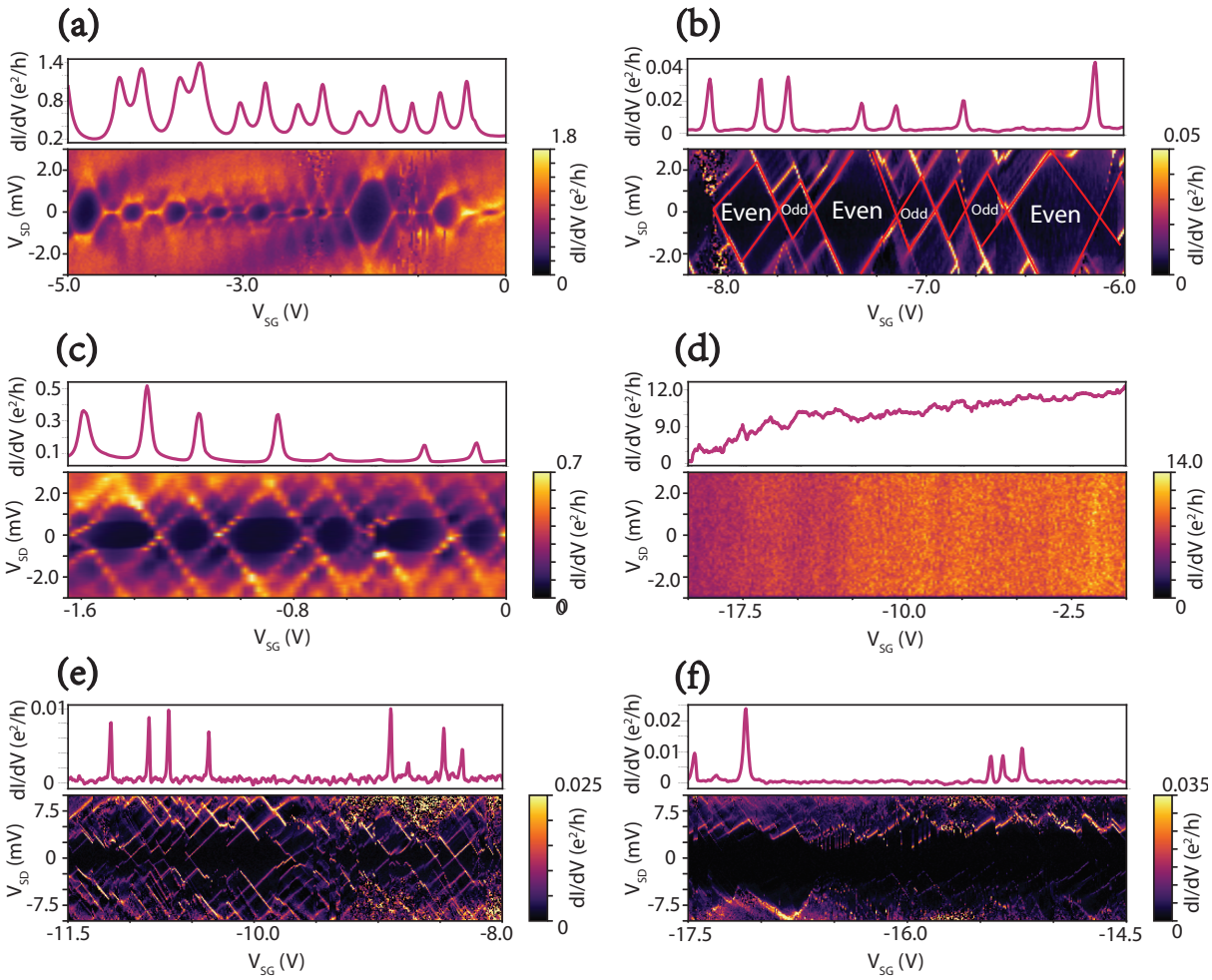


Figure 4.10: All models of electron transport regimes collected from the measurement on the 3 shot sample of the QDev1248 substrate. These models are also mentioned in Table 4.1, and each of them has been introduced in Chapter 2. (a) The plot of V_{SG} without supplying V_{BG} of the QD1 at 1C, whose conductance resonances and CBs display Kondo effect. (b) The sample measured on the QD2 at 3C under V_{BG} = -10 V which displays CBs with switching large and small sizes of diamonds (labeled as even and odd). Using red full lines as auxiliaries to highlight some unclear edges of Coulomb diamonds with low conductance. (c) The plot from the QD1 at 1C under V_{BG} = -10 V, whose CBs behave similarly to classical CBs, as the vertical lengths of each diamond are almost the same. (d) The QD4 of 1C without supplying V_{BG}, which does not display conductance resonances or CBs as its conductance is too high to pinch off. (e-f) Different display of CBs under different ranges of V_{SG} under V_{BG} = -20 V of the QD2 of 3C. Even a few Coulomb peaks still exist, and most electron channels are closed. (e) is at a lower range of V_{SG} and (f) is at a higher range.

CBs when supplying finite V_{SD}. As the temperature for measurement on Triton is much lower than Heliox, the Kondo effect reflected on both conductance, and CBs (Fig 4.10a) is available to be observed under low enough temperature [24]. But for other gateable devices, the conductance keeps pretty low, so the Kondo effect is not prominent to be displayed. At that time, sometimes the precondition for classical CB as $\Delta E \ll k_B T$ is not satisfied [18]. Instead, the Coulomb diamond would display as even-odd regimes (shown in Fig 4.10b)[29] [20], which has been introduced in Section 2.3.2. Sometimes the difference of addition energy between even ($E_c + \Delta E$) and odd electrons (E_c) is not really obvious (shown in Fig 4.10c) [18] [29], which means that the charging energy (E_c) is extremely bigger than the particle level spacing (ΔE) and this device works very similar with classical CBs. For ungateable devices, when the conductance is always keeping huge and unable to pinch off, the conductance versus gate voltages would display as smooth curves without any Coulomb peaks (shown in Fig 4.10d) as most channels for electron transport are unable to be closed. Conversely, some devices often stay at very low conductance, which is always pinch-off. They do not have conductance resonances as very few electrons could tunnel through the dot, but these electrons still leave several Coulomb picks when zooming in on much smaller ranges of gate voltages. Fig 4.10e and Fig 4.10f show two typical plots of very closed regimes: on Fig. 4.10e, the edges of CBs at higher V_{SD} values are much more visible, and this phenomenon often exists at low V_g. In Fig 4.10f which often exists at high V_g, the conductance around zero bias is too weak to see the edges of CBs on the first excited state, but the second or even higher resonant tunneling is still visible. This difference in CBs is mainly caused by the size of QD, which will be discussed in the following sections. Devices on nanowires from the Qdev1248 substrate do not have as huge resistances as some devices on nanowires from the QDev1197 substrate to repress the movement of electrons, and for all devices on this sample, the channels for electron transport are possible to be open. For all these listed typical electron transports, whether these devices could pinch-off and how to achieve pinch-off play very important roles in determining what CB transport regime they are, and this property is shown by the background color of the second row of each device on Table 4.1 referring to the color bar of Fig 4.9.

The last row shows the value of resistance of each device without any voltage supplements. For devices with very low resistance, their conductance would be too huge to pinch off. If one device can pinch off under a low gate voltage, it would be easier to find conductance resonances and clear CBs.

4.2.4 Conductance

Fig 4.11 gathers the plots of conductance versus one V_g under several distant values of another gate voltage for all devices of 3C, and the same comparison of

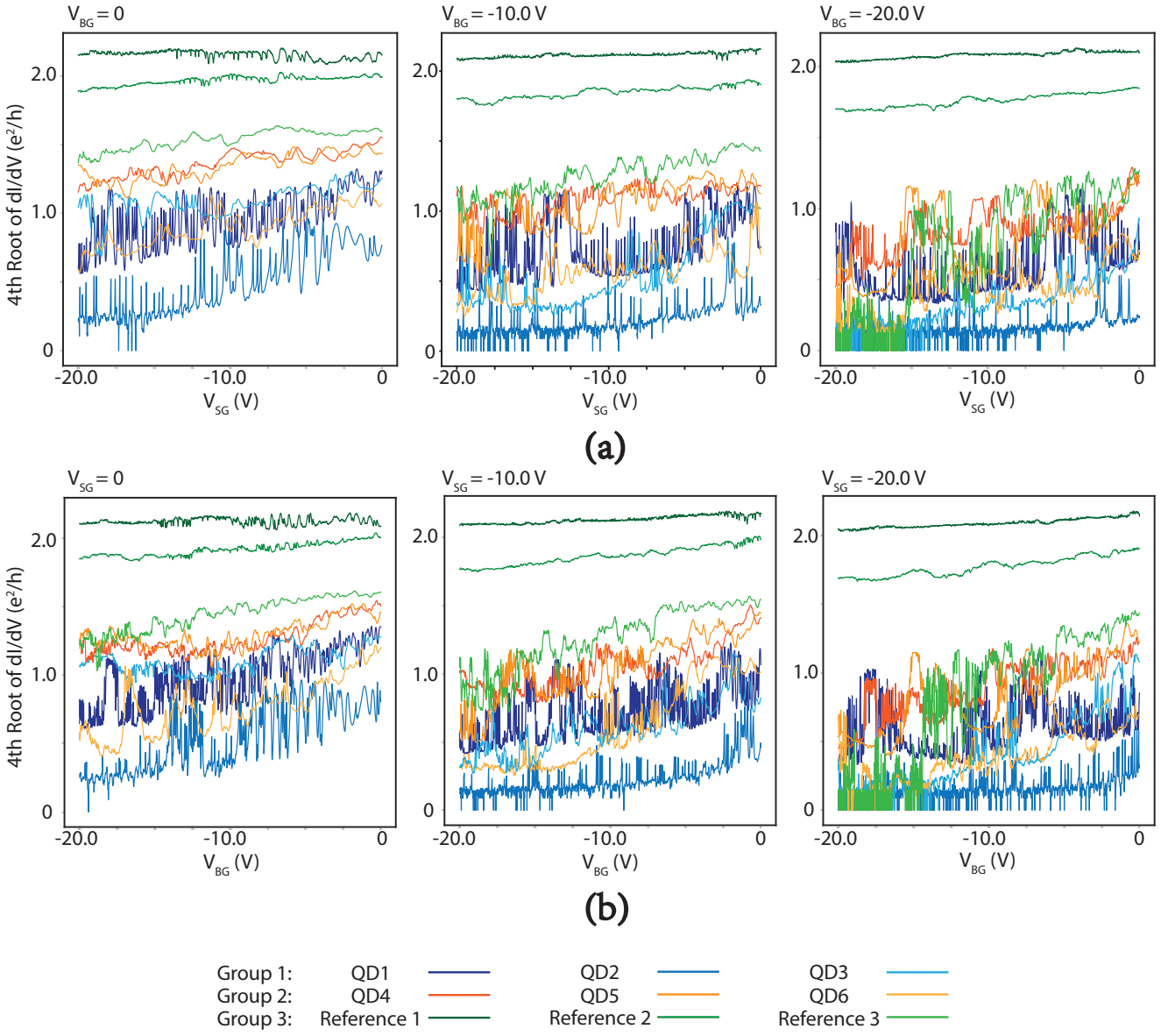


Figure 4.11: Combination of the conductance of all devices with respect to the same gate voltage under three different values of another gate voltage. Here it plots the fourth root of each conductance in order to show much clarity of their ranking in conductance. As explained in the previous section, these nine devices on the same nanowire are divided into three groups according to their growth time of barriers. (a) Conductance vs. V_{SG} with supplying V_{BG} = 0, -10 v, and -20 V. (b) Conductance vs. V_{BG} under V_{SG} = 0, -10 V, and -20 V.

the other three nanowires are listed in Appendix. As explained in the previous section, all nine devices for measurement on this nanowire shown in Fig 4.7 are divided into three groups according to the growth time of their barriers: group 1 contains QD1 to QD3, whose barriers were grown for 5 s, group 2 includes QD4 to QD6 with 2 s growth time of barriers, and groups 3 are references without barriers, which can be used for comparing with QDs on how barriers to control conductance. Then within each group, for QDs, as the sequence of ranking numbers goes higher, the growth time of the ZB segment between barriers (or represent the length of the QD) will be lower; for the three references, higher order of sequence means a lower diameter of the nanowire segment between its two contacts.

From this figure, it is clear that the conductance of devices without barriers in group 3 is extremely higher than the devices in the other two groups which have barriers, and in general, the plots of conductance of references are flatter without displaying periodic spikes.

In the previous measurement on the QDev1197 samples, it has been shown that barriers grown for 5 s are available to quantize electrons tunneling across the barriers. For this QDev1248 sample, the devices of group 1, whose barriers' growth time is also 5 s (containing all four nanowires, not only the 3C shown in Fig 4.11), even though the length of the segments between barriers are different, most of them are very easy to pinch off, which means that these devices are gateable enough to be controlled by supplying gate voltages. For devices in group 2, overall, their magnitudes of conductance are higher than QDs in group 1. These devices are also more difficult to pinch off as they require much higher gate voltages to achieve it, and some of them even unable to pinch off. It means that barriers grown for 2 s do not have enough resistance and ability to close the channels to block the transition of electrons, and then the tunneled electrons cannot be gated as quantized. Therefore, for InAs/InAsSb QDs, barriers grown for 5 s might be close to the thinnest acceptable barriers to form workable QDs.

It is clear that for devices in group 3, whose variable is only the diameter of the nanowire, as the diameter goes smaller, the conductance clearly slumps fast, and till reference 3, the conductance has been very similar to the values of devices in group 2, which is shown in Fig 4.12. It shows that the width of QDs (also the diameter of nanowires) plays the main role in determining the values of conductance. This property is also verified by comparing the conductance of devices at the same positions of nanowires with different 'shot numbers'. In previous sections of QDev1197 samples, when the 'shot number' is greater than 25, for all devices with different growth times of barriers, their conductances are all at huge magnitudes and unable to pinch off. The same condition happens on devices of the 6 shot sample of QDev1248. Besides the factor of nanowires' diameter, the ratio of the barrier's length and the length of the ZB segment between barriers also influences the formation of resonances because the periodic gate oscillation would

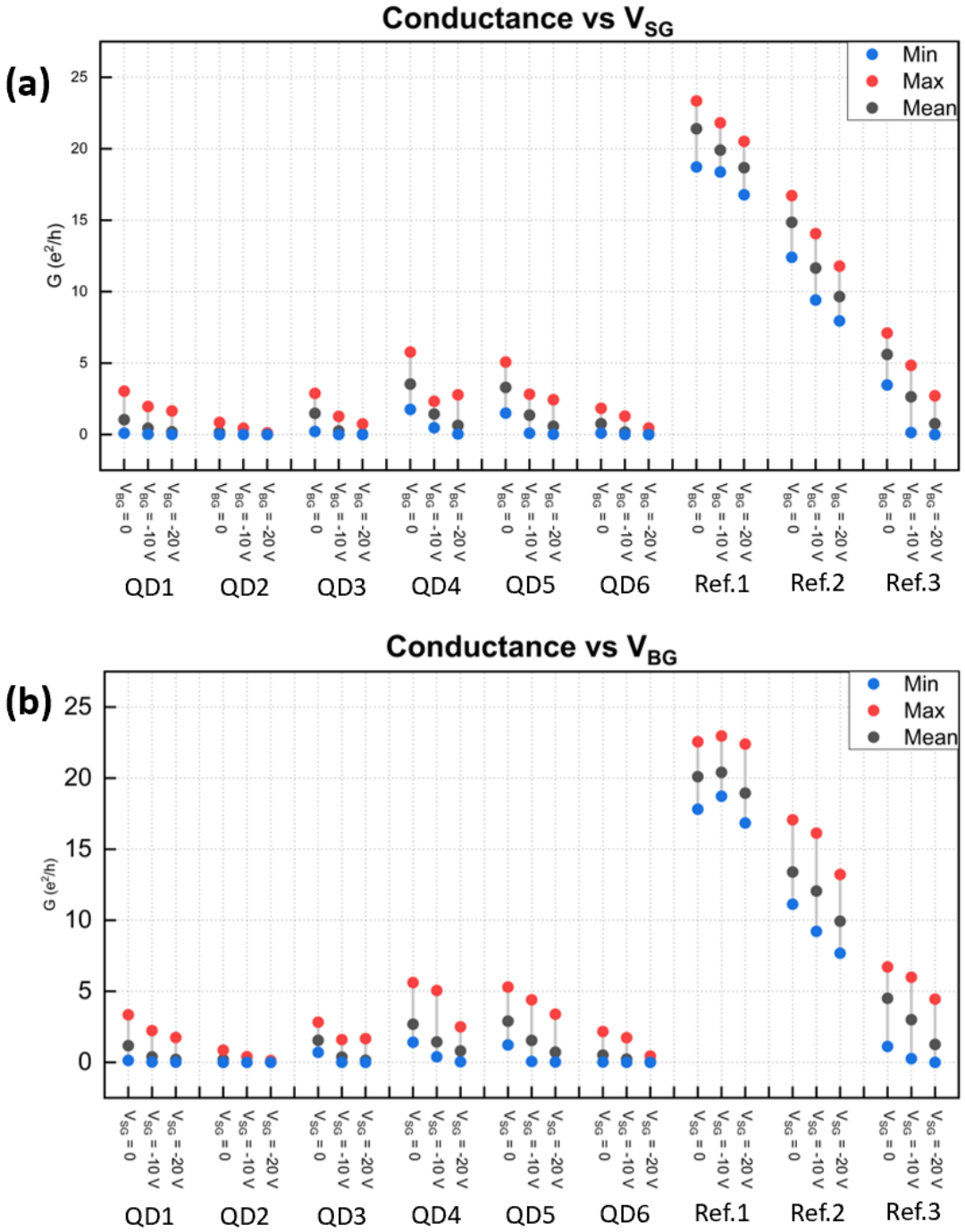


Figure 4.12: The account of average, maximum, and minimum conductance of all devices displayed in Fig 4.11, which is more clear to show the distribution of each conductance for comparing.

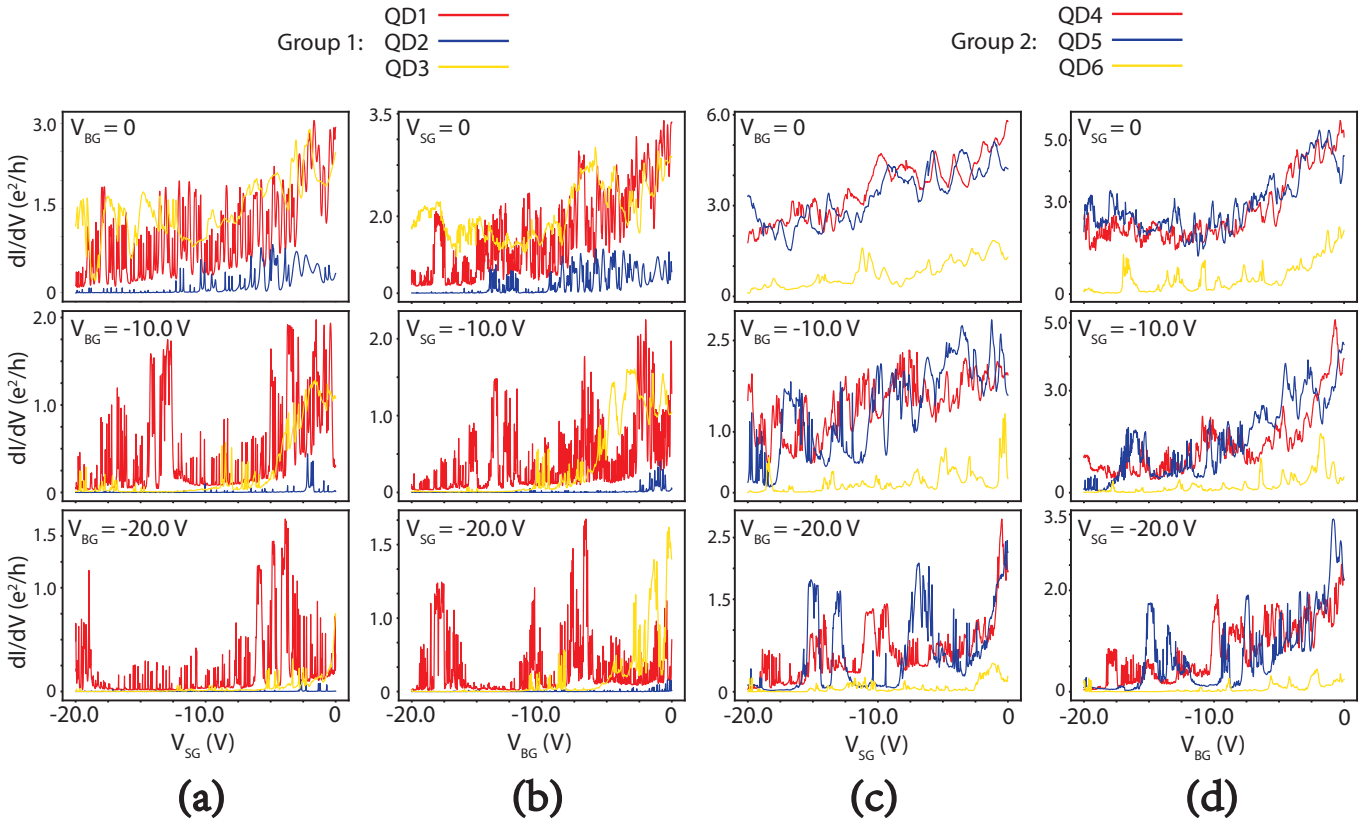


Figure 4.13: Zoom in on Fig 4.11 and focus on plots of conductance of devices in group 1 and group 2 separately. (a-b) show the rank of conductance of devices in group 1 with respect to the V_{SG} or V_{BG} under three different constant values of another V_g. (c-d) displays the same thing in group 2.

be broken when the combination of growth direction is stronger than it of lateral direction [6] [40]. This theory can be validated by comparing the measurement of both QDev1197 and QDev1248. On devices of Qdev1197 samples, whose growth time of barriers are mostly greater than devices of QDev1248 samples, the conductance resonances could be observed till the 8 shot sample, and for QDev1248, it starts to be unable to find any periodic oscillations on devices of only 6 shot samples.

When zooming in on Fig 4.11 to focus on the plots of conductance within group 1 and group 2, which has been shown in Fig 4.13, it shows that for devices in group 2, whose barriers are much thinner, the overall magnitudes of conductance are still related to the order of these devices: as the rank of the device goes higher, the conductance mostly becomes lower with inapparent differences. This trend also spreads to devices in group 1, but the conductance difference within

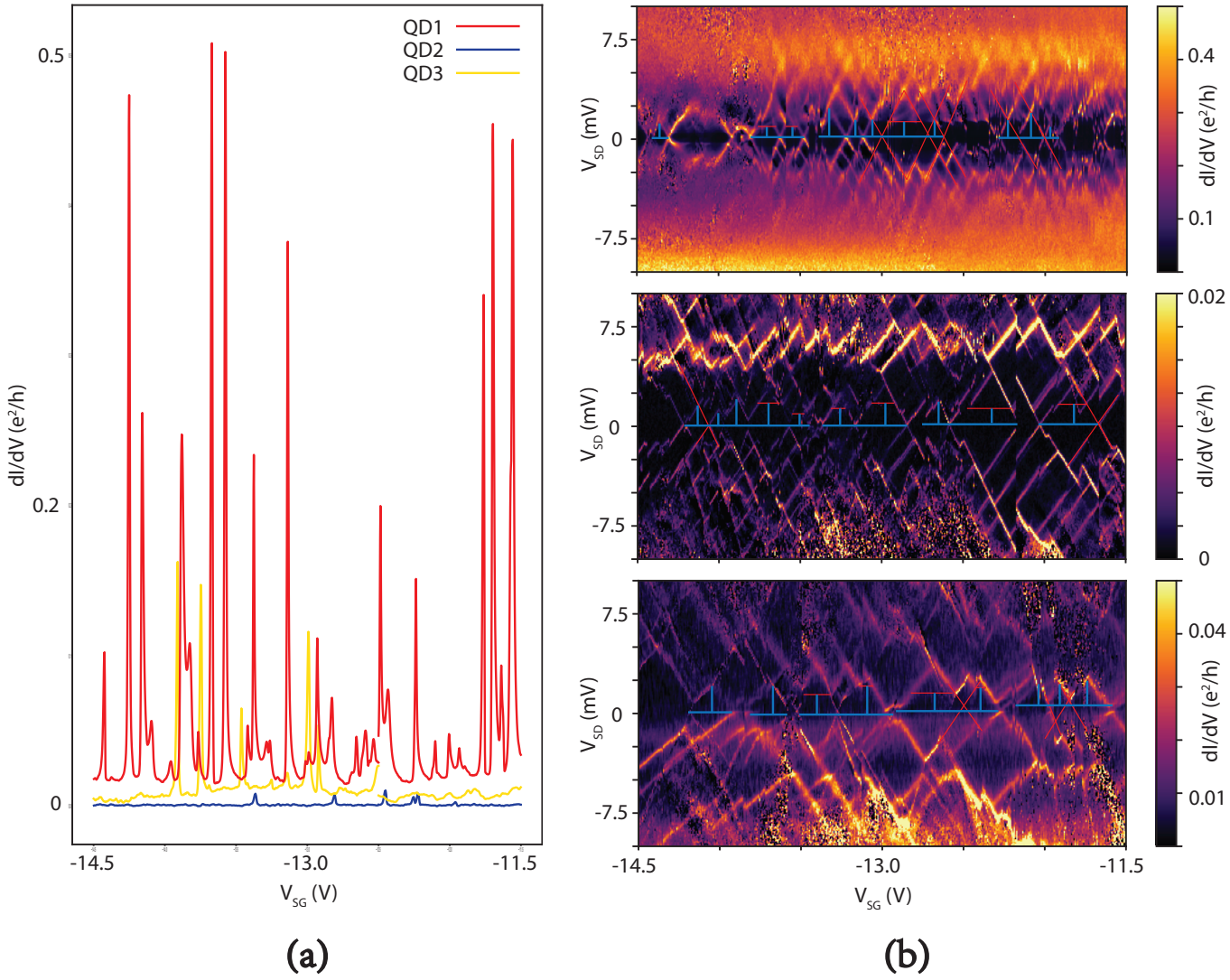


Figure 4.14: The swapping of V_{SG} of devices in group 1 form -11.5 V to -14.5 V, which is pinch-off and displaying CBs with visible E_{add} and ΔV_g under V_{BG} = -20 V. (a) Differential conductance dI/dV, with respect to V_{SG} of all these three devices with clear Coulomb peaks displaying. (b) Conductance as a function of V_{SD} and V_{SG}. These three figures (from top to bottom are QD1, QD2, and QD3) display all visible E_{add} and ΔV_g (marked by vertical and horizontal blue full lines). Some red full lines are used for complementing some unclear CBs or pointing out excited states.

devices in group 1 is not obvious (especially under supplying another gate voltage with high values). In theory, the length of the dot might only influence the oscillation of Coulomb peaks [6] or the shapes of conductance geometry [9], so this conductance difference between devices in each group might be caused by the discrepancy of the width of devices (also the diameters of the nanowire at the positions of these devices exist) which is decreasing from bottom to the top. This inference can be verified by further experiments if possible.

4.2.5 Coulomb Blockades

This section researches the CBs of each device to check how each researching factor influences their addition energies (E_{add}) and the addition of gate voltage to emit one more electron (ΔV_g). In this section, it is still possible to use devices on the nanowire at the 3C position of QDev1248 substrate because each device on this nanowire, it exits some pinch-off regions where electrons are depleted. Therefore, it is possible to capture leaked electrons when swapping gate voltages.

During the measurement of each V_g when staying another V_g at high values, the measured conductance would be lower. For these devices, when keeping one gate voltage constant at -20 V, it is possible to observe pinch-off regions for all these six QDs, which can be shown in Fig 4.13. For devices in group 1, for the range of V_{SG} from -12 V to -17 V and V_{BG} from -12.5 V to -15 V, all these three QDs are close to being depleted of electrons but still displaying some emitted electrons.

In Fig 4.14, it selects the range of V_{SG} from -11.5 V to -14.5 V, where the CB figures of all these three devices in group 1 display visible E_{add} and ΔV_g. From the plot of conductance with respect to different values of V_{SG} displayed in Fig 4.14a, it shows that from QD1 to QD3, there will be fewer Coulomb peaks with lower conductance. The difference in conductance might be caused by the difference in the width of devices, and the decrease in the number of Coulomb peaks might be caused by the shortening of the ZB segment's length, which has been discussed in the previous sections. The breaking of Coulomb oscillation from the unbalance of confinement in two directions of QDs can also be shown by comparing the CBs in Fig 4.14b. From these figures, In the figure of QD1, the conductance around zero bias is too high to make CBs at higher levels obvious. For QD2, the conductance around zero bias becomes much lower, then the CBs at higher levels become more visible, and all CBs are close to grid shaped arrangement. Till QD3, the conductance around zero bias regions becomes even lower, and CBs at higher V_{SG} regions even vanish, which has been shown in Fig 4.10f. This phenomenon might be caused by decreasing the number of electrons tunneled through the QDs at zero bias. Therefore, the contrast between the conductance at high V_{SD} and around zero bias would display as the differences of figures in Fig 4.14b

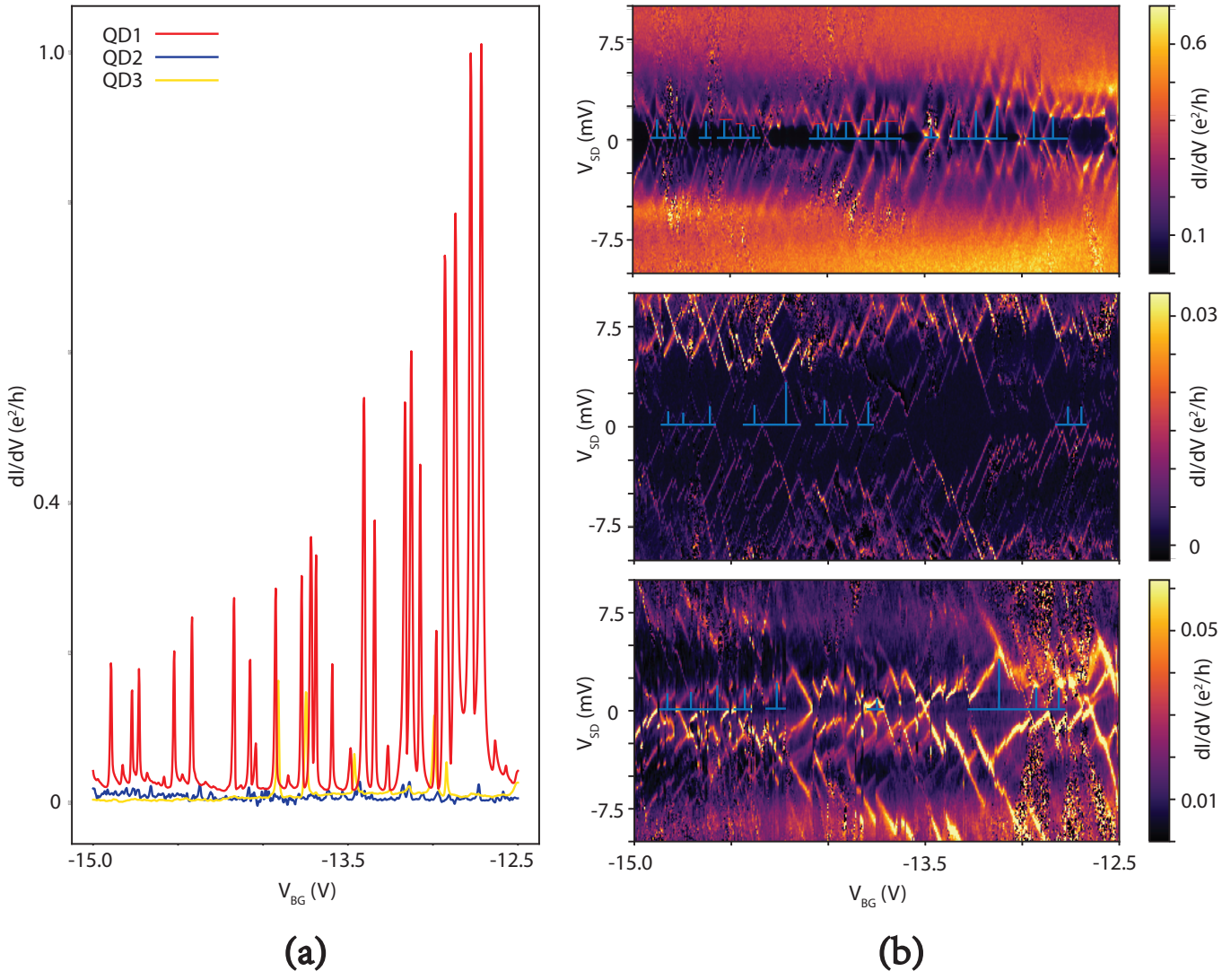


Figure 4.15: The same measurement and collection of visible E_{add} and ΔV_g by plotting V_{BG} toward the same devices as shown in Fig 4.14 under V_{SG} = -20 V.

There is the same measurement on the backgate when keeping V_{SG} = -20 V, which has been shown in Fig 4.15. The phenomenons from comparing all outputs are very similar to the measurement on the sidegate discussed above.

For devices in group 2, as the conductance of all three devices mostly stays at high magnitudes, it is hard to find out their common pinch-off ranges of gate voltages. Finally, several small regions are selected for the same measurement as the devices in group 1, which is shown in Fig 4.16.

Fig 4.16 displays the results of the same measurement on pinch-off regions of devices in group 2. Some variation trends (e.g., the decrease of the number of Coulomb peaks, the height of Coulomb peaks, and the clarity of CBs) of several properties from QD1 to QD3 also exist from QD4 to QD6s. For devices in group 2, there are even fewer Coulomb peaks and visible CBs to collect values of E_{add} and ΔV_g. For QD6, all channels seem completely closed and almost no any electrons are emitted within selected regions. Therefore, there are no CBs gotten for recording E_{add} and ΔV_g in QD6.

All visible E_{add} and ΔV_g on both sidegates and backgates within the focused regions have been displayed in Fig 4.17. From these data, it shows that both addition energy and addition gate voltages are randomly distributed in a similar range, which fits the theory that the additional energy of QD depends on the materials for production and is not really related to the size of QDs [30] [34].

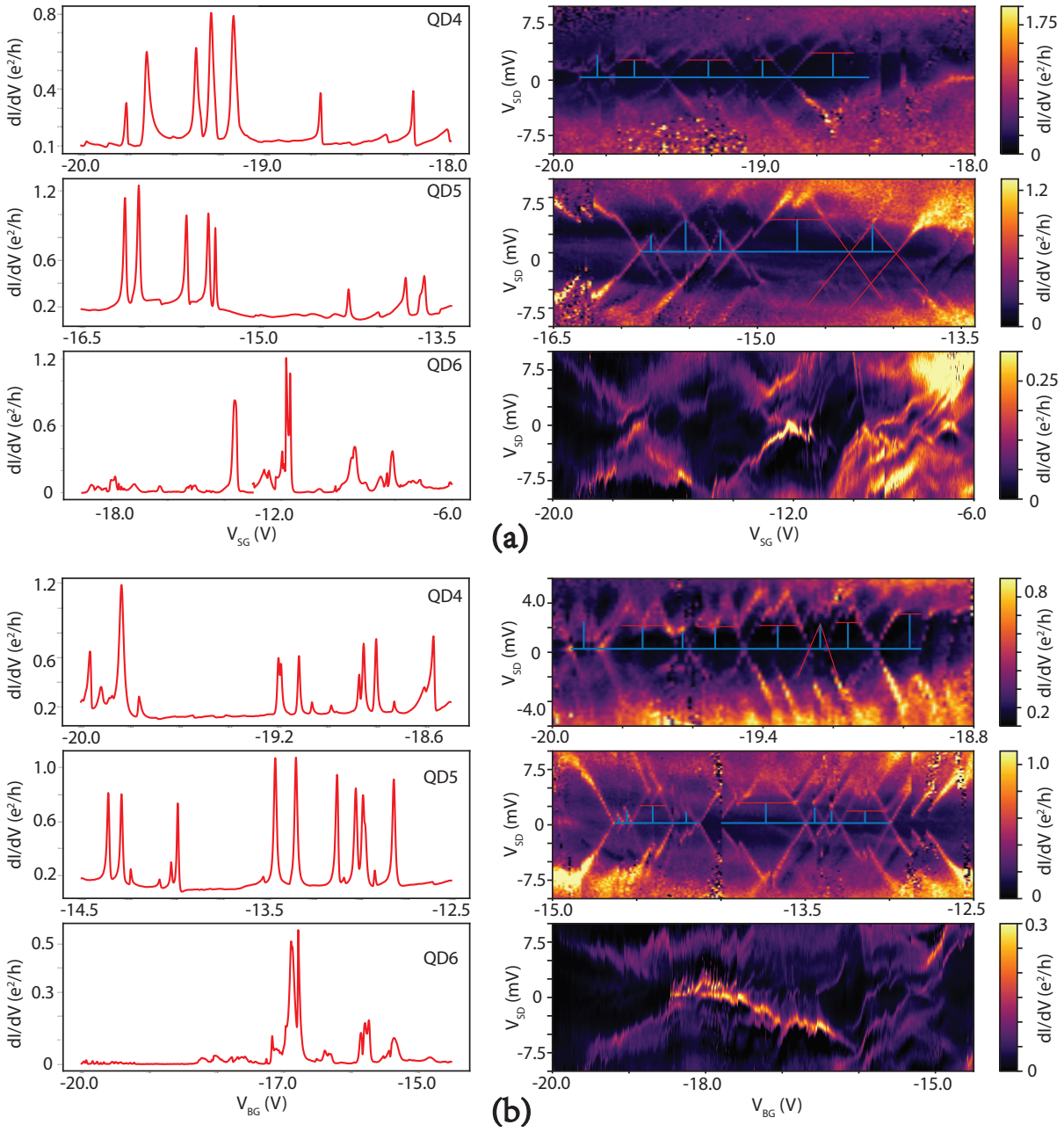


Figure 4.16: The swapping of both two V_g of devices in group 2, which is pinch-off under -20 V of another gate voltage. QD4 and QD5 are available to obtain CBs with visible E_{add} and ΔV_g, and QD6 are unable to find them. (a) The left figures show the differential conductance dI/dV with respect to V_{SG} of the pinch-off regions of all these three devices. The right figures display the conductance as a function of V_{SD} (from -10 V to 10 V) and V_{SG}. (b) The same measurement for V_{BG} of all three devices in group 2.

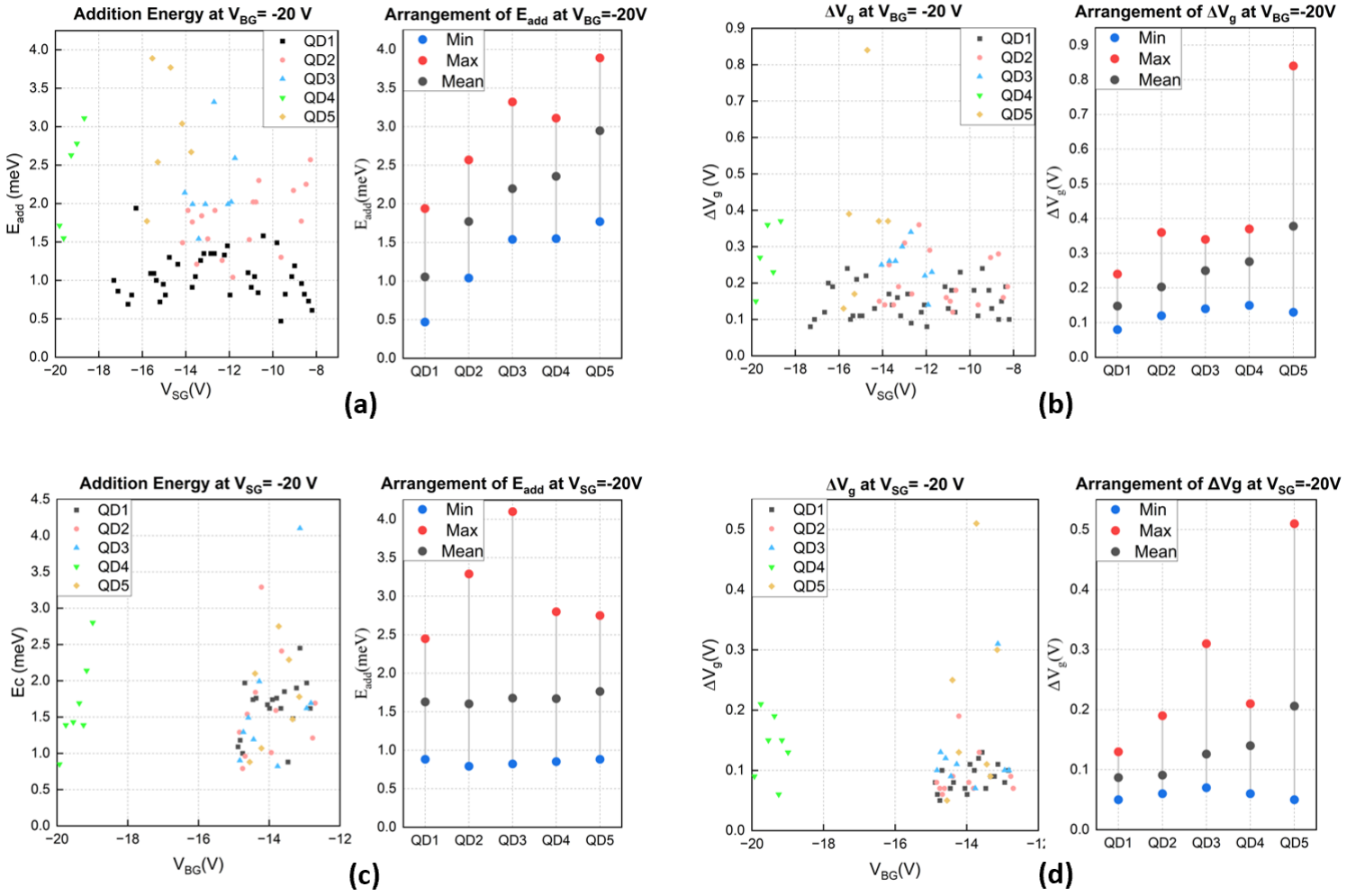


Figure 4.17: Collected E_{add} and ΔV_g of all visible CBs. The left row shows the position arrangement of E_{add} or ΔV_g. The vertical axis displays the values of each E_{add} or ΔV_g, and the horizontal axis shows the corresponding gate voltages to collect these data. The right row shows the value arrangement (shown by a high-low display with maximum, average, and minimum) of all data displayed in the corresponding position arrangement. (a-b) E_{add} and ΔV_g of V_{SG} of QD1 to QD5 under V_{BG} = -20 V. (c-d)E_{add} and ΔV_g of V_{BG} of QD1 to QD5 under V_{SG} = -20V.

Chapter 5

Conclusions and Outlook

5.1 Conclusion

In summary, the research of InAs/InAsSb QDs confirms the controllability of electron transport by supplying different gate voltages. Initially, it confirms that the combination of these two III-V materials is able to form gateable QDs. The first part of this thesis focusing on researching nanowires on the QDev1197 substrate truly realizes some objects: the appropriate range of growth temperature has been narrowed to around 433 $^{\circ}C$, and several combinations of growth time of each segment forming the QDs have been verified to be able to grow well-defined QDs with long and stable Coulomb resonances for further researches.

Zoom in to each QD formed of different III-V materials, an appropriate thickness of QDs' barriers with WZ structure is effective and necessary in controlling electron transport. However, this 'appropriate thickness' is not a constant value, the ratio between the barrier thickness and either the axial (shown in devices in each group of the QDev1248 research) or radial (shown in the QD at the same positions of nanowires with different 'shot numbers') length of the QD. The same ratio may even behave differently on QD with different sizes.

Chapter 2 raised two factors that theoretically determine the excitation spectrum of islands in the QD: a lower temperature and smaller sizes of the QD. The first one has been approved by the results measured in two different fridges. Under lower temperatures, the classical Coulomb resonances are overcome. Instead, more properties of the multi-electron system could be observed. It means that the energy level splitting is much more effective under 26 mK. However, the factor of the size of QD cannot be approved as these two growths of nanowires do not contain distinctly workable huge QDs.

5.2 Outlook

There are still a lot of QDs on both two substrates not follow the overall tendency of electron transport. On the one hand, the reason might be that traditional axial growth of group III-V semiconductor nanowires cannot exactly decide the crystal structures and the purity or specific length of each segment, so developing more techniques of nanowire growth might be more helpful. On the other hand, besides the cleaning by oxygen plasma and milling during fabrication, there may still be some oxide layers there, or the nanowires are damaged during the cleaning. Some designs for testing it could be considered in further research.

This thesis has not been able to verify the rule of the size of QD. It may also mean finding out the maximum tolerable size of QD and the width of barriers in order to find the boundary of quantum confinement. And the greatest regret is that this thesis does not consider the factor of a magnetic field. It requires a lot of further experiments on the perfection of the InAs/InAsSb QD technique.

Bibliography

[1] Nano™ pmma and copolymer. https://kayakuam.com/wp-content/uploads/2019/09/PMMA$_{D}ata_{S}heet.pdf$. *Accessed* : $2022-11-24$.

[2] Yoram Alhassid. The statistical theory of quantum dots. *Reviews of Modern Physics*, 72(4):895, 2000.

[3] Joerg Appenzeller, Joachim Knoch, Mikael T Bjork, Heike Riel, Heinz Schmid, and Walter Riess. Toward nanowire electronics. *IEEE Transactions on electron devices*, 55(11):2827–2845, 2008.

[4] Carlo WJ Beenakker. Theory of coulomb-blockade oscillations in the conductance of a quantum dot. *Physical Review B*, 44(4):1646, 1991.

[5] MJ Biercuk, S Garaj, N Mason, JM Chow, and CM Marcus. Gate-defined quantum dots on carbon nanotubes. *Nano letters*, 5(7):1267–1271, 2005.

[6] Mikael T Björk, Claes Thelander, Adam E Hansen, Linus E Jensen, Magnus W Larsson, L Reine Wallenberg, and Lars Samuelson. Few-electron quantum dots in nanowires. *Nano Letters*, 4(9):1621–1625, 2004.

[7] Jessica L Boland, Francesca Amaduzzi, Sabrina Sterzl, Heidi Potts, Laura M Herz, Anna Fontcuberta i Morral, and Michael B Johnston. High electron mobility and insights into temperature-dependent scattering mechanisms in inassb nanowires. *Nano letters*, 18(6):3703–3710, 2018.

[8] I-Ju Chen. *Thermally and Optically Excited Electron Transport in Semiconductor Nanowires*. Division of Solid State Physics, Lund University, Box 118, SE-221 00 Lund . . . , 2018.

[9] Menglu Chen, Guohua Shen, and Philippe Guyot-Sionnest. Size distribution effects on mobility and intraband gap of hgse quantum dots. *The Journal of Physical Chemistry C*, 124(29):16216–16221, 2020.

[10] Jesús A Del Alamo. Nanometre-scale electronics with iii–v compound semiconductors. *Nature*, 479(7373):317–323, 2011.

[11] Kimberly A Dick, Claes Thelander, Lars Samuelson, and Philippe Caroff. Crystal phase engineering in single inas nanowires. *Nano letters*, 10(9):3494–3499, 2010.

[12] Vladimir G Dubrovskii, Yury Berdnikov, Jan Schmidtbauer, Mattias Borg, Kristian Storm, Knut Deppert, and Jonas Johansson. Length distributions of nanowires growing by surface diffusion. *Crystal Growth & Design*, 16(4):2167–2172, 2016.

[13] Vladimir G Dubrovskii, Rodion R Reznik, Igor V Ilkiv, Konstantin P Kotlyar, Ilya P Soshnikov, Evgenii V Ubyivovk, Sergey V Mikushev, and George E Cirlin. Low-temperature growth of au-catalyzed inas nanowires: Experiment and theory. *physica status solidi (RRL)–Rapid Research Letters*, 16(1):2100401, 2022.

[14] Michael Dunlap and JE Adaskaveg. Introduction to the scanning electron microscope. *Theory, practice, & procedures. Facility for Advance Instrumentation. UC Davis*, 52, 1997.

[15] CC Escott, FA Zwanenburg, and A Morello. Resonant tunnelling features in the transport spectroscopy of quantum dots. *arXiv preprint arXiv:1002.2270*, 2010.

[16] Claus Fühner. *Magneto-transport investigations on multi-electron quantum dots: Coulomb blockade, Kondo effect, and Fano regime*. PhD thesis, Hannover: Universität, 2002.

[17] A Fuhrer, Thomas Ihn, Klaus Ensslin, Werner Wegscheider, and Max Bichler. Kondo effect in a many-electron quantum ring. *Physical review letters*, 93(17):176803, 2004.

[18] H van Houten, CWJ Beenakker, and AAM Staring. Coulomb-blockade oscillations in semiconductor nanostructures. In *Single charge tunneling*, pages 167–216. Springer, 1992.

[19] Thomas Ihn. *Semiconductor Nanostructures: Quantum states and electronic transport*. OUP Oxford, 2009.

[20] Heejun Jeong. Odd-even effects in small quantum dots. *Journal of the Korean Physical Society*, 45(6):1562, 2004.

[21] Hannah J Joyce, Qiang Gao, H Hoe Tan, Chennupati Jagadish, Yong Kim, Jin Zou, Leigh M Smith, Howard E Jackson, Jan M Yarrison-Rice, Patrick Parkinson, et al. Iii–v semiconductor nanowires for optoelectronic device applications. *Progress in Quantum Electronics*, 35(2-3):23–75, 2011.

[22] Christian Helmut Jünger. *Transport spectroscopy of semiconductor superconductor nanowire hybrid devices*. PhD thesis, University_of_Basel, 2019.

[23] Levente J Klein, Donald E Savage, and Mark A Eriksson. Coulomb blockade and kondo effect in a few-electron silicon/silicon-germanium quantum dot. *Applied Physics Letters*, 90(3):033103, 2007.

[24] Leo Kouwenhoven and Leonid Glazman. Revival of the kondo effect. *Physics world*, 14(1):33, 2001.

[25] RAA Kubiak, EHC Parker, S Newstead, and JJ Harris. The morphology and electrical properties of heteroepitaxial inas prepared by mbe. *Applied Physics A*, 35(1):61–66, 1984.

[26] Dong Liang, Juan Du, and Xuan PA Gao. Inas nanowire devices with strong gate tunability: fundamental electron transport properties and application prospects: a review. *Journal of Materials Science & Technology*, 31(6):542–555, 2015.

[27] Morten Hannibal Madsen, Peter Krogstrup, Erik Johnson, Sriram Venkatesan, Erika Mühlbauer, Christina Scheu, Claus B Sørensen, and Jesper Nygård. Experimental determination of adatom diffusion lengths for growth of inas nanowires. *Journal of crystal growth*, 364:16–22, 2013.

[28] K Miura, Y Nagai, Y Iguchi, M Tsubokura, H Okada, and Y Kawamura. Mbe growth of thick ingaasn layers lattice-matched to inp substrates. In *2007 IEEE 19th International Conference on Indium Phosphide & Related Materials*, pages 376–379. IEEE, 2007.

[29] S Moriyama, T Fuse, M Suzuki, T Yamaguchi, and K Ishibashi. Pulse-excited current measurements in carbon nanotube quantum dots. In *Journal of Physics: Conference Series*, volume 38, page 003. IOP Publishing, 2006.

[30] Joel Moser and Adrian Bachtold. Fabrication of large addition energy quantum dots in graphene. *Applied Physics Letters*, 95(17):173506, 2009.

[31] Ravindiran Munusami and Shankar Prabhakar. Group iii–v semiconductor high electron mobility transistor on si substrate. In *Different Types of Field-Effect Transistors-Theory and Applications*. IntechOpen, 2017.

[32] Malin Nilsson. *Charge and Spin Transport in Parallel-Coupled Quantum Dots in Nanowires*. Division of Solid State Physics, Department of Physics, Lund University, 2018.

[33] Malin Nilsson, Luna Namazi, Sebastian Lehmann, Martin Leijnse, Kimberly A Dick, and Claes Thelander. Single-electron transport in inas nanowire quantum dots formed by crystal phase engineering. *Physical Review B*, 93(19):195422, 2016.

[34] T Nowozin, D Bimberg, K Daqrouq, MN Ajour, and M Awedh. Materials for future quantum dot-based memories. *Journal of Nanomaterials*, 2013, 2013.

[35] Jesper Nygård, David Henry Cobden, and Poul Erik Lindelof. Kondo physics in carbon nanotubes. *Nature*, 408(6810):342–346, 2000.

[36] Stephanie M Reimann and Matti Manninen. Electronic structure of quantum dots. *Reviews of modern physics*, 74(4):1283, 2002.

[37] SL Sharp, RJ Warmack, JP Goudonnet, I Lee, and TL Ferrell. Spectroscopy and imaging using the photon scanning-tunneling microscope. *Accounts of chemical research*, 26(7):377–382, 1993.

[38] Alexander Soibel, David Z Ting, Anita M Fisher, Arezou Khoshakhlagh, Brian Pepper, and Sarath D Gunapala. Temperature dependence of diffusion length and mobility in mid-wavelength inas/inassb superlattice infrared detectors. *Applied Physics Letters*, 117(23):231103, 2020.

[39] Claes Thelander, Prabhat Agarwal, S Brongersma, Joël Eymery, Lou-Fé Feiner, Alfred Forchel, M Scheffler, W Riess, BJ Ohlsson, U Gösele, et al. Nanowire-based one-dimensional electronics. *Materials today*, 9(10):28–35, 2006.

[40] Hiroaki Ueno Hiroaki Ueno, Katsuji Moriyasu Katsuji Moriyasu, Yuuko Wada Yuuko Wada, Shin-ichi Osako Shin-ichi Osako, Hitoshi Kubo Hitoshi Kubo, Nobuya Mori Nobuya Mori, and Chihiro Hamaguchi Chihiro Hamaguchi. Conductance through laterally coupled quantum dots. *Japanese journal of applied physics*, 38(1S):332, 1999.

[41] Steven H Voldman. The state of the art of electrostatic discharge protection: Physics, technology, circuits, design, simulation, and scaling. *IEEE Journal of Solid-State Circuits*, 34(9):1272–1282, 1999.

[42] Georg W Winkler, QuanSheng Wu, Matthias Troyer, Peter Krogstrup, and Alexey A Soluyanov. Topological phases in inas 1- x sb x: from novel topological semimetal to majorana wire. *Physical Review Letters*, 117(7):076403, 2016.

Appendices

Appendix A

Conductance of 3 shot Nanowires on QDev1248

Besides the nanowire deposited at the 3C position of the 3 shot sample of QDev1248 shown in Fig. 4.8d, which is chosen to be displayed in the main text, the devices on the other three nanowires (1C, 2B, and 3D in Fig. 4.8b, c, and e) were also measured according to the same process of 3C. However, for each of these three nanowires, several devices behave differently from the same positions on other nanowires. This Appendix shows the combination of conductance of all devices under different gate voltages (similar to Fig 4.11), lists the distribution of conductance (similar to Fig 4.12), and zooms in on each group of devices (similar with Fig 4.13) to check whether the conductance varying according to the change of each researching variables is similar to the same devices on other nanowires. If not, then analyze some possible reasons that caused these differences.

A.1 1C

Figure A.1 to A.3 show the plots of conductance of devices of nanowire on 1C position of the sample shown in Fig 4.8b.

Fig A.1 and Fig A.2 shows that the conductance of QD4 is always higher than reference 3, which is opposite to the 3C and expected as samples with barriers often have higher resistance. One possible reason is that when growing this QD, as its position is very far from the substrate, the diffused adatoms scattered from the substrate were hard to reach the Au droplet to join the nucleation. Therefore, the thickness of the barrier might be much thinner than expected, whose contribution of resistance is smaller than the decrease in diameter compared with reference 3.

When zooming in on the conductance of devices in group 1 shown in Fig A.2 and A.3, the QD2 has unusual high conductance all the time. Compared

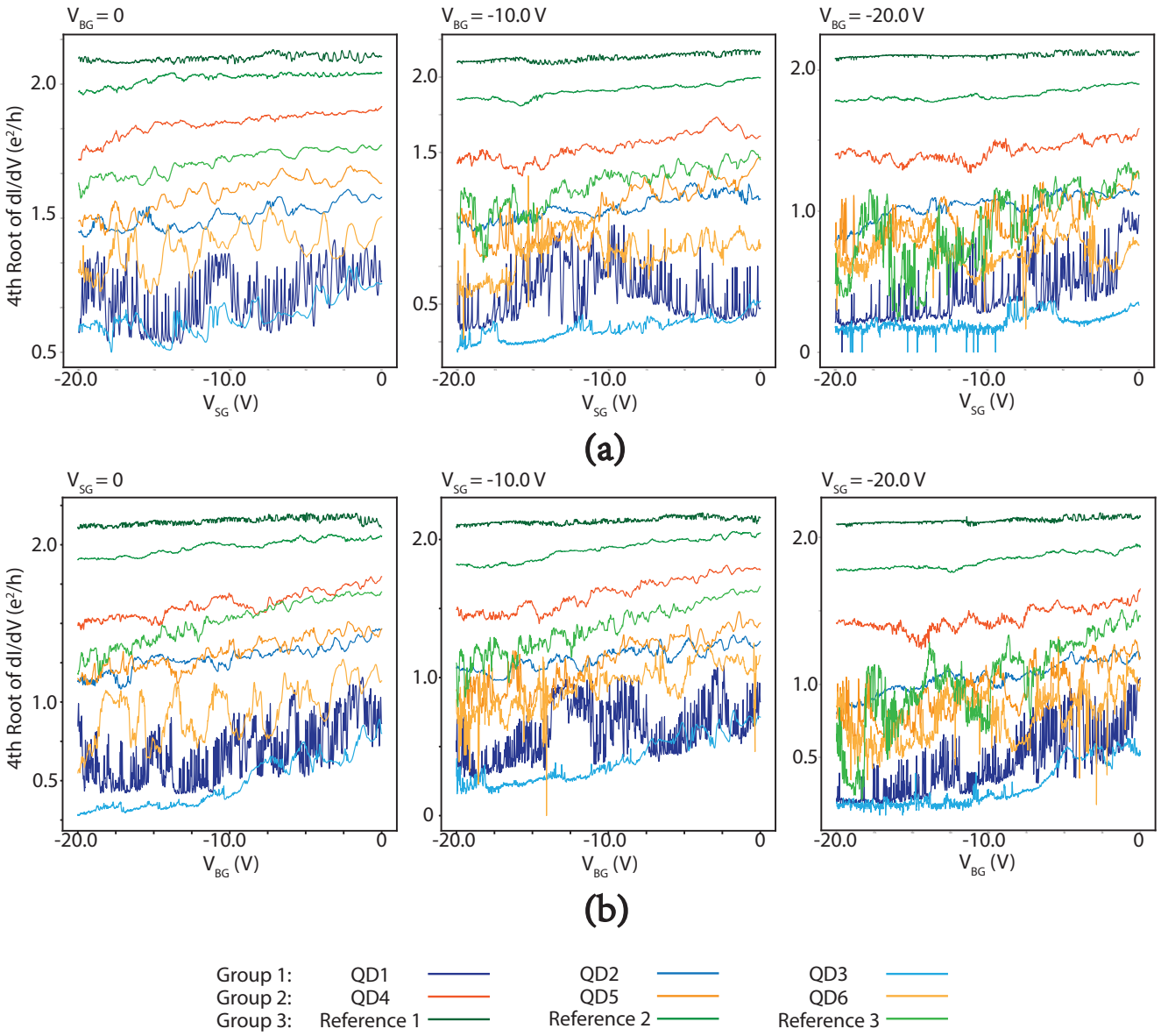


Figure A.1: Combination of the fourth root of conductance vs one V_g of all devices on the 1C nanowire under three different values of another V_g.

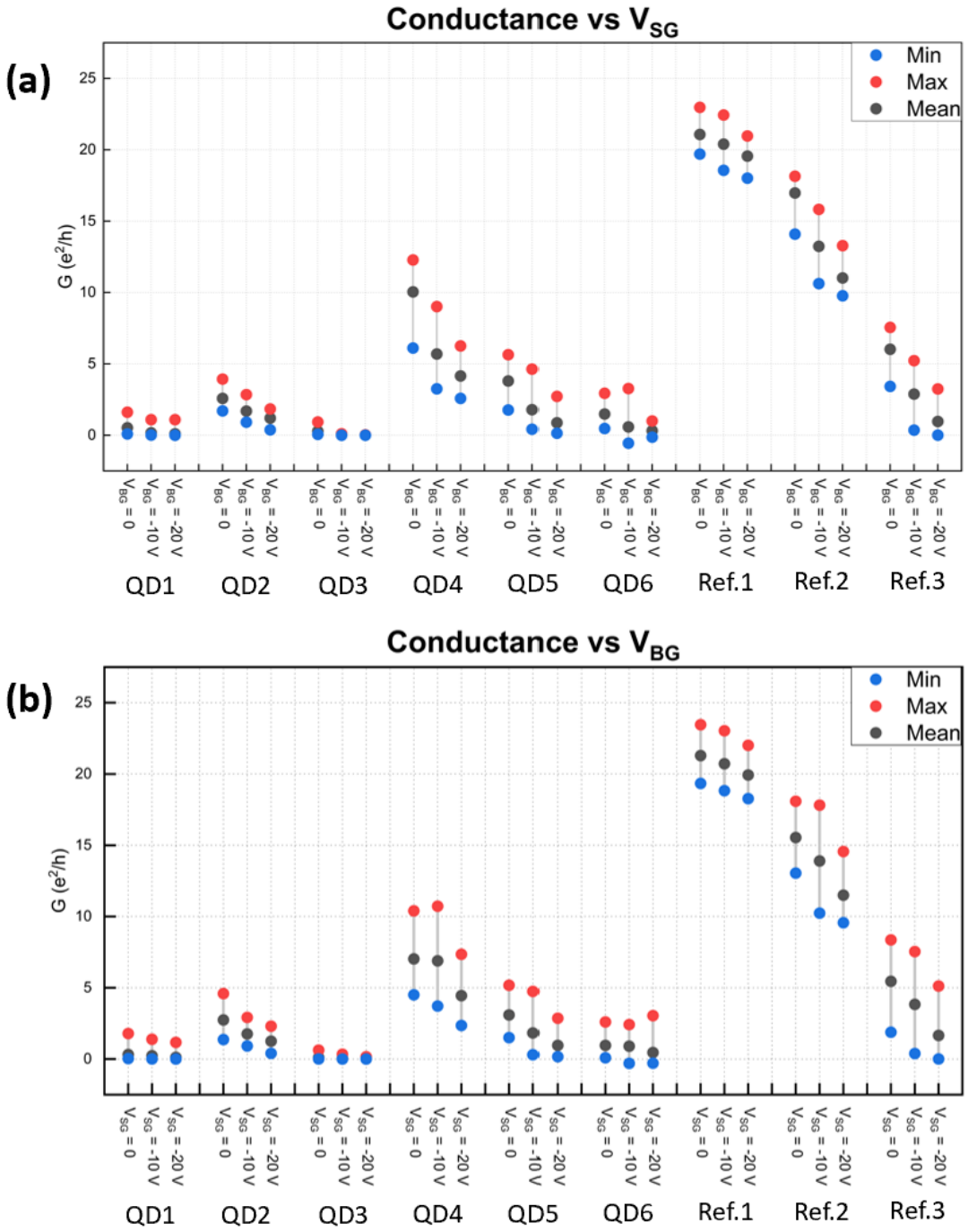


Figure A.2: The high-low charts explain the maximum, minimum, and mean values of conductance of each device in Fig A.1 to show the distribution of their conductance.

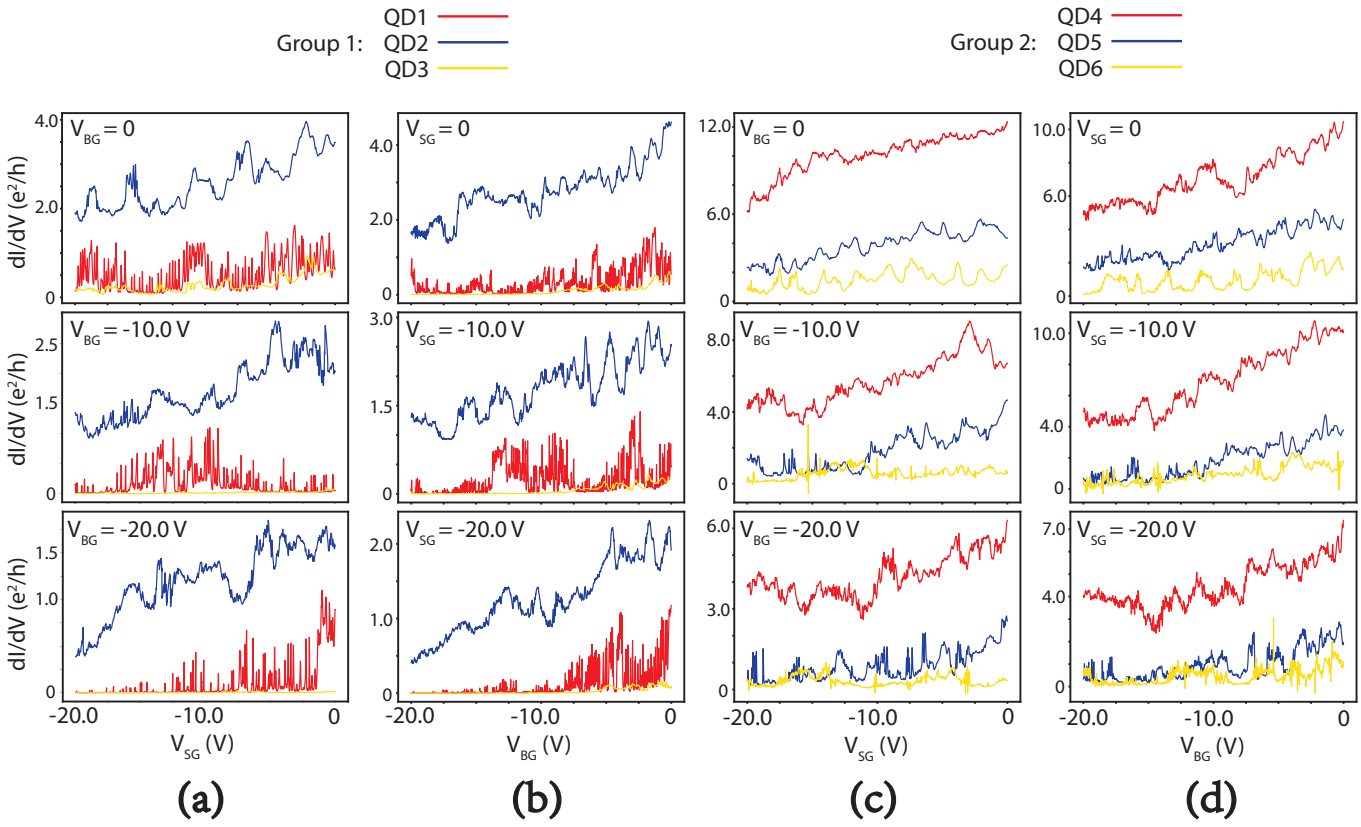


Figure A.3: Zoom into the conductance of devices within group 1 and 2, which is not obvious enough in Figure A.1.

with other devices which are hard to pinch off, the plots of this QD are not really smooth, which might be caused by some impurities within this QD, for example, when growing the barriers of this QD, some undepleted Sb particles joined the formation of the barriers. Therefore, there are some islands within the barriers to make electrons transport through the QD much easier. However, the impurity is not too much and even distributed, so it displays as unstable conductance instead of a smooth curve with high values.

A.2 2B

The same measured data from devices on the nanowire at 2B as displayed in the previous section are shown in Figure A.5 to A.7.

The most unique result is that for reference 3 on this nanowire, its conductance is more affected by higher gate voltages than other devices even including QDs, and the conductance is even easy to pinch-off, which is completely different from other references. One possible reason is that after fabrication, the practical distance between sidegates and devices on this nanowire is the shortest within all these four nanowires (the distance of other three nanowires from their sidegates is at least 100 nm, and for this one, the distance is only around 40 nm). Therefore, all devices on this nanowire would be affected much more than the same devices on other nanowires, and as the diameter of reference 3, whose position is the farthest from the root of the nanowire, is the smallest, the diameter of reference 3 might be so small that its sidegate is able to force all charges of the pointed segment.

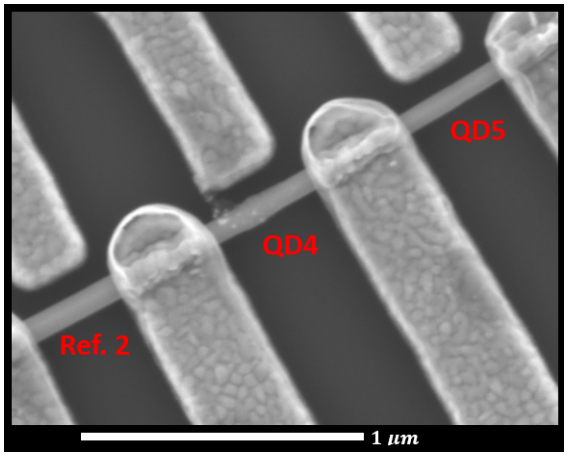


Figure A.4: Zoom into Ref.2 to QD5 of nanowire at 2B after liftoff and before measurement.

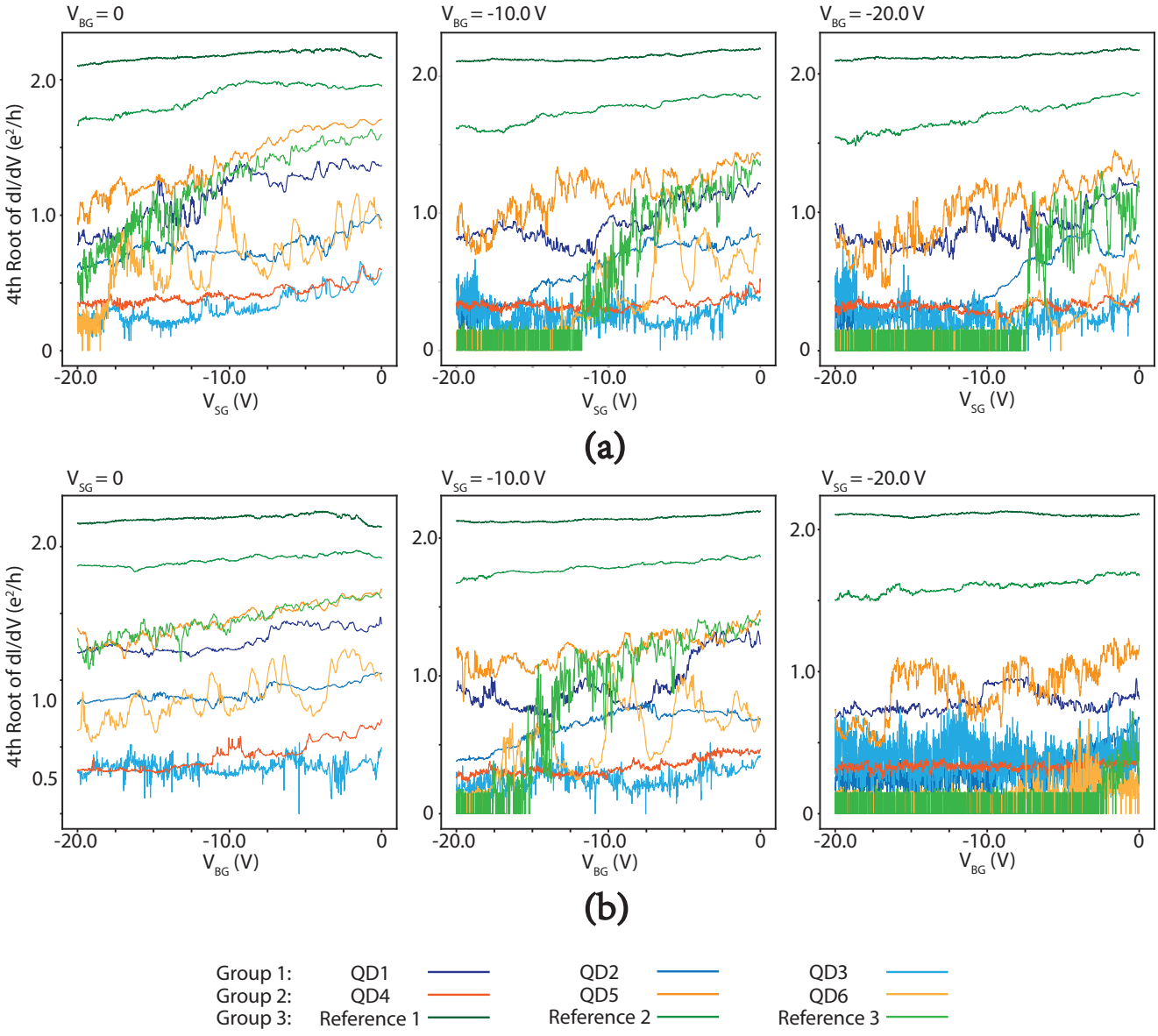


Figure A.5: Combination of the fourth root of conductance vs one V_g of all devices at 1C nanowire under three different values of another V_g.

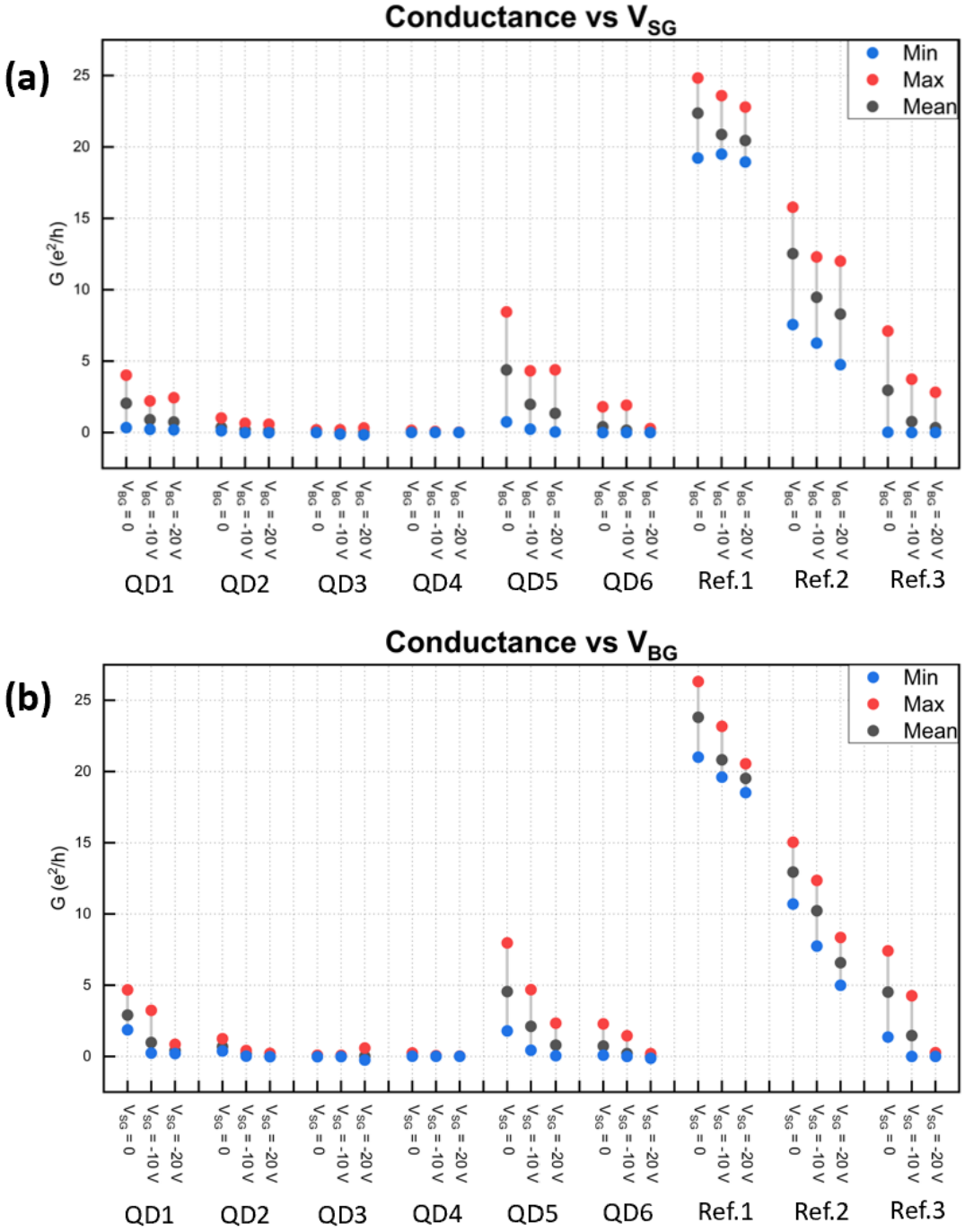


Figure A.6: The high-low charts explain the maximum, minimum, and mean values of conductance of each device in Fig A.5 to show their conductance distribution.

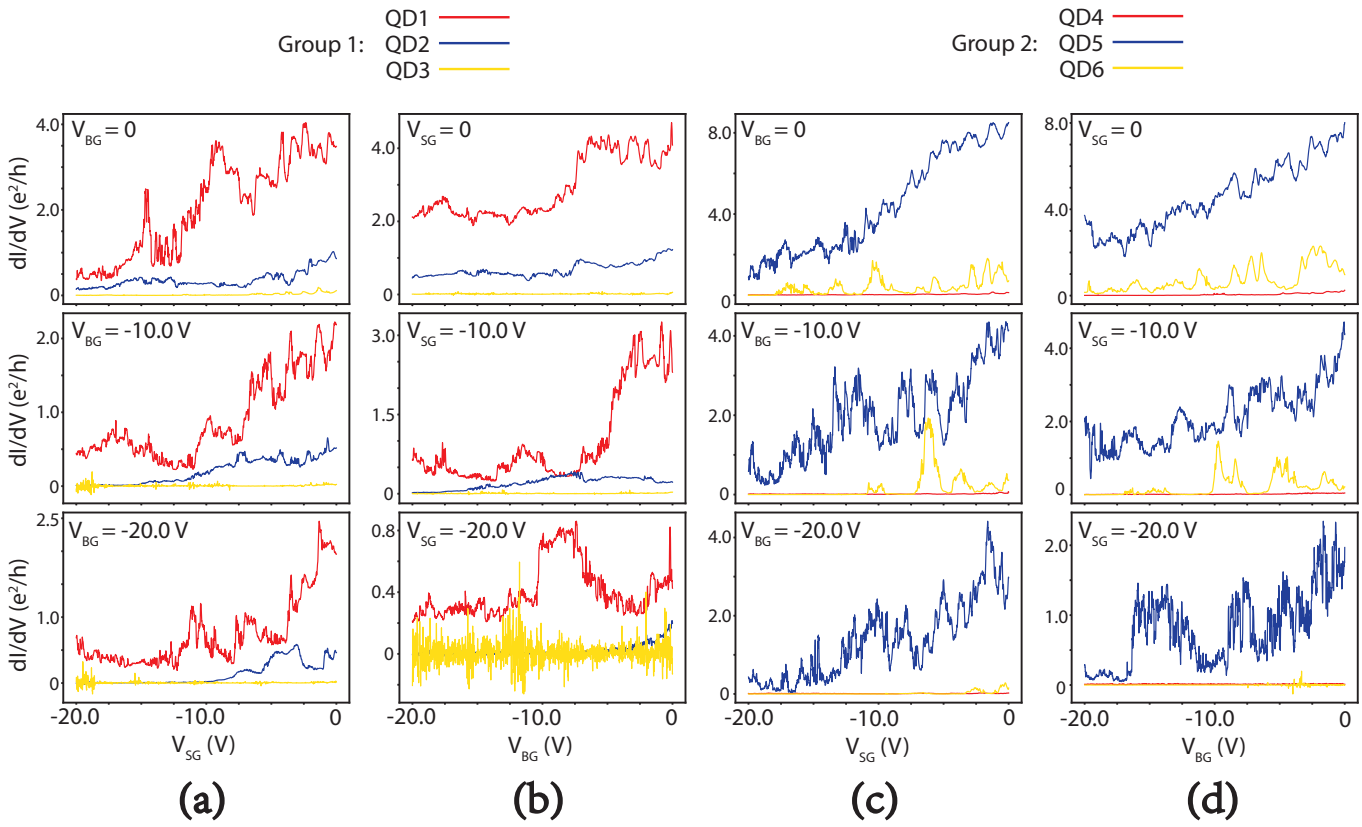


Figure A.7: Zoom into the conductance of devices within group 1 and 2, which is not obvious enough in Figure A.5.

Another special thing is that most electron channels of QD3 and QD4 on this nanowire are easy to be closed under negative V_g, and when moving to positive gate voltages, the channels are easy to be opened soon. For QD3, it may also be caused by the greater effect of the sidegate because the distance between the sidegates and devices is much higher than others, and for other nanowires, QD3s mostly have the lowest conductance, the improved sidegate voltages toward devices on this nanowires make it easier to pinch-off. For QD4, when zooming in to the SEM image of QD4, compare with two nearby devices, this QD is stained with some unknown things and its shape seems a little bit different from either bare segments of InAsSb (compared with Ref. 2) or QDs (compared with QD5). Therefore, this device might be damaged or doped by some impurity to make its resistance much higher.

A.3 3D

Figure A.8 to A.10 show the plots of conductance of devices on nanowire at the 3D position of the sample shown in Fig 4.8e.

The main problem of this device is that QD4 and QD5 cannot be separately plugged in V_{SD}. Instead, when skipping their shared plug-in contact and hooking the other two contacts to connect these two devices in series, it is electric. Therefore, there might be a break of the segment between these two devices or the circuit from the metal contact to the motherboard (and even the breakout box of the Triton fridge).

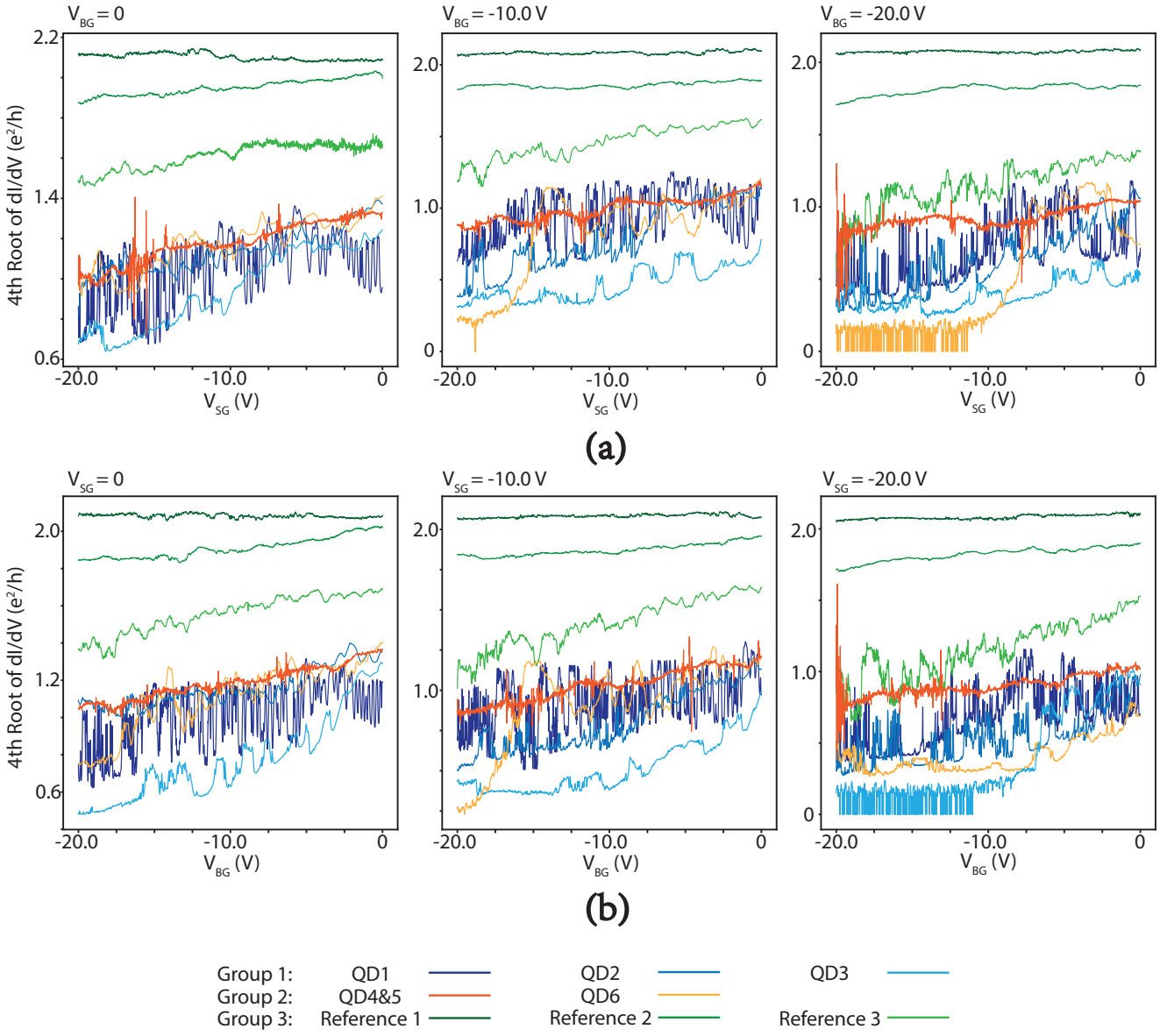


Figure A.8: Combination of the fourth root of conductance vs one V_g of all devices on the 1C nanowire under three different values of another V_g.

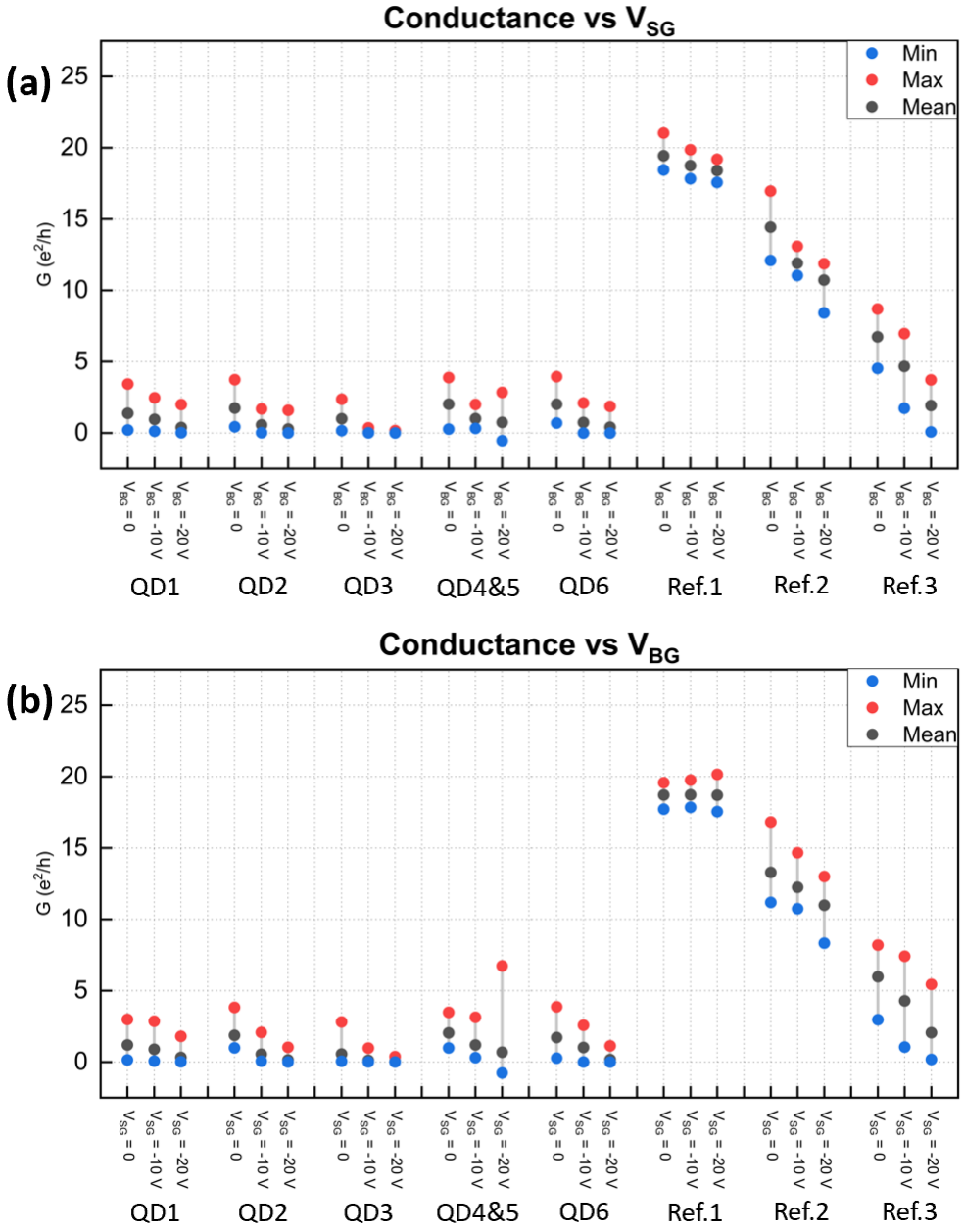


Figure A.9: The high-low charts explain the maximum, minimum, and mean values of conductance of each device in Fig A.8 to show their conductance distribution.

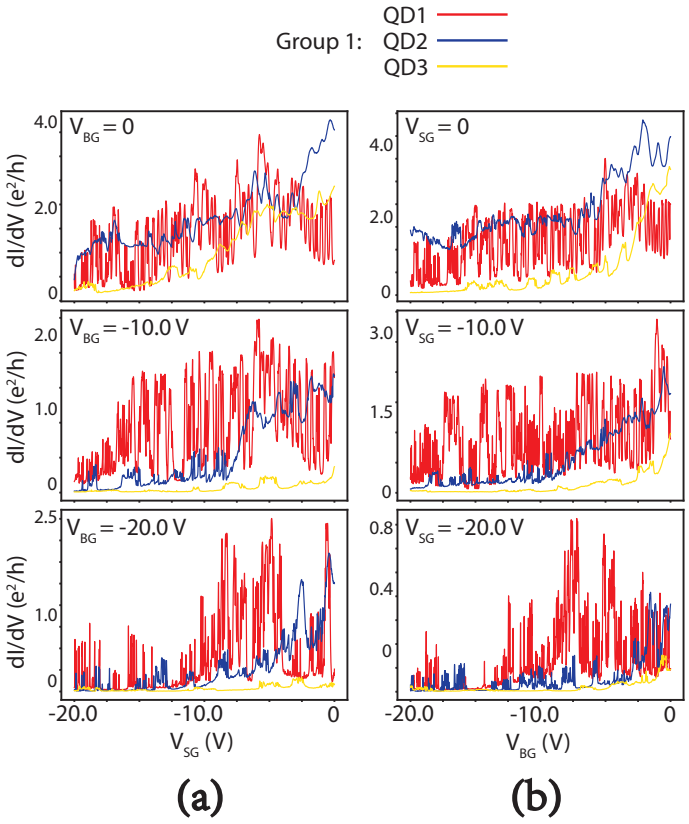


Figure A.10: Zoom into the conductance of QDs within group 1, which is not obvious enough in Figure A.8.