QUANTUM DEVICES WITH GROUP IV ELEMENTS

GROWTH, FABRICATION AND MEASUREMENTS

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Now you can rest.

ABSTRACT

Silicon and germanium are promising material platforms for hosting quantum processors based on spin qubits. In material synthesis, chemical vapour deposition methods have since dominated the field, producing state-of-the-art heterostructures. This work aims to explore the capabilities of molecular beam epitaxy. The study narrates the entire process, from receiving a Si(001) wafer to performing electrical measurements in quantum devices used for spin qubits.

First, the crystal growth and characterization of germanium quantum wells on virtual substrates using solid-source molecular beam epitaxy are presented. The focus then shifts to wafer preparation, employing an in-situ atomic hydrogen irradiation surface treatment technique to remove the native wafer oxide at significantly reduced temperatures. The heterostructures of this study are free from crosshatch dislocations and have the lowest root-mean-square surface roughness at approximately 500 pm. Comprehensive structural characterization by high-resolution transmission electron microscopy, X-ray diffraction reciprocal space mapping, atomic force microscopy, and Nomarski optical microscopy, along with the evaluation of threading dislocation density explore figures of merit of the heterostructures. Novel approaches with ex-situ deposition of superconducting films on the heterostructures aim to address hybrid experiments. The analysis closes with perspectives on future advancements and potential applications of the studied heterostructures.

The high-quality morphological features of the heterostructures motivate the investigation of their electrical properties. The second part of this thesis presents the fabrication methodologies of quantum devices on planar group IV substrates. In addition to the Ge/SiGe heterostructures, the Si/SiGe and SiMOS platforms, both in-house and foundry-fabricated devices, are also reviewed. In contrast to the conventional presentation of the tools and methods, this thesis addresses the troubleshooting of the failure modes that occurred in the fabrication of quantum devices.

Last, the devices were initially screened in a continuous adiabatic demagnetisation refrigerator, followed by more comprehensive characterisation in a dilution refrigerator. Hall measurements in Ge heterostructures explore the charge carrier properties in terms of mobility, indicating low percolation density. Quantum dot devices in the presented material platforms reach the few-carriers occupancy in both holes and electrons opening the path for spin-qubit experiments.

RESUMÉ

Silicium og germanium er lovende materialeplatforme til spin-qubit-baserede kvanteprocessorer. Inden for materialesyntese har metoder for kemisk dampudfældning domineret feltet og produceret state-of-the-art heterostrukturer. Dette studie har til formål at udforske mulighederne ved molekylærstråleepitaksi. Afhandlingen beskriver hele processen, fra modtagelse af en Si(001)-wafer til udførelse af elektriske målinger i kvanteenheder, der bruges til spin-qubits.

Først præsenteres brugen af solid-source molekylærstråleepitaksi til krystalvækst og karakterisering af germanium-kvantebrønde på virtuelle substrater. Derefter fokuseres der på forberedelse af wafers, gennem en in-situ teknik til overfladebehandling med atomisk hydrogenbestråling for at fjerne det oprindelige waferoxid ved betydeligt lavere temperaturer. Heterostrukturerne i denne undersøgelse er fri for krydsskraveringsforskydninger og overfladeruheden har den laveste effektivværdi på cirka 500 pm. Heterostrukturernes kvalitet analyseres gennem omfattende strukturel karakterisering i form af højtopløsnings-transmissionselektronmikroskopi, røntgendiffraktion reciprocal space mapping, atomisk kraft mikroskopi og optisk Nomarski-mikroskopi, samt evaluering af trådnings-forskydningsdensitet. Nye methoder der bruger ex-situ aflejring af superledende film på heterostrukturerne arbejder frem mod at understøtte hybride eksperimenter. Analysen afsluttes med perspektiver på fremtidig udvikling og potentielle anvendelser af de undersøgte heterostrukturer.

Den høje kvalitet af heterostrukturernes morfologiske træk igangsatte undersøgelsen af deres elektriske egenskaber. Den anden del af denne afhandling præsenterer fabrikationsmetoderne for kvanteenheder på plane gruppe-IV-subtrater. Ud over Ge/SiGe heterostrukturerne bedømmes også Si/SiGe og SiMOS platformene, og enheder fremstillet in-house og på støberi. I modsætning til den konventionelle præsentation af værktøjer og metoder, adresserer denne afhandling fejlfinding af tilstande, der opstod under fremstillingen af kvanteenheder.

Til sidst blev enhederne screenet i et kontinuerligt adiabatisk demagnetiseringskøleskab, efterfulgt af en mere omfattende karakterisering i et fortyndingskøleskab. Hall-målinger i Ge-heterostrukturer udforsker ladningsbærer-egenskaberne med hensyn til mobilitet, hvilket indikerer lav perkolationstæthed. Kvantepunktsenheder i de præsenterede materialeplatforme opnår lav bærer-tæthed i både huller og elektroner, hvilket baner vejen for spin-qubit-eksperimenter.

PUBLICATIONS

This thesis incorporates the findings of manuscript [1]. The candidate contributed to publications [2-4] while enrolled in the PhD programme, but no experimental data are included in this thesis.

[1] **Charalampos Lampadaris**, William Iain Leonard Lawrie, Jesús Herranz Zamorano, Sabbir A Khan, Oliver Liebe, Johanna Malina Zeis, Sara Martí-Sánchez, Marc Bodifoll, Jordi Arbiol, Peter Krogstrup, and Ferdinand Kuemmeth. "Flat and Shallow: A crosshatch-free germanium spin qubit platform." In: *Manuscript under preparation* (2024).

[2] Yan Chen, David van Driel, **Charalampos Lampadaris**, Sabbir A Khan, Khalifah Alattallah, Lunjie Zeng, Eva Olsson, Tom Dvir, Peter Krogstrup, and Yu Liu. "Gate-tunable superconductivity in hybrid InSb–Pb nanowires." In: *Applied Physics Letters* 123.8 (2023).

[3] Sabbir A Khan, Sara Martí-Sánchez, Dags Olsteins, **Charalampos Lampadaris**, Damon James Carrad, Yu Liu, Judith Quiñones, Maria Chiara Spadaro, Thomas Sand Jespersen, Peter Krogstrup, et al. "Epitaxially driven phase selectivity of Sn in hybrid quantum nanowires." In: *ACS nano* 17.12 (2023), pp. 11794–11804.

[4] Sabbir A Khan, **Charalampos Lampadaris**, Ajuan Cui, Lukas Stampfer, Yu Liu, Sebastian J Pauka, Martin E Cachaza, Elisabetta M Fiordaliso, Jung-Hyun Kang, Svetlana Korneychuk, et al. "Highly transparent gatable superconducting shadow junctions." In: *ACS nano* 14.11 (2020), pp. 14605–14615.

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Of course, before defining ourselves with any occupation or title, we are all humans with physical limitations. I would like to thank the university for offering support via Prescriba and **Lejla** for all her help dealing with stress and abnormal working hours during these years.

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Nina I'm deeply thankful that you dealt with me all these years. Thank you for your patience in all the times that *I would come back home early*. The best is coming now. Thank you for **Finny**. Thank you for being the best partner I could ever imagine. I love you deeply. Thank you for being always there for me.

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1 INTRODUCTION

Quantum information theory describes how information can be stored and operated in the form of quantum states. In contrast to the classical information theory where the bits are expressed as 0 or 1, **qubits** are expressed as a quantum state $|\Psi\rangle$ that is the superposition of the quantum states $|0\rangle$ and $|1\rangle$ as $|\Psi\rangle = a|0\rangle + b|1\rangle$, with $a^2 + b^2 = 1$. The criteria for the physical implementation of quantum computation have been laid down since 2000 [1].

A plethora of quantum systems have been suggested for the realisation of qubits, but the community has not settled on one candidate. Overall, quantum computers are still in a very premature state. As a plethora of different platforms is continuously being developed, this thesis focuses on the qubits that encode the quantum information on the spin degree of freedom in a charge carrier [2]. Currently, the most advanced spin qubit system comprises a dozen qubits [3]. Towards the scalability, many suggestions have been made, including large arrays and intermediate couplers [4–7]. Machine learning algorithms simplify complex multi-qubit systems with automated tuning protocols [8, 9].

Advancements in the miniaturisation and scalability of transistors and integrated circuits were highly influenced by material development. Similar to classical computers, quantum processors require high-quality components. This thesis addresses perspectives in **materials science** with the motivation to enhance qubit quality. The research focuses on the material properties and lays the foundation for the next stage of investigation, which is qubit characterisation. Once the second stage is understood, one can turn their interest to quantum information.

In the *Roadmap on quantum nanotechnologies* published in 2021 by Laucht et al. [10], the authors state that "it is still under consideration whether Si is preferable to GaAs when considering all factors as an ideal candidate for realising quantum computing based on spin-qubits". However, notable advancements in the field over the subsequent years have significantly influenced this statement, elevating **Group IV** materials, such as Si and Ge, as the most promising candidates for the practical implementation of spin qubits.

Figure 1.1 illustrates the evolving landscape in the spin qubit research. Based on the review of performance metrics [11], the trend in material platform choice is shifting towards group IV materials. The presented dataset comprises 319 publications, where 92 refer to III/V platforms and 227 to IV group elements. Each datapoint in the bins is a reported coherence time. It is noteworthy that although

the publication volume concerning III-V-based qubits spans over two decades, the amount of data in the later-developed platform is more than double. This high engagement clashes with the earlier quoted statement indicating a rapidly developing field. It is only reasonable to anticipate major advancements in the next decade.

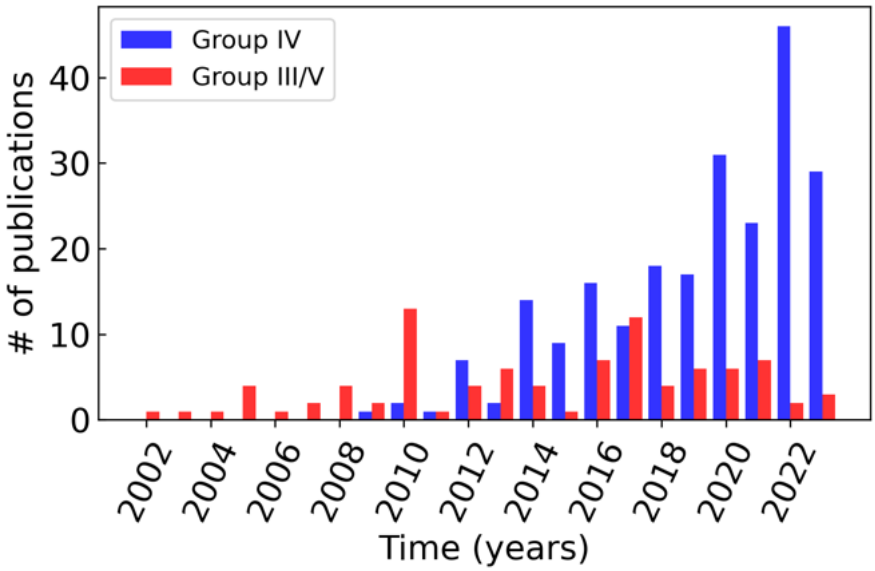


Figure 1.1: Performance metrics of spin qubits devices: trend on reported coherence times in spin qubits. Through the last years, the interest has shifted towards group IV spin qubits.

From an academic point of view, the isotopic purification of Si has made group IV platforms very appealing. In contrast to the GaAs–based spin qubits where magnetic noise is the main source of decoherence [12] Si and Ge sources can be processed to minimise the non-zero nuclear spins. The process is succeeded via cascading centrifugation in specialised facilities [13]. Moreover, the implementation of CMOS technologies for on-chip architectures makes Si a very promising candidate for the industry.

Even though this thesis focuses on group IV heterostructures, the attended PhD programme involved multiple side-projects that are not discussed. For the first year, the publication from the master's was completed [14], and the primary research focus of the three-year program was determined to be on the exploration of novel superconductors in hybrid III/V nanowires. Then, a year later, this project was completed, and the author moved to the growth of high mobility Ge heterostructures. This project was in collaboration with industry but was discontinued due to executive decisions. Following the termination of the project, the author participated in a joint project on selective area grown III/V nanowires. The work of this project was presented at the Nanowire week of 2022, and the results are included in the Appendix E. Moving on, the author shifted gears and supervisors and

began a new journey in the fabrication and measurements of group IV heterostructures. There the main focus was electrons on isotopically purified Si heterostructures. In parallel, the grown germanium heterostructures were investigated.

This thesis presents the entire procedure to create a spin qubit: from the moment that a packed Si substrate is received from the manufacturer up to the point of the double quantum dot formation at the few-carrier regime to demonstrate spin qubit experiments. The thesis is divided into three parts: **Growth**, **Fabrication** and **Measurements**. Each part provides a theoretical background or experimental introduction to the equipment as an introduction chapter, followed by a second one presenting the experimental findings. After the introduction **Chapter 1**, crystal growth theory, together with the technological implementations of crystal synthesis in the laboratory, are presented in **Chatper 2**. **Chapter 3** introduces the surface treatment techniques and the grown epitaxial films. The structural characterisation of this chapter provides insight into the properties of the samples highlighting the remarkable flat surfaces that were achieved in this study. Proceeding to **Part II** and **Chapter 4** the device fabrication techniques are presented followed the device implementations of the study in **Chapter 5**. In **Part III Chapter 6** presents the theoretical background of the quantum dots and introduces the measurement equipment. **Chapter 7** concludes the research by presenting electrical characterisation results on Hall and quantum dot measurements in the addressed platforms, such as Ge/SiGe heterostructures, Si/SiGe heterostructures and SiMOS that are in-house and foundry fabricated. Closing, the complete study is summarised in **Chapter 8** of the conclusions.

Although this thesis does not cover the topics of **teaching** and **scientific outreach**, the author wishes to share his thoughts on the subject. Instructors should approach tutorials with the assumption that students are starting from scratch and have no expectations from them. Positive reinforcement and patience lead to faster progress. This approach will soon motivate students to become independent and to collaborate as experienced experimentalists. More importantly, they will appreciate scientific research. The only requirement from the students is humility. Overconfidence in a laboratory can result in biased conclusions or, even worse, put the equipment and their lives at risk. These insights are based on the author's personal experiences as both an instructor and a student. Remember to have fun, and **please take care of your students**.

This thesis is intended to serve as a handbook for future researchers who will ambitiously attempt to produce spin qubit heterostructures and devices. It addresses potential challenges and provides insights into the fabrication tools and processes. Whether the reader is new to the field and is seeking an introduction, or has experience but is looking for answers, this thesis attempts to satisfy their needs. For

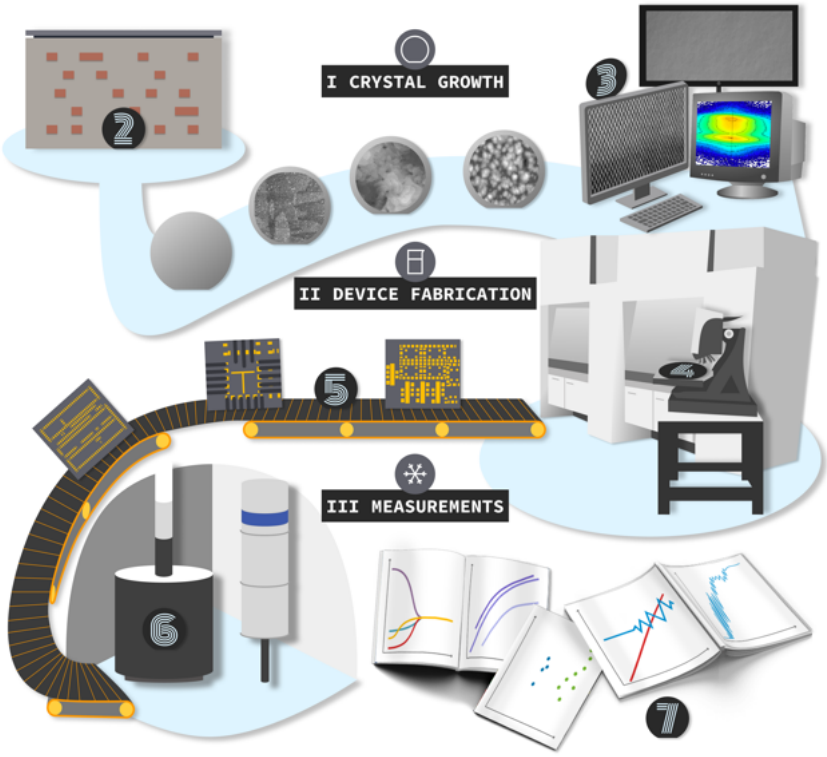


Figure 1.2: Visualisation of the contents of this thesis. Three main parts are distinguished: (I) Growth, (II) Fabrication, and (III) Measurements

ease of reference, each chapter begins with a glossary of terminology used in the everyday lab life. The author blesses them with courage and extends his best wishes for success.

Charalampos (Harry) Lampadaris
Copenhagen, 2024

Part I

CRYSTAL GROWTH

2

PRINCIPLES AND METHODS

This chapter introduces the principles and methods of crystal growth epitaxy. This thesis focuses on group IV compound semiconductors and specific examples are based on this group. The chapter begins with a presentation of the different growth modes, followed by the principles of homoepitaxial and heteroepitaxial growth. The discussion extends to the theoretical frameworks of dislocation theory and mass transport, which are essential for optimizing the quality of semiconductor heterostructures. Special attention is given to the process of oxide desorption, analysing techniques used in the experimental methods of this thesis. After laying the foundations for the crystal growth, we proceed with the crystal synthesis techniques, starting with Molecular Beam Epitaxy (MBE). This is the crystal growth technique that was employed in this thesis to prepare Ge/SiGe heterostructures. The capabilities and technical details of this method are listed to highlight the advantages and the motivation for using this crystal growth technique. The chapter concludes with a comparative analysis of MBE and Chemical Vapor Deposition (CVD), outlining their respective advantages for different semiconductor applications, thereby providing essential insights into choosing the appropriate method based on specific industrial needs and scientific research goals.

Parts of this chapter are based on the author's notes from the courses taught by **Jonas Johansson** titled *Crystal Growth and Semiconductor Epitaxy* and *Nanomaterials: Thermodynamics and Kinetics* from Lund University in the academic year 2020-2021. The author extends his heartfelt gratitude for the invaluable contributions to the understanding of the subject.

2.1 CRYSTAL GROWTH

2.1.1 *Growth modes*

Crystal growth is the incorporation of adatoms in a crystal. The term *adatom* is a portmanteau of the words *adsorbed* and *atom*. Adatoms diffuse on the crystal's surface and minimize their energy on a lattice site. After that they are incorporated in the bulk. In the theory of crystal growth, three growth modes are distinguished: **Frank - Van der Merwe**, **Volmer - Weber** and **Stranski - Krastanov** [15]. Each one of these modes depends on the surface energy and the nucleus-surface contact angle. As seen in Figure 2.1, by defining a nucleus (n) as the incorporation site for the adatoms on a substrate (s) in an ambient (α) environment, the contact angle is defined as the tangent of the nucleus at the point of contact with the substrate. The surface energy is given by the formula $\gamma_{\alpha s} = \gamma_{ns} + \cos\theta \cdot \gamma_{\alpha n}$, where γ_{xy} is the surface energy for each interface described by the x, y indices. Each mode results in unique nanostructures that can be implemented as quantum devices. Most commonly, growth modes are implemented for charge carrier confinement in reduced dimensions.

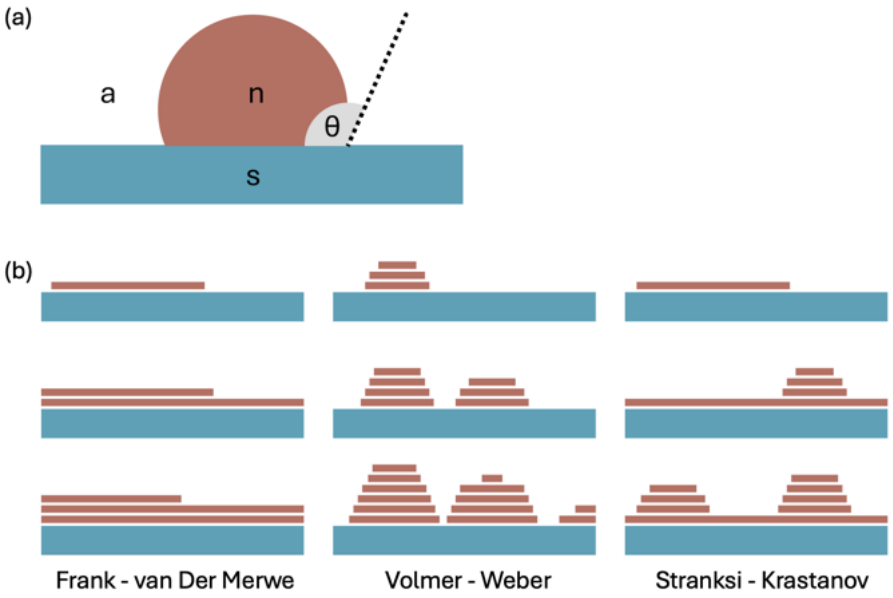


Figure 2.1: (a) Schematic of a nucleus on a substrate. The tangent at the edge of the nucleus indicates the contact angle θ. (b) Schematics of the three growth modes: Frank - Van der Merwe, Volmer - Weber and Stranski - Krastanov (from left to right)

In **Frank - Van der Merwe** mode, also called **layer-by-layer** growth, the contact angle θ is zero. The ambient-surface energy (γ_{as}) is often larger than the two other surface energies in sum ($\gamma_{ns} + \gamma_{na}$), resulting in a flat *wetting* layer. The adatoms are incorporated directly on the step edges of the vicinal surface with a small miscut. This mode is desired

for the realisation of 2D electronic materials. The highest success of layer-by-layer growth can be achieved when the deposited atoms are the same species as the substrate. Moreover, as it will be introduced later in this chapter, by using *lattice engineering*, it is possible to control the lattice constant of the deposited layers to achieve 2D growth of materials. This is also the objective of this study.

For the opposite case, the contact angle θ becomes maximum at π. This is the **Volmer - Weber** growth mode and is dominated by island formation. The nucleus-surface energy (γ_{ns}) is larger than the sum of the other two ($\gamma_{as} + \gamma_{na}$). Under these conditions, adatoms form 3D islands that usually develop in equilibrium shapes based on Wulff constructions [15], a geometric method used to predict the shapes of crystals based on the minimisation of the nucleation energy. In cases where the lattice constant of the substrate and the nuclei have a significant difference, the 3D island formation usually dominates. In group IV elements, a popular application of this mode is in the case of the germanium huts [16], where Ge islands are formed scattered on a Si substrate.

Last, the mixed phenomena of the two modes are described by the **Stranski - Krastanov** growth mode. The growth here starts with a 2D layer-by-layer and the creation of a wetting layer, and as the surface energy of the crystal changes, the contact angle is influenced, resulting in the formation of 3D islands. The ability to control the thickness of the wetting layer before island formation allows the fine-tuning of the electronic and optical properties of the nanostructures, enhancing device performance and opening pathways to novel applications.

2.1.2 *Epitaxial layer growth: homoepitaxy*

In the exploration of 2D crystal growth, we will focus first on the atomic-scale processes and the energetical phenomena that determine the features. Following, we understand the features of the surface characteristics by analysing properties such as surface relaxation and surface reconstruction.

Step-flow: Ehrlich-Schwoebel barrier

An adatom on a terraced surface can either move towards the edge of the higher or the lower step. In a descending step, the adatom is reflected due to the repulsive Ehrlich-Schwoebel barrier E_{ES}. In contrast to the diffusion in the flat surface, the edge step has a higher potential due to the lack of nearest neighbours. This leads to the reflection of the descending adatoms. On the contrary, an adatom at an ascending step experiences a trapping potential E_S that leads to incorporation.

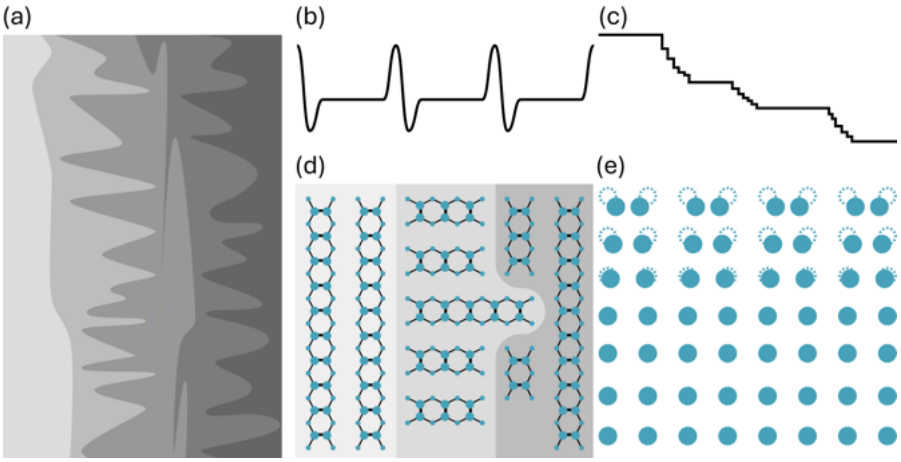


Figure 2.2: Features of epitaxial growth: (a) illustration of atomic steps in Si (001). Bright shading indicates upper steps wheres dark lower. (b) The ES barrier E_{ES} that modulates the incorporation of adatoms on upper and lower steps with a respective Si vicinal surface. When the ES barrier is not controlled, step-bunching is observed, as illustrated in (c). (d) The rough and smooth edges of each step correspond to a Si (001) surface with a 2×2 reconstruction. (d) A top-view atomic representation of the 2×2 surface reconstruction. (e) Side view showing the surface relaxation of a cubic crystal with a dimerisation for the surface reconstruction. The shadows behind the spheres represent the positions of the atoms without any surface effect being present.

This lack of symmetry can lead to step bunching and consequently disturb the step-flow growth. It has a significant effect since it dictates the growth mode by limiting the diffusion of adatoms across step edges, leading to the accumulation of material on upper terraces and resulting in rougher surface textures. The Ehrlich-Schwoebel barrier dominates the reflection of the adatoms leading to inhomogenous step-flow growth. Understanding and manipulating this barrier allows the control of layer and interface uniformity. In Figure 2.2 (b) the ES barrier is presented corresponding to the steps illustrated in 2.2 (d). When the ES barrier is significantly high step-bunching is occured as shown in the schematic cross-section of 2.2 (c).

Surface relaxation

In a hypothetical perfect crystal without surface anomalies, the inner atoms are equally bound by the top and bottom neighbouring species, forming uniformly spaced planes. However, close to the surface, planes experience the crystal potential only from one direction since there is no force from the ambient side. The symmetry is disrupted, and the last few planes are shifted towards the bulk. This phenomenon is called **surface relaxation** and refers to the contraction of the close-to-

the-surface planes. It can significantly alter the surface properties of materials, such as the electronic band structure.

Surface reconstruction

Similarly, the atoms bond with their neighbours inside the crystal based on their crystallographic properties. However, on the surface, the atoms have unsaturated bonds (dangling bonds) due to the lack of neighbouring atoms. Thus, the formation of dimers contributes to the energy minimisation in this atomic layer. As a result, a new 2D unit cell is created on the top surface. This rearrangement phenomenon is called **surface reconstruction**.

In the case of Si(001) there are two possible 2×2 atom rearrangements S_A and S_B, where one is more favourable than the other $S_A < S_B$. This inequality creates a vicinal surface where planes S_A have minimum energy and S_B planes don't. This comes from the fact that the surface unit cells of each plane are 90° rotated due to the bulk crystal symmetry. This leads to smooth edges for S_A planes and to kinked (rough) edges for S_B planes. The phenomenon was mesoscopically observable in this study and will be discussed further in the results.

2.2 VIRTUAL SUBSTRATES: HETEROEPITAXY

In heterostructures like the ones we studied in this thesis, epilayers have different lattice constants. The structural and functional integration of the layers is challenging due to the lattice mismatch. To address the issue, a **virtual substrate** (VS) is employed to act as a buffer layer and accommodate all the imperfections, facilitating enhanced structural coherence. In our approximations, we define the **natural misfit** as $f_0 = \frac{a_S - a_L}{a_L}$, where a_S is the lattice constant of the substrate and a_L is the lattice constant of the deposited layer. When the epilayers are thin, the mismatch is expressed in terms of strain, and the layer adapts the lattice constant of the parental crystal. However, if the layer gets thicker, excess strain in the crystal is released in the form of dislocations, and the layer adapts the lattice constant of the bulk material. Since we are dealing with multi-epitaxial growth, we aim to induce strain relaxation in the buffer layers and eliminate the propagation of dislocations as we get closer to the carrier region. Moreover, the objectives of device realisation require strained layers to enhance the electronic properties of the system. Thus, careful development of crystal synthesis is crucial for the success of the project.

Critical thickness h_c is a criterion to define elastic or plastic relaxation of the epitaxially grown layer. When the layer is thicker than h_c, strain is relaxed by introducing dislocations, and the layer is **plastically relaxed**. On the other hand, maintaining a layer thickness below the critical limit, there is no dislocation formation and the layer is **elastically relaxed**. Both cases have a direct effect on the electronic structure of the system and can be utilised for the realisation of unique material properties. In literature, many methods exist to increase the critical thickness and reduce dislocations by plastic relaxation. Dislocations are inversely proportional to the layer thickness. Thus, growing thick buffer layers is a way to minimise the dislocation density. Also, buffer layers with a graded composition to transition from one lattice constant to another effectively reduce strain fields in the crystal. It has to be noted here that linear buffer layers are the most common approach, but studies have shown that a non-linear profile can also be advantageous [17]. For the current study, thick buffer layers and linear grading are employed to control the critical thickness and reduce the dislocation density.

2.2.1 *Dislocation theory*

One of the main pitfalls of virtual substrates is the formation of dislocations due to the high lattice mismatch. The most common mode of relaxation is the formation of *misfit dislocations*, which is the formation of gaps in the lattice domain at the interface of the two crystals. The missing atomic planes on one side of the crystal arise

from the mismatch and disrupt the continuity of the lattice on the vertical axis. A mechanical and electronic degradation in the material quality is expected.

Within Burger's theory, two vectors and a loop are required to describe a dislocation. Small vectors with the length of one lattice constant start from a point and create a loop. If no dislocations exist in the crystal, this would result in a *closed* loop. In the presence of a dislocation, an additional vector is needed to create a closed loop, known as the **Burgers vector** $\overrightarrow{b}$. The loop enclosing the dislocation is called **Burgers circuit**. The dislocation itself is manifested by the insertion of an extra atomic plane within the crystal called the **dislocation plane**. Last, the vector running along the dislocation plane is called **line vector** $\overrightarrow{l}$. Based on the two vectors' angles, dislocations are classified into two main types, the **edge** and **screw** dislocations. On the former, the condition is $\overrightarrow{l} \perp \overrightarrow{b}$ and on the latter, $\overrightarrow{l} \parallel \overrightarrow{b}$. Typically, in nature, dislocations are mixed with an edge and a screw component ($\overrightarrow{l} \cdot \overrightarrow{b} = lb\cos\phi$). Dislocations originate on surfaces and interfaces. When they can propagate through layers, they are called **threading dislocations**, and they can form **dislocation networks**.

Misfit dislocations are equilibrium misfit defects. They are most commonly generated at the interface between the two layers. Misfit dislocations produce pairs of threading dislocations. Furthermore, threading dislocations can exist from lower layers inside the substrate and propagate through interfaces. This transmission is usually accompanied by a displacement due to the misfit stresses. Many models were developed to associate the critical thickness of a heteroepitaxial growth with the misfit dislocations. They are based on the stress comparison between a fully strained and a relaxed layer. In Figure 2.3 a, the representation of a misfit dislocation with the associated planes and vectors is illustrated.

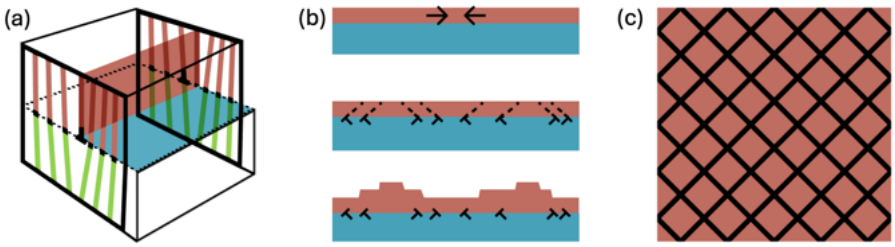


Figure 2.3: (a) A misfit dislocation in a crystal arising from lattice mismatch between two planes. Vectors related to the dislocation are denoted for clarity. (b) Network of dislocations in diamond crystals arising from the excess stain of the epitaxial layer and resulting in surface undulations similar to the ones of the schematic in (c), indicating a crosshatch pattern.

In the heteroepitaxy of SiGe layers on Si(001), 60° dislocations are common at the interface [15]. These defects propagate by glide in low-

energy {111} slip planes, resulting in a network of misfit dislocations along [110] and [1-10] directions. This is based on the diamond crystal structure of Si and Ge, where they have Burgers vector in the <110> directions and {111} slip plane.

The network of misfit dislocations is projected at the surface of the heterostructures with a **crosshatch pattern**. In Figure 2.3 b, a demonstration of the relaxation from the excess strain between the substrate and the upper layer results in misfit dislocations that influence the surface morphology and form periodic irregularities. The crosshatch pattern arises due to the relaxation of the strain through the formation of these dislocations, which intersect and create a distinctive grid-like appearance on the surface. In semiconductor applications, where electronic properties are sensitive to structural defects, the presence of this pattern can impact the uniformity and performance of the devices. Thus, understanding and addressing this issue can be crucial for the development of quantum devices.

Point defects and impurities are also another source of dislocation nucleation in these systems. They are expressed as half-loops at the film surface and propagated as threading dislocations. Focusing only on the periodic 60° misfit dislocations, we can express the critical thickness for the strained layer according to transcendent equation 2.1 [15]. For different misfits between the VS and the thin film, we can calculate the critical thickness h_c.

$$h_c = b\frac{1-\nu\cos^2\alpha}{8\pi|f_0|(1+\nu)\sin\alpha\cos\beta}\ln\left(\frac{\rho h_c}{b}\right) \tag{2.1}$$

Assuming biaxially strained layers with a given Poisson ratio $\nu = 0.25$ and setting the factor $\rho = 4$ for the strain energy of the dislocation core, we can numerically obtain the plots of Figure 2.3 b. According to the diamond structure assumptions that we introduced, the dislocation-related angles α and β are 60° and 54.7°, whereas $b = \frac{a}{2} \times [101]$. Based on these calculations, we see that the critical thickness of the heterostructures should be a few monolayers. However, experimentally, we will see that this can be extended.

The growth conditions, such as temperature and growth rate, have yet to be investigated, and a comprehensive study is outside the scope of this thesis. However, here, we provide evidence that compared to the more conventional fast growth rate of chemical vapour deposition techniques, a low growth rate could be beneficial for avoiding the formation of dislocation networks.

2.2.2 *Mass transport*

Diffusion is mass transport by atomic motion. Three mechanisms are distinguished in mass diffusion in solids. First, **substitutional diffu-**

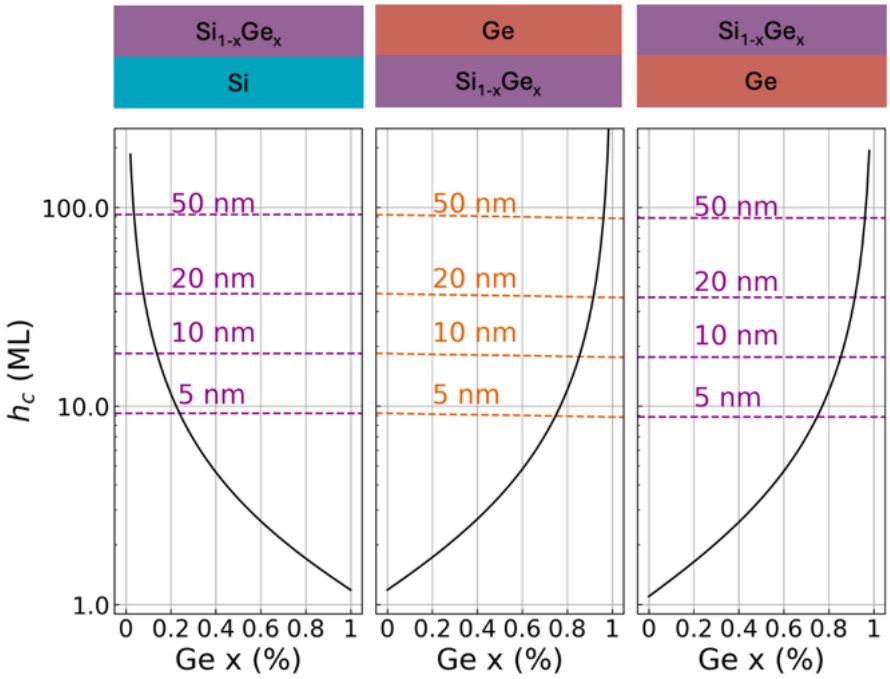


Figure 2.4: Critical layer thickness based on equation 2.1 for the three cases encountered in this study. The units of the y-axis are in monolayers of the deposited crystal. Annotated dashed lines give the conversion into layer thickness in units of nm. The conversion is based on Vegard's rule

sion occurs when an atom swaps places with a vacancy. The second mechanism is **interstitial diffusion**, which occurs in the interstices of the lattice. This phenomenon requires the small diffusing atoms and weak bonding energy of the diffusion atoms to the crystal sites. Last, is **swapping places** between the particles. In steady-state the diffusion flux does not change in time and the mass diffusion flux is described by Fick's first law $\overrightarrow{J} = -\mathbf{D}\overrightarrow{\nabla}c$, where $\overrightarrow{J}$ is the net flux of atoms, $\mathbf{D}$ is the temperature-dependent diffusion coefficient tensor and $\overrightarrow{\nabla}c$ is the concentration gradient.

A very fascinating phenomenon related to mass transport is the formation of **Kirkendall voids**. In alloys, atomic species have different diffusion coefficients, and mass transport due to substitutional diffusion in the crystal is not balanced. The larger diffusivity of one elemental component over the other leads to the formation of voids, inhomogeneities in the alloy, and porosity. Kirkendall [18] first demonstrated this phenomenon with a brass (alloy of Cu-66% and Zn-34%) bar and Mo (insoluble) rods as markers inside it. The bar was coated with Cu. Under elevated temperature, Zn diffused towards the shell, moving the Mo rods closer to each other. As we will see in the results, pure layers of Si and Ge under elevated temperatures can exhibit similar phenomena by creating vacancies in the layers.

2.3 OXIDE DESORPTION

To initiate crystal growth, the surface of the wafer is required to be pristine without defects or impurities that may hinder the growth process. In this thesis, crystal growth was performed always on Si (001) wafers. However, preconditioning of the surface is required to achieve clean and atomically flat synthesised surfaces. The removal of a native oxide layer (SiO_2) poses a significant challenge, and in this thesis, we investigated this subject with multiple approaches. In general, native oxides form naturally when silicon is exposed to oxygen, either during wafer processing or from ambient air. In the high vacuum systems that we employ for this study, we are confident that once the oxide is removed, we can safely proceed to the next processes. Moreover, the capabilities for controlled oxidation provide a significant advantage on the termination film of the heterostructures.

The removal of the oxide layer is often referred to as **oxide desorption** and can be addressed by multiple methods. A conventional approach to remove surface oxides is by thermally activating the wafer native oxide. However, prolonged dwelling at these temperatures can also activate the atoms of the substrate and form vacancies that will be detrimental to the quality of the growth. This method depends on the oxide thickness as well as the operational temperature.

Another method that operates at much lower substrate temperatures and hence reduces the probability of the formation of surface defects is desorption by **atomic-hydrogen (a-H) irradiation**. By supplying hydrogen radicals, SiO_2 and hydrocarbons have been shown to be removed completely at significantly lower temperatures [19]. The required dose for oxide removal depends on the technical details of the chamber, such as the cracking efficiency of the atomic hydrogen source and the distance between the source to the sample. This makes the process unique to every apparatus, and individual optimisation is required in every setup. The chemical reaction for the desorption of SiO_2 is assumed [20] to be

$$SiO_2\,(s) + 2\,H^*\,(g) \longrightarrow SiO\,(g) + H_2O\,(g)$$

Elemental analysis of processed wafers with each method is required to gain knowledge insights about the background contamination arising from the purity of the initial clean surface. As it has already been shown in *Yujia Liu's* PhD thesis [19], the level of carbon and oxygen contamination is significantly reduced with the use of a-H. The experimental evidence from her thesis is provided in Figure 2.5. Overall, a-H offers higher selectivity, where H reacts only with the native oxide and carbide contaminations and not with the Si atoms of the substrate. Moreover, this gives the opportunity to perform the process at a lower temperature and contributes to a lower thermal load for the

surface atoms. As a result, the combination of surface flatness with the low impurity background can initiate flatter epitaxial growth with a minimum level of contaminants. The impurities elemental analysis motivated this study to compare different substrate preparation methods and verify the advantages of adopting a-H irradiation in the substrate preparation process. However, due to time constraints, these experiments are not included in this thesis but only in the manuscript of [21].

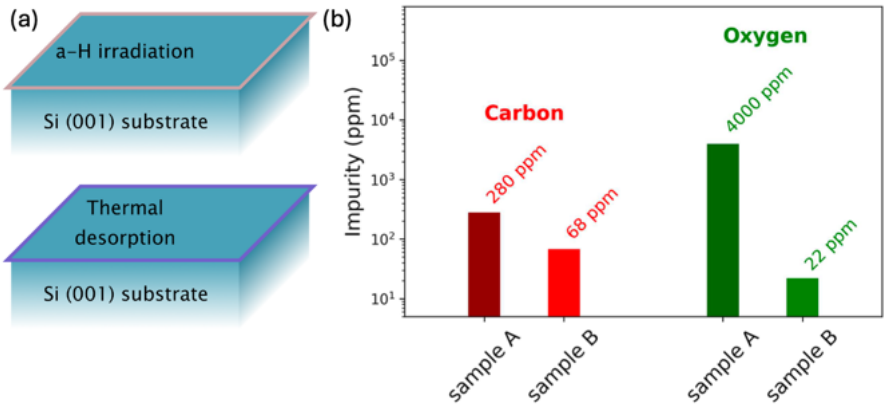


Figure 2.5: (a) Schematics of a-H irradiation and thermal activation. (b) Secondary-ion mass spectroscopy data from Reference [19] motivate the use of a-H irradiation also for the low impurity levels.

2.4 MOLECULAR BEAM EPITAXY

MBE is a crystal growth technique developed in the 1960s for the synthesis of single-crystal semiconductor films. The principle of the system is simple: a thermally activated molecular beam deposits material on a host crystal with atomic precision. MBE offers precise monitoring of thickness and structural characteristics through in-situ capabilities such as RHEED and QCM. The most pronounced characteristic of the technique is the ultra-high vacuum. The material sources are heated up and evaporated towards a rotated substrate. While in literature, Knudsen cells [15] are commonly associated with MBE, the experiments described in this thesis utilise electron beam evaporated sources. In this case, the apparatus is also known as solid-source MBE (SS-MBE).

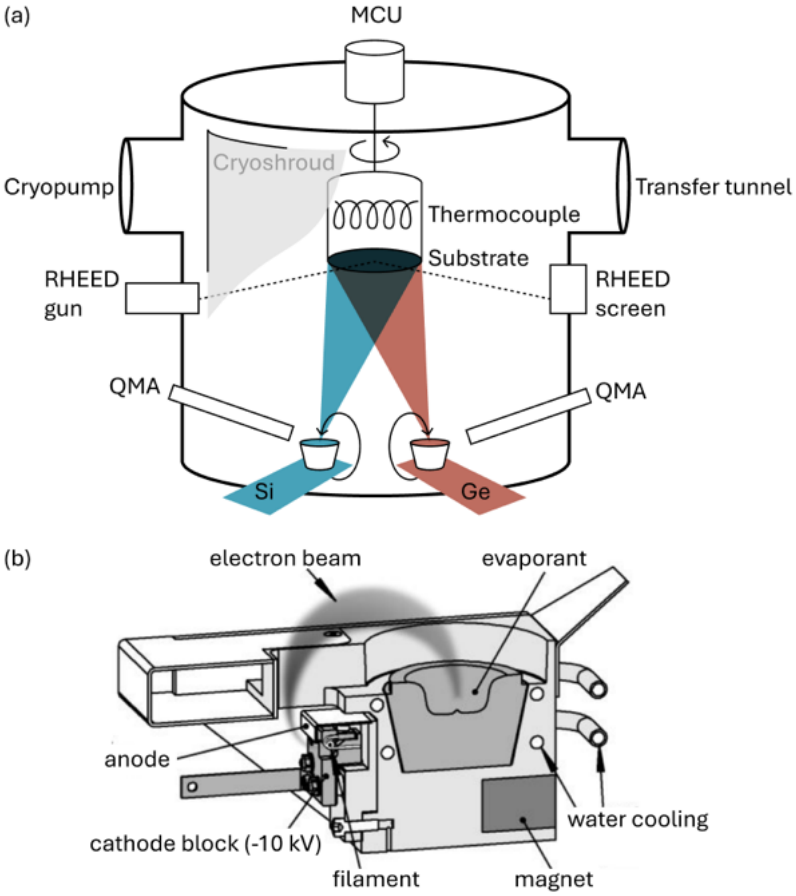


Figure 2.6: (a) A schematic of an SS-MBE chamber with all the essential components. The sources are in crucibles, and their evaporation is based on the principles of electron beam evaporation, as illustrated in (b). The main components of the MBE chamber from top to bottom are the substrate manipulator with a thermocouple, a cryoshroud, cryopumps, RHEED components, quadrupole mass analysers, and material sources.

The requirement for ultra-high vacuum conditions ensures the molecular (or atomic) nature of the sources. This lack of atmospheric particles in the chamber ensures the high quality of the films since there are no impurities to be incorporated. All materials within the vacuum chamber exhibit minimal gas evolution and high chemical stability. Molybdenum, stainless steel and tantalum are the most common manufacturing materials to fulfill this requirement. Large cryogenic pumping systems ensure continuous UHV. Once the tool is evacuated from atmospheric pressure, baking with heater filaments (usually built-in bake-out jackets) is required to desorb contaminants and moisture from the side walls of the main chamber.

In the SS-MBE, molecular evaporation is realised by electron beam sources. Their operation is described below, accompanied by the illustration of Figure 2.6 b. A tungsten coil filament is heated by a high current, and due to thermionic emissions from the hot surface, electrons exceed the binding energy with a low velocity. An anode is held on a ground potential, and a cathode, where the electrons accelerate, is on a negative high voltage, typically -10 kV. If the beam is not deflected, the electrons reach the anode. However, by employing a special geometry on the cathode's edge shield, a sharp bow in the electric field lines makes the electrons miss the anode as a target. Then a transverse-field magnetic lens bends the electron beam 270°. A special focusing configuration is required in this step to produce a small beam impact spot for high evaporation rates at relatively low power inputs. Last, the robustness of the design should be highlighted, where the separation of the filament from the crucible via the electrostatic lenses provides a long lifetime for the components.

Upon impact, 99.9% of the beam penetrates the material, heating it by electron-electron interaction yielding an energy flux $10^4 \mathrm{Wcm}^{-2}$. Materials employed should be able to dissipate this energy by evaporation, conduction and radiation. If the energy is not dissipated, vapour bubbles cause material *spitting*. There are multiple techniques to keep the power density constant while increasing the evaporation rate. Defocussing of the beam or sweeping the beam around the crucible area are usually employed to distribute the energy across the entire material surface while keeping high rates. In general terms, evaporation from an electron-beam source has many similarities with evaporation from a convection-heated source. Two key differences distinguish electron-beam sources: The crucible is cooled and does not react with the evaporated material, resulting in higher purity. Second, the high energy flux can produce high temperatures typically at 10^5 K resulting in high evaporation rates.

2.5 COMPARISON BETWEEN MBE AND CVD METHODS

Chemical vapour deposition

Another method for growing epitaxial structures is the **chemical vapour deposition** (CVD), which has a different adatom incorporation principle. In CVD, precursor gases transferred by a carrier gas enter the chamber, where chemical reactions occur on the wafer surface, followed by adatom incorporation in the crystal. CVD had a crucial role in the progress of SiGe epitaxy, facilitating both industrial-scale integration and academic research in nanostructure development. Initially, the technique faced challenges, with early attempts at Si film deposition requiring high temperatures above 1000°C. Technological advancements in vacuum technologies have led to more controlled and efficient processes, reducing the growth temperature to around 500°C for high-quality thin layers and enabling the precise growth of SiGe epitaxial layers at lower temperatures with improved quality and scalability. Low pressure and temperature growth suppresses oxygen and moisture levels in the chamber and reduces the adatom diffusion, contributing to sharp interfaces and thin films. In Table 2.1, typical pressure ranges for various CVD techniques are given. Nowadays, a reduced pressure CVD (RP-CVD) technique is the state-of-the-art method to produce wafers for semiconductor spin qubits [22, 23]. Most common precursors for Si and Ge epitaxy are SiH_4, Si_2H_6, SiH_2Cl_2 and GeH_4. These precursors are transported with a carrier gas, which is usually H_2, onto the chamber, where chemisorption, the chemical reaction of the wafer with the precursors, takes place. Chemical reactions at the hot wafer surface lead to epitaxial layer growth. The volatile reaction byproducts of the reaction are transported with the carrier gas to the vent.

Type	Base pressure (mbar)	Deposition pressure (mbar)
Atmospheric pressure	10^3	10^3
Reduced pressure	10^{-2}	$10^1 - 10^2$
Low-pressure	$10^{-7} - 10^{-9}$	$10^{-1} - 10^0$
Ultra-high vacuum	10^{-9}	10^{-3}

Table 2.1: Pressure levels on different CVD systems based on Reference [24]. MBE operates at UHV and the deposition pressure is as low as 10^{-9}mbar.

The core principles of the CVD method can be distinguished into five processes as depicted in Figure 2.7. The precursor gases are transferred in the reactor by the carrier gas representing the **source**. Upon reaching the wafer, the chemical surface reaction occurs, chemical reactions, with **adsorption**, diffusion of the atoms leading to nucleation,

crystal growth, and **desorption** of the chemical reaction byproducts. Vertical diffusive transport, from the carrier gas to the surface and vice versa, contributes to the incorporation of gas molecules into the chemical processes. The growth rate is limited by the slowest process among the three incorporation steps. In Figure 2.7, the key components of the CVD growth method are highlighted through a schematic representation. Following the objectives of this thesis, the description is given for Si homoepitaxy. Additionally, a diagram of a CVD chamber is provided to facilitate an easier visualization of the apparatus.

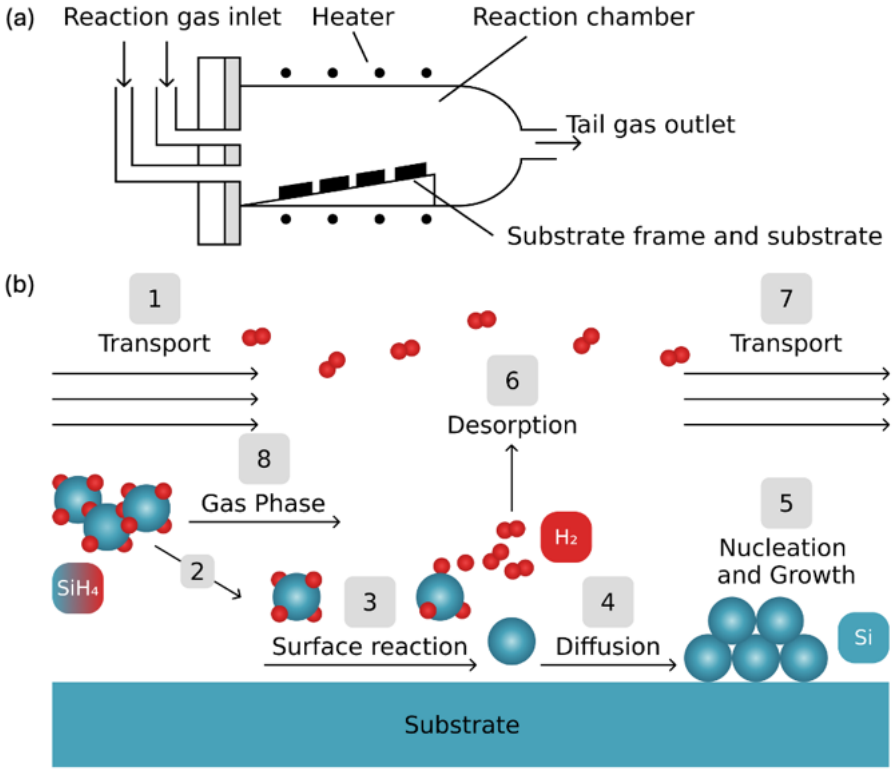


Figure 2.7: (a)Schematic of a CVD chamber containing the essential components. (b) Illustration of the CVD growth method. A H_2 carrier gas is used, and SiH_4 is the precursor gas to incorporate Si atoms in a Si substrate. All steps related to incorporation are annotated for clarity. The representation does not flow any specific crystallography.

Comparison of growth methods

The two crystal growth methods described in this chapter have unique technical specifications, operational principles, and capabilities. We aim to identify their respective strengths in terms of efficiency, scalability, and quality while focusing on specific applications. We provide insights into the suitability of each of the processes in materials synthesis and further device fabrication. Additionally, we discuss potential perspectives for future research directions.

Oxide quality

One of the most important differences lies in the vacuum conditions of each technique. In MBE, not only the growth but also the handling of the wafers takes place under UHV. This means that the terminating surfaces stay pristine without the incorporation of impurities. More importantly, the oxidation of the terminating layers is usually under controlled pure oxygen, which is the highest quality of oxide one can produce. In contrast, in CVD (even with reduced pressure), crystal growth is performed under hydrogen flow, and the surface termination is under atmospheric air. This incorporates nitrogen and atmospheric impurities that can act as two-level systems. Many techniques have been developed to increase the quality of this oxide, such as, for example, with the growth of dichlorosilane SiH_2Cl_2. This brings, in principle, MBE samples to a more advantageous point regarding charge noise from the heterostructure. However, a comparison of fabricated wafers from MBE and CVD is not reasonable unless the devices have undergone the same steps and were processed by the same tools. For example, the oxide dielectrics may have detrimental effects on the system's noise level. Even though it is independent of the growth technique, it may produce misleading results, so a one-to-one comparison is yet to be demonstrated.

Temperature range and growth rate

MBE operates at lower temperatures, which can kinetically suppress misfit dislocation formation. This is also combined with the limited growth rate and low pressures, providing optimal conditions for flat and thin film epitaxy. It has been observed that MBE-grown strained ^{28}Si and Ge layers on relaxed SiGe substrates are free of misfit dislocations, even when their thicknesses exceed the critical thickness [19]. On the other hand, CVD is known for the higher temperatures in the reactor but also the enhanced growth rates. However, the operational vacuum is inferior compared to MBE techniques, resulting in the incorporation of a large number of impurities in the crystal. To counteract this, high growth rates are employed to produce more pristine samples.

Scalability

Although MBE can produce high-quality samples, the accommodation in large-scale industrial settings is limited due to inherently low throughput. For example, in the cases of Si and Ge that this thesis focuses on, the atomic beams are directed on a single rotated wafer and simultaneous processing of multiple wafers is impossible. The sources have limited material, and frequent calibrations are essential for high reproducibility. Moreover, lack of uniformity occurs when wafers above 200 mm are employed [15], whereas standard large-scale integration processes employ 300 mm wafers or larger. Last, MBE

systems are highly demanding and expensive. The requirement for continuous vacuum and cryogenic cooling circulation is a daily challenge for the laboratory's economy. Moreover, the long downtimes for maintenance and regular material refilling accompanied by post-maintenance chamber baking limit the availability of the system and require thorough planning before conducting a research investigation. On the other hand, CVD offers parallel processing of multiple wafers up to 12 inches, and it is compatible with large-scale infrastructures. This makes CVD SiGe knowledge easily transferable from academic labs to industry.

Physical challenges for the experimentalist

In CVD, the high growth rates stand for the benefit of the experimentalist. The growth time of a CVD heterostructure can be ten times shorter than that produced by standard MBE. Consequently, growing a single wafer is less time-consuming, allowing the development of multiple samples within the same day. In contrast, only a single MBE wafer can be developed in a day.

To grasp the level of challenge, the workflow processing is demonstrated here. Each wafer was initially loaded in the heating station for cleaning with atomic hydrogen irradiation. This required coordination with the members of the MBE cluster since the gas handling lines are used for both oxygen and hydrogen. The cleaning process is classified as high-risk and no such similar experiments should run in parallel. The total process for the surface treatment could take over an hour, and afterwards, the wafers were loaded in the MBE chamber for crystal growth. It must be mentioned that transferring the samples between different chambers requires the coordination of two people: one to control the holder and one to guide them from the viewport. The growth process lasted approximately eight hours. Both before and after the growth recipe, manual ramping of the sources was required until reaching the automatic control range of the PID (Proportional – Integral – Derivative) controller. With only two wafer holders available, it was only possible to up to perform two growths in two consecutive days. The following day was reserved for unloading and initial processing tasks such as cleaving, AFM, and cross-sectional SEM. Subsequently, coordination with cluster members was demanded to ensure the availability of the transfer tunnel, load-lock, and cleanroom wet bench for chemical processing. In summary, due to physical constraints, we were limited to growing a maximum of four wafers per week. The slower development pace and the physical challenges associated with long hours spent inside the lab make CVD development a superior method for SiGe thick heterostructures.

Electrical properties

In the research of Ge/SiGe heterostructures, it is common knowl-

edge that hole mobilities are remarkably enhanced by CVD and the optimisation for MBE methods has been left behind. In this study, we hope to inspire laboratories for further development of MBE samples and to explore the capabilities and limitations of this technique.

Remarks

To conclude, both methods have their respective advantages and disadvantages. In Table 2.2, a summary captures the distinct differences in terms of physical properties and tool capabilities. It is clear that there is not one tool to rule them all. The experimentalist should carefully assess the specific qualities they seek and balance them against the inherent limitations. This thesis attempts to provide evidence and bridge existing gaps between the two approaches that lead to qualitative differences. Furthermore, the potential of hybrid SiGe heterostructures has been demonstrated in multiple studies [25, 26], showing that combining the strengths of both CVD and MBE techniques can yield significant benefits. These hybrid approaches, even though they are challenging to implement, can have a valuable impact on the general development of quantum technologies.

	MBE	CVD
Growth rate	Only low	Only high
Termination	Oxidation	Ambient air
Temperature range	Low to high	Only high
Pressure range	UHV	Air to RP
Capacity	Low	High

Table 2.2: Comparison of the physical limitations and tool specifications between the MBE and CVD methods.

3

GERMANIUM HETEROSTRUCTURES BY SS-MBE

This chapter introduces the methodologies and systems utilized in the realisation of Ge heterostructures via SS-MBE. Focusing on the initial development of the heterostructures, the preparation stages are described, such as source calibration, surface treatment, and the formation of the VS. Having all the details presented, the grown heterostructures are introduced along with their detailed specifications. A comprehensive overview of the structural characterization techniques follows. Imaging and elemental analysis techniques such as Transmission Electron Microscopy (TEM), X-ray Diffraction Reciprocal Space Mapping (XRD RSM), Atomic Force Microscopy (AFM), and Nomarski Optical Microscopy, along with the evaluation of threading dislocation density (TDD) comprise the characterisation of the structural features of the grown wafers. This chapter introduces the ex-situ deposition of niobium-titanium nitride (NbTiN) and explores the capabilities of the heterostructures towards spin-photon coupling. Lastly, the insights gained from these investigations offer perspectives on future advancements and potential applications of the studied heterostructures.

The project was conceptualised under the supervision of **Peter Krogstrup** towards record mobility Ge quantum wells and was initially commenced in collaboration with **Henrik Ingerslev**. Once underway, the SiGe team was composed of the author, **Jesús Herranz Zamorano** and **Sabbir Ahmed Khan**. The crystal growths, AFM, SEM, and XRD data were taken in different stages of the project, and all three team members contributed. The analysis was performed by the author. Special thanks go to **Evgeniy Shkondin** for his invaluable support with the XRD tool at DTU. The TEM was performed by **Sara Martí-Sánchez** and **Marc Botifoll** under the supervision of **Jordi Arbiol** in Institut Català de Nanociència i Nanotecnologia (ICN2).

3.1 THE MBE SYSTEM

We use a customised SS-MBE system based on the *Dr. Eberl MBE Komponenten GmbH OCTOPLUS 600* with two electron gun evaporators for the Si and Ge sources. It is part of a cluster with multiple MBE systems located at the *Microsoft Quantum Materials Lab* in Lyngby, Copenhagen. All MBE systems are connected in series via a UHV linear transfer tunnel (LLT). A vacuum glove box is mounted to the load lock to insert the wafers in a cassette and transfer them further into the tunnel trolleys. Transfer rods are used to move the substrates between different vacuum chambers while maintaining the UHV. A heated station (HTS) is located between the MBE system and the UHV LTT. Manual gate valves separate all UHV components. The samples are treated with a second degassing in the HTS via atomic hydrogen (a-H) cleaning by a hydrogen atomic beam source (HABS) located at the bottom of the chamber. The HTS is equipped with a motorized gas supply of purified H_2 and a quadrupole mass analyzer (QMA) to supervise the chemical characteristics of desorption and monitor the UHV. A schematic representation with the vacuum chambers of the cluster related to this study is presented in Figure 3.1 a.

The main MBE chamber is equipped with two cryogenic pumps to maintain UHV. This results in base pressure of 10^{-12} mbar and a pressure of 10^{-11} mbar while performing the growth. Liquid nitrogen (LN2) cooling significantly reduces the equilibrium pressure during material evaporation. The main purpose of the cooling shroud is residual gas condensation and the absorption of heat radiation from thermal sources. Consequently, it contributes to maintaining low pressures. Crystal growth is performed on high-resistivity intrinsic Si (001) 2-inch wafers purchased from Siltronic. The wafers are mounted facing down to the sources on a rotating substrate manipulator. The rotation of the substrate contributes to uniform growth distribution during evaporation. The manipulator controls the growth temperature with a heater and a thermocouple at the back of the sample. Two electron beam evaporators with a 100 cm^2 pocket size for matrix elements are connected at the bottom of cell ports for vertical evaporation of Si and Ge. Respective QMA's control the output of the sources. These mass spectrometers detect and count the mass of gas ions for each source material. During evaporation, Si and Ge, the beam current is correlated with the monitored QMA value. For Si and Ge electron beam evaporators, optimisation set out the deposition range in a span from 0.01 to 2.0 Å/s.

A very useful feature of the system is the refill charge pills of Si and Ge that are installed to the base flange of the sources. When the source material gets depleted, a drop in the growth rate is observed, the growth terminates immediately, and the electron beam current returns to safe mode, avoiding any damage to the instrumentation.

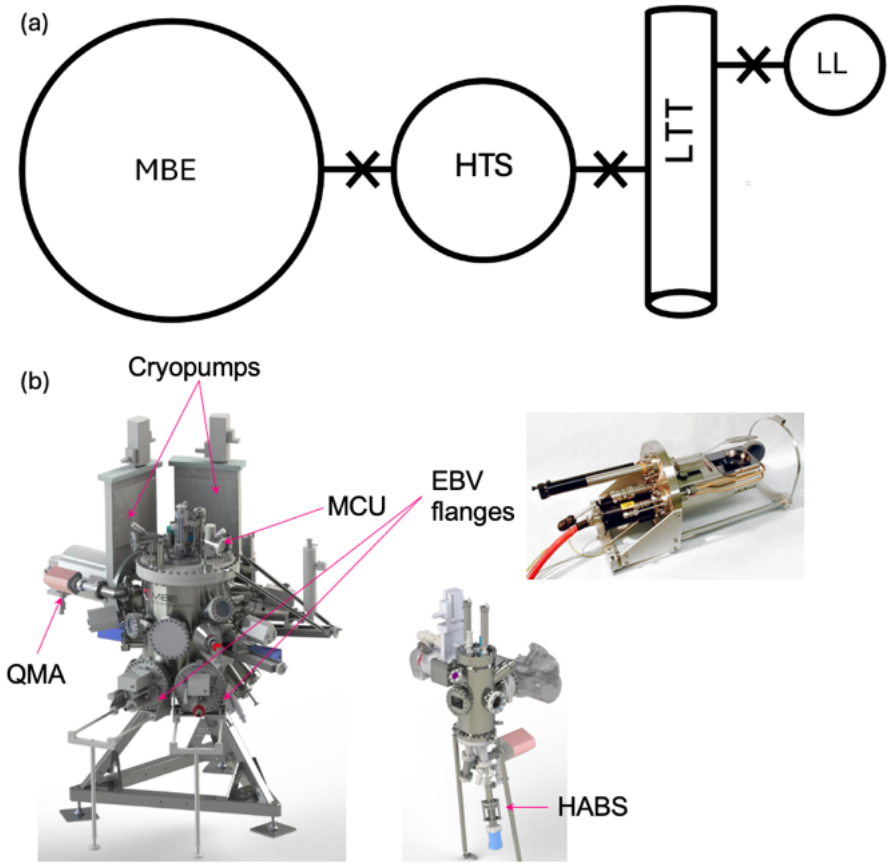


Figure 3.1: The SS-MBE system of this study. (a) A schematic of the used components in the cluster. (b) Designs of the SS-MBE and the HTS annotated with the most relevant components. A picture of the Si electron beam source is given for clarity.

Then, with the use of a slider, the first available recharge pill can be pushed forward and dropped into the almost empty crucible. Once the refill is complete, melting of the new material together with the remains of the old one is recommended. Once the process is complete, a new calibration growth is required.

The system is also equipped with a Quartz Crystal Microbalance (QCM) for monitoring the evaporation rate. It also contains an electron gun paired with a fluorescent screen monitored by a digital camera for Reflection High-Energy Electron Diffraction (RHEED) analysis, which allows in-situ monitoring of the crystal surface morphology, identifying layer-by-layer growth. Last, a pyrometer is located at the bottom of the chamber to monitor the wafer temperature. However, these components were diagnosed as faulty after their installation and maintenance required to return to an operational state.

It is important to mention that this MBE system was connected in series to more growth chamber ana analysis systems dedicated to *Industrial Corporate Research and Development*. Thus, maintenance was a task that required resources and downtime for the whole industrial lab.

This is, of course, not an ideal situation for Research and Development. Thus, component optimisation of the presented chamber was of low priority, and it was only possible to proceed with the necessary and functional resources to demonstrate proof of concepts and explore the capabilities of the system.

3.2 THE SAMPLES

3.2.1 *Source calibration*

The control parameter for the growth rate is the current of the electron gun. This current is translated to the *EpiCAD* software in **power (%)**. Then, the power is correlated to the **voltage** values of the QMA sensors dedicated to each source (cross-beam examination). Using a standard growth time of **30 minutes**, thick Si and Ge stacking layers grow with different QMA values **(0.6, 0.9, 1.2, 1.5 V)** to get a relation between layer thickness and material flux. Pure layers of Si and Ge give the advantage of high contrast between the two materials when characterised by cross-sectional SEM. Avoiding alloy concentrations and using elemental layers simplifies the growth rate calculations. However, achieving flat and smooth interfaces in such stained layers is challenging. Originally, the realisation of thin layers was not trivial due to the high uncertainty in growth rate. One key feature that helped significantly to achieve flat interfaces was the control of the Ge growth temperature. Five calibration growths were attempted and are presented in this section.

Before diving into the results, it is useful for the reader to learn about our calibration protocol and characterisation routines. Ex-situ characterization with cross-sectional SEM is used to obtain quick feedback on the linear relation between the Si or Ge layer thicknesses and the QMA values. Once the SEM images are taken, the thickness of each layer is calculated by the *ProSEM* software via contrast image analysis. Then, the linear relations for each material are uploaded to the EpiCAD software and the new crystal growths are configured with the latest calibration analysis. Moreover, the alloy concentration x in $Si_{1-x}Ge_x$ can also be tuned under the updated EpiCAD configuration data. For example, if 2 V give 2 nm of Si in 4 minutes and 1.5 V give 8 nm of Ge, then having both sources open for 4 minutes, an alloy of $Si_{1-x}Ge_x$ with $x = 0.8$ and total thickness of 10 nm can be obtained.

On the first attempt of calibrations, the interfaces between Si and Ge had significantly high roughness. However, this was sufficient to obtain a first estimate of the growth rates, which made possible the growth of the first Ge quantum well growth. Progress in the wafer preparation techniques prior to crystal growth led us to oxide-free and hydrocarbon-free surfaces. Additionally, the modification of the growth temperature ($T_{Si} = 650°C$ and $T_{Ge} = 450°C$) optimised further the calibration data and provided more accurate control of the growth rate. Moreover, with this evidence, the alloy composition was more accurately controlled for the growth of $Si_{1-x}Ge_x$ spacers and the reverse linear graded buffer layer in the heterostructures. Such a calibration proved essential for our work and was repeated regularly (every month) to keep track of the remaining material in the crucibles.

More details about the exact calibration recipe are included in the Appendix A.

A schematic of a typical calibration growth is shown in Figure 3.2 a. Moreover, typical cross-sectional SEM images of (b) the last calibration with the smoothest possible interfaces and (c) earlier stage calibration samples with high interface roughness demonstrate the process of obtaining the growth rate based on layer thickness. Bright layers indicate Ge, whereas dark layers indicate Si.

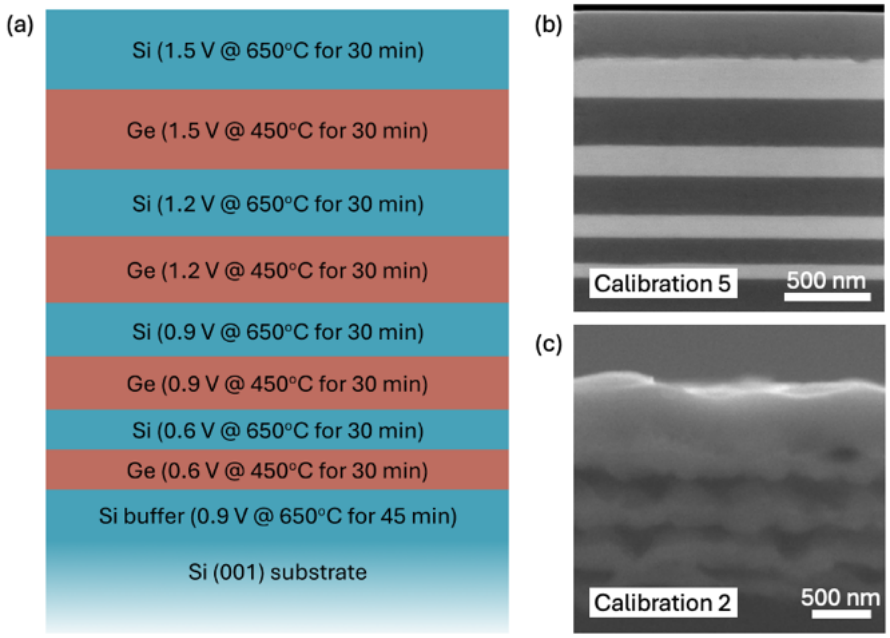


Figure 3.2: Calibration growths: (a) Schematic of the calibration growths showing the values given by the EpiCAD software, the growth temperature and duration for each layer. (b,c) Cross-sectional SEM images of different calibration rounds. In the case of (b) the Ge growth temperature was kept at 450 °C and for (b) at 650 °C.

The growth rate is calculated as the ratio of the layer thickness divided by the growth time (30 mins). Figure 3.3 presents all the successful calibration growths. Interestingly, in the **Calibration 5** sample, the growth rate of Si reached a maximum value of 0.115 Å/sec due to source limitations. This is a clear demonstration of the disadvantages when growing with SS-MBE. The low growth rate of approximately 0.15 Å/sec extends the growth time of a thick heterostructure significantly.

3.2.2 *Surface preparation*

Prior to crystal growth, clean substrate surfaces are vital to avoid impurities and dislocations. Therefore, two cleaning procedures were developed. The atmospheric oxygen reacts with the surface of the Si wafers, forming a thin layer of SiO_2. This oxide layer and any

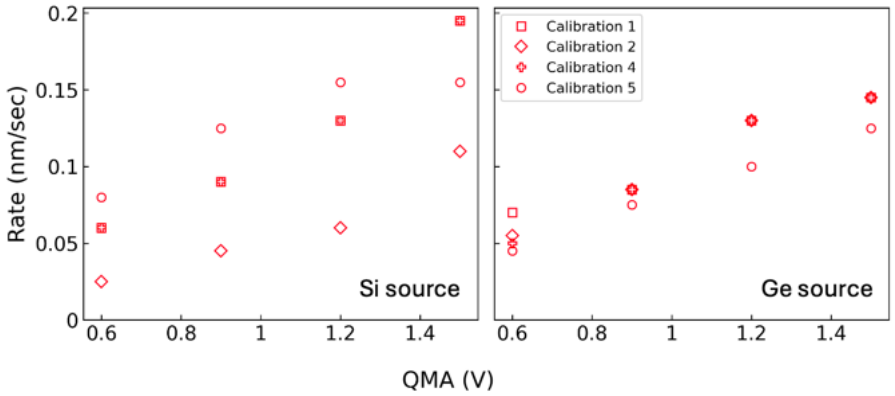


Figure 3.3: Calibration growth analysis: Datasets for Si (left) and Ge (right) sources are imported to EpiCad software to calculate composition and layer thickness while growing the heterostructures

other possible surface contaminants must be removed. Even though these are thermally activated reactants, overheating introduces defects in the crystal and compromises the quality. Two approaches were investigated to clean the wafer surface and structural characterisation was employed following the hypothesis that atomic steps would be visible only if the surface is not damaged and the native oxide is completely removed. In Figure 3.4 a, the hypothesis for a successful surface treatment is demonstrated with simple illustrations.

On the one hand, oxide thermal desorption was implemented. The wafers were first thermally outgassed in the HST for 1 hour at 800°C and then transferred to the MBE chamber. There, the samples were heated up to 1100°C for 10 minutes, while the temperature was controlled by the thermocouple of the manipulator. After the surface treatment, 300 nm of Si in a step-flow process were grown. As seen in Figure 3.4 b, atomically flat terraces were observed by AFM. Moreover, the interface between the Si wafer and the grown Si could not be resolved by cross-sectional SEM. Even though the characterization approaches verified our hypothesis, the thermal load of 800°C for one hour was a factor that needed further investigation.

Towards the optimization of the cleaning process, we implemented a-H and wet chemical etching with hydrofluoride (HF) in the cleanroom. Adding these two elements, a minimization of oxide residues together with low carbon concentration is possible [19]. For this experimental method, the surface treatment began in the cleanroom, where the samples were immersed in HF of 10% concentration for 1 minute and then in Milli-Q (MQ) water for 1 more minute. Following, they were loaded in the MBE loadlock. This was a relatively quick procedure since native oxide grows again on a clean sample. In the load lock, the samples are outgassed at 150°C for 10 hours with a pressure in the range of 10^{-9}mbar. Then, the samples were transferred to the HTS and heated to 800°C. In parallel, H_2 gas was supplied via

the HABS and heated at approximately 1550°C. This temperature breaks the molecular H_2 bonds and releases a-H in the chamber. For 10 minutes, a-H reacted with the oxide residues on the surface of the wafer, resulting in an intact surface. Similarly, with the oxide thermal desorption processed wafers, we grew 300 nm of Si, and then characterized them by AFM and cross-sectional SEM. As seen in Figure 3.4 c, atomic steps were observed in this method, providing high-quality crystal structures with reproducibility.

Overall, the root-mean-square (RMS) surface roughness is similar in both cases below 0.2 nm. However, the duration of the oxide thermal desorption method was one hour compared to the 10-minute a-H treatment. However, the thermal load was minimised, lowering the thermal budget of the wafer giving a significant advantage to the minimisation of any defect formation on the clean Si surface

Last, a-H treated sample without the HF immersion was tested. In this final case, higher surface roughness without detectable atomic terraces and mosaicity were observed in AFM. Moreover, the interface between the Si substrate and the grown Si was visible by cross-sectional SEM. This was a crosscheck that validated the hypothesis since the native oxide was partially removed from the initial Si surface.

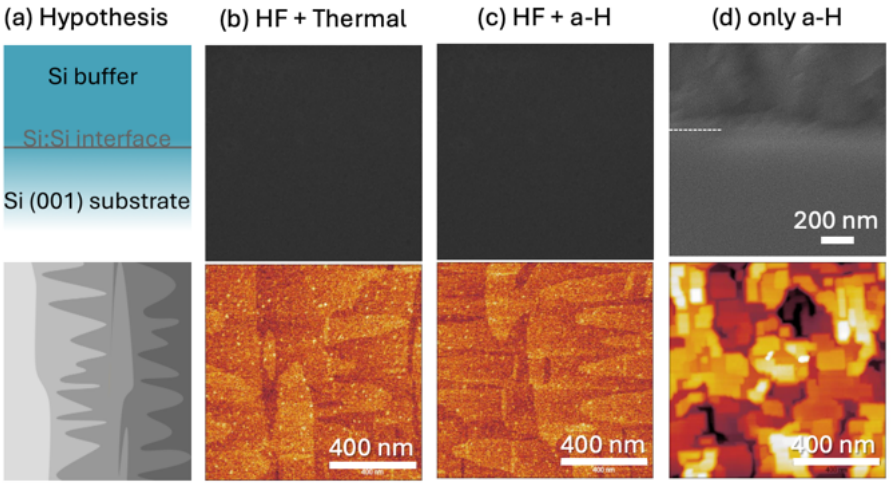


Figure 3.4: Surface treatment methods of the wafers. (a) The hypothesis where a successful surface treatment results in pristine homoepitaxial interfaces that are not visible in a cross-sectional SEM and atomic steps are observed by AFM. (b,c) Surface treatment approaches with (c) oxide thermal desorption and a-H cleaning. Both methods utilise HF wet etching prior to loading. (d) A structure where the oxide is partially removed as no HF treatment was performed but bare a-H cleaning.

3.2.3 *Virtual substrate*

The successful oxide desorption lays the foundation for the growth of the virtual substrate. In Figure 3.5, 300 nm of Si are grown and the virtual substrate (VS) is defined by growing additionally 300 nm of relaxed Ge (rGe). This VS is utilised to grow the reverse linear graded (RLG) buffer layer starting from a 100% concentration of Ge and reaching a Si_xGe_{1-x} alloy with a composition of $x = 0.2$ ($Si_{0.2}Ge_{0.8}$). This pseudomorphic growth increases the critical thickness of the compressively strained Ge (sGe) layer that hosts a 2-dimensional hole gas (2DHG) near the surface of the final heterostructure. Figure 3.5 a displays the homoepitaxial growth of Si on the Si (001) substrate. Atomic steps are visible, with the terrace edges displaying an alternating roughness every other step, following the theory of 2×2 surface reconstruction [15].

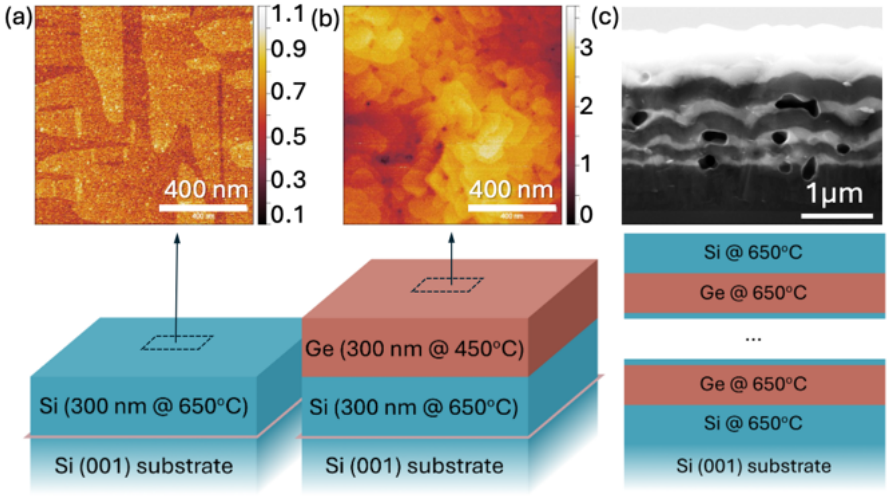


Figure 3.5: Buffer layer growth optimisation. (a) Si homoepitaxy. (b) Ge on Si heteroepitaxy. (c) effect of growth temperature and formation of Kirkendall voids due to the interdiffusion of Ge into Si.

Figure 3.5 b describes the formation of the Ge virtual substrate. As expected, the RMS roughness is significantly increased compared to the homoepitaxial growth due to the high lattice mismatch of 4.71% between Si and Ge. Pits are visible, indicating strain relaxation and dislocations [27]. We address these defects in the next step with the growth of the RLG layer and the thick buffer layer of $Si_{0.2}Ge_{0.8}$. The growth temperature for Ge is optimized to be 450°C. Above that temperature limit, diffusion of Ge into the Si layers can be observed following the Kirkendall void formation [28]. In Figure 3.5 c, a cross-sectional SEM image of thick buffers of Ge and Si (based on the calibration samples) is presented, where voids are formed due to the high growth temperature of Ge (650°C). In contrast, the low-temperature growth of Ge contributes to minimal interface roughness. According to the

TEM analysis of the complete heterostructures described further in the reading, the highly-strained Si-Ge interface is the origin of all the defects propagated on the upper layers.

3.2.4 *The heterostructures*

With the surface preparation techniques optimised and the buffer layer parameters adjusted, it is now possible to introduce the heterostructures. Here, all the growths are displayed regardless of their success. It should be stated that even though the suitable growth parameters from the previous sections were identified, the growth of the heterostructures did not follow as a natural occurrence. On the contrary, full-stack growths were attempted in parallel with the buffer optimisation.

In total **six** heterostructures were grown. Even though not all parameters were optimized, this gave clearer insights into identifying failure modes and highlighting the success of the final heterostructures. Three independent pairs (presented here as **Groups**) of heterostructures were grown while a single parameter was tuned for comparison. Figures 3.6, 3.7, and 3.8 demonstrate the surface morphologies in terms of AFM, paired with the schematic of the detailed layer stack. In the main Table of Appendix A, the cumulative growth parameters are listed.

In **Group A**, a comparison between the surface treatment methods is attempted. As described earlier in this chapter, thermal oxide desorption and a-H cleaning were employed as the two surface treatment methods. **Sample 1** employed the former and **Sample 2** the latter. However, at that stage of development, the optimal growth temperature of Ge was still an unexplored parameter, and both heterostructures exhibited high interface roughness. Both samples were discarded from any further consideration in experiments, but their valuable feedback motivated the reduction of temperature and the optimization of surface cleaning recipes. In Figure 3.6, AFM images of the surface morphology demonstrate the high surface roughness of 7.88 nm and 61.13 nm, respectively.

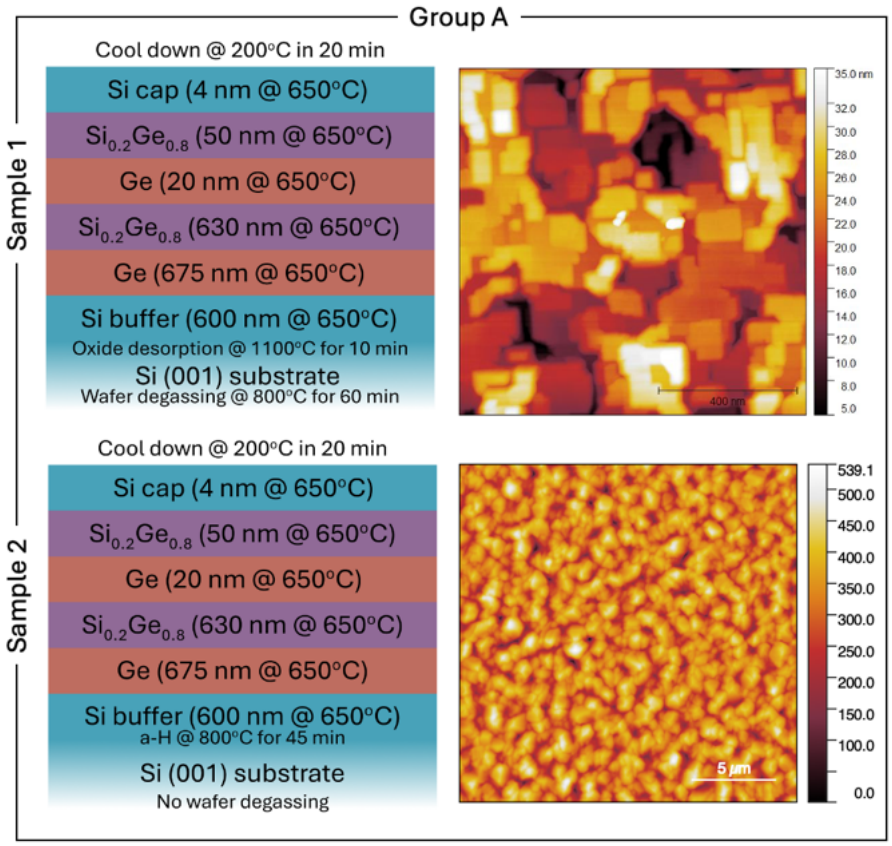


Figure 3.6: Schematics and surface morphology of Group A heterostructures. Scale bars are 400nm and 5µm for **Sample 1** and **Sample 2** respectively, and height color bar has units of nm.

In **Group B**, the growth temperature of Ge had been optimized at 450°C, and as a result, these heterostructures were considered for further applications. However, no measurement results are presented in this thesis. The surface preparation for both samples was successfully achieved by oxide thermal desorption at 1100°C for 1 hour. A single parameter was tuned between the twin growths of Group B: the temperature of the Si capping layer. The temperature of the terminating layer of **Sample 3** was 650°C, and of **Sample 4** was 450°C. According to Reference [29], once the strained Ge layer is grown, the temperature should not be increased further since diffusion can have detrimental effects on the electronic properties. Comparing the RMS surface roughness of **Sample 3** and **Sample 4**, this is verified in this thesis. This can be interpreted as increased dislocation density and higher interface roughness inside the heterostructure of the heated sample. Similar to annealing processes, dislocation phenomena may arise [30]. Last, it should be mentioned that these heterostructures *did not* employ the RLG buffer growth method but a single thick and relaxed layer of $Si_{0.2}Ge_{0.8}$ comprised the VS with a total thickness of 1000 nm.

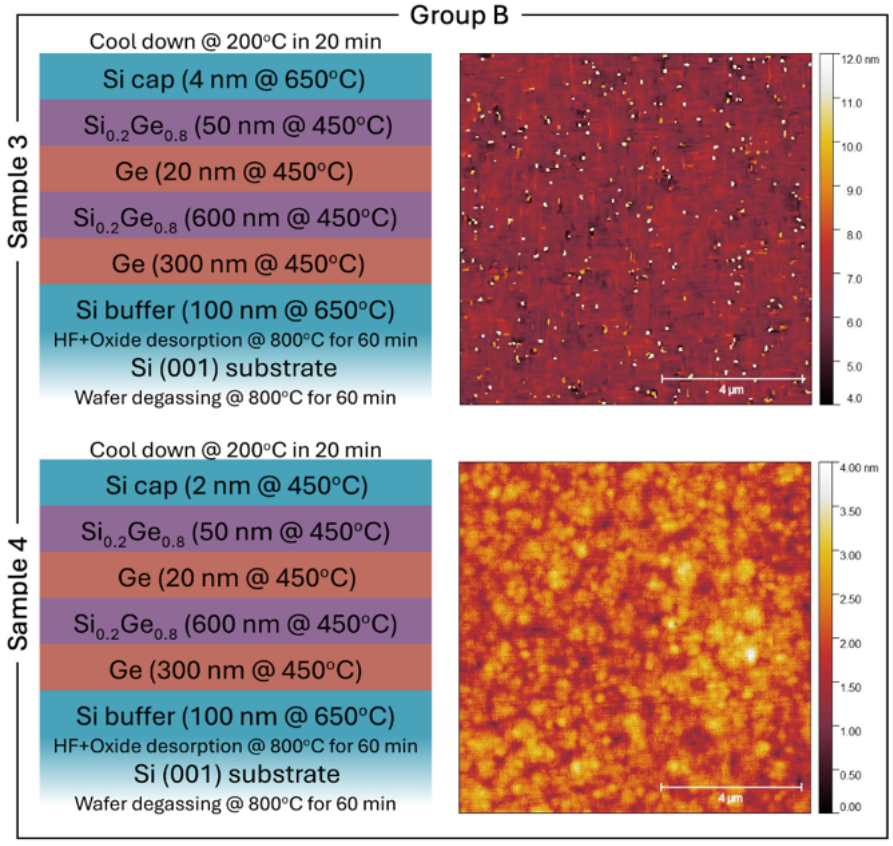


Figure 3.7: Schematics and surface morphology of Group B heterostructures. Scale bars are 4µm and height color bar has units of nm.

In **Group C**, two heterostructures were grown under the same conditions, but the thickness of the buffer layers was tuned. Both samples were prepared by chemical etching in the cleanroom and atomic hydrogen cleaning (800°C for 10 minutes). The total buffer thickness of **Sample 5** was 1000 nm, and of **Sample 6** was 2000 nm. Once the first silicon buffer was grown, the temperature was kept at 450°C for the whole procedure. The RLG method was employed for both samples. These two growths were shipped for TEM, giving insights into the elemental composition and the dislocation formation. These results are presented later in this chapter.

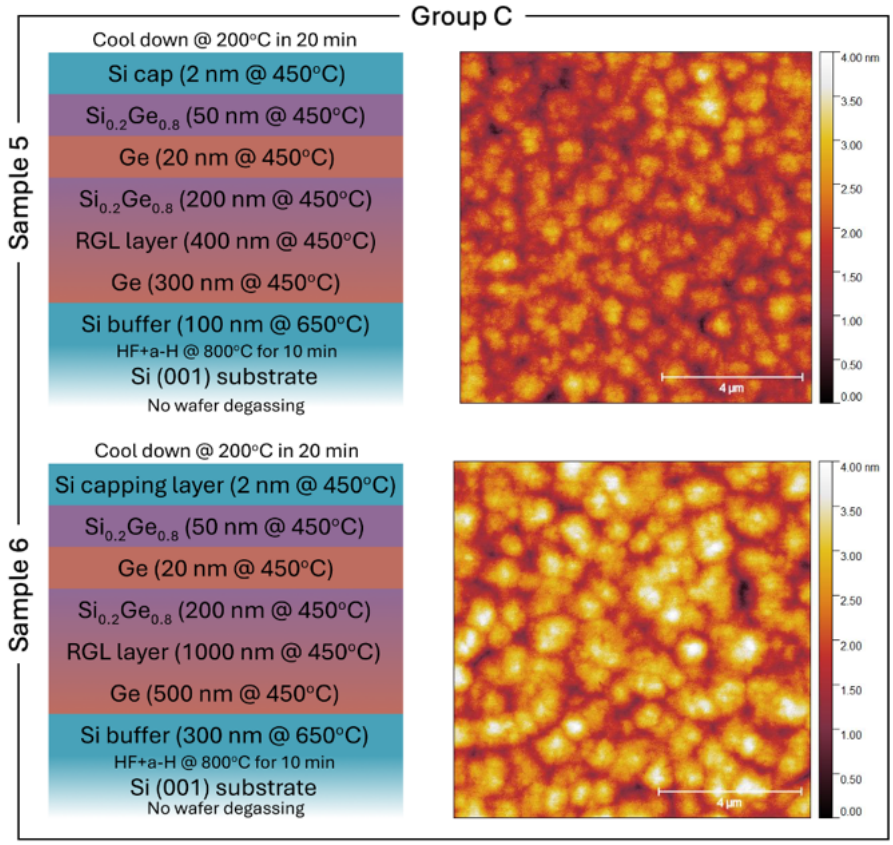


Figure 3.8: Schematics and AFM surface morphology of Group C heterostructures. Scale bars are 4µm and height color bar has units of nm.

This project was terminated abruptly once a maintenance of the MBE was required.

The collaboration between the university and Microsoft was terminated and we lost access to the lab.

3.3 STRUCTURAL CHARACTERISATION

With the heterostructures fully developed, the focus shifts to the structural analysis of their morphological characteristics. To ensure that all readers, regardless of their background, can fully comprehend the discussion, each characterization method begins with a brief description of the principles and the involved instrumentation. Once all the elements necessary to understand the data are demonstrated, the results are presented and analysed.

3.3.1 *Transmission electron microscopy*

The two final heterostructures (**Sample 5** and **Sample 6**) were sent for TEM analysis at *ICN2*. The investigation primarily aimed to assess the interface roughness of the strained Ge quantum wells. Additionally, the comparison between the two wafers would hint at the appropriate buffer layer thickness and the potential advantages in terms of strain relaxation. However, during the TEM analysis, executive decisions terminated the project and there was no possibility to implement the feedback from the structural characterization.

In general terms, TEM provides the most insight into the crystal structure of a periodic material. It is usually combined with a technique called focused ion beam (FIB) that etches the substrate in a trench, leaving a thin slice of material exposed. This lamella can then be manipulated and transferred on a TEM membrane grid for further analysis. It is common for the lamellas to have a tapered profile because of the etching profile of the ion bean. This means that chemical composition can be misleading, and geometric phase analysis (GPA) is required to extrapolate valuable parameters such as strain and composition accurately. In contrast to the SEM techniques, TEM uses the tunnelling effect of the electrons to obtain the signal from the investigated material. Electrons are accelerated via a high-voltage source and are focused via objective lenses to be transmitted through the material on a detector. The data from a high-resolution TEM image are usually bright and shadowed regions, depending on whether the electrons can be transmitted or blocked through the crystal, respectively. Fast Fourier Transform is commonly used to identify the frequency peaks that will give information about the crystallography of the transmitted lattice plane. With this information, we can access mismatch and strain.

In the analysis of the two heterostructures of **Sample 5** and **Sample 6**, we identify treading dislocations arising from the mismatch of the lowest buffer layers. In Figure 3.9, real space rotation and dilation maps at the interface of Si and Ge indicate the source of dislocations in the heterostructure. The high mismatch between two elements (4.23%) makes it a highly strained interface. This strain is mostly plastic,

reflected by the misfit dislocations created by the (-220) vertical planes. The elastic strain is only a compressive -0.263% in this family of planes. This high mismatch density generates a large amount of defects. Some are visible close to the interface. Twin planes along {-111} and stacking faults are indicated by the coloured lines.

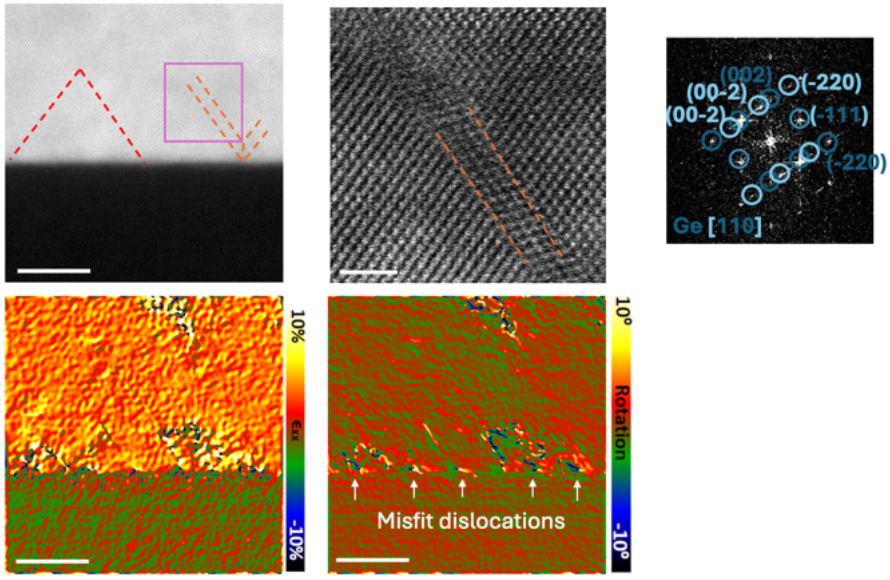


Figure 3.9: TEM analysis of the interface between Si and Ge buffer layers. Misfit dislocations originate from the interface.

From the interface and already in the graded layer, we observe some vertical contrast shifts, which are attributed to edge threading dislocations. These are typical in highly strained Ge systems, edge dislocations in the (001) planes whose dislocation line is perpendicular to this plane and goes through the [001], appearing as a vertical line when, as in this case, the zone axis is [110]. It should be noted the possibility of some of these lines being screw dislocations that are also typical in highly strained Ge. However, to verify their existence, steps in the upper interface should be visible, but there is no evidence in the analysed lamella.

The thick buffer layers contribute to the elimination of the threading dislocations. Here, The comparison of **Sample 5** and **Sample 6** suggests that even thicker layers ($> 2\mu m$) may contribute to defect-free active regions. Compositional analysis verifies the linearity through the RLG, meeting the expectations. Moreover, the dislocation density is decreased close to the active region, producing sharp interfaces and dislocation-free areas as the ones presented in Figure 3.10. The epitaxy of the sGe with the spacer layers is perfect, in agreement with the low mismatch.

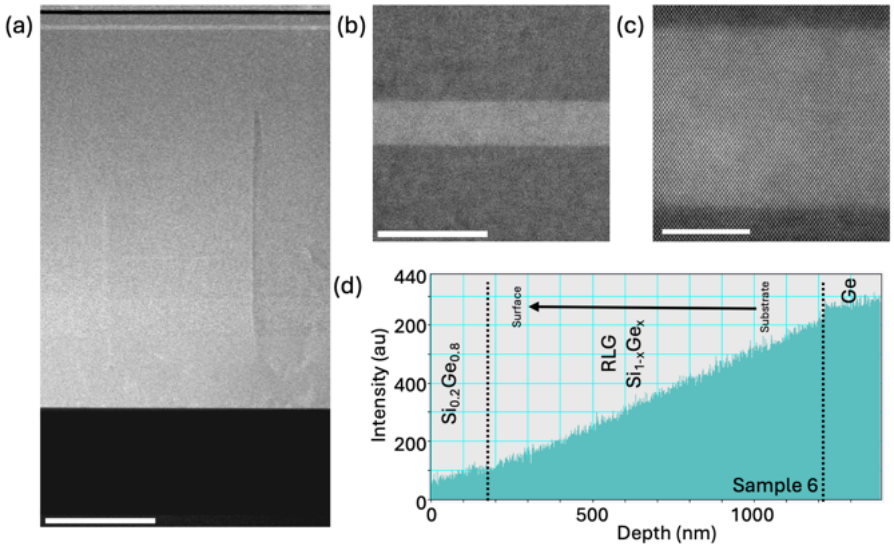


Figure 3.10: HR-TEM of **Sample 6**. Sharp interfaces at the sGe quantum well are visible with absence of structural defects close to the quantum well. Scale bars correspond to 500, 50, and 10 nm (a-c).

3.3.2 *X-ray diffraction reciprocal space mapping*

XRD is an experimental technique for observing diffraction patterns by irradiating materials with X-rays. In its core theory, XRD is based on Bragg's reflections. Specifically for crystals, diffraction patterns can be predicted using calculations based on *dynamical diffraction theory*. This analysis can be combined with the experimental data to identify deviations from the ideal crystals. Typically, modelling epilayers is a rigorous process, with precision limited to a few monolayers. Increasing the system's complexity to include multiple buffer layers usually necessitates approximations and raises computational complexity. Therefore, when performing X-ray diffraction here, the focus is primarily on the qualitative effects of strain and dislocations that arise from controlling layer thickness and composition.

Describing the formalism of XRD in detail is beyond the scope of this thesis. However, data can be non-intuitive, and researchers from different fields tend to skim or disregard them. A more thorough introduction can be found in Reference [31]. Even if readers prefer to skip the detailed analysis, the discussion here introduces the reciprocal space maps based on the diffraction vector, which should be sufficient to comprehend the experimental data.

Starting from the incident and diffracted beam similar to the schematic of Figure 3.11, the difference of the two vectors $\overrightarrow{k} = \overrightarrow{k_s} - \overrightarrow{k_i}$ is called the diffraction vector, where the indices s and i stand for *incident* and *scattered*. When the two beams are coordinated, such as lattice planes give the maximum signal, then a peak is identified in the spectrum. These identified peaks are related to a particular lattice direction and

crystallography of the diffracted material. The control over the two vectors produces the $\omega/2\theta$ plot or the **rocking curve**. Except for the angular relation of the two detectors on the xz-plane, an additional azimuthal degree of freedom contributes to the complete representation of the diffraction intensities into a **2D map** representation. With these combinations, we can reconstruct the reciprocal space via the Ewald sphere construction, similar to what is described in Figure 3.11. Due to time constrain, only a small portion of the RSM is usually scanned in high resolution. Data from XRD can be non-intuitive, especially for multi-layer complicated growths. For these cases, layers are presented in a more qualitative format, resembling more mass spectroscopy data rather than a real space TEM image. The intensity peaks have little evidence with respect to their depth in the heterostructure, and they are all projected in terms of lattice constant and intensity. The most interesting part of RSM comes from asymmetrical detection angles. Strained layers have a different lattice constant than the relaxed but the same elemental composition. The strained peak will not intercept the (0,0) reciprocal coordinates and will be an outlier from the relaxation line of the substrate. If this peak falls below the relaxation axis, then it is compressively strained, and if it lies above, then it is tensilely strained. In Figure 3.11, a graphical representation of a reciprocal space mapping in Ge/SiGe is given for better visualisation.

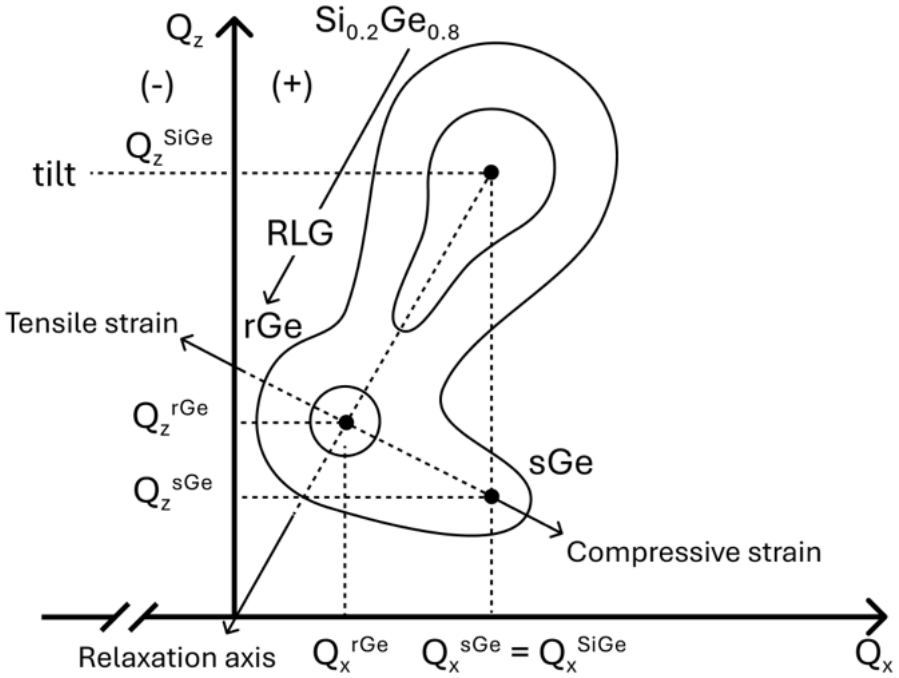


Figure 3.11: Schematic describing the elements needed for XRD RSM technique. The investigated sample is a sGe quantum well with an RLG buffer layer. The scan is taken at an asymmetrical direction. A peak below the relaxation line indicates compressive strain, whereas above tensile strain.

The reciprocal space maps are obtained by a Rigaku SmartLab 1.2 kW XRD high-resolution θ/θ closed loop goniometer drive system with a Cu Kα1 source. The typical tube voltage is 40-45 kV with a current of approximately 30 mA. A 2-bounce Ge(220) monochromator and a parallel beam split are necessary to achieve the desired angular resolution. The increased resolution reduces the intensity of the incident ray. As a result, the diffracted signal is also weak. The low number of counts increases dramatically the acquisition time. Using a sample size above 1×1 cm^2 or employing larger length-limiting slits are usually sufficient techniques to counteract the low-intensity input in the detector. The incident plane of the X-rays is the xz, and the origin of the reciprocal coordinates Q_x and Q_z lies in the substrate's reciprocal lattice point (RLP).

As described in the crystal growth methods of Chapter 3.2, four samples were assessed for further investigation (**Samples 3-6**). All four heterostructures were scanned in the symmetrical (004) direction. Due to limited laboratory time, only two of these samples (**Sample 4** and **Sample 6**) were analysed for the asymmetrical (224) axis to quantify strain. Furthermore, a pair of asymmetric Bragg reflections (113) and (-1-13) were employed in **Sample 6** to explore any possible deviation of the lattice planes from the main growth axis of (001). In the Table of Appendix A, the explored XRD RMS axes for each sample are listed.

Sample 4

Figure 3.12 demonstrates the RSM on (004) and (224) axes for **Sample 4**. On the other hand, Figure 3.13 presents the complete dataset for **Sample 6** for all four axes. The most prominent difference between sample groups **B** and **C** is the existence of the *RLG buffer layer*. In the RSM data, this is expressed by an extended ridge from the $Si_{0.2}Ge_{0.8}$ to the related Ge peak due to the existence of intermediate compositions in the heterostructure. In contrast to the contour shown in Figure 3.11, when the RLG is absent, the peaks of $Si_{0.2}Ge_{0.8}$ and rGe are well separated. This is well demonstrated in 3.12.

A technical detail that should be mentioned is the difference in intensity between each map. It should not be of great concern since the wafer pieces have non-standard sizes, leading to diffraction signals of different intensities. In particular, for relatively small samples, the diffracted signal is low, increasing the acquisition time.

The faint signal below the rGe peak indicates the sGe quantum well layer. However, quantifying the signal is challenging and the evidence of strain are presented in a qualitative format. Last, an overrelaxation of the $Si_{0.2}Ge_{0.8}$ buffer is visible in the asymmetrical RMS. This phenomenon is explained by the thermal expansion coefficient, leading to an additional tensile strain of the buffer. The sGe layer and the

$Si_{0.2}Ge_{0.8}$ buffer share the same horizontal reciprocal coordinate Q_x, indicating lattice matching and compressive strain.

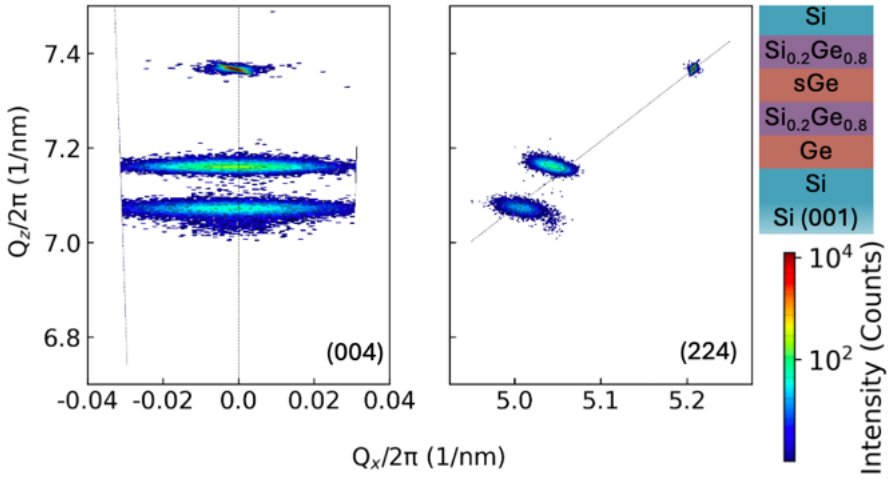


Figure 3.12: XRD RSM of the symmetrical (004) and asymmetrical (224) axes. Indices in each map indicate the used axis. The dotted lines indicate the relaxation axis.

Sample 6

Figure 3.13 demonstrates the RSM on (004), (224), (113) and (-1-13) axes. By measuring the values of the diffraction peaks at the grazing-incidence (Q_{x+}, Q_{z+}) and grazing-exit (Q_{x-}, Q_{z-}) geometries it is possible to evaluate the tilt angle as $\eta = \frac{\tau_+ + \tau_-}{2}$, where $\tau_\pm = \arctan(\frac{Q_{x\pm}}{Q_{z\pm}})$. The two last axes were used to explore the deviation of the lattice planes from the main growth axis of (001). Moreover, complementary analysis from the asymmetrical (224) direction gives more insights into the strain of the quantum well.

Focusing on the asymmetrical RSM, it is possible to calculate the structural characteristics of the investigated samples. First, the parallel and perpendicular lattice constants are calculated based on the crystallography of the sample and the (hkl) diffraction plane: $\alpha_\parallel = \frac{\sqrt{h^2+k^2}}{Q_x}$ and $\alpha_\perp = \frac{\sqrt{l^2}}{Q_z}$, respectively. It should be noted that the notation (x) and $(\parallel)$ and (z) and $(\perp)$ are used interchangeably. Following the natural misfit formula, the parallel and vertical mismatch can be calculated as $f_\parallel = \frac{\alpha_{\parallel,sGe} - \alpha_{\parallel,SiGe}}{\alpha_{\parallel,SiGe}}$ and $f_\perp = \frac{\alpha_{\perp,sGe} - \alpha_{\perp,SiGe}}{\alpha_{\perp,SiGe}}$, respectively. Lastly, the relaxation rate of the sGe layer can be calculated based on the formula $R = \frac{\alpha_{\parallel,sGe} - \alpha_{\parallel,SiGe}}{\alpha_{\parallel,rGe} - \alpha_{\parallel,SiGe}}$. In Table 3.1, the analysed lattice parameters for each case are given.

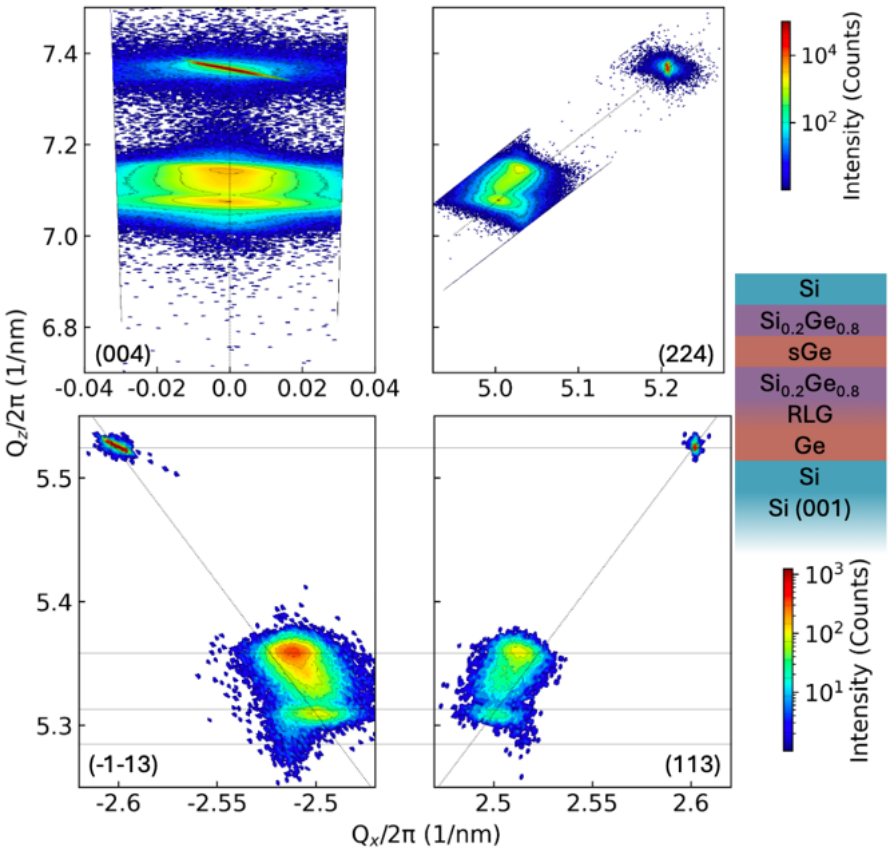


Figure 3.13: XRD RSM of the symmetrical (004) and asymmetrical (224), (113), and (-1-13) axes. Indices in each map indicate the used axis. For the case of (113), the symmetrical scan (-1-13) over Q_z was taken to compare the positioning of each plane. No tilt is observed. All peaks are positioned with equal values for Q_z as it is indicated by the horizontal annotated lines.

To conclude, both investigated structures indicate the existence of strain. The high uncertainties from the low signals of the investigated samples make it challenging to evaluate accurately the strain and mismatch in the layers.

3.3.3 *AFM analysis*

Focusing more on the surface of the wafers, AFM is employed to extract the topographical features of the wafers. This method utilises a sharp tip on a cantilever together with aligned laser beams and a quadrant photodetector. The sample is placed on a motorised stage and scans are obtained in a raster pattern. A driving force is applied to the cantilever, and the tip interacts with the morphological features of the surface. The ringing signal from the surface is separated from the driving force allowing sub-nanometer topographical precision. We use a *Bruker Dimension Icon AFM* in *ScanAsyst* mode, and areas from

(hkl)	Layer	$\alpha_{\perp}$	$\alpha_{\parallel}$	$f_{\perp}$	$f_{\parallel}$	R
(224)	SiGe	0.5598	0.5625	0.0103	-0.0002	-3.5766
	sGe	0.5655	0.5624			
	rGe	0.5652	0.5651			
(113)	SiGe	0.5598	0.5626	0.0104	0.0000	0.6278
	sGe	0.5656	0.5626			
	rGe	0.5651	0.5654			
(-1-13)	SiGe	0.5650	-0.5658	0.0116	-0.0008	-19.1174
	sGe	0.5663	-0.5630			
	rGe	0.5598	-0.5634			

Table 3.1: Structural quantitative analysis for **Sample 6**. The parallel and vertical misfit, as well as the strain relaxation, is calculated for (224), (113) and (-1-13) axes.

$20 \times 20\mu m^2$ down to $1 \times 1\mu m^2$ are scanned to characterise the surfaces and obtain local features.

In Figure 3.14 a, we plot the RMS values for the six heterostructures. The first two attempts to grow heterostructures had dramatically high surface roughness due to not optimised substrate preparation and growth temperature. The rest of the heterostructures, where Ge was grown at 450°C, had significantly low values and a minimum of 390 Å for **Sample 4**. This sample was chosen as the platform to grow epitaxially NbTiN for spin-photon experiments with superconducting resonators.

In Figure 3.14 b, all the available RMS surface roughness values in literature based on our current knowledge are compiled into a plot [23, 25, 32–41]. The heterostructures featuring the presented RMS values all contain a **shallow Ge quantum well**. The x-axis of the plot has no significant meaning as the data are plotted in descending order for visualisation purposes. The maximum RMS roughness is above 5 nm. The state-of-the-art samples for spin qubit experiments exhibit a roughness of around 2 nm. At the low end, we report flat surfaces of only 0.48 nm. We are aware that another Ge/SiGe heterostructure in the literature exhibits equally low RMS surface roughness but does not feature a shallow quantum well [42]. Rather, a deep one at approximately 500 nm below the surface gives the advantage of eliminating the dislocations in this thick layer. However, this architecture is detrimental to any spin-qubit applications. Lastly, annotations above each element indicate whether or not a crosshatch pattern is formed on the surface. Colour coding indicates the method employed for crystal growth.

One of the most intriguing features of these samples is the lack of a crosshatch pattern on the surface. As it is already described in Figure 2.3, the strain in the interface of the heterostructures forms a dislocation network with a 60° orientation resulting in regular surface

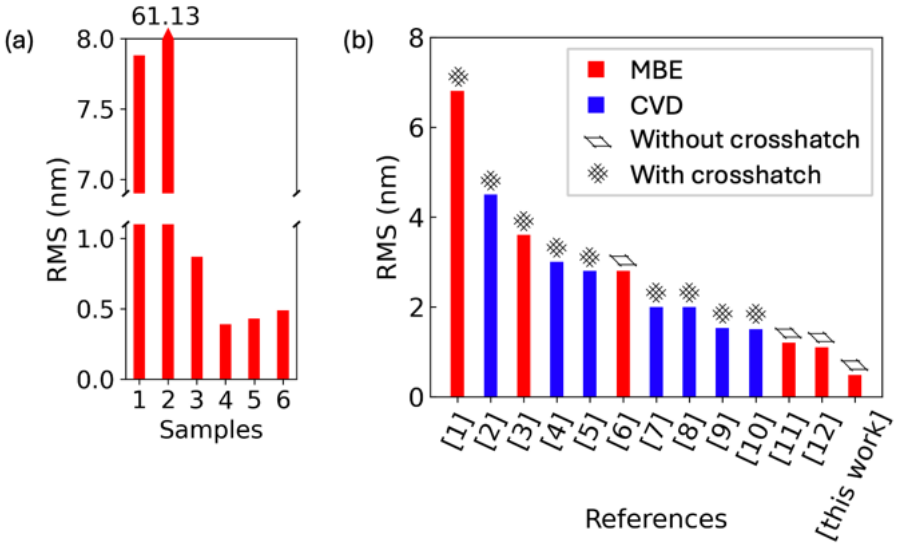


Figure 3.14: (a) RMS surface roughness obtained by AFM for all six grown heterostructures. (b) Literature review of RMS surface roughness. Samples are segregated based on growth technique and modulation doping. Annotations highlight the surface characteristics. In Appendix B, the matching of the reference numbering is given.

undulations. This study is not the first demonstration of the absence of the crosshatch pattern from the surface of Ge/SiGe heterostructures. Advancements in the early 2000s, particularly in MBE, have provided insights into low-temperature growth techniques that could eliminate this feature. Reference [40] investigated the transition via the employment of low-temperature buffer growth. Similar to the findings of our study, heteroepitaxial buffer layers with a high composition of Ge (>70%) at low temperatures (400°C) can produce crosshatch-free surfaces. However, when growing at 600°C, even for lower mismatch, the surfaces exhibit a crosshatch pattern. Surprisingly, although the majority of the state-of-the-art CVD heterostructures with over 1 million mobility employ low-temperature buffer growth techniques, the elimination of the crosshatch pattern remains unsolved. The element of low growth rate provided by MBE could be the missing link to produce crosshatch-free patterns. However, the limited growth rate in our study, as well as the termination of the project, did not make it possible to verify this hypothesis.

3.3.4 *Nomarski optical microscopy*

The low RMS surface roughness is a feature characteristic demanding further investigation. First and foremost, the scale of this effect needs to be identified. Optical microscopy on darkfield mode and the Differential Interference-Contrast (DIC) method are employed to identify large-scale features beyond the scan range of AFM.

On the one hand, darkfield optical microscopy utilises a darkfield condenser lens that blocks the light from the objective lens. In this way, only the scattered light from the surface of the sample is detected on the screen. Typically, the wafer surface is smooth, and only structures with morphological features are visible in darkfield. In practice, crosshatch patterns appear illuminated as a grid against the dark background of the wafer. On the other hand, DIC (or Nomarski) microscopy through the objective lens with optical filters that polarize the incoming light [43]. As a result, features are enhanced through the polarization of the reflected light. It should be noted that identifying surface features on low-contrast surfaces is very challenging due to the low polarisation. In Figure 3.15, schematics of brightfield, darkfield and DIC microscopy methods are presented, highlighting their key differences. Below each schematic, an acquired image of an identical quantum dot device is provided for clarity.

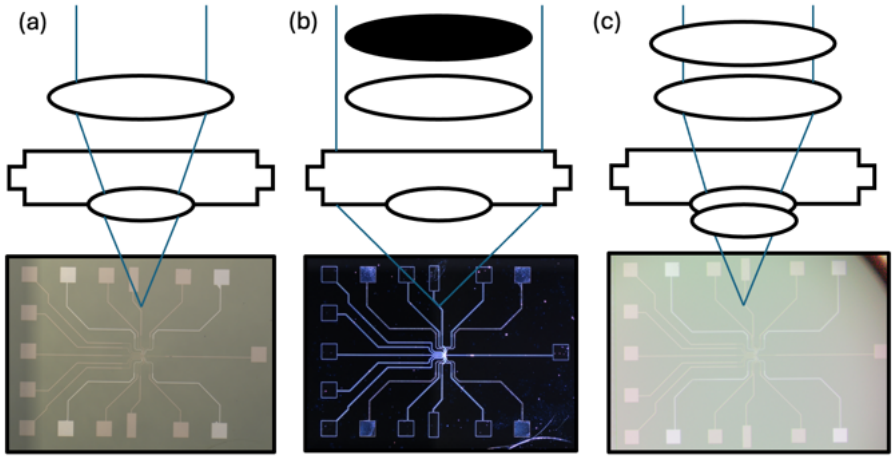


Figure 3.15: Review of optical imaging techniques: Comparison of an optical image obtained by (a) brightfield, (b) darkfield, (c) DIC optical microscopy methods. The subject examined in all cases is a quantum dot device for a more clear comparison of the optical result of each method.

In Figure 3.16, a compilation of DIC optical images indicates the structural characteristics of the samples. **Samples 3 - 6** all featured similar surface morphology and here **Sample 4** and **Sample 6** are presented. With permission of *Ferdinand Kuemmeth* an alternative wafer grown by CVD was used for comparison, to validate the results of the optical technique and also to identify the contrast between each sample. The foreign heterostructure is grown in the *Scappucci lab, TU Delft* and features a 20 nm thick sGe quantum well 50 nm below the surface. It is encapsulated in $Si_{0.2}Ge_{0.8}$ spacers, employing the RLG buffer layer technique and grown on a high resistivity Si(001) wafer [44]. The growth temperature remained at 400°C once the quantum well was grown and the exact thicknesses of the buffer layers are unknown. Periodic surface undulations are only visible on the foreign samples

in contrast to the samples presented in this thesis. This comparison validates the imaging technique for the two former surfaces and verifies the different surface features. The polarised light in each image had originally a different hue, but for comparison and simplicity, all three images were grayscaled.

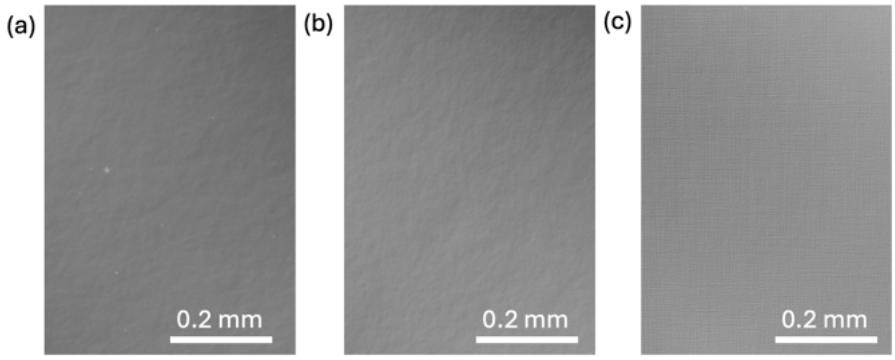


Figure 3.16: Grayscale DIC optical microscopy images of three Ge heterostructures. (a) **Sample 4** and (b) **Sample 6** do not exhibit a crosshatch pattern in contrast to (c) the heterostructure with ID **QT828** from **TU Delft**.

3.3.5 *Threading dislocation density*

Quantifying threading dislocation density is crucial to determine the quality of the wafer. This is usually achieved by etching the heterostructure and counting the dislocation pits either with AFM or optically. There are different approaches for etching the heterostructures, either with wet chemical etching [45] or chemical vapour etching [23]. Due to the lack of compatibility with cleanroom regulations and in combination with the limited time, the characterisation of the pit density was solely performed by AFM on the buffer samples. The main source of dislocations in the heterostructures lies in the Si-Ge interface at the lower buffers. This has been already verified by the TEM analysis. Thus, it is only reasonable to focus on the sample that contains only the Ge buffer layer. AFM on the surface of the Ge layer indicates a TDD of $2.2 \cdot 10^5 \text{cm}^{-2}$ for the wafer processed by atomic hydrogen.

Following up with Figure 3.14, almost half of the studies reporting the RMS surface roughness also provide the TDD. In Figure 3.17 b, the two values are correlated, indicating that a low TDD is accompanied by a low RMS surface roughness. Moreover, the results collectively are in agreement with the experimental study from Reference [40] shown in 3.17 c. In this plot, the RMS roughness follows the same trend as the TDD. In particular, the low-temperature growth (right data points) has the lowest surface roughness with a crosshatch-free surface. In contrast, high growth temperatures (left data points) exhibit higher surface roughness with a crosshatch pattern visible on the surface.

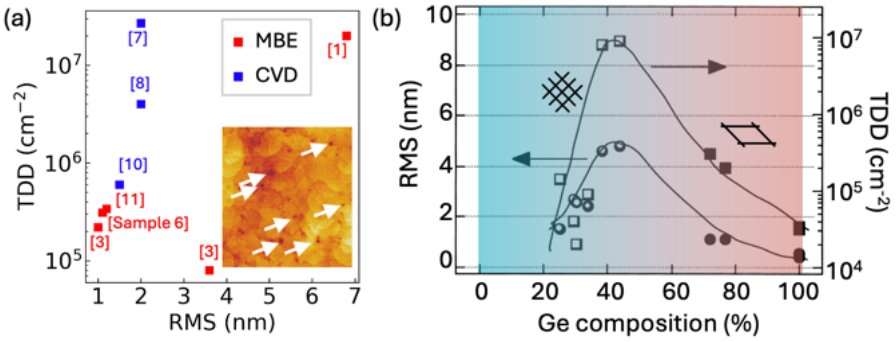


Figure 3.17: (a) Evolution of TDD as a function of RMS in literature. The inset corresponds to an AFM image used to count the amount of dislocations. Some dislocation pits are annotated by white arrows. The literature data points correspond to the same table of Appendix B similarly to the AFM analysis. (b) Annotated plot from Reference [40] indicating RMS, TDD and crosshatch formation as a function of alloy composition and growth temperature of $Si_{1-x}Ge_x$ on Si (001).

As a next step to the characterisation of these samples, the author suggests Schimel etching for different durations to identify the evolution of TDD inside the heterostructure. Possibly, this can give an indication regarding the future buffer layer thicknesses that one should aim to achieve dislocation-free samples at the active quantum well region.

3.4 PERSPECTIVES

At the beginning of this project, the objective was to achieve record mobility heterostructures without having a clear purpose and application in mind. Of course, having an expensive ultra-clean chamber funded by corporate collaborative projects requires the validation of the investment. Replicating figures of merit comparable to the state-of-the-art samples is a reasonable approach, even though it hinders academic creativity and freedom.

Moving on and removing the corporate myopic lenses, the application of spin qubits focuses on large-range flat surfaces and interfaces and a low percolation threshold at the low charge carrier density regime. Thus, the careful assessment of the structural characteristics of the heterostructures is necessary to develop state-of-the-art spin qubit samples.

Moreover, the flat surfaces directed the research to a very fascinating but also challenging path. The deposition of NbTiN, conceptualized by **Anasua Chatterjee**, brought fresh insights into potential applications. **Martin Bjergfeld** optimised and deposited the film at the University of Copenhagen. **Bertram Brovang** and **Miguel Carrera Belo** performed the fabrication and simulations on the hybrid structure. The author expresses his deep gratitude for their willingness to collaborate and their ambition for the project. The experiments are currently ongoing and only a small portion will be discussed in this thesis.

3.4.1 *Ex-situ deposition of niobium-titanium nitride*

The deposition of a superconductor on semiconducting heterostructures opens new pathways to quantum information [46]. The initial attempts to couple GaAs quantum dots with superconductors were challenging due to the piezoelectricity of III/V materials [47]. On the other hand, Si and Ge do not suffer from this effect, but the overall complexity of the platform is more challenging.

Regarding the MBE system and the RF sputtering of NbTiN, the author was not able to attend the crystal growth due to limited access to the MBE facility. The chamber is dedicated to thin film deposition with electron beam evaporators (Al, Sn, Pb) and RF sputtering (NbTiN, MgB_2). The system has a base pressure of approximately $5 \cdot 10^{-10}$mbar. For the sputtering of NbTiN, an AC source generates the plasma into the chamber. Nb and Ti targets together with a constant flow of N_2 and Ar control the stoichiometry of the deposited film. During the process, the chamber pressure is at the range of 10^{-3}mbar.

Before loading, wet chemical etching with HF of 5% concentration for 1 min, followed by MQ passivation, was performed on the wet chemical bench next to the load lock of the MBE. Standard cleaning

procedures were followed for the preparation of the wafer, such as initial degassing of the trolley and surface thermal treatment. the former was baked at 200°C for 2 hours, and the latter was outgassed at 300°C for 5 hours. During growth, the stage and the chamber were not cooled or warmed (operation at room temperature), and the chamber pressure was at $1.89 \cdot 10^{-3}$mbar. The gas flow of N_2/Ar were set at 8/16 sccm for each case, and the source power was set at 200 W. The duration of the deposition was fixed at 20 mins.

The demonstrated deposition on the heterostructure came after an optimisation series both on stoichiometry and film thickness. These growths were performed on high resistivity Si (001) and the film thickness was characterised by ellipsometry. Once the film thickness was reproducible at 5 nm, the deposition under the same conditions on **Sample 3** was performed. The Si substrate with the same parameters is presented in Table 3.2. Four-probe measurements on the surface of the wafer were employed to calculate the film resistance. By assuming the critical temperature of NbTiN film at 7 K, it was possible to extrapolate the kinetic inductance of the film.

Sample ID	Layer stack	Resistance	Kinetic inductance
I	Si + 4.84 nm	259Ω	232.19pH/□
II	**Sample 3** + 4.84 nm	71.76Ω	61.22pH/□

Table 3.2: Resistance and kinetic inductance of the sputtered NbTiN films on Si and an on **Sample 3**. The resistance was calculated via a four-probe measurement and the kinetic inductance was simulated.

From electrical experiments performed in Chapter 7.2.1, with emphasis on Figure 7.8, it is very likely that the quality of the wafers was compromised. First, the high-quality native oxide was decomposed from the chemical etching with HF, transforming the wafer from accumulation to depletion mode for the device fabrication. Second, even though the thermal budget of 300°C is lower than the growth temperature of 450°C, an intermixing of the layers might be possible, transforming the sharp interfaces to more gradient compositional transitions. This may contribute to multiple scattering mechanisms, such as scattering from the interface roughness and alloy impurities. However, diffusion has to be verified by TEM. Also, the detrimental effects on the electronic properties need to be identified after device fabrication. It should be mentioned that the deposition of an Al film on top of the heterostructure was already queued as a growth, but the project terminated prematurely.

3.4.2 *Suggestions*

Closing the crystal growth investigation, future perspectives for the curious experimentalist are suggested. These proposed directions aim to optimise the performance of the current heterostructures and also identify new application domains. First, just by focusing on the already utilised approaches, further optimisation will be discussed. Further, the application to novel devices with the introduction of alternative terminating layers will be reviewed. Last, the incorporation of non-Si/Ge materials is presented.

Substrates, buffer layers and isotopes

Since the growth focus of this study is sGe quantum well it would be more beneficial to mitigate from the Si(001) to Ge(001) substrates. Even though it is less standard for industrial applications, the overall reduction of strain due to the lattice mismatch and also the different thermal coefficients is more beneficial and should definitely be on the list of every experimentalist. Similar to Si, Ge substrates are expected to freeze out at lower temperatures imposing no substrate leakage issues. The benefit of such substrates has already been demonstrated by Stehouwer et al. [23]. The application in MBE-grown heterostructures may result in excellent morphological properties.

Following the insightful feedback from the TEM analysis and without major adaptation of the last grown heterostructure (**Sample 6**), it is clear that thicker buffer layers will be beneficial for enhancing the crystallinity and reducing the dislocation density. Moreover, it would be beneficial to study the crystallinity of Ge and Si layers as a function of temperature and identify the lowest boundary. However, for such a study, the use of the pyrometer is essential to report accurate data.

Last, regarding the material sources, it is important to mention the availability of isotopically purified material sources for both Si [13] and Ge [48, 49]. However, even though such materials are, in principle, obtainable for the laboratories, their access is exclusive and is dominated by political decisions. This only creates barriers to science and the development of society in general. Laboratories that were able to resource such materials have reported significant improvement of coherence times in their qubits [50–52].

Superlattices and non-linear graded buffer layers

The buffer layer growths are a common technique to eliminate the dislocation density. The misfit dislocations arise at the epitaxial interface between Si and Ge buffers. The reduction of the density is achieved by the growth of thick buffer layers. Eliminating the remaining dislocations can be achieved by the growth of superlattices. For

example, between the Ge buffer and the RLG layer, a superlattice of $Ge/Si_{0.2}Ge_{0.8}$ can be utilised as a dislocation filter and achieve a dislocation-free VS of $Si_{0.2}Ge_{0.8}$. Then, the sGe quantum well is expected to have no defects. When such a superlattice grows over a dislocated layer, the strain at the superlattice interfaces effectively traps propagating dislocations [53].

Moreover, adopting a non-linear buffer layer presents a promising avenue for driving the dislocations away from the growth axis. This strategy capitalizes both the critical thickness dependence on concentration and the TTD profile. Firstly, the critical thickness dependence on concentration implies that the point at which dislocations begin to form can be altered. By strategically adjusting the composition profile, it is possible to delay the onset of dislocation formation. Secondly, Choi et al. [17] investigated linear, convex, and concave graded profiles and identified enhancement of optical and electron transport properties in the case of the convex. Furthermore, the non-linear nature of the buffer layer profile allows for precise control over the distribution of strain and defect interactions within the epitaxial structure. Overall, the implementation of a non-linear buffer layer represents a sophisticated approach to optimizing the growth process in heterostructures. Through careful design and engineering, this technique has the potential to significantly improve the quality and performance of epitaxially grown materials.

Terminating oxides and hybrid materials

Similar to the high-quality SiO_2 capping layer by MBE, terminating the growth with a germanium capping layer could be useful to reduce excess strain and the difference in thermal expansion coefficients. Studies have focused more on the formation of a GeO_2 dielectric and its application in MOSFET devices [54, 55]. In the book *Molecular Beam Epitaxy: From Research to Mass Production* [56], Maksym Myronov suggests the implementation of GeO_2 as a trivial approach for terminating the surface of the heterostructures. However, more than five years later the reported samples still are terminated with Si.

To expand this approach to a more device-related application, it would be beneficial to perform dedicated oxidation techniques to directly deposit the first dielectric layer without breaking the vacuum. Then, local etching for the ohmics can be performed similarly to the standard techniques for metal deposition. Then, the first gate layer can be deposited without the need for any additional dielectric. Probably, since the surface of the wafer is intact, the electronic performance of the devices related to noise will be significantly low. Of course, more advanced approaches may require additional chambers and tools connected in a vacuum, which can be costly or incompatible with the existing system.

Expanding the discussion from Si and Ge terminating materials to elements with superconducting properties, it is possible to realise hybrid structures. Semiconducting-superconducting devices showing hard superconducting gap [57], proximitised quantum dots [58], gate-tunable superconducting qubits (gatemons) [59], and superconducting resonators coupled to quantum dots (spin-photon) [46] are the most related topics that can be realised in these hybrid systems. While this work demonstrates the ex-situ deposition of NbTiN sputtering on the heterostructures, the original plan of the study was growing Al in-situ. The in-situ growth of Al can also be combined with the controlled oxidation in a layer-by-layer format to realise high-quality dielectrics.

Alloys and dopants

Sn is an essential element in the semiconductor industry. It has two stable phases, α and β that can be controlled by lattice engineering [60]. This selectivity determines the electronic properties of the film. Moreover, GeSn alloys are low-bandgap semiconductors suitable for photonic and optoelectronic applications [61]. Electronic properties of sGe in ternary (Si)GeSn heterostructures [62] and the optimisation of the epitaxy of $Ge_{1-x}Sn_x$ [63] have been studied, revealing their potential in the field.

Delta doping is a typical approach when aiming for high-mobility electronics. This can be realised in a single layer either above, below, or bilaterally of the quantum well. Ionised impurities such as dopants limit mobility, and the doping layer is located away from the active region. However, *scattering from impurities* limits the electronic quality of the system. As it will be reviewed later in Chapter 7.1, the state-of-the-art sGe samples demonstrate excellent electronic properties without the requirement of doping. High doping densities may result in parallel conducting channels, excitation of additional subbands and, of course, scattering from impurities. Alternative techniques have been proposed to reduce the detrimental effects of doping and enhance the electronic properties. However, the majority of these proposals are focused on the III/V platforms [64, 65]. Examples of high mobility techniques in III/V heterostructures may also be realised in group IV grown samples. An example that one could try is the doping-well structure from Loren Pfeiffer's research group [66, 67]. For example, the B delta doping may be more efficient by using flanks with different elemental compositions trapping the impurities more efficiently.

Part II

DEVICE FABRICATION

4

TOOLS

The purpose of this chapter is to inform the reader about the fabrication methods of quantum devices on planar heterostructures. For every technique, a brief overview of the associated tool will be given. More importantly, we focus on the rationale behind the choice of each tool. During fabrication, we encountered and systematically addressed multiple failure modes. For this reason, we highlight suggestions to eliminate failure modes and produce successful devices. The chapter covers CAD design, lithography techniques with optimization of an electron beam lithography recipe, metal and dielectric thin film deposition, etching methods, wirebonding, and characterization of the final device.

Important keywords that the reader should distinguish are listed below:
Device or **quantum device**: A quantum dot or Hall bar that we aim to probe electrically and conduct relevant experiments on.
Chip is a piece from the diced wafer that has undergone the complete fabrication process.
Dummy chip is a piece of substrate similar to the one of the heterostructure but without any epilayer*. It is used either for dose testing or for evaluating the film thickness.
Bondpads: Large metallic areas on the chip to place the wirebond and electrically connect the chip to the measurement setup.
The term *sample* will be explicitly avoided in this chapter to prevent confusion.

It must be stressed that device fabrication with a feature size of 50 nm in an academic cleanroom can be very challenging. Multiple users specialise in different material platforms and regularly try new non-standardised recipes. The experimentalist must always have a clear mind when in the cleanroom, review all the steps before running a recipe, and have enough courage to accept unsuccessful outcomes.

* For example, if one uses Si/SiGe on Si(001), then the dummy chips are Si(001) pieces. Similarly, if one uses InAs on a GaAs substrate, then the dummies should be GaAs. In less conventional cases, it is common to use as dummies old and discarded equivalent heterostructures.

4.1 DESIGN

There are numerous software options available for designing quantum devices, each offering unique strengths and particular suitability. It should be emphasised that no single software is universally suited for the design of quantum devices. Even within the same research groups, it is common for experimentalists to use different software that meets their specific needs and personal preferences. Table 4.1 lists the most commonly used CAD software within the *Center for Quantum Devices*. By interviewing the users, the main strengths and weaknesses were identified and presented here.

Software	Pros	Cons	Cost
AutoCAD	Wide range of applications	Not compatible with `.GDS` files	Licensed: 2342€/yr
KLayout	Can add and align optical & SEM images: great for nanowire fabrication	Not user friendly	Open source
CleWin	Can add scripts	Not compatible with MAC.	Licensed: 1295€
PHIDL	Easy to parameterise	Can take time to set up the first design	Open source

Table 4.1: CAD software guide listing advantages, limitations, and cost to help users identify the most suitable software for their specific design requirements.

The single requirement for design software is the compatibility of the exported file format. All recommended software meet this criterion. As discussed in the introduction to lithography, following the design preparation, electron beam doses are assigned to the exposed features using another software called *BEAMER*. The accepted file formats include `.GDS`, `.DXF`, and `.CIFF`.

To provide more insights into the software choices of the users, it is necessary to step outside the scope of this thesis. Unlike the 2D carrier systems, where the device design can be well-defined, nanowires deposited by a micromanipulator needle or even by dry deposition are scattered across the chip. To identify the nanowires' precise positions, local markers combined with imaging (optical, SEM or AFM) are required. This necessity becomes more critical when the nanowires contain local nanostructures such as shadow junctions [14]. Once these images are acquired, they can be imported into the KLayout software. Within KLayout, it is possible to align the markers of the images with the ones from the design for accurate representation. Then, it is possible to pattern the leads and gate electrodes according to the

experimental pursuits. Unless the design is well standardised, it is common that the probes are manually drawn.

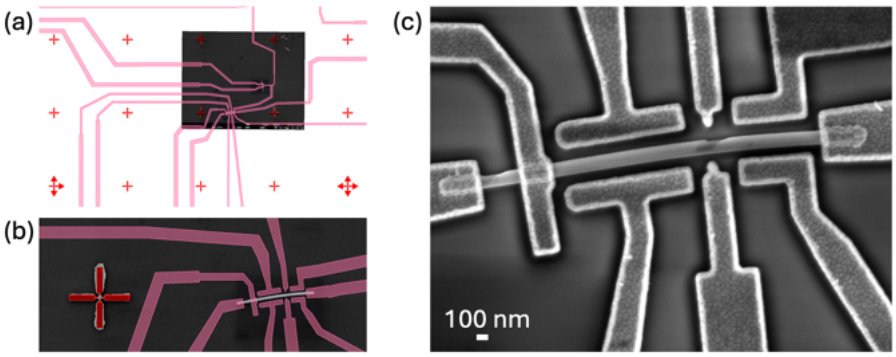


Figure 4.1: Designing a quantum device on a deposited nanowire: (a,b) An aligned SEM image of a nanowire with the design of the leads. KLayout is used for the design realisation. (c) An SEM image of the fabricated device.

Focusing more on the specifics of this thesis, most of the devices have been realised by a hybrid of parameterised and manual design. This gives significant advantages and exploits the maximum available chip surface. In Figure 4.2, we present the combination of the two methods and the final seamless outcome.

For the active device region, PHIDL was used to adjust the quantum dot array gate dimensions and CleWin was used for a standard layout of outer leads and the chip outline. On the one hand, PHIDL is a robust tool for altering gate lengths, the number and pitch of the dots, and the distances between sensor dots and gate arrays. This parametrised design is especially advantageous when scaling up. The exported designs are characterised by consistency and can be realised within seconds. In `github` of spin qubit members, codes for quantum dot arrays are provided. If the chip design is always under development or the chip size is inconsistent, then the configuration of the devices is not standard. In order to utilise the maximum area of the chip, a manual placement of the quantum devices is required. Thus, a hybrid approach worked best for this thesis.

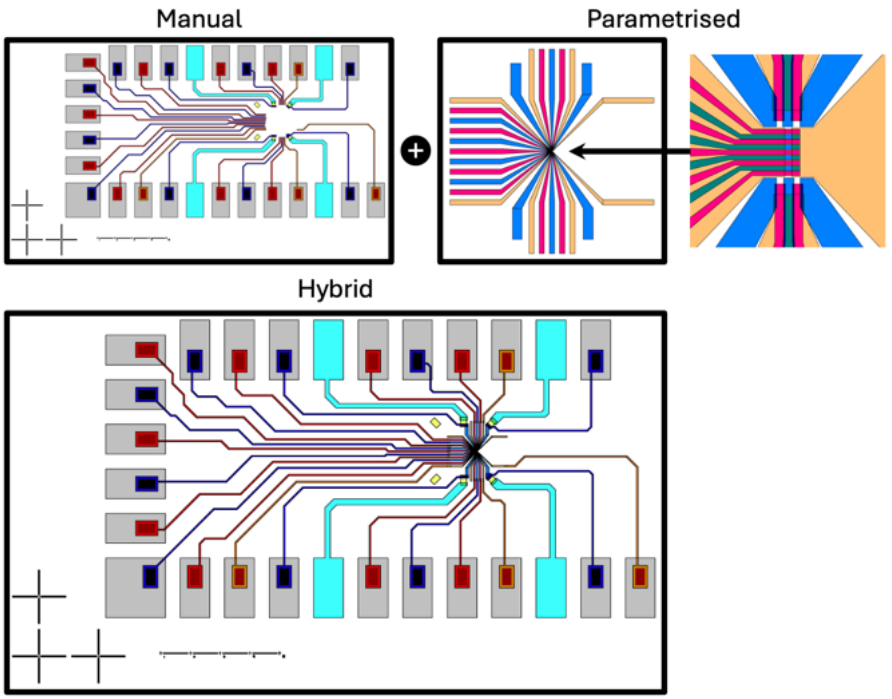


Figure 4.2: Designing a quantum device on a planar system: The hybrid design with the parameterised quantum dot dimensions by PHIDL and the manual outline by CleWin

4.2 ELECTRON BEAM LITHOGRAPHY

Electron beam lithography (EBL) is an essential nanofabrication technique. It enables the precise patterning of nanostructures to develop advanced quantum devices. Here, the review of the principles of EBL will be presented briefly. The main focus is on parameter optimisation with dose testing to reach maximum accuracy with respect to the tool and the materials employed. Additionally, a discussion on practical considerations navigates the reader through potential challenges and aims for successful fabrication.

The first step to preparing an EBL recipe is to identify the minimum feature sizes and the thickness of the deposited materials. In the case that the lithography is used for etching (wet or dry), then considerations regarding the durability of the resist polymer during etching should be taken. Also, it should be noted that if the minimum features and the distances between nanostructures are above a few microns, there is no reason to utilise this tool. It is expensive, time-consuming, and the parameter optimisation takes a few sessions that, in total, can last a week or more. In the case of large features, the use of optical lithography is highly recommended since it's much faster, and there is no need for recipe optimization. However, if the design contains both small and large features, then one should use only EBL and two different beam sizes to expose everything in one session.

Before any exposure, the design is processed for proximity correction to achieve homogeneous dose distribution in the exposed areas. In the Center for Quantum Devices, we widely use *BEAMER* [68]. *Beamfox Proximity* is an open-source alternative that has gained a reputation over the last few years [69]. For **dose testing**, one can use standard designs from *BEAMER*. However, especially for very fine features (below 80 nm), the best testing design is the one of the actual quantum device. In multi-layered quantum dot devices, a more thorough investigation of the accurate dose requires multiple dose tests on top of each gate layer resembling the actual device. In this case, the backscattered electrons from the metallic layers affect the energy distribution of the beam on the polymer.

Two resist types were used in this thesis, CSAR (poly(α-methylstyrene-co-chloromethacrylic acid methyl ester)) and PMMA (polymethyl methacrylate). After many processes, the author highly recommends the use of CSAR. According to the manufacturer, CSAR is more sensitive than PMMA resist and gives a stronger contrast. These product specifications provide a more time-efficient writing time on the EBL tool, and the nanostructures are more pronounced. Resists come in different concentrations to control the coating thickness. This information is usually enclosed in the manufacturer's brochure [70]. The rule of thumb is that the resist thickness should be 2-3 times higher than the metal deposition thickness. The spin coating can also modulate the thickness of the resist. We prefer to reach the saturation of the spin curve. The typical spinning time is 60 sec at 4000rpm. The baking time is also standard at the hotplate at 185°C for 2 mins.

An EBL tool has three primary tuning parameters: the beam current, the beam aperture, and the exposure time of a single beam spot. A matching between the beam spot size and the minimum design pixel is required. On the one hand, the beam spot value depends on the tool specifications. Figure 4.3 a shows the beam spot size as a function of the beam current and the aperture size. Moreover, the exposure is segmented into "write fields". When the stage aligns the centre of a write field with the centre of the beam, the design of that write field is exposed. Once the segment's exposure is complete, the beam gets blanked, and the stage moves to the next write field by aligning again the center of a write field with the center of the beam. There are predefined write field sizes for each tool. Each write field is segmented to correspond to a pixel value. For standard exposures, this pixel should be at least 10 times smaller than the minimal nanostructure feature and equal to the beam spot size.

By assigning a dose (in $\mu C/cm^2$), we effectively control the duration that the beam is unblanked to cause the scission of the polymer chains of the resist under the conditions we described above. Every resist has an operational dose range. This can be easily found either by the manufacturer or from previous fabrication attempts. A dose test aims

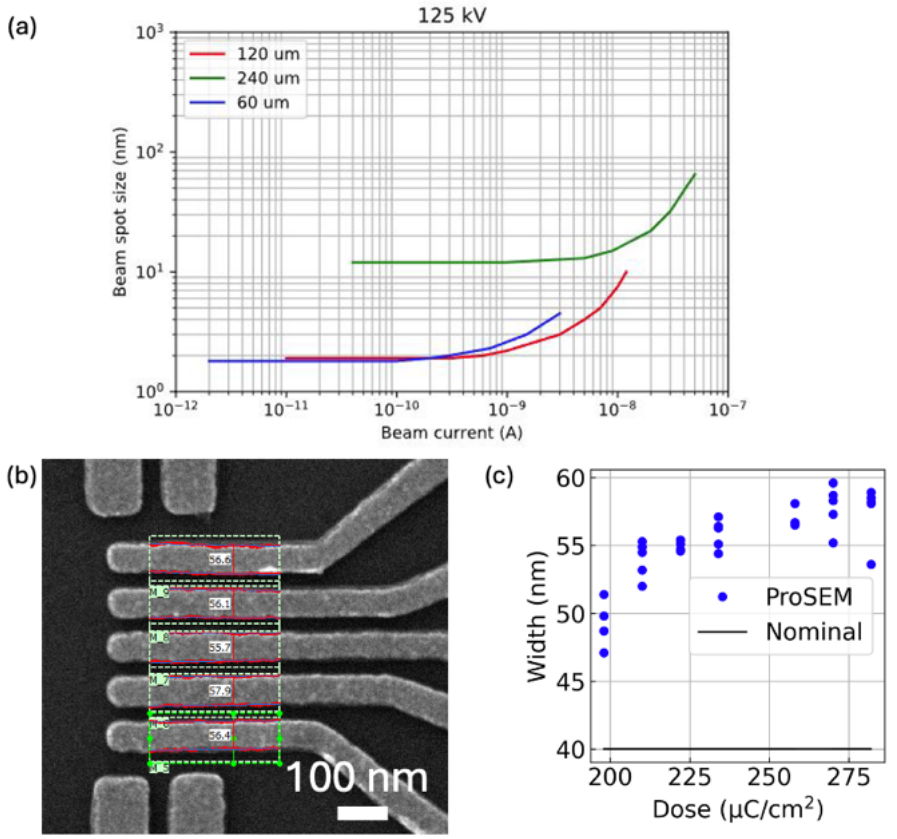


Figure 4.3: Guidelines to perform a does test with electron beam lithography: (a) *Elionix ELS-F125* 125 keV specifications. (b) Semi-automated dose testing analysis of a single SEM image by *ProSEM*. (c) Plotted dose testing results. The nominal feature size was 40 nm, but SEM analysis showed larger features.

to identify the precise dose that matches the sizes of the design and the fabricated nanostructure. Thus, devices in a suitable dose range are fabricated on a dummy chip. With the use of SEM and an image processing software, the fabricated nanostructures are characterised. *ProSEM* is a semi-automated software that can identify structures with similar morphological characteristics. Figure 4.3 b is a processed image where the width of the elongated probes is identified. In Figure 4.3 c the results of the dose test are plotted. The 40 nm features were scaled up by 25% to 50%. By repeating the process, one can identify the matching features. However, critical structures may still experience variations and inaccuracies. To maximise the success of the fabrication, it is highly recommended to include devices with small deviations from the nominal design.

4.3 THIN FILM DEPOSITION: METALS AND DIELECTRICS

Metal deposition

Metal deposition is a PVD process in a reduced-vacuum chamber with base pressure typically ranging at 10^{-8} bar. It is used to realise the metallic leads of the devices and has in-situ dry etching capabilities. The systems available in the cleanroom of University of Copenhagen come from AJA International †. In Figure 4.4, we characterised the grain size and roughness between Pd and Al gates. The grain size is comparable, as is the RMS roughness. However, following advancements in literature, we proceeded with the use of Pd for the gate layers [71]. For the ohmic layers, wet chemical etching with HF and Al is used. For the gate layers, a 5 nm Ti adhesion metal layer was used before the 20 nm of Pd. For the lift-off, we use 1,3-dioxolane for CSAR and Acetone (or NMP) for PMMA resist. A method to accelerate the lift-off process and avoid metal depositing at the edges of the chip is to cover the edges of the chip with Al foil prior to metal deposition. In this way, the perimeter of the chip will be metal-free, and the solution will dissolve effectively the resist.

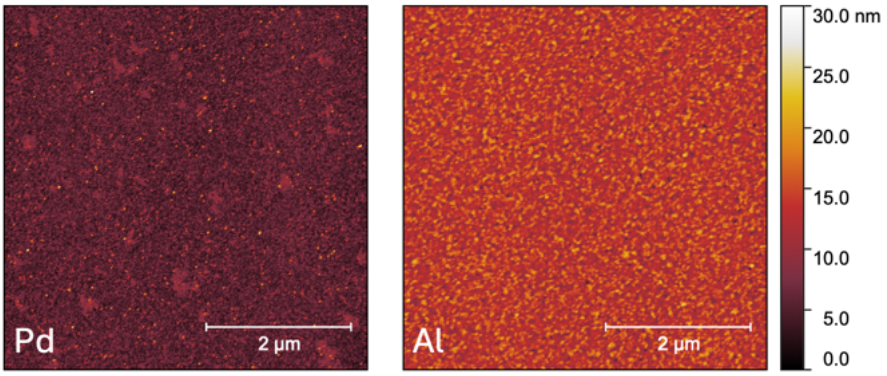


Figure 4.4: AFM images of deposited Pd (left) and Al (right) films.

Atomic layer deposition

Atomic layer deposition (ALD) is a film deposition technique closely resembling the CVD method. Here, the source gases are introduced into the main chamber through valve pulses and transferred via a carrier gas, such as N_2. The two gases (precursor and co-reactant H_2O) are alternately pulsed to perform self-terminating surface-based reactions. This process results in highly uniform and conformal thin films, ideal for coating complex surface features like thin nanowires, narrow trenches, or steep steps. Despite the continuous N_2 flow, the

† According to an AJA International representative, AJA is not an abbreviation, but it is inspired by the following album: https://open.spotify.com/album/1hOK2ey9W76x9GnftSRgrw?si=jhi_LI0XTMy9FrviUCj_-g

entire procedure takes place under vacuum below 1mbar. The typical temperature deposition spans from 90°C up to 300°C depending on the process requirements.

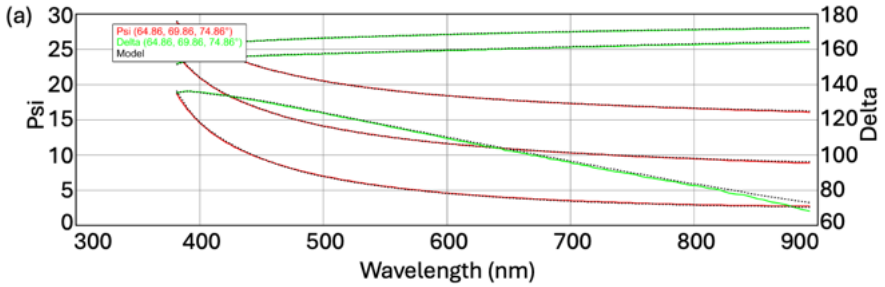
In this thesis, low-k dielectric Al_2O_3 is explicitly used. Even though the cleanroom has capabilities for high-k dielectrics such as HfO_2, it is not recommended for the electrical measurements of this study. The fabricated devices are multilayer gate-based, meaning that the topmost layers usually have a much lower effective electrical field than the bottom gate layers, which is detrimental to the properties of the devices.

In its core application, ALD produces reliably thin dielectric films with excellent electrical insulation between layers. However, contamination can compromise the quality and result in shorts between gates or a low breakdown voltage, usually referred to as *leakage*. In this thesis, we had to troubleshoot many fabricated chips and identify their failure mechanisms. Trying different ALD tools proved to be the most reliable approach to increase the success yield. Moreover, we attempted to develop methods to test the dielectric quality, but the correlation between the test structures and the measured quantum devices was low. Since the scope of this thesis was not to identify the failure mechanisms (this is a task delegated to the tool manager), we proceeded with avoiding the tools that repeatedly gave a low success rate.

Each ALD process was carried out in parallel with a dummy Si chip to evaluate the film thickness via ellipsometry. It is a non-destructive optical technique used to evaluate the thickness and the optical properties of thin films. By modelling the refractive indices of the films and analyzing the reflected light at multiple angles, it is possible to accurately calculate the film thickness. Of course, if the layer structure is complicated, the fitting may fail, but for single deposited samples like the ones used in this study, it is possible to get high precision.

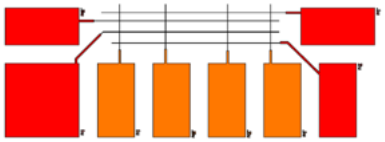
Additionally, metal-oxide-metal capacitor devices were fabricated to assess film quality. Figure 4.5 a, introduces the design of a single capacitor device. The device features multiple Pd-AlOx-Pd junctions arranged in a grid configuration, with all connections *floating*‡. This arrangement allows the addressability of each junction and the individual assessment of the breakdown voltage. Although the assessment indicated a low breakdown voltage, the quantum devices performed better than anticipated. This procedure failed to give a valid assessment of the quality of the dielectric film and did not give any insightful correlation. It is important to note that the overlapping area of the junctions in the capacitor devices was much larger compared to that in the quantum devices, which could explain the variation in performance.

‡ On the breakout box with coaxial BNC connectors, *float* means that the inner and outer core are separated, whereas *ground* means that the core and the shell are connected.



(b)

(c)



(d)

Length (µm)	0.1	0.5	1.0	2
0.1	-	-	0	6 V
0.2	5 V	7 V	-	6 V
0.5	-	-	0.2 V	-
1.0	-	-	0	-

Figure 4.5: (a) Fitting of the ellipsometry data from a dummy chip. (b) An illustration of a single metal-oxide-metal capacitor device. (c) The device grid of metal-oxide-metal capacitors. (d) The evaluation matrices of the breakdown voltage of the device grid.

Closing, an alternative technique to the Pd metal deposition and the Al_2O_3 ALD, is the self-oxidation of Al. In this process, the deposited Al gate layer is oxidised either in air or in a controlled oxygen environment. This has the advantage of the creation of a direct Al film on top of the device. Thus, there is no need to deposit an additional dielectric film to protect the gates from leakage. However, the larger reported Al grain size has moved the community away from this technique. A possible approach that might be interesting for a future study is the formation of a Ti:Pd:Al gate stack, followed by controllable oxidation. Concerns for the success of the process are the coverage of Al on Pd, the grain size of Al on Pd, and the dielectric quality of the oxidised Al.

4.4 ETCHING

The fabrication of quantum devices relies on etching techniques to manipulate the planar geometry of the substrate and ensure optimal performance of the device. Here, we present two fabrication routines, together with their objectives and optimisation of their recipe. Firstly, the **dry etch** approach of argon ions on Si in a vacuum chamber is presented, followed by the **wet etch** method of chemicals in the cleanroom for Al_2O_3 removal. In this study, both processes have low control over the crystallinity of the structure, which classifies them as anisotropic etching procedures.

Dry etching

On the one hand, to ensure electrical isolation between the devices and avoid mechanical deformation of the surface from wirebonding, as discussed later, we use dry etch at a depth below the quantum well, which is least (50+20)=70nm. The 2D carrier gas will be present only in the mesa area, and the rest of the substrate will be electrically isolated due to the freeze out of the substrate at low temperatures. To ensure the electrical connectivity of the gates at the mesa steep escarpment, we fabricate lithographically shorted wires, and we probe them to evaluate the electrical connectivity at the two ends. If the resistance is equal to the line resistance (short), then the climb is successful. In Figure 4.6, the design of the shorting wires is presented.

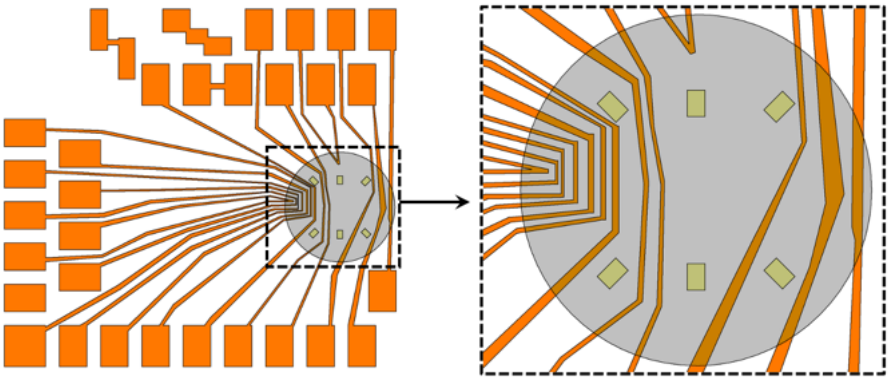


Figure 4.6: CAD design of mesa climbing test structures.

The dry etch is performed using an AJA tool with a technique called Kaufman milling. The substrate is lithographically patterned with only a few areas covered (these will host the 2D carrier gas), and Ar ions bombard the surface from a gun to the target where the substrate is mounted. Because of the heavy thermal load of the process, the photoresist is at high risk of hardening and being deposited permanently on the surface. This is why the procedure should be repeated in short

time intervals to achieve the desired etching time with a low thermal load.

To identify the etching rate, multiple small pieces of patterned Ge/SiGe heterostructure substrate were used, and the process was repeated for different etching durations. Once all the substrates were etched, the etching depth was assessed by a profilometer, which was plotted and fitted to calculate the etching rate. Since all the heterostructures had the same depth, we proceeded with using the 2×3 mins to ensure sufficient depth. The etch rate of the process was found to be 24.3nm/min. The sample stage was rotating at maximum speed with 45° angle with respect to the source; the Ar flow was set at 15 sccm with a chamber pressure of 1 mTorr and the beam voltage was set at 600V. For more information regarding the process, the complete recipe is detailed in Appendix C.

Kaufman milling is an add-on for one AJA tool (AJA1). However, depending on the preferences of the user, it might not be possible to perform in-situ etching prior to metal deposition. The second tool (AJA2) has an alternative etching method using an RF source and generates plasma in the chamber, similar to an inductively coupled plasma etching tool (ICP). Another set of etch tests were run but multiple parameters were varied at the same time. This made it difficult to explore a single parameter space and extrapolate conclusions for the etch rate. The results of the etching tests are presented in Table 4.2 and AFM analysis of the etching is presented in Figures 4.7 b and c. The AFM images of the RF etched surfaces are presented in Appendix B. No etching rate was possible to be identified due to the dual parameter variation (time and power).

RF Power	Duration	RMS etch	Etch depth
15 W	20 mins	nm	32.4 nm
25 W	10 mins	nm	37.3 nm
50 W	5 mins	nm	46.1 nm

Table 4.2: RF etching results from AJA2 system on **Sample 6**. The RF power and process duration control the etching depth. AFM analysis focuses on the etching depth and roughness of the etched area. In Appendix B, the AFM images of the RF etched surfaces are presented.

Wet etching

On the other hand, for the etching of Al_2O_3 ALD a wet etching process is required in the cleanroom. The objective of this task is to remove the oxide layer locally and ensure the DC electrical connectivity of different gate layers. The final goal of the process is also related to avoiding wirebonding substrate mechanical deformation. To begin with, we use MF32A and MQ passivation on a Si (001) wafer with the

same deposited oxide (both in thickness and quality). With the use of ellipsometry, the thickness of the oxide can be assessed in regular time intervals. From Figure 4.5 c, it is clear that in low oxide thicknesses, the ellipsometry fails, and we cannot maintain an accurate evaluation. However, the etching rate can be calculated using the rest of the points. This gives an etching rate of approximately 2nm/min.

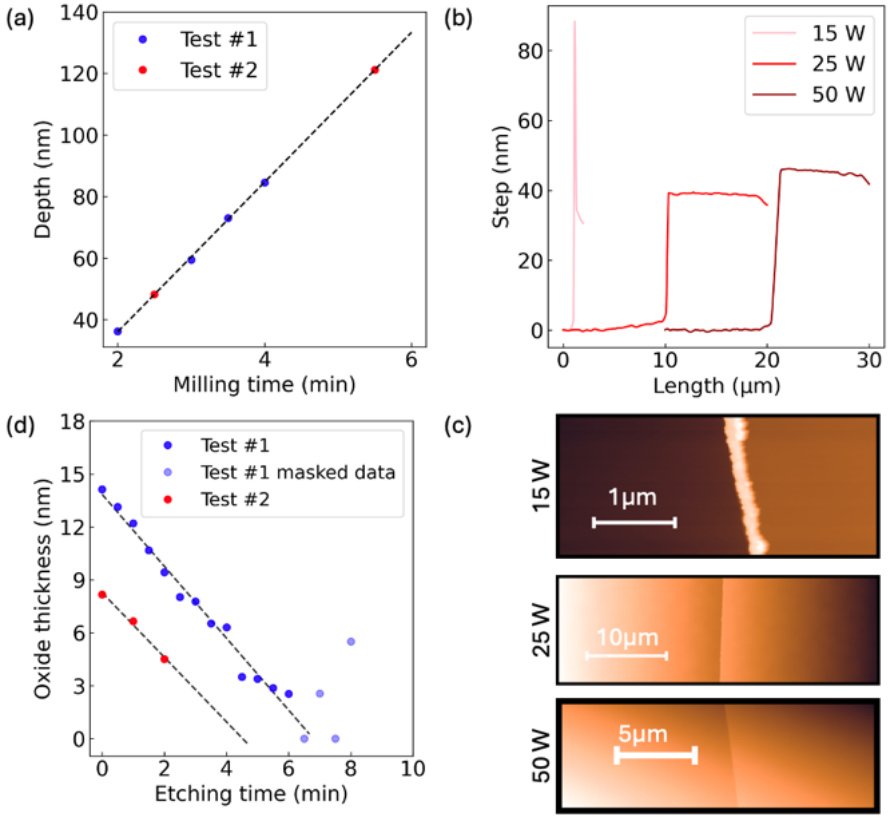


Figure 4.7: Analysis of etching tests. (a) DC (Kaufman) dry etch test The fitting reveals the etch rate of the heterostructure. (b-c) AFM analysis of RF dry etch test on the heterostructures: (b) Cross-sections indicating the etch depth and (c) AFM images of the etching step (e) Wet etch test of Al_2O_3 ALD films.

4.5 WIREBONDING TECHNIQUES WITH 2DS

Wirebonding is an essential process to achieve electrical connections down to the chip level. Here, the aim is to provide an overview of the main techniques and critical aspects of wirebonding, and its influence on device fabrication. A more detailed description of the electrical connections of the chip related to the measurement apparatus will be discussed further in the reading.

The chip is mounted to a cavity with electrical connections called **daughterboard**. The mounting can be achieved either with PMMA or silver-paint. The daughterboard will be connected to the **motherboard** and further to the electrical connections of the refrigerator. A semi-automatic **F/S Bondtec 5630** wirebonder is used in the cleanroom at the University of Copenhagen. An Al:Si (99:1) wire with a thickness of 25 μm uses pressure and ultrasonic power to connect the PCB pads to the substrate pads. In Figure 4.8, an image demonstrates the movement of the wirebonder head from the PCB pad to the Chip pad.

The two described approaches for substrate etching both aim to address the elimination of leakage to the substrate via mechanical deformation due to wirebonding. Mesa etch (via DC argon – Kaufman milling) or protection bonding pads (200 nm of Ti) were employed on different fabrication attempts. In Figure 4.8 b, the two different methods of bondpads are presented, as well as the failure mode when none of the approaches is implemented. In the first case, the bondpads don't have a 2D carrier gas beneath since it has been removed via the dry etching process. In the second case, the substrate remains intact. Large Ti pads of 200 nm are deposited on top of the gate pads for protection. In between the lower and upper pads, small etching windows were opened to remove the ALD oxide and ensure the electrical connection between the two layers. Although anecdotal evidence indicates that mesa etch can be detrimental to the quality of the devices, substrate leakage has been successfully eliminated. On the other hand, wirebonding on the thick stack of Ti can sometimes produce failure modes. For example, when the bondhead is misaligned from the target position, the wirebond is placed partially off the tick bondpad and on the substrate, which results in mechanical deformation.

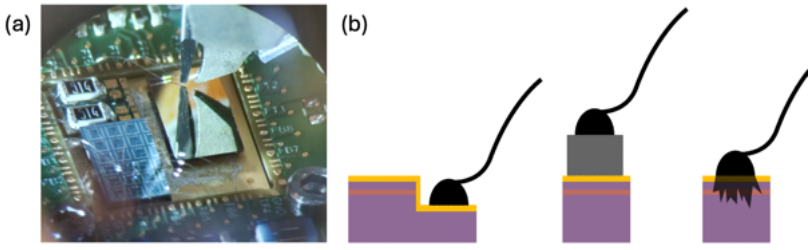


Figure 4.8: (a) An image of the wirebonder head while bonding on the substrate and (b) different wirebonding approaches to address the substrate leakage.

4.6 SAMPLE CHARACTERIZATION TECHNIQUES

Inspection of the final outcome of the fabrication is necessary due to the low reproducibility of lithography and the various failure modes discussed in this chapter. During all fabrication steps, the devices are inspected by optical microscopy for any obvious failures. Once the chip is complete, test structures identical to the quantum devices are characterised by SEM. Due to the carbon deposition on the surface of the inspected subject, the inspection of the devices dedicated to measurements should be avoided. To circumvent this issue, AFM can be used as a more reliable alternative for precise measurements. Since AFM is a non-destructive technique, it is possible to get the topography of the device. However, every scan takes at least 5 minutes and identifying the range of interest can take up to 10 minutes. This means that with eight devices, one can spend two hours. On the contrary, the total time of the SEM inspection can be done in less than 15 minutes. Figure 4.9 presents an identical device scanned both by AFM and SEM.

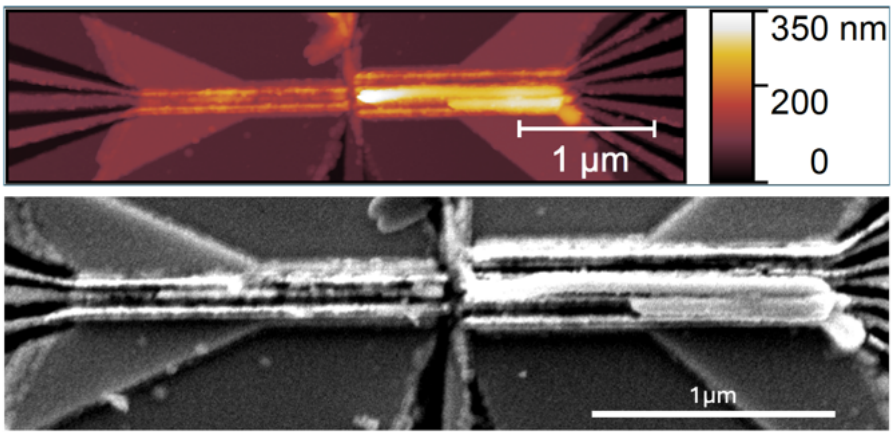


Figure 4.9: A Si triple quantum dot array scanned by AFM (upper) and SEM (lower).

5

QUANTUM DEVICES

This chapter focuses on the functionality of the quantum devices. Two distinct sets will be addressed, Hall bars and linear quantum dot arrays. The material platform extends from Ge/SiGe heterostructures to Si/SiGe and SiMOS, both academically fabricated but also produced in foundries. The fabrication relies heavily on lithography techniques to achieve precise patterning. Due to the critical dimensions that the devices require, multiple failure modes were observed. An extended discussion on the fabrication challenges is presented to avoid future students falling into the same pitfalls. Moreover, the discussion continues by addressing the challenges associated with the measurements and suggesting solutions based on the findings.

Three different projects are involved in this chapter. The first is related to Part i of this thesis. The target is to fabricate quantum devices with the purpose of characterising the electrical properties of the quantum wells for the first time. The second project focuses on the realisation of spin-qubits on isotopically purified ^{28}Si/SiGe heterostructures. Last, the final project explores the capabilities of foundry-fabricated devices. In this chapter, the role of foundries and the types of devices that we received will be presented.

For the Ge project, **Oliver Liebe** developed the lithography recipes, providing invaluable contributions that accelerated the project. The initial discussions during the design development were inspired by **Georgios Katsaros's** group. The author extends his deepest gratitude for the feedback and inspiration that Gergios offered unconditionally.

5.1 GERMANIUM DEVICES

Germanium combines several outstanding properties that make it highly advantageous for the fabrication and operation of spin qubits. One of the essential criteria for future quantum technologies is the technological potential to purify germanium in its natural abundance and cancel the effects of nuclear spin. Such a possibility has already been demonstrated in crystal growth [13, 52]. Moreover, results on ^{28}Si devices highlight the significant advantage in coherence times after isotopic purification.

Regarding the fabrication of quantum dot arrays, Ge has a smaller effective mass compared to Si, making the fabrication process less challenging and more forgiving. The good electronic properties, such as high carrier mobility and low percolation density, indicate the high potential of the material platform. Additionally, the tunable spin-orbit coupling [46, 72] and the low operational magnetic fields [73] provide fewer requirements to operate spin qubits and open the way to new approaches. The compatibility of Ge quantum wells with superconductors and the realisation of hybrid quantum devices is an additional advantage for future technologies. From the coupling of qubits via superconducting mediators [6] to the spin-photon coupling via superconducting resonators without piezoelectric effects like the ones in III/Vs open the way to many opportunities. Last, the challenge of the valley degeneracy is not a concern in Ge. In sGe quantum wells, the strain typically lifts the degeneracy of heavy and light hole subbands, simplifying the electronic structure of the system.

The devices included in the *manuscript under preparation* [21] are fabricated on **Sample 6** heterostructure. Here, the fabrication details are presented. Two types of devices were used in this study to characterise the heterostructures. Hall bar devices and linear quadruple quantum dot arrays with lateral sensors at the array edges were fabricated on the same chip. In Figure 5.1, optical images of the entire chip surface, as well as close-up images of the quantum dot array (SEM) and Hall bar (optical), are presented.

For the fabrication of the chip presented in Figure 5.1 a the process started with the Au markers. Afterwards, the substrate was etched, leaving mesas as the active regions. The 22 nm Al ohmic contacts were annealed in the *Rapid Thermal Annealer* for 15 minutes at 350 °C under Ar atmosphere. Afterwards, the contrast of the ohmic contacts changed as seen in Figure 5.1 c at the darkfield view of the Hall bar device. The first Pd gate layer introduced the screening and barrier gates for the quantum dot array as well as the top-gate for the Hall bar device. Above and below this deposited layer, 10 nm of Al_2O_3 were deposited for electrical isolation of the gate stacks. Last, a final Pd layer was deposited to form the plungers of the quantum dot array.

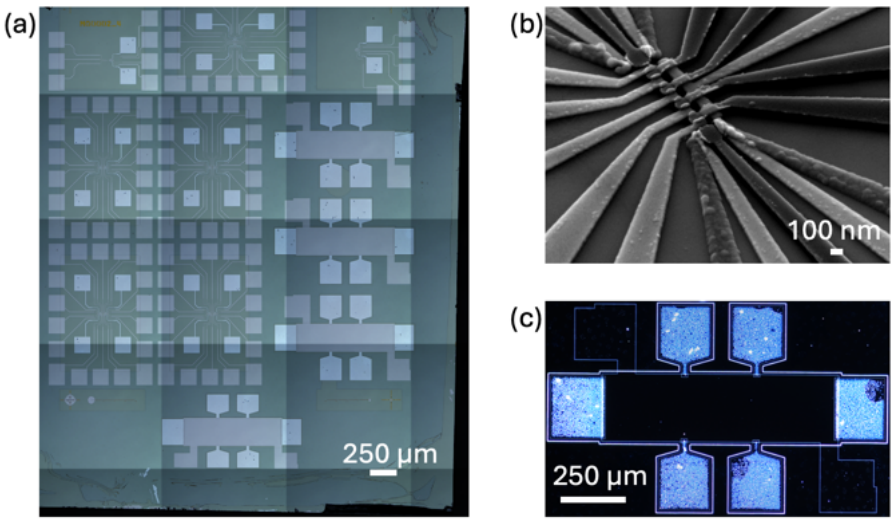


Figure 5.1: (a) Large-scale optical image of the chip. The mesh of the image is an artefact from the image reconstruction. (b) Tilted-SEM image of a quadruple quantum dot array. (c) Darkfield optical image of a Hall bar device

To ensure the climbing of the gates at the mesa, the bondpads were optimised to be by 20% on top of the mesa. This maximum coverage ensured successful climbing without the need to run any diagnostics. The rest of the pad (80%) on top of the substrate was sufficient to wirebond with maximal success. No gate leakage was observed due to mechanical deformation of the substrate.

5.2 SILICON DEVICES

Silicon field-effect transistor (FET) devices require dopant regions to achieve highly conductive carrier reservoirs. This can be achieved either with p or n doping implantation. In the case that the target is to form a 2DEG then phosphorus ions (P^+) are deposited in lithographically defined windows. In Figure 5.2 a and b, a schematic of a Si FET with electrons as carriers is illustrated. A metallic top-gate above a dielectric can allow the formation of a 2DEG above a certain electric field corresponding to a $V_{threshold}$ voltage. For the confinement of the electrons in zero dimensions and the formation of a quantum dot, the single top-gate is segmented into at least five gate electrodes*. From the implantation regions, **accumulation** gates bring the highly conductive 2DEG close to the quantum dot electrodes, accumulating

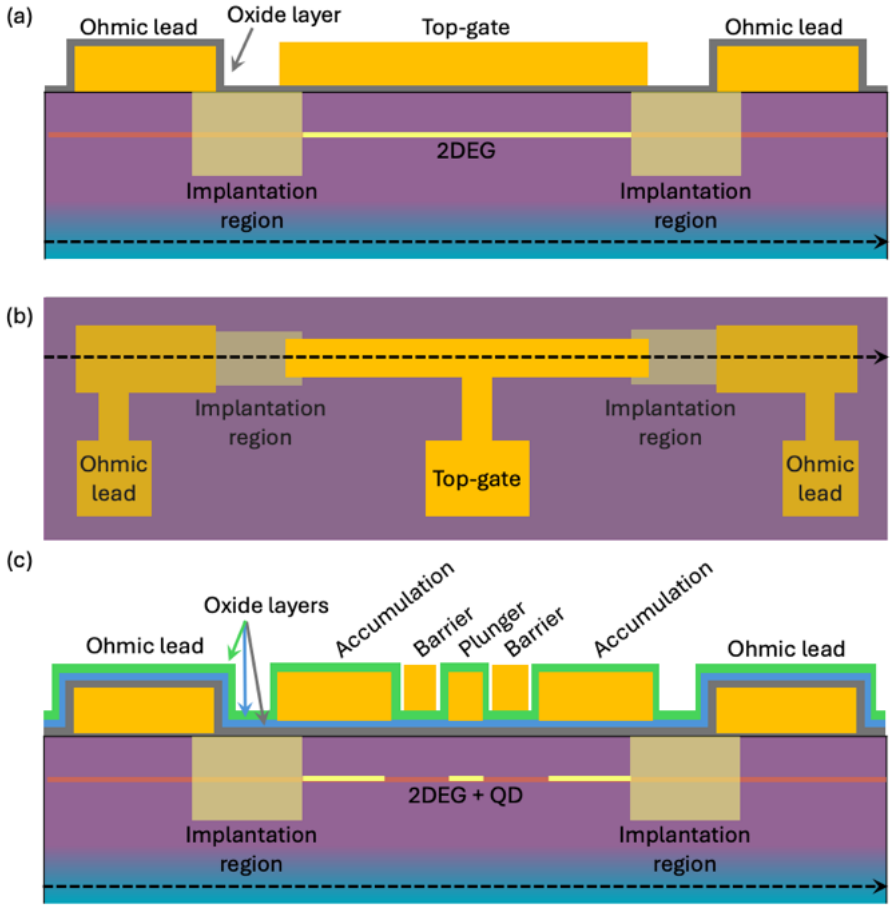


Figure 5.2: The formation of a 2DEG in a Si heterostructure with n-doped regions. (a) A cross-sectional and (b) a top view schematic of a Si FET device exhibiting a 2DEG. (c) A cross-sectional schematic of a quantum dot Si quantum dot device. The single top-gate is split into multiple segments allowing the confinement of the 2DEG and the formation of a quantum dot.

* additional electrodes are needed as screening gates

charges underneath. Then, typically to the standard single quantum dot design, a set of **barrier** gates is used as tunnel barriers and a **plunger** gate is used to tune the chemical potential and the occupation of a quantum dot. For the P^+ implantation, optical lithographic openings were defined and the samples were shipped to *Sherbrooke University, Canada* for the implantation procedure. In Figure 5.3 a and b, a design CAD and a brightfield optical image, respectively, demonstrate the ohmic electrode, implantation region and accumulation gate. Below the accumulation gate an ALD oxide layer is deposited for electrical insulation. The heterostructure used in this study is grown by CVD in the *Scappucci Lab, TU Delft*. In Figure 5.3 c the heterostructure of the project is given based on Reference [74]. The quantum well features an isotopically purified ^{28}Si with a low concentration of ^{29}Si at 800 ppm. The shallow quantum well is buried 30 nm below the surface and is only 8 nm thick. In Figure 5.3 d, the simulation of **Stopping and Range of Ions in Matter** (SRIM) is given based on the parameters of the heterostructure and the ion implantation dose.

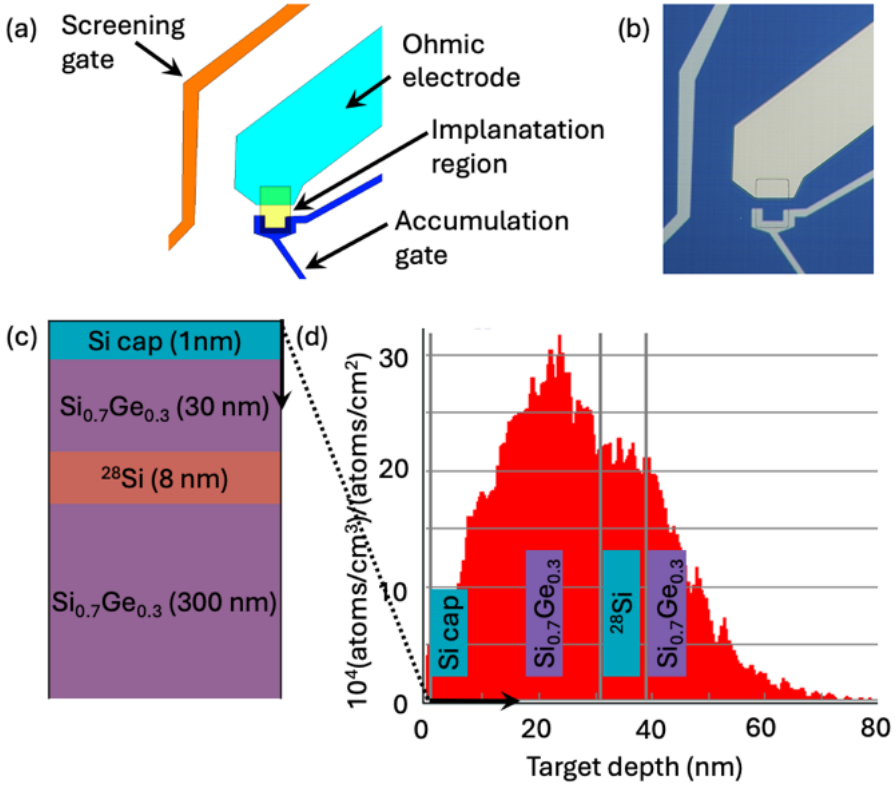


Figure 5.3: Implantation in Si: (a) A CAD design of an implantation region together with the ohmic and accumulation gate electrodes. (b) The associated optical image of the fabricated device. (c) The $^{28}Si/SiGe$ heterostructure from the *Scappucci lab*. The 8 nm thin ^{28}Si quantum well is 30 nm below the surface encapsulated in $Si_{0.7}Ge_{0.3}$ spacers. (d) The distribution of P^+ ions from SRIM based on the dose and heterostructure parameters.

Multiple chips were fabricated using different techniques, and only the final fabrication version will be reviewed here. Based on the clean-room experience, it contains all the necessary ingredients for a possibly successful outcome. In Figure 5.2 a, a large-scale optical image of the final chip is given. SEM images of the lateral (b) and parallel (c) sensor designs are also presented in Figure 5.2. The ohmics are fabricated with optical lithography and HF etching prior to Pd deposition. In contrast to Ge devices, no annealing step is needed. The three gate layers of *screening*, *accumulation/plunger* and *barrier* gates are deposited in the order that were mentioned. ALD Al_2O_3 is used to insulate electrically gates in close proximity.

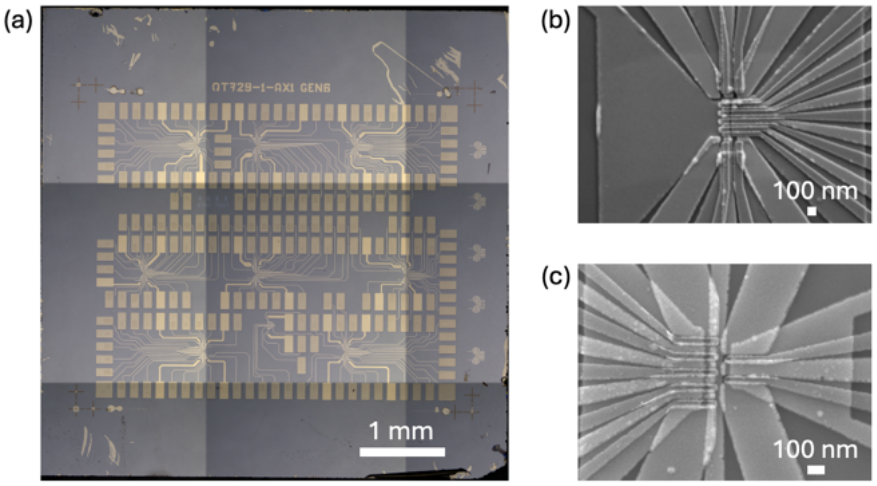


Figure 5.4: (a) Large-scale optical image of the chip. The mesh of the image is an artefact from the image reconstruction. (b) SEM image of a linear triple quantum dot array with lateral sensor dots at the edges. (c) SEM image of a linear triple quantum dot array with a sensor parallel to the array channel.

5.3 IN-HOUSE DEVICE CHALLENGES

Overall, the Si/SiGe were very challenging. **11** chips were fabricated, and different parameters were tuned in every attempt. Compared to the success of the Ge/SiGe, only **4** chips were fabricated until we measured a successful one.

In the following paragraphs, the identified failure mechanisms are listed and tacking solutions are suggested. It is worth mentioning that even though there were successful fabrication rounds, the electrical tuning of the devices brought up new challenges. This diagnostic will also be commented on here.

5.3.1 *Fabrication*

- Various e-beam resists such as A3, double layer of A2 and CSAR4 were used in different fabrication attempts. We settled on CSAR4 since it requires a lower dose (faster exposure) and has a larger dose tolerance. However, this does not apply to critical features.
- The cleanroom at the University of Copenhagen has two EBL tools with different specifications. Both tools have been used in different fabrication attempts. In one of them, dramatic misalignment between the different layers has been observed. This resulted in an overlap between the finger gates of the plunger and the barrier gates, making tuning impossible. This tool was not used later.
- We made many devices using one of the ALD tools at the University of Copenhagen (Cambridge systems). However, it seemed unreliable, often resulting in leakage and shorts between gate layers. We decided to find solutions outside the institute, and we used the ALD tool at the Technical University of Denmark (PicoSun), which resulted in a higher yield. Moreover, the breakdown voltages observed were much higher.
- Metal-Oxide-Metal devices were employed as test structures for characterising the dielectric, but the results were inconsistent with the fabricated quantum dot arrays. In particular, even though the test structures indicated leakage, the devices were successful. In the future, it would be interesting to identify correlations between the test nanostructure and the quantum dot array gates.
- Two methods were investigated to eliminate leakage to the substrate via mechanical deformation due to wire bonding as discussed in the previous section.
- In contrast to the two rounds of the germanium devices, the additional round increases dramatically the chances for failure.

Three-layered EBL fabricated devices are most likely to fail. Throughout this project, we struggled a lot with shorted and leaking gates. Three gate layers significantly increase the chances of getting a failed gate. In addition, they increase the fabrication time that potentially could have been used to fabricate more but simpler and more successful devices.

- Stressing the issue of reproducibility, we have observed that even test structures for SEM in between gate layer rounds can still vary from the real device significantly.
- The inconsistency of the final device outcome led us to run a dose test prior to each fabrication attempt.

5.3.2 *Measurements*

- As it is described in Chapter 5.2, the spin qubit community has two state-of-the-art designs for fabricating 1D quantum dot arrays. Due to the challenges of achieving charge sensing both designs were explored with bigger success shown on the lateral sensor devices. This design works better and doubles the chances of creating a single singlet-triplet qubit on each side of the array. Of course, with this geometry, it is only possible to read up to three quantum dots, which limits the one-dimensional array to six quantum dots in a row.
- Regardless of the design, it was always challenging to perform RF reflectometry in Si. For the implantation regions, an old design was followed without paying extra attention to the location of the ohmics contacts. According to Reference [75], the implantation region should reach as close to the active region as possible. This can prevent the change in the resonance frequency from being caused by the large semiconducting region below the accumulation gate, but since the accumulation gate is smaller, the signal will not shunt through the ground and will be reflected at the sensor quantum dot.
- Screening of single devices in a quick loading system (such as a Kiutra L-type or a cryo-prober) can significantly contribute to a faster feedback loop. Loading and unloading from such a cryostat doesn't result in electrostatic discharge. To prove that, we loaded a fully functional device multiple times to observe if ESD would blow it up. However, this was not observed. Moreover, the device was transferred to a different motherboard and loaded to a different refrigerator. In that case as well, no ESD was observed. When we tried to remove the wire bonds from another fully functional device and bond in a different configuration, some of the gates shorted with each other, making the

device non-functional. To conclude, once a fully functional device is identified in a screening refrigerator, the chip can be safely transferred to a dilution refrigerator.

5.4 FOUNDRY-FABRICATED DEVICES

Foundries are facilities that fabricate semiconductor chips. Although they are often associated with *fabrication facilities*, these two terms do not always coincide. Foundries, in principle, fabricate on designs that *fabless* companies have provided. In addition to manufacturing, fabrication facilities are also involved in the development of the chips, such as design and characterisation. In this thesis, no distinction will be made and the term foundry will be generically applied in all cases.

Foundries have the knowledge to prototype semiconducting devices rapidly and reproducibly. They have a significant qualitative advantage in terms of designs, fabrication processes and materials. The characterisation of samples produced in 300 mm integrated silicon MOS platforms generates a large amount of data that can provide resourceful feedback and accelerate the development of a spin-based quantum processor. In addition, the advancements in flexible back-end-of-line integration and control periphery for large-scale qubit arrays give an extra advantage once the number of qubits becomes unmanageable.

Realising the potential market towards the realisation of many-qubit quantum processors, foundries implement their expertise to the latest academic advances. In this attempt, many consortiums have formed over the past decades. The University of Copenhagen has been a member of the **Quantum Large Scale Integration in Silicon (QLSI)** European consortium. Group IV semiconductor spin qubits is a very appealing platform for foundries since they have excelled in their fabrication techniques with semiconductor chips for the industry. Of course, a transition to chips related to quantum computing is not straightforward and requires a lot of optimisation. The reliability of the tools provides a low deviation in the properties of the final devices. However, there is always the risk that the properties of the devices won't meet the experimentalist's requirements. For that, more specific **Process Design Kits** (PDK) should be developed with the aim of quantum device optimisation. In contrast to a regular PDK, there is an extra requirement for characterisation at cryogenic temperatures to ensure accurate data quality.

Similar to what is taught in undergraduate statistics, the advantage of foundry devices is a very small spread, but the results can be outside the zone of interest, meaning low accuracy but high precision. On the other hand, in academic labs, the exact opposite scenario occurs. The yield of the devices is low, but a few of them may be functional, meaning higher accuracy but low precision.

Throughout the collaboration with IMEC, a handful of chips were received both in Si/SiGe heterostructures and in the SiMOS platform. Devices on the same chip exhibited similar features. For example, if one device showed high-quality results, then a similar behaviour

would be observed across the majority of the devices. In the same way, if some of the devices seemed problematic with leakage and not good turn-on characteristics, most likely, the entire chip would be problematic. The demonstration of Si/SiGe devices will be omitted here since their functionality is already described in Chapter 5.2. Instead, the discussion will focus on SiMOS quantum dot devices.

The best way to conceptualise the SiMOS quantum dots is by introducing the metal-oxide-semiconductor field-effect transistor (MOSFET). First, a Si substrate is the host material platform. Doped regions act as highly conductive carrier reservoirs. In this thesis, only n-type doping was investigated. For simplicity, the discussion will continue by focusing on electrons as carriers. An oxide layer insulates electrically the ohmic regions and the substrate from any deposited gate above them. Metallic electrodes (top-gates) can be used to apply electric fields that allow the formation of a 2DEG below them. The vertical confinement of the 2DEG is realised at the interface of the Si substrate and the oxide. Depending on the chosen geometry for the top-gates the confinement can be reduced to 1 and 0 dimensions.

Multiple current paths can be realised using complex geometries in such structures. For example, in Figure 5.5 b, a double quantum dot array has a proximate sensing quantum dot, and the two devices share the same source. With two multimeters, it is possible to keep track of the two current paths illustrated by the black arrows. This is a typical device of the quantum dot arrays that were used in the lab from imec. They are fabricated using a 300 mm integration flow. Initial chips were using TiN gates [76], but later, they were substituted by polycrystalline silicon [77]. Introducing the same material for the gate stack and the substrate has the advantage of minimizing the difference in thermal expansion coefficients. This reduces the strain impact on the substrate from the deposited gates and minimises further disorder [78]. It is worth mentioning that above the Si(001) substrate, a layer of ^{28}Si is deposited to enhance the qubit quality.

Regardless of the material, the gate stack comprises a screening gate, a set of barrier gates and a set of plunger gates. Very interestingly, even though the gates of the qubit array and the sensor have similar functionality, don't belong in the same layer stacks. First, only the single screening gate is deposited. Usually, it forms a c-shape and in its cavity, the quantum dot array is enclosed. The second layer that is deposited is the green-coloured gates of Figure 5.5 b. On the sensor side, these gates correspond to the barrier gates, and on the quantum dot array side, they correspond to the reservoir and the two plunger gates. Last, the final layer is deposited, which has a dual purpose for the sensor quantum dot. It is a continuous metal strip that is used to bring the carriers close to the dot, i.e. accumulation gates, and to tune the chemical potential. On the side of the array, the deposited gates

are solely used as tunnel barriers. Between each gate layer, 5 nm of thermally grown SiO_2 film ensures electrical insulation.

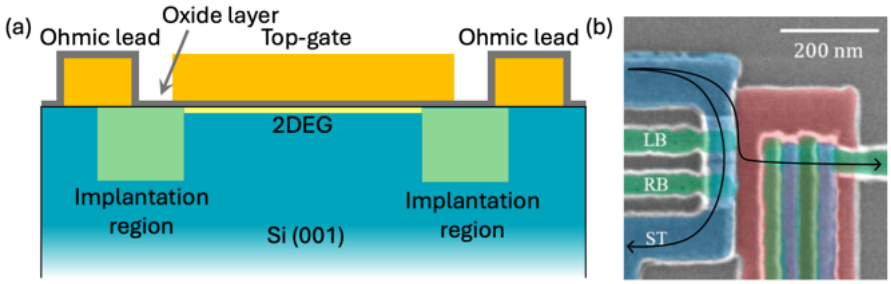


Figure 5.5: (a) A MOSFET schematic. (c) An SEM image of a double quantum dot array with the sensor. Arrows indicate the two paths.

Once the chips are cleaved, each device is tested at room temperature for leakage and then shipped to the laboratory. Once the chips are received and documented, only bonding is necessary to begin the cryogenic testing. In Figure 5.6, optical images of the chip at different stages demonstrate the processing prior to loading.

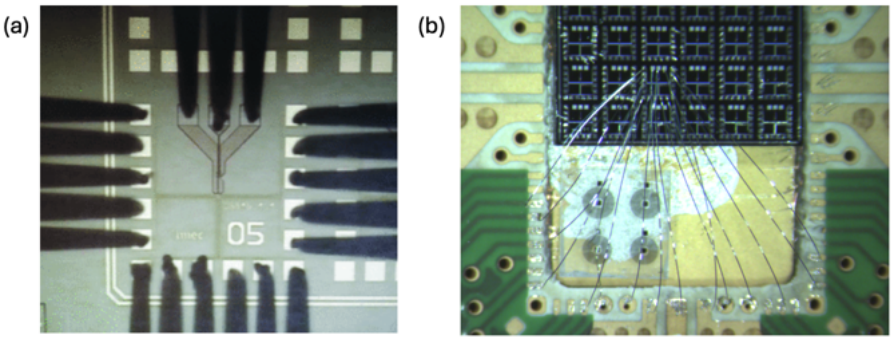


Figure 5.6: Electrical screening of foundry devices: (a) An optical image from [76] demonstrating the room temperature probing. (b) An SEM image after wirebonding.

Part III

MEASUREMENTS

6

SPIN QUBITS WITH SEMICONDUCTOR QUANTUM DOTS

Although this thesis does not reach into practical implementations of spin qubits, it lays the foundational groundwork for future research. It serves as a comprehensive guide for the next generation of students, enabling them to fabricate devices with well-defined characteristics and further perform qubit operations.

To begin with, the fundamental aspects of quantum dots will be discussed, including theory and technical details. Specific interest in the next steps after the realisation of quantum dots will be given to the spin property of the charge carriers. The conceptualisation of the conversion of the spin to charge will be discussed. As a final point, this chapter introduces the measurement setup, including the refrigerators, relevant measurement techniques and established characterisation sequences.

The author is grateful to **Fabrizio Berritta** and **Tsung-Lin Chung** for all the discussions and their patience on the wiring of the setup and the correct configuration of the instruments.

Important keywords that the reader should distinguish are listed below. Moreover, parts of the equipment in the lab are provided by *QDevil, now part of Quantum Machines* and the naming is explained for clarity:
Gate: Electrostatic gate that control the local potential environment.
Ohmic: Electrode probing the carrier reservoir of a quantum device. The current in the ohmics features a linear (ohmic) relation with the source-drain voltage.
Daughterboard or **chip carrier**: A printed circuit board (PCB) with a cavity and interconnections that allows the electrical connections between the chip and the measurement hardware
Motherboard: A PCB that contains all the essential connections and wiring. The daughterboard is attached via Au fuzz buttons and an interposer to the motherboard.
Puck: A cylindrical enclosure containing the motherboard and has external connections. It is attached at the coldest stage of the cryostat either by the use of a loadlock (without breaking the vacuum and warming up) or by opening the cryostat (in atmosphere).
Breakout box: Distribution of the electrical connections from the cryostat to the experimental setup. Each electrical line can be addressed individually and corresponds to a unique number.

BNC cables: Bayonet Neill–Concelman **coaxial cables** with a bayonet locking connector at the two ends. It is used to connect instruments to the electrical lines of the breakout box.
Float/Ground/Bus: The three modes of each line in a breakout box controlled by internal switches. **Float** separates the inner and outer core, whereas **ground** connects them. **Bus** also separates the inner and outer core and additionally, connects the line to a common addressable line.
Acquisition computer: A computer controlling the instruments and performing the measurements.
Fridge: The refrigerator or cryostat that cools down the chips.
QBoard: Daughterboard
QFilter: cryogenic RC and LC filters
QBox: Breakout box
QDac and **QDac-II**: Models of digital-to-analog converters

6.1 QUANTUM DOTS

Electron confinement through bandgap engineering is a method for reducing the electronic dimensionality of a system. It is crucial to the development of today's technologies with applications ranging from lasers and light-emitting diodes to quantum processors. In its broad sense, it utilises the epitaxy of multiple layers with wider and narrower bandgaps to confine the charge carriers in thin layers. Sophisticated material stacks and thicknesses control the strain and subband energy levels. This technique is robust and versatile allowing the design of devices with tailored electronic and optical properties.

Nanofabrication methods can offer confinement down to one and zero dimensions. Electrostatic gating forms a local potential that accumulates or depletes carriers in a quantum well region. This effect can form field-effect transistors and quantum point contacts. Furthermore, by splitting these gates into multiple segments, the one-dimensional channels can be further confined to zero dimensions forming quantum dots. Figure 6.1 reviews the charge carrier confinement from bulk down to a single quantum dot. The dimensionality of the system influences the density of states offering different physical phenomena.

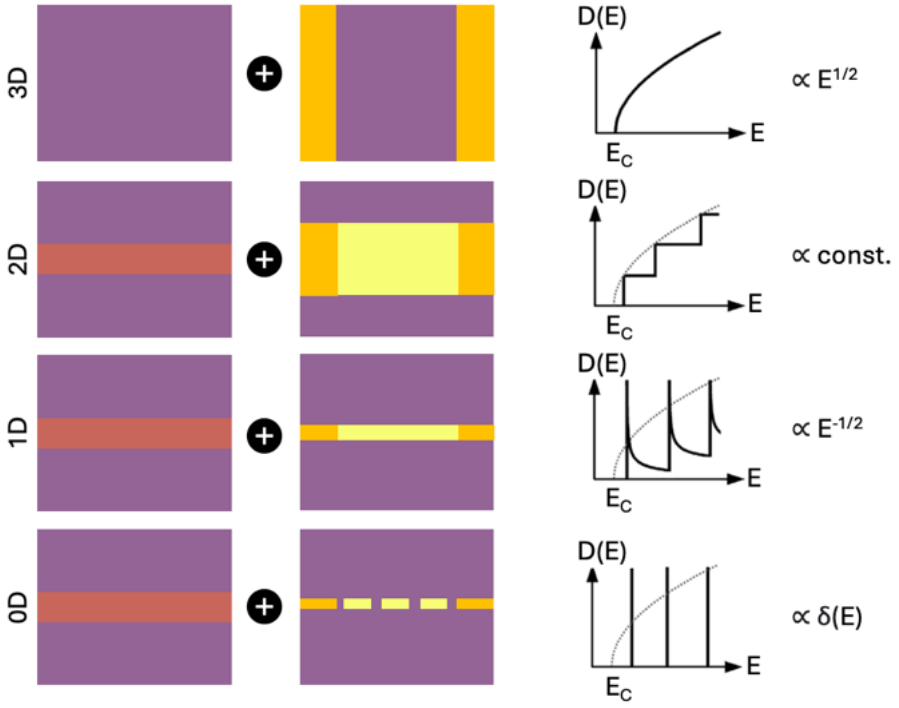


Figure 6.1: Charge carrier confinement from 3 (top) to 0 dimensions (bottom) and associated density of states (right). The left column displays cross-sectional schematics of the vertical confinement via bandgap engineering. Combining the substrates of the left column with the gating geometries of the middle column, it is possible to achieve confinement in all dimensions. The electronic system is described by the density of stats as shown in the right column.

If the quantum dot gates are segmented further in complex geometries, multiple zero-dimensional objects can be formed, creating chains and arrays of quantum dots. From there, only fascinating applications can be realised by exploiting the capabilities of electrostatic gating and bandgap engineering in multiple quantum dots. In Figure 6.2 two different cases of complex (a) vertical [79] and (b) lateral [4] confinement are presented.

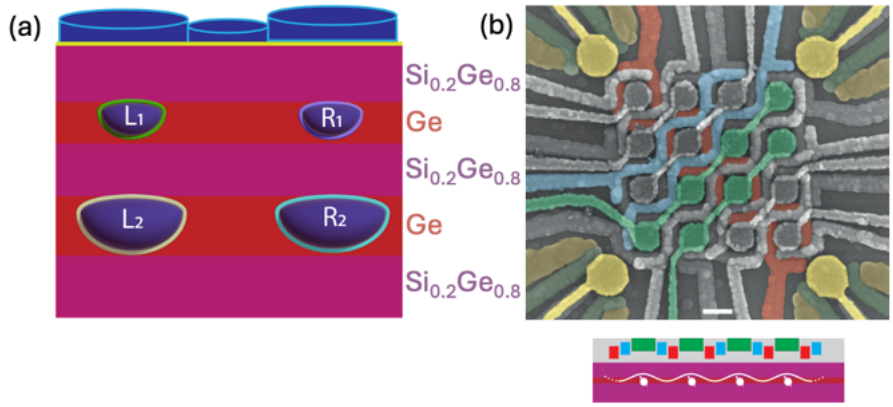


Figure 6.2: Quantum dot arrays utilising electrostatic confinement from (a) bandgap engineering [79] and (b) complex gate geometries [4].

Single quantum dot

Focusing more on the specifics of a quantum dot, a plunger gate is used to modulate its electrochemical potential. Reservoirs at a finite bias and temperature provide the carriers to the system. In Figure 6.3, the loading of electrons in a single quantum dot is presented. When an energy level is aligned with the source and drain transport is allowed (Figure 6.3 a). Increasing the gate voltage, electrons are loaded in the system in discrete levels. The occupancy of the quantum dot is described by the number N in Figure 6.3. When no energy level is aligned with the source and drain, then the quantum dot goes into Coulomb blockade (Figure 6.3 b). By increasing the Source-Drain voltage, the window for transport gets broader, and the coulomb blockade regime gets smaller, as illustrated in Figure 6.3 e.

The barrier gates between the reservoir and the plunger gates control the electrostatic potential environment and effectively the couplings Γ_S and Γ_D of the quantum dot with the Source and the Drain, respectively. Adding an electron in a quantum dot requires energy $Ec = \frac{e^2}{C}$ where C is the total capacitance. The thermal energy of the system k_BT should be much lower than the charging energy to ensure single-electron tunnelling.

In Figure 6.3 d, an illustration of a typical bias spectroscopy diagram describes the measurements in a quantum dot. Dark-shaded areas indicate electron transport while white areas indicate Coulomb blockade.

On the x-axis, the gate voltage V_g of the plunger gate of the quantum dot is tuned, similar to the moving of the chemical potential. On the y-axis, the Source-Drain voltage V_{SD} widow indicates the bias window of the schematics. Last, when measuring the current I_{SD} through a quantum dot, for positive bias voltages, the current is positive, and for negative bias voltages, the current is negative. However, no distinction is made on the plot of Figure 6.3 d, since its purpose is solely the description of coulomb blockade.

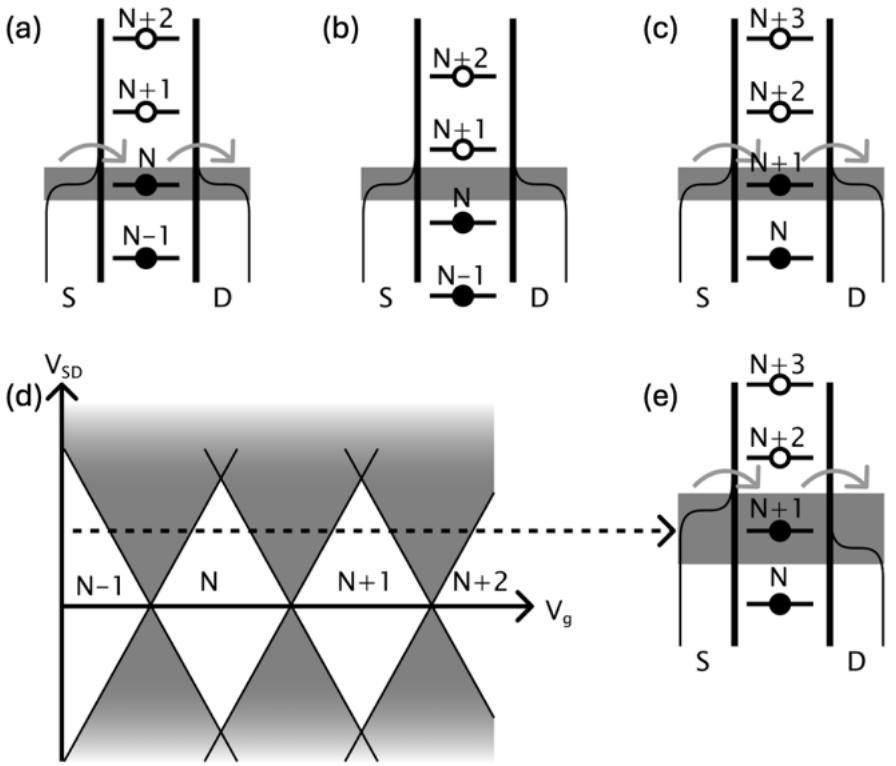


Figure 6.3: Coulomb Blockade of a single quantum dot. Energy levels indicate the electronic occupation of the quantum dot. N indicates the number of electrons occupied in the quantum dot. White colour is identified as no transport in the plot and gray as transport. No distinction between negative and positive current is given here. In the white areas, the quantum dot is in Coulomb blockade and has a constant charge occupancy.

Double quantum dot

Extending the description from a single quantum dot to two connected in series, transport is allowed when the chemical potentials of both dots are inside the available bias range. The transport of a double quantum dot is visualised as a combination of two single quantum dots. The two plunger gates are plotted on the xy-plane, and the colourmap indicates the electron transport through the system. Quantum dots are not objects isolated from their environment. Rather, they adhere to any charge disturbance. In short, they are capacitively

coupled to any proximate system. Gates controlling neighbouring quantum dots contribute electrostatically to the entire landscape. Thus a more accurate visualisation of the transport through the double quantum dot requires slanted transport lines indicating the capacitive effect of the two plunger gates.

In Figure 6.4 a, a graph of a double quantum dot is given. Outside of the main plot, the signal for each individual quantum dot is plotted as Coulomb peaks. The peaks are extended into the 2D representation for a double quantum dot. Parallel lines indicate the gate configuration where the chemical potential of a dot is aligned to the source-drain bias window. In a double quantum dot, current is obtained at the points where the parallel lines intersect, and the chemical potentials of the two quantum dots are aligned.

Three main classifications are distinguished as the inter-dot coupling increases [80]. First, similar to Figure 6.4 a, the two quantum dots are weackly coupled to each other. While the middle barrier gate becomes less opaque, the double quantum dot has increased inter-dot tunnel coupling, where it is possible to perform transition of carriers inside the quantum dot. Additional feature signals occur at the *charge anticrossings* and the charge stability diagram has a honeycomb pattern (Figure 6.4 b). Further, the double quantum dot becomes almost a large single quantum dot at the strong coupling regime (Figure 6.4 c).

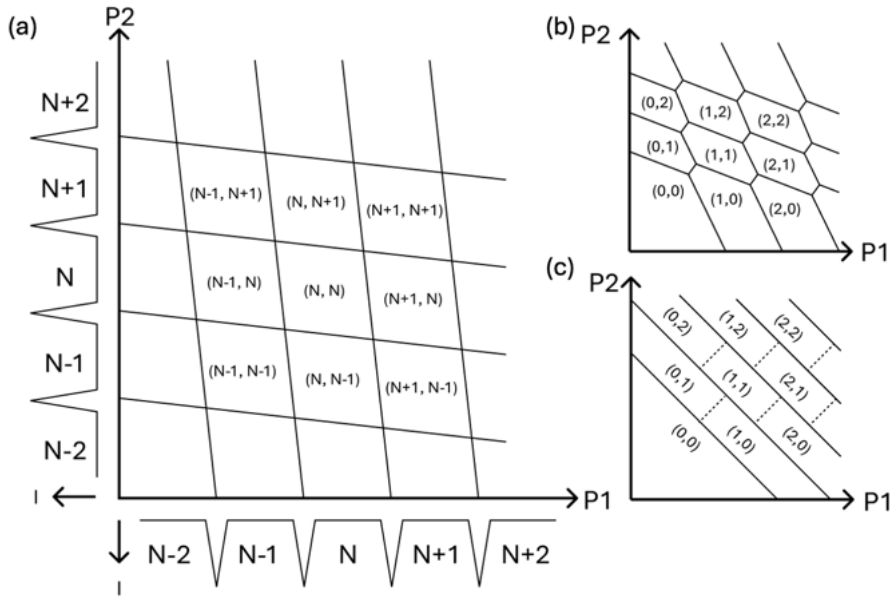


Figure 6.4: Double quantum dot and coupling configurations. (a) Diagram for the formation of a double quantum dot in the weak inter-dot tunnel coupling regime. N denotes the number of charges in each quantum dot. Transport occurs at the intersection of the parallel lines. (b,c) A double quantum dot with increased inter-dot tunnel coupling (from b to c).

Charge sensing

In a more practical application, quantum dots can be used as electrometers. Utilizing the capacitive effects between individual quantum dots, it is possible to monitor the charge occupancy of a neighbouring quantum dot. Coulomb peaks are distinguished for their high aspect ratio features. This means that small changes on the x-axis of the gate voltage can lead to large deviations on the y-axis of current. As a result, this technique makes current measurements through the investigated quantum dot system redundant. A charge sensor is usually employed to detect the charge occupancy for up to three quantum dots [81]. It is important to mention that in this technique, the charge sensor channel is capacitively coupled to the sensed quantum dot. Thus, two different current paths need to be realised. In this way, if a capacitive shift occurs in a neighbouring dot (such as loading an electron), then the signal of the sensing quantum dot will be disturbed, indicating a change in the environment.

As it has been demonstrated in [82], by using a 2×2 array, it is possible to combine the previous discussion in a complete quantum device. On the one hand, the two double dots can be in the tunnel coupling regime. They are isolated from the two lateral dots that are strongly coupled into a single dot that serves as a charge sensor. All the dots can be addressed with that objective without having design limitations, as is usually the case of the design presented in chapter 5.4.

6.2 SPIN-TO-CHARGE FOR SPIN QUBITS

In the laboratory, no equipment can directly record the spin property of the electrons (or holes). This is a fundamental problem for the spin qubits systems since there is not a *spin-meter* tool for quantum dots to be used as a detector. No matter the setup that is used, the data are stored as voltages or currents coming either from the amplitude of the RF signal of the capacitive and resistive changes of the tank circuit or the DC current of the device. However, by utilizing Pauli's exclusion principle in quantum dots, it is possible to identify if a spin is up or down. In particular, this means that by transferring a charge carrier in the quantum dot, it pairs as spin up and down, but it will not pair as spin up and up or down and down. This technique of identifying signal features and translating them to spin is called **spin-to-charge conversion**.

Further, by identifying the spins in a single, double or triple quantum dot, it is possible to form a spin qubit. Spin qubits come in different forms. The most simple case is the **Loss-DiVincenzo qubit** [2], where a single quantum dot is required and the quantum information is stored to the spin property of the carrier. Using a double quantum dot, a **Singlet-Triplet qubit** can be used at the low occupancy with the singlet and the triplet states defining the ground and excited states of the qubit along the detuning axis [83]. Last, the exchange-only qubit involves three electrons in a triple quantum dot, with the readout focusing on the different spin and charge configurations [84]. This thesis will not go deeper in the details of the qubits and the author hopes that this will be a task for the next generation of students in the lab.

For completeness, the methods of the chapter will close with the introduction of the two techniques widely used for spin-to-charge conversion.

For the first approach, a single quantum dot and a loading reservoir are sufficient. Using two energy levels (ground state and excited state with different spin configurations) the charge carrier can tunnel into the dot and depending on its spin, it gets loaded on the ground or excited state. This by itself is not indicative of the spin state of the system. However, the excited state has a relaxation time that can be detected with a change (**blip**) in the reservoir signal. As a consequence, the logic says that if this small signal is detected, then the carrier is loaded in the excited state, and if nothing is detected, then the carrier is always in the ground state. This technique is called **Elzerman readout** and it was demonstrated first by Elzerman et al. in 2004 [85]. In Figure 6.5 a, the visual representation of the spin-to-charge conversion is demonstrated.

The second spin-to-charge method requires a double quantum dot in the few-carrier occupancy and thus is more challenging. To simplify the discussion, the example of a two-electron double quantum dot will be used. If the two electrons are under the same plunger gate, the two electron spins are aligned in any possible configuration. However, moving from the random spin configuration to the restricted single side with two electrons, the electron spin cannot always tunnel while keeping its spin property. This technique is called **Pauli Spin Blockade** (PSB) and is widely used on singlet-triplet qubits [86].

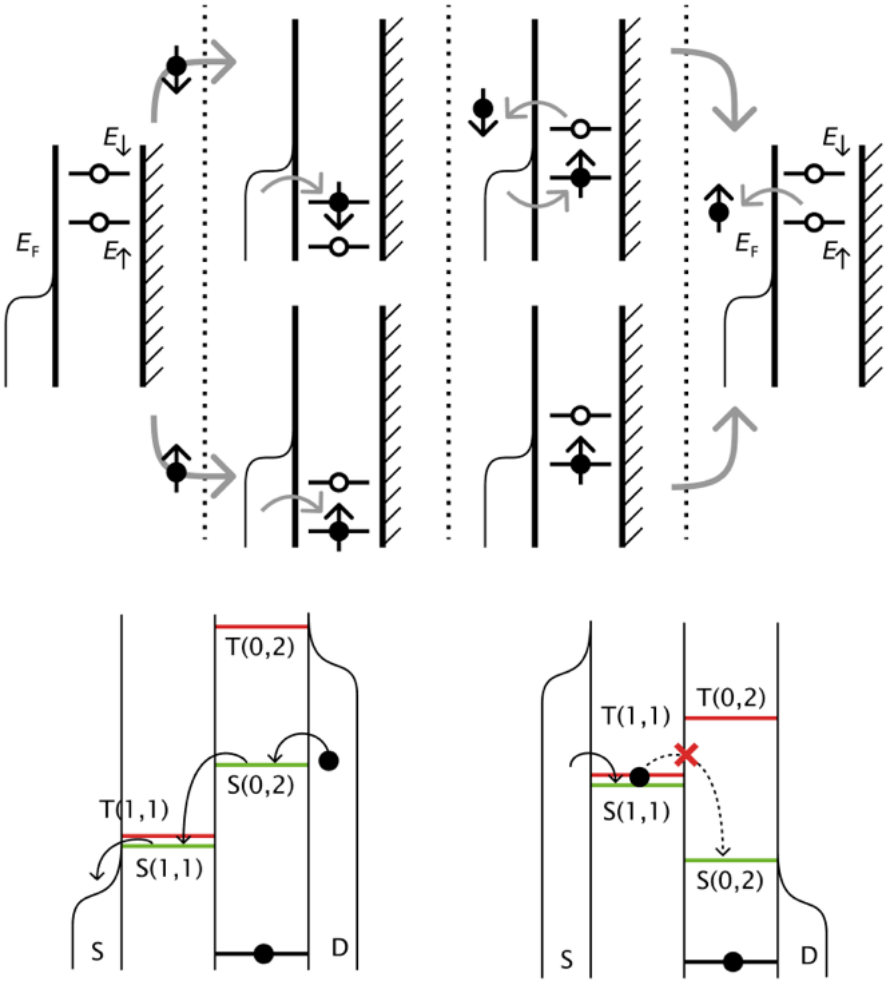


Figure 6.5: Spin-to-charge conversions in (a) single and (b) double quantum dots. In (a), a charge carrier tunnels in the dot either in spin up or down and occupies the ground or excited state, respectively. With a pulse and a waiting time, it is possible to detect or not a loading of another electron in the system. This signal in current is translated to spin. In (b), a double quantum dot is required if it has the same spin as the one that is occupied in the quantum dot. Then, due to Pauli's exclusion principle, it is blocked, and cannot tunnel.

6.3 REFRIGERATORS

In this thesis, the electrical characterisation of quantum devices is heavily based on the so-called dry fridges. This means that all cryoliquids are contained in closed-cycle lines and under regular conditions, there are no losses. The two refrigerator technologies that are employed in this thesis are the adiabatic demagnetization and the dilution unit. The former utilises weak paramagnetic materials that due to entropy conservation act as heat sinks and the latter is based on the physical properties of the He isotopes. Both setups have multiple cooling stages to reduce the heat load on the sample region. Also, both systems, from room temperature, are cooled firstly by a pulse tube connected to a compressor. This is a standard closed He circuit under high pressure that precools at approximately 4 K.

Dilution refrigerator

In 1951, H. London proposed the working principle of a dilution refrigerator at Oxford LT meeting. More than a decade later, the first unit in operation was built at Leiden University, reaching 220 mK [87]. The non-availability of ^{3}He hampered early realizations of a dilution refrigerator. Nowadays, the main source of the isotope comes from the military. Tritium is used for atomic bombs, but luckily for humanity, it has a half-life decaying time of 12.5 years, after which it becomes a stable ^{3}He isotope that can be used as cryoliquid. Even though politics play an important role, many companies in the Western world have been established, making the installation and operation of such cryostats a trivial procedure.

The principle of a dilution unit is based on the extraordinary properties of helium. There are two stable isotopes of He, the fermionic ^{3}He and the bosonic ^{4}He. At the limit of 0 K, ^{3}He has 6.4% solubility into ^{4}He. In practice, a ^{3}He atom is more strongly bound into pure liquid ^{4}He than into pure ^{3}He. Using the phase diagram of helium-isotope mixtures, the thermodynamics behind the operation of a dilution unit are explained. For a comprehensive explanation of the principles of a dilution refrigerator, the reader may refer to [87] and to the respective manual of the refrigerator that they are planning to use.

Some of the requirements for a closed-cycle dilution refrigerator are listed below:

- Low pressures with complex pumping systems.
- Safety valves to avoid blocks and securely store exchange gasses.
- A cold trap that acts as a purifier of the mixture. It is cooled by LN2 and the vessel contains activated charcoal, so any other gas freezes on the surface before it moves in the lines of the dilution unit that could potentially block them.

- Leak detectors to detect leakage of mixture.

In the experiments involved in this thesis, dilution refrigerators from two companies were used. Their principle is the same, and their operation temperature is similar, but the interface of each apparatus is different. Both systems use bottom loaders for fast and efficient puck exchange. The first is a *Bluefors BF-XLD400*, and the second is an *Oxford Instruments Triton 400*.

Adiabatic demagnetisation refrigerator

Adiabatic demagnetisation refrigerators (ADR) are significantly older than dilution refrigerators. Their principle is based on the magnetic properties of specific materials acting as heat sinks to the cooling target. Two types of ADR are distinguished in terms of operational temperature ranges. Standard ADR uses weak paramagnetic salt cores and relies on the demagnetisation of electron shells in the crystal. The achievable temperatures are reaching to few mK. On the other hand, nuclear-ADR employs nuclear magnet cores and utilises the demagnetisation of the nuclear spins. This technique is combined with dilution refrigerators and can reach temperatures as low as few μK. Record-low temperatures have been achieved by two nuclear demagnetization stages in cascade with rhodium at approximately 100 pK in Helsinki, 1999 [88].

In its essence, ADR requires an external magnetic field, a material for the demagnetisation, a pre-cooling bath and heat switches. The external magnetic field first magnetises the dipoles of the atoms, thereby decreasing the entropy and heat capacity of the material. This causes the core to heat up. While the magnetic field is held constant to prevent the dipoles from reabsorbing heat, the excess energy is dissipated at the pre-cooling bath. Once the core and the thermal bath reach thermal equilibrium, the heat switches isolate the core and the sample from the environment. Then, the magnetic field is adiabatically swept down, causing the magnetic moments to overcome the field (i.e., stay aligned), and the sample cools down (adiabatic demagnetization). Thermal energy from the sample stage is transferred to the magnetic moments of the core, causing demagnetization and, in parallel, cooling the sample. At a zero magnetic field, the magnetic dipoles are random again, and a single ADR cycle is completed.

Focusing more on the ADR system of this research, a continuous-ADR (cADR) Kiutra * L-type rapid cryostat is employed. It has a base temperature of 100 mK in one-shot mode and continuous operation at 300 mK. It is common to mistakenly assume that the 300 mK operation utilises ^{3}He for cooling. However, only a pulse tube and a helium compressor are used for pre-cooling at 3.2 K. Below that limit, the operation is solely based on the paramagnetic salts (Figure

* Pronounced [kɪuːtrɑ] and not [kaɪuːtrɑ]

6.7 a). The continuous operation is based on two paramagnetic salts with individual magnets coupled in series. Once the first core is depleted, the second is deployed, while the first is recharged. The system heavily depends on the operation of mechanical switches. In Figure 6.6, the cryostat itself, its internal components, as well as the puck are presented. In Figure 6.6 b, the sample magnet and one of the ADR magnets are visible. The system was open for maintenance and the main stage was uninstalled from the middle of the plates. The detached sample stage is presented in Figure 6.6 c. Electrical connections, including 40 DC ports and 4 RF lines, comprise the measurement capabilities.

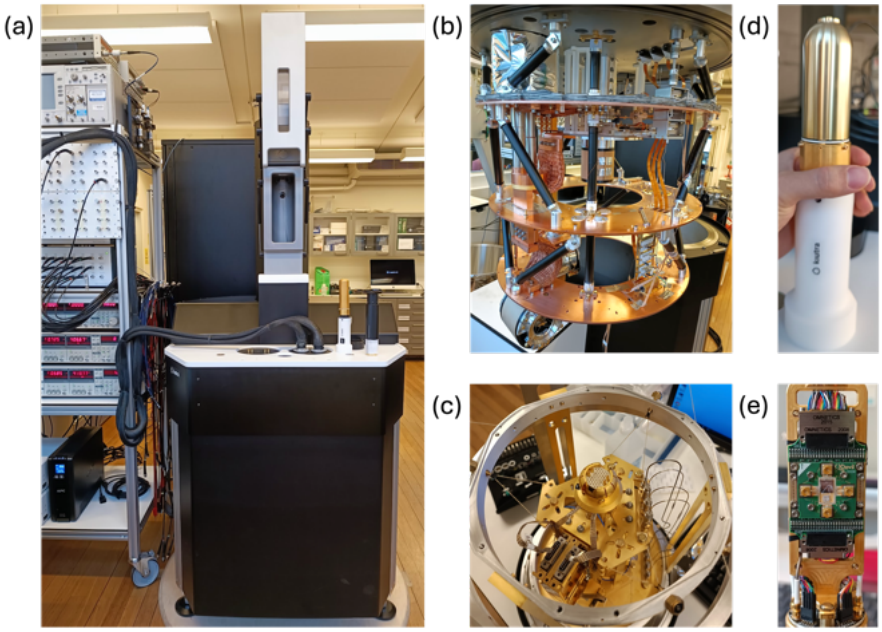


Figure 6.6: The Kiutra L-type cryostat. (a) The cryostat in the lab with the loadlock gate open. On the left, the measurement rack is partially visible and behind the cryostat control rack is installed. (b) The cooling stages of the cryostat. On the low left corner, one of the ADR magnets is visible. (c) The sample stage of the cryostat. (d) A closed puck before loading. (e) An open puck with a QBoard and a chip mounted.

The operation of a cADR cycle is illustrated in Figure 6.7 a and described below. Both ADR units are magnetized ($B_{ADR1,2} = 4T$) with all heat switches closed, maintaining the temperature set by the cryocooler (T_{base}). **Unit 2** is then decoupled and demagnetized, effectively cooling the sample stage to the desired operational temperature T_{op}. Before the end the cycle of **Unit 2**, **Unit 1** is disconnected from the cryocooler and demagnetized, resulting in a temperature lower than T_{op}. This imbalance results to a sub-mK disturbance† of the system during the recharging of **Unit 2**. Once **Unit 1** is depleted, the connec-

† Based on the temperature sensors of the refrigerator

tion between the units is reopened, and **Unit 1** is regenerated by the cryocooler. This cyclic process can continue indefinitely. We have performed experiments lasting more than a month without disruptions.

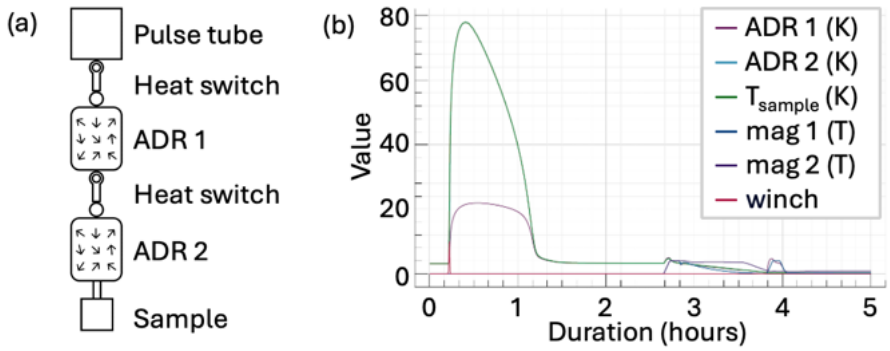


Figure 6.7: (a) The configuration of the cADR unit. (b) A plot with the temperature and magnetic field values in a cooldown of a puck using the automated loadlock.

Closing, the most remarkable feature of the system should be highlighted. The loading mechanism is completely automated, requiring only inserting the puck in the loadlock and pressing the **Load** button. Built-in turbo and scroll pumps take care of the vacuum conditions prior to loading. An automated script ensures the safe transfer of the puck from the load lock on the stage. The experimentalist is released from the burden of manual loading and can relax while the sample cools down. After approximately **one hour**, the sample is already thermalised with the cryocooler at 3.2 K and can initiate the ADR for further cooling. In Figure 6.7 b, the cooling diagram demonstrates the described efficiency. After loading, the stage is heated by the room temperature puck above 70 K. After approximately one hour, thermalisation is achieved, and it is possible to initiate further cooling. During this waiting time, it is possible to document and run the first diagnostic tests on the quantum device. It is possible to queue the ADR cooling, but in the case of Figure 6.7 b, it was initiated manually. This is the reason that the time span of the cooling was 4 hours, and it can easily reduced below 3 hours.

Some closing remarks about the further capabilities of the system arise from conversations of the author with the Kiutra team. For example, adding a third ADR unit to the system with a third magnet is motivated by the limited cooling benefits it provides, which fails to justify its addition as an efficient solution. Furthermore, the presence of paramagnetic salts imposes constraints, as at sufficiently low temperatures, they transition into either diamagnetic or ferromagnetic states, thereby restricting the achievable minimum temperature.

6.4 MEASUREMENT METHODS

DC measurements

DC measurements are an essential part of the initial screening of quantum devices. In this thesis, they are performed either by solely using the QDac-II or with a combination of QDac-II and a digital multimeter (DMM). Regardless of the setup, all instruments are connected to an acquisition computer and traces are acquired via QCoDeS, a Python-based data acquisition framework ‡. Every measurement trace is meshed, and each measured datapoint returns to the acquisition computer before taking the next one. The continuous communication of the instrumentation and the control computer increases significantly the duration of a single trace measurement. More advanced protocols by sending triggering pulses to the instruments and communicating only at the beginning and end of each measurement contribute to a shorter acquisition time.

Even though it is possible to reduce the duration of each measurement, the setup acquires data at a slow rate. The intrinsic limitations of this method make it inevitable to move towards faster measurement techniques such as Radio-frequency reflectometry. Before moving to the next technique the physical limitations of the DC measurements will be reviewed.

First, the *integration time* (t_{int}) of the DMM is the averaging time of the input signal. The transient fluctuations are smoothed out, resulting in less noisy and more reliable measurements. The experimentalist can select their suitable integration time, which is a balance between the noise of the system and the available laboratory time. On top of this time, the communication between the acquisition computer (t_{comm}) and the DMM increases the measurement duration. Last, the regular 1D sweep from **QCoDeS**, called **do1d**, has an additional delay time (t_{delay}) between each datapoint. In total, the measurement time of a 1D trace (t_{total}) with N datapoints can be expressed as $t_{total} = N \cdot (t_{int} + t_{comm} + t_{delay})$. With the more complex buffered acquisition techniques, this time can be reduced to $t_{total} = N \cdot \tilde{t}_{delay}$, where $\tilde{t}_{delay}$ is the time between each measurement inside the DMM with $\tilde{t}_{delay} \leq t_{int}$.

A second limiting factor of a DC measurement has to do with the wiring of the setup. All cryostats in the lab are equipped with RC/LC QFilters providing cut-off frequencies at 65 kHz and 225 MHz, respectively. In addition, the motherboard also includes RC low-pass filters with $R_{LP} = 1.2k\Omega$ and $C_{LP} = 1nF$ providing a total cut-off frequency of approximately 30 kHz.

‡ **QCoDeS** was developed by the **Q**uantum computing consortium between **Co**penhagen, **De**lft, and **S**ydney Universities and Microsoft.

Leakage matrix

The QDac-II tool has source-measurement capabilities making it an ideal candidate for initial device screening. A script can program the tool to address all the electrodes of the device and measure the resistance between each element. This reduces the time spent on diagnostics, identifies possible errors in the setup and produces consistent data. Even though it is called *leakage matrix*, it is quite misleading since it cannot identify leakages between the electrodes. Rather, it can identify shorts and, in general, conductive paths. Thus, names such as **shorts matrix** or **conductance matrix** are far more suitable. Technically the method that is followed to identify leakage is by sweeping the gate voltages on extreme values and recording the gate current. Once the current increases exponentially, the breakdown voltage of the dielectric is observed. In the case of the leakage matrix, small steps of maximum 5 mV are applied when the ohmics are included in the dictionary, whereas the dielectrics can endure up to a few V.

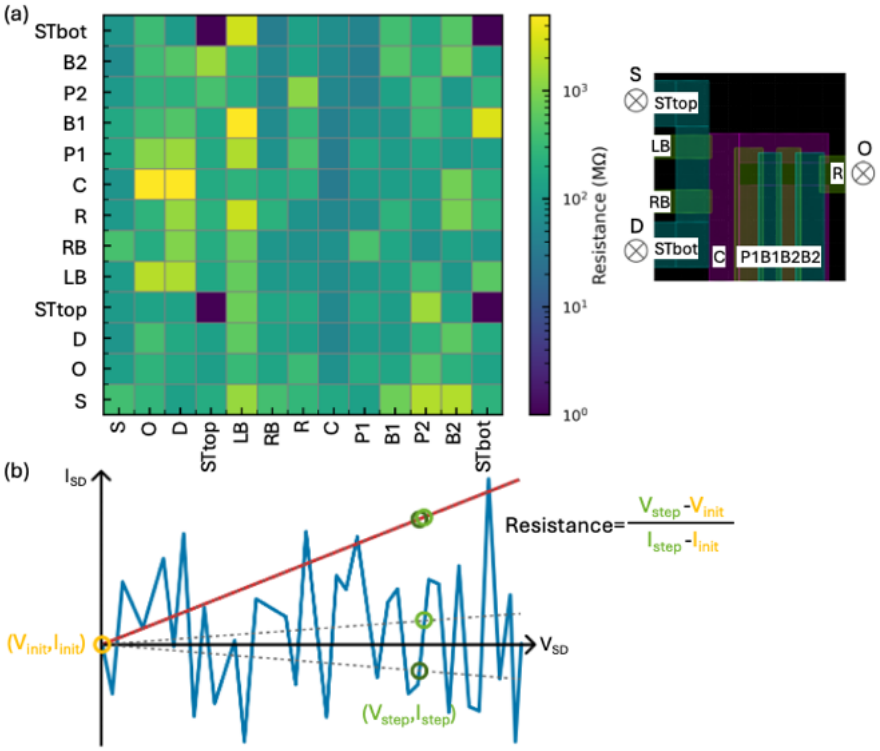


Figure 6.8: (a) A leakage matrix of a foundry fabricated SiMOS quantum dot. By design, the STtop and STbot gates are shorted, as indicated by the dark blue conductive pixels. (b) IV curves describing the method to extract the matrix elements. Only two points are needed in the leakage matrix algorithm to calculate each pixel. From electrodes with ohmic characteristics, the matrix elements can be accurately measured. The calculation fails for highly resistive samples.

In its core principle, the leakage matrix contains a dictionary with all the electrodes that will be addressed and a step voltage that will be used to evaluate the resistance. The most reliable method to calculate the resistance is by taking an IV curve and fitting Ohm's law. However, taking a line trace increases significantly the duration of the experiment. Thus, the resistance of each element is calculated only with two datapoints. The first is the initial value that the electrodes are set (V_{init}, I_{init}) and the second is set by the step value $(V_{step}+, I_{step})$, where $V_{step} = V_{init} + \text{step}$. For N electrodes, an $N \times N$ table with all the conductance combinations is extracted. This table can be repeated for any gate configuration (while the device is on or off) and can be acquired in less than two minutes. In principle, the table is expected to be symmetrical over the main diagonal. However, due to high resistance and high fluctuations, the accuracy of the conductance of an open circuit is low. In Figure 6.8 b, the qualitative difference between a highly resistive and a finite resistive channels is given. The fluctuations of the highly resistive plot fail to give a good estimate of the resistance. For example, small shifts on the voltage axis can result in a large deviation of the resistance values (fits between the dark and light green points). This is not the case for the electrodes exhibiting ohmic behaviour. However, one should not worry about that, since it only means that the gates are highly resistive as expected.

Lock-in measurements

Closing the DC measurement methods, another technique used in this thesis is based on the lock-in amplifiers. Hall bars and bias spectroscopy of quantum dots employed this technique. In both cases an AC signal of a frequency below 150 Hz was used to probe the quantum device. First, a voltage divider reduced the input signal by 10^{-5} and from the drain of the device, an I/V converter with a typical amplification of 10^7 returned the signal to the lock-in for homodyne detection [89]. Only the signal with the exact input frequency is addressed. Although lock-in measurements are robust, they are time-consuming. A very important feature of the measurements is that, in contrast to the DMM setup where the measured component is current, in the lock-in techniques the measured component is the differential signal.

In practice, in Coulomb blockade spectroscopy of a DMM and a lock-in, the latter is the derivative signal of the former. This means that the current signal switches from positive to negative, whereas the amplitude of the lock-in stays positive for both positive and negative bias voltage values.

Hall bars require multiple lock-in amplifiers to detect the transverse and longitudinal components. The signal of the sourcing lock-in is distributed to the rest of the secondary lock-ins to perform homodyne

detection at the same frequency. In Figure 6.9, a schematic of a DC setup is presented, including the described instrumentation. The DC and AC setups can operate simultaneously.

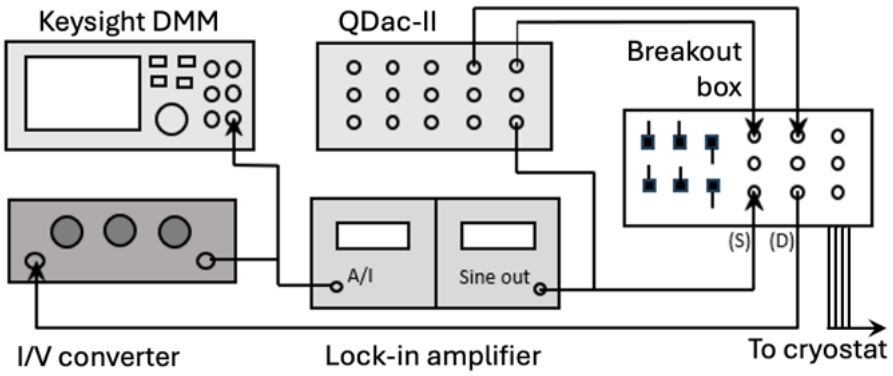


Figure 6.9: Schematic of a DC setup with a combination of DMM and a lock-in amplifier. QDac-II provides the voltage-bias DC sourcing.

RF Reflectometry

In its core principle, a high-frequency signal excites a tank circuit and the reflected signal is recorded. The tank circuit is connected to the quantum dot device, and by changing the resistance (impedance) of the device, the circuit changes its response to the excitation signal. This thesis will not dive into the details of RF reflectometry. The author guides the curious readers to the elaborate review of Reference [90].

One qualitative difference between RF and DC traces is that when the device is off, no DC current is observed, and once the device turns on, a positive current is recorded from source to drain. On the other hand, in RF reflectometry, the on and off state have to do with the response of the device to the tank circuit. If the device is off, then the signal is reflected and a resonance frequency is observed on the spectrum. When the device is in saturation, the signal is dissipated, and no response from the tank circuit is observed. this is also translated from a low signal to a higher signal, but there is not a zero value similar to the DC measurements. Also, depending on the I/Q configuration of the setup, it is possible that instead of an increase, the device turn-on can be observed as a decrease in signal response.

For the homebuilt demodulation setup, an RF signal generator source is required to provide the RF signal. A directional coupler splits the signal into two sides for the readout and the input of the refrigerator. The initial power of the signal is high, and an attenuator reduces it. On the ports of the refrigerator, high and low-pass filters are used to cut off unwanted signals outside of the range of interest. From the reflection port, the signal is amplified and fed through the mixer, where the DC component (I) is obtained and measured by a DMM. Similar to the lock-in amplifier that measures **X and Y**, this method measures **I and Q** components. Since the presented setup

measures only I, a phase shifter should be used at the input signal to identify the maximum amplitude. A schematic similar to the one described in this paragraph is presented in Figure 6.10 a.

More sophisticated setups contain the components internally, making the life of the experimentalist easier by avoiding additional troubleshooting of each component. It can be also seen as a black box that is connected to the transmission and reflection ports of the refrigerator and configured via an online interface. A **Rohde & Schwarz vector network analyzer**, a **Zurich Instruments ultra-high frequency lock-in amplifier UHFLI 600 MHz**, and a **Quantum Machines OP-X+** are the most common instruments in the *Center for Quantum Devices* to perform RF reflectometry with.

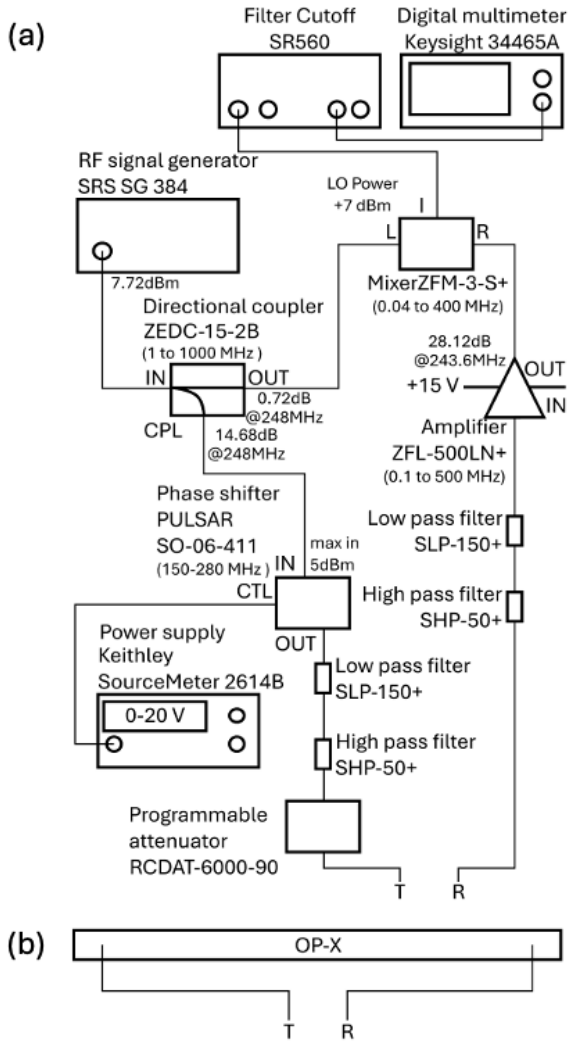


Figure 6.10: Schematics of RF setups. (a) Homebuild demodulation setup with a frequency bandwidth of 100 MHz. (b) The OP-X+ setup. The RF signal is supplied to the transmission line (T) of the cryostat and the reflection line (R) line provides the signal for demodulation.

6.5 SETUP WIRINGS

In this section, the RF and DC wiring of **Bluefors BF-XLD400** is discussed (Figure 6.11). In Appendix B the wirings of the other two refrigerators are given. All setups use the same cryogenic filtering and PCB configurations. All the lines are thermally anchored on each plate for thermalisation. On the motherboard additional RC filters and bias tees are used for DC and RF addressing of each line. The motherboards and daughterboards are provided by QDevil.

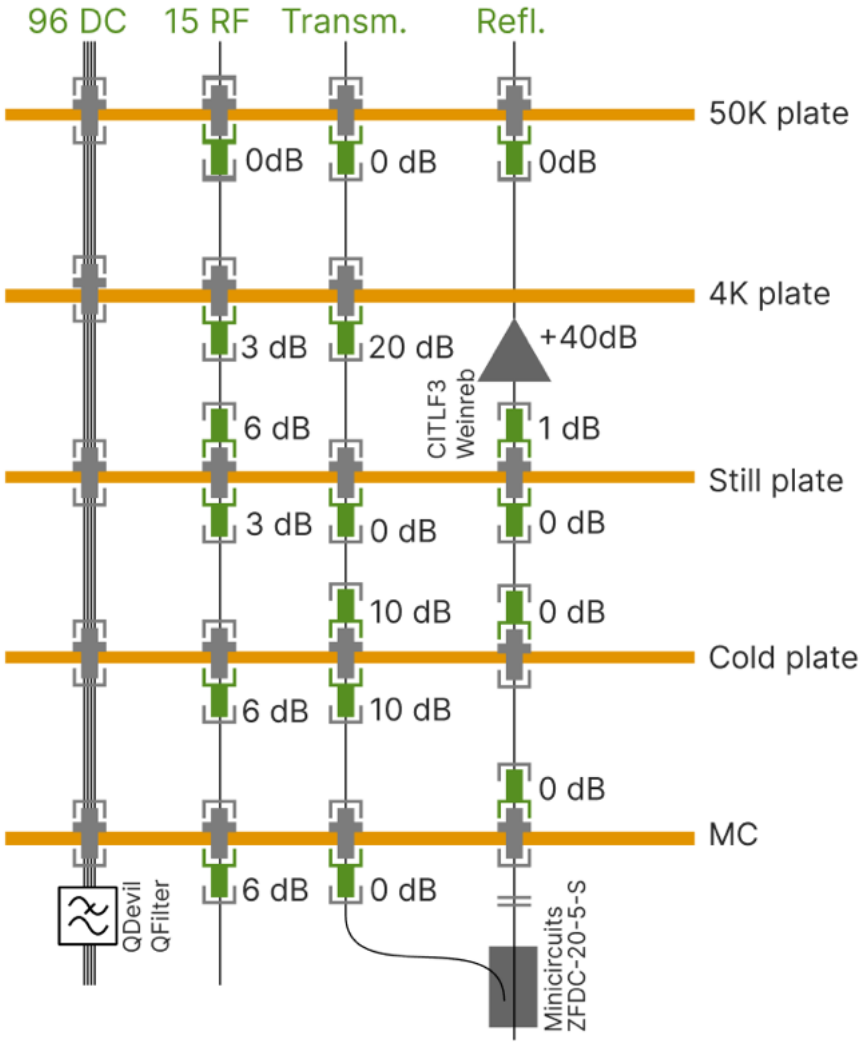


Figure 6.11: The Bluefors BF-XLD400 wiring. For DC lines, the thermal anchoring on each plate is indicated by the grey brackets.

6.6 EFFICIENT CRYOGENIC FEEDBACK

Successful device fabrication is not only determined by visual inspection but, more importantly, electrically. The workflow discussed here was featured in a poster presentation at *Cryocourse 2023, Helsinki* and *Silicon Quantum Information Processing Workshop 2023, Glasgow*.

Using a dilution refrigerator is both time consuming and expensive to run such tests. At this level, a more efficient feedback loop was developed to provide important insights. The necessary workflow is listed below. It was initially inspired by Reference [82] and developed further by our experience in the lab.

- Test for electrical shorts within gate electrodes
- Test for turn-on behaviour active device regions
- Quantify electrical leakage between gate electrodes
- Confirm ohmic behaviour of device contacts
- Confirm isolation of each transport channel
- Coulomb blockade of quantum dots sensors
- Evaluate charge sensitivity of sensor dots (DC)
- Verify single-charge occupation within qubit dots
- Evaluate high-frequency response for reflectometry

The cADR **L-Type Rapid** cryostat has both DC and RF capabilities, making it an ideal candidate for fast characterisation feedback. It is equipped with 40 DC lines, 2 high-frequency control lines and an RF reflectometry wiring. All lines are attenuated and thermally anchored on each refrigerator stage to minimise the heat load and thermal radiation effects. In Appendix B the schematic of the wiring of the cryostat is provided (Figure B.6). Once all the criteria are fulfilled, the device can be unloaded and further used for experiments in a dilution refrigerator.

Transferring the device from one setup to another is a notorious procedure. Experimentalists often claim that their devices might suffer from electrostatic discharge (ESD) events where two or more gates might get shorted due to excessively high voltages discharging directly to the leads. EDS protection equipment is usually sufficient to avoid such catastrophes. Overall, it is essential to keep the sample grounded as much as possible and transport it as little as possible. One peculiarity of the cARD **L-Type Rapid** cryostat that puzzled many colleagues is that the DC pins of the puck are electrically floating while loading or unloading. Based on our day-to-day experience and

the multiple tested devices (successful and failed), we can extrapolate that if the device is intact before the loading process, it can be loaded and unloaded several times without ESD events. Thus, we conclude that loading or unloading is not detrimental to the device.

Once the device is at the base temperature in a dilution refrigerator, we employ a similar characterisation protocol to identify the success of the transfer. With prior knowledge from the cADR L-Type measurements, reaching the few-electron regime is easier and faster. Most of the devices were investigated in an **Oxford Instruments Triton 400**. The capabilities are higher, with 48 DC lines, 16 high-frequency control lines and an RF reflectometry wiring. Moreover, the setup is equipped with an OP-X+, an FPGA (Field-Programmable Gate Array) with real-time computational capabilities [91, 92].

7

ELECTRICAL CHARACTERISATION

Through this thesis, the preparation of a quantum device has been described, from the point of receiving the wafers from a manufacturer to loading the quantum device into a refrigerator. The theoretical motivation for the measurements is already established, and the main experimental findings are discussed in this chapter. Measurements of Hall bar and quantum dot devices are presented, along with valuable experimental techniques and metrics. The material platforms employed in this study are heterostructures of Ge/SiGe and Si/SiGe, as well as foundry-based SiMOS.

With this chapter, the results of this reading conclude. In principle, the electrical characteristics of the Ge/SiGe heterostructures could potentially provide valuable insights for further optimisation of the growth qualities. Moreover, we address the challenges of the fabrication of Si/SiGe heterostructures and present the characterisation of SiMOS quantum dots.

The author primarily measured the presented quantum devices. Contributions from students and colleagues are listed as follows. For the Ge project **Johanna Malina Zeiss** under the supervision of the brilliant **Will Lawrie**, obtained the data while the author was absent due to the change of academic environment. The SiMOS results were obtained in different stages by multiple contributors, such as **Anton Zubchenko**, **Ida Vaaben Ladeford** and **Agnete Larsen**. In all the stages **Fabrizio Berritta** was on the side advising on strategies and providing his valuable insights. The Si/SiGe results were taken primarily by the author, and **Ida Vaaben Ladeford** and **Agnete Larsen** provided valuable contributions and wonderful time in the lab.

7.1 HALL CHARACTERISATION

For the characterisation of quantum wells, carrier mobility is commonly used to evaluate their electronic properties. Typically, the reported mobility, also known as **peak mobility** μ_{max}, corresponds to the maximum mobility achievable across the explored carrier density range. This can be achieved in a 2D system by sweeping the top-gate and recording the magnetoresistance along the longitudinal (R_{XX}) and transverse (R_{XY}) directions of the Hall bar (xx and xy directions). Several publications in the literature underscore the achievement of *high* [36, 37, 40], *very high* [93, 94], and *ultra-high* [33, 34] mobility. However, when considering spin qubits and their footprint, it may not be the most relevant metric.

Spin-qubits hosted by semiconductor quantum dots operate in a low carrier density regime, which is significantly offset from the peak mobility carrier density regime. While high-quality structural and electronic properties are essential, peak mobility is a feature that cannot be exploited in our applications directly. It is recognized that 2D systems, like the ones we investigate here, undergo a 2D metal-insulator transition that is a density-inhomogeneity-driven percolation transition [95]. Each device has a minimum carrier density corresponding to the metal-to-insulator transition. This metric, known as **percolation density** p_p, is particularly relevant to quantum dots of low occupancy and provides a critical figure of merit in assessing their performance.

Scattering mechanisms

Any effect resulting in carrier momentum relaxation is classified as a **scattering mechanism**. By investigating mobility as a function of carrier density, multiple regions with different slopes can be distinguished. The changes in the dependence arise from the contributions of the scattering mechanisms that limit mobility at different carrier density regimes. The individual contributions are summed up and described by Matthiessen's rule [45]:

$$\frac{1}{\mu} = \frac{1}{\mu_{RI}} + \frac{1}{\mu_{SD}} + \frac{1}{\mu_{UBI}} + \frac{1}{\mu_{VS}} + \frac{1}{\mu_{AS}} + \frac{1}{\mu_{IR}} + \frac{1}{\mu_{TD}}, \tag{7.1}$$

where the indices are described in Table B.2. At low temperatures, optical and acoustic phonon scattering is suppressed. In the dependence of mobility as a function of carrier density, regions where the slope remains constant are fitted with a power law $\propto p_{2DHG}^{\kappa}$. The exponent κ indicates the primary scattering mechanism in the system. The discussion of mobility evolution with carrier density is based on the work of Montoer et al. [96]. Table B.2 presents the suggested scattering mechanisms and their corresponding exponent. These details are used

later in the experimental analysis to identify the limiting contributions in the system and provide feedback for future crystal growths.

Scattering mechanism	Symbol	κ_{low}
Remote impurities	RI	1.5
Strain distributions	SD	1.5
Uniform background impurities	UBI	0.5
Vicinal surfaces	VS	0
Alloy scattering	AS	-1
Interface roughenss	IR	-1
Threading dislocations	TD	-1.5

Table 7.1: Scattering mechanisms based on Reference [96]. A power law fits the mobility curves as a function of carrier density. The exponents are associated with a dominant scattering contribution.

Remote impurity scattering is caused by localised dopants (in the form of delta doping) outside the 2D carrier region. Also, literature associates this mechanism with scattering from remote impurities at the interface between the dielectric and the semiconductor [97]. For shallow heterostructures, such an effect may have a significant impact since the quantum well is close to the surface. The carrier density evolves with an exponent of 1.5 or higher [29].

A similar carrier density dependence is observed from **strain distributions** arising from inhomogeneities in the array of misfit segments. This model assumes 60° dislocations, which also corresponds to the crosshatch patterning of the heterostructures reviewed in Part i of this thesis. Even though literature refers to the exponent of 1.5 as *remote impurity scattering from the interface between the semiconductor and the dielectric* [29, 97], it would be reasonable to assume that strain effects may play an important role. Even though multiple and thick buffer layers are used to eliminate misfit dislocations and reduce the dislocation density, it is obvious that if a crosshatch occurs, this mechanism should be taken into account.

The conceptualisation of remote impurity scattering is based on delta doping. By extending the delta peak to a uniform distribution, the mobility-limiting mechanism is considered to be scattering from **uniform background impurities**. Their density is significantly lower in comparison to the remote impurity mechanism, but they are present across all layers.

Reducing the exponent of carrier density to a horizontal line with constant mobility over the carrier density **vicinal surface scattering** is observed. In that case, *vicinal surfaces*, an intrinsically morphological feature of the wafers by the manufacturer as well as *step-bunches* by lacking the control of the *Ehrlich-Schwoebel barrier* (chapter 2.1.2) may

result into scattering. Although this mechanism is relevant in the cases of surface transport, shallow quantum wells may also be influenced.

Alloy scattering is another mechanism that should be negligible inside the pure quantum well. However, especially after device fabrication, the wafer undergoes a lot of thermal treatment, and additional strain is put on the heterostructures from the deposited metallic gates. Also, the finite barrier height at the quantum well interfaces means that the wavefunction extends into the $Si_{0.2}Ge_{0.8}$ spacers. All these reasons make it likely that additional Si atoms can be present in the quantum well region and cause scattering from alloy atoms.

Expanding further the idea of a gradient transition between the spacers and the quantum well, **interface roughness scattering** is usually observed at higher carrier densities. The carriers of the highly accumulated quantum well penetrate into the spacer, limiting mobility with an exponent of -1, similar to the alloy scattering. Moreover, any deviation from an ideal sharp interface may enhance the scattering due to interface roughness.

Last, the role of **threading dislocations** can be detrimental to the electronic properties of the quantum well. The exponent of -1.5 is indicative of the weight of the detrimental effects that this scattering mechanism can have on mobility. The reduction of threading dislocations is achieved by thick buffer growths and layers that can trap the dislocations or guide them away from the active region [98].

The review of the scattering mechanisms aims to highlight the significance of the transport-to-growth correlation. Emphasis is given to identifying the limiting mechanisms in the electronic properties. By conceptualizing crystal growths that are directed away from the specified limitations, it is possible to enhance the electronic properties. It is important to note that even though the exponent may indicate a primary contribution, multiple scattering mechanisms are present, making the analysis more difficult. Intricate models are built based on the material parameters to fit the entire carrier density range and identify the system limitations. This is a quite rigorous process and it will be omitted here. Figure 7.1 presents an intuitive illustration of the scattering mechanisms in a Ge/SiGe heterostructure.

Peak mobility

For the extraction of the peak mobility, the current across the Hall bar I_{SD} is required to be constant and only low magnetic fields are required for these measurements. The transverse ρ_{XX} and perpendicular ρ_{XY} resistivities are calculated based on the geometric factor L/W of the device geometry, where L is the distance between the XX leads and W is the width of the Hall bar. The slope of ρ_{XY} in the magnetic field domain is required to extract the 2D carrier density(p_{2DHG}, where

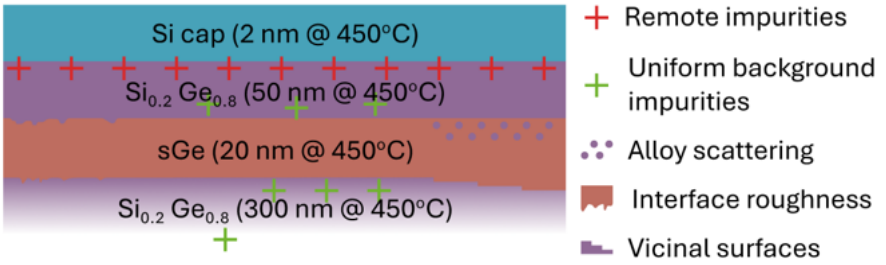


Figure 7.1: Illustration of the scattering mechanisms for a Ge/SiGe heterostructure. The identification of each mechanism is successful by assuming the morphological conditions of the device based on the structural characterisation and the fitting results of mobility as a function of carrier density.

the 2DHG index indicates holes as the charge carriers. Finally, for the particular gate voltage (or carrier density) that the magnetoconductance is obtained and the carrier mobility can be calculated as $\mu_{max} = \frac{1}{p_{2DHG}\rho_{XX}e}$, where e is the elemental charge. The repetition of the same measurement from the pinch-off to the saturation of a gate trace can reveal the peak mobility of the system.

On the other hand, the extraction of the percolation density follows the same experimental process, but the analysis differs. The focus is only on the data, where the perpendicular magnetic field is zero ($B_\perp = 0$). Instead of plotting the resistivity, the interest is inverted to the longitudinal conductivity σ_{XX}. Fitting the data with the percolation theory function $A(p_{2DHG} - p_p)^p$ the extraction of the percolation density p_p is possible. The exponent p is an indication of the 2D conductivity nature of the system, with an ideal value of 1.31 [99]. Experimentalists fit the data with the exponent either floating and or fixed at the ideal value. In this thesis both cases are explored.

7.1.1 *Ge/SiGe MBE Hall Bars*

The germanium heterostructures of Part i require thorough characterisation as they are the first reported undoped quantum wells produced by MBE. Moreover, motivated by the TEM and AFM analysis, the correlation of surface morphology with respect to the electrical properties was attempted. In this study, due to the fabrication challenges, only the heterostructure named **Sample 6** was investigated. All the measurements presented in the following analysis were taken at the base temperature of a dilution refrigerator at approximately 8 mK and employed voltage-bias lock-in techniques. A small AC excitation together with a DC voltage were applied to the source of each sample.

Three Hall bars were characterised in terms of magnetic and electric fields. The magnetic field was swept from -100 mT up to 6 T. The gate voltage was swept from a regime where each of the Hall bars was non-conducting to the voltage at which conductance saturated. One limiting factor in these measurements was the fabrication failure modes. A source-drain reservoir in two out of the three Hall bars was non-operational. To circumvent this issue, we used one of the voltage probes as a drain. In principle, the topology of the system stays the same and should not influence the transport. The two devices were compared with the fully functional third one to verify the validity of this claim. The electrical properties revealed similar features.

In Figure 7.2, false-coloured large-scale optical images of a typical Hall bar, together with the schematics of each measurement configuration, are presented. Each column corresponds to one of the measured devices (**Device 1**, **Device 2** and **Device 3**). The aspect ratio of the L/W is approximately 1, and the top-gate is separated from the surface by 9 nm of Al_2O_3. More details about the design and fabrication have already been discussed on chapter 5.1 In Figure 7.2 b, the leakage matrices highlight the accumulation-mode feature of the devices since the pixels of these plots are above the MΩ range. The top right 2×2 pixels correspond to the two shorted sides of the top-gate. Each device has unique turn-on characteristics due to the failure modes mentioned earlier.

Initial screening displayed in Figures 7.2 d-i was performed with the **QDac-II**, a digital-to-analogue converter which is equipped with source-measurement units. In this way, it was possible to keep track of the leakage for each probe and gate while sweeping the voltages. Once the turn-on and saturation points were identified for each device, the initial QDac-II wiring was switched to the standard lock-in configuration as displayed in Figures 7.2 a-c. Then, repeating and verifying the turn-on with the new setup, the magnetotransport measurements were commenced.

Regarding the results of the screening, **Device 1** had a probe that did not turn on. **Device 2** had one of the reservoir leads (in the figure

denoted by *S*) shorted to the top-gate. To successfully perform the Hall measurements, that lead is disconnected from the DAC and is floating at the breakout box to eliminate leakage. Thus, only five curves are obtained at the device turn-on. Last, **Device 3** was the only device that the leakage matrix and the turn-on characteristics were functioning.

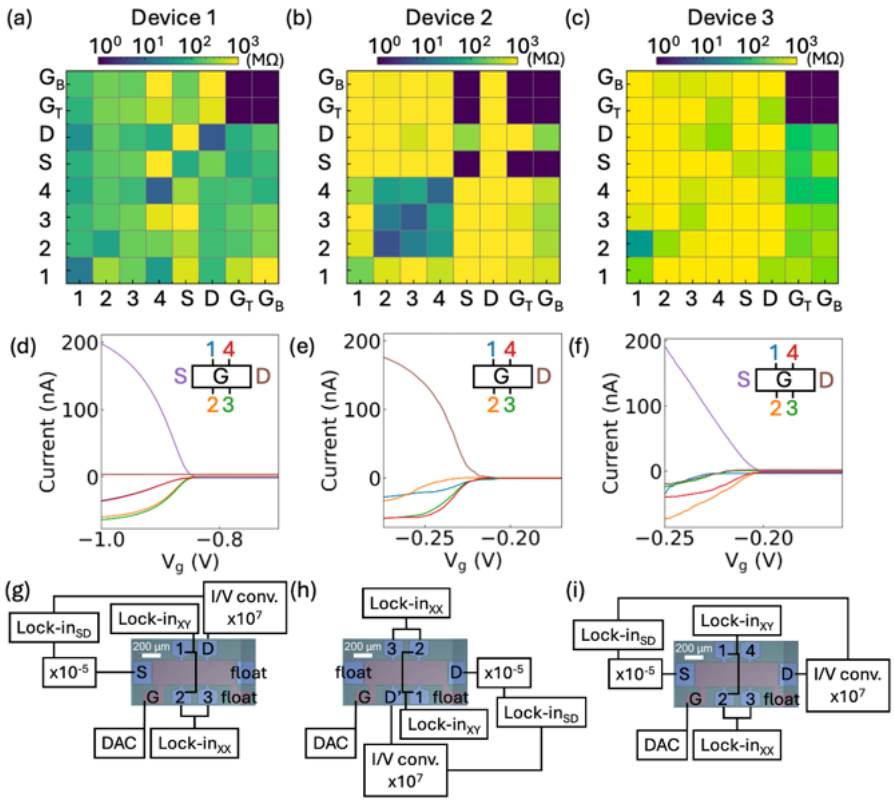


Figure 7.2: Screening of germanium Hall bars and lock-in measurement configuration. Three devices were investigated: Device 1 in (a, d, g), Device 2 in (b, e, h) and Device 3 in (c, f, i). On the top (a-c) panels, the leakage matrix for each device is presented. The units of the colorbar are MΩ, and its lower end is saturated for better visualisation. In the middle (d-f) panels, the turn on characteristics are plotted. The colour of each line corresponds to the same colour voltage probe in the inset of each plot. Measurements on panels (a-f) were taken with a QDac-II DAC. Panels (g-i) are schematics of the lock-in configuration based on the available leads of each Hall bar device.

Focusing first on the low magnetic field regime, the ρ_{XX} values are linearly fitted as a function of the magnetic field to calculate the carrier density. Then, with the respective values of ρ_{XY}, the carrier mobility is extracted. In Figure 7.3 a, mobility as a function of carrier density is plotted. Constant carrier density regimes are fitted with power laws $\mu \propto p_{2DHG}^{\kappa}$. The low exponent values of 0.466 ± 0.004 and 0.2799 ± 0.0015 for the high and low carrier density regime respectively suggest that the main scattering mechanism is uniform background impurities. This indicates that the dominating scattering

mechanism is not remote impurities scattering as it is usually the case for high mobility undoped Ge heterostructures grown by CVD [29].

In the absence of a perpendicular magnetic field and for the entire carrier density range, another power law fits the longitudinal conductivity and provides the percolation threshold for the metal-to-insulator transition $\sigma_{XX} = A(p_{2DHG} - p_p)^p$. In Figure 7.3 b, transverse conductivity as a function of carrier density is plotted. With the exponent fixed at 1.31 for a 2D system [95], the percolation density is on average $0.919 \pm 0.016 \cdot 10^{10}\text{cm}^{-2}$. By assigning the exponent as a fitting parameter, the percolation density shifts to higher values of $1.819 \pm 0.021 \cdot 10^{10}\text{cm}^{-2}$ with an exponent of 1.2004 ± 0.0026. The complete set of fitting parameters is presented in Table 7.2. The fitted parameters are compared with the literature in Figure 7.4 b. Even though the peak mobility of the reported devices is much lower than the state-of-the-art CVD heterostructures, the percolation density has low desirable values that motivate the fabrication and measurement of quantum dots.

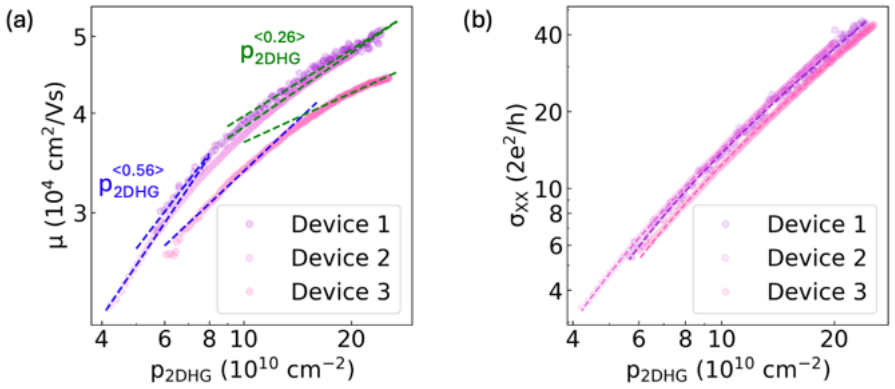


Figure 7.3: (a) Mobility and (b) zero-field conductivity as a function of carrier density for all three devices. (a) A low and high carrier density regime is used to fit with a power law the data. (b) The entire carrier density range is fitted to extract the percolation density.

	κ_{low}	κ_{high}	p	$p_{p,float}$ (10^{10}cm^{-2})	$p_{p,fixed}$ (10^{10}cm^{-2})
Device 1	0.59 ± 0.03	0.279 ± 0.005	1.11 ± 0.04	2.5 ± 0.4	0.50 ± 0.14
Device 2	0.670 ± 0.009	0.3097 ± 0.0019	1.2164 ± 0.0029	1.721 ± 0.023	0.993 ± 0.018
Device 3	0.423 ± 0.004	0.206 ± 0.003	1.134 ± 0.006	2.47 ± 0.06	0.59 ± 0.04

Table 7.2: Fitting values of mobility power laws and percolation density from Figure 7.3. The zero-field conductivity data are fitted with the exponent as a fitting parameter (floating) and fixed at 1.31 as it is theorised for 2D systems.

To explore further the dominating scattering mechanism, feedback from the crystal growth is essential. Here, three approaches are sug-

gested for future experiments. First, exploring the **quantum well thickness** may confirm that mobility limitations occur predominantly in very thin Ge layers [100]. Moreover, incorporating Si at the spacer barriers and making a **smooth transition** from $Si_{0.2}Ge_{0.8}$ to sGe may provide details on interface scattering [32]. Lastly, a technical detail that warrants investigation is the waiting time between $Si_{0.2}Ge_{0.8}$ growth and sGe growth. Typically, all heterostructures of the study had 2 mins (see Appendix A) waiting time between any changes at the growth. Even though the chamber has a high-quality vacuum, it should be verified that any **waiting time** does not contribute to the incorporation of impurities.

Reviewing the literature of the last forty years, from the first publication of People and Bean [101] until the latest evidence of this thesis, peak mobilities have remarkably improved in Ge heterostructures. In Figure 7.4 a, a historical evolution of the research field in terms of peak mobility is reviewed. The cited work is presented in the Appendix B. Novel techniques that eliminate dislocations in the substrate and better understanding of growth dynamics have resulted in peak mobility values above one million. One interesting perspective of the samples is that remote delta doping does not necessarily result in high-mobility heterostructures. Ionised impurities act as scattering centres, limiting mobility. Moreover, impurity incorporation in the crystal generates an interface that locally alters the lattice constant and allows dislocation formation. The doping layer needs to be close to the quantum well to provide carriers. However, having a dislocation generator close to the quantum well can only be detrimental to the electronic properties of the sample.

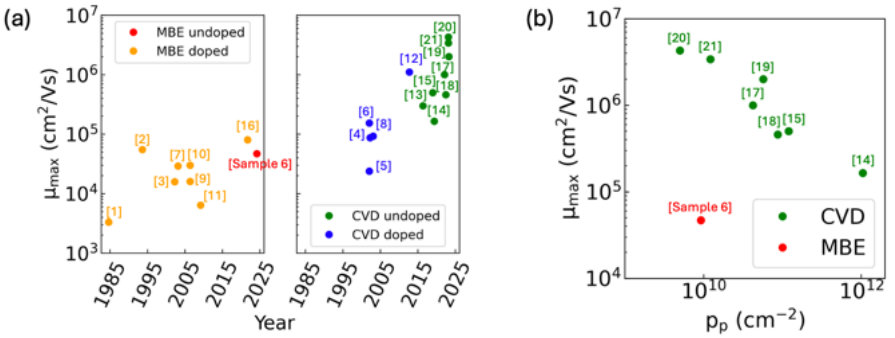


Figure 7.4: (a) Historical evolution of mobility in Ge quantum wells values over the last 40 years. The two plots are segregated based on the growth technique. Each technique is distinguished between doped and undoped heterostructures (b) Dependence of percolation density with peak mobility. The presented heterostructure of this thesis has significantly low mobility but the second-lowest percolation density in the literature. In Appendix B, the matching of the annotated references with the bibliography is given.

Closing the Hall characterisation of Ge heterostructures, the large field magnetoresistance is plotted in Figure 7.5. The 2D maps of ρ_{XX} and ρ_{XY} as a function of magnetic field and carrier density for **Device 3** indicate quantized plateaus that follow the formula $\rho_{XY} = \frac{2\pi\hbar}{e^2}\frac{1}{\nu}$, where ν is the filling factor for the Landau levels [102]. The plateaus are accompanied by near-zero dips in ρ_{XX}. In Appendix B, the results of **Device 1** and **Device 2** are presented.

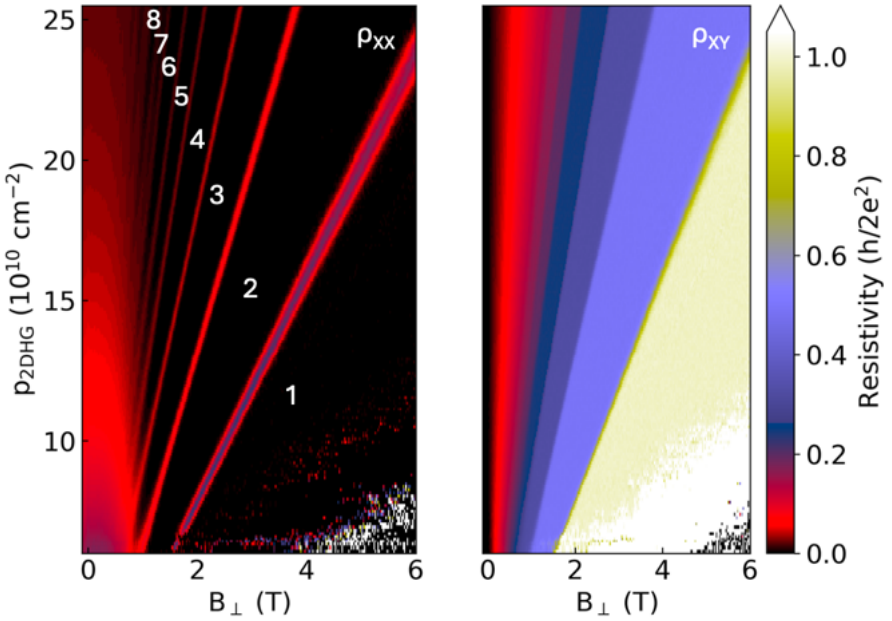


Figure 7.5: Large-field magnetoresistivity for Device 3. Annotations in the ρ_{XX} plot indicate the Landau levels as the magnetic field evolves.

7.1.2 *Si/SiGe CVD Hall Bars*

As described in the previous chapter, Si requires doped implantation regions and accumulation gates to bring the carriers to the active Hall bar region. Alternatively, one can prepare their implanted regions directly on the edge of the Hall bar. However, this was not possible for the explore devices since this process was time-consuming, and Hall measurements were not a priority for these samples. In Figure 7.6 a, a CAD drawing of the Hall bar design is presented. It has an aspect ratio between L/W of 3.25, and 6 nm of Al_2O_3 separate the top-gate from the accumulation gates. An additional 6 nm of Al_2O_3 ALD film covers the substrate to ensure no transport between the accumulation gates and the substrate. Standard lock-in voltage bias techniques were employed to measure this sample. An AC excitation of 14 µV was sent to the source, and three lock-in amplifiers recorded I_{XX}, V_{XX}, and V_{XY} while the magnetic field was swept from -100 mT to +800 mT.

In Figure 7.6 b, the magnetotransport data are presented. This measurement was not repeated for multiple gate values to identify peak mobility, but these measurements were only performed for diagnostics of the heterostructure. The gate configurations are denoted in Figure 7.6 b for clarity. Following the calculations described above and presented in 7.6, we find an electron mobility $0.166 \cdot 10^6 \text{cm}^2/\text{Vs}$ at a corresponding electron density of $3.67 \cdot 10^{11}$ cm^{-2}.

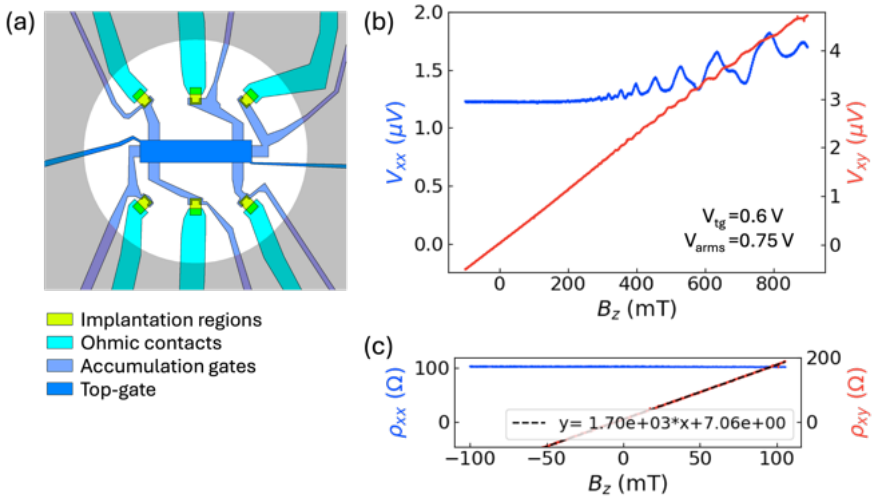


Figure 7.6: Si low-field magnetotransport. (a) CAD drawing of the measured device with the colour coding gate labels for clarity. The grey area denotes the mesa etched substrate. Full-range (b) and low-field (c) range magnetotransport measurements used for mobility calculation.

7.2 QUANTUM DOT CHARACTERISATION

Noise characterisation

Charge noise is the main source of decoherence for group IV spin qubits. It stems from local fluctuations in the electrostatic environment, such as two-level systems from interface traps in the dielectric, limiting the coherence times and operational fidelity of the qubits [103].

To analyse the noise spectrum of a device, it is necessary to measure a Coulomb peak alongside its corresponding bias spectroscopy. From the latter, the lever arm α can be calculated. Utilizing the Coulomb peak, time traces at various points along the peak are recorded. First and foremost, the points of maximum sensitivity are obtained. These are the flanks of the peak, where the derivative of the gate trace becomes maximum in absolute value. Moreover, to assess the device sensitivity relative to the background noise inherent in the setup, additional time traces are recorded both at the peak and within the Coulomb blockade regime. Once the current signal I from the *I/V converter* is obtained, using *Fast Fourier Transformation*, the time trace is translated to the frequency domain. The current noise spectrum, expressed as S_I, with the use of the lever arm α can be converted to units of energy according to the following formula:

$$\mathrm{PSD} = \sqrt{S_E} = \alpha\sqrt{S_I} \cdot \left(\frac{dI}{dV_P}\right)^{-1} \tag{7.2}$$

To characterise the noise in qubit systems, first, it is important to identify the addressable frequency bandwidth of operation. Typically, qubit manipulation is achieved by controlling local electrostatic potentials through voltages applied to gate electrodes. Since the gates are susceptible to noise fluctuations, any action related to them is performed with limited fidelity. Low-frequency (1/f) noise dominates the spectral characteristics at frequencies close to 1 Hz. Even though qubit operations may occur at high frequencies (in the range of MHz) characterising the noise at low frequencies is still relevant. The reference noise at 1 Hz enables consistent comparison and benchmarking of the low-frequency noise performance between different devices and methods. Last, the noise spectrum can be fitted by a $1/f^{\beta}$ function to identify any additional noise contribution mechanism in the system.

A significant advantage of characterising the noise in this bandwidth is the simplicity of the setup. This implies both on device architecture and on measurement apparatus. On the one hand, a single quantum dot is sufficient without the need to accommodate complex array geometries. On the other hand, the acquisition of the current time traces relies on standard DC apparatus without the need for complicated measurement schemes.

Thermometry

Dilution refrigerators can achieve temperatures of few tens of mK. However, it is important to understand the method used to identify the temperature. For example, the temperature value from a **ruthenium oxide** temperature sensor indicates the temperature related to phonons in the material. This is a resistive thermometer calibrated based on four-probe measurements as a function of temperature and thus is classified as a *secondary thermometer*. Focusing more on the electronic setup connected to the cryogenic apparatus, additional thermal sources, such as noise and power generating systems, contribute to the equilibrium of the cooled device. As a result, the effective temperature of the electrons of the device is much higher than the one indicated by the external sensor. By the use of a Coulomb peak it is possible to extract the information about the electronic temperature. This non-invasive type of thermometry has no need for calibration and thus **Coulomb Blockade Thermometers** are classified as *primary thermometers*.

For devices deep in the Coulomb blockade region, the following formula may be applied to a Coulomb peak to identify the electron temperature of the quantum dot.

$$G = \frac{G^{(0)}}{\cosh^2[\alpha(V_P - V_P^{(0)})/2k_BT]} \tag{7.3}$$

where G is the conductance as a function of gate voltage V_P, $G^{(0)}$ is the maximum conductance of the peak at the corresponding gate voltage $V_P^{(0)}$, α is the lever arm, k_B is the Boltzmann constant and T is the electron temperature. Equation 7.3 is valid when the condition for the charging energy is fulfilled ($E_C \leq k_BT$). In other cases, effects such as strong coupling from the leads and the power from the instrumentation may lead to increased electron temperature.

For more details on Coulomb blockade thermometry, the reader can refer to the following publications [104, 105]. Moreover, recent advancements with RF reflectometry techniques might be interesting to explore [106].

7.2.1 *Ge/SiGe MBE Quantum Dots*

Germanium devices fabricated based on the recipe of Appendix C were loaded in a *Bluefors BF-XLD400* dilution refrigerator to investigate quantum dots in Ge quantum wells grown by MBE for the first time. The goal of the devices was to form double quantum dots on each side of the quadruple array at the low-hole regime. In this way, reaching the few holes occupancy, it would be possible to identify the (0,2) and (1,1) hole states for spin-to-charge conversion by Pauli Spin Blockade. Overall, the fabrication was challenging, and producing a functional spin qubit was not possible. However, tuning the sensors and reaching the few-carrier regime for a single quantum dot was possible, and these results are presented here.

The bottleneck towards successful spin qubit measurements was device fabrication, both the lithography and the dielectrics. First, during the dose tests, it was possible to identify the right dose, but then, during the device fabrication in the heterostructures, the features were overexposed. To overcome this issue, the design of some devices was adjusted to a wider-spread gate configuration to compensate for the overexposure. The measurement results of this chapter are based on devices whose geometrical features adhere to the nominal design specifications. Thus, gaps between the gates were visible. As we will see, this contributes to the formation of unintentional quantum dots and charged regions on the wafer, which makes the electrostatic potential more complicated and possibly increases the charge noise. Moreover, previous fabrication attempts suffered from gate leakage and shorted gates, turning successful lithographies into unsuccessful samples. To conclude, the fabrication of thin gates that overlap with their adjacent ones is necessary, and rigorous optimization is required.

Before presenting the results from the successful fabrication, we start with an interesting perspective of an unsuccessful fabrication. In that case, the heterostructure was first etched with HF 5% to remove the Si terminating layer and identify any advantages of this process step. Figure 7.7 presents the leakage matrix and the ohmic behaviour of the reservoir leads of a device with all the gates grounded. Under these conditions, the device is highly conductive. Interestingly, the decomposition of the Si-MBE terminated layer with controlled oxidation affects the switching of the device mode from accumulation to depletion. In practice, this means that the threshold voltage has been moved to positive values. The threshold voltage is high enough, such as the 2DHG is uncontrolled and the gates cannot pinch off the channel. In practice, there is always transport around the device. In Figure 7.8, the pinch off with the residual current demonstrates the failure mode of this chip. In principle, the current from the source and the drain should reach zero, but a conductive path around the device persists once the inner path is depleted. This failure mode provides

a very impactful insight: over-etching of the ohmic contacts can lead to a different operation mode, and one should be very cautious at this fabrication step. Future approaches with in-situ dry etching prior to metal deposition should be explored as an alternative to substrate over-etch.

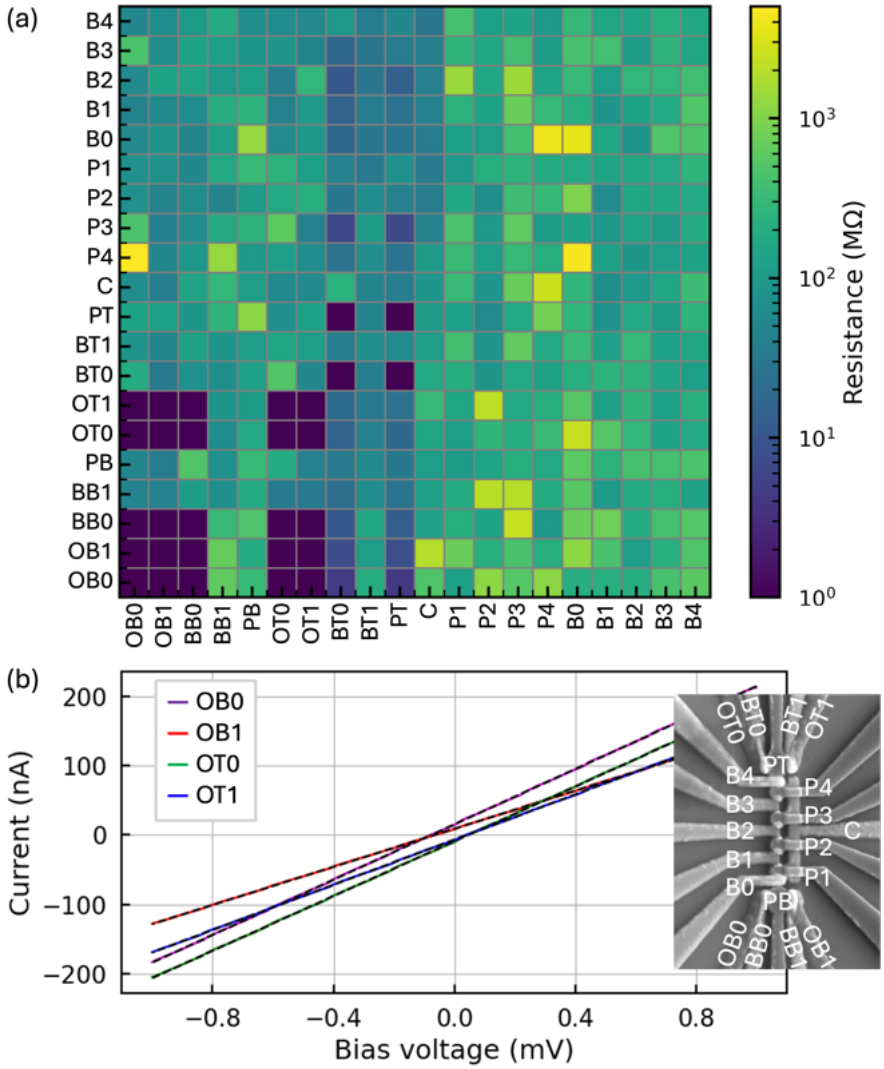


Figure 7.7: Germanium quantum dots in depletion mode due to etching of the termination layer with HF as discussed in the main text. (a) Leakage matrix and (b) IV curves of the ohmic contacts while all gates are grounded. The index in the plot is an SEM image indicating the nomenclature of the electrodes.

Focusing on the successful fabrication process, in Figure 7.9 b, the bias spectroscopy of the sensor dot is presented and measured by RF reflectometry. A constant RF signal of a frequency 142.2MHz generated by the **Quantum Machines OP-X+** was used to record the tank circuit response connected to the ohmic **O1**. Even though the sensing quantum dot is nominally defined below the plunger gate

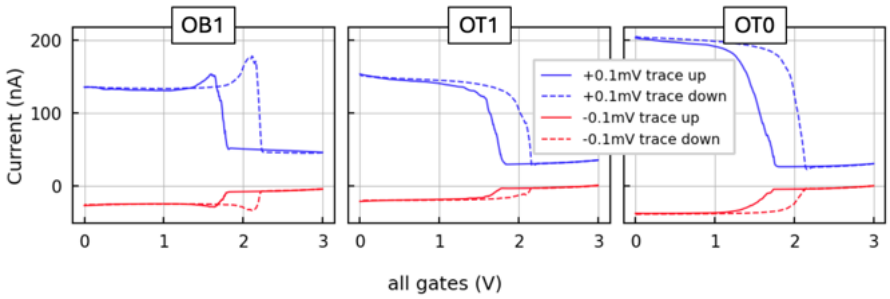


Figure 7.8: Residual current in pinch off with all gates towards positive gate values. A residual current occurs due to a conductive path around the device. Blue curves mark positive bias voltage of 0.1mV and red negative bias voltage of -0.1mV. Sold lines indicate trace up of the gates, whereas dashed lines indicate trace down.

PS, an unintentional dot was formed below **B1**, which is the tunnel barrier of the sensor with the quantum dot array. This event probably has to do with the gap between the sensor and the quantum dot array. The bias spectroscopy reveals quantum dot behaviour of the object under investigation. We try avoiding using the term *single quantum dot* here because even though we see this electronic behaviour, other electrostatic contributions may indicate that this might be a double quantum dot. The lever arm of the object was found to be approximately $\alpha = 0.084\text{eV}/\text{V}$.

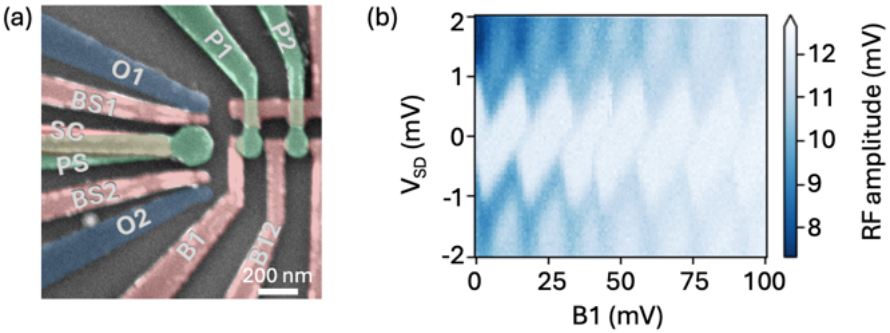


Figure 7.9: Bias spectroscopy of a Ge/SiGe quantum dot. (a) A false-coloured SEM image of a device identical to the one measured device. (b) Bias spectroscopy of a quantum dot below gate B1.

Furthermore, using the derived lever arm and focusing on one Coulomb peak, it is possible to perform noise spectroscopy and identify quantitative metrics for the quality of the device and its hosting heterostructure. Of course, as it has already been mentioned in the beginning, the noise measurements presented here are not a direct indication of the quality of the quantum well but a combination of the crystalline quality and the fabrication methods. It is clear that if the deposited Al_2O_3 dielectrics are of low quality and contribute to increased noise, the total device performance would be sub-optimal.

In addition, the observation of unintentional proximate quantum dots can increase the total noise as an additional fluctuating system. In addition to the device presented in Figure 7.9, a second quantum dot was investigated with a lever arm of $\alpha = 0.053\text{eV/V}$.

A **Keysight 34465A** digital multimeter connected to a **Basel SP983c** I/V converter with $\times 10^7\text{V/A}$ amplification are used to record DC time traces from the drain of the device. The minimum acquisition time is 80 msec, and each measurement duration is 160 sec. In Figure 7.10 a, the gate trace through the selected Coulomb peak is presented together with its numerical derivative. To be certain that the correct datapoint on Figure 7.10 a is selected, additional traces that stopped at the point of interest were taken before each time trace. This ensured the valid values for the numerical derivative. In Figure 7.10 b, the time traces are presented.

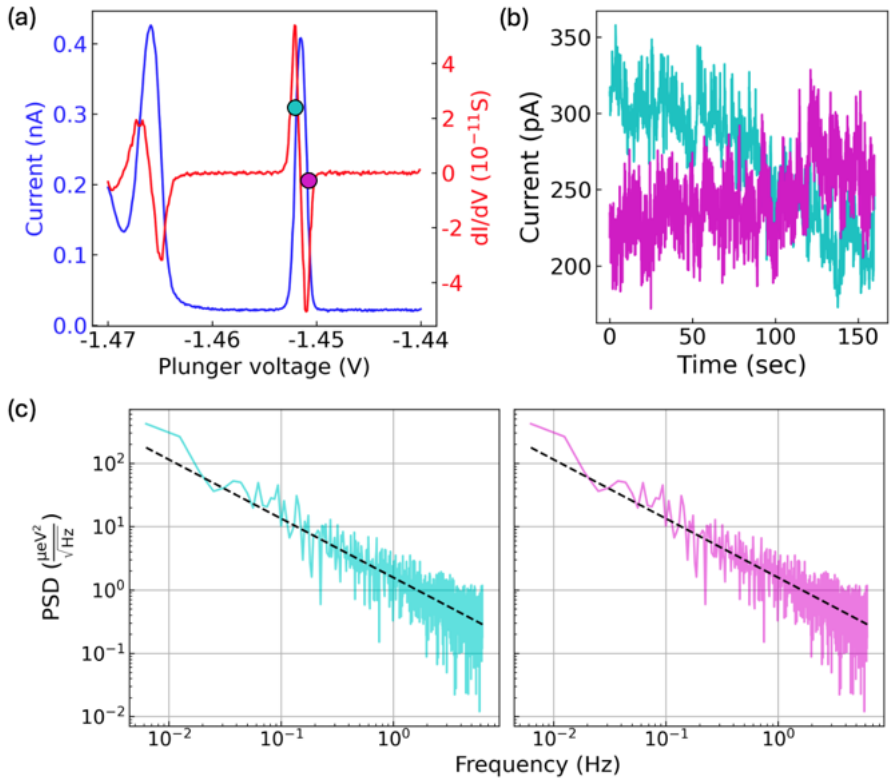


Figure 7.10: Noise investigation for the Ge/SiGe quantum dot. (a) Plunger gate trace and numerical derivative (b) Time traces at the selected sides of the Coulomb peak. (c) Power spectral density on the left (left) and right (right) flank of the Coulomb peak.

In Figure 7.10 c, *Fast Fourier transform* has been applied to the data of Figure 7.10 b together with Equation 7.2. This translates the noise spectrum from base units of current to units base of voltage by the use of the quantum dot lever arm. A fit is used to extrapolate the $1/f^{\beta}$ noise exponent. The noise at 1 Hz is $0.82 \pm 0.02 \frac{\mu eV}{\sqrt{Hz}}$ and $1.57 \pm 0.04 \frac{\mu eV}{\sqrt{Hz}}$

for the right and left flank, respectively. The exponent in all cases lies above 1 with an average value of $\overline{\beta} = 1.6625 \pm 0.024$.

In total, out of 2 devices, always parked on the flanks of the Coulomb peak, the statistical average was $\overline{\sqrt{R_E}} = 1.005 \pm 0.013 \frac{\mu eV}{\sqrt{Hz}}$ at 1 Hz. In contrast to Reference [107], the charge noise of the Ge/SiGe in this thesis has more than a two-fold increase.

Closing, single hole occupancy and charge sensing were demonstrated by using the quantum dot array next to the sensor dot. In Figure 7.11, a 2D map of plunger gates **P1** and **P2** is explored in RF reflectometry and charge sensing via the sensor dot. Even though charge sensing events from the holes below gate P1 are observed, no sensing events can be detected in P2. No failure mode of the P2 is observed since the charge sensing events of the P1 gate experience a capacitive shift while sweeping the P2 gate. The inability to detect charges at the P2 gate might be, again, a consequence of the fabrication challenges. The single-hole occupancy is in good agreement with the low percolation density demonstrated in a chapter in this chapter.

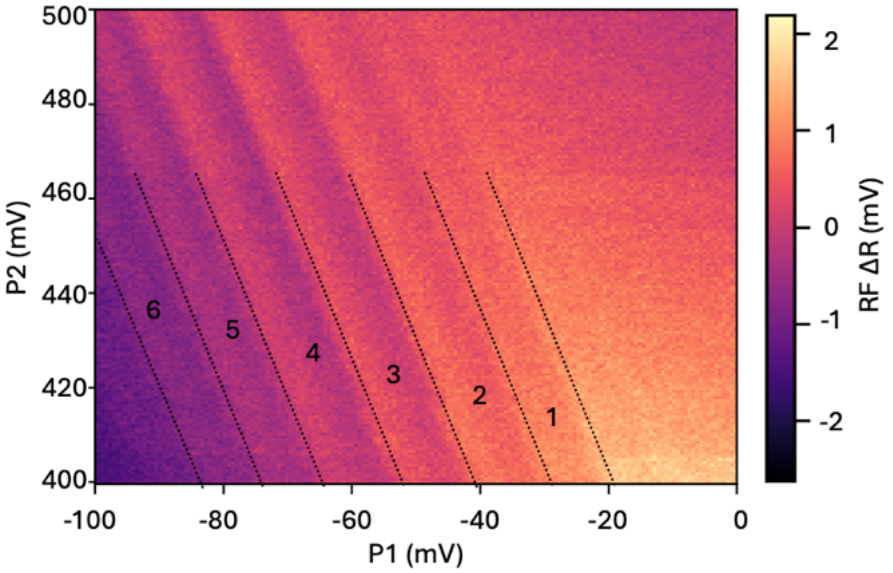


Figure 7.11: Charge sensing of the last holes in the quantum dot array. A quantum dot is located below P1 and is observed via RF reflectometry from the sensor quantum dot. The signal ΔR indicates the subtracted average value of each column.

7.2.2 *Si/SiGe CVD Quantum dots*

In this section, measurements of Si/SiGe heterostructures will be presented. The material platform features a 2DEG hosted by ^{28}Si with 800 parts per million (ppm) residual concentration of ^{29}Si [74, 76]. Natural Si (^{nat}Si) in its natural abundance has three isotopes, and one of them has a nuclear spin of $I = +1/2$. The concentration of the non-zero nuclear spin isotope is low, at 4.7% or 47000 ppm, and can be lowered further by centrifugation of $^{nat}SiF_4$. Producing such a high-purity source is very challenging, and developments in the field are slow due to manufacturing roadblocks. It is worth mentioning that while the growth project was still ongoing in 2021, we received our isotopically purified Si source, but it was never loaded in the MBE. Moving on to the applications of the isotopically purified materials, it was shown in 2014 at the University of New South Wales [50] that reducing the concentration of ^{29}Si at the active region results in a longer coherence time of the qubits. This was also a critical advantage of group IV spin qubits over the III/V GaAs platform.

In-house fabricated Si quantum dots were measured with the purpose of making Si spin-qubits in heterostructures without the need for micromagnets or stripline antennas based on Gilbert et al. [108]. The spins are manipulated by high-frequency pulses on the gates adjacent to the quantum dots. However, the requirements to perform these experiments were never fulfilled, and here, only the initial tuning of the dots, as well as failure modes, is presented. In particular, in order to reach the level of spin qubit experiments, the quantum dot array should be in the few-electron configuration measured by RF reflectometry. The formation of single, double and triple dots is presented here, as well as charge sensing and attempts for RF reflectometry. According to the workflow presented in chapter 6.6 the quantum dot devices were first loaded in the Kiutra L-Type Rapid cryostat for the initial characterisation. Since none of the devices fulfilled all the requirements, all the measurements below were performed either at 100 mK (base temperature of one-shot cooling) or 300 mK (base temperature of continuous cooling).

Setup troubleshooting

Before exploring the quantum dot measuremnts a useful aspect of devices came while troubleshooting the Kiutra L-Type cryostat. Si/SiGe quantum dots were used as a diagnostic to identify noise levels and optimise the setup. Noise rectification was observed while screening the devices. Figure 7.12 a, demonstrates bias spectroscopy of a Si/SiGe quantum dot device with highly distorted features. First, the Coulomb diamonds are smeared out with low visibility and low feature resolution. Secondly, the zero level of the bias leaks to the other side, similar to the explanation of Figure 7.12 c [109]. The zero current level $I = 0$ shows non-linear characteristics associated with the heat current related to the multi-level effects. As a result the noise source may be contributing to the system as a thermoelectric generator.

This noise rectification was the indicator that the setup needed investigation. The apparatus error was found to be in the ground connections. Once the grounding of the cryostat and the measurement setup was rewired, a repeat of the bias spectroscopy was attempted for the same device. The improvement of the signal was remarkable, with well-resolved features. By using an HP35670A signal analyser and measuring the V_{rms} at the 50 Hz peak through an Ithaco preamplifier according to the experimental procedure presented in Reference [110] a 2 orders of magnitude noise reduction was achieved. From 371 mVrms it dropped down to 2.4 mVrms. A similar effect can also be observed when a high-power RF signal is sent in the cryostat.

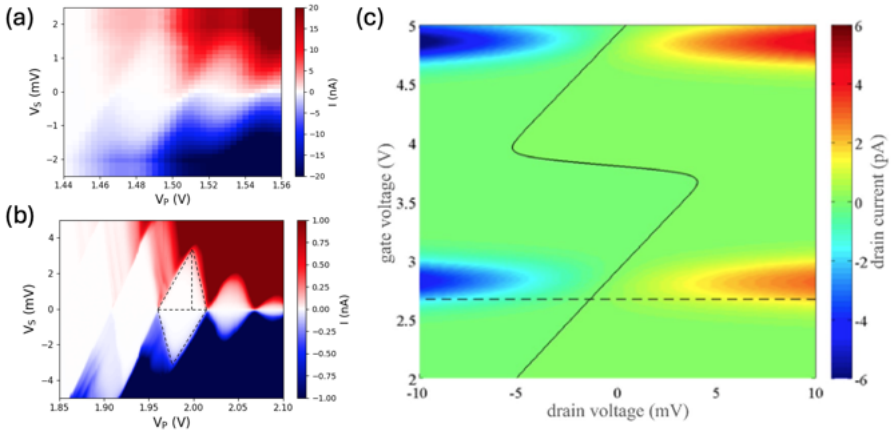


Figure 7.12: Noise rectification in quantum dots due to faulty grounding. (a) Bias spectroscopy of a quantum dot with a source noise in the apparatus. The Coulomb diamonds are distorted from the noise source. (b) Bias spectroscopy of the same quantum dot after identifying the noise source. (d) Reference [109] simulating the observed phenomenon of (a).

Thermometry

Benchmarking the capabilities of *Kiutra L-Type Rapid* cryostat and in combination with the availability of Si quantum dots, this set a good playground to characterise the electron temperature in the system. Using a similar quantum dot device as with the one from Figure 7.12, temperature dependence at different gate traces is taken, revealing the broadening of the Coulomb peaks.

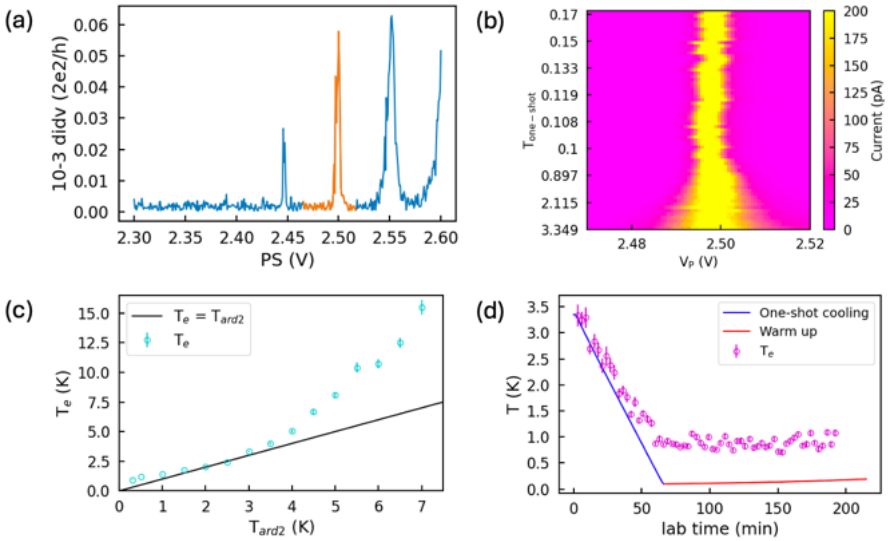


Figure 7.13: Thermometry of a Si/SiGe quantum dot in the Kiutra L-Type rapid cryostat. (a) Coulomb blockade with lock-in techniques. The chosen Coulomb peak is marked with orange colour. (b)Time evolution over the y-axis of the investigated Coulomb peak from (a). (c,d) Calculated electron temperature in a warm-up and one-shot cooling of the device. Solid lines indicate the note temperature as it was set from the cryostat.

Triple quantum dots in 28Si

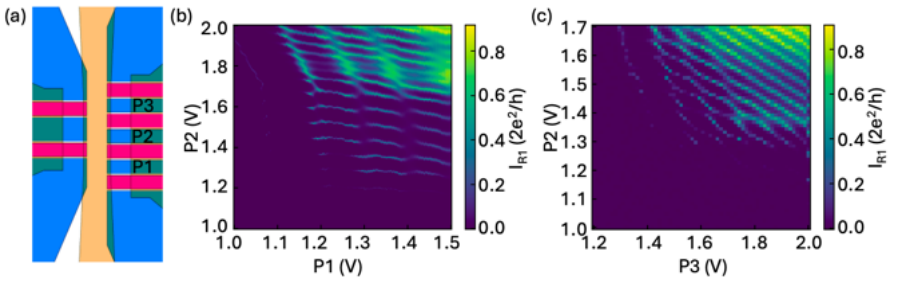


Figure 7.14: Si/SiGe triple quantum dots in transport: (a) A CAD design indicating the plunger gates that the quantum dots are formed. (b,c) Double quantum dots under (b) P1 and P2 gates and (c) P2 and P3 gates. While the measurement was taken, the third quantum dot was confined. This sequential measurement indicates a triple quantum dot below P1, P2 and P3.

DC transport measurements in the array using the parallel sensor design lead to the formation of a triple quantum dot in the multi-electron regime. A direct visualisation of a triple quantum dot via a single measurement is not possible due to the dimensionality of the system [111]. However, indirect observation by taking 2D maps of neighbouring plunger gate pairs of the array (**P1 vs P2** and **P2 vs P3**) leads to the conclusion that a triple quantum dot is in the array. The plots were only successfully acquired in DC transport of the quantum dot array. In parallel, the DC sensor signal was recorded without showing the characteristic charge transitions of the capacitive coupled quantum dot. In Figure 7.14, the formation of a triple quantum dot by the indirect observation of a double dot under the pairs **P1 & P2** and **P2 & P3** is presented.

To troubleshoot the inability to perform charge sensing, tuning of the coupling of the two current paths via the screening gates was attempted. In Figure 7.15 (b-e), the dependence of the two screening gates for the quantum dot under the plunger gate P2 is reviewed. On the top graphs, the current from the sensor quantum dot (OS1) is showing no charging events to the respective signal recorded from the array side (OD1). The graphs presented in these figures omit the axis values for simplicity, focusing only on the qualitative elements of the absence of charge sensing.

Last, the capacitive coupling of the sensor was investigated by employing two two-coulomb peaks at 600mV and 560 mV. In Figure 7.15 f, a bar chart map with the capacitive elements of the array indicates that the most sensitive region is near the quantum dot inder P2 gate (in this plot, P stands for plunger and B for barrier gates). However, even though the most capacitively coupled quantum dot was chosen it was not possible to demonstrate charge sensing.

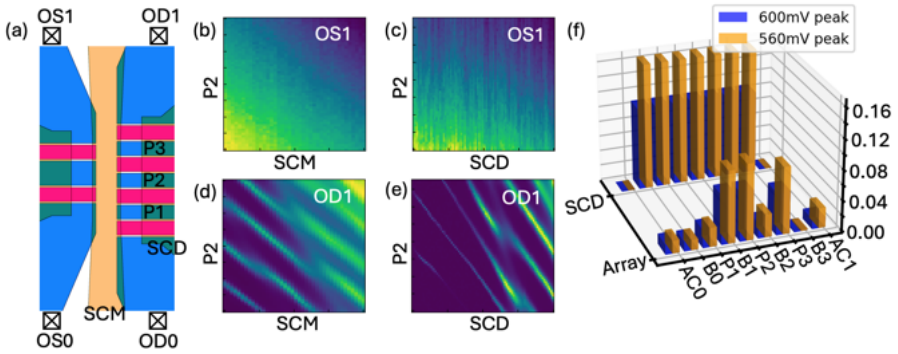


Figure 7.15: Troubleshooting the charge sensing in Si/SiGe with the parallel sensor design. (a) A CAD design indicating the plunger gates that the utilised gates. (b,c) Current signal of a quantum dot under P2 as a function of (b) SCM and (c) SCD screening gates. The purpose of this experiment was to confine the dot closer to the SCM gate and enhance the visibility from the sensor quantum dot. (d,e) The respective current signal of the sensor dot for the plots of (b, c). In (b-e), the axes values are omitted for simplicity. (f) Cross-capacitance of the sensor signal with respect to the gates of the device.

Lateral sensor design

Closing the Si/SiGe in-house fabricated heterostructures, a new design inspired by Reference [51] was attempted as discussed in Chapter 5.2. The advantage of the design is the proximity of the sensors to the quantum dot array. It resembles the design described in the Ge/SiGe heterostructures because, due to the effective mass of Si, the gate features are much smaller. In Figure 7.16, charge sensing at the P4 quantum dot is demonstrated.

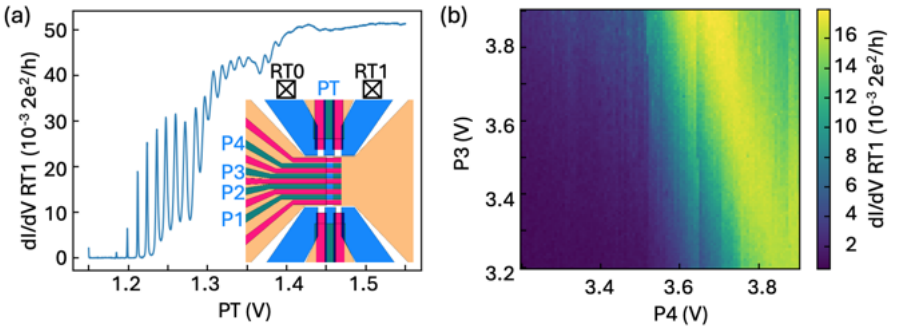


Figure 7.16: Signs of charge sensing in Si/SiGe with the lateral sensor design. (a) Electron transport signal from the charge sensor under PT. Inset is a CAD design of the lateral sensor design indicating the plunger gates. (b) Charge sensing of quantum dot below P4 via the top charge sensor under PT. No quantum dot is visible under P3.

7.2.3 *Foundry-based quantum dots*

This part is called generically *foundry-based* quantum dots because during the consortium with imec both Si/SiGe heterostructures and SiMOS chips were delivered. To make the transition smoother, a short introduction to the findings of Si/SiGe foundry heterostructures will be given, followed by the SiMOS results.

Si/SiGe foundry-based quantum dots

Si/SiGe heterostructures are less commonly used in industry and require optimisation. The devices measured comprise linear quantum dot arrays with either lateral or parallel sensors. For the cases where the gates were not shorted, significant **current drift** was observed with **inconsistent gate traces** in every sweep. Moreover, the electron confinement was not sufficient to show quantum dot behaviour.

SiMOS foundry-based quantum dots

The SiMOS platform was more developed than the Si/SiGe heterostructures. The possibility of forming a double quantum dot on the array leads to the realisation of Singlet-Triplet qubits. However, The bottleneck in this approach was RF reflectometry. Multiple setups for RF reflectometry were attempted, but none was able to give response at the quantum dot regime. The RF signal from the accumulation gates is shunting directly to the ground, and different approaches have been utilised through the years to address this issue [75, 112, 113]. The attempted wirebonding configurations are listed below:

1. Wirebond the QBoard smd inductors to the ohmic.
2. Wirebond superconducting spiral inductors to the ohmic.
3. Wirebond superconducting spiral inductors to the top-gate (accumulation/plunger or barrier).
4. Wirebond superconducting spiral inductors to the barrier gate and connect in parallel a capacitor.
5. Wirebond the QBoard smd inductors to the accumulation / plunger gates and add 100kΩ resistors to the ohmics.

In Figure 7.17, the configuration No. 4 of the list above is presented. Although the current and the RF signal match well when sweeping with all three gates, this is not the case when forming a quantum dot. Even though the current indicates Coulomb peaks, no response in the RF amplitude is recorded. The settings of the setup were tuned for maximum sensitivity without any visible variation in the received signal.

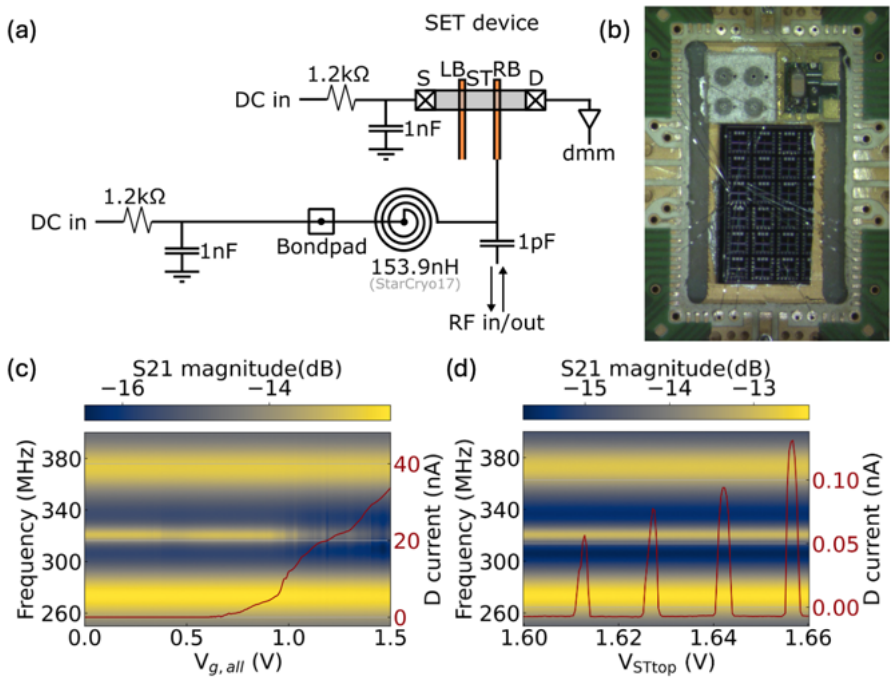


Figure 7.17: RF reflectometry of the sensor quantum dot by sweeping all the gates together. The RF signal is sent to a NbTiN superconducting resonator of inductance 100 nH and is wirebonded to the barrier gate RB. A signal response is observed at the range 1-2 V as indicated by the background colour.

Last, another device wirebonded similar to the described configuration of No. it was again not possible to respond to the RF signal. However, the DC measurements that were carried out showed single electron occupancy as shown in Figures 7.18 a-c. in contrast to the measurements presented in Figure 7.14 the reservoir of the double quantum dot was grounded and a proximate quantum dot was used as a charge sensor. The coupling of the double quantum dot was tunable, realising weak and strong coupling as shown in Figures 7.18 a and b, respectively. At low electron occupancy RF reflectometry was attempted without any success.

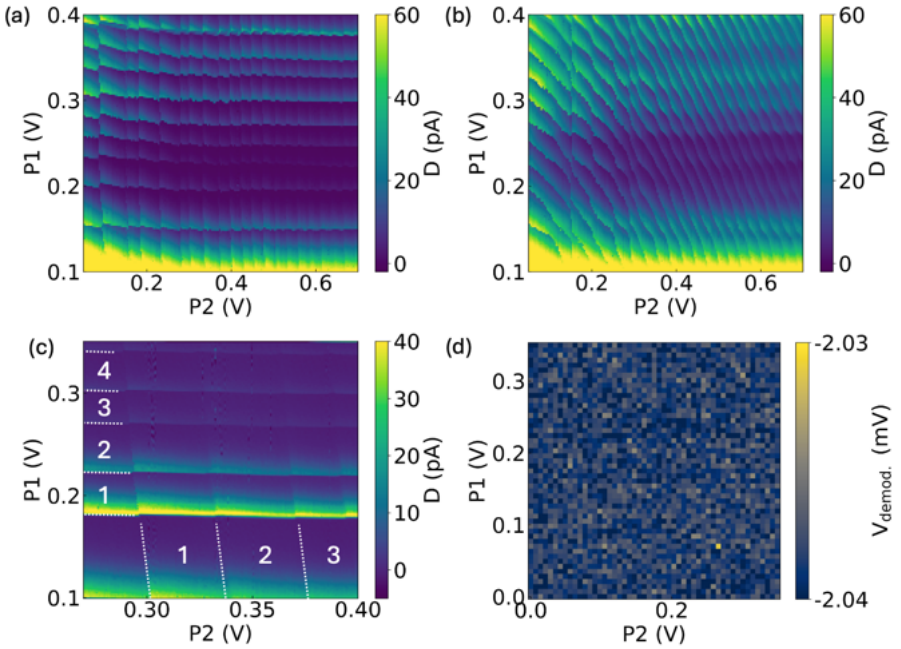


Figure 7.18: Double quantum dot of a SiMOS device. Few-electron occupation of a double quantum dot in (a) large scale and (b) focused at the last electrons. (c) The RF reflectometry signal of the same measurement as (b). No changes in the amplitude are observed.

8

CONCLUSIONS

This thesis showcased the entire experimental methodology for the production of a spin qubit device. Thorough structural and electrical characterisation demonstrated the potential and limitations of different group IV spin qubit platforms.

The initialisation of the experimental procedure began from the moment of receiving the Si(001) substrates from the manufacturer. Details and limitations of the molecular beam epitaxy system indicated the possible experimental directions in the material synthesis. Initially, the sources were calibrated based on standardised protocols, and the surface of the wafer was developed using two different experimental techniques. The first utilised thermal oxide desorption, whereas the second focused on the minimisation of the thermal load by atomic hydrogen irradiation. In parallel to the surface treatment optimisation, the growth temperature for germanium and silicon was reduced to achieve sharp interfaces. With that four heterostructures were grown successfully with the potential to be used for further exploration.

Structural characterisation targeted to identify the quality of the crystal growth. On the one hand, high-resolution transmission electron microscopy verified the pristine interfaces of the quantum well at the atomic level with no visible dislocations. On the other hand, the X-ray diffraction reciprocal space mapping verified the strain in the active region that results in the separation of heavy and light holes subbands. Atomic force microscopy on the wafer surfaces indicated the minimum surface roughness of shallow germanium quantum wells with the absence of a crosshatch pattern on the surface. This morphological effect, based on the reported literature review, is attributed to the low temperature and growth rate that a molecular beam epitaxy system provides. The absence of the pattern was also verified by the Nomarski optical microscopy method, and a heterostructure of a similar stacking grown by chemical vapour deposition was compared. Due to physical limitations the threading dislocation density was explored in a non-invasive way and indicated very low densities similar to the state-of-the-art heterostructures.

Even though the project was not able to progress further in the crystal growth direction, the interest and curiosity of individuals contributed to the utilisation of the produced samples. The sputtering of NbTiN on one of the heterostructures aims to explore the coupling of spins with photons via coplanar waveguide superconducting resonators. The first part of the thesis closed with suggestions for future directions of the heterostructures.

In the second part of the thesis, the tools and methods widely used for quantum device patterning were initially reviewed. Emphasis was given to the development process rather than to the working principles of the tools. This was the first introduction of different material platforms that were investigated during this research. The in-house fabrication of Si/SiGe heterostructures was widely troubleshooted without the possibility to realise successfully a spin-qubit. Moreover, as members of the quantum large-scale integration consortium, foundry devices in Si/SiGe heterostructures and SiMOS platform were explored for the same purposes highlighting the challenges of radio-frequency reflectometry in the Si platform. The closing of this part was dedicated to the failure mechanisms both on the fabrication and also the troubleshooting from the measurement feedback.

The last part of this thesis explores the electrical properties of the quantum devices that were introduced in the previous part. An introduction to the experiments by reviewing the formation of quantum dots is given. Moreover, a preview of the setup is presented to clarify the demonstrated experiments. Electrical measurements on Hall devices and quantum dots comprise the final results.

On the one hand, Hall characterisation of Ge/SiGe aims to extract metrics for the grown heterostructures from the first part of this thesis and identify the limiting factors in carrier mobility. It is seen that scattering from uniform background impurities is the dominating mechanism. Moreover, the peak mobility is similar to the highest values reported for Ge heterostructures grown by molecular beam epitaxy. However, the heterostructures produced by chemical vapour deposition techniques exhibit approximately two orders of magnitude higher mobility. However, the percolation density of the measured devices is comparable to the state-of-the-art samples, a metric of value for spin qubit devices.

On the other hand, the exploration of quantum dots is performed in equal depths for all material platforms. First, for the Ge/SiGe heterostructures, the formation of a single quantum dot is demonstrated together with charge noise spectroscopy. The noise level of the system is double compared to the current literature. This was the only investigated material platform where radio-frequency reflectometry worked successfully. In the case of Si/SiGe and SiMOS multiple configuration techniques were employed to optimise the challenges without a clear success. However, in the direct current measurements in SiMOS devices, they were able to isolate single electrons in double quantum dots, but the signal had no visibility in the MHz readout range.

Closing by addressing the challenges and limitations in the fabrication of quantum devices, it is important to clarify that progress in the

lab is not linear. Starting from point zero and reaching the finishing line at the end of the project is probably a recipe for intense and stressful work hours. It is highly beneficial to learn about all the stages of the research in parallel and pair experimentalists to address the project from different perspectives.

Specifically, stemming from the cases of continuously failed fabrication attempts, it is highly advised to reduce the complexity of the device. This will give the researcher the opportunity to learn about further unexplored methods in the project. Optimising other features down in the pipeline will give the benefit of faster progress when a complex functional device is delivered. Returning to the cleanroom to fabricate after measurements can be challenging. However, the brain is not overwhelmed with failures. Rather, it is carrying the wisdom of the recently acquired knowledge.

"In nearly twenty years of digging whales on every continent, the number of times I had ever found a complete skeleton of a fossil whale was exactly zero" [114]. My endeavour in the fabrication of quantum devices is nearly a third of Nick Pyernson's experience in his book **Spying on Whales**. However, when I read this sentence, it deeply touched my heart. I can paraphrase the quoted text on the following: "In all these years of fabricating quantum devices, the number of times I had ever succeeded in preparing a fully operational quantum dot device with expected properties was exactly zero". Every fabrication in the academic cleanroom maintains a level of uncertainty that is impossible to eliminate.

Part IV

APPENDIX

A

HETEROSTRUCTE PARAMETERS

	Sample ID	1	2	3	4	5	6
	Sample alias	*TEST1*	*TEST2*	*GeQW650*	*GeQW450*	*MQ0001*	*MQ0002*
Pre-growth	a-H treat.	✗	✓	✗	✗	✓	✓
	Thermal treat.	✓	✗	✓	✓	✗	✗
	HF immers.	✗	✗	✓	✓	✓	✓
	Treat. T	1100°C	800°C	800°C	800°C	800°C	800°C
	Treat. duration	10 min	45 min	60 min	60 min	10 min	10 min
Growth	Si buffer T	650°C	650°C	650°C	650°C	650°C	650°C
	Si buffer thick.	600 nm	600 nm	100 nm	100 nm	**100 nm**	**300 nm**
	Ge buffer T	650°C	650°C	450°C	450°C	450°C	450°C
	Ge buffer thick.	675 nm	675 nm	300 nm	300 nm	**300 nm**	**500 nm**
	RLG	✗	✗	✗	✗	✓	✓
	RLG T	-	-	-	-	450°C	450°C
	RLG thick.	-	-	-	-	**400 nm**	**1000 nm**
	$Si_{0.2}Ge_{0.8}$ buffer T	650°C	650°C	450°C	450°C	450°C	450°C
	$Si_{0.2}Ge_{0.8}$ buffer thick.	630 nm	630 nm	600 nm	600 nm	200 nm	200 nm
	Ge QW T	650°C	650°C	450°C	450°C	450°C	450°C
	Ge QW thick.	20 nm	20 nm	20 nm	20 nm	20 nm	20 nm
	$Si_{0.2}Ge_{0.8}$ spacer T	650°C	650°C	450°C	450°C	450°C	450°C
	$Si_{0.2}Ge_{0.8}$ spacer thick.	50 nm	50 nm	50 nm	50 nm	50 nm	50 nm
	Si cap growth T	650°C	650°C	**650°C**	**450°C**	450°C	450°C
	Si cap thick.	5 nm	5 nm	2 nm	2 nm	2 nm	2 nm
Characterisation	AFM	✓	-	✓	✓	✓	✓
	AFM rms	7.88 nm	61.13 nm	0.87 nm	0.39 nm	0.43 nm	0.48 nm
	TEM	✗	✗	✗	✗	✓	✓
	XRD RMS (004)	✗	✗	✓	✓	✓	✓
	XRD RMS (224)	✗	✗	✗	✓	✗	✓
	XRD RMS (113)	✗	✗	✗	✗	✗	✓
	XRD RMS (-1-13)	✗	✗	✗	✗	✗	✓
	X-SEM	✓	✓	✓	✓	✓	✓

Technical details of sources - Evaporation materials

High-purity Si block, single crystalline, $\rho >$ 1000 Ωcm, shaped for EBV200-100, mass 250 g
High-purity Si recharge block, single crystalline, $\rho >$ 1000 Ωcm, ∅36 × 20 mass 45 g, for use with the evaporant refill unit ERU16-100 (accepts two blocks)
High-purity Ge block, single crystalline, purity 6N, $\rho >$ 40 Ωcm, mass 250 g, shaped for Si crucible liner No. 485-00-057

Technical details of calibration growths

- Substrate surface treatment (prior growth - in cleanroom): Wet chemical etching with HF for 1 min and a-H for 10 min at 800°C
- Prior calibration: Si buffer 0.9V for 45 min at 650°C
- QCM values for Si and Ge sources: 0.6, 0.9, 1.2, 1.5 V
- Each layer was grown for 30 mins
- $T_{growth,Si} = 650°C$ and $T_{growth,Ge} = 450°C$
- 15 min temperature ramp + 5 min waiting time when alternating between each layer
- Characterisation: Cross-sectional SEM

B

SUPPLEMENTARY CHARACTERISATION

B.1 (004) XRD-RSM

The complete sets of the symmetrical XRD-RSM are given here

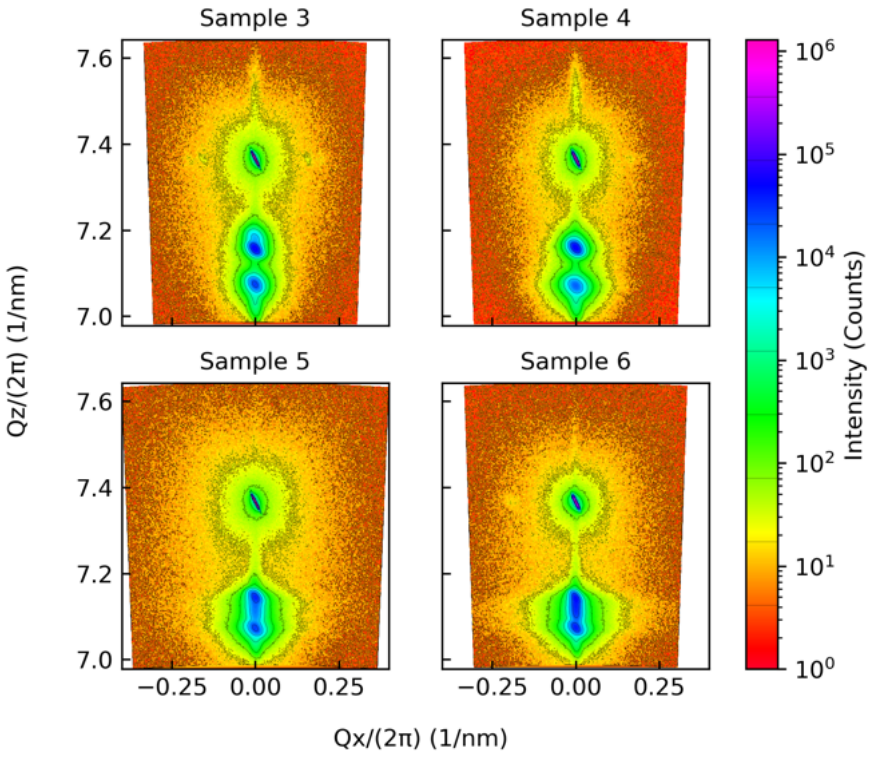


Figure B.1: XRD RSM of the symmetrical (004) axis for all investigated samples.

B.2 TEM ANALYSIS ON SAMPLE 5

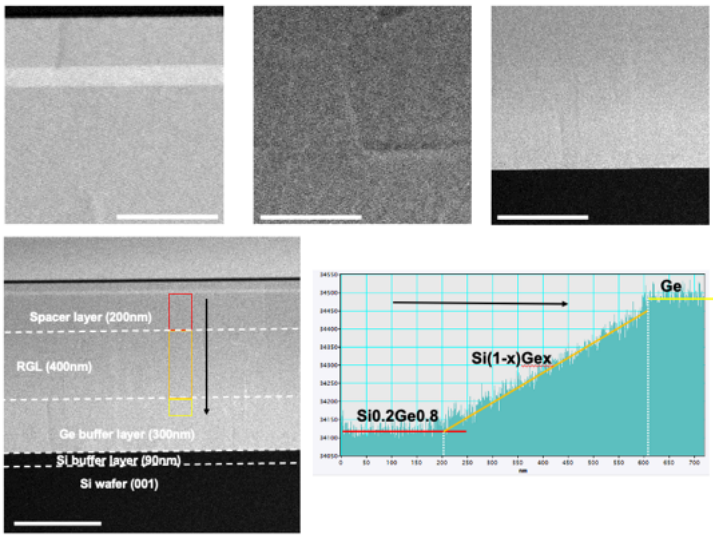


Figure B.2: Overview of the TEM analysis for Sample 5.

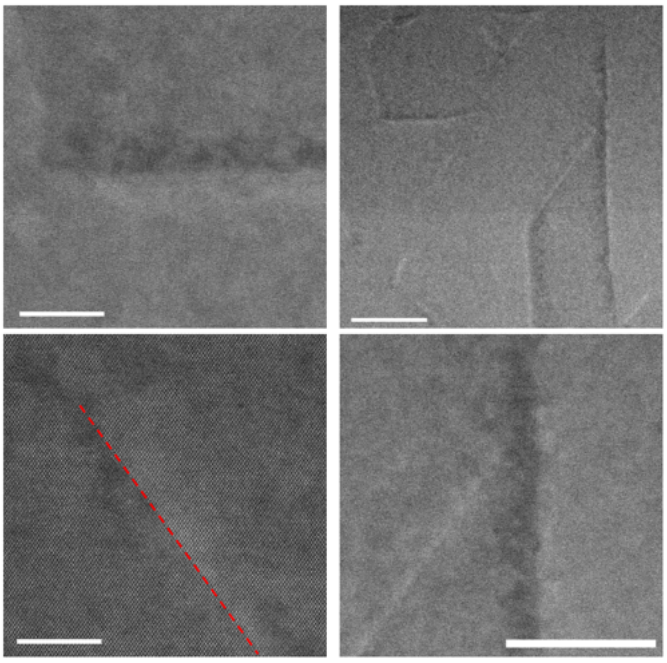


Figure B.3: Dislocations at the RLG layer for Sample 5.

B.3 SETUP WIRINGS

Oxford Instruments Triton 400 wiring

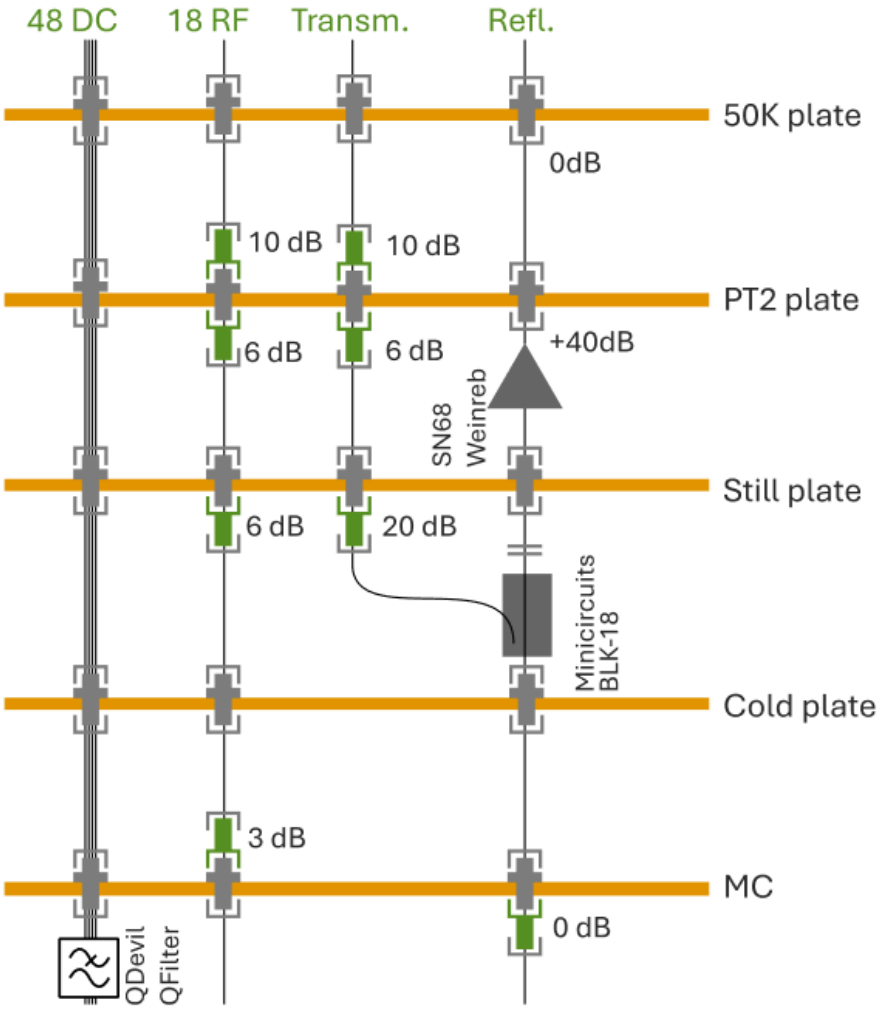


Figure B.4: The Oxford Instruments Triton 400 wiring

Kiutra L-type Rapid

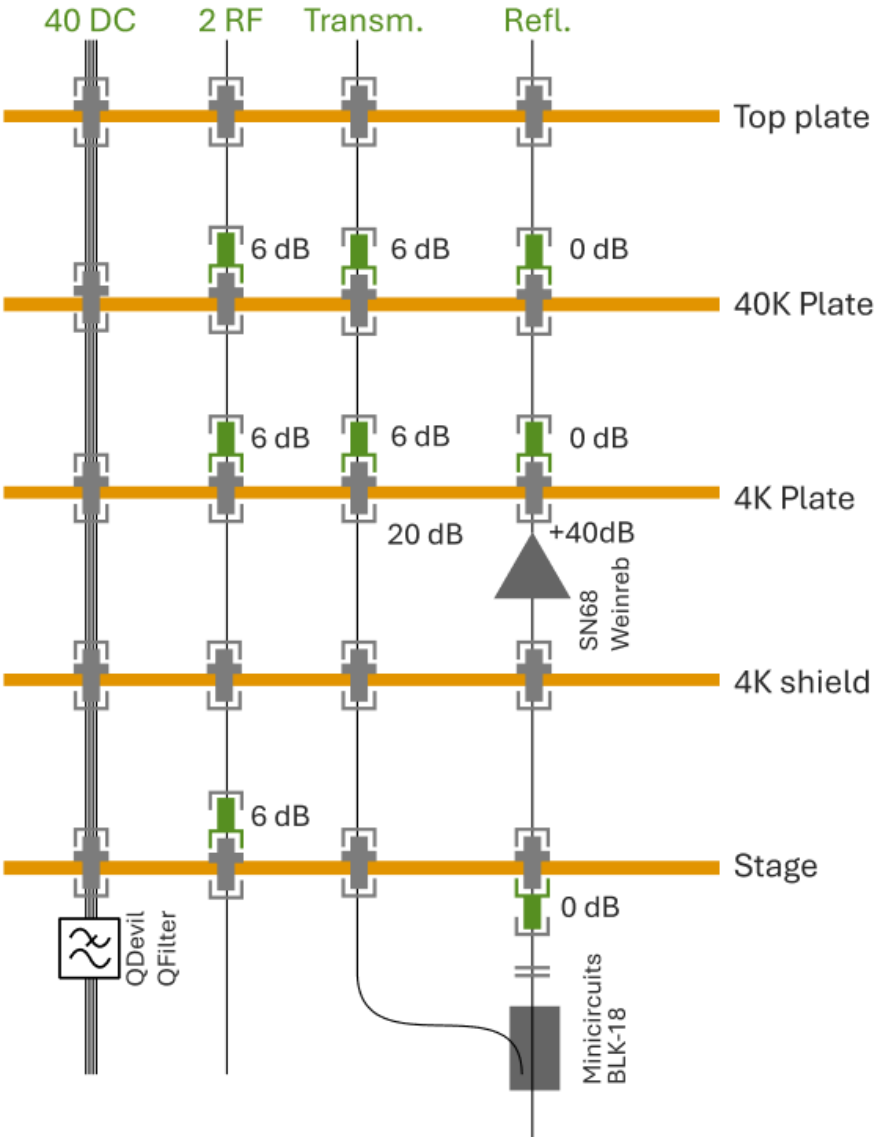


Figure B.5: The Kiutra L-type cryostat wiring

B.4 MAGNETOTRANSPORT FOR DEVICE 1 AND 2

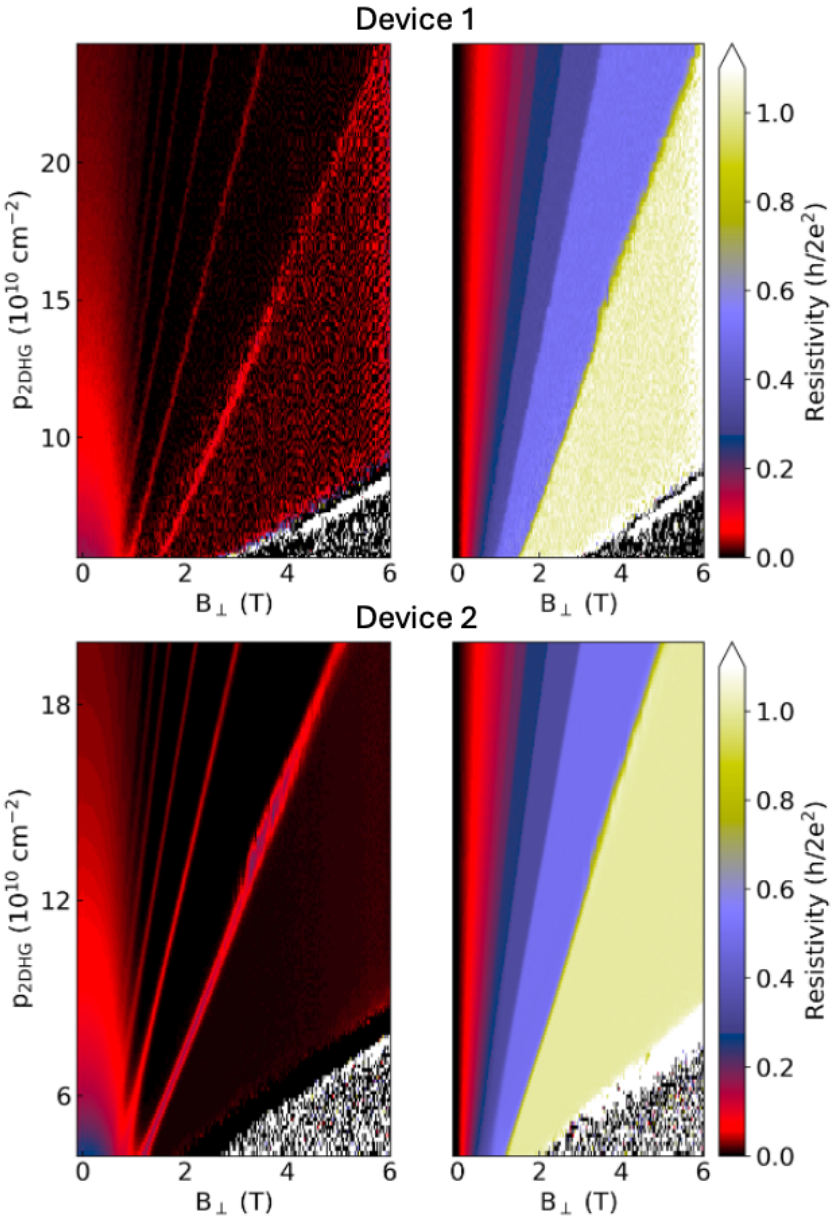


Figure B.6: Magnetoresistivity measurements on the longitudinal (left) and transverse (right) directions of Hall bar devices 1 (upper) and 2 (lower).

B.5 CROSS-REFERENCES FOR AFM AND MOBILITY PLOTS

AFM plot

Reference in plot	RMS value	Growth method	Reference in Bibliography
[1]	6.8 nm	MBE	[38]
[2]	4.5 nm	CVD	[25]
[3]	3.6 nm	MBE	[40]
[4]	3.0 nm	MBE	[41]
[5]	2.8 nm	CVD	[32]
[6]	2.8 nm	MBE	[36]
[7]	2.0 nm	CVD	[35]
[8]	2.0 nm	CVD	[33]
[9]	1.53nm	CVD	[34]
[10]	1.5 nm	CVD	[23]
[11]	1.2 nm	MBE	[37]
[12]	1.1 nm	MBE	[40]
[this work]	0.48 nm	MBE	[21]

Table B.1: Matching of references between Figure 3.14 and the bibliography.

Mobility plot

Reference in plot	Peak mobility	Doping	Growth method	Reference in Bibliography
[1]	3300 cm^2/Vs	✓	MBE	[101]
[2]	55000 cm^2/Vs	✓	MBE	[93]
[3]	15770 cm^2/Vs	✓	MBE	[115]
[4]	87000 cm^2/Vs	✓	CVD	[94]
[5]	23800 cm^2/Vs	✓	CVD	[25]
[6]	154000 cm^2/Vs	✓	CVD	[25]
[7]	29000 cm^2/Vs	✓	MBE	[116]
[8]	91900 cm^2/Vs	✓	CVD	[117]
[9]	16000 cm^2/Vs	✓	MBE	[118]
[10]	30000 cm^2/Vs	✓	MBE	[118]
[11]	6360 cm^2/Vs	✓	MBE	[37]
[12]	1100000 cm^2/Vs	✓	CVD	[33]
[13]	300000 cm^2/Vs	✗	CVD	[42]
[14]	164000 cm^2/Vs	✗	CVD	[119]
[15]	500000 cm^2/Vs	✗	CVD	[29]
[16]	80000 cm^2/Vs	✓	MBE	[36]
[17]	1000000 cm^2/Vs	✗	CVD	[44]
[18]	460000 cm^2/Vs	✗	CVD	[35]
[19]	2000000 cm^2/Vs	✗	CVD	[34]
[20]	4300000 cm^2/Vs	✗	CVD	[22]
[21]	3400000 cm^2/Vs	✗	CVD	[23]
[this work]	46790 cm^2/Vs	✗	MBE	[21]

Table B.2: Matching of references between Figure 3.14 and the bibliography.

C

FABRICATION RECIPE FOR GERMANIUM HETEROSTRUCTURES

This is the fabrication recipe followed for the fabrication of the Ge/SiGe quantum dot devices of chapter 4 in the thesis. The electron beam lithography steps are the same for the fabrication recipe of Si/SiGe quantum dot devices. However, there are key differences in the process steps described in the main text, and relevant recipe segments are included in Appendix D.

Disclaimer: Even though the EBL doses are listed here (used in February 2024), one should be careful and run their own dose tests for critical structures. In the span of one month, we have seen a lot of variation in the dose and low reproducibility.

Wafer ID	MQ0002(AA)
Chip ID	MQ0002_4
Sample dimension	4.2x5.3 mm^2
Design dimension	3.4x4.5 mm^2 placed at the center of the chip

C.1 PRELIMINARY CHARACTERISATION OF THE CHIP PRIOR FABRICATION

AFM scanning
Differential interference contrast microscopy (Nomarski method)
Dark and bright field large-scale optical images

C.2 CLEANING

1,3-dioxolane 5 mins sonication at 80% power and 80kHz
1,3-dioxolane 2 mins (in new clean beaker)
Acetone 5 mins sonication at 80% power and 80kHz
Acetone 2 mins (in new clean beaker)
IPA 2 mins
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 2 mins
Dark and bright field optical inspection

C.3 GLOBAL ALIGNMENT MARKS

Spin coating (Cleanroom)
Spin resist CSAR4 at 4000 rpm for 1 min
Post-baking at 185°C for 2 mins
Dark and bright field optical inspection
Electron beam lithography (Elionix 125 keV)
Need to find the right values for these here
Fine structures only: 1nA 250μC/cm^2 on write fields 100x100cm2 with 50000 dots (pitch 1) and base dose time 0.014us
Development (Cleanroom)
O-Oxylene for 45 sec
IPA 30 sec
Dry with N2 gun
Oxygen plasma ash 1 min
Dark and bright field optical inspection
Au deposition (AJA 2 system)
55 nm of Au with rate approximately 0.1nm/sec
Lift off (Cleanroom)
1,3-dioxolane 5 mins sonication at 80% power and 80kHz
1,3-dioxolane 2 mins (in new clean beaker)
Acetone 5 mins sonication at 80% power and 80kHz
Acetone 2 mins (in new clean beaker)
IPA 2 mins**
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 4 mins
Dark and bright field optical inspection

C.4 MESA DRY ETCH

Spin coating (Cleanroom)
Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min
Optical lithography (Heidelberg μmg501)
Defocus -1 and exposure time 30 ms
Development (Cleanroom)
AZ developer for 35 sec
MQ 30 sec
Dry with N2 gun
Oxygen plasma ash 1 min
Dark and bright field optical inspection with light filter
Kaufman milling (AJA 1)
2x3mins at 600V and 1 mTorr with the stage 90 degrees to the source and maximum spinning (2 mins break in between the two rounds to

cool off)
Strip off resist (Cleanroom)
Acetone 5 mins sonication at 80%power and 80kHz
Acetone 2 mins (in new clean beaker)
IPA 2 mins**
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 2 mins
Dark and bright field optical inspection

C.5 OHMIC CONTACTS

Spin coating (Cleanroom)
Spin resist A4 at 4000 rpm for 1 min
Post-baking at 185°C for 2 mins
Dark and bright field optical inspection
Electron beam lithography (Elionix 125 keV)
Need to find the right values for these here
Fine structures: 1nA 700$\mu C/cm^2$ on write fields 100x100um2 with 50000 dots (pitch 1) and base dose time 0.014us
Rough structures: 60nA 1000$\mu C/cm^2$ on write fields 500x500um2 with 50000 dots (pitch 8) and base dose time 0.014us
Development and HF etch (Cleanroom)
MIBK/IPA (1:3) for 1 min
IPA 15sec
BHF 10 sec
MQ rinse
MQ 10 sec
MQ 10 sec
Dry with N2 gun
Mount chip on the deposition holder
Transfer fast but carefully to the metal deposition chamber
Al deposition (AJA 2 system)
22 nm of Al with rate approximately 0.1nm/sec
Lift off (Cleanroom)
Acetone overnight
Acetone 5 mins sonication at 30% power and 80kHz
Acetone 2 mins (in new clean beaker)
IPA 2 mins**
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 2 mins
Dark and bright field optical inspection
Rapid thermal annealing (AccuThermo AW 610)
350°C for 15 mins in argon flow

Dark and bright field optical inspection
Atomic layer deposition (ALD2 Vecco system)
Add a dummy sample next to the chip for film characterisation
AlOx: 165 cycles at 110°C (20 msec Al precursor/H2O pulsing and 30 sec waiting)
Dark and bright field optical inspection
Ellipsometry on the dummy wafer

C.6 FIRST GATE LAYER (HALL BAR TOP GATE AND BARRIER GATES)

Spin coating (Cleanroom)
Spin resist CSAR4 at 4000 rpm for 1 min
Post-baking at 185°C for 2 mins
Dark and bright field optical inspection
Electron beam lithography (Elionix 125 keV)
Need to find the right values for these here
Fine structures: 500pA 275$\mu C/cm^2$ on write fields 100x100um2 with 50000 dots (pitch 1)
Rough structures: 60nA 400$\mu C/cm^2$ on write fields 500x500um2 with 50000 dots (pitch 8)
Development (Cleanroom)
O-Oxylene for 45 sec
IPA 30 sec
Dry with N2 gun
Oxygen plasma ash 1 min
Dark and bright field optical inspection
Ti/Pd deposition (AJA 2 system)
5 nm of Ti with rate approximately 0.1nm/sec
25 nm of Pd with rate approximately 0.1nm/sec
Lift off (Cleanroom)
1,3-dioxolane overnight
1,3-dioxolane 5 mins sonication at 30% power and 80kHz
1,3-dioxolane 2 mins (in new clean beaker)
Acetone 5 mins sonication at 30% power and 80kHz
Acetone 2 mins (in new clean beaker)
IPA 2 mins**
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 4 mins
Dark and bright field optical inspection
Atomic layer deposition (ALD2 Vecco system)
Add a dummy sample next to the chip for film characterisation
AlOx: 165 cycles at 110°C (20 msec Al precursor/H2O pulsing and 30 sec waiting)
Dark and bright field optical inspection

Ellipsometry on the dummy wafer

C.7 SECOND GATE LAYER (PLUNGER GATES)

Spin coating (Cleanroom)
Spin resist CSAR4 at 4000 rpm for 1 min
Post-baking at 185°C for 2 mins
Dark and bright field optical inspection
Electron beam lithography (Elionix 125 keV)
Need to find the right values for these here
Fine structures: 500pA 275μC/cm^2 on write fields 100x100um2 with 50000 dots (pitch 1)
Rough structures: 60nA 400μC/cm^2 on write fields 500x500um2 with 50000 dots (pitch 8)
Development (Cleanroom)
O-Oxylene for 45 sec
IPA 30 sec
Dry with N2 gun
Oxygen plasma ash 1 min
Dark and bright field optical inspection
Ti/Pd deposition (AJA 2 system)
5 nm of Ti with rate approximately 0.1nm/sec
25 nm of Pd with rate approximately 0.1nm/sec
Lift off (Cleanroom)
1,3-dioxolane overnight
1,3-dioxolane 5 mins sonication at 30% power and 80kHz
1,3-dioxolane 2 mins (in new clean beaker)
Acetone 5 mins sonication at 30% power and 80kHz
Acetone 2 mins (in new clean beaker)
IPA 2 mins**
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 4 mins
Dark and bright field optical inspection

C.8 FINAL CHARACTERISATION

Dark and bright field large-scale optical images
SEM characterisation on the dummy structures
AFM on real devices

** Wet optical inspection. If the lift-off or strip-off is not complete do not dry your sample, but repeat the cleaning until you have a pristine surface.

C.9 GENERAL COMMENT: HOW TO FIND ACCURATELY THE CENTER OF A RECTANGULAR-SHAPED CHIP WITH THE SEM OF THE EBL

Rough estimation
Measure roughly in an optical microscope your chip dimensions $(x_{optical}, y_{optical})$
Load your sample in the EBL tool
Find the low left edge of your chip
x-direction
Move by $x_{optical}$ towards right
Adjust the x position by N_x increments of 0.01 mm until you find the low right corner of your chip, where $N_x \in \mathbb{Z}$
Move back to the low left corner of your chip
Verify that the accurate x-dimension of your chip is:
$x_{SEM} = x_{optical} + N_x \cdot 0.01\text{mm}$
If not, repeat the process and find the accurate x_{SEM}
Repeat the process for the y-direction
Once you find the accurate (x_{SEM}, y_{SEM}) move to the low left corner once more
Move by $(\frac{x_{SEM}}{2}, \frac{y_{SEM}}{2})$
Now at the WECAS software, you can place your pattern at the center of your chip

D

FABRICATION DIFFERENCES IN SILICON HETEROSTRUCTURES

D.1 FABRICATION OF IMPLANTATION CHIP

Spin coating (Cleanroom)
Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min
Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min
Optical lithography (Heidelberg μmg501)
Defocus -2 and exposure time 30 msec
Development
AZ developer for 60 sec
MQ 30 sec
Dry with N2 gun
Oxygen plasma ash 2 mins
Double seal sample for shipping to University of Sherbrooke.

D.2 SIMULATIONS WITH SRIM

Initial simulations using the Stopping and Range of Ions in Matter (SRIM) software were used to identify the right dose. In Figure 5.3 a simulated ion range is presented based on the employed heterostructure. The simulations presented here are heavily based on the work that **Fabio Ansaloni** did during his PhD, and the author is very grateful for the initialisation of the code.

To get a bit more insight into the simulation procedure in Figure, we see the simulated intensity after the ion implantation in the heterostructure towards the Z direction (with z=0 being the surface and positive values towards the Si substrate). The ion density is calculated at the peak of the histogram. According to the documentation "the ordinate is set so that by multiplying by an ion-beam dose, normally in units of atoms/cm^2, the plot reads directly as a concentration in units of atoms/cm^3. For example, if the ion beam dies is 10^{14}atoms/cm^2, then an ordinate value of 1000 directly converts to a density of 10^{17}atoms/cm^3".

D.3 ION IMPLANTATION CONDITIONS

Verifying the ion beam conditions by the simulation, we proceed by using the recommended values from the growth group of Giordano Scappucci in TU Delft. We use P^+ ions with a source acceleration voltage of 20 keV, and dose of $10^{15}cm^{-2}$. Activation annealing is performed at 700°C for 12 seconds after implantation and the resist strip-off is performed right after the procedure with acetone, IPA and drying with N2 similar to the recipes described in appendix C.

D.4 OHMIC CONTACTS

Spin coating (Cleanroom)
Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min
Optical lithography (Heidelberg μmg501)
Defocus -2 and exposure time 30 msec
Development and HF etch (Cleanroom)
AZ developer for 35 sec
MQ 30 sec
HF 5% 10 sec
MQ rinse
MQ 60 sec
Dry with N2 gun
Mount chip on the deposition holder
Transfer fast but carefully to the deposition chamber
Ti/Pd deposition (AJA 2 system)
5/65 nm of Ti/Pd with rate approximately 0.1nm/sec
Lift off
NMP at 80°C for 10 mins
NMP at 80°C for 10 mins (new beaker)
Acetone 2 mins
Acetone 2 mins (in new clean beaker)
IPA 2 mins
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 2 mins
Atomic layer deposition (PicoSun system)
Double seal sample for transferring outside of cleanroom
Transfer the sample to the Technical University of Denmark (NanoLab)
AlOx according to the standard DTU, Nanolab recipe
Transfer the sample back to the University of Copenhagen (QDev)
Dark and bright field optical inspection
Ellipsometry on the dummy wafer

D.5 GATE LAYERS

Gate layers are fabricated in a similar way as the Ge/SiGe devices. Here we just list the deposition sequence of the gate layers.

1. Screening gates
2. Accumulation and plunger gates
3. Barrier gates

D.6 PROTECTION BONDING PADS

The etching windows are smaller than the original gate pads and their purpose is to locally remove the dielectric and expose the metallic film

Spin coating (Cleanroom)
Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min
Optical lithography (Heidelberg μmg501)
Defocus -1 and exposure time 30 msec
Development
AZ developer for 35 sec
MQ 15 sec
Dry with N2 gun
Oxygen plasma ash 1 min
Wet etching
Post-baking at 115°Cfor 1 min (resist reflow)
MF32A 8 mins (etch rate 2nm/min, see etch tests)
MQ 30 sec
Dry with N2 gun
Lift off
NMP at 80°C for 10 mins
NMP at 80°C for 10 mins (new beaker)
Acetone 2 mins
Acetone 2 mins (in new clean beaker)
IPA 2 mins
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 2 mins

The protection pads are larger than the original gate pads and the etching windows. Their purpose is to protect the substrate from leakage due to mechanical deformation.

Spin coating
Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min

Spin resist AZ1505 at 4000 rpm for 1 min
Post-baking at 115°C for 1 min
Optical lithography (Heidelberg μmg501)
Defocus -1 and exposure time 30 msec
Development
AZ developer for 60 sec
MQ 15 sec
Dry with N2 gun
Oxygen plasma ash 1 min
Ti deposition (AJA 2 system)
200 nm of Ti with rate approximately 0.2nm/sec
Lift off
NMP at 80°C for 10 mins
NMP at 80°C for 10 mins (new beaker)
Acetone 2 mins
Acetone 2 mins (in new clean beaker)
IPA 2 mins
IPA 2 mins (in new clean beaker)
Dry with N2 gun
Oxygen plasma ash 2 mins

E

CAPPED INAS SAG GATE-TUNABLE NANOWIRES

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Abstract

InAs selective area grown (SAG) nanowires are a promising platform to investigate hybrid quantum transport phenomena [120]. One of the prerequisites for quantum device applications is high electron mobility. It has been reported that the growth temperature of the semiconducting channel affects electron mobility [121]. Surface states are another limiting factor in electron mobility. This issue has been addressed in two-dimensional electron systems by adding an upper barrier above the transport channel [122]. In this work, we implement this method to understand the confinement of the electron wavefunction in InAs SAG structures grown on GaAs(100) substrates by molecular beam epitaxy (MBE). In particular, we compare identical InAs SAG nanowires grown with and without the capping layer. We characterize both hall bars and field-effect nanowire transistors grown along two different crystallographic orientations. We find that the material intermixing between the capping layer and the transport channel hinders the advantages of the capping layer resulting in alloy scattering. Transmission electron microscopy structural characterizations along with chemical composition analysis support the data.

Following, the three main figures of the presented poster are displayed.

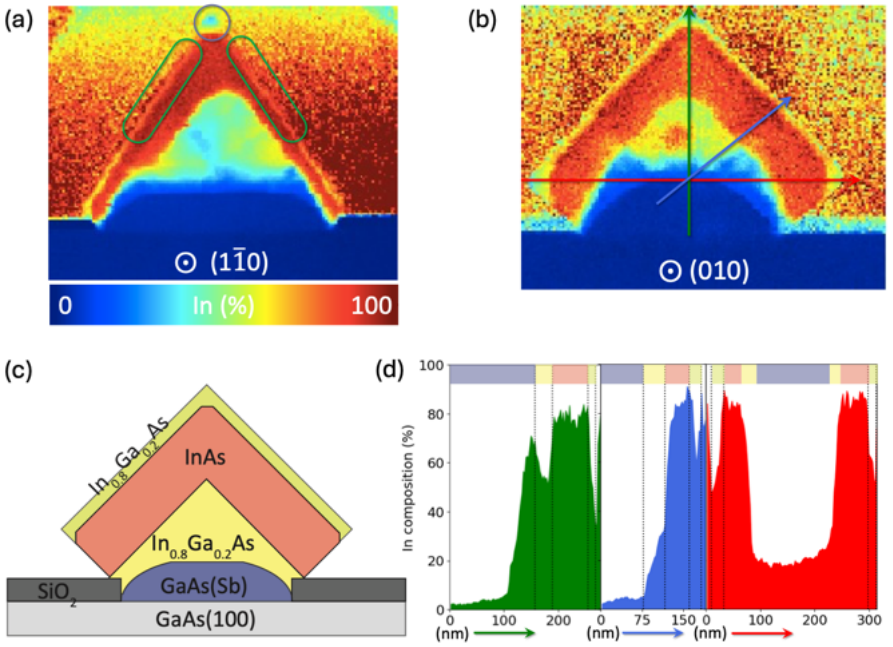

Figure E.1: TEM electron energy loss spectroscopy (EELS) compositional analysis. Both nanowires have an InGaAs cap, but its growth is promoted in the [010] direction rather than in [1-10]. The nanowire comprises an $In_{0.8}Ga_{0.2}As$ buffer channel, an InAs conductive channel and a capping layer of $In_{0.8}Ga_{0.2}As$. A cross-sectional schematic is provided in (c). (a) EELS map for the (1-10) orientation. High Ga accumulation in the corners, together with a lack of a Ga composition in the facets, minimise the thickness of the capping layer. Moreover, abrupt compositional changes in the structure generate dislocations. (b) For the (010) orientation, EELS reveals $\approx$ 50% Ga in the capping layer, a In(Ga)As transport channel with 80-90% In and fluctuations from the buffer are accompanied with similar fluctuations in the capping layer, (d) Indicates the elemental analysis of In across the coloured arrows of (b).

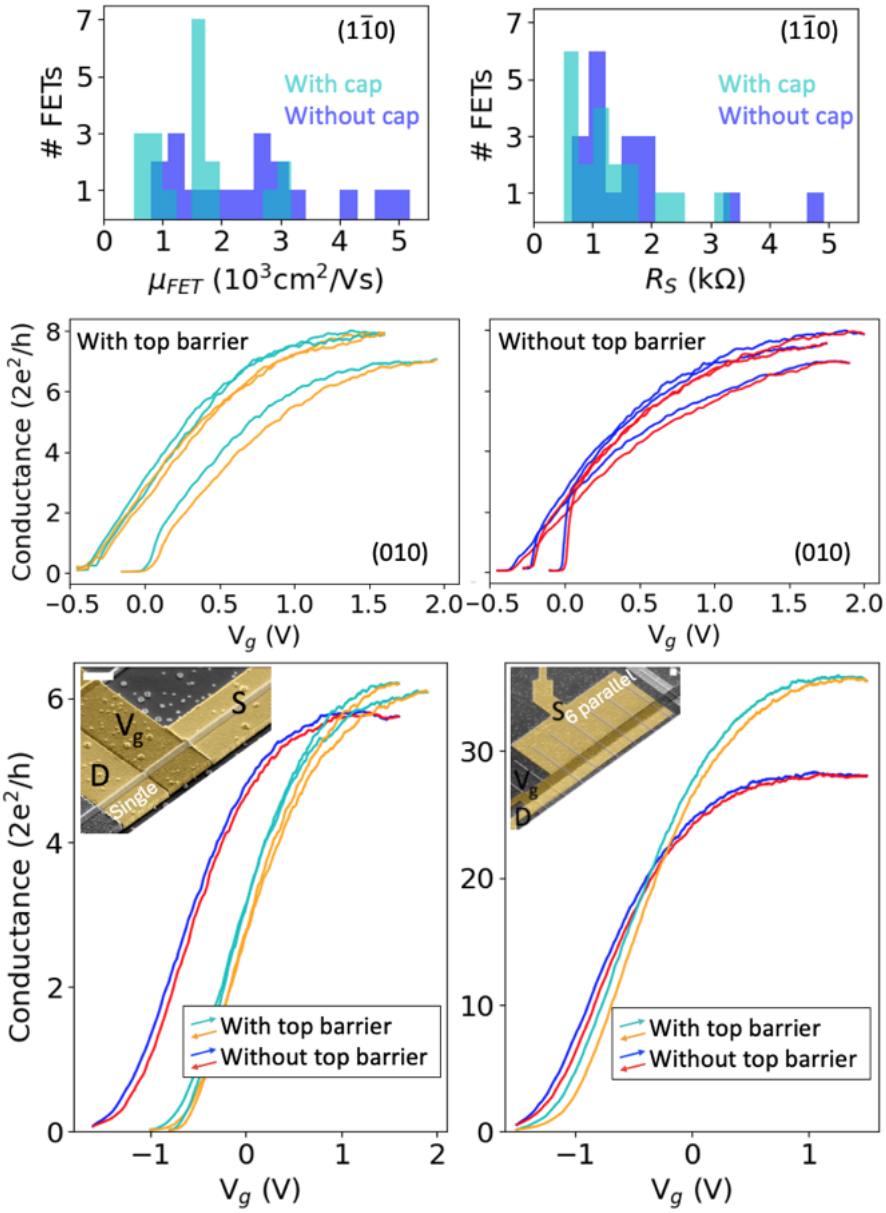

Figure E.2: Field-effect transistor pinch off plots. 37 nanowires (NWs) in total have been investigated for their pinch-off characteristics. Two different chips from two different growths were fabricated with single and multiple NWs, as shown in the insets. Mobility was fitted based on Reference [123].

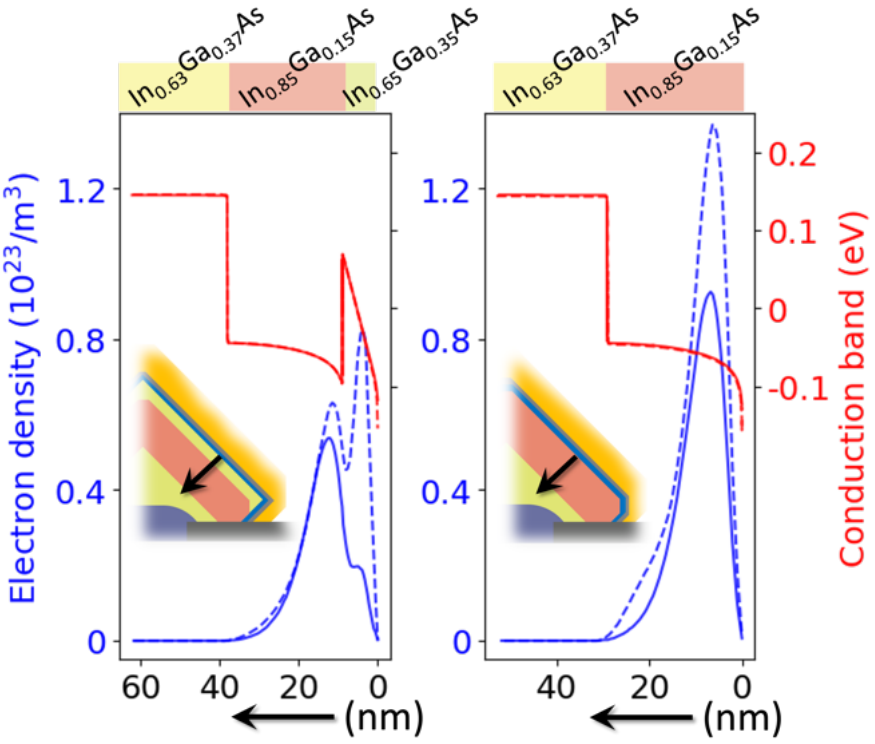

Figure E.3: Schrödinger-Poisson simulations with COMSOL. The electronic structure with (left) and without (right) the capping layer was explored.

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