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PhD Thesis

Cryogenic On-Chip Multiplexing Using SAG Nanowires

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Abstract

This thesis explores on-chip multiplexer circuits based on selective area growth nanowires as means of expanding the scale of measurements at cryogenic temperatures. Even though scalability of quantum electronics platforms and circuits is a commonly discussed aspect, a limiting factor for any materials platform is the number of transmission lines in cryogenic measurement setups which is limited by the available cooling power. Multiplexer circuits overcome this limitation by using control lines to address an exponential number of outputs. Here the operation and fault-tolerance of such circuits is presented. The circuits are then used to investigate the variability of nominally identical transistors based on selective area growth nanowires with statistical significance and the reproducibility of gate-defined quantum dot device parameters across nanowires. Additionally, the circuits are used to study the effect of systematic variations in nanowire geometry and structure on the electron transport properties.

The presented methods expand the toolbox for optimizing selective area growth based on electron transport feedback, provide a possible direction for scaling up cryogenic circuits, and establish a process for benchmarking a system. The measurements take advantage of the scalability and versatility of selective area growth nanowires and attest to the suitability of the platform for scalable quantum electronics.

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To anyone reading this work - I hope you find it interesting and useful, and perhaps it will help you in your own journey.

Contents

List of Abbreviations

AC	Alternating current
AFM	Atomic force microscopy
ALD	Atomic layer deposition
CCVS	Current controlled voltage source
CMOS	Complementary metal-oxide-semiconductor
CSAR	Chemical semi amplified resist
DAC	Digital-to-analog converter
DC	Direct current
DUT	Devices under test
EBL	Electron beam lithography
EELS	Electron energy loss spectroscopy
FET	Field effect transistor
FIB	Focused ion beam
GPA	Geometric phase analysis
HAADF-STEM	High angle annular dark field scanning TEM
HRTEM	High resolution transmission electron microscope
ICP	Inductively coupled plasma
IPA	2-propanol
MBE	Molecular beam epitaxy
MIBK	Methyl isobutyl ketone
NW	Nanowire
PMMA	Polymethyl methacrylate
QD	Quantum dot
RF	Radio frequency
RIE	Reactive ion etching
RT	Room temperature

SAG	Selective area growth
SEM	Scanning electron microscope
TASE	Template-assisted selective epitaxy
TEM	Transmission electron microscope
VLS	Vapor-liquid-solid
VLSI	Very large scale integration
2DEG	2-dimensional electron gas

List of Figures

1 | Introduction

Over the past decades, low temperature studies of mesoscopic electronics have improved the understanding of the role of quantum phenomena in electronic devices. Driven by ongoing developments in fabrication techniques, cryogenic technologies, and material science, the realization of circuits and devices incorporating a large number of interacting quantum systems appears within reach [1, 2] potentially enabling quantum processors and simulators able to tackle important problems intractable on classical computers. However, the scaling of quantum circuits poses new challenges to both control electronics, device reproducibility, and material developments. Recently several studies of measurement automation [3, 4] and the implementation of control electronics at the deep cryogenic level have emerged and schemes for multiplexing control and read-out of quantum devices are being developed [5–8].

On the material side, the performance of quantum devices is closely tied to the quality of the underlying materials and the push towards complex devices requires detailed knowledge of the correlation between parameters of material synthesis and fabrication, structural properties, and device performance [9, 10]. However, conclusions are often based on results from a few selected devices measured under the relevant conditions due to the extensive efforts of device fabrication and low-temperature measurements. When scaling quantum circuits, individual device characterization becomes increasingly unfeasible and establishing material parameters and their variability and reproducibility with statistical significance is a more efficient approach.

Semiconductor nanowires (NWs) present many of the challenges of upscaling quantum materials and have been a workhorse of exploratory quantum electronics experiments due to their high crystal

quality, intrinsic nanoscale confinement, and ease of forming electrical contacts. However, the out-of-plane growth of traditional vapor-liquid-solid (VLS) nanowires means realizing complex devices and circuits requires manual transfer of individual NWs from the growth to the device substrate - a methodology unsuitable for large scale circuits incorporating thousands of NWs. Selective area growth (SAG) provides a promising alternative [11–14] allowing planar NW growth directly on the device substrate at positions which can be accurately defined by lithography. Key experiments based on SAG NWs have already been reported such as field effect transistors (FETs) [15, 16], NW Hall bars [17], quantum interferometers [18, 19], hybrid superconducting devices [18, 20] and quantum dots (QDs) [21]. However, while large scale networks and NW arrays have been grown [12, 19, 22] and promoted as a platform for large-scale circuits, low temperature electron transport experiments have still been limited to devices based on single or few NWs. So far the scalability and reproducibility of SAG - which are arguably the main motivations for using the platform - have yet to be addressed either on the structural or on the electronic level.

Here this issue is addressed and the first steps in investigating SAG as a scalable platform for quantum electronics are taken. Large-scale arrays of nominally identical InAs SAG nanostructures are used to demonstrate the fabrication and sub-kelvin operation of SAG NW devices incorporating thousands of interconnected NWs. By connecting SAG NW circuits in multiplexer-demultiplexer configurations the SAG scalability is utilized to perform semi-automatic characterization on large ensembles of individual NWFET devices allowing to extract the key material parameters with statistical significance. With this approach, the number of SAG NW devices which can be characterized at low temperatures is effectively limited only by the time of measurements breaking the bottleneck of traditional measurement schemes where the limit is set by the number of electrical connections in the

cryostat (limited by the cooling power) and the space available on the device chips.

Device-to-device reproducibility is of key importance for the scalability of quantum circuits [23, 24]. The multiplexer circuits enable us to evaluate reproducibility at a scale unprecedented for NW devices. In all, more than 1500 devices were measured and analysed throughout this work. The three most important result classes presented in detail are an array of 256 nominally identical FET devices, 50 FETs of varying length, and 20 QD devices.

From analysis of statistical correlations across the nominally identical FETs it is possible to separate the contributions from structural variations and electrostatic variations related to random charged impurities in the device vicinity. Results from the FET length study give insight into the semiconductor channel near the metal contacts and provide information about the semiconductor conductivity. Finally, the statistical properties and reproducibility of SAG NW-based QDs - the canonical element of NW quantum electronics - are studied. The simultaneous creation and tunability of a large number of SAG NW QDs using a common set of local gates shared across a large QD ensemble is demonstrated and a study of the statistical distribution and correlation of QD parameters is performed both within single QDs and across the QD ensemble.

The results presented demonstrate SAG NWs as a promising material platform for scalable quantum electronic circuits and add an important tool for large-scale characterization and automation to the electron transport experiment toolbox.

2 State of the Art

2.1 Platforms for Quantum Electronics

Parameters of Importance

Quantum electronics is a field of study that involves the manipulation and control of charge carrier quantum states. There are several key parameters to consider regarding potential platforms for quantum electronics applications.

The first parameter is confinement of charge carriers (throughout we will focus on electrons). When the physical dimensions of a structure are reduced such that they are comparable to the electron de Broglie wavelength, the electrons become confined to discrete quantum mechanical energy levels which form the basis of quantum electronics. This confinement can be realized in 2D systems such as 2-dimensional electron gasses (2DEGs), graphene, and MoS_2, 1D nanowires and carbon nanotubes, or 0D quantum dots (QDs), molecules, and ions.

The material system should have high tunability to allow for control of the energy levels and charge carrier density in the system. A quantum electronics platform should be responsive to electric and/or magnetic fields. Semiconductors are at the center of modern classical electronics due to their gateability and also makes semiconductors an attractive platform for quantum electronics.

Temperature is also an important variable - to resolve electron quantum states in transport measurements the thermal energy k_BT should be smaller than the characteristic energy scales of electron transitions, otherwise transitions between states can be thermally activated. This generally restricts quantum electronic experiments to cryogenic temperatures.

Charge carrier mobility is an important indicator of material quality. A higher mobility indicates fewer scattering sources and thus low disorder in the system. Charge carrier mobility is one of the most

important benchmarks used when optimizing material synthesis [25].

Some intrinsic properties to consider when selecting materials are the effective electron mass m^* and spin-orbit interaction (SOI). The effective mass describes electron behaviour in a crystal and reaction to external electric and magnetic fields and is closely related to the curvature of the energy bands in the material. A lower m^* results in a higher μ and higher maximum charge carrier velocity. Due to their low m^* III/V semiconductors such as InAs and InSb are attractive material platforms for quantum electronics [26]. Spin-orbit interaction arises from broken inversion symmetries and can be affected by external electric fields allowing to manipulate spins via electrostatic gating rather than applied magnetic fields which improves scalability, energy consumption and allows for simple local control of spins [27]. Spin-orbit interaction is also theorized to be an important component for p-wave superconductivity in proximitized semiconductors which can host topological bound states that could allow to realize topologically protected quantum computing [27, 28]

Practicalities of device fabrication should also be considered such as the ease of forming electrical contacts. For charge transport experiments it is desirable to be able to easily realize ohmic source and drain contacts to the semiconductor. Even without a native surface oxide layer it is possible for a Schottky barrier to form at the interface between the metal and the semiconductor if the work function of the semiconductor is larger than that of the metal (for an n-type semiconductor) leading to non-linear current-voltage characteristics [26]. In this case doping or alloying can be used to lower the barrier at the interface and realise ohmic transport but this complicates the fabrication process and introduces defects in the crystal lattice.

A final aspect to consider is scalability. Scalability is often mentioned when considering platforms for quantum electronics but can be difficult to define accurately. In this context scalability implies repro-

ducibility of the system parameters within the experiment tolerance and the ability to increase the size and complexity of the system while minimizing required human labour. To clarify, quadrupling the size or complexity of the system should not quadruple the amount of human work required. Most increase in processing time should come from automated process steps such as lithography and device designs should be reusable between samples and parameterized if possible. Scalability is not always necessary for research purposes, but it is beneficial when conducting experiments which have a small chance of success in each device and crucial for practical applications of quantum electronics.

Scaling and Limitations

Scalability is an aspect that is often considered in the context of quantum electronic systems as it is expected that any real application of the technology will require very large scale integration (VLSI) - the ability to integrate $> 10^3$ individual components on a single chip [29]. Likewise, in exploratory fundamental research the complexity of realising large numbers of devices limits the ability to explore systematic relations between electron transport phenomena and device geometry or the search for exotic low-yield phenomena. In quantum computing the state of the art in various qubit systems and quantum computing circuits has matured to the point where individual elements are of sufficient quality that scaling the systems into a usable quantum computation circuit becomes feasible. However, the number of interoperable elements necessary for useful applications poses challenges in implementation [5, 30, 31].

Practical applications of quantum computing might require millions or even billions of physical qubits [5, 30, 31]. Similarly, in fundamental research aimed at advancing our understanding of quantum devices and searching for rare transport phenomena can require multiple device fabrication cycles and cooldowns just to yield single or few

examples. The geometry and dimensions of devices are also crucial parameters and systematic optimization requires a large number of individual devices. Such research can be greatly accelerated by having a larger number of devices per chip to reduce the time and operating costs incurred.

A limiting factor in realising measurements of a large number of quantum devices is the fact that cryogenic measurement systems are limited not just by the dimensions of the refrigerated space but also by the number of transmission lines connecting the refrigerated sample to the room temperature measurement and control equipment. The number of these transmission lines is limited by both space and cooling power [2, 7]. Each transmission line has to be routed down to the mixing chamber from the top plate of the dilution refrigerator and adds a heat load to the cryostat. At some point, even if it is possible to fit a large number of transmission lines in the cryostat physically, it becomes unfeasible to provide enough cooling power. Furthermore, the physical dimensions of the chip are an important bottleneck. Even if it was possible to provide large numbers of transmission lines inside the cryostat, making connections to individual devices (e.g. via bondpads) becomes an unfeasible task. A different approach to scale up measurement capacity is to integrate on-chip control circuitry into experimental device designs which reduces the number of necessary room temperature connections per element.

Another challenge with scaling quantum electronic circuits is the reproducibility and reliability of circuit components. As the number of individual circuit elements increases it becomes unfeasible to individually characterize each component. Instead, a method to benchmark the platform and establish tolerances for components is needed allowing to establish if the material platform is suitable for the desired application and design circuits and protocols with the component tolerances in mind.

Common Material Platforms

Given these aspects, let us consider some popular material platforms and their respective pros and cons for use in quantum electronics.

One of the first platforms enabling mesoscopic physics and still widely used for quantum electronics and condensed matter experiments is 2DEG realized in GaAs/AlGaAs heterostructures [32]. The charge carrier density of a 2DEG can be locally controlled by electrostatic gating and very high charge carrier mobilities ($> 10^6\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$) have been achieved in 2DEG systems at millikelvin temperatures [32–34].

The planar geometry of the structure allows for largely freeform device fabrication directly on the substrate without constraints of positioning or interconnecting branching current paths, making the platform suitable for large-scale circuits and industrial-scale fabrication of high electron mobility transistor components. However, the freedom of device design comes with the cost of additional complexity when it comes to 1D confinement of charge carriers. Pseudo-1D channels can be created in a 2DEG system by employing electrostatic gates to deplete the 2DEG surrounding the desired channel. This approach comes with the drawback of taking up transmission lines. Another option is to define the geometry by etching away parts of the heterostructure leaving a pseudo-1D channel, yet such a top-down approach introduces edge roughness which contributes to disorder and charge-traps in the system [35, 36]. The 2DEG can be protected from surface noise sources by increasing its depth [37], however, this reduces the sharpness of electric fields acting on the electrons in the 2DEG [38]. Furthermore, it can be challenging to establish ohmic contact to the 2DEG. Common methods include recessing the contacts, ion implantation, or annealing to establish contact to the buried 2DEG [39, 40] which also

increase the number of impurities.

Most modern classical electronics are Si-based due to its abundance, physical, electrical, and chemical properties. Silicon has a relatively large bandgap of 1.12 eV, and $m^* = 0.33$. As a monoelemental crystal it also has bulk-inversion and structural-inversion symmetry leading to negligible electron spin-orbit coupling [41]. Si monocrystals can be produced with extremely high purity by the Czochralski process [42]. Furthermore, Si can be isotopically purified removing the spinful ^{29}Si isotopes resulting in pure spinless ^{28}Si eliminating nuclear spin noise from spin qubit devices

It is also tempting to realize quantum electronics on bulk Si due to the advanced state of the Si industry possibly integrating the new technology into the existing foundries and applying existing know-how and well-established processes. Important devices such as quantum dots which are important components in sensing and lasing applications as well as building blocks for electron spin and charge based quantum computing can be realized on Si [43, 44]. Integrated circuits can be created on bulk Si wafers by local doping, and SiOx is a chemically stable dielectric useful for fabricating gates. Silicon native oxide has no charge traps in contrast to other semiconductor native oxides making Si based devices electrically extremely stable. However, the dopants used in fabrication are also impurities and can affect e.g. charge carrier mobility [45, 46].

Graphene - a monolayer of C atoms arranged in a honeycomb lattice - is another commonly used 2D platform. The bandgap of graphene is zero making it a semimetal and both hole and electron charge carriers can be induced by electrostatic gating [47]. Graphene also has a low electron effective mass $m^* = 0.012$ [48] and high mobility $\mu > 10^4\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ [47]. Due to its monolayer nature, electrons in graphene are very sensitive to the environment - new properties can be engineered by combining graphene with other materials e.g hexagonal

BN [49] or by stacking multiple layers of graphene e.g. magic-angle graphene [50]. However, this also means that surface adherents or substrate impurities can act as electron scattering sources.

Another C allotrope of interest is carbon nanotubes - effectively a sheet of graphene rolled into a tube-shape - carbon nanotubes confine electrons to a 1D channel. The bandgap of carbon nanotubes differs from that of graphene and depends on the extract structure and shape of the carbon nanotube ranging from metallic to semiconductor behaviour [51]. Carbon nanotubes have been used to realize single-electron transistors and QDs [52].

A challenge associated with graphene and carbon nanotubes is scaling and handling. Fabrication of graphene or carbon nanotube devices requires manual manipulation of small graphene sheets or individual nanotubes complicating the fabrication and increasing the time cost of producing devices.

Nanowires grown via the vapour-liquid-solid (VLS) method have been a very important platform for quantum electronics experiments. The benefits of the VLS NWs is that they can have an extremely high crystal purity and few defects [53, 54] and electrons are confined to a quasi-1D channel by the high aspect ratio crystal structure. Amongst the most popular materials for VLS growth are InAs and InSb - II-I/V semiconductors with low m^* (0.023 and 0.015 respectively) [55] although other materials such as GaAs, GaN, and Si are also used in this geometry. In the case of InAs and InSb conduction electrons are confined near the surface of the NW due to surface states and ohmic contacts can be readily made to these NWs after removal of native surface oxide [56].

Similar to graphene and carbon nanotubes, the principal drawback of out-of-plane NWs is the need to transfer the NWs unto another substrate for device fabrication which complicates the process of fabricating large numbers of individual devices. Although devices have

been realized directly on as-grown out-of-plane nanowires [57–59], the device geometry is severely limited in this configuration allowing only simple devices. To realize complex devices implementing multiple local gates on VLS NWs it is beneficial to first lay down the NWs onto an insulating substrate [60]. This can be achieved either by micromanipulation, bulk mechanical transfer using e.g. a cleanroom wipe, or by drop-casting from a solution. Precise positioning of the NWs has been shown using electric fields to manipulate the NWs [61, 62], however, this adds a layer of complexity to scalable device fabrication

A relative newcomer to the field of semiconductor electronics is selective area growth (SAG). The concept of SAG - growth of crystalline nanoscale structures in positions lithographically defined by a mask - dates as far back as 1977 [63] and truly selective growth on the substrate but not the mask was already achieved in 1984 [64]. However, semiconductor SAG as well as a related process - template assisted selective epitaxy (TASE) - structures have only recently gathered widespread interest as a platform for quantum electronics [12, 65–72]. The promise of SAG is to combine the scalability of 2DEGs with the intrinsic crystal confinement of VLS NWs. Selective area growth NWs are at the core of the work presented here and will be discussed in more detail in the following Section.

2.2 Selective Area Growth

The SAG Process

Selective area growth aims to combine the benefits of bottom-up VLS NW growth with the versatility and scalabilty of 2DEGs. Selective area growth of semiconductor materials takes advantage of the thermodynamics and kinetics of adatoms to promote growth only in defined regions of the growth substrate by means of a lithographically patterned mask.

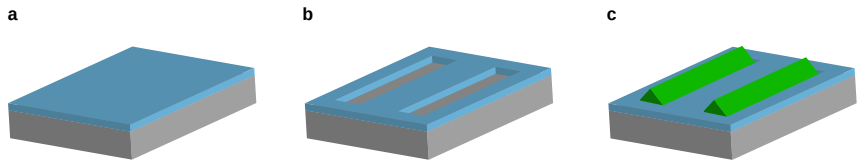


Figure 2.1: **a** Growth substrate (gray) with mask (blue). **b** Openings for SAG are patterned into the mask. **c** NW growth in the mask openings (green).

The growth substrate is first covered by a thin mask - typically silicon oxide or silicon nitride (Fig. 2.1a) and openings defining the positions and geometry of the growth are lithographically patterned and etched into the mask to expose the underlying substrate (Fig. 2.1b). During growth the process parameters are fine-tuned such that material growth happens only on the exposed substrate surfaces while adatoms on the mask desorb resulting in selective growth (Fig. 2.1c). Growth of SAG structures can be realized by molecular beam epitaxy (MBE) [73], metalorganic vapor phase epitaxy [12], chemical beam epitaxy, and other processes [74]. The SAG NWs used in this study

were grown by MBE, hence in this Section focus will be on the MBE process.

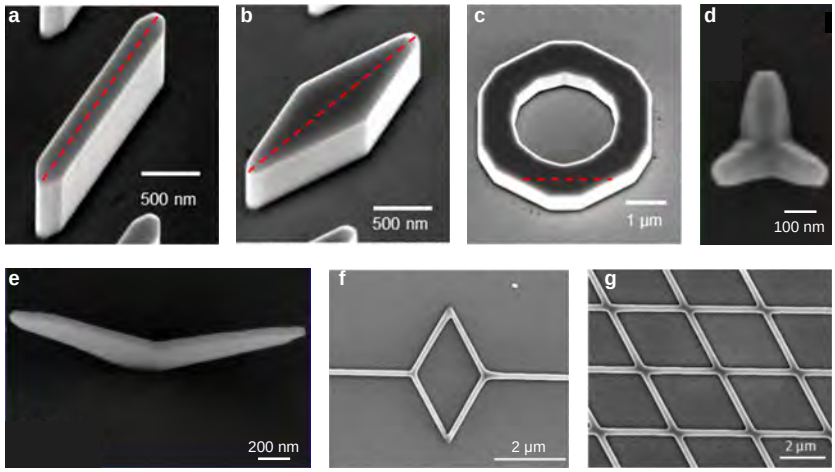


Figure 2.2: **a,b** SAG nano-membranes/fins. **c** SAG in-plane ring. **d** "tripod" shaped SAG nano-membrane. **e** "V-shaped" SAG nano-membrane, contact with substrate in center. **f** network of in-plane SAG NWs forming an Aharonov-Bohm ring like geometry. **g** periodic lattice network of in-plane SAG NWs. Panels a-c from [69], d, e from [65], and f, g from [75]

Selective area growth has been used to grow catalyst-free out-of-plane NWs as well as nano-membranes of various shapes such as fins, tripods, v-shapes, and rings [65–69] and importantly as in-plane NWs and NW networks [12, 70–72] examples of which are shown in the SEM micrographs in Fig. 2.2. Bottom-up grown out-of-plane NWs provide benefits such as crystal confinement of electrons and high crystal purity compared to 2DEGs where confinement has to be achieved either by etching which introduces defects or by electrostatic gating which does not achieve hard confinement and complicates device geome-

try [35, 36, 38, 76]. On the other hand, out-of-plane NWs are often limited in device geometry without manual redeposition onto another substrate and can only have very few epitaxial interconnects between NWs. In-plane NWs and NW networks provide an attractive scalable alternative to out-of-plane NWs with simplified post-growth device fabrication and potential for multiple interconnects between NWs while retaining the crystal quantum confinement of large aspect-ratio NWs.

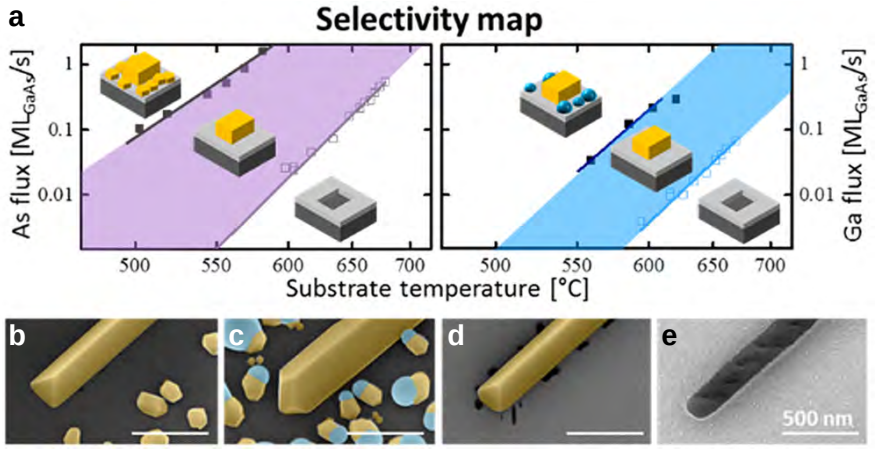


Figure 2.3: **a** Selectivity map showing growth modes for different combinations of substrate temperatures and III/V fluxes for GaAs. **b** parasitic III-V crystallite growth on mask surface alongside monocrystal growth inside mask opening. [c] III and III-V cluster formation on the mask alongside III-V monocrystal growth inside the mask opening. **d** Perfectly selective III-V monocrystal growth inside the mask opening. **e** Decomposition of III-V crystal (no growth). Figure adapted from [75]

Due to the ultra-high vacuum and lack of precursor chemicals, the MBE process can realize extremely high purity crystals [54]. However, optimizing the growth can be challenging due to many tunable param-

eters such as temperature, flux, the III/V-ratio, and the dimensions and density of the grown structures. Fig. 2.3 shows the possible processes for GaAs SAG growth [75]. Depending on the growth conditions nucleation can occur either as crystallites on the mask as well as single crystalline growth inside the mask openings (Fig. 2.3b), formation of III/III-V clusters on the mask along the single crystalline growth inside the mask openings (Fig. 2.3c), selective growth of III/V single crystal inside the mask openings (Fig. 2.3d), or no growth anywhere on the sample (Fig. 2.3e) [75]. For III/V SAG, the substrate temperature and III/V fluxes are tuned such that adatoms have an effective zero sticking coefficient on the substrate mask and a non-zero sticking coefficient on the growth substrate in the mask openings [70, 75], this leads to crystal growth on the substrate inside the mask openings while minimal growth occurs on the mask itself.

Interface Optimization

A challenge for SAG NWs is the NW-substrate interface, as the NWs are grown in-plane on the substrate there is a bi-crystal interface between the substrate and the NW. It is also generally not useful to grow semiconductor NWs directly on a substrate of the same material as typically it is desired for the substrate to be insulating to allow direct fabrication of devices on the as-grown sample. These aspects limit the options for substrate/NW material combinations.

Typically there will be a significant crystal lattice mismatch between the NW material and the substrate leading to strain and defect generation at the bi-crystal interface. A mismatch in lattice constants forces the NW crystal lattice to deform elastically to match the crystal lattice of the substrate inducing strain in the lattice. For a strained interface it may at some thickness become energetically favourable to relax the strain at the interface inelastically by forming misfit dislocations [77].

Furthermore, the surface of the growth substrate is typically damaged during the etching of the mask and the pre-growth annealing (Fig. 2.4, left) which is necessary to remove the surface oxide before growth [72]. This poses a challenge as the damaged substrate surface induces a large number of crystal defects. Additionally, intermixing of material from the substrate and the NW material occurs in these heteroepitaxial systems leading to further degradation of crystal quality [78–80].

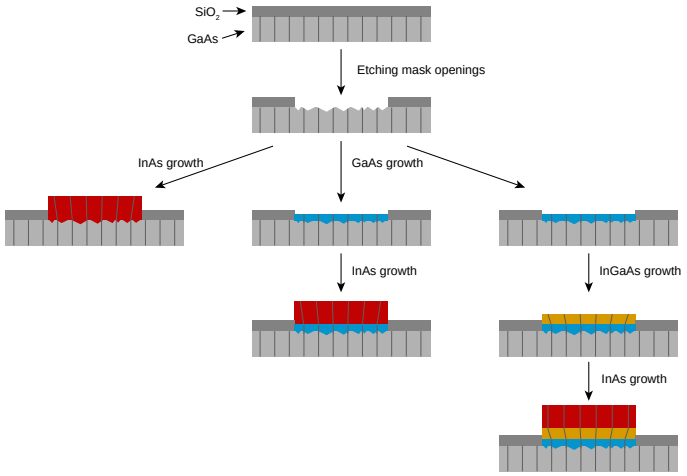


Figure 2.4: Simplified schematic representation of InAs SAG NW growth steps. Left: InAs growth directly on the damaged GaAs substrate. Middle: InAs growth with an intermediary homoepitaxial GaAs buffer. Right: InAs growth with a homoepitaxial GaAs buffer and heteroepitaxial InGaAs buffer. Lines represent simplified crystal lattice planes to illustrate strain.

These crystal defects act as electron scattering sites and charge traps, consequently this leads to degraded electrical performance of the SAG nanostructures evidenced by reduced charge carrier mobil-

ity. Defects may also cause hysteretic electric field response, and large device-to-device variance observed when when operating topgated devices at low charge carrier concentrations as the charge carriers are pushed towards the defect-rich bi-crystal interface by the gate electric field [72].

The problems arising from the bi-crystal interface can be partially mitigated by growing a buffer layer on the substrate prior to the growth of the active transport layer. Growth of a homoepitaxial buffer (Fig. 2.4, middle) helps reforming the crystal structure of the growth substrate damaged by pre-growth processing resulting in a cleaner interface with the NW by trapping defects and contaminants at the substrate-buffer interface [72]. Experiments on NW field effect transistor devices have shown that reduction of interface defects created by substrate processing by the introduction of a homoepitaxial buffer layer greatly reduces gate hysteresis and ensures that NWs can be consistently pinched off at similar threshold gate voltages [72]. Reported values of charge carrier field effect mobility in in-plane InAs SAG NWs with homoepitaxial buffers at millikelvin temperatures are typically in the range of $500 - 5000\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ [18, 72].

Additionally, intermediary buffers can be grown between the homoepitaxial buffer and the desired NW material (Fig. 2.4, right) to ensure most of the elastic and inelastic relaxation due to lattice constant mismatch takes place at the buffer-substrate interface trapping defects further away from the electron transport channel thus improving the device electrical performance [81]. It has been shown that by confining relaxation induced defects and material intermixing to a heteroepitaxial buffer layer thus spatially separating these from the conduction channel it is possible to effectively double the field effect mobility compared to structures with only a homoepitaxial buffer. This allows to achieve electron mobility values of $> 10^4\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ [81] which is comparable to mobility values reported in VLS InAs NWs -

typically in the range $2 \cdot 10^3 - 2 \cdot 10^4\,\mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$ [82–85]

SAG NW Geometry

An important advantage of SAG NWs is the possibility of epitaxial NW interconnections between NWs with different orientations which enables the growth of in-plane NW networks [12, 72] relaxing the 1D constraint of VLS NWs. Epitaxial interconnects are challenging to realize in VLS NWs as the NWs cross during axial growth and merge by radial growth. This requires precise NW catalyst positioning and multiple growth directions from the substrate. Due to these restrictions only fairly few interconnects such as a cross-shape have been realized [73, 86].

The ability to create such interconnected networks in in-plane SAG NWs provides much more flexibility in device design allowing for better characterization of electron transport in these structures by enabling more sophisticated electronic devices such as Hall bars (Fig. 2.5a) or Aharonov-Bohm ring-like geometries (Fig. 2.5b). These are standard geometries on 2DEG systems but are very difficult to achieve on single NWs [12, 72, 75, 87, 88]. NW networks are also a crucial building block in some proposed quantum computing schemes [28]. It has been shown that ballistic electron transport is possible through such in-plane NW interconnects realized by SAG or TASE [72, 89] which is crucial for transfer of quantum information between components in quantum electronic networks where coherence of 1D states needs to be maintained [89].

However, a constraint to the geometry of NW structures and networks is crystal symmetries. The NW growth directions are constrained to high-symmetry crystal directions [12, 75]. The crystal direction also dictates the NW facets and thus the shape and morphology of the NW via surface free energy minimization and growth kinetics [75, 90]. These aspects should be taken into account when

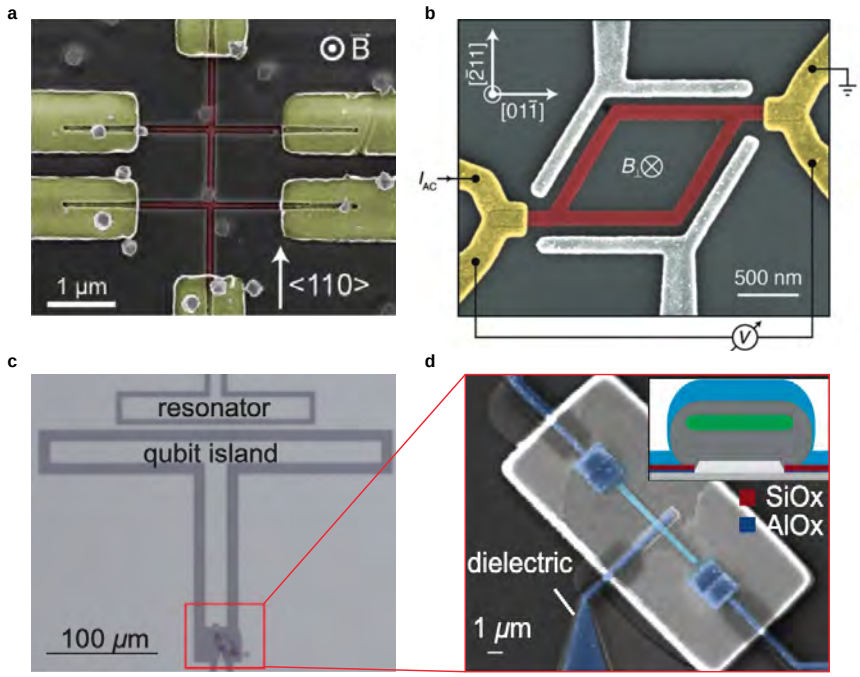


Figure 2.5: **a** SEM micrograph of Ge SAG Hall bar device. Ge in red, Ti/Au contacts in gold. **b** SEM micrograph of a PbTe SAG Aharonov-Bohm ring . PbTe in red, Ti/Au contacts in gold. **c** Optical microscope micrograph of an InAs/Al SAG NW based gatemon qubit. **d** SEM micrograph of the area in the red square in c showing the Josephson junction of the gatemon qubit. Al contacts and leads in blue. Panel a from [87], panel b from [88], panels c and d from [20].

designing experiments that require multiple directions of NWs and makes the choice of growth substrate crystal orientation an important consideration [75].

Selective area growth is also compatible with in-situ deposition of superconductor after semiconductor growth which allows to realize semiconductor-superconductor hybrid NW devices with a pristine

interface between the two materials [73]. In such hybrid systems superconductivity is induced in the semiconductor via the proximity effect and the pristine interface is an important factor in realising an induced superconducting gap with a low density of subgap states which is required to reduce the quasiparticle poisoning rate [91, 92]. The interaction between the superconductor and semiconductor properties enables the formation of topologically (non-)trivial bound states in the system which are important building-blocks for proposed quantum information and quantum computing applications as well as the realisation of gate-tunable Josephson junctions which are crucial components in gatemon qubit designs [93, 94].

Selective area growth provides flexibility in semiconductor shape and circuit design while also retaining crystal confinement of electrons. The platform is well-suited for fabricating large numbers of devices and scalable circuits as the NW positions and dimensions are lithographically defined. It is also possible to realize complex interconnected NW networks. On the other hand, due to the in-plane growth axial structures are not possible [12] and substrate-NW material combinations are limited as non-matching lattice constants lead to crystal degradation and leakage through the substrate is a concern. While there are challenges originating from the NW-substrate interface, ongoing advances in growth methods continuously improve the material quality. In terms of electron mobility, the platform can stand up to traditional material platforms such as VLS NWs. However, the prospects of scalability promised by the platform have not yet been adequately taken advantage of in existing research.

While SAG NWs are unlikely to replace complementary metal-oxide-semiconductor (CMOS) as the technology of choice for industry-scale quantum devices, scalable SAG circuits can be invaluable tools in exploratory research that does not warrant the cost of CMOS foundry

production lines. Functional circuits based on SAG NWs could be integrated into the standard research laboratory fabrication flows as a part of the experimental device fabrication. In this work steps are taken to address the aspects of scalability and large-scale characterization of quantum electronic circuits based on SAG NWs.

3

3 Materials and Methods

3.1 SAG NWs Used in This Study

The nanowires investigated in this study are $[0\,1\,\bar{1}]$ oriented InAs SAG NWs grown on a semi-insulating GaAs (3 1 1)A substrate by molecular beam epitaxy (MBE). The NW positions are defined by a 10 nm SiO_2 mask layer deposited on an epi-ready GaAs substrate via plasma enhanced chemical vapour deposition; openings in the mask are defined by electron beam lithography (EBL) and inductively coupled plasma reactive ion etching (ICP RIE). The NWs were grown and analyzed via atomic force microscopy (AFM) by Gunjan Nagda.

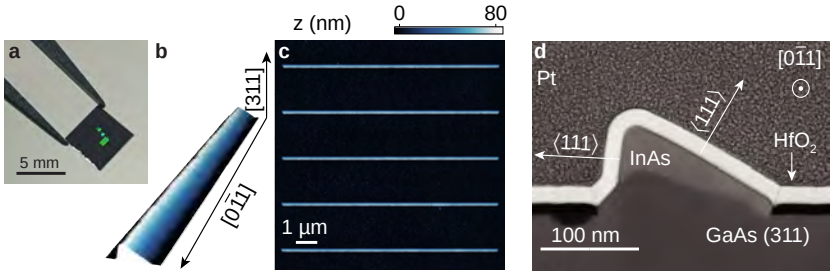
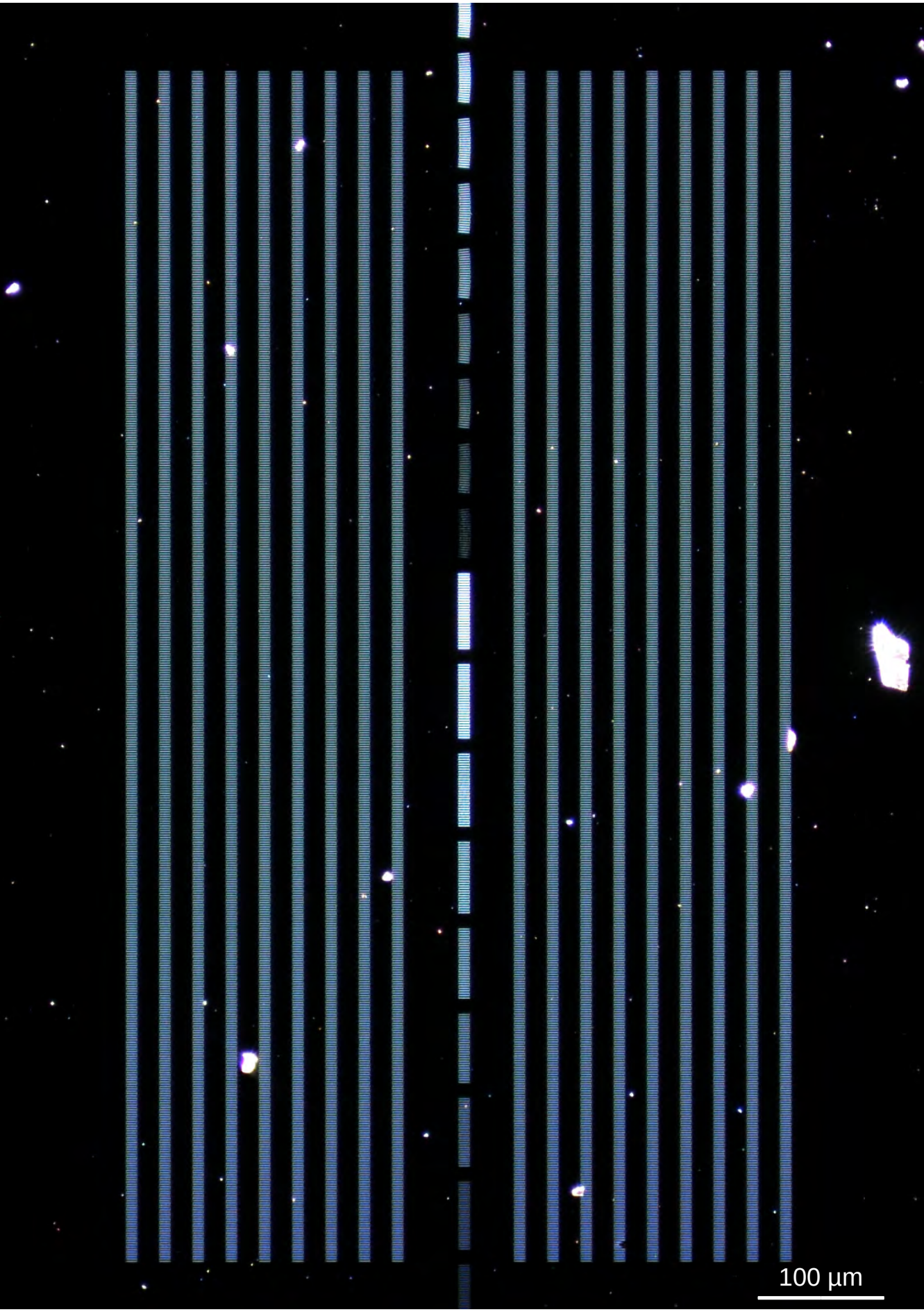


Figure 3.1: **a** Photograph of a chip from the SAG growth wafer. The large nanowire arrays can be seen by the naked eye in green as a result of interference of the reflected light from the periodic structures. **b** 3D render of an AFM scan of a single SAG NW. **c** AFM micrograph of 5 SAG NWs from the large array. **d** Cross-section TEM micrograph of the SAG NW. The asymmetric shape is due to the (3 1 1) crystal orientation of the growth substrate. (AFM data credit: Gunjan Nagda; TEM credit: Sara Marti-Sanchez, Jordi Arbiol)


100 µm

A GaAs(Sb)/InAs double layer is selectively grown in the openings where the GaAs(Sb) buffer is introduced to improve the crystal surface before the growth of the InAs NW as described previously in Section 2.2. A 3D render of an AFM scan of a single NW is shown in Fig. 3.1b and a cross-section TEM micrograph of a typical NW is shown in Fig. 3.1d. As a result of the (3 1 1) orientation of the substrate the resulting NWs have an asymmetric cross-section. The asymmetric shape of the NWs is not relevant for the reproducibility and scalability aspects of the study which could equally well have been based on conventional (1 1 1) or (1 0 0) substrates.

As discussed in Section 2.2 the possibility of scaling the growth is a key feature of SAG. In this regard, one of the open questions in SAG growth is the reproducibility of NWs when grown nominally identical. A darkfield optical microscope micrograph shown on page 27 shows an example of a large NW array. The NW array is large enough to be seen by the naked eye (Fig. 3.1a). The SAG NW arrays are visible in green by the naked eye due to interference of light reflected from the large periodic structures. The growth windows in the mask were arranged in two equal 512×8 arrays of $10 \times 0.15\,\mu$m rectangular openings with pitches between openings $\Delta x = 30\,\mu$m and $\Delta y = 2\,\mu$m. As an example, 5 SAG NWs from these arrays are shown in Fig. 3.1c.

The $100\,\mu$m gap between the arrays contains arrays of openings with widths varying from 80 nm to 300 nm and misalignment to the $[0\,1\,\bar{1}]$ direction of up to $\pm 5^\circ$ with a step size of 0.5°. The effect of the misalignment and NW dimensions will be explored in Chapter 6. However, before delving into this, the basics of device fabrication and cryostat operation will be discussed.

3.2 Device Fabrication Basics

Devices incorporating SAG NWs are fabricated directly on the as-grown substrate using the growth design as reference for NW positions. The growth design includes cross-shaped alignment marks which are used for aligning the lithography steps used for defining gates and contacts. A simplified schematic of the device fabrication process of a NWFET device is shown in Fig. 3.2 and detailed recipes used for device fabrication are described in Appendix A.

Electron beam lithography (EBL) is used to define openings in a PMMA resist mask. The secondary electrons induced by the primary beam break down the polymer bonds making exposed areas soluble in MIBK (Fig. 3.2b, c). With proper optimization this technique allows to define features with a characteristic scale $< 10\,\text{nm}$. Metal is then deposited on the sample using electron beam evaporation. To realize ohmic contact to the InAs NWs it is necessary to remove native oxide form the NW surface prior to deposition of the metal. Here Ar ion RF milling is used inside the electron beam evaporator chamber for oxide removal and Ti/Au contacts are deposited immediately after (Fig. 3.2d, e). The thickness of the contacts depends on the topography of the sample - if the contacts must climb steep inclines their thickness should be increased. For the SAG NWs in this work 150 nm is sufficient. A small (5 nm) Ti layer is necessary to ensure sticking of Au to the SiOx surface of the SAG mask. The PMMA mask is subsequently removed by acetone lifting off metal from the masked areas and leaving it only in the patterned locations (Fig. 3.2f).

Topgates and metal lead crossings are realized by depositing a global dielectric layer using atomic layer deposition (ALD). A nominally 15 nm layer of HfO_2 is grown after the deposition of the contacts

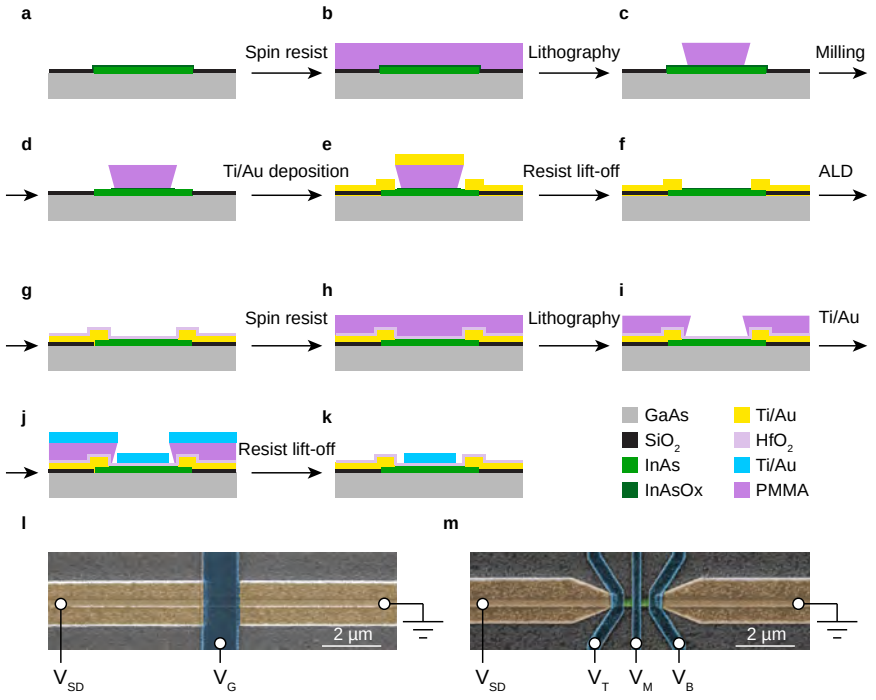


Figure 3.2: **a-k** Simplified schematic illustrations of key aspects of the device fabrication process, cross-section view. GaAs substrate in gray, SAG SiO_2 mask in dark gray, InAs NW in green, InAs native oxide in dark green, PMMA resist in purple, Ti/Au ohmic contacts in yellow, HfO_2 in pink, Ti/Au topgate in blue. **l (m)** SEM micrograph of a finished NWFET (QD) device, top view. Ti/Au ohmic contacts in gold, Ti/Au topgate in blue.

(Fig. 3.2g). Ti/Au gates are then fabricated using the same process as for the contacts excluding milling as oxide removal is not necessary in this step (Fig. 3.2h-k).

Fabricating dense interconnected device designs over a large area it is also important to ensure the amount of particulate on the device substrate is minimised. A piece of dust in the wrong place can, for

example, cause a discontinuity in a gate control line that is shared by hundreds of devices by obscuring lithography or metal deposition. Metal that has not properly lifted off can short an FET that is responsible for correctly addressing devices. To minimise the chance of dust settling on the sample it is transported face-down in a closed concave box. Prior to important fabrication steps the sample is examined in a darkfield optical microscope for any large particles and ultrasound cleaning is used if necessary to remove any particulate.

3.3 Cryogenic Measurement Setup

Low-temperature measurements were carried out in an Oxford Triton dry dilution refrigerator. A dilution refrigerator achieves cooling through continuous mixing of ^{3}He and ^{4}He - an endothermic reaction. A schematic of the cooling circuit is shown in Fig. 3.3a. During cooldown the ^{3}He/^{4}He gas mixture is first cooled down in the pre-cool circuit (red) using a pulse tube cooler, the gas is circulated passing through heat exchangers to also cool the dilution unit. When the system reaches a temperature of 10 K the pre-cool loop is evacuated and isolated [95].

The mixture is further cooled and condensed in the dilution circuit (green), the mixture is first compressed and then passed through a series of heat exchangers on the pulse-tube cooler to reduce the temperature of the gas to about 4 K. The mixture is then cooled even further using the Joule-Thomson effect, where the gas is throttled and undergoes an isenthalpic expansion. The mixture then reaches the dilution unit. Inside the mixing chamber there is a saturated mixture of ^{3}He in ^{4}He (dilute phase) and a phase of pure liquid ^{3}He (saturated phase). This phase separation is possible due to the finite miscibility of ^{3}He and ^{4}He below a temperature of about 870 mK. The mixing chamber is connected to a still, where evaporation of ^{3}He from the ^{3}He/^{4}He mixture takes place. The still is pumped on by a vacuum pump to promote evaporation of ^{3}He. Due to a difference in partial pressures between ^{3}He and ^{4}He at sub-Kelvin temperatures, the vapor phase in the still is $\sim$ 90% ^{3}He. The evaporation of ^{3}He in the still creates an osmotic pressure drawing ^{3}He from the saturated phase across the phase boundary into the dilute phase in the mixing chamber. The ^{3}He evaporated from the still is recondensed and returned

to the mixing realising a closed-loop [95].

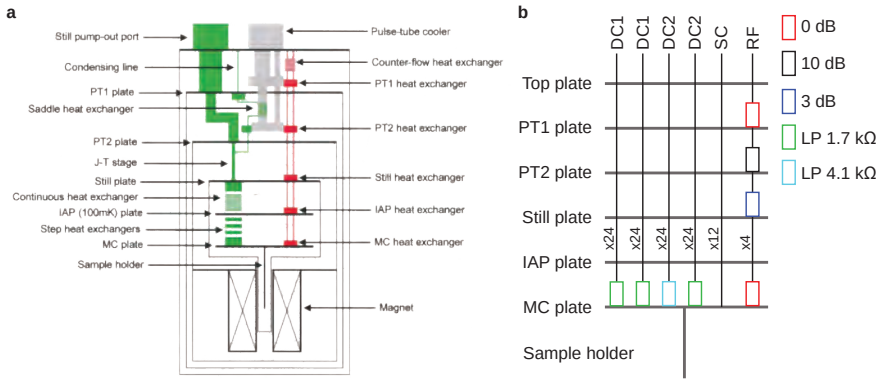


Figure 3.3: **a** Schematic of the cooling circuit in an Oxford Triton 200/400 dilution refrigerator. The dilution circuit is is shown in green and the pre-cool circuit is shown in red. Schematic adapted from [95]. **b** Schematic of the transmission lines in the specific cryostat used for the cryogenic measurements in this work. The cryostat has 96 filtered DC lines, 12 unfiltered superconducting lines, and 4 filtered RF lines.

The experiment electrical wiring in a dilution refrigerator depends on the specific setup. A schematic of the wiring in the dilution refrigerator used in the measurements presented in this work is shown in Fig. 3.3b. This cryostat has 4 filtered RF lines for high frequency signal transmission, 12 unfiltered superconducting (SC) lines for flux-biasing, and 96 filtered DC lines for low frequency signal transmission. Only the DC lines were used for the measurements presented here. The filters in these transmission lines are multi-stage low-pass (LP) filters incorporating both pi-filters and RC filters. The pi-filters have a cutoff frequency of $\sim 1\,\mathrm{MHz}$ and the RC filters have a cutoff frequency of $\sim 5\,\mathrm{kHz}$. The cryostat is also equipped with a superconductor vector magnet with a maximum magnetic field of $1\,\mathrm{T}$, $1\,\mathrm{T}$, and $6\,\mathrm{T}$ for the three sets of coils.

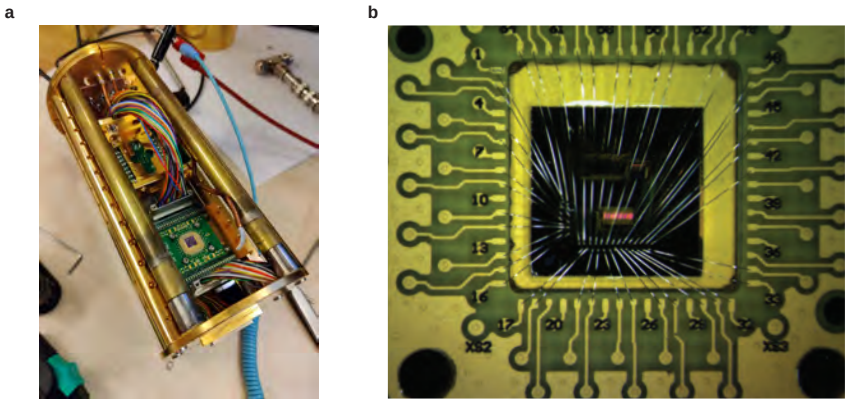


Figure 3.4: **a** A photograph of a puck (outer shell removed) used to load samples into the cryostat and establish electrical connections between the sample and the fridge wiring. In this configuration two samples with up to 48 DC connections each can be loaded. **b** Optical microscope micrograph of device chip adhered to the daughterboard. Aluminium bonds are used to connect the device leads to the daughterboard pins.

The samples are loaded into the cryostat using a cylindrical metal enclosure known as a "puck", a photogaph of which is shown in Fig. 3.4a (without the outer shielding). The puck realizes both thermal and electrical contact between the sample and the cryostat. The puck shown in Fig. 3.4a is configured to accept two samples on the two motherboards with up to 48 DC connections each. After fabrication the device substrate is adhered to a daughterboard by silverglue, PMMA, or epoxy, connections between the device leads and the daughterboard pins are established using aluminium bondwire as shown in Fig. 3.4b. The daughterboard containing the sample is mounted to the motherboard in the puck by screws. Electrical contact between the daughterboard and the motherboard is established by an interposer containing gold-plated beryllium copper fuzz-buttons.

The density of electrical connections in the photographs in Fig. 3.4 should be noted. As mentioned in Section 5.2, space is a limiting factor for the number of devices in cryogenic electronic measurements. Considering the physical dimensions of the puck and the density of the bonds it would be unfeasible to achieve e.g. 10 times as much connections in the same way.

4

4 Cryogenic Multiplexers

4.1 Off-Chip Multiplexing

One way to overcome the limitation on the number of electrical connections in cryogenic measurements is to make the best use of the available transmission lines by including a multiplexer in the measurement circuit. A multiplexer circuit enables addressing of a large number of outputs using few control lines thus allowing to scale the number of available devices on-chip without increasing the number of transmission lines in the cryostat.

One challenge to consider when implementing additional logic elements is the extreme environment that these circuits must reliably operate in. Quantum electronic devices are typically operated at $T < 1\,\mathrm{K}$ and often at high magentic fields. Nevertheless, it has been shown that both off-the-shelf cryogenic CMOS multiplexers [6] as well as custom CMOS multiplexer circuits [96] can be integrated off-chip into the measurement circuit and operated successfully.

There are benefits of keeping the multiplexer circuit off-chip. First, this approach is independent of the material used in the experimental devices on-chip. Second, the fabrication process of the experimental devices is not affected. No additional fabrication steps are necessary as the multiplexer circuit can be bought off-the-shelf or the fabrication can be outsourced to a CMOS foundry [96]. However, the drawback of keeping the multiplexer off-chip is that connections between the multiplexer outputs and the on-chip devices will typically still have to be made via bondwires. While modern auto-bonders can make a large number of bonds automatically there is still limited space for bondpads on-chip.

4.2 SAG NW Transistors

To address both the limitations imposed by the number of transmission lines and bondpads an on-chip circuit will be considered with FETs being the core element of the circuit. The focus of this work is InAs SAG NWs, thus it is important to establish whether SAG NWFETs incorporating single or multiple NWs in parallel feature robust ON/OFF states when operated at two extreme values of gate potential exceeding the scale of any inter-NW variation.

To fabricate devices, ohmic Ti/Au contacts are realized using standard fabrication techniques and 15 nm of HfO_2 deposited by atomic layer deposition separates the NWs from Ti/Au top gates as described in Section 3.2. A step-by-step walkthrough of the fabrication process is provided in Appendix A.

Single NW Transistors

First, consider a simple NWFET using a single InAs SAG NW as the gate-tunable $1\,\mu$m long semiconductor channel as shown in Fig. 4.1a. Figure 4.1b shows I_{SD} as a function of V_G on a logarithmic scale for an NWFET device at various source drain bias voltages $V_{SD} = 1\,\text{mV}$, $2\,\text{mV}$, $3\,\text{mV}$, $4\,\text{mV}$, $5\,\text{mV}$ at a temperature of $5.5\,K$.

The NWFET has a negative V_{TH} and can be pinched off by applying negative gate voltage V_G exhibiting typical n-type transistor behaviour as expected from InAs NWs [60, 97]. The device can be pinched off to the measurement noise-floor at all investigated values of V_{SD} and the ON/OFF ratio varies from $\sim 10^3$ to $\sim 10^4$ in the investigated source-drain voltage range.

By fitting a linear function to the subthreshold region the average subthreshold slope is $\sim 11\,\text{mV/dec}$ at a temperature of $5.5\,\text{K}$ while the

thermionic limit at this temperature is 1 mV/dec. The increase in the subthreshold slope above the thermionic limit points to detrimental interface states at the gate dielectric [60, 98, 99].

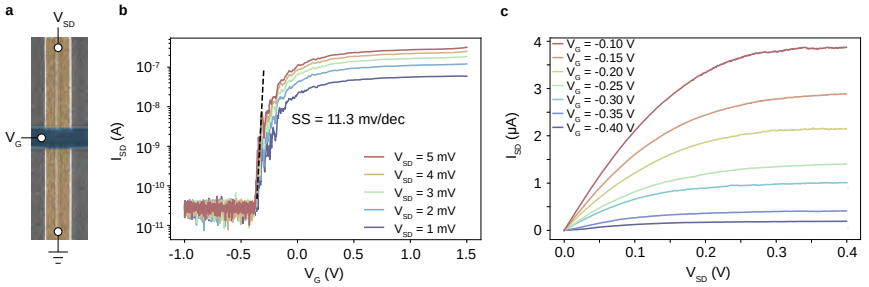


Figure 4.1: **a** SEM micrograph of a SAG NW-base FET device. Ti/Au ohmic contacts in gold, and a Ti/Au topgate separated from the semiconductor by 15 nm of HfO_2 in blue. **b** Subthreshold region of I_{SD} at different applied V_{SD}. The subthreshold slope is 11.3mV/dec. **c** I_{SD} through a SAG NWFET as function of applied V_{SD} at various V_G. The current saturates to different values based on applied gate potential.

Exploring the output characteristics of the SAG NWFET Fig. 4.1c shows the transistor source-drain current I_{SD} as function of V_{SD} at different values of V_G. The NWFET exhibits gate voltage dependent current saturation with I_{SD} saturating to $I_{SDS}(V_G)$. This is important FET behaviour which allows to potentially use such SAG NWFETs as constant current sources/sinks or amplifiers in on-chip circuits [99, 100].

FETs Consisting of Multiple NWs

Next, consider NWFETs consisting of multiple SAG NWs connected in parallel. Using multiple NWs connected in parallel as the active elements of the NWFETs yields important benefits. First, it increases the overall ON-state conductance of the NWFET leading to a

lower series resistance when used as a part of a larger circuit. Second, the conductance fluctuations present in the individual NWs at millikelvin temperatures are averaged out resulting in a more consistent conductance curve and reducing the variability of elements [101–103]. Finally, it also functions as an important redundancy - as it is possible in rare cases for NW growth to be inhomogeneous or discontinuous, incorporating multiple NWs protects against possible broken conductance channels leading to non-functional transistors in the circuit.

Figure. 4.2a shows an SEM micrograph of a device similar to the one in Fig. 4.1a consisting of four parallel NWs from the NW array connected in an FET geometry with a channel length of 1 μm. Ohmic contacts are shown in gold and two top-gates are shown in blue/gray. For this device the gate shown in gray is screened by the ohmic contact underneath as illustrated in the cross-section schematic in Fig. 4.2b and is inactive.

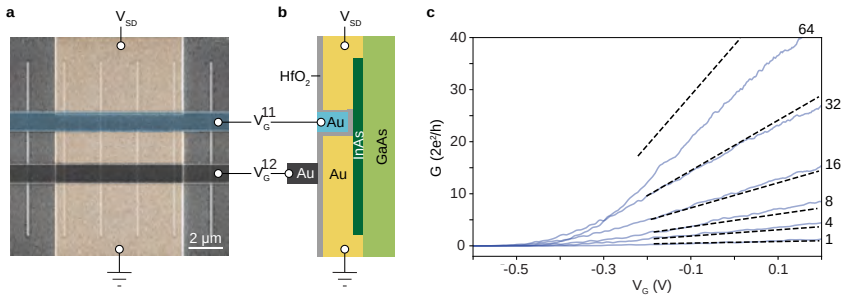


Figure 4.2: **a** SEM micrograph of a NWFET based on 4 SAG NWs, Ti/Au Ohmic contacts in gold, Ti/Au gate in blue. The gate in dark gray is screened by the underlying ohmic contact as shown in b. **b** Cross-section schematic of the device in a. **c** Conductance as function of V_G for NWFETs based on 1, 4, 8 ,16, 32, and 64 SAG NWs in parallel.

Figure 4.2c shows the conductance as a function of V_G for NWFET

devices with different numbers N (indicated next to each trace) of NWs connected in parallel analogous to the geometry of the device in Fig. 4.2a after subtraction of a constant series resistance of the circuit R_s. As before, the devices act as n-type FETs with a threshold voltage $V_{TH} \sim -0.4\,V$ and the dashed lines show the linear trend expected in the case where each NW contributes equally to the conductance $G = N \cdot m(V_G - V_{TH})$ where $m = 1.5\,2e^2/hV$. Importantly, all NWs can be brought into pinch-off with V_{TH} varying by $< 100\,mV$ between devices allowing the use of large-N SAG NWFETs as building blocks for larger interconnected SAG circuits.

The results from these measurements show that NWFETs based on single or multiple InAs SAG NWs exhibit robust ON/OFF states even when a large number of NWs are used in parallel as the active elements. This shows that, together with the simplified scalability and fabrication of SAG compared to VLS NWs, such NWFETs are suitable for use as building blocks of on-chip electronic circuits.

Modelling Gate Capacitance of NWFETs

The gate capacitance of an NWFET is an important parameter for analysis e.g. for extracting field-effect mobility [104]. However, this value is difficult to measure directly. As capacitance depends on the materials and geometry of the system, modelling can be used for an estimate.

Gate capacitance for single-NW FET devices is estimated using the ANSYS® Electronics Desktop 2021 R2 software. Model NWFET devices are rendered based on measurements from AFM, SEM, and cross-section TEM for lengths 50 nm, 300 nm, 800 nm, 3 μm, and 6 μm of the semiconductor NW segment. An example model is shown in Fig. 4.3a. The Maxwell3D module of the software models electrostatics using finite element analysis and solves Maxwell's equations [105] in a finite region of space [106]. From the resulting values shown in

Fig. 4.3b a capacitance C per unit length L of $\sim 5.4\,\mathrm{fF}/\mu\mathrm{m}$ is extracted to find the capacitance for other NW segment lengths.

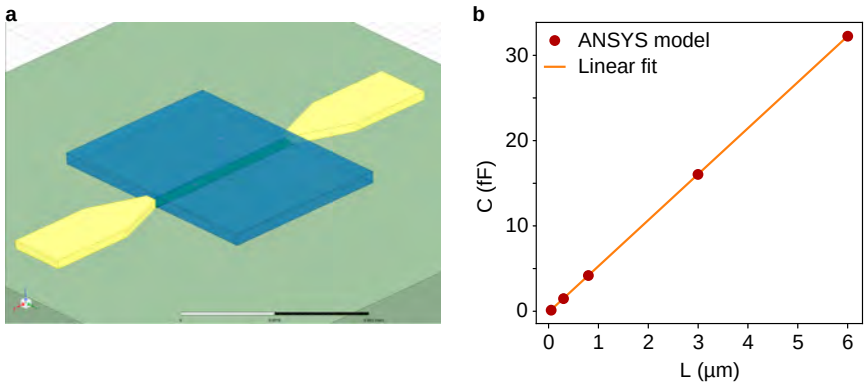


Figure 4.3: **a** 3D model of a NWFET device with a $3\,\mu\mathrm{m}$ long InAs channel rendered in ANSYS software based on AFM, SEM, and TEM measurements. Ti/Au contacts in yellow, Ti/Au topgate in blue **b** Capacitance values calculated by the model for different InAs channel lengths and linear fit to the results.

4.3 SAG Multiplexer

SAG-Based Multiplexer-Demultiplexer Circuit

A key result of this thesis is to demonstrate that using the scalability of SAG NWs it is possible to realize complex on-chip circuits incorporating thousands of individual NWs such as a multiplexer circuit described already in Section 4.1.

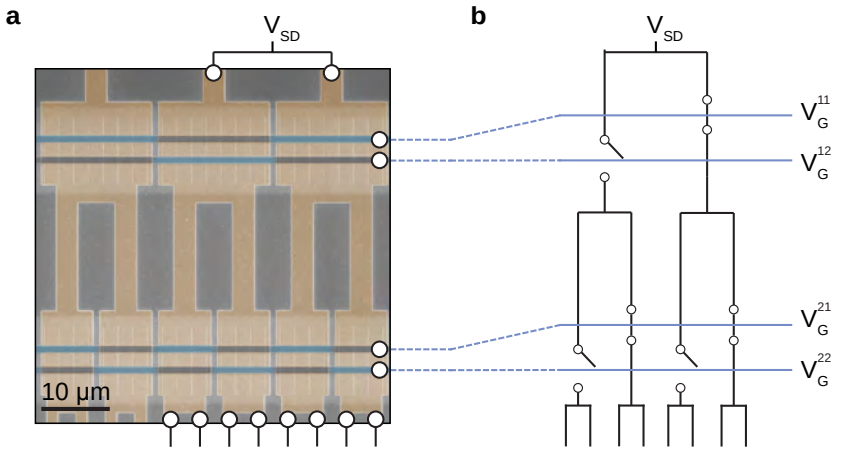
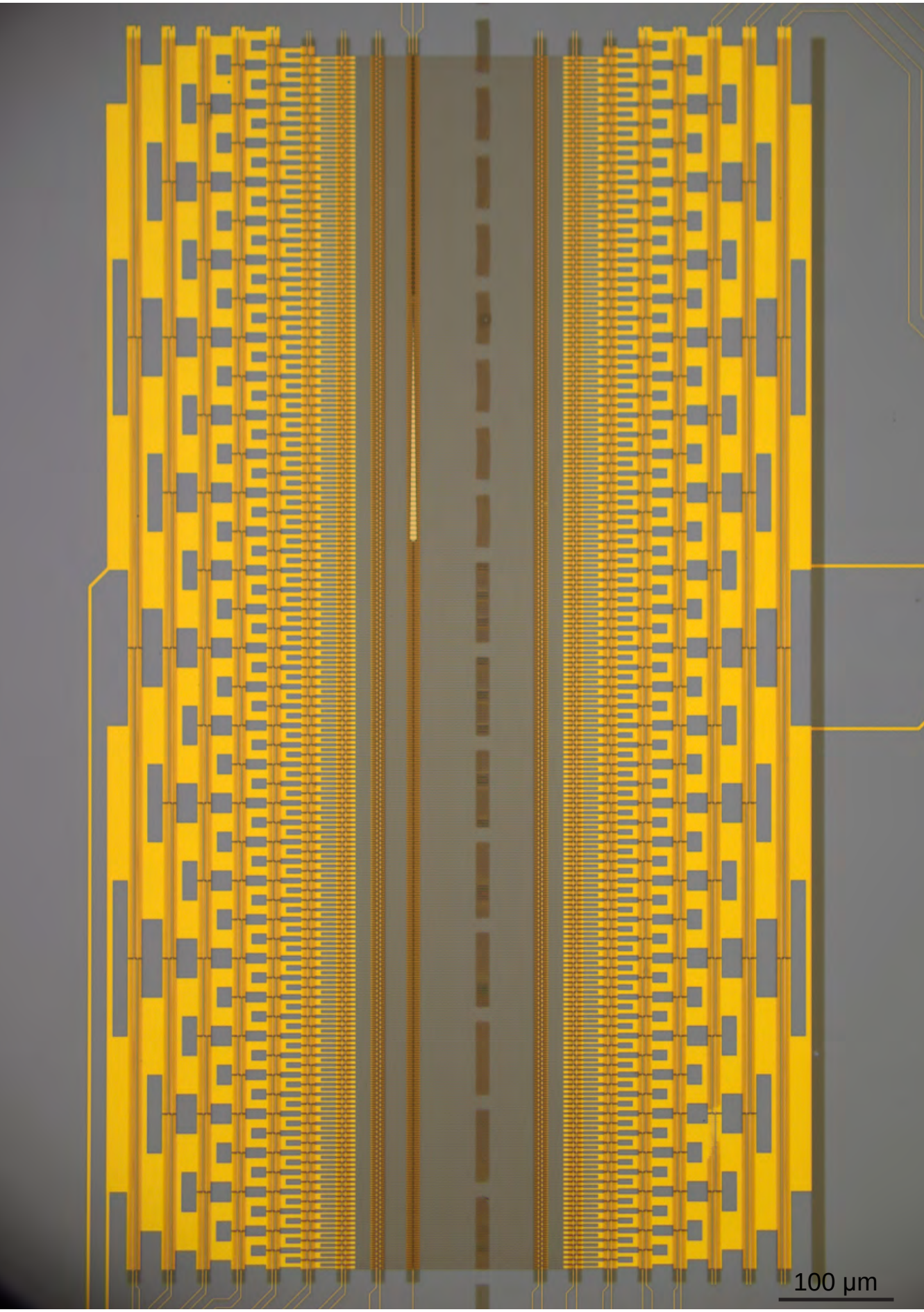


Figure 4.4: **a** SEM micrograph showing a few multiplexer NWFET units in two levels. Ti/Au contacts in gold, Ti/Au gates in blue where NWs are affected, gray where the gate is screened by the underlying contact. **b** Schematic representation of the circuit in a. Each level splits the current path into two and a specific path can be chosen by the appropriate combination of gate voltages.

Figure 4.4 shows an example of a unitcell of such a circuit where multiple NWFET devices are chained into a levelled multiplexer structure [7, 107]. The fabrication of multiplexer leads and gates does not

differ from the fabrication process of the single SAG NW devices in this study which means that the multiplexer circuit can be fabricated in tandem with the devices it will address and does not add additional fabrication steps. Each level in the structure corresponds to devices fabricated on different rows of the SAG NW array shown on page 27. The relative positions of the NWFET ohmic contacts alternate such that for each NWFET only one of the two gates (which both extend straight across the entire level) tunes the electron density in the NWs while the other is screened by the metallic contact (Fig. 4.2a, b). Input signals are thus directed through the multiplexer as illustrated in the schematic in Fig. 4.4. Each level requires two gates and doubles the number of accessible multiplexer outputs and each output can be uniquely addressed by biasing the corresponding combination of gates. The number of available outputs is then 2^L where L is the number of levels in the circuit. To compare, for a motherboard with 48 transmission lines it would be possible to realize 16 individual FET devices. However, implementing a multiplexer circuit and a shared gate it is theoretically possible to realize 2^{23} ($> 8 \cdot 10^6$) devices with the same amount of transmission lines.

A multiplexer circuit allowing for measurement of 500 individual devices is shown in the optical microscope micrograph on page 46. Note that the multiplexer circuit is coupled to a complementry demultiplexer circuit which is a functionally identical mirrored multiplexer circuit. The devices under test (DUT) are located between the two circuits. Each multiplexer output acts as a source lead for an individual device while each demultiplexer output acts as a drain lead. The inclusion of the demultiplexer circuit allows to validate that the multiplexer circuit is addressing unique outputs without parallel channels which might be the case if some of the NWFETs comprising the circuit are non-functional and fail to pinch-off.


100 µm

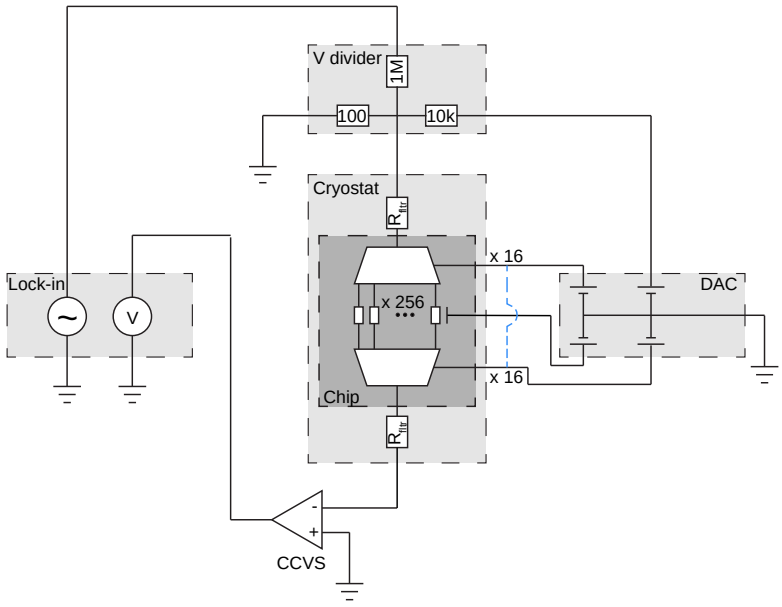


Figure 4.5: Schematic of the measurement circuit used to measure the NW devices. Here an example is given for a circuit with 256 active NW devices. 16 gates must be operated for the multiplexer and 16 for the demultiplexer. Coupling the multiplexer and demultiplexer control gates by the blue dashed line allows to half the necessary DAC outputs. The 256 NW devices can share common gates.

A simplified schematic of the measurement circuit used to characterize the InAs SAG NW devices is shown in Fig. 4.5. A small AC signal is supplied by a Zurich Instruments MFLI lock-in amplifier and offset by a DC signal supplied by a QDev 48-output digital to analog converter (DAC). The voltage signals are scaled and combined by a $10^{-4}/10^{-2}$ AC/DC voltage divider/adder and applied to the multiplexer input. If it is not needed to operate the multiplexer and demultiplexer outputs independently, each multiplexer and demultiplexer control channel can be coupled as indicated by the blue dashed line

in Fig. 4.5 to halve the number of DAC outputs needed for control of the circuit. It is technically also possible to couple the multiplexer and demultiplexer control lines on-chip to halve the number of transmission lines from room temperature to cryogenic temperatures. This was not done here to enable control of individual gates for diagnostics purposes discussed below. The demultiplexer output is amplified by a current controlled voltage source (CCVS) and measured via the lock-in amplifier. The NW devices are located between the multiplexer and demultiplexer and shared crossbar gates are used to control the large number of devices with just a few gate lines.

Circuit Verification

With many electronic elements working in tandem during the use of the circuit it is necessary to verify the circuit operation. To conclusively test that the multiplexer circuit is functioning as intended, it is connected back-to-back to a demultiplexer circuit. An optical microscope micrograph of a full 16-output multiplexer-demultiplexer circuit is shown in Fig. 4.6a. The inclusion of the demultiplexer circuit allows to validate that the multiplexer circuit is addressing unique outputs without parallel channels which might be the case if some of the NWFETs comprising the circuit are non-functional and fail to pinch-off.

A powerful way of gaining insight to the performance of the circuit is to probe all combinations of multiplexer outputs versus all demultiplexer outputs while measuring the conductance. The result is a "conductance matrix" such as the one shown in Fig. 4.6b for the multiplexer-demultiplexer pair in Fig. 4.6a. The main diagonal feature (black arrow) shows that conductance is high when the multiplexer and demultiplexer address the same output. This is expected in the case of normal operation of the circuit when the DUT are conducting and shows that no FETs fail to open. However, there are also

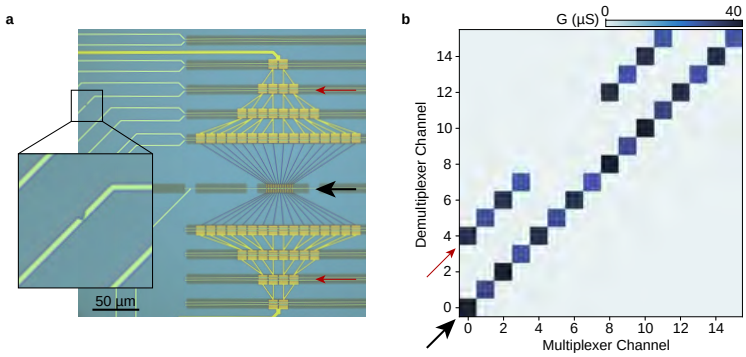


Figure 4.6: **a** A 4 level multiplexer connected to a 4 level demultiplexer circuit providing 16 outputs. Inset shows zoomned-in view of a broken gate control line. **b** The respective conductance matrix of all combinations of multiplexer and demultiplexer outputs. The black and red arrows indicate conductance features originating from levels shown by the corresponding arrows in a.

additional off-diagonal conductance features present (red arrow). To explain these additional features it is considered how the matrix features are formed and how various failures would manifest in a smaller circuit.

As an illustration, consider the 2-output multiplexer-demultiplexer circuit in Fig. 4.7 showing all possible gate voltage combinations where gates on the same level have opposite polarity in the case of normal operation and common faults. Red colored gates indicate positive voltage (transistor ON-state) and blue indicates negative voltage (transistor OFF-state), the two possible current paths are indicated by purple and orange and the corresponding color in the matrix elements indicates which current path contributes to the conductance. If everything is working perfectly as shown in Fig. 4.7a, only the diagonal elements have non-zero conductance and only one current path contributes to each non-zero matrix element. A gate that fails to pinch-off the NW

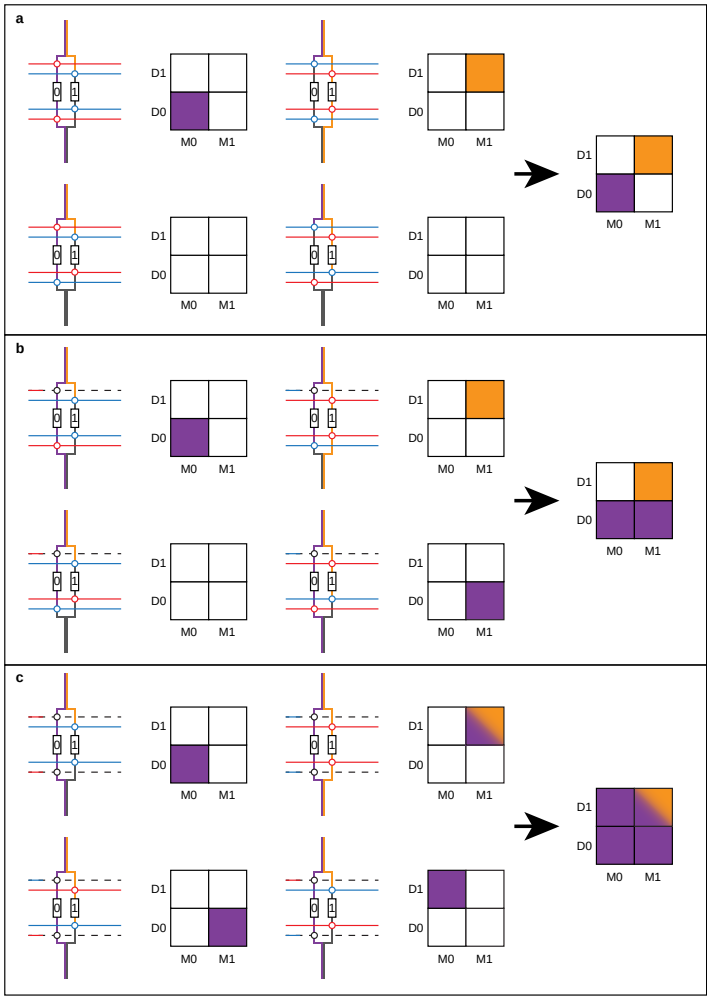


Figure 4.7: **a** Breakdown of matrix pattern with fully functioning gates. **b** Breakdown of matrix pattern for a non-functioning gate (can't pinch off). Devices can still be uniquely addressed. **c** Breakdown of matrix pattern for symmetrically non-functioning gates. Some devices can no longer be uniquely addressed.

shows up as an off-diagonal non-zero conductance element as shown

in Fig. 4.7b, however, the failing gate is compensated by the equivalent gate in the symmetric demultiplexer circuit and it is still possible to uniquely address individual devices as the conductance of each on-diagonal element still only has contributions from only a single current path. The circuit only fails to address a unique device when gates fail symmetrically on both sides of the multiplexer-demultiplexer circuit as shown in Fig. 4.7c, this can be identified in the matrix pattern as symmetric off-diagonal elements. In this case some devices can no longer be uniquely addressed as there will always be another device connected in parallel that cannot be excluded from the measurement.

Scaling up, a larger multiplexer-demultiplexer circuit consisting of 8 outputs is considered in Fig. 4.8. Failing transistors (OFF-state not possible) in various locations are marked with colored crosses in Fig. 4.8a, corresponding features in the matrix pattern are shown in Fig. 4.8b. From the matrix pattern it is possible to identify on which level of the multiplexer-demultiplexer circuit the failing gate is located - the further away the signature is from the main diagonal, the earlier in the branching the gate failure has occurred. However, it cannot be established from the matrix pattern itself which specific gate on which side of the multiplexer-demultiplexer circuit is non-functioning as some gate failures produce identical matrix patterns as illustrated by the purple and orange features in Fig. 4.8. In the case where one of the gates on a level is non functional, meaning half of the transistors in that level cannot be pinched off, the resulting patterns will be periodic with a periodicity of 2^L, where $L \in [1, L_{\max}]$ is the level in which the failure occurs counting from the side closest to the device layer. Additionally, errors can compound creating additional patterns in the matrix. Patterns related to individual failures only appear 2^L outputs away from the main diagonal. However, multiple failures can compound as illustrated in Fig. 4.8c, d. Individually the failures would produce the same patterns as the purple and blue features in Fig. 4.8b

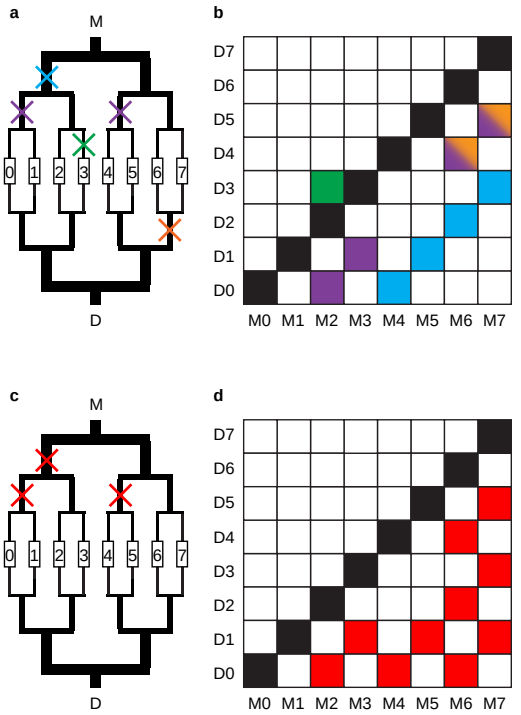


Figure 4.8: **a** Schematic multiplexer explaining the matrix pattern. Colored crosses indicate example locations of non-functioning FETs and correspond to the pixels in b. **b** Example matrix pattern, black pixels indicate the normal operation with matching multiplexer-demultiplexer outputs, colored pixels show patterns caused by non-functioning FETs. The failure patterns are not completely unique, as shown by the orange/purple pixels. **c, d** Example of compounding errors. The off-diagonal feature starting at M6 is a result of compounding the errors starting at M2 and M4.

but together they compound to form an additional matrix feature at $2^{L1} + 2^{L2}$ as shown in Fig. 4.8d.

An important conclusion from this analysis is the robustness of

the multiplexer-demultiplexer circuit as gate failures in one half of the circuit can be compensated by the other half of the circuit. In the case of using a single multiplexer circuit as in traditional circuits where all devices share a common drain any failing gates will immediately reduce the number of uniquely addressable devices without an easy way to diagnose the fault. In a multiplexer-demultiplexer circuit a symmetric gate failure is the only way the circuit can fail to address outputs uniquely and such a failure is directly visible in the conductance matrix greatly increasing the reliability of the circuit and offering protection against fabrication faults.

Returning to the 16 output multiplexer in Fig. 4.6 the off-diagonal conductance features in the matrix can now be correlated to a failure to pinch off one of the gates on layer three (counting from the output side) on either the multiplexer or the demultiplexer circuit, indicated by the red arrows in Fig. 4.6a, similar to the theoretical failure in Fig. 4.8 indicated in blue. In fact, the source of the failure in this case can likely be attributed to the damaged gate line seen in the zoom-in in Fig. 4.6a which causes half of the transistors in that level to fail to pinch-off consistent with the periodic features in the conductance matrix.

500 Output Multiplexer-Demultiplexer Circuit

Scaling up further, Fig. 4.9a (larger image on page 46) shows an 8-level multiplexer connected back-to-back to a corresponding 8-level demultiplexer circuit. The circuit allows for selective biasing of 500 different DUT situated in the gap between the multiplexer-demultiplexer units (black arrows in Fig. 4.9a). In this case the DUT consists of individual SAG NW devices with different geometries and the SEM micrograph in Fig. 4.9b shows DUT devices # 70 - # 77 corresponding to the blue rectangle in Fig. 4.9a. In this range odd-numbered devices #71,73,75,... are identical SAG NWFETs with a 150 nm con-

tact separation and a common top gate. Even-numbered channels, however, consist of simple metal shorts allowing confirmation of successful operation of the multiplexer-demultiplexer circuit irrespective of the performance of the DUT. Further, the shorted lines enable measurements of the reference resistance of the multiplexer and demultiplexer path for each DUT. As the current path between a DUT and the short adjacent to it differ only by one transistor on the multiplexer side and one transistor on the demultiplexer side, it provides a good estimate of the series resistance from the multiplexer circuit, filters in the cryostat, and transmission lines.

Figure 4.9c shows the conductance of the circuit for each of the 65536 unique combinations of the first 256 multiplexer and 256 demultiplexer channels. The measurement was performed at a temperature of $\sim$ 20 mK with positive voltage on the gates of the DUT ensuring the devices in the DUT layer are passing current. High conductance is observed along the main diagonal (black arrow) confirming the expected finite current when both multiplexer and de-multiplexer address the same channel. This also confirms that all DUT are conducting and that none of the 1996 SAG NWFETs of the multiplexer/demultiplexer pair fail to open which would lead to periodic regions of no conductance along the diagonal.

Again, in the ideal case these would be the only non-zero values of the conductance matrix in Fig. 4.9. However, off-diagonal transport is also clearly observed (blue/teal arrows) which correspond to NWFETs failing to pinch-off. In Fig. 4.9c, the extent of the off-diagonal features show that it is entire levels of the multiplexer that fail rather than individual NWFETs. Since it was identified in Section 4.2 that the InAs SAG NWFETs have a negative threshold voltage (Fig. 4.2a) such failure naturally corresponds to e.g. disconnected gate control lines. The repeating features with a period of 128, 64, and 4 channels (teal, blue, and red arrows respectively) in Fig. 4.9c-f indicate the failing of one

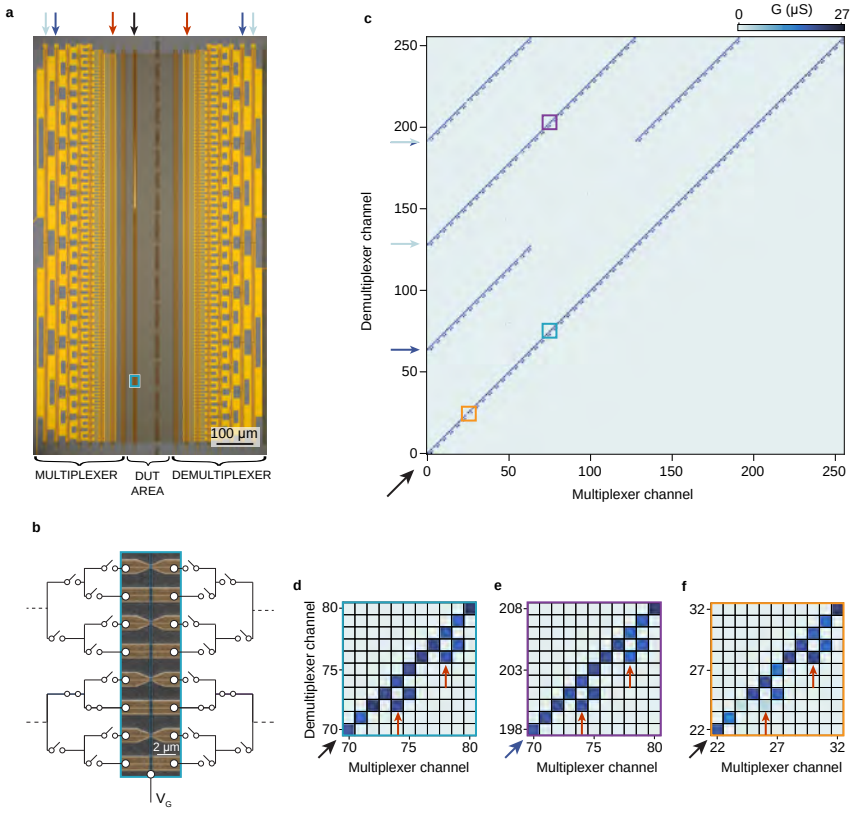


Figure 4.9: **a** Optical microscope micrograph of InAs NWFET-based multiplexer-demultiplexer circuit. DUT indicated by the black arrow. Colored arrows correspond to the features in c-f. **b** SEM micrograph of the area in the blue rectangle in a showing 8 DUT and schematic representation of partial multiplexer-demultiplexer circuit, Ti/Au contacts in gold, Ti/Au topgate in blue. **c** Conductance matrix of the first 256 channels. The diagonal feature shows that that all of the devices under test are conducting, off-diagonal features indicate gate failures with possible locations indicated by the corresponding arrows in a. **d-f** Segments of the conductance matrix corresponding to the respective colorful squares in b.

of the gates in the multiplexer levels marked with the corresponding arrows in Fig. 4.9a. The feature appearing at demultiplexer chanel 192 (64 + 128) is a compound feature from the errors marked with blue and teal arrows. A rare example of a single NWFET in the DUT layer failing to turn on is shown by the zoom in Fig. 4.9f.

Importantly, as discussed above, combinations of failures which would make unique DUT addressing impossible would appear as finite transport occurring at symmetric positions relative to the diagonal; such features are not observed in Fig. 4.9c-f meaning that any DUT can be uniquely addressed regardless of the failures present. Across 500 DUT, Fig. 4.9f represents the only observed failure which confirms again the high yield of SAG NW devices.

The two gates in each multiplexer level can also be operated independently allowing for both gates to be set to accumulation or depletion mode if desired. It is useful to be able to set both gates to depletion mode when performing initial benchmarking of the multiplexer circuit. While the matrix patterns described above are useful for visualising the successful operation and any possible faults of the multiplexer, it is a very time consuming measurement to perform. A faster way to verify proper operation of the circuit is to set all gates to accumulation mode and then attempt to pinch-off the circuit by sequentially setting both gates on each level to depletion. Failure to pinch off the circuit will indicate a faulty gate on that level, the specific failing gate can then be identified by cross-referencing the mirror-symmetric gates on the other side of the multiplexer-demultiplexer circuit. In some cases it can also be beneficial to set pairs of gates into accumulation regime, this allows e.g. connecting multiple devices in a parallel circuit. Another potential application could be to use a multiplexer circuit to address a large number of gates, in this case it could be possible to select different configurations of gate voltages at the multiplexer outputs e.g. for charge shuttling experiments by

having multiple pairs of multiplexer gates set to accumulation mode.

The successful realization of multiplexer-demultiplexer circuits shows the high yield of InAs SAG NWFET devices and allows addressing of a very large number of devices under cryogenic temperatures. This breaks the traditional bottleneck of sub-kelvin temperature electrical measurements - the number of electrical connections between the room temperature instruments and the devices at the deep cryogenic level. The number of which is limited by the available cooling power and the dimensions of the cryostat. Implementing the multiplexer circuit exponentially increases the number of available connections meaning the number of devices that can be characterized is effectively limited only by the time of measurements. Furthermore, switching between devices in the circuit does not require changing of physical cables and can be integrated into automatic measurement loops allowing large numbers of repetitive measurements to be executed without human input over a long period of time.

5

5 SAG Nanowire Reproducibility

5.1 SAG NW Structural Variability

The results presented in this chapter focus on the reproducibility and scalability aspects of devices based on InAs SAG NWs. Scalability is one of the main reasons for using SAG NWs as discussed in Section 2. Key aspects of scalability are the ability to grow the NWs in defined positions and that the NW properties are reproducible within the thresholds of the desired application. There are various sources of irreproducibility, such as structural variance either intrinsic or due to fabrication/growth processes and electrical variance due to impurities.

It is important to establish the morphological and structural variability of these NWs to accurately interpret the electron transport data. The large arrays of nominally identical SAG NWs described previously in Section 3.1 are investigated via AFM, to establish the variability of the NW physical dimensions.

Variation on Single NW Scale

Despite the parallel fabrication and growth of the SAG NWs, several effects lead to structural variations at different length-scales both within individual NWs and between NWs across the arrays. On the microscopic level the InAs SAG NW crystal structure exhibits stacking faults and dislocations due to the lattice mismatch with the underlying GaAs. These effects result in variations in the NWs on the nanometer scale and will effectively be averaged when considering electron transport in micrometer-scale devices. Thus, these presumably contribute to overall reduction in e.g. charge carrier mobility [81] and device variability. On the larger scale the pre-growth processing of the substrates using EBL and etching also leads to structural variation. Typical values of oxide mask etch roughness are on the order of $1 - 2\,\mathrm{nm}$ and such roughness will translate into variations of the NW profile which can also extend along the NW with a length scale

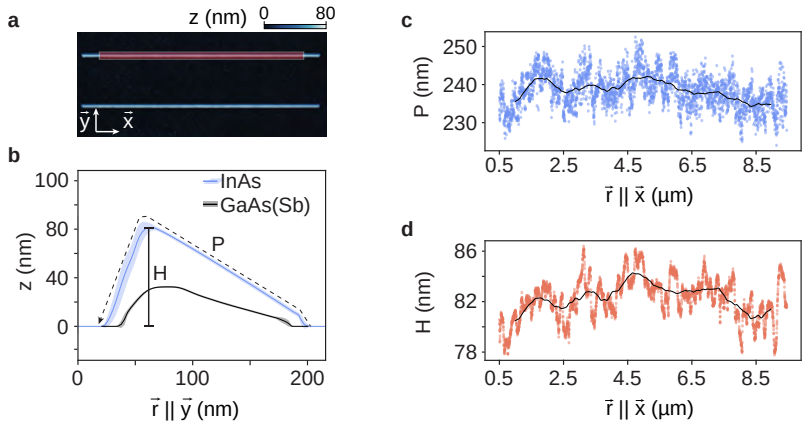


Figure 5.1: **a** AFM micrograph of 2 SAG NWs, the red box indicates the area of the NWs scanned for the data in b-d. The vectors $\vec{x}$ and $\vec{y}$ are 1 μm long. **b** The mean profile of InAs NW and GaAs(Sb) buffer from AFM scans averaged over 9 μm and 2 μm long NW segments respectively. The colored bands show the standard deviation. **c,(d)** P (H) as defined in panel b along the length of the NW disregarding 0.5 μm tapered segments on the ends of the NW. The black line indicates the average value over 1 μm. (AFM data credit: Gunjan Nagda)

set by the diffusion length of In adatoms.

Figure 5.1a shows an AFM micrograph of two example SAG NWs from a large array. The ends of the NWs are tapered due to the source growth mode of the GaAs at the ends of the NWs [108] thus only the 9 μm segment in the red box is analyzed in the following. Figure 5.1b shows the average profile across the NW segments averaged over a length of 9 μm. The NW height H and facet length P serve as proxy variables for the physical dimensions of the conduction channel in the semiconductor NWs. For InAs NWs, transport at low temperature is usually dominated by a surface accumulation layer and thus in the simplest case the conductance is proportional to P [56]. Figure 5.1c and d shows examples of P and H along the length of a NW and the

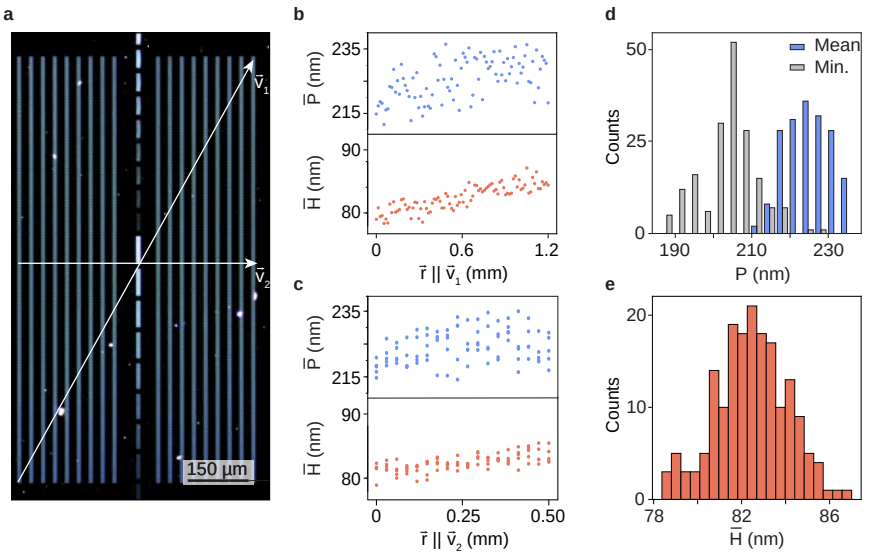


Figure 5.2: **a** Darkfield optical microscope micrograph of an array of SAG NWs which are used to fabricate devices. Vectors $\vec{v}_1$ and $\vec{v}_2$ indicate the directions along which the AFM measurements in b-e were taken. **b (c)** $\overline{P}$ and $\overline{H}$ over 1 µm NW segments taken approximately along $\vec{v}_1$ ($\vec{v}_2$). **d** Histograms of mean and minimum P across 180 NWs. **e** Histogram of mean H across 180 NWs. (AFM data credit: Gunjan Nagda)

solid black lines show the value at each point averaged over a $1\,\mu$m window to better visualise any trend on the NW-scale. Variation along a single nanowire is $\sim 5\%$ with no obvious trends thus the mean value is used to describe each NW.

NW Variation Across the Substrate

Spatial variations in the substrate temperature and flux-distributions across the substrate during growth can lead to systematic variations across the growth wafer on the millimeter scale. To

investigate the variations in the NW morphology topographic AFM micrographs of 180 individual NWs approximately following the vectors $\vec{v_1}$ and $\vec{v_2}$ (90 NWs in each direction) in Fig. 5.2a spanning the entire spatial dimensions of the NW array were analyzed.

Considering the mean values of H and P of each NW segment $\overline{H}$ and $\overline{P}$ as a function of position along the two vectors $\vec{v_1}$ and $\vec{v_2}$ (Fig. 5.2b and c respectively). It can be observed that there is a notable slope to the data indicating systematic variation across the spatial extent of the arrays. As the two slopes along $\vec{v_1}$ and $\vec{v_2}$ are approximately the same, it can be concluded that the long-range variation is generally constrained to the $\vec{v_2}$ direction. The comparative electrical measurements in the following Sections are based on a row of devices extending perpendicular to the $\vec{v_2}$ direction thus it is expected that the long-range variation observed here has negligible influence on the comparison of electron transport parameters between devices.

Figure 5.2d and e show the distributions of $\overline{H}$ and $\overline{P}$ as well as the minimum facet length $P_{\min}$ across the NWs. The minimum facet length is also considered here as segments of reduced P might act as bottlenecks limiting the conductance through the NW. From the distributions it can be observed that although all growth and fabrication parameters were kept constant across the SAG NW array, there are still normalized standard deviations $\sigma_{\mathrm{H}}/\overline{H} = 2\%$ and $\sigma_{\mathrm{P}}/\overline{P} = 2.5\%$ to the parameters. This nanoscale structural variability of the nominally identical NWs may influence the reproducibility of the electrical characteristics of quantum devices based on the NWs and will be explored in the following Sections.

5.2 Variance of FET Parameters

To explore the variance of electrical properties between nominally identical SAG devices the multiplexer-demultiplexer circuit is used to investigate the statistical distribution and reproducibility of electrical parameters of SAG NWFETs by characterizing 256 lithographically identical NWFET devices from the multiplexer level closest to the DUT layer. Each NWFET incorporates a single SAG NW with a contact separation of 1 μm.

Conductance as a function of V_{G} was measured for each device at a temperature of 20 mK with the gate being swept from positive to negative voltage and back. The measurement was repeated with the devices warmed to 100 K, the devices were then brought to RT and cooled back down to 20 mK for a final round of measurement resulting in 1536 conductance traces to be analyzed. Performing such a measurement of high statistical significance without multiplexing would require considerable time in terms of multiple device fabrications, cooldowns and manual changing of cabling.

Figure 5.3a shows the conductance $G(V_{\mathrm{G}})$ measured at a temperature of 20 mK and at 100 K after subtraction of series resistance R_{s} for the first 128 devices. The full dataset including the raw data of all 256 devices and both rounds of measurements at 20 mK is included in Appendix B1. The devices reproduce the n-type FET transfer characteristics similar to that observed in Fig. 4.2c in Section 4.2. Fitting each curve to the standard expression $G^{-1} = R_{\mathrm{s}} + L^2/(\mu_{\mathrm{FE}} C(V - V_{\mathrm{TH}})$ [104] we extract the field effect mobility μ_{FE}, threshold voltage V_{TH}, and series resistance R_{s} for each trace. Here L is the known length of the semiconductor segment, $C = 5.4$ fF the gate capacitance estimated from an ANSYS electrostatic model as described in Section 3. The

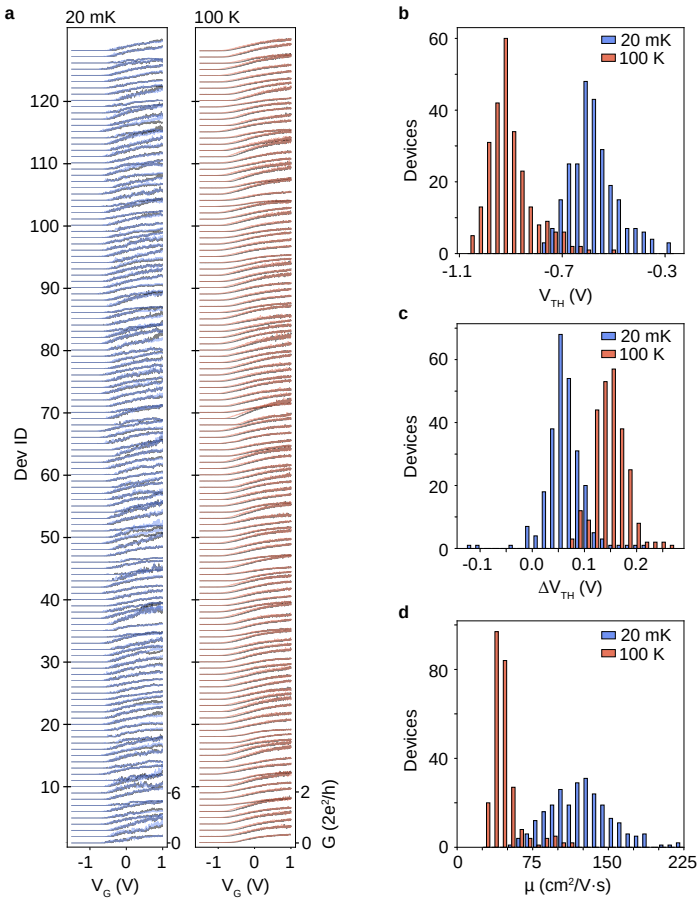


Figure 5.3: **a** G as a function of (V_{G}) of 128 NWFET devices made from single SAG NWs offset in conductance by $0.1 \times 2e^2/h$ (20 mK traces) and $0.25 \times 2e^2/h$ (100 K traces) for clarity. Gate voltage swept from positive to negative (black) and from negative to positive (blue/red). Series resistance is estimated from the fit and subtracted. **b-d** Histograms of V_{TH} (voltage swept from negative to positive), ΔV_{TH}, and μ_{FE} respectively for 256 devices measured at 20 mK (blue) and 100 K (red).

series resistance R_s accounts for the circuit resistance and contact resistance to the SAG NW.

Since the expression used is valid only when the Drude model [104, 109] of conduction is applicable, i.e. above the percolation regime [110], the fit range for each measurement is chosen by first smoothing the pinch-off curve using Savitzky-Golay filtering and then identifying the gate voltage at which the conductance rises to 5% of its maximum value. The non-filtered data in the range from the identified gate voltage to the largest applied positive gate voltage is then used for fitting. The fit yields the values for V_{TH}, μ_{FE}, and R_s and all other parameters are fixed. The values are used for relative comparisons between devices and any systematic biases of the model are assumed to be the same across devices.

In addition to the continuous modulation of the carrier density of the NW, the field from the gate can activate rearrangements or cause filling of charge-traps in the vicinity of the devices [111–113]. This leads to hysteresis in electrical devices [114] and introduces an important complication for the tuning of multi-component quantum circuits as the device configuration depends not only on the position in gate-space but also on the history and trajectory taken to get there. As a measure of gate hysteresis in the SAG NWFETs the difference of threshold voltages $\Delta V_{TH} = V_{TH}^{dwn} - V_{TH}^{up}$ measured for the V_G sweep directions from negative to positive (up) or vice-versa (dwn) is used.

In the following analysis emphasis will be placed on investigating the statistics of these three fundamentally important electron transport parameters - V_{TH}, ΔV_{TH}, and μ_{FE}. When designing electronic circuits that require multiple elements working in tandem with gates shared across individual elements it is required that threshold voltages are reasonably similar and reliably reproducible within known tolerances across devices and that hysteresis is minimal compared to the operating voltage range of the gates. Similarly, electron mobility

is a key parameter for electronic devices which influences device metrics such as the switching frequency of FETs and serves as a proxy indicator of disorder via the electron scattering rate [115].

As the electron transport characteristics of NWFETs depend on the structural qualities of the underlying NWs, the distributions of electron transport parameters reflect the variance between individual NWs shown in Section 5.1. Furthermore, the electron transport parameters are strongly influenced by scattering and screening resulting from charged impurities the magnitude of which depends on the quality of oxides and surface adsorbents such as resist residues [116]. These depend largely on the materials used, the processing during fabrication, and the experimental conditions and while these impurities can be minimized they are difficult to eliminate. These charged impurities are static at millikelvin temperatures, but can be thermally activated at higher temperatures and randomized by thermal cycling [23, 24, 117, 118]. Thus, correlating device electron transport parameters at sub-kelvin temperatures before and after thermal cycling decouples the contributions from structural variations and random impurity charges as structural variations will be unchanged by thermal cycling while random impurity charges are randomized by thermal cycling [23, 24, 117–119]. This provides insight into the relative effects of the structural variations and impurity charges. Figure 5.3 summarizes the distributions of V_{TH} (Fig. 5.3b), ΔV_{TH} (Fig. 5.3c), and μ_{FE} (Fig. 5.3d). Furthermore, Fig. 5.4 shows correlations between the parameters at $T = 20\,\mathrm{mK}$ and $T = 100\,\mathrm{K}$ and between two cooldowns to 20 mK. Additional correlations between transport parameters are included in Appendix B3.

Threshold Voltage

First considering V_{TH}, Fig. 5.3b shows the distributions of V_{TH} for 256 NWFET devices at 20 mK and 100 K. At a temperature of

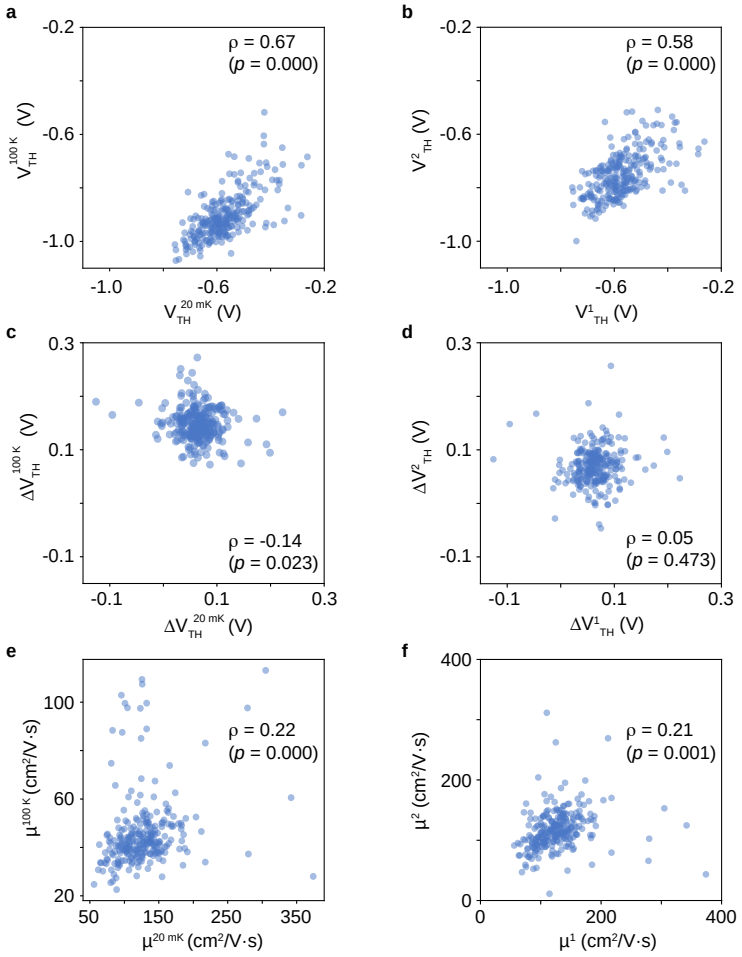


Figure 5.4: **a, b** Correlations between V_{TH} at 20 mk and 100 K and between two cooldowns to 20 mK respectively. **c, d** Correlations between ΔV_{TH} at 20 mk and 100 K and between two cooldowns to 20 mK respectively. **e, f** Correlations between μ_{FE} at 20 mk and 100 K and between two cooldowns to 20 mK respectively.

20 mK V_{TH} across 256 NWFET devices is distributed around a mean value of of -572 mV with a standard deviation of 91 mV. At higher

temperatures the threshold voltage of the devices shifts towards more negative values. At a temperature of 100 K the mean of V_{TH} shifts to −905 mV while the standard deviation of 87 mV remains similar to the 20 mK case. Such shifts with increasing temperature are predominantly attributed to the decrease in charge trap lifetime and, to a lesser extent, the shift of the Fermi level deeper into the conduction band [112].

There is also a correlation between the V_{TH} values across devices at 20 mK and at 100 K with Pearson's correlation coefficient [120] $\rho = 0.67\,(p = 0.000)$ (Fig. 5.4a) and also between the two cooldowns to 20 mK $\rho = 0.58\,(p = 0.000)$ (Fig. 5.4b), showing that devices which exhibited a higher V_{TH} in the first cooldown generally retained a higher V_{TH} also after warming up and thermal cycling. The correlation indicates that the structural variation of the NWs has a significant influence on the variability of V_{TH} while the dispersion shows that there is also a non-negligible influence from the impurity charges.

Hysteresis

Similarly, Fig. 5.3c shows the distributions of ΔV_{TH} for the same devices when V_{G} is swept in the range −1.5 V to +1 V. ΔV_{TH} is distributed around a mean of 64 mV with a standard deviation of 37 mV at a temperature of 20 mK. ΔV_{TH} increases to a mean value of 148 mV with a standard deviation of 31 mV when the temperature is increased to 100 K.

Correlating the ΔV_{TH} values across devices at 20 mK and at 100 K it can be seen that there is no correlation across devices $\rho = -0.14\,(p = 0.023)$ (Fig. 5.4d) and the standard deviations are similar. There is also no correlation between the ΔV_{TH} values before and after thermal cycling $\rho = 0.05\,(p = 0.473)$ (Fig. 5.4c). The hysteresis in NWFETs is caused by gate activated rearrangement of charged impurities near the NW channel, this process is more efficient

at higher temperature [113, 114] explaining the observed increase in the magnitude of the hysteresis at increased temperatures. The lack of correlation between ΔV_{TH} is consistent with the interpretation that ΔV_{TH} is mainly governed by random impurity charges the configuration of which is randomized between cooldowns and not specific NW structural properties. The magnitude of ΔV_{TH} also remains similar before and after thermal cycling indicating that it does not improve or degrade with repeated thermal cycling.

Electron Mobility

Moving on to electron mobility, Fig. 5.3d shows the distributions of μ_{FE}, at a temperature of 20 mK centered around a mean value of $127\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ with a standard deviation of $41\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. The observed mobility values for these NWs are significantly lower than observed in other SAG InAs NW studies where values $\sim 10^3$ were found [72, 81]. The relatively low μ_{FE} values [72, 81] for this new type of SAG NWs grown on GaAs [3 1 1] could likely be improved by optimizing the SAG NW structure for high mobility by taking similar steps as shown by previous work such as a buffer layer confining the misfit dislocations and interface strain away from the conduction channel [81].

Increasing the temperature to 100 K the mobility is further reduced to a mean value of $46\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ with a standard deviation of $15\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. A reduction in charge carrier mobility in InAs NWs with increasing temperature has been associated with an increase in the number of thermally activated charged surface scatterers [121] as well as an increase in the electron-phonon scattering rate as phonon density increases with temperature [122]. Similar to V_{TH}, it can be seen in Fig. 5.4e, f that there is a weak correlation in device μ_{FE} at 20 mK and 100 K $\rho = 0.22\,(p = 0.000)$ and between cooldowns $\rho = 0.21\,(p = 0.001)$) pointing towards dependence of μ_{FE} on NW structure. This is in agreement with previous research showing the

effect of interface strain and defects caused by the lattice mismatch between the NW and the buffer layer on the charge carrier mobility [81, 123]. However, the strong dispersion in Fig. 5.4e, f indicates that the random impurity charges also have a sizeable influence on μ_{FE}.

As a statistically significant number of devices have been investigated, it can be seen that the combined effect of unintentional structural variations across NWs and the random configuration of impurity charges in the immediate surroundings of the NWs can cause a change in the charge carrier mobility of a factor of two. This demonstrates the importance of reproducing results when performing material characterization studies and the characterization method developed here will be a useful tool for future optimization of SAG NW parameters. Furthermore, even without additional optimization the variability of V_{TH} and magnitude ΔV_{TH} of the current structures are sufficiently low to realize large-scale functional circuits such as the the multiplexer-demultiplexer circuit presented here

5.3 Basics of QDs

Quantum dots have a wide range of potential applications in sensor technology [124–126], lasing [127, 128], and continue to be one of the most promising qubit platforms [129–131]. QD qubits have been demonstrated in GaAs based 2DEGs [131, 132], graphene [133, 134], III-V VLS-grown NWs [132, 135], and silicon [43, 44]. This Section gives a brief introduction to the basics of QDs and serves as background for the interpretation of the measurements in Section 5.4. The following text in this Section summarises the relevant insights of the basics of QD as context for the next Section. For a more exhaustive description the interested reader is directed to Chapter 18 in [26].

Quantum dots are "0-dimensional" objects that are weakly coupled to their environment and and of such small dimensions that the addition of single electrons is governed by classical Coulomb repulsion of electrons already on the dot and/or the nature of the zero-dimensional quantum mechanical energy levels. The electron confinement needed to realize QDs can be defined by the physical dimensions of the system or by electrostatic gating. Semiconductor NWs are an attractive platform for realising QDs as the electrons are confined to a 1D channel by the crystal and gates can be used to define two tunnel barriers forming the QD. An example of such a device is illustrated in Fig. 5.5c with two topgates (blue) controlling the tunnel coupling between the source/drain (gold) and the QD and a plunger topgate (red) is used to tune the electron density on the QD.

When the tunnel coupling Γ between the QD and the source/drain leads is low (tunneling resistance $>> h/2e^2$) the charge on the QD is quantized in units of e, i.e. the number of electrons on the QD is an integer number N. An addition energy E_{add} must be overcome to add

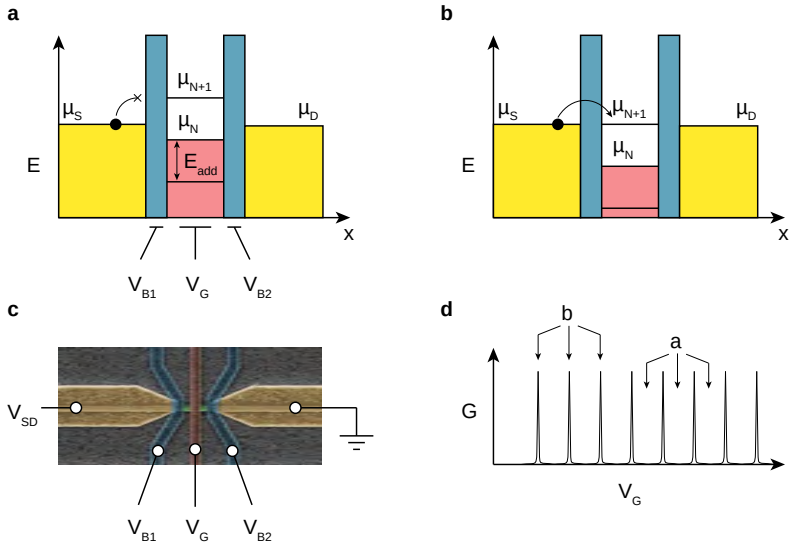


Figure 5.5: **a** Simplified energy diagram of QD in Coulomb blockade. **b** Simplified energy diagram of zero bias transport through a QD. **c** SEM micrograph of NW QD device. Source and drain contacts in gold, barrier gates in blue, plunger gate in red and InAs NW in green. **d** Illustration of $G(V_\mathrm{G})$ for a QD. Conductance resonances correspond to the energy diagram in b and regions of zero conductance correspond to energy diagram in a.

an electron $N+1$ to a QD with N electrons. The addition energy of the QD is simply the Coulomb energy $E_\mathrm{C} = e^2/C$ plus the confinement energy (single-particle level spacing) which can be estimated from the particle-in-a-box approximation to be $\Delta E = h^2/(8m^*L^2)$, where C is the capacitance, m^* is the electron effective mass, and L is the distance between the barriers. To resolve E_add the thermal energy of the system $k_\mathrm{B}T$ must be much smaller than E_add.

Using the plunger gate voltage V_G the chemical potential in the QD can be tuned such that the chemical potential for adding an elec-

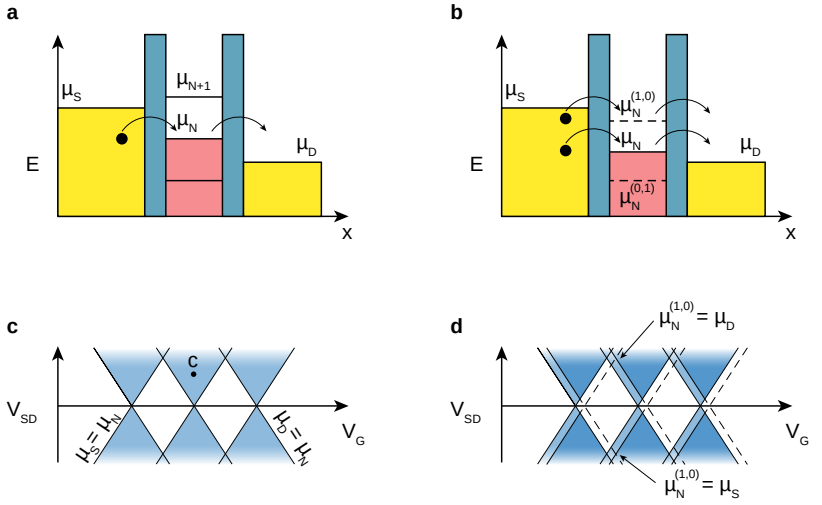


Figure 5.6: **a** Simplified energy diagram of electron transport through QD with bias applied to source and drain. **b** Simplified energy diagram of electron transport through QD via an excited state. **c** Illustration of $G(V_\mathrm{G}, V_\mathrm{SD})$, conductance occurs in the blue shaded regions. The diagonal lines show cases where $\mu_\mathrm{S,D} = \mu_N$. Conductance at the dot corresponds to the energy diagram in a. **d** Illustration of $G(V_\mathrm{G}, V_\mathrm{SD})$ including transport through an excited state

tron μ_{N+1} is equal to the chemical potentials in the source (μ_S) and drain (μ_D). In this situation where $\mu_\mathrm{S} \approx \mu_{N+1} \approx \mu_\mathrm{D}$ electrons can tunnel onto and off from the QD sequentially one by one (Fig. 5.5b). However, if the chemical potentials are tuned to a situation where $\mu_N < \mu_\mathrm{S,D}$ and $\mu_{N+1} > \mu_\mathrm{S,D}$, electron transport through the QD is blocked (Fig. 5.5a), this is called Coulomb blockade. Current through the dot is observed when the QD energy levels are in resonance with $\mu_\mathrm{S,D}$ (Fig. 5.5d). The spacing between the resonance peaks in gate voltage ΔV_G is proportional to E_add with the gate leverarm α as the coefficient of proportionality $E_\mathrm{add} = e\alpha\Delta V_\mathrm{G}$. If the tunnel coupling between the QD and leads is low, the shape of the resonance peaks

can be approximated by a Lorentzian.

Similarly, applying a potential difference V_{SD} between the source and drain such that $\mu_{\mathrm{S}} \geq \mu_N \geq \mu_{\mathrm{D}}$ allows current to flow from source to drain through the QD (Fig. 5.6a). By mapping out $G(V_{\mathrm{G}}, V_{\mathrm{SD}})$, diamond shaped regions of zero conductance where the QD is in Coulomb blockade are revealed in the source-drain bias spectrum (Fig. 5.6c). The positive slopes defining the edges of these Coulomb diamonds correspond to a situation where $\mu_{\mathrm{S}} = \mu_N$ and the negative slopes where $\mu_{\mathrm{D}} = \mu_N$. The height of the Coulomb diamonds corresponds to the QD addition energy ($\mu_{\mathrm{S}} = \mu_{N+1}$ and $\mu_{\mathrm{D}} = \mu_N$) and the ratio between the Coulomb diamond height and width provides α of the plunger gate.

In addition to electron transport through QD ground states, excited states can also contribute to electron transport through the QD if both the excited state $\mu_N^{(n,m)}$ and the ground state μ_N are within the bias window ($\mu_{\mathrm{D}} : \mu_{\mathrm{S}}$) (Fig. 5.6b). Electron transport through excited states manifests as lines parallel to the Coulomb diamond edges in source-drain bias spectroscopy (Fig. 5.6d). The energy difference between the Coulomb diamond boundary and the excited state in V_{SD} can be used to extract ΔE.

5.4 Quantum Dots in SAG NWs

Scaling from the well-demonstrated instances of single and handfuls of interconnected QDs to large-scale quantum circuits and computers recalls many of the issues discussed thus far; e.g. the problematic nature of increasing cryogenic wiring and statistically significant evaluation of device reproducibility. In this respect, the intrinsic confinement of NWs may provide a benefit over 2D systems which require gate-defined confinement. Cross-bar gate geometries where a common set of gates are used for overall tuning of a large QD array may reduce the number of gate-lines required per device [136].

Sharing of gates in the cross-bar geometry requires a degree of reproducibility between devices. However, acquiring statistical information regarding the device variability in NW devices is not an easy task. While QDs in VLS NWs have been studied for decades [137–143], the scaling and reproducibility have not been explored due to the fabrication challenges inherent to the platform.

Here the multiplexer-demultiplexer circuit is employed to realize and characterize a large array of SAG NW-based QD devices providing insight into the reproducibility and variability of such devices. Figure 5.7a shows an SEM micrograph of a part of an array of 50 lithographically identical SAG QD devices embedded in the multiplexer-demultiplexer DUT layer. Each device consists of a SAG NW with two ohmic contacts spaced by 900 nm and the devices in the array share three local cross-bar top-gates with an inter-gate spacing of 150 nm. The outer gates are 300 nm wide and have a 120 nm overlap with the contacts. A schematic depiction of the system is shown in Fig. 5.7b. Even though the devices are defined identically, variations in the NW structure and the disorder electrostatic potential leads to differences

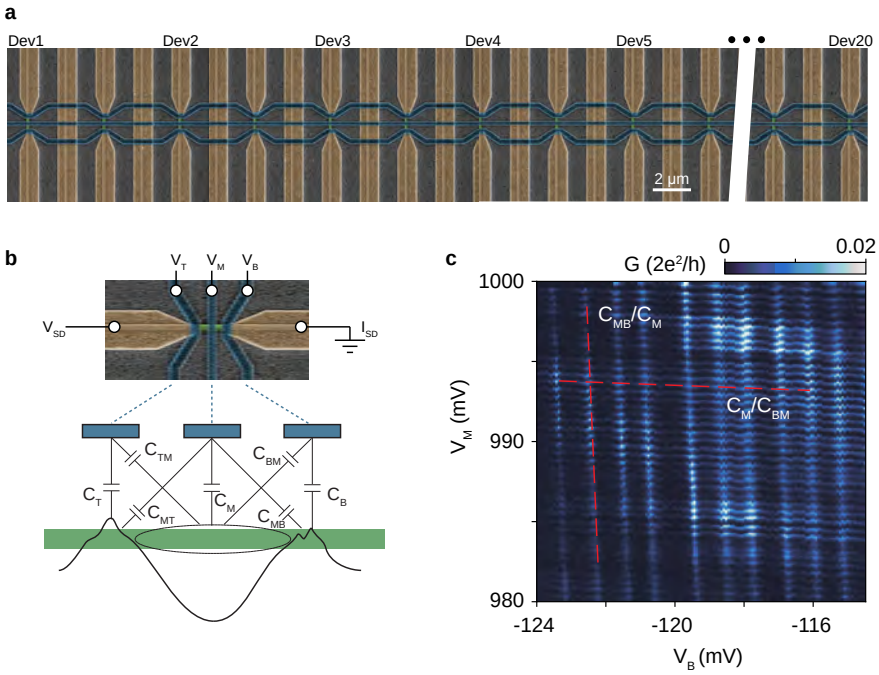


Figure 5.7: **a** False colored SEM micrograph of multiple QD devices. Ti/Au contacts in gold, InAs in green and Ti/Au top gates in blue. The gates are shared between 50 devices of which 20 were measured. **b** Schematic depiction of the system and the relevant capacitances **c** Conductance as function of V_B and V_M. Red dashed lines indicate the cross-capacitances.

between the devices [23, 24].

Applying negative potentials V_T and V_B to the outer gates induces tunnel barriers thus defining a QD in the middle NW segment which can be tuned by the potential V_M applied to the 200 nm wide middle gate. Finite capacitive coupling of the barrier gates to the QD and the middle gate to the barriers illustrated in Fig. 5.7b also has to be taken into account. As an example, consider the conductance as function of V_B and V_M shown in Fig. 5.7c. Two sets of resonances can be observed -

nearly horizontal and nearly vertical. The horizontal features are more coupled to V_M and result from the QD formed in the middle segment. The vertical resonances, however, are strongly coupled to V_B and are attributed to accidental QDs below the barrier gate resulting from the local disorder potential. The slopes of the resonances indicated by the dashed red lines show the ratio of couplings to both gates.

QD Parameters of a Single Device

All 50 QD devices were measured, but the new paradigm of multiplexer enabled-measurements revealed a new bottleneck; data analysis time. Since this is is still done semi-manually, every second device (denoted Dev1-Dev20 in Fig. 5.7a) was characterised in depth, to ensure that the entire spatial extent of the array was covered. Further in-depth analysis could be enabled by machine learning techniques [3, 4, 23, 144, 145].

First consider a single QD device, Fig. 5.8d shows the conductance G of Dev1 as a function of V_T and V_B for fixed $V_M = 1\,\mathrm{V}$. The NW can be pinched off by either gate at $\sim -300\,\mathrm{mV}$ and the pinch-off of each gate is independent of the potential on the other consistent with a negligible cross-capacitance as expected due to the spatial separation of the barrier gates and the screening by the middle gate. As before, the horizontal and vertical resonances observed in Fig. 5.8d are attributed to disorder-related potential fluctuations below each gate.

Figure 5.8a shows the differential conductance dI_{SD}/dV_{SD} as a function of V_{SD} and V_M acquired with compensated parameter $V_{T(B)} = V^0_{T(B)} + C_{T(B),M} \cdot V_M$ where $V^0_T, V^0_B = 140, 40\,\mathrm{mV}$ (red dot in panel c). The second term accounts for couplings $C_{MT} = -0.032\,\mathrm{V/V}$ and $C_{MB} = -0.022\,\mathrm{V/V}$ of the middle gate to the barriers discussed before. This compensation ensures the effective tunnel barriers are kept constant during the V_M sweep by compensating V_T and V_B.

Well-defined Coulomb diamonds are clearly observed in the spec-

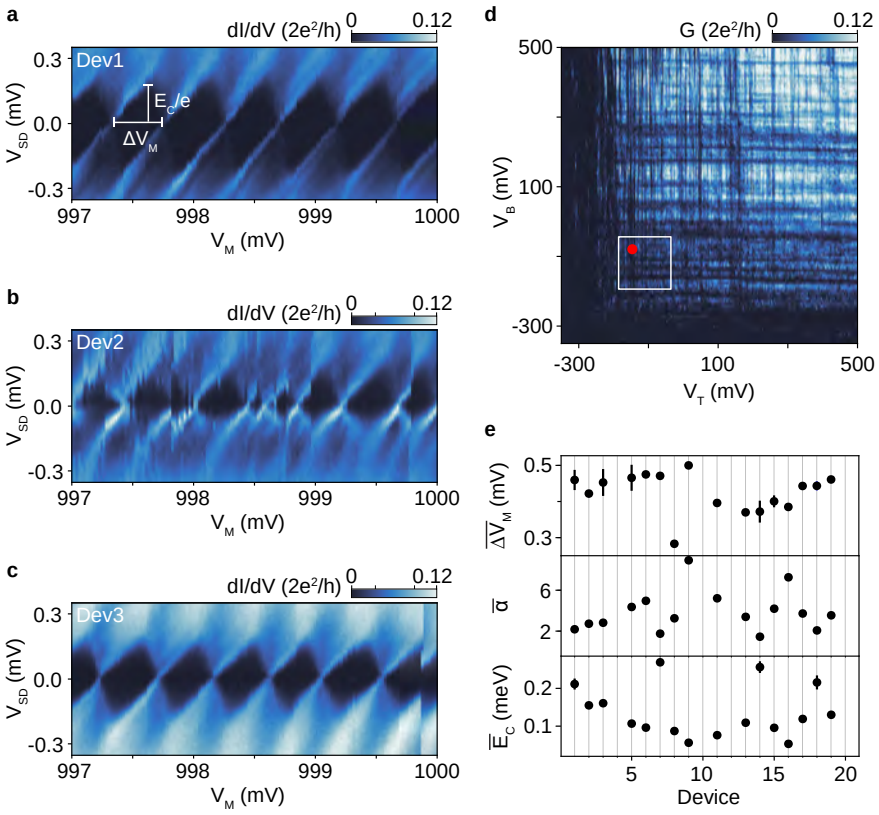


Figure 5.8: **a-c** Source-drain bias spectra of Dev1-Dev3 taken for V_{T} and V_{B} values corresponding to the red dot in d. **d** Conductance as function of V_{T} and V_{B} for Dev1. **e** $\overline{\Delta V_{\mathrm{M}}}$, $\overline{\alpha}$, and $\overline{E_{\mathrm{C}}}$ extracted from bias spectra for Dev1-Dev20.

trum in Fig. 5.8a. As discussed in Section 5.3 the height of each Coulomb diamond gives the addition energy $E_{\mathrm{add}} = eV_{\mathrm{SD}}$. Based on the approximately constant size between even and odd Coulomb diamonds it is assumed that the QD level spacing ΔE is much smaller than the electrostatic charging energy E_{C} ($\Delta E \sim 0.1E_{\mathrm{C}}$) and $E_{\mathrm{C}} \sim E_{\mathrm{add}}$. This will be expanded upon in later analysis.

With that in mind an average charging energy $\overline{E_C} \sim 210 \pm 15\,\mu$eV and average peak spacing $\overline{\Delta V_M} \sim 0.4\,$mV is extracted. This corresponds to a gate capacitance of $e/\Delta V_M \sim 0.4\,$fF in good agreement with the capacitance $C_M = 0.38\,$fF expected from a simple parallel plate capacitor model supporting that the QD confinement is defined by the gates as intended and not random disorder potential.

The QD Ensamble

Thus far the values of cross-bar potentials $V^0_{T(B)}$ have been chosen specifically for tuning Dev1 into the Coulomb blockade regime, now the entire QD ensemble is considered. The QD devices are lithographically identical, however, the structural and electrostatic variations of the nominally identical NW lead to a finite width of the V_{TH} distribution as discussed in Sections 5.2 and 5.1. To address the reproducibility and scalability aspects of SAG NW QDs it is investigated to what degree common cross-bar gate potentials can simultaneously tune devices across the NW array.

Maintaining the tuning parameters chosen for Dev1, automated source-drain bias spectroscopy measurements are performed for Dev2-20. The resulting spectra for Dev2 and Dev3 are shown in Fig. 5.8b and c and the spectra of other devices are included in Appendix B4. Here a challenge associated with the operation of the multiplexer-demultiplexer circuit should be noted - devices that are not actively addressed are electrically floating. This means that after addressing a device it takes some time for the electrostatic environment to settle as a result switchy behaviour can be observed in these source-drain bias spectra. Out of the 20 measured devices 16 show at least one complete, well-defined Coulomb diamond. However, qualitatively all 20 devices show signatures of Coulomb blockade. This was also later confirmed by measurements with a longer waiting time before starting a measurement after addressing a new device but this data is not

analyzed as part of this thesis.

The mean values of ΔV_{M}, E_{C}, and leverarm α are extracted for all 16 devices where at least one complete Coulomb diamond can be identified and shown in Fig. 5.8e. At these specific barrier gate potentials ΔV_{M} varies across devices from $283\,\mu$V to $500\,\mu$V with a mean value of $425\,\mu$V. Similarly, α varies from 1.45, to 8.93 with a mean of 3.87 and E_{C} varies from $53\,\mu$eV to $269\,\mu$eV with a mean of $140\,\mu$eV. Across all the devices ΔV_{M} and E_{C} are of similar magnitude indicating that the measured QDs are of similar dimensions and defined by V_{T} and V_{B} rather than random disorder.

Common Tuning of the QD Ensamble

To investigate the sensitivity of the SAG QD ensemble to the common cross-bar tuning, zero bias conductance as a function of middle gate potential $G(V_{\mathrm{M}})$ was measured for all 20 devices for 11×11 evenly spaced combinations of (V_{T}, V_{B}) forming a grid spanning the white square in Fig. 5.8d resulting 2420 individual $G(V_{\mathrm{M}})$ traces. As an example, 220 normalized $G(V_{\mathrm{M}})$ traces are shown in Fig. 5.9a for $V_{\mathrm{B}} = -50\,\mathrm{mV}$ to $-200\,\mathrm{mV}$ with $V_{\mathrm{T}} = -50\,\mathrm{mV}$ to give an overall impression of the collected data.

In each of the 2420 traces any Coulomb peaks were manually identified. To facilitate the process an interactive python program was developed. The program displays datasets sequentially and allows to identify the range in which Coulomb peaks occur for use in fitting later. Any Coulomb peaks can be marked by clicking in the vicinity of the peak. The cursor snaps to local maxima streamlining the process.

The identified peaks were then fit to a sequence of Lorentzians as shown in Fig. 5.9b from which the average Coulomb blockade peak spacings $\overline{\Delta V_{\mathrm{M}}}$, and the average value of the ratio of peak width to peak spacing $\overline{\Gamma}$ (proportional to the QD tunnel coupling) are extracted

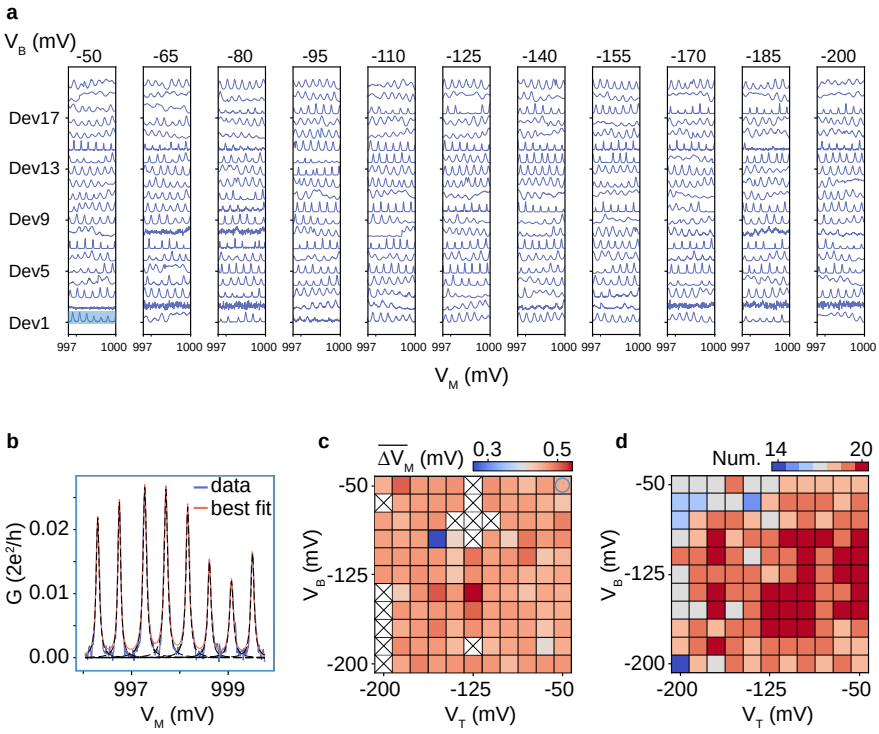


Figure 5.9: **a** Examples of $G(V_\mathrm{M})$ for $V_\mathrm{T} = -50\,\mathrm{mV}$ and $V_\mathrm{B} = -50\,\mathrm{mV}$ to $-200\,\mathrm{mV}$ corresponding to the rightmost column of c and d. Conductance normalized 0 to 1 and offset by 1.2 for clarity. **b** Example of data and fit for Dev1 with $V_\mathrm{T,B} = -50\,\mathrm{mV}$ (blue rectangle in a and blue circle in c). **c** Map showing $\overline{\Delta V_\mathrm{M}}$ of Dev1 for various V_T and V_B combinations. Crossed areas have no identifiable Coulomb peaks. **d** Number of devices with identifiable Coulomb peaks at various combinations of V_T and V_B voltages.

for each device. The averages are calculated for each $G(V_\mathrm{M})$ trace individually. $\overline{\Delta V_\mathrm{M}}$ is simply the arithmetic mean of all ΔV_M and $\overline{\Gamma}$ is calculated as the ratio of the mean full width at half maximum for all peaks and $\overline{\Delta V_\mathrm{M}}$. As an example, Fig. 5.9c shows $\overline{\Delta V_\mathrm{M}}$ at each of the 121 combinations of (V_T, V_B) for Dev1. Coulomb blockade peaks

with a consistent peak spacing were found in 108 of the 121 points in gate-space and gate-space points where no peaks were observed are marked with crosses.

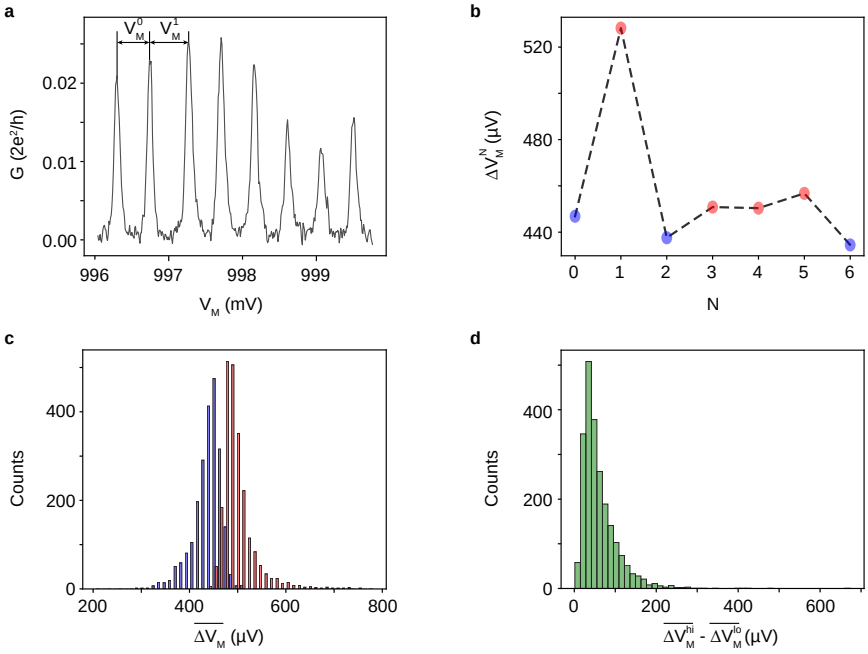


Figure 5.10: **a** Example of $G(V_\mathrm{M})$, $\Delta V_\mathrm{M} \propto E_\mathrm{add}$. **b** Variation in ΔV_M as function of added electron. Blue and red indicates the sorting into V_M^lo and V_M^hi respectively. **c** Distribution of $\overline{V_\mathrm{M}^\mathrm{lo}}$ (blue) and $\overline{V_\mathrm{M}^\mathrm{hi}}$ (red) across all $G(V_\mathrm{M})$ traces. **d** Distribution of $\overline{V_\mathrm{M}^\mathrm{hi}} - \overline{V_\mathrm{M}^\mathrm{lo}}$ proportional to ΔE

It should be noted that this treatment considering mean values assumes that the QD level spacing ΔE is much smaller than the electrostatic charging energy E_C. This can be verified by observing the features produced by excited states in the source-drain bias spectra. An additional test is to compare the magnitude of even and odd ΔV_M which is proportional to the addition energy E_add for each $G(V_\mathrm{M})$

trace (Fig. 5.10a). For each odd electron $E_{\mathrm{add}} = E_{\mathrm{C}}$ while for even electrons $E_{\mathrm{add}} = E_{\mathrm{C}} + \Delta E$. The exact electron occupancy in these experiments is unknown, thus to automate the analysis V_{M} for each $G(V_{\mathrm{M}})$ trace is split into the lesser half and the greater half (blue and red circles in Fig. 5.10b) and averaged yielding $\overline{V_{\mathrm{M}}^{\mathrm{lo}}}$ and $\overline{V_{\mathrm{M}}^{\mathrm{hi}}}$ (blue and red histograms in Fig. 5.10c). The difference $\overline{V_{\mathrm{M}}^{\mathrm{hi}}} - \overline{V_{\mathrm{M}}^{\mathrm{lo}}}$ is proportional to ΔE. From the distribution in Fig. 5.10d it is found that the magnitude of ΔE is $\sim 10\%$ of E_{C} and this is consistent with the excited states observed in bias spectra. Thus it is considered in the analysis that $\Delta E << E_{\mathrm{C}}$.

Considering all 20 devices, Fig. 5.9d shows the number of devices at each combination of (V_{T}, V_{B}) that show identifiable Coulomb peaks in $G(V_{\mathrm{M}})$ with a consistent peak spacing. Similar to the SAG NWFET devices, all measured QD devices are operational and QDs are consistently formed across all devices when keeping common values of the cross-bar gate tuning. In 93% of the measured $G(V_{\mathrm{M}})$ traces across a range of barrier gate potentials Coulomb peaks could be identified and there are significant regions in parameter space where all devices concurrently exhibit Coulomb blockade.

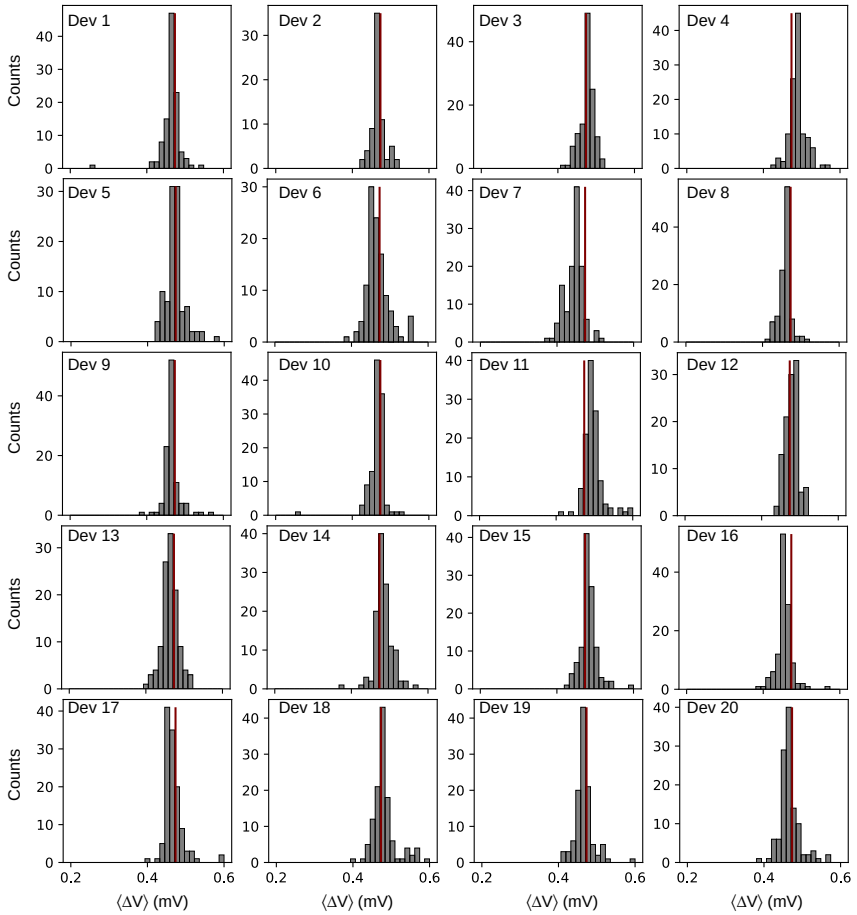


Figure 5.11: Histograms showing distributions of $\overline{\Delta V_{\mathrm{M}}}$ across all barrier gate voltage combinations for individual QD devices discussed in 5.4. The red line indicates the overall mean between all data points across all devices.

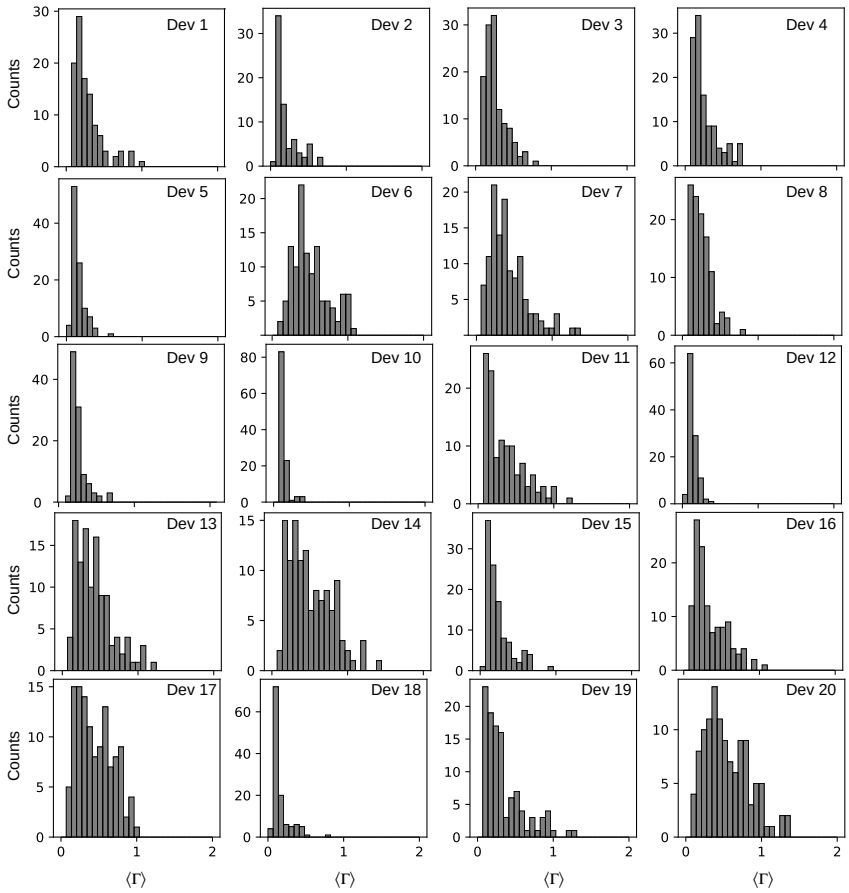


Figure 5.12: Histograms showing distributions of $\overline{\Gamma}$ across all barrier gate voltage combinations for individual QD devices discussed in 5.4.

QD Statistics

Figure 5.11 and Fig. 5.12 shows histograms of $\overline{\Delta V_{\mathrm{M}}}$ and $\overline{\Gamma}$ for all 20 QD devices across all 121 combinations of (V_{T}, V_{B}). The distribution of $\overline{\Delta V_{\mathrm{M}}}$ across all devices and points in gate-space is shown in Fig. 5.13a and has a mean of 471 μV and a standard deviation of 27 μV. Similarly, Fig. 5.13b shows the distribution of $\overline{\Gamma}$.

The distribution of $\overline{\Gamma}$ is strongly shifted towards narrow peaks. Assuming a typical charging energy of 140 μeV by taking the mean value of $\overline{E_{\mathrm{C}}}$ extracted from the bias spectra of all devices (Fig. 5.8a), the most probable $\overline{\Gamma}$ is 18 μeV. This is close to the lower limit set by thermal broadening $\Gamma_T = 3.5 k_{\mathrm{B}} T = 9\,\mu$eV assuming an electron temperature $\sim$ 25 mK. However, the spread of the distribution also shows that a range of tunnel couplings are realized in the chosen range of barrier gate potentials.

Similar to the FET characteristics investigated in Section 5.2, the reproducibility of $\overline{\Delta V_{\mathrm{M}}}$ and $\overline{\Gamma}$ across nominally identical devices is affected both by variations in the geometry of the device and the electrostatic environment. The conductance resonances below the barrier gates evident as the horizontal and vertical structures in Fig. 5.7c are natural sources of variation since the modulation of the conductance at the QD operation range close to pinch-off corresponds to variations in tunnel couplings and the electrostatic confinement. Comparing the distributions of individual devices in Fig. 5.13c (also Fig. 5.11 and Fig. 5.12) it is evident that some devices (e.g. Dev10 and Dev12) have a much narrower distribution of $\overline{\Gamma}$ and $\overline{\Delta V_{\mathrm{M}}}$ than others (e.g. Dev11 and Dev13) consistent with a variation of the overall V_{TH}. The interquartile range (a useful metric for spread in highly skewed distributions) of the $\overline{\Gamma}$ distributions also shows variations among devices and correlates with the interquartile range of the $\overline{\Delta V_{\mathrm{M}}}$ distributions as seen in Fig. 5.13b ($\rho = 0.53$; $p = 0.016$).

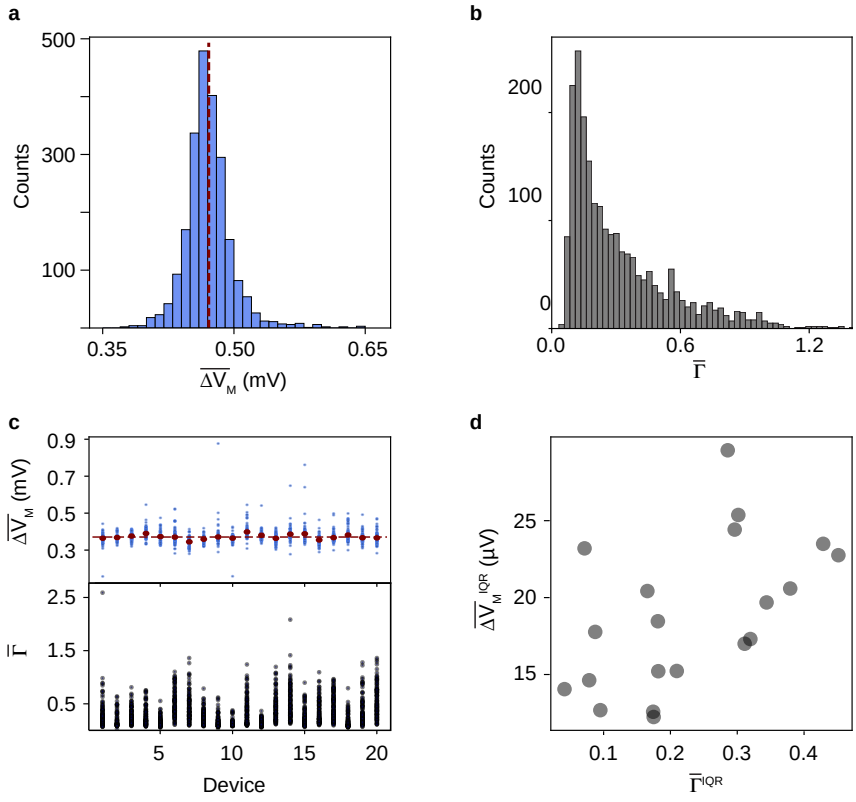


Figure 5.13: **a, b** Histogram of $\overline{\Delta V_{\mathrm{M}}}$ and $\overline{\Gamma}$ respectively for 20 QD devices across 121 V_{T} and V_{B} combinations. **c** $\overline{\Delta V_{\mathrm{M}}}$ and $\overline{\Gamma}$ distributions for Dev1-Dev20, red points indicate individual device mean, red line shows overall mean across all devices. **d** Correlation between the interquartile range of $\overline{\Gamma}$ and $\langle \Delta V_{\mathrm{TH}} \rangle$ for individual devices.

It is important to note that the proof of principle QD array used in these measurements uses relatively large gate pitches and NW widths which is the reason for the comparatively small E_{add}. It is straightforward to optimize these geometries for controlling the energy scales of the QDs, fabricating multi-dot systems on the same NW [146] and

optimizing the sensitivity of the QDs to the environment. In this respect, the multiplexer-demultiplexer setup demonstrated here can be an efficient tool for quantifying the results of such efforts allowing benchmarking of the system and establishing tolerances. It should also be noted that from the QD measurements presented the electron occupation is not known and for the SAG NW QDs to be relevant as qubits both individual tuning gates and charge sensors will have to be integrated in order to realize the few-electron regime. Again, this regime has been demonstrated for VLS NWs [147, 148] and similar strategies can likely be employed in this system.

Combined, the results presented in this Section show that SAG NWs can serve as a scalable platform for realising large ensembles of QDs. Using standard procedures devices show sufficiently low variability that common gate parameters can simultaneously tune the entire ensemble into the Coulomb blockade regime with consistent parameters both across devices and barrier gate potentials. The multiplexer-demultiplexer setup allows to quantify the reproducibility of QD parameters and suggests that local fluctuations in the electrostatic environment play a dominating role in device variance. This is similar to the situation in conventional VLS NW QDs where charge traps in the gate oxide are often dominating [149]. It is likely that the methods developed for achieving monotonic pinch-off and quantum point contact behavior in VLS NWs [150, 151] can also be successfully employed here.

6

6 Effect of Dimensions and Morphology

6.1 FET Parameter Dependence on Channel Length

The greatly increased device count enabled by the multiplexer-demultiplexer circuit can also be used to probe the correlation between device geometry and device performance with a level of detail unfeasible using traditional measurement procedures. Trends based on device geometry, for example semiconductor channel length, are typically difficult to establish convincingly due to the limited number of devices available and conclusions often rely on the results from few devices. It has been established in Sections 5.1 and 5.2 that NW structure influences the electron transport characteristics of NWFET devices. In this Section the dependence of NWFET electron transport characteristics on semiconductor NW segment length, width, and crystal misalignment is investigated by comparing devices where these parameters are systematically varied.

Figure 6.1a shows a series of 50 NWFET devices with the semiconductor NW segment length L linearly decreasing from 6 μm to 50 nm and the gate electrode covers the entire semiconductor segment. The source and drain contacts of the 50 nm long junction device are shorted as a result of fabrication failure and the device cannot be used, all other devices function as intended. Each NWFET device has a short on the adjacent multiplexer output for estimating the circuit series resistance. However, it must be noted that this does not exclude contact resistance R_{C} to the NW thus the total resistance of each device is $R = R_{\mathrm{NW}} + R_{\mathrm{C}}$, where R_{NW} is the resistance of the NW. The electron transport characteristics are investigated at $T = 100\,\mathrm{K}$ (Fig. 6.1b, c, d) and $T = 20\,\mathrm{mK}$ (Fig. 6.1e, f, g).

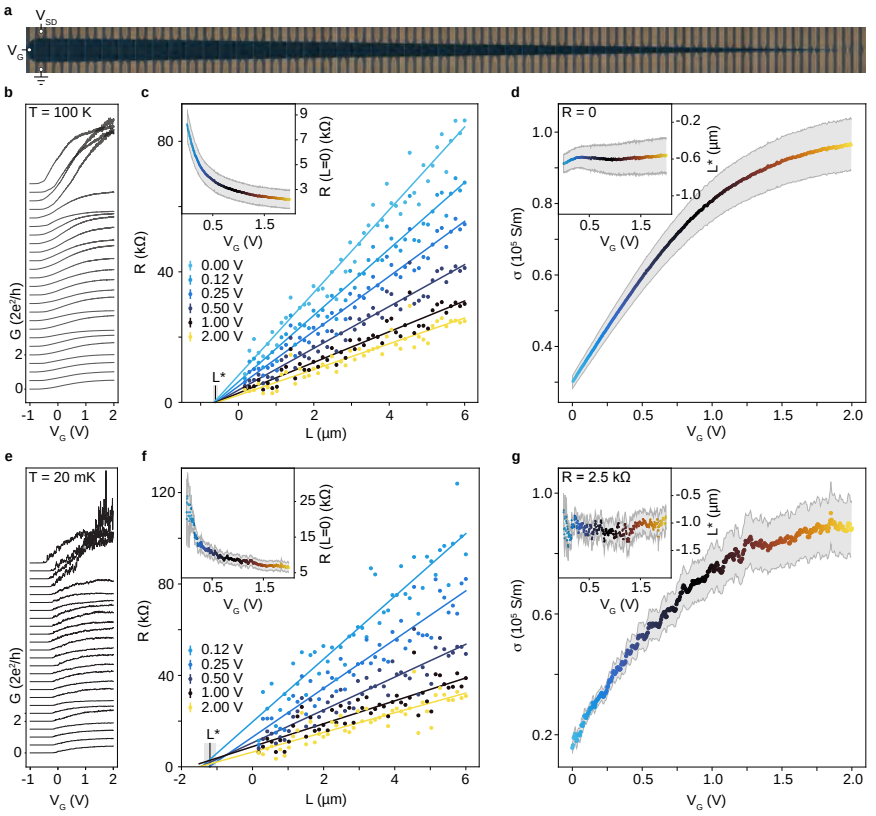


Figure 6.1: **a** SEM micrograph of NWFET devices with length of the semiconductor channel changing linearly from 6 µm to 50 nm. A short adjacent to each device allows to estimate the circuit series resistance. Ti/Au ohmic contacts in gold and Ti/Au topgate in blue. **b** **(e)** G after subtraction of circuit series resistance as function of V_G at $T = 100\,\mathrm{K}$ ($T = 20\,\mathrm{mK}$) for every odd device with InAs channel lengths decreasing from bottom to top. The traces are offset by e^2/h in G for clarity. **c** **(f)** $R(L)$ at various V_G with $T = 100\,\mathrm{K}$ ($T = 20\,\mathrm{mK}$) with linear fits to the data. Colors match the points in d (g). Inset shows $R(L = 0, V_\mathrm{G})$. **d** **(g)** Conductivity as function of V_G at $T = 100\,\mathrm{K}$ ($T = 20\,\mathrm{mK}$). Inset shows channel length correction L^* as function of V_G. Grey bands show the confidence intervals.

Figure 6.1b shows conductance G as function of gate voltage V_G for every odd-numbered device with L decreasing from 6 μm to 170 nm bottom trace to top trace (Full dataset is shown in B2). Circuit series resistance estimated from the adjacent shorts is subtracted and the traces are offset in conductance by e^2/h for clarity. The device resistance increases linearly with decreasing channel length as seen in Fig. 6.1c where plots of $R(L)$ are shown for selected values of V_G consistent with $R = R_C + R_{NW}$ where $R_{NW} = \rho\frac{L}{A}$ and R_C is the contact resistance. The solid lines show linear fits to the data and by extrapolating to $R(L = 0)$ ($R \to R_C$ for $L \to 0$) it is possible to estimate R_C [152].

The inset to Fig. 6.1c shows the resulting R_C values as a function of V_G. The values range from 2 kΩ to 8 kΩ, surprisingly, there is also a systematic dependence on V_G. This is unexpected since R_C ideally is constant and the local topgates do not affect the NW underneath the contacts as a global backgate might. Extrapolating the linear fits to their crossing point a common R_C in the range $0 - 500\,\Omega$ is found at $L = L^* = -0.6 \pm 0.2\,\mu$m (inset of Fig. 6.1d) [153].

A possible explanation for these two phenomena is that the true length of the semiconductor channel is larger than the lithographically defined spacing between the contacts. Thus, instead of electrical contact between the Ti/Au and InAs abruptly forming at the edge of the metal contact the data is consistent with a contact formed gradually over a distance of $\sim L^*/2$ from the edge of the metal at both the source and drain contact. Performing the same analysis for the data where $T = 20$ mK reveals similar trends, and the extrapolated $R(L)$ trends yield $R_C \sim 2.5$ kΩ and $L^* = -1 \pm 0.5\,\mu$m. The increase in R_C with decreasing temperature is consistent with a lower number of thermally excited carriers [154].

Using the cross-section area of the InAs nanowire $A \sim 2630\,\text{nm}^2$ from the TEM and AFM analysis discussed in Section 5.1 it is possible

to extract the conductivity σ as a function of V_G from the slopes of the linear fits to $R(L)$ in Fig. 6.1c, f independent of R_C. The extracted $\sigma(V_G)$ are shown in Fig. 6.1d, g, it is observed that for $V_G < 0.75\,V$ σ increases linearly consistent with the Drude model $\sigma = \mu n e$, where $n \propto V_G$ is the charge carrier density and e is the electron charge. This is consistent with constant electron mobility μ, however, the absolute value of μ cannot be extracted as the value of V_G where n becomes vanishingly small is unknown. It is also observed that for $V_G > 0.75\,V$ the slope of $\sigma(V_G)$ decreases indicating reducing μ due to increased contribution from electron sub-band scattering and surface scattering as n increases and electrons are pulled closer to the NW surface where charge traps contribute to increased scattering [72, 98, 155].

6.2 Mask Opening Influence on SAG NW Morphology

Selective area growth NWs are defined by openings in the oxide mask. As these openings are lithographically defined, they can be adjusted to control the resulting NW morphology. Increasing the width of the mask opening allows a larger growth area, but the size of the NWs is still limited by the amount of material available. The orientation of the SAG NWs is constrained by the high symmetry crystal directions due to thermodynamic energy minimization [88]. Misalignment of the oxide mask openings can occur due to a combination of improper alignment during lithography and incorrect cut of the wafer major flat. Even if the mask openings are not properly aligned with the underlying crystal directions, the NWs will still retain the preferred high symmetry facets and if the misalignment is sufficient this will lead to dislocations, steps, and discontinuities [73, 88] in the resulting NWs which can also affect the electrical properties of the NWs.

We now consider SAG NWs that are grown on GaAs [3 1 1] substrates and are oriented lengthwise along the $[0\,\bar{1}\,1]$ crystal direction resulting (1 1 1) NW facets as discussed in Section 3.1. Nanowires defined by mask openings 80, 100, 140, 180, 220, 260, and 300 nm wide (W1-W7) and intentionally misaligned to the $[0\,\bar{1}\,1]$ crystal direction by $\pm 5^\circ$ are explored to investigate the effect on the NW morphology.

Figure 6.2a shows AFM micrographs of segments of InAs SAG NWs defined by mask opening widths W1-W7 with misalignment to the $[0\,\bar{1}\,1]$ crystal direction $\theta = \pm 5^\circ$ and Fig. 6.2b shows AFM micrographs for the case $\theta = 0$. As the mask opening width is increased the width of the NWs also increases, however, the NW size is lim-

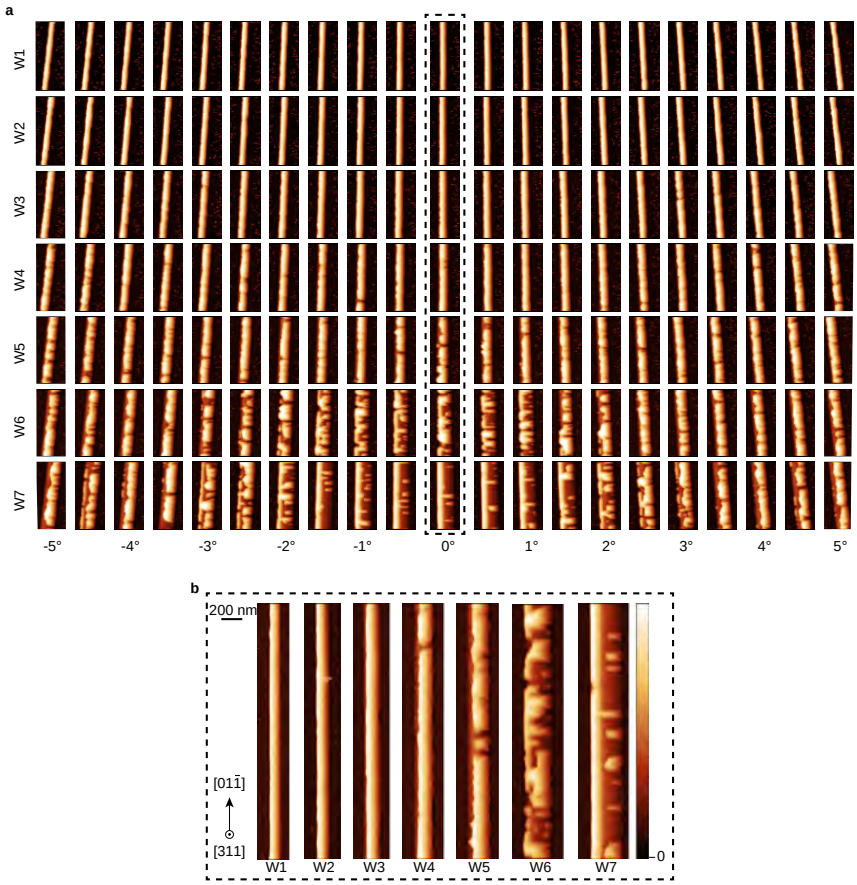


Figure 6.2: **a** AFM micrographs of SAG NW segments defined by $80 - 300\,\text{nm}$ (W1-W7) mask openings misaligned to the $[0\,1\,\bar{1}]$ crystal direction by $\pm 5°$. **b** AFM micrographs of InAs SAG NW segments defined by mask opening widths (W1-W7) aligned to the $[0\,1\,\bar{1}]$ crystal direction. (AFM credit: Gunjan Nagda)

ited by the amount of available material leading to discontinuous NW growth and inhomogeneous morphology for W4-W7. Taking a closer look, Fig. 6.3 shows high angle annular dark-field scanning transmission electron microscope (HAADF-STEM) micrographs of focused ion

beam (FIB) cross sections of NWs. Additionally, Fig. 6.3 also shows GPA revealing dilatation and rotation of the $(1\,\overline{1}\,\overline{1})$ and $(1\,1\,1)$ crystal planes in the NWs. Cross section analysis is only available for NW widths W1-W4 and W7 ($\theta = 0$) due to the complexity and time consuming nature of sample preparation and analysis.

Combining the insights from the AFM and cross-section TEM it can be observed that the NW morphology gradually changes as the width of the mask openings increases. For the narrowest mask openings (W1, W2) the InAs covers both facets of the GaAs buffer but as the width of the mask opening increases there is not enough material available to cover the entire GaAs buffer. The NW morphology then changes to form a continuous film on the largest buffer facet (W3, W4, W5), however, as the opening is increased further, partially discontinuous growth occurs on both facets of the buffer (W6). Discontinuities and variation of NW width occur frequently for widths W4-W6. Finally, for the widest mask opening (W7) the NW growth results in InAs covering only the smaller facet of the buffer yielding an approximately symmetric, continuous, and tilted (relative to substrate surface) NW. Even though from AFM the NWs defined by mask opening width W7 appear narrower with widths comparable to NWs defined by W2 or W3, cross-section TEM reveals that the NWs defined by W7 still have the largest cross-section area.

The dilatation and rotation GPA maps show that an array of misfit dislocations is generated at the GaAs/InAs interface as an inelastic strain relaxation mechanism [156]. Elastic asymmetric rotation of the crystal planes is also observed in the rotation maps as another relaxation mechanism. From the dilatation maps it is seen that the InAs crystal planes are compressed and relax gradually for W1-W4 in Fig. 6.3 while for W7 the relaxation is comparatively abrupt and localized closer to the GaAs/InAs interface.

Spatially-resolved elemental composition of the NW cross-sections

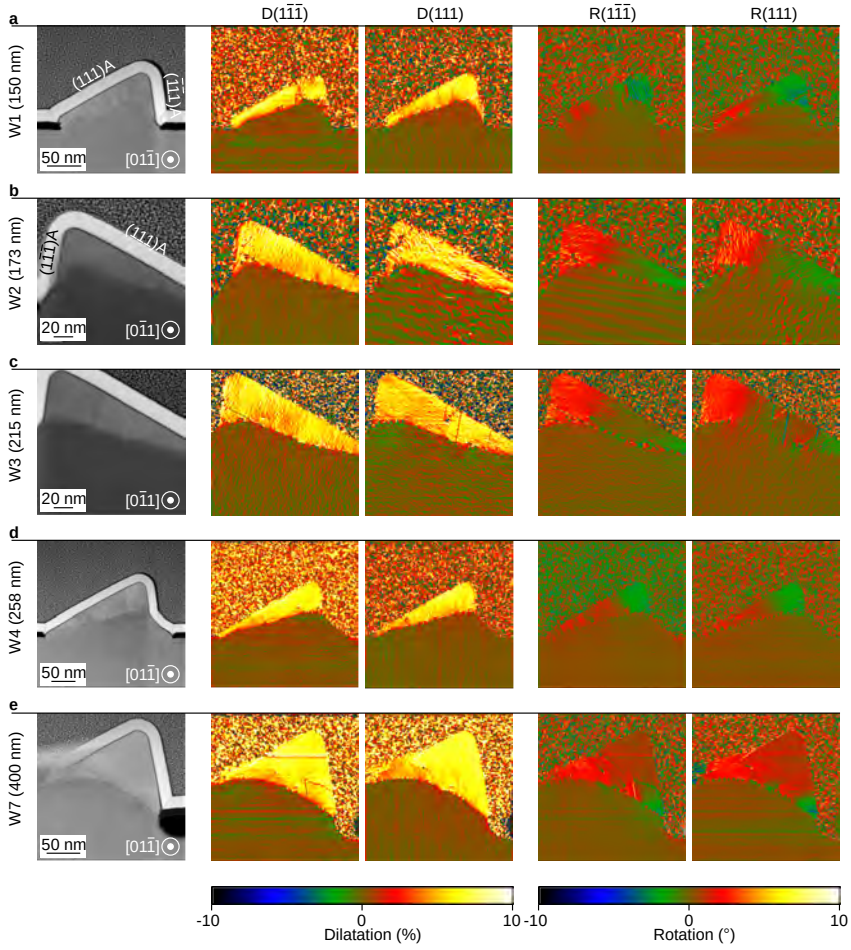


Figure 6.3: HAADF-STEM micrographs of SAG NW FIB cross sections as well as GPA dilatation and rotation maps of $(1\,\bar{1}\,\bar{1})$ and $(1\,1\,1)$ crystal planes for NW widths W1, W2, W3, W4, W7. (data credit: Sara Marti-Sanchez, Jordi Arbiol)

is acquired via EELS. The top and bottom rows of Fig. 6.4 show the relative atomic percent of In and Ga respectively. The composition maps reveal diffusion of Ga into the InAs NW from the buffer. A

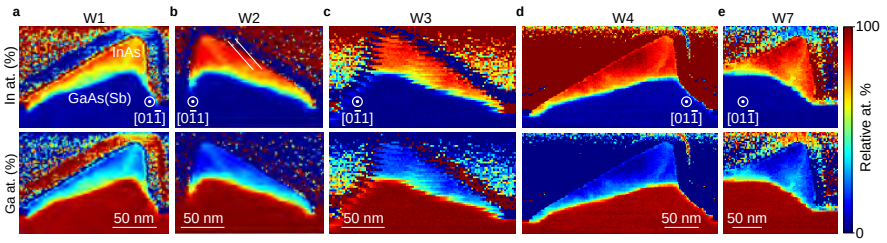


Figure 6.4: **a-e** Atomic composition EELS map relative to In (top row) and Ga (bottom row) of NWs defined by mask opening widths W1-W4 and W7 respectively. The distortion in c is caused by spatial drift. (EELS data credit: Sara Marti-Sanchez, Jordi Arbiol)

transition zone is observed at the interface where the relative atomic percent of In and Ga is approximately $50\% - 50\%$. Most of the bulk of the InAs NW also contains traces of Ga and the Ga concentration decreases towards the outer surface of the NW. For W1, the outer layers of the NW still contain $\sim 20\%$ Ga, for W2 and W3 the Ga content at the surface decreases to $\sim 10\%$, and for W4 and W7 regions of pure InAs (within measurement limits) exist at the outer layers of the NWs. The transition to InAs is also more abrupt for W7 in agreement with the strain relaxation observed by GPA. The Ga diffusion into the InAs is driven by the strain between the mismatched InAs and GaAs crystal lattices [71, 81, 157].

The NWs, though nominally identical, retain structural variation, which may reflect on the variability of electron transport parameters between lithographically identical devices. Various potential sources of electron scattering such as strain and interface defects are also identified. NWs of different widths in the same growth defined by changing the size of the mask openings also exhibit morphological and crystallographic variation which adds a layer of complexity to comparisons between the NW electron transport parameters.

6.3 FET Parameter Dependence on Mask Opening Geometry

Having seen the dramatic effect of mask opening width and alignment on the structural properties of SAG NWs, the effect on the electrical performance is now considered. Here the multiplexer-demultiplexer circuit again allows for a systematic investigation. To investigate the effect that the mask opening width and NW misalignment to the high-symmetry crystal directions of the growth substrate has on the electrical performance of NW devices a series of NWFETs were characterized.

Figure 6.5a-c shows optical microscope micrographs of multiplexer-demultiplexer circuits realized on the same growth wafer as the circuit discussed in the Section 5.2. A number of nominally identical NWFET devices for mask openings of widths 80, 180, and 300 nm (W1, W4, and W7) aligned to the $[0\,\bar{1}\,1]$ crystal direction are measured using the two circuits in Fig. 6.5a and b. Fig. 6.5d shows an SEM micrograph of the devices in the red box in Fig. 6.5b. The circuit shown in Fig. 6.5c is used to measure FETs based on NWs defined by mask openings deliberately misaligned to the $[0\,\bar{1}\,1]$ direction of the growth substrate by up to $\pm 4.5°$ with a step of $1°$ and widths of the mask openings: 80, 100, 140, 180, 220, 260 nm (W1-W6). An SEM micrograph of the NWFET devices is shown in Fig. 6.6e corresponding to the black rectangle in Fig. 6.6c. All NWFET devices have a semiconductor channel length of 1 µm and share a common topgate which spans the entire length of the channel, as before, adjacent shorts are used to estimate circuit series resistance.

Figure 6.6a-f shows $G(V_G)$ for each angle of misalignment to the

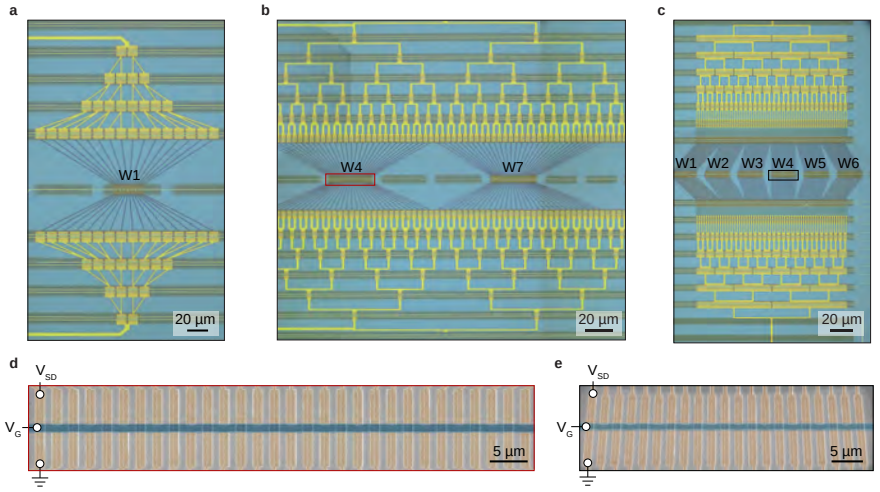


Figure 6.5: **a,b** Optical microscope micrographs of multiplexer circuits used to measure FET devices based on NWs defined by mask openings W1, W4, W7 aligned to the $[0\,\bar{1}\,1]$ crystal direction. **c** Optical microscope micrograph of a multiplexer circuit used to measure FET devices based on NWs defined by mask openings W1-W6 misaligned to the $[0\,\bar{1}\,1]$ crystal direction by $\pm 4.5°$. **d (e)** SEM micrograph of NWFET devices in the red (black) box in b (c). Ti/Au contacts in gold, Ti/Au topgate in blue.

$[0\,\bar{1}\,1]$ crystal direction θ for NWFETs based on NWs defined by mask openings W1-W6. For W1-W3 all devices are functioning as FETs, however for W4-W6 non-functional devices are observed indicated by the red arrows in Fig. 6.6. This is likely due to discontinuous InAs in the region beneath the gate as identified in Section 6.2 that the nanowires are often discontinuous for mask openings W4-W6 due to insufficient material.

Figure 6.6g-i shows $V_{\mathrm{TH}}(\theta)$, $\mu_{\mathrm{FE}}(\theta)$, and conductance $G^{1.5\mathrm{V}}(\theta)$ at fixed gate voltage $V_{\mathrm{G}} = V_{\mathrm{TH}} + 1.5\,\mathrm{V}$ respectively with data from non-functional devices dropped. No systematic dependence on θ is ob-

served for any of the mask opening widths W1-W6, however, some outliers can be identified marked by black arrows in Fig. 6.6. These outliers only appear for W4 and W5 and a likely explanation is that the poor NW structure for these mask opening widths results in thin constrictions that act as bottlenecks for electron transport. Removing these outliers does not reveal an underlying trend.

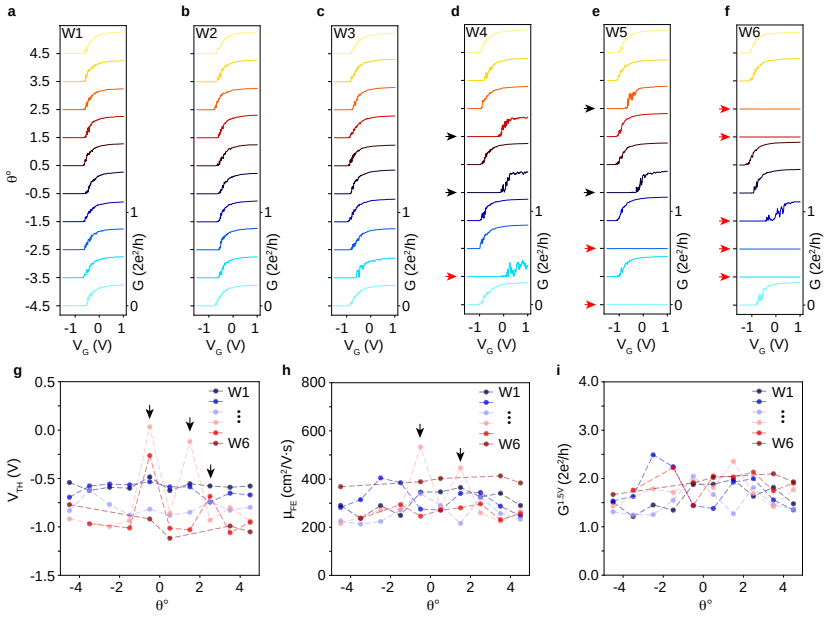


Figure 6.6: **a-f** Conductance as a function of V_{G} for different θ and mask openings widths (W1-W6). Traces offset in G by $0.3 \times 2e^2/h$ for clarity. **i-k** V_{TH}, μ_{FE}, and $G^{1.5\mathrm{V}}$ respectively as function of misalignment angle. **g, h, i** V_{TH}, μ_{FE}, and $G^1.5V$ respectively as a function of θ for mask opening widths W1-W6.

Considering the NWFETs aligned to the $[0\,\bar{1}\,1]$ crystal direction, the $G(V_{\mathrm{G}})$ of FETs based on NWs defined by mask opening widths W1, W4, and W7 is shown in Fig. 6.7a-c. For mask opening width W4 four devices are non-functional (red arrows in Fig. 6.7b), however,

for W7 no non-functional devices are observed confirming that the altered NW morphology discussed in Section 6.2 typically results in a continuous InAs NW. Comparing the V_{TH} and μ_{FE} of the FETs based on aligned NWs to the ones based on misaligned NWs (Fig. 6.7d and e) reveals a V_{TH} offset of $+0.2\,\mathrm{mV}$ and a doubling of μ_{FE} for the NWFETs aligned with the high-symmetry crystal direction. This indicates that the alignment of NWs to the crystal directions of the growth substrate is of paramount importance as misalignment as small as 0.5° can halve μ_{FE}.

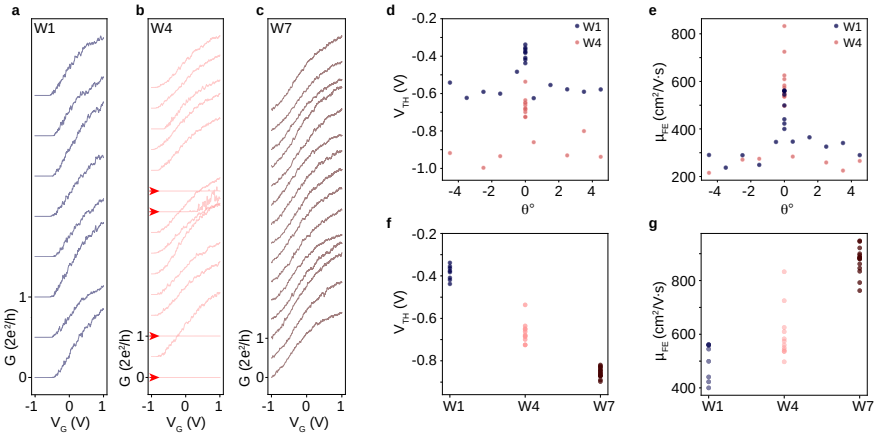


Figure 6.7: **a-c** $G(V_{\mathrm{G}})$ after subtraction of series resistance from adjacent short for W1, W4, and W7 respectively. Conductance traces offset in G by e^2/h for clarity. **d** $V_{\mathrm{TH}}(\theta)$ for W1 and W4. **e** $\mu_{\mathrm{FE}}(\theta)$ for W1 and W4. **f** V_{TH} as function of mask opening width. **g** μ_{FE} as function of mask opening width.

Comparing the electron transport properties of the aligned NWFETs based on NWs defined by different widths of mask openings, Fig. 6.7f and g show V_{TH} and μ_{FE} for mask openings W1, W4, and W7. The V_{TH} of the NWFETs decreases from $\sim -0.45\,\mathrm{V}$ to $\sim -0.90\,\mathrm{V}$. This can be related to the decreasing channel width - as the geomet-

rical size of the NWs decreases for smaller mask opening widths, V_{TH} increases due to quantum confinement effects in narrow channels [158–160].

An increase in μ_{FE} with increasing mask opening width is also observed (Fig. 6.7g). As the nanowire dimensions are proportional to the mask opening width a possible explanation is that for smaller NW widths the scattering at the NW surface plays a more important role [83, 161, 162]. From the structural study presented in Section 6.2 it also observed that strain relaxation is more confined to the vicinity of the InAs/GaAs interface for NWs defined by mask opening W7 possibly further reducing electron scattering rate and improving μ_{FE}. Of course it is important to note that the accuracy of the extracted value of μ_{FE} depends on the estimate of the gate capacitance. If the NW morphology change has a significant impact on the capacitance this can have an effect on the observed trend of μ_{FE}.

The results presented in this Section were acquired as part of prototyping the on-chip multiplexer circuit, thus the experiment is not tailored to comprehensively investigate the observed phenomena, however, the first steps have been made. It is observed that the alignment of the SAG mask openings to the high symmetry crystal directions of the growth substrate is of extreme importance as even a misalignment of 0.5° shifts the NWFET V_{TH} and halves μ_{FE}. However, no trends for $\theta > 0.5°$ are observed. With such a strong dependence on very small angles the tolerances of alignment may be more important than expected. The width of the mask openings together with the growth parameters affects the resulting morphology of the NWs which affects the electron transport parameters. To further explore these aspects more granularity of misalignment angles could reveal the trends of electron parameters for $\theta < 0.5°$, importantly, with $\theta = 0°$ NWFETs for all mask opening widths.

7 In-Plane VLS Growth From Out-of-Plane Facets

Freestanding NWs such as the ones grown via the VLS process are a commonly used platform for fundamental research into quantum electron transport phenomena in confined quasi-1D systems and QDs. Under the correct growth conditions these NWs can have an extremely good crystal quality with few defects and quasi-1D confinement is realized directly by the geometry of the NW crystal. Another benefit of freestanding NWs is the ease of depositing superconductor on semiconductor NWs in-situ, resulting in a clean semiconductor-superconductor interface. Numerous methods have also been developed for tailored shadow-masking of NWs during superconductor deposition to realize Josephson junctions or NS junctions without ex-situ post-processing which can degrade the transport properties of the resulting devices [73, 139, 163].

However, freestanding vertical NWs come with a serious downside - poor scalability. Fabrication of devices based on freestanding NWs will typically require to mechanically break and transfer the NWs from the growth substrate to a fabrication substrate with prepatterned marks for alignment of following lithography steps. While this is not unfeasible for small-scale fundamental research, it makes the integration of such NWs into industrial-scale foundry processes unimaginable. If NW growth from vertical trench walls could be realized, it would be possible to either develop methods to fabricate devices directly on the growth substrate or transfer the NWs in bulk using a stamping method similar to those used with graphene. Additionally shadow patterning similar to the oxide bridges described in [163] could be realized directly by tailoring the shape of the trench ends to shadow parts of the nanowires grown in the trenches.

In the VLS growth process InAs NWs readily nucleate on InAs (1 1 1)B (As-terminated) facets from Au catalyst droplets. The polarity of the substrate is important as the NW growth must match the polarity of the substrate and In and As adatoms have different diffu-

sion rates. Indium adatoms are less mobile than As adatoms thus they are more likely to nucleate a NW on an As-terminated substrate. In the case of an In-terminated substrate the As adatoms desorb to the vapour phase rapidly and NW nucleation rate is low. Aside from the obvious growth on standard epi-ready InAs (1 1 1)B substrates VLS NWs have previously been grown on angled facets realized by etching trenches with (1 1 1)B facets into (1 $\bar{1}$ 0) substrates [73, 86]. This enabled realization of shadowed Josephson junctions by having a NW grown from one of the trench walls shadow a NW grown form the other wall during deposition of superconductor [86]. Growing NWs from angled trench walls also allows merging NWs into crosses [73] and "hashtags" [164] for multiterminal devices. Taking this approach one step further, an attempt to improve the scalability of VLS NWs was made by trying to develop a method for in-plane growth of VLS NWs in trenches with vertical (1 1 1)B sidewalls.

The challenges associated with realising Au-catalysed NW growth on a vertical facet are producing vertical (1 1 1)B trench sidewalls and then depositing Au catalyst on a vertical surface. Trenches with vertical (1 1 1) facet sidewalls can be realized by etching into (2 1 1)B substrates yielding an A-polar (In-terminated) facet on one of the sidewalls and a B-polar (As-terminated) facet on the other. To achieve vertical sidewalls it is necessary to have an anisotropic etching method were the etch rate into the (2 1 1) substrate is much higher than the lateral etch rate. Wet etching methods are most commonly isotropic with no specific facet selectivity, however solutions with varying etch rates for different crystal directions are reported in literature. Etch recipes based on H_3PO_4 [163], HF [165], and HCl [166] were investigated and representative SEM micrographs of the results are shown in Fig. 7.1; the exact recipes and expected etch rates are listed in Appendix A.

Anisotropic InAs (2 1 1) Etching

Each of the attempted wet etch methods was found to be unsuitable for realizing trenches with vertical (1 1 1) facets in InAs (2 1 1)B substrates. A cross-section SEM micrograph of a circular patterned etched by the H_3PO_4-based solution is shown in Fig. 7.1a. The etch appears to be isotropic with similar etch rates downward and sideways and no preferred in-plane direction. Qualitatively the surfaces of the etched area also show high degrees of roughness unsuitable for catalyzed nucleation of VLS NWs. The etch rate matches the rate in literature at $\sim 1.5\,\mu$m/min and tweaking the ratios to reduce etch rate may improve surface roughness but due to the isotropic nature of the etch this was not pursued. For the HF-based etch solution, Fig. 7.1c shows a tilted SEM micrograph of a circular pattern etched into the InAs (1 1 1)B surface after 2 h of etching. The depth of the etch is $\sim 1.8\,\mu$m and the etch is isotropic and smooth, unsuitable for realizing facet-selective etching. The etch rate of ~ 15 nm/min for InAs is somewhat slower than reported in literature for GaAs (20 nm/min). Finally, Fig. 7.1 shows a tilted SEM micrograph of the InAs after 5 mins of etching with HCl-based etch. Bizzarely, the plateaus inidcated by the white arrows correspond to the square openings in the resist mask. The etch solution appears to run underneath the resist and etch faster under the resist. This behaviour was observed consistently for HCl-based etch solutions. Even though there appears to be some anisotropy to the etch, a suitable solution was not found.

For anisotropic etch profiles it is common to employ dry-etching procedures such as ICP RIE, as the ions are delivered to the substrate in a directional manner by the electromagnetic field the resulting etch is generally much more anisotropic than typical wet etch solutions. Through iterations of the ICP RIE process a recipe (see Appendix A) was developed that shows somewhat promising results in realizing

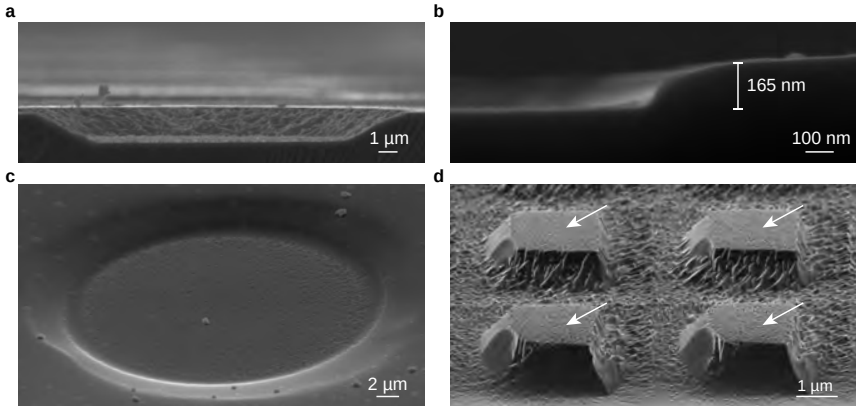


Figure 7.1: **a** SEM micrograph of InAs cross-section after 1 min of etching with H_3PO_4-based etch. Depth $\sim 1.5\,\mu$m **b** SEM micrograph of InAs cross-section after etching with ICP RIE. **c** SEM micrograph of InAs after 2 h of etching with HF-based etch. Depth $\sim 1.8\,\mu$m **d** tilted SEM micrograph of InAs after 5 mins of etching with HCl-based etch. Arrows indicate the defined mask openings.

vertical side walls. Figure 7.1b shows a cross-section SEM of a trench etched by ICP RIE, though the side walls are not fully vertical they are steeper than observed for the wet etch methods. However, a consistent problem encountered is that the ratio of the etch rate for the InAs and the resist mask used to define the etch region is not favourable for etching trenches that are deep enough for VLS growth on the sidewalls. For both PMMA and CSAR resists the ratio of etch rates between resist and InAs was $> 2:1$ making it impractical to use this approach for etching deep trenches.

A successful method to realize deep trenches with vertical sidewalls was found to be extensive Ar ion Kaufman milling. Compared to the ICP RIE the PMMA resist used to define the trenches was found to be much more resistant to Ar ion milling with an etch ra-

tio PMMA:InAs of 3:8. The full recipe is described in Appendix A2. Milling at a 45° incident angle along the $\langle 1\,\bar{1}\,0\rangle$ direction results in trenches with well-defined (2 1 1)B bottom and (1 1 1) sidewalls as can be seen in Fig. 7.2d-f. In each trench one of the (1 1 1) facets is A polar while the other is B polar depending on the rotation of the wafer. However, when milling the trenches the orientation of the wafer relative to the ion source is important. Fig. 7.2 shows the difference between milling parallel to the $(1\,\bar{1}\,0)$ facets and parallel to the (1 1 1) facets. When milling along the $(1\,\bar{1}\,0)$ facets the bottom of the trench does not form a smooth (2 1 1) facet but instead results in dense slanted "spikes" as shown in the SEM micrographs in Fig. 7.2a and b. The angle of the spikes does not match the milling angle but the angle of the (1 1 1) facets indicated by the dashed green lines in the simulated InAs crystal in Fig. 7.2c. Conversely, milling parallel to the (1 1 1) facets results in both a flat (2 1 1) trench bottom and smooth (1 1 1) trench walls as seen in in Fig. 7.2d and e.

Depositing Catalyst on Vertical Facets

While Au catalyst can be deposited on 45° facets using standard techniques, a new approach is needed for deposition on the 90° sidewalls. To deposit Au catalyst droplets on the vertical sidewalls of the trench a multi-layer resist stack of PMMA and PMMA co-polymer was used. Figure 7.3a shows a schematic representation of the resist stack. The wafer is first covered with a thick layer of PMMA co-polymer to fill up the trenches and a thin layer of PMMA is spun on top for defining the Au droplet positions. A cross-section SEM micrograph of the trench filled with resist can be seen in Fig. 7.3b, here thinner co-polymer was used the filling of the trench is expected to be more complete and closer to the schematic in Fig. 7.3a in further steps. Due to the mismatch in required exposure dose between the co-polymer and the PMMA the co-polymer is greatly overexposed when using a

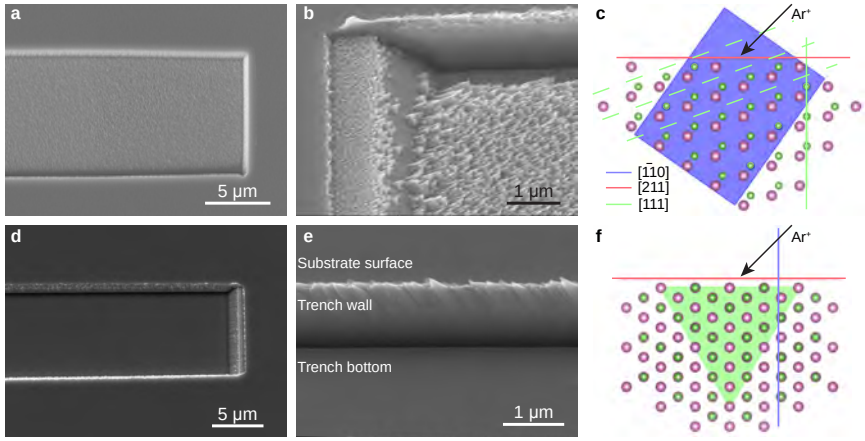


Figure 7.2: **a** Tilted SEM micrograph of trench in an InAs (2 1 1)B substrate, milling direction aligned along the $\langle 1\,1\,1 \rangle$ direction. The trench bottom is extremely rough. **b** Close-up tilted SEM micrograph of trench in a, the $(1\,\bar{1}\,0)$ facet is smooth, but faceted crystallites fill the trench bottom. **c** VESTA simulation of InAs crystal. Dashed green lines show possible (1 1 1) facets for the crystallites. **d** Tilted SEM micrograph of trench in an InAs (2 1 1)B substrate, milling direction aligned along the $\langle 1\,\bar{1}\,0 \rangle$ direction. The trench bottom is smooth. **e** Close-up tilted SEM micrograph of trench in d. The (1 1 1) facet of the trench wall and the (2 1 1) facet of the trench bottom is smooth aside from the corner between the substrate surface and the trench wall. **f** VESTA simulation of InAs crystal. The crystal is flat relative to the milling direction ensuring a flat (2 1 1) trench bottom.

dose sufficient for exposing dots in the PMMA and produces a large undercut. If the location of the electron beam spot is close enough to the trench sidewall, the undercut in the co-polymer is large enough to expose the (1 1 1) facet allowing to deposit Au at a 45° angle onto the vertical sidewall as shown in the schematic in Fig. 7.3c. Figure 7.3d and e show tilted SEM micrographs of Au catalyst droplets (gold) on the vertical trench sidewall, the colors in Fig. 7.3e are intended to help

the reader understand the perspective with the wafer surface in blue and the vertical sidewall in green, the gray area between is the rough corner between the substrate surface and the trench sidewall resulting from imperfect alignment during milling. The roughness visible on the side facet is resist and InAs residue due to insufficient substrate cleaning after resist stripping in this test sample and is not present in future samples where thorough oxygen ashing is used post milling to clean the substrate surface.

Growth Results

Once the Au catalyst droplets are deposited on the trench sidewalls the substrate is ready for MBE growth. Fig. 7.3 f shows a schematic of the desired result - VLS NWs growing horizontally from the vertical (1 1 1)B facet of the trench sidewall. Due to the presumption that the trench would inhibit the impinging material flux during MBE growth, the growth parameters were altered from standard MBE VLS InAs NW growth by increasing growth time and the material flux.

The result of the MBE growth can be seen in the cross-section SEM micrographs in Fig. 7.3 g and h. Unfortunately, the trenches appear to trap incoming material and the surface roughness caused by the milling serves as nucleation sites for self-catalysed parasitic NW growth. Incoming material is trapped by the trenches resulting in the growth of a forest of random, irregular, and extremely long self-catalysed NWs as seen in Fig. 7.3g.

The growth conditions are also promoting significant undesirable substrate surface growth. Fig. 7.3h shows the trench cross-section after growth, extensive formation of (1 1 1)B facets in the trenches and on the substrate surface occurs to cover up the (1 1 1)A and (2 1 1)B facets with energetically favourable (1 1 1)B facets. A possible Au-catalysed intentional NW in Fig. 7.3h is highlighted in green but this is inconclusive and the overall growth conditions are not suitable for

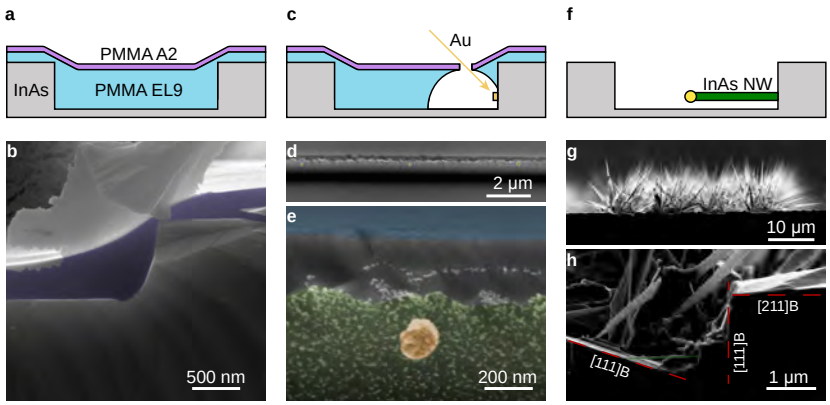


Figure 7.3: **a** Schematic of resist stack. The trenched InAs substrate is covered by two layers of PMMA EL6 and one layer of PMMA A2. **b** SEM micrograph of a cross-section of the InAs substrate cleaved across a trench filled with two layers of EL6 and a layer of A2. The purple area shows the PMMA coverage, the PMMA is covered with Au to reduce sample charging. **c** Schematic of the resist stack after exposure and development and the deposition of Au on the vertical facet. Au is deposited at a 45° angle. **d** SEM micrograph of multiple Au catalyst droplets on the vertical facet of the trench. **e** Close-up SEM micrograph of an Au catalyst droplet (gold) on the vertical facet (green) of the trench. Substrate surface in blue, rough transition edge in gray. **f** Schematic of expected end result with an horizontal InAs NW grown from the vertical trench facet. **g** SEM of a cross-section of the substrate after MBE growth. Due to sub-optimal growth conditions and material accumulation sites the trenches are filled with self-catalysed NWs growing in poorly defined directions. **h** Close-up SEM of a cross-section of a trench after MBE growth. Another (1 1 1)B facet has been reformed in place of the (2 1 1)B and (1 1 1)A facets in the trench. A possible catalyst-defined NW can be seen (green).

selective NW growth.

The concept of VLS NWs growing in trenches from vertical facets

is likely realisable by optimising growth conditions. An ALD AlOx layer can be grown on the entire substrate after milling the trenches and selectively removed using HF prior to Au deposition to prevent substrate growth and nucleation of parasitic self-catalyzed NWs. However, even if the NW growth is realized there are still challenges to surmount to make the platform scalable and useful for nanoelectronics. The growth substrate is conducting so it would still be necessary to either transfer the NWs onto another substrate for device fabrication via e.g. a stamp or to cover the growth substrate with dielectric and fabricate devices directly. While the concept is interesting and there are possibilities for NW shadowing by tailoring the trench shape and depositing e.g. superconductor at an angle, it cannot surpass existing materials platforms such as SAG and 2DEGs in terms of scalability.

8 Conclusions and Outlook

The results presented show SAG NWs as an attractive platform for scalable bottom-up on-chip electronic circuits. Pre-growth definition of NW positions enables fabrication of circuits covering large areas and implementing thousands of individual NWs. In Section 4.2 It has been shown that NWFETs based on single or multiple InAs SAG NWs can be reliably fabricated and exhibit reproducible electron transport parameters. This enables the creation of large-scale on-chip circuits such as the multiplexer-demultiplexer circuit presented in Section 4 which was used to semi-automatically characterize a large number of individual NW devices in a single cooldown. The measurements of 256 nominally identical NWFET devices shown in Section 5.2 show the variability of electron transport parameters such as V_{TH}, ΔV_{TH}, and μ_{FE} with statistical significance.

An ensemble of QD devices presented in Section 5.4 was fabricated using shared cross-bar topgates to define and tune the QDs and gate-defined QDs were induced in 20 SAG NWs. Quantum dot couplings were investigated in a range of barrier gate potentials and it was shown that configurations of barrier gate potentials exist where all 20 devices are in the Coulomb blockade regime. Questions remain about using shared cross-bar gates to reliably tune an ensemble of SAG QDs to the last electron due to the disorder potential. The multiplexer circuit would be an invaluable tool for further research into the potential variations along a single NW and across NW arrays.

The results presented establish a method for large-scale characterization which can be used for further optimising reproducibility of SAG quantum devices and systematically establishing the relationship between growth design and device performance. Such a method could be used to benchmark a system, establishing the tolerance of the components to avoid characterizing every individual device in a

circuit.

Going further, an aspect that has not been explored here is the possibility of growing branched NW structures and networks. Here only two-terminal devices were investigated but it is possible to adjust the design to realize multiterminal devices on single NWs or branched NW networks. Alternatively, the multiplexer circuit could be used to control a large number of electrostatic gates. By individual control of each multiplexer level it would also possible in such a system to address multiple gates at the multiplexer outputs at the same time. Such a circuit could be used for e.g. charge shuttling experiments [167].

Furthermore, SAG NWs are easily contacted by superconductors and thus well suited for hybrid quantum devices [93], and bulk device characterization may allow to hunt for rare and elusive phenomena. Additionally, the multiplexer itself can be fabricated using superconductor leads, replacing the NWFETs with Josephson junctions and used to realize and control a large number of flux-lines.

Overall, SAG nanowires can be readily integrated into on-chip circuitry without significantly complicating the fabrication process. Such circuits then allow for scaling up the number of devices available at cryogenic temperatures without the need to add additional transmission lines to the cryostat and enables automation of measurements. Important steps have been made to utilize the potential of SAG NWs and set a course for scaling up quantum device circuits.

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Appendix A Fabrication Recipes

A1 InAs (2 1 1)B etching

A1.1 Phosphoric Acid Etch

Etch solution [163]:

- 20 ml H_2O
- 7.5 g citric acid $HOC(CO_2H)(CH_2CO_2H)_2$
- 10 ml 85% H_3PO_4
- 6 ml 30% H_2O_2

Expected etch rate: 1.5 μm/min

A1.2 Hydrofluoric Acid Etch

Etch solution [165]:

- 30 ml H_2O
- 3 ml 1% HF
- 0.1 ml 30% H_2O_2

Expected etch rate: 20 nm/min

A1.3 Hydrochloric Acid Etch

Etch solution [166]:

- 20 ml H_2O
- 7.5 g citric acid $HOC(CO_2H)(CH_2CO_2H)_2$
- 2 ml 30% H_2O_2

- 1 ml 40% HCl

Expected etch rate: 300 nm/min

A1.4 ICP RIE etch

Gasses:

- 7.5 sccm BCl_3
- 2.5 sccm Cl_2
- 5 sccm Ar

Process parameters:

- Temperature: $20°C$
- Pressure: 4 mTorr
- ICP power: 600 W
- RF power: 20 W
- Time: 1 min

A2 Vertical Sidewall Trenches and Catalyst Deposition

A step-by-step recipe for realizing $\sim 1\,\mu$m deep trenches with vertical (1 1 1) side facets on a (2 1 1)B InAs substrate and subsequently depositing Au catalyst droplets in lithographically defined positions on the vertical facets.

1. Resist mask for trenches
   - 1.1 Spin coat PMMA A6 at 4000 RPM for 60 s
   - 1.2 Bake at 185 °C hotplate for 60 s
   - 1.3 Repeat steps 1.1 and 1.2 for second layer
   - 1.4 Approximate resist thickness: 1 µm
2. Exposure of trenches
   - Acceleration voltage: 125 kV
   - Beam current: 40 nA
   - Aperture: 240 µm
   - Spot size: 48 nm
   - Step size: 50 nm
   - Area dose: 800 µC/cm^2
3. Developing trenches
   - 3.1 MIBK:IPA 1:3 60 s
   - 3.2 IPA 30 s
   - 3.3 N_2 blow-dry
   - 3.4 Oxygen plasma ash 4 mins
   - 3.5 MIBK:IPS 1:3 30 s

3.6 IPA 30 s

3.7 N_2 blow-dry

4. Mill trenches

4.1 Voltage: 600 V

4.2 Ar flow: 15 sccm

4.3 pressure: 1 mTorr

4.4 Sample tilted 45° relative to incident ions, aligned with the $\langle 1\,\bar{1}\,0 \rangle$ direction

4.5 Mill 8 mins

4.6 Let system cool down with Ar flow but no plasma for 8 mins

4.7 Change sample tilt to -45°

4.8 Repeat steps 5, 6, 7 twice more

4.9 Expected trench depth: 1 µm

5. Strip resist

5.1 50 °C acetone + sonication 30 mins

5.2 RT acetone overnight

5.3 Oxygen plasma ash 60 s

6. AlOx deposition

- Temperature: 180 °c
- Cycles: 150
- Expected oxide thickness: 15 nm

7. Resist mask for catalyst droplets

7.1 Spin coat PMMA EL9 at 4000 RPM for 45 s

7.2 Bake at 185 °C hotplate for 60 s

7.3 repeat steps 7.1 and 7.2

7.4 Spin coat PMMA A2 at 4000 RPM for 45 s

7.5 Bake at 185 °C hotplate for 60 s

8. Exposure of droplet positions

   - Acceleration voltage: 100 kV
   - Beam current: 500 pA
   - Step size: 5 nm
   - dot dose time: 300 µs/dot

9. Developing trenches

   9.1 MIBK:IPA 1:3 60 s

   9.2 IPA 30 s

   9.3 N_2 blow-dry

   9.4 Oxygen plasma ash 60 s

10. AlOx etch and InAs native oxide removal

    10.1 Buffered HF 20s

    10.2 H_2O 30 s

    10.3 transfer to second H_2O beaker 60 s

11. Au catalyst deposition

    - Sample tilted 45° relative to Au crucible
    - Evaporate 20 nm of Au at a rate of approximately 2 Å/s

12. Strip resist

    12.1 50 °C acetone. Agitate with pipette until most of visible Au/PMMA is rmeoved

12.2 Transfer to another 50 °C acetone beaker, leave overnight

12.3 IPA 30 s

12.4 N_2 blow-dry

12.5 Oxygen plasma ash 60 s

A3 Multiplexer fabrication

The multiplexer devices are fabricated using mostly standard semiconductor fabrication procedures and can be fabricated in parallel with the desired test devices. Due to the physical scale and the interconnected nature of the multiplexer circuit it is more important than usual for academic research to ensure high cleanness of the sample as stray particles can cause broken connections. On a positive side, as SAG is grown directly on the device substrate, sonication can be used much more liberally than with e.g. VLS NW devices which have the risk of delaminating from the device substrate.

1. NWs: SAG InAs on GaAs [3 1 1]
2. Resist mask for ohmic contacts
    2.1 Inspect sample in dark-field optical microscope. Clean in IPA if dust particles present in circuit area.
    2.2 Spin coat PMMA A4 at 4000 RPM for 60 s
    2.3 Bake at 185 °C for 1 min (hotplate) covered to protect from dust
3. EBL exposure of ohmic contacts and leads
    - N_2 blow the sample to remove any dust after mounting
    - Acceleration voltage: 125 kV
    - Beam current: 1 nA
    - Beam spot size 2.2 nm
    - Beam step size: 2.5 nm
    - Area dose: 630 µC/cm^2

4. EBL exposure of bondpads
    - Acceleration voltage: 125 kV
    - Beam current: 20 nA
    - Beam spot size 22.4 nm
    - Beam step size: 20 nm
    - Area dose: 630 µC/cm^2
5. Develop mask
    5.1 MIBK:IPA 1:3 90 s
    5.2 IPA 30 s
    5.3 N_2 blow-dry
    5.4 Oxygen plasma ash 60 s
6. Deposit ohmic contacts and bondpads using e-beam evaporation
    6.1 Ar ion RF milling at 15 W 18 mTorr for 2 mins to remove native oxide
    6.2 Deposit 5 nm of Ti at a rate of 1 Å/s
    6.3 Deposit 150 nm of Au at a rate of 2 Å/s
7. Strip resist
    7.1 50 °C acetone for 1 h
    7.2 Sonicate in 50 °C acetone at 37 kHz for 5 mins
    7.3 Sonicate in 50 °C acetone at 80 kHz for 2 mins
    7.4 IPA 30 s
    7.5 N_2 blow-dry
    7.6 Inspect in optical microscope. Repeat steps 7.2-7.5 if any parts of the mask hasn't lifted off.

7.7 Oxygen plasma ash for 2 mins

8. Deposit ALD gate dielectric HfO_2
   - Pump on chamber for 10 h
   - Temperature: 110 °C
   - 150 cycles (Expected thickness: 15 nm)
9. Resist mask for gates. Same as step 2
10. Exposure of gate leads and bondpands. Same as steps 3 and 4 respectively
11. Develop mask. Same as step 5
12. Deposit gate electrodes
    12.1 Deposit 5 nm of Ti at a rate of 1 Å/s
    12.2 Deposit 150 nm of Au at a rate of 2 Å/s
13. Strip resist
    13.1 50 °C acetone for 1 h
    13.2 Sonicate in 50 °C acetone at 37 kHz for 30 s
    13.3 Sonicate in 50 °C acetone at 80 kHz for 30 s
    13.4 IPA 30 s
    13.5 N_2 blow-dry
    13.6 Inspect in optical microscope. Repeat steps 13.2-13.5 if any parts of the mask hasn't lifted off.
    13.7 Oxygen plasma ash for 2 mins

Appendix B Extended Data

B1 Full Dataset of NWFET Devices

Figure B.1 Shows the full data set of the measurements shown in Fig. 5.3 consisting of pinch-off curves for 256 lithographically identical NWFET devices. The devices used are the NWFETs in the last level (closest to DUT) of the source multiplexer shown in Section 4 Fig. 4.9 which contain a single NW per transistor. During the measurement the gates of the devices in the DUT area are set to +2 V and the gates of the last level FETs are operated independently in the source and drain multiplexer.

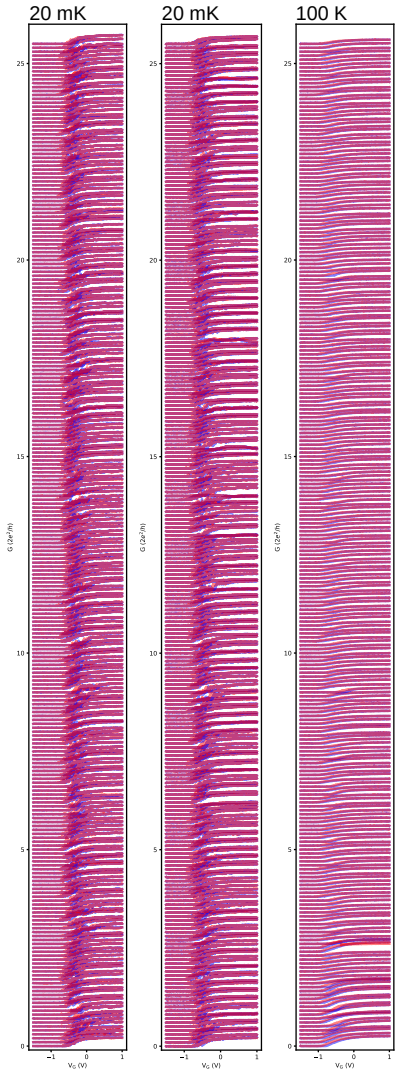

Figure B.1: Raw data of pinch-off curves of 256 lithographically identical transistor devices, traces offset in conductance for clarity. Two rounds of measurements at 20 mK in two separate cooldowns and a set of measurements at 100 K. Gate voltage swept from negative (positive) to positive (negative) in red (blue).

B2 Full Dataset of Length Dependence Devices

Figure B.2 shows the full data set of conductance G as a function of V_{G} used for the analysis discussed in Section 6.1. Gate voltage V_{G} is swept from positive to negative (blue) and negative to positive (red), each trace is offset from the previous in G by e^2/h for clarity. Semiconductor segment length decreases from bottom to top.

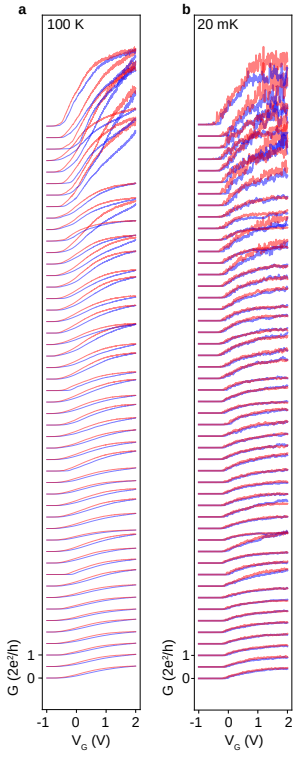

Figure B.2: **a (b)**Full dataset of $G(V_{\mathrm{G}})$ with $T = 100\,\mathrm{K}$ ($T = 20\,\mathrm{mK}$) for the NWFET analysis discussed in Section 6.1. Traces offset in G by e^2/h for clarity.

B3 Additional Correlation Between NWFET Parameters

Figure B.3 shows additional correlations between electron transport parameters of the NWFET devices. Correlations between the parameters at 100 K and the parameters after the second cooldown to 20 mK (Fig. B.3a, e) are similar to the correlations of the first cooldown shown in Section 5.2 Fig. 5.4. There is weak correlation between V_{TH} and ΔV_{TH} (Fig. B.3b-d) and also between V_{TH} and μ_{FE} (Fig. B.3f-h) which may be due to the charge trap potential affecting the two parameters similarly.

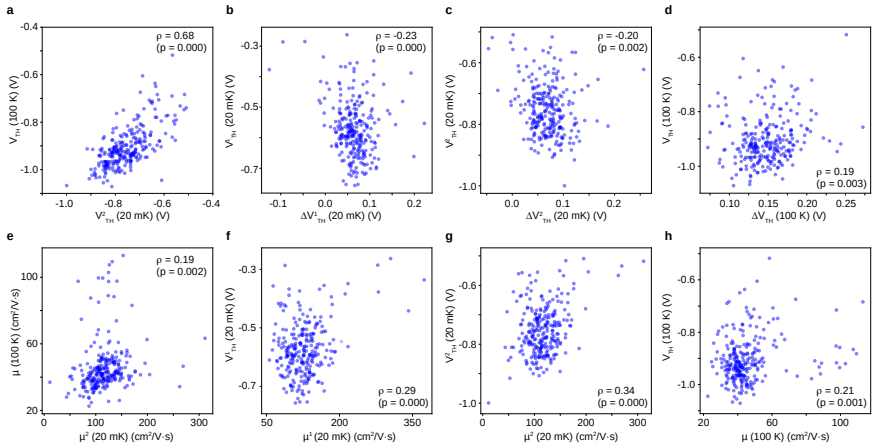

Figure B.3: **a** correlation between threshold voltage at 20 mK (second cooldown) and 100 K. **b-d** correlation between hysteresis and threshold voltage for 20 mK (coolodwn 1 and cooldown 2) and 100 K. **e** correlation between mobility at 20 mK (second cooldown) and at 100 K. **f-h** correlation between mobility and threshold voltage for 20 mK (coolodwn 1 and cooldown 2) and 100 K.

B4 Source-drain Bias Spectroscopy on Other QD Devices

Figure B.4a-s shows the source-drain bias spectra of the remaining 19 devices used for the QD analysis in Section 5.4. All bias spectra were taken sequentially at the same barrier gate configuration and the same V_{SD} and V_{M} range using an automated measurement. The barrier gates were trained by sweeping up and down prior to the source-drain bias measurement after switching to a new device to stabilize the electrostatic environment.

Qualitatively all 20 devices show Coulomb blockade-like features although for some devices either the QD is poorly defined due to a sub-optimal barrier gate configuration or the DC bias range is too large to accurately resolve the Coulomb diamond height.

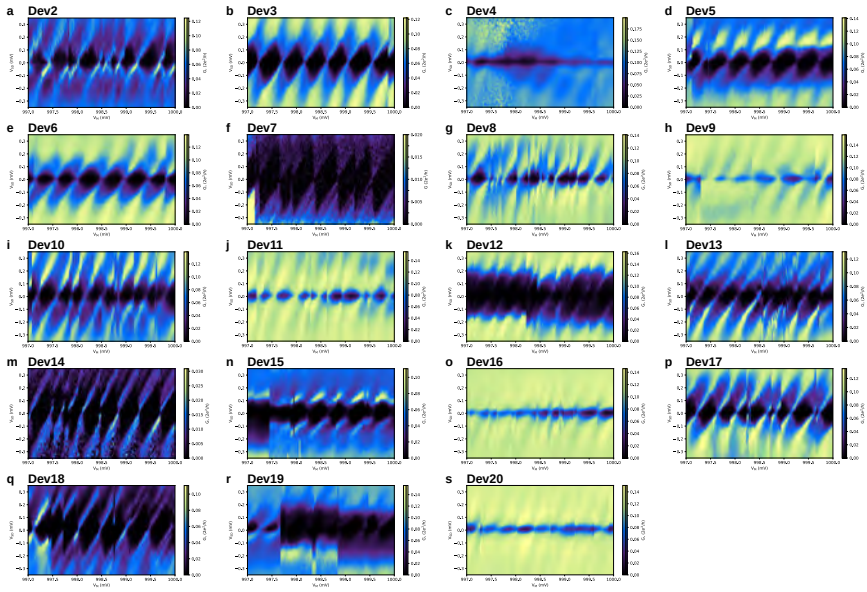

Figure B.4: **a-s** Source-drain bias spectroscopy of Dev2 to Dev20 used for the QD analysis in Section 5.4.

The height and width of each full and well-defined Coulomb diamond was manually measured to extract the mean charging energy $\langle E_\mathrm{C} \rangle$ and mean Coulomb peak spacing $\langle V_\mathrm{M} \rangle$ as well as the mean lever-arm $\langle \alpha \rangle = \frac{\langle V_\mathrm{M} \rangle}{\langle E_\mathrm{C} \rangle}$ for each device.

Dansk Abstrakt

Denne afhandling undersøger on-chip multiplexerkredsløb baseret på selective area growth nanotråde som et middel til at udvide målestokken for målinger ved kryogene temperaturer. Selvom skaleringen af kvantelektronikplatforme og kredsløb er et almindeligt diskuteret aspekt, er en begrænsende faktor for enhver materialeplatform antallet af transmissionslinjer i kryogene måleopsætninger, som igen er begrænset af den tilgængelige køleeffekt. Multiplexerkredsløb overvinder denne begrænsning ved at bruge kontrolledninger til at adressere et eksponentielt antal udgange. Her præsenteres drift og fejltolerance af sådanne kredsløb. Kredsløbene bruges derefter til at undersøge variabiliteten af nominelt identiske transistorer baseret på selective area growth nanotråde med statistisk signifikans og reproducerbarheden af gate-definerede kvanteprik parametre på tværs af nanotråde. Derudover bruges kredsløbene til at studere effekten af systematiske variationer i nanotrådegeometri og -struktur på elektrontransportegenskaberne.

De præsenterede metoder udvider værktøjskassen til at optimere selective area growth baseret på elektrontransportfeedback, giver en mulig retning for at skalerere kryogene kredsløb og etablerer en proces til benchmarking af et system. Målingerne udnytter skalerbarheden og alsidigheden af selective area growth nanotråde og vidner om platformens egnethed til skalerbar kvantelektronik.