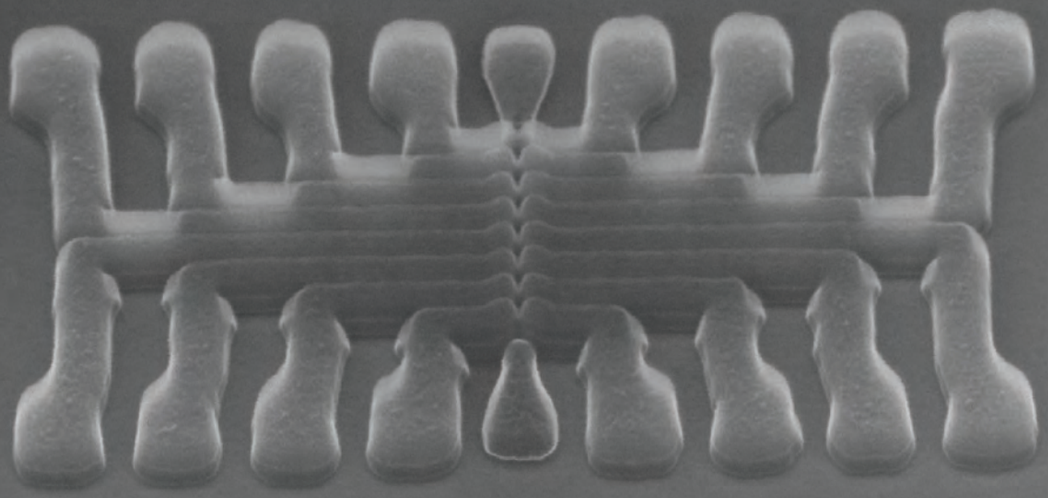

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Single-electron control in one- and two-dimensional arrays of quantum dots in silicon

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Single-electron control in one- and two-dimensional arrays of silicon quantum dots

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Abstract

The recent demonstration of computational speedup achieved by a noisy intermediate-scale quantum circuit, compared to a classical supercomputer, has accelerated even more the pursuit for the implementation of a universal quantum computer. The results achieved by the quantum hardware and algorithm communities have moved the industry-academia alliance one step closer to quantum computing's "Hello World" era.

Among the viable systems for the physical implementation of a quantum computer, silicon spin qubits are at the forefront of quantum research today, partly due to their exceedingly long coherence times and a reduced on-chip footprint. Furthermore, massive parallel fabrication of spin qubit hardware in CMOS foundries shows the potential for large-scale production.

In this thesis, I analyse and compare two different silicon spin qubit platforms; one is university-fabricated while the other is based on quantum dots produced in a CMOS foundry. I study their behavior in the few-electron regime using advanced radio-frequency techniques, enabling fast charge sensing and gate-based dispersive readout, the latter being a strong candidate for achieving compact readout and wiring of a large-scale quantum computer.

Using the university-fabricated device, I show the ability to read out the single-electron spin configuration in 24 µs, a fundamental requirement for the implementation of a spin qubit. Nevertheless, the reproducibility of these devices is low and their fabrication is complicated for a typical academic cleanroom.

Motivated by the recent demonstration of a CMOS spin qubit, I then analyse the performance of a foundry fabricated two-dimensional array of CMOS quantum dots. Developing a hybrid dispersive charge-sensing technique, I demonstrate for these devices all the major functionalities of state-of-the-art university fabricated quantum dot devices. By harnessing the two-dimensionality of the system I report in the time domain deterministic single-electron movement and charge swaps within the array.

Contents

List of publications

1. C. Volk, A. Chatterjee, **F. Ansaloni**, C. M. Marcus and F. Kuemmeth, Fast charge sensing of Si/SiGe quantum dots via a high-frequency accumulation gate, *Nano Lett.* **19**, 5628 (2019).

2. **F. Ansaloni***, A. Chatterjee*, H. Bohuslavskyi, L. Hutin, M. Vinet and F. Kuemmeth, Single-electron control in a two-dimensional CMOS quantum dot array, *in preparation.*

3. H. Bohuslavskyi*, **F. Ansaloni***, A. Chatterjee, F. Fedele, J. Li, B. Venitucci, Y.M. Niquet, L. Hutin, M. Vinet and F. Kuemmeth, Charge and dispersive sensing of tunable quantum dots in a CMOS silicon nanowire transistor, *in preparation.*

4. A. Chatterjee*, **F. Ansaloni***, F. Fedele, H. Bohuslavskyi, L. Hutin, M. Vinet and F. Kuemmeth, Digital detection of high-dimensional Coulomb diamonds, *in preparation.*

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1

Background and Motivation

The 21st century is witnessing an unprecedented technological development. Over the past two decades, the requirement for more powerful and faster computers has been exponentially increasing. However, Moore's law, describing the biennial doubling of the number of field effect transistors (FET) in integrated circuits, has reached a saturation plateau. In fact, as transistors are shrunk to increasingly smaller dimensions, now approaching the 3nm node [1], the rise of quantum phenomena becomes inevitable, making classical transistor devices not suitable for classical computation anymore. On the other hand, the capabilities of classical computers are not able to solve certain problems in a reasonable computational time, as prime number factorization [2] and complex simulations. In order to address these limitations using unconventional approaches, two different computational architectures are nowadays investigated

by foundries as well as research laboratories: *Neuromorphic computation* [3] and *Quantum computation* [4, 5]. Neuromorphic computation exploits classical transistors (i.e. classical bits) to mimic neuro-biological architectures present in the nervous system, introduced by Mead in the 1990s [3]. On the other hand, quantum computation disrupts the paradigm of classical computation, introducing a new unit of information: the quantum bit or qubit. Qubits are quantum mechanical entities with no classical counterpart, requiring the employment of "quantum transistors". Quantum computation using quantum machines was firstly theoretically investigated by Benioff and Feynman in the early 1980s [4, 5]. The extremely improved performance of quantum computers stems from the exploitation of quantum parallelism and entanglement between quantum bits, two quantum mechanical properties that have no classical analogue [6].

FETs encode classical bits as two-level systems, where the two states "0" and "1" can be seen as either the presence or the absence of an electronic current flowing through the transistor. The information is encoded in a quantum-mechanical two-level system, where additionally to the states "0" and "1" , the "quantum transistor" can also be in a superposition of these two states. In order to identify a suitable platform, five criteria that were introduced by DiVincenzo in 2000 [7] have to be met and are going to be presented in the next section. Since the development of the idea of a universal quantum computer, scientists have identified a wide range of "quantum transistors", ranging from semiconducting quantum dots [8], single donor atoms in semiconductors [9], Josephson junctions embedded in superconducting circuits [10], trapped isolated ions [11], photons [12], topological states [13] and many more.

With such new capabilities, quantum computers will be able to solve a variety of problems that nowadays seem to be impossible to solve in a lifetime, even with the most powerful supercomputer in the world. Some examples are related to the field of physics, as the exact resolution of quantum systems using quantum simulators [5]. More generally, universal quantum computers are expected to be necessary to solve problems in many scientific fields, ranging from chemistry [14] to computer science [15]. Recently, a superconducting circuit

processor implementing 53 qubits, has showed the capability to outperform a classical supercomputer [16].
The work presented in this thesis investigates the properties of seminconducting quantum dot devices in group IV materials as "quantum transistors" for qubit implementations. The thesis focuses on the comparison between quantum dot devices fabricated in university cleanrooms and semiconducting foundries, highlighting strengths and limitations of both platforms for the implementation of a quantum dot universal quantum computer.

1.1 A scalable spin-qubit quantum computer

Quantum dots in semiconducting materials are one of the many platforms for the implementation of qubits. As discussed in the next chapter, quantum dots are nano-sized devices able to trap and hold a single-electron charge, by means of electrostatic fields generated via metallic electrodes. As a single electron is trapped in these devices, either the presence or the absence of the electronic charge can be used as a quantum two-level system, yielding a charge qubit [17]. Differently from state-of-the-art classical bits, quantum bits are highly susceptible to environmental noise. For example, due to their charge nature, charge qubits couple strongly to the electrical noise coming from the gate electrodes, leading to a lifetime of the quantum state of the order of hundreds of picoseconds [17]. By operating these qubits at sweet spots, where the qubits are less sensitive to electrical gate noise, coherence times have been extended to a few nanoseconds [18], and recent development showed the capability to reach tens of nanoseconds [19]. However, these time scales are not enough to implement long computational sequences. As a consequence, scientists had to come up with smart ideas to encode the quantum information into degrees of freedom that weakly interact with the environment. This would enable an intrinsic protection against the loss of coherence, such that the information could be stored for a time long enough to enable the computation. For single electron trapped in quantum dots, this has been achieved by encoding the information in the spin degree of freedom, a quantity that only couples to magnetic noise,

and not directly to electrical noise. This has led to the development of spin qubits [8, 9], where the quantum information can be stored up to seconds, placing spin qubits among the most suitable candidates for the development of a universal quantum computer. However, the "quiet" nature of spins, which protects spin qubits from environmental decoherence, is simultaneously hiding them from the user's control and readout. This has required the development of new techniques to enable spin-qubit control and manipulation, where the spin state is accessed via electrostatic manipulation, as discussed in section 2.2.

1.1.1 DiVincenzo criteria

Quantum two-level systems have to meet five criteria in order to be employed as qubit platforms. These criteria were introduced in 2000 by David DiVincenzo and they are known as DiVincenzo's criteria. Spin qubits satisfy each of the following requirements, as discussed in section 2.2.

- **A scalable physical system with well characterized qubits:** the Hamiltonian of the physical system that encodes the qubits has to be fully known. This means that the coupling parameters of the qubit processor to the environment as well as in between qubits have to be known. In a fully scaled quantum computer, the lack of such knowledge would appear as errors in the computation process. The higher is the knowledge of the coupling strengths, the more reduced is the possibility of computational errors. As the computational error is made small enough, it can be corrected using quantum error correction algorithms [20].

- **Initialization to a fiducial state:** it is essential that a quantum bit is initialized to a fiducial state with the highest fidelity possible (ideally 100%). If the fidelity of the initialization is too low, we would not benefit from the speed-up offered by a quantum computer. Due to the importance of this parameter, the community has defined the quantity T_1 as the time required for a qubit to naturally relax from its excited state to the fiducial initial state.

- **Long coherence time:** the preservation of the qubit quantum state has to be long compared to other time scales, for example the time required to compute one qubit gate. This parameter, also known as intrinsic coherence time, and identified as T_2^* , represents the time over which the quantum nature of the state is reduced by 1/e. The scale of the coherence time is set by the nature of the qubit itself and its coupling to external sources of noise.
- **Sets of universal quantum gates:** in order to manipulate qubits to perform the computation, it is necessary to implement operations that change the state of the qubit, usually achieved by unitary transformations. A complete set of quantum gates represent a finite set of transformations which can be used to reproduce any change in the qubit state. An example of a universal set of quantum gates is offered by single-qubit rotations plus the controlled-NOT two-qubit gate.
- **Readout capability:** As the computation step is concluded, the final quantum state has to be read out with a high fidelity. This defines the quantum efficiency of the computation. In order to achieve high fidelity readout, increasing the quantum efficiency, repetition codes can be used.

1.1.2 Silicon spin qubits

Since the beginning of this century, semiconducting platforms including III-V compounds (GaAs [21] and InAs [22]) or group IV materials (Si [23] and Ge [24]) have been identified as suitable candidates to host spin qubits. In particular, initial efforts focused on GaAs/AlGaAs heterostructures, owing the high quality of the material and its amenability to nanofabrication. Scientists have shown the capability of performing single [25] and two-qubit [26] gates in this platform as well as all the other ingredients required to implement a universal quantum computer. However, despite the exciting results achieved, GaAs suffers from the presence of fluctuating spinful nuclei in the atomic lattice, which couple via the hyperfine interaction with the single spins, leading to fast decoherence times (tens of nanoseconds). In order to obtain better spin

qubits different solutions are possible, such as the implementation of refocusing pulse sequences (a technique borrowed from the nuclear magnetic resonance community) able to extend the coherence time of about five orders of magnitude [27] or moving to group IV materials.
Silicon and germanium heterostructures are nowadays the leading platforms for the implementation of spin qubits. Light-hole carriers in germanium are predicted to weakly couple to the nuclear spin bath, which has recently enabled the demonstration of long coherence times of the order of hundreds of nanoseconds for nanowire structures [28] as well as two-dimensional heterostructures [24, 29]. On the other hand, naturally abundant silicon is composed by three isotopes: Si^{28}, Si^{29} and Si^{30}. Amongst them, Si^{28} and Si^{30} represent the 95% of the total nuclei isotopes and have a spin zero. Therefore, only 5% of silicon nuclei in the crystal lattice (with a spin 1/2) interact with the electronic spins. This makes silicon an attractive environment for the implementation of spin qubits, where coherence times have been shown to last for microseconds [23]. Furthermore, using isotopic enrichment, spinful Si^{29} nuclei are reduced down to a few parts per billion, such that an almost perfect semiconducting spin vacuum can be achieved, extending the coherence times up to half a minute [30], setting the record for condensed matter qubits. Recent developments in silicon-based spin qubits have led to the demonstration of 99.9% fidelity single-qubit gates [31], approaching the limit for the implementation of quantum error correction algorithms, two-qubit gates [32–34] as well as the first implementation of the Deutsch-Josza and the Grover search algorithms [35].
However, the fabrication of silicon devices has proven not to be as reliable as for GaAs devices, a pressing bottleneck for research groups. In fact, due to the strain arising at the interface between metallic leads and the material, unwanted quantum dots are usually formed in the nanodevices, reducing the control over the coupling terms and reproducibility of silicon quantum dots and spin qubits. Recently, two reliable solutions have become available, improving the quality of silicon devices. Relying on university cleanrooms, research groups have developed fabrication processes where design rules for quantum dots have become more demanding, for example reducing the gate pitch in

between quantum dots. One of the idea behind this approach is to aim at the full electrostatic control of the semiconducting region where the quantum hardware is hosted [36, 37]. This has enabled the formation of reproducible quantum dot features across many devices over the last five years. Simultaneously, silicon foundries have also started pursuing the fabrication of silicon quantum dot devices, using fabrication flows similar to those developed for FET transistors. Silicon foundries have shown the ability to form increasingly smaller, more controllable and more reproducible quantum dot devices over the past decade. This development culminated with the demonstration of the first spin qubit in a foundry device in 2016 [38].
The implementation of progressively smaller quantum dots has recently enabled the demonstration of qubit operation above 1K [39, 40]. If high fidelity qubit operations were demonstrated above 1.5 K, the requirement of He^3 for quantum computer cooling units would not be necessary anymore, massively reducing the costs of a physical quantum computer.

Semiconductor foundries

As introduced in the beginning of this chapter, further shrinking of FET devices dimensions in order to keep up with the prediction of Moore's law, is becoming harder. In fact, as the FET gate length approaches few nanometers, quantum effects become non-negligible in these devices. This would be highly detrimental for storing classical information, due to the probabilistic nature of quantum mechanics. However, these phenomena can be harnessed for the implementation of semiconducting spin-qubit devices [38, 41–43]. Semiconductor foundries have been developing silicon technology for few decades, reaching a remarkable high-quality silicon fabrication in ultra-clean environments. Furthermore, the production of silicon quantum dots has been demonstrated on 300 mm technology, moving the production of these devices one step closer to mass production. Eventually, it would be easier for foundries to fabricate spin-qubit quantum circuits with integrated classical electronics for qubit control, manipulation and readout.

1.2 Quantum dot arrays

Spin qubits have come a long way since their first implementation in the beginning of this century. Despite all the single ingredients for the implementation of a scalable quantum computer have been demonstrated, this platform intrinsically lacks elements for mid- and long-range qubits interaction, due to the locality of quantum dot devices. On one hand, circuit quantum electrodynamic (cQED) elements can be used to couple spin qubits over millimeters distances. Superconducting coplanar waveguide resonators have been recently implemented to show the coupling of microwave photons to a single-electron spin [44, 45], as well as the coupling between either two electronic charges [46] or spins [47] placed millimeters apart. However, light and spin are not directly interacting, therefore in order to achieve a strong coupling regime it is necessary to operate the qubits in a hybrid regime, where a spin qubit acquires a charge-like character in order to interact with the photon. Such a hybrid qubit could couple more easily to environmental noise.
On the other hand, many research groups have started exploring the properties of arrays of quantum dots. Ideally, a long chain of quantum dots could be used to quickly move the quantum information over mid- and long-range distances by quickly coherently shuttling spins across the quantum dots. Theoretical proposal exist that utilize bucket-brigade spin shuttling to enable quantum state coherent transfer (CTAP) [48, 49]. Bucket-brigade electron transfer has been achieved in a one-dimensional linear chain of quantum dots both in GaAs [50] and Si [51].
Since the implementation of the first quantum dots, research groups have been developing increasingly longer one-dimensional arrays, moving from a single quantum dot [52], all the way to an array of nine quantum dots [53]. The exploration of the second dimension has been limited to triple quantum dots arranged in triangular lattices, used to explored the physics of spin-frustrated systems [54]. The reduced exploration of two-dimensional arrays can in part be attributed to the readout techniques that have been implemented to achieve high-fidelity readout in the few-electrons regime. This technique, known as

charge sensing, is discussed in more details in section 3.3.1. Charge sensing requires the presence of a highly sensitive charge meter (usually a second quantum dot) placed in close proximity with the quantum dot used to encode the qubit, therefore physically occupying the second dimension [51, 55]. Only recently two-dimensional arrays of quantum dots have been implemented in GaAs, where a 2x2 array with nearest neighbour tunnel coupling [56] has been used as a quantum simulator to study Nagaoka ferromagnetism, a ferromagnetic phase predicted in the 1960s [57]. Similarly, the spin properties of a 3x3 array of quantum dots in GaAs have been studied, investigating its suitability for spin-qubit applications [58]. Regarding group IV materials, the reconfigurable occupation of a 2x2 array in Ge heterostructure has been investigated, showing the ability to form double quantum dots incorporating charge sensing capabilities [59]. Using the same platform, it has also been shown the ability to perform spin-qubit operations in the single-hole regime [29]. However, in all these devices, charge sensing is still implemented to achieve high-fidelity readout. In silicon, the transport properties of a quadruple quantum dot have been addressed, investigating this nanodevice as a possible scalable quantum information architecture [60].

One of the solutions remove the requirement of an additional charge sensor has been found by implementing gate-based dispersive readout. This technique makes use of one of the quantum dots in the array as the sensor of the surrounding quantum dots [43, 61, 62], and it has proven to be a valuable alternative for high-fidelity quantum dots and qubits readout. The readout signal intensity of this technique is inversely proportional to the distance between the electrodes controlling the quantum dot and the quantum dot itself. Such a distance usually ranges from 20 to 50 nanometers for electrostatically defined semiconducting quantum dots. In the foundry devices investigated in this thesis, the quantum dots are generated much closer to the control electrodes (few nanometers), boosting the readout efficiency. In chapter 5 and 5 we explore the potential of a foundry-fabricated array of 2x2 quantum dots in silicon using gate-based dispersive readout. Similar readout improvements for gate-based readout has also been shown in germanium hut wires [63].

The notions introduced so far place silicon spin qubits among one of the most promising candidates for the realisation of a fully functional universal quantum computer, and set the stage for a truly exciting decade of quantum computing experiments to be performed.

1.3 Thesis outline

The experiments described in this thesis aim at the study of silicon quantum dot devices for their implementation in a spin-qubit quantum computer. The initial part of this dissertation is devoted to the study of university fabricated one-dimensional arrays of quantum dot devices, developed in Si/SiGe heterostructures. Two different architectures are investigated: first we discuss single-gate-layer devices, presenting their fabrication and the capability to perform single-spin real-time detection. Subsequently, we move to the discussion of overlapping-gate gate architectures, presenting their fabrication and initial transport characterization. The comparison is later extended to state-of-the-art foundry-fabricated silicon quantum dot devices, arranged in a two-dimensional array. Developing a hybrid readout technique, combining gate-based and charge sensing, we demonstrate high tunability and reconfigurability of the array. Additionally, future directions as well as initial experiments to develop a spin-qubit quantum computer using these foundry-fabricated quantum dot devices are laid out.
This thesis is organised as follow:
Chapter 2 introduces the theoretical background for single and double quantum dot systems, analysing their main transport features. Subsequently, different spin-qubit implementations are discussed.
Chapter 3 is focused on the description of the experimental techniques as well as the cryogenic setup that has been used to perform these experiments. We analyse the reflectometry setup that has been used in this work, comparing the capabilities and limitations of charge sensing using RF-SET (implemented in Si/SiGe quantum dots) in contrast with gate based dispersive readout (exploited in CMOS devices). Furthermore, nanofabrication techniques employed

to realise state-of-the-art Si/SiGe quantum dots devices using university cleanrooms are described. Eventually, we outline the working principle of silicon nanowire devices produced by the industrial foundry CEA-Leti.

In **Chapter 4** we present the study of double and triple quantum dots using single-gate-layer devices on Si/SiGe heterostructures, investigated using charge sensing techniques via an RF-SET. Charge sensing enabled the detection of single-spin tunneling events using real-time measurements at 24 µs integration time, a requirement to implement Loss-DiVincenzo qubits. Subsequently, we introduce the results obtained for the overlapping gate geometry devices. The better versatility of these devices has already been proven to be a key element in the development of the next-generation of university fabricated quantum dots devices.

Chapter 5 concerns the study of the foundry FDSOI devices implementing gate-based reflectometry readout. The main focus is directed towards the study of a two-dimensional array of quantum dots, involving four quantum dots. In order to extensively characterize the device, we introduce a new hybrid readout technique, combining charge sensing and gate-based dispersive readout. This technique overcomes the limitations arising from a purely dispersive readout, enabling to access single-electron occupation for each quantum dot.

In **Chapter 6** we harness the readout technique introduced in the previous chapter to further develop the study of the two-dimensional array. The main outcome of this chapter is the implementation of a protocol to study the shuttling of two electrons in two dimensions within the array. Furthermore, we show how the high charge sensitivity inherited from the charge hybrid readout technique allows us to develop a measurement architecture which dramatically shrinks the acquisition time for high-dimensional charge states. This might be beneficial in the study of higher dimensional quantum dot arrays.

In **Chapter 7** we outline the main outcomes of this dissertation, discussing future experiments oriented toward the development of a spin-qubit quantum computer based on foundry-fabricated quantum dots.

2

A Short Introduction to Quantum Dots and Spin Qubits

The first part of this chapter gives an overview over gate-defined single and double quantum dot systems. In the second part, we outline different proposals for the implementation of spin qubits, discussing their advantages and disadvantages.

2.1 Quantum dots

In a real atom the positive charge of the protons generates an attractive potential that counteracts the repulsion of the closely packed electrons. Similarly, quantum dots are artificial nanostructures that exploit attractive potentials to

confine a finite number of electrons in solid state materials.
Twenty years of technological progress led to the discovery of a wide range of trapping potentials that can be used to confine electrons, such as electrostatic gating [52], strain effects [64] and crystal confinement [65]. Fig. 2.1.1(a) shows an example of an electrostatically formed quantum dot. Negatively charged metallic leads (in light grey) induce electrostatic fields in the underlying GaAs/AlGaAs compound, trapping electrons in the central region. Fig. 2.1.1(b) and (c) report an example of quantum dots induced because of crystal structure confinement. A quantum dot is formed in an InAs nanowire crystal (light grey). The change in material composition, in this case replacing the InAs with InP (dark grey), induces the confining potential. The InP is identified by the white arrows in Fig. 2.1.1(b) and (c). A schematic of strained induced quantum dots is reported in Fig. 2.1.1(d). An island of InP deposited on the surface of GaAs induces a quantum dot in the underlying InGaAs layer. Despite having different architectures, all systems mentioned above share several key features: the confinement of the electrons in the three spatial dimensions and the implementation in a solid state material. Due to their similarity to real atoms, quantum dots are often called "artificial atoms".
Unlike real atoms, the orbital level spacing in semiconducting quantum dots is of the order of a few meV due to the increased electronic Bohr radius and reduced effective mass m* [66]. The combination of increased Bohr radius and reduced m*, enables the study of spin-orbital effects at moderate magnetic fields (<3 T) for quantum dots. In real atoms, the observation of similar interactions would require magnetic fields on the order of 10 kT[1].
Just as two hydrogens atoms can be brought together to form a molecule (H_2), two quantum dots can be placed one next to the each other to form artificial molecules (investigated in section. 2.1.2), making quantum dots a very unique table-top simulator for "artificial chemistry".

[1] Typically, such magnetic fields can only be found in neutron stars.

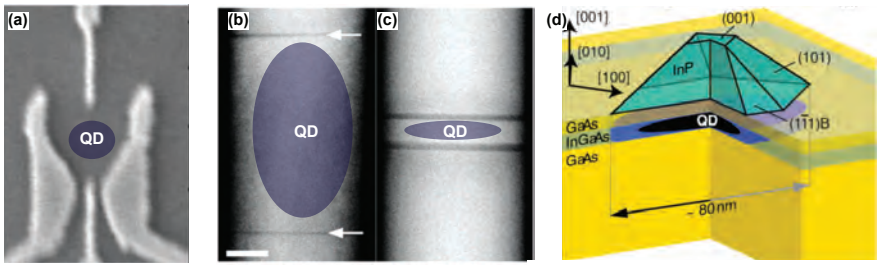


Figure 2.1.1 – Quantum dots. (a) Micrograph of a laterally defined quantum dot in a GaAs semiconductor heterostructure (dark grey). Metallic leads (light grey) confine the electrons, forming a quantum dot (QD) in the central area [52]. (b) and (c) Micrograph of InAs nanowires (light grey). Quantum dots (QD) are formed by crystal structure confinement. A different material, InP (dark-grey) defines the extension of the quantum dots in the InAs. [65]. (d) Sketch of strain induced quantum dots (QD). An island of InP with a finite size induces a quantum dot in the underlying InGaAs quantum well [67].

Coulomb blockade

The electrons trapped in the quantum dot are all densely packed together leading to the presence of electrostatic repulsion between each others. Therefore, in order to add one more electron to the quantum dot, energy has to be supplied from the environment to overcome the electrostatic forces. The presence of electrostatic forces that avoid the continuous flowing of electrons through the quantum dot give rise to Coulomb blockade, a distinctive feature of quantum dots. This can be further explained using the following phenomenological picture.

A quantum dot can be considered to be a metallic island (i.e. considering the presence of the electrons only), which holds a charge $Q = eN$, where N is the number of electrons, and has a self-capacitance C. The electrostatic energy of the quantum dot island is given by $E_{el}(N) = (eN)^2/C$. In order to add one additional electron to the island, the energy $E_{add} = E_{el}(N+1) - E_{el}(N) = eN/C$ has to be supplied. This yields a charging energy:

$$E_c = E_{add}(N+1) - E_{add}(N) = e/C. \tag{2.1}$$

Considering a semiconducting quantum dot with a radius of hundreds of nm and C $\sim$ 50 aF (which is a reasonable assumption for these systems), constant charging energies in the order of 1 mV (in the limit N >> 1) can be calculated. The charging energy is the energy that has to be supplied by the environment to add one more electron to the system, due to electrostatic repulsion.
A quantum dot can be probed using transport measurements. The charge transfer through the quantum dot is strongly dependent on the energy levels distribution. Anytime a quantum dot energy levels align with the Fermi energy (E_F) of the reservoirs, the electrons are allowed to move across the quantum dot giving rise to current peaks in transport measurements, called Coulomb peaks. When the energy levels are not aligned with the E_F, the system is blocked, and the current suppressed. The regions in between current peaks, where no transport is allowed, are known as Coulomb blockaded regions, or Coulomb valleys. This gives rise to a non-linear I-V characteristic, a signature of quantum dots.

2.1.1 Constant interaction model

We now introduce the constant interaction model [68–70], a theoretical model that allows the extension of the phenomenological results previously obtained to a systems containing many quantum dots. As seen in Fig. 2.1.2(a), quantum dots can be pictured as islands of charges coupled to electronic reservoirs, source (S) and drain (D). The couplings are usually realised via tunnel barriers that can be modeled as a parallel circuit of capacitors and resistors, where the RC time constant of the circuit sets the timescale of the tunneling events (i.e. only after a finite rise time, the electron will tunnel either into or out the quantum dot). Additionally, a capacitance C_g couples the dot to a plunger gate (V_g). The plunger gate provides the external energy to move the ladder of energy levels within the quantum dot.
In an experiment, the island's self capacitance introduced in the previous section is given by $C = C_S + C_D + C_g$, with C_i being the capacitance between the island and the source, drain and gate electrodes, respectively. The to-

tal charge for N electrons in the quantum dot can now be defined as $Q = e(N - N_0) - C_g V_g - C_S V_S - C_D V_D$ where N_0 is the charge at $V_g = 0$. Calculating the electrochemical potential $\mu_N = E_{el}(N) - E_{el}(N-1)$ of the quantum dot, it yields a charging energy:

$$\Delta\mu_N = \mu_{N+1} - \mu_N = E_C + \Delta E \tag{2.2}$$

where we recover again $E_C = e^2/C$ and ΔE is now introduced to represent additional quantum mechanical energy states. As the gate voltage of the quantum dot is swept, the current through the device does not increase linearly, but it presents resonances anytime the additional energy supplied from the plunger gate matches the charging energy. This leads to the non-linear transport characteristics in Fig. 2.1.2(b). Fig. 2.1.2(c) reports a sketch of the current flowing through a quantum dot as a function of the bias windows $V_{SD} = V_S - V_D$ and plunger voltage V_g. The current shows a response typical of quantum dots, called Coulomb diamonds. Charging energies can also be extracted from Coulomb diamonds when the condition $\Delta\mu_N = \alpha V_{SD}$ is met. α is known as the lever arm and it represents the conversion parameter from gate voltage to energy. When arrays of quantum dots are studied, it is beneficial to introduce a matrix form of the constant interaction model [69].
We now consider a network of N capacitive coupled nodes (where a node can either be a quantum dot or a voltage supply). The charge at the i^{th} node can be written as the sum of all the other charges arising from the capacitors c_{ik} connecting the i^{th} node to the surrounding nodes k in the network. If V_i is the voltage on the i^{th} node:

$$Q_i = \sum_{k=1}^{N} c_{ik}(V_i - V_k) \rightarrow \vec{Q} = \hat{C}\vec{V} \text{ where } \begin{cases} C_{ii} = \sum_{k\neq j}^{N} c_{jk} \\ C_{ik} = C_{ki} = -c_{jk} \end{cases} \tag{2.3}$$

where $\hat{C}$ is called the capacitance matrix. The electrostatic energy of the system is given by the the sum of the electrostatic energy stored on the $N(N+1)/2$

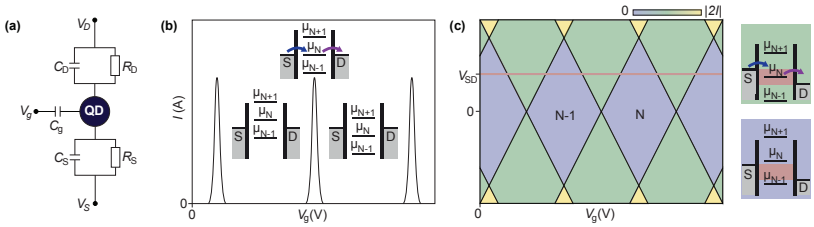


Figure 2.1.2 – Single quantum dot. (a) Circuit diagram for a single quantum dot (QD), tunnel coupled to source (S) and drain (D) and capacitively coupled to a gate electrode V_g. (b) Schematic of the non linear I-V characteristic of a quantum dot. On top of a Coulomb peaks μ_N is aligned with the electrochemical potentials of the reservoirs. Once this condition is not met anymore the system falls in a Coulomb valley and the current is suppressed. (c) Schematic of the current flowing in a quantum dot as a function of the V_{SD} bias window. In the low bias regime ($V_{SD} < \Delta\mu_N$) diamond shaped region of suppressed current are present. As $V_{SD} > \Delta\mu_N$, known as high bias regime, the current can flow through multiple channels.

capacitors in the network, yielding $E_{el} = 1/2\vec{V}C\vec{V}$. The voltage array can also be seen as $\vec{V} = \vec{V}_v + \vec{V}_c$, where $\vec{V}_c$ is the contribution from voltage sources[2], which is always know in an experiment. $\vec{V}_v$ is the actual voltage on the charge nodes that has to be identified. Analogously, $\vec{Q} = \vec{Q}_v + \vec{Q}_c$, yielding the block matrix form of equation 2.3:

$$\begin{pmatrix} Q_c \\ Q_v \end{pmatrix} = \begin{pmatrix} C_{cc} & C_{cv} \\ C_{vc} & C_{vv} \end{pmatrix} \begin{pmatrix} V_c \\ V_v \end{pmatrix} \rightarrow \vec{V}_c = \hat{C}_{cc}^{-1}(\vec{Q}_c - C_{cv}\vec{V}_v) \tag{2.4}$$

The resulting equation enables the calculation of the electrostatic energy E_{el}, relying only on the knowledge of the charge on the dots, the capacitances between the dots, and the capacitances between the dots and the gates. All of these quantities can be experimentally measured. The knowledge of the interdot (C_{cc}) and dot to gates (C_{cv}) capacitance matrices will be shown to be essential to perform the experiment in chapter 5 and chapter 6.

[2]Voltage sources can be included in the network by treating them as nodes with large capacitances to ground and large charges on them.

2.1.2 Double quantum dots

Complex chemical compounds can be build starting from the knowledge of atoms and molecules. Similarly, complex quantum dot networks can be investigated starting from the properties of single and double dots.
Fig. 2.1.3(a) shows the circuit diagram used to describe a double quantum dot, where we introduce the interdot tunnel coupling (C_m). Implementing the constant interaction model introduced in section 2.1.1, we can derive the electrochemical potential μ_1 and μ_2 of the quantum dots, yielding the definition of charging energies $E_{C1}(C_{g1}, C_m)$ and $E_{C1}(C_{g2}, C_m)$ as well as a mutual charging energy $E_{Cm}(C_{g1}, C_{g2}, C_m)$[3]. The mutual charging energy represents the energy variation of one of the two quantum dots when an electron is added to the other one. Fig. 2.1.2(b),(c) and (d) show schematics of the ground state charge occupation of a double dot in the case $C_m = 0$, $C_m < C_{g1(g2)}$ and $C_m > C_{g1(g2)}$, for a fixed $V_{SD} = 0$, respectively. For the fully uncoupled quantum dots, the charge occupation of each dot is controlled by its own plunger gate $V_{g1(2)}$. As C_m increases to intermediate values $0 < C_m < C_{g1(g2)}$, the correction term E_{Cm} becomes non-negligible, leading to a reshaping of the regions of stable charge into hexagons. As a single electron is loaded into one of the quantum dots, the electron shifts the charge transition of the other quantum dot, leading to the rise of two new lines in the charge stability diagram, known as *interdot* charge transitions (ICTs). The charge stability diagram introduced in Fig. 2.1.2(c) is known as a honeycomb diagram, a characteristic feature of double quantum dots. In the limit of very strong C_m, the two dots merge into a single dot, and striped regions of constant charge are visible in the charge stability diagram, with total charge $N = N_1 + N_2$.
It is interesting to consider how current can flow in a double quantum dot system. In Fig. 2.1.2 (c) we can identify points where three lines meet, separating three regions with different charge ground states. These points are known as triple points and they are the only gate-space regions where current is able to

[3] A full derivation of these quantities can be found here [69].

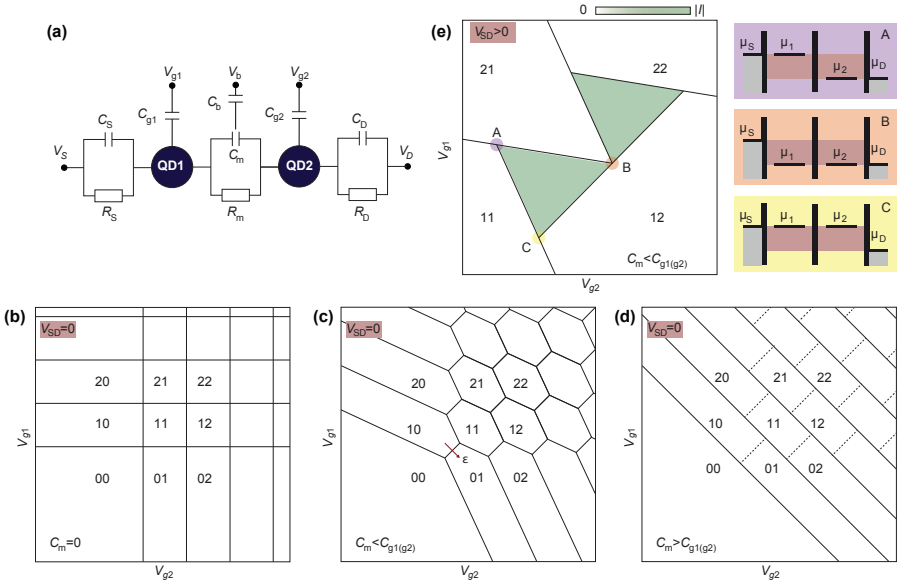


Figure 2.1.3 – Double quantum dot.(a) Circuit diagram for a double quantum dot. The interdot coupling strength is represented by C_m and R_m. V_b is the electrode that controls the strength of the mutual capacitance C_m. (b)(c)(d) Schematic double dot charge stability diagrams for different regimes of the capacitive coupling C_m for (b) zero, (c) intermediate and (d) strong values. These diagrams are shown in the absence of source-drain bias. (e) Interdot charge transition in presence of a finite source-drain bias $V_{SD} > 0$. Current can only flow within the green triangular region defined by the three energy configuration on the right. Elsewhere current is blockaded.

flow, in the absence of bias. Triple points corresponds to the configurations in which the chemical potential of the reservoirs are aligned with both the energy levels of the right and left quantum dots. As the system experiences $V_{SD} > 0$, triangular regions of non-suppressed current are visible, as shown in Fig. 2.1.3(e). These triangles enclose a region in gate space in which the chemical potentials of the quantum dots μ_1 and μ_2 lie in the window opened by the V_{SD} bias. Considering a series double quantum dot at low temperature $k_BT \ll E_{C1(C2)}$, current can flow if the dot closer to the drain has a lower energy potential compared to the quantum dot closer to the source. In fact,

electron hopping between the quantum dots always happens from higher to lower energy. For $V_{SD} > \Delta E$, the system enters the high bias regime, where multiple energy states lie within the bias window. This leads to the presence of fine features within the bias triangle, as multiple channels can contribute to the current signal [69].

2.1.3 Interdot tunnel coupling

So far we considered a purely classical capacitance model to understand the physics of a double quantum dot. However, quantum mechanics plays a fundamental role, since it describes the rate of electrons hopping between the two quantum dots. This is crucial when performing double quantum dot experiments. Let us consider a gate electrode V_b connected to the interdot tunnel barrier via a capacitance C_b as in Fig 2.1.3(a). By tuning V_b, the strength of tunnel barrier can be tuned, which, phenomenologically, can be seen as the effect of increasing or decreasing the resistor R_m, modifying the RC time that the electron would require to move in between dots[4]. This can also be seen using a description based on quantum mechanics wavefunctions. By tuning the barrier gate, we are able to control the overlap of the electron wavefunction inside the quantum dots. This can also be seen in terms of artificial chemistry: when the tunnel barrier is made large (high R_m values), electrons are localised on both dots, forming an ionic-like molecular bond, whereas for low R_m, the electrons are delocalised between the two dots yielding a covalent-like bond. When considering a tunable interdot strength, a double quantum dot can be described by a matrix model as follow:

$$H = \begin{pmatrix} \varepsilon & t_c \\ t_c & \varepsilon \end{pmatrix} \tag{2.5}$$

with $\varepsilon = V_{g1} - V_{g2}$ defined as the detuning parameter (see Fig. 2.1.3(c)) and t_c defined as the tunnel coupling element that describes the strength of the

[4]Here we are making an analogy between the charge and discharge time of an RC electrical circuit, since the two concepts are similar.

mutual interaction. Solving the Hamiltonian defined in equation 2.5, it yields the following ground state energy solution:

$$E_G = \frac{1}{2}\left(E_L - E_R - \sqrt{(E_L - E_R)^2 - 4t_c^2}\right) \tag{2.6}$$

where E_L and E_R are the energies of the uncoupled left and right quantum dot. As the molecule moves from ionic to covalent bond, the ground state of the system is represented by a higher percentage of wavefunction mixing, up to a maximum of 50% at $\varepsilon = 0$. For simplicity let us consider a single electron trapped in the double dot for a matrix element $t_c \neq 0$. At the maximum mixing detuning value, the electron can be seen as spatially delocalised in the double quantum dot, making it very polarisable. This feature is going to be important for the understanding of the readout technique explained in chapter 3. By evaluating the first excited state solution E_E, the tunnel coupling rate is given by $2t_c = E_E - E_G$, at the condition $\varepsilon = 0$.

2.2 Spin qubits

As introduced in chapter 1, classical computers rely on classical bits as a building block unit, and classical bit can only be in two states "0" or "1". Quantum computers use quantum bits, which, in addition to the two classical states, allow the system to explore any superposition of these states during computation. The qubit wavefunction can be described as follow:

$$|\Psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \text{ with } \alpha^2 + \beta^2 = 1 \tag{2.7}$$

where α^2 and β^2 are the probabilities of finding the system in either the $|0\rangle$ or the $|1\rangle$ state, respectively. Since the probability of any wavefunction has to be normalized, it is convenient to rewrite equation 2.7 in spherical coordinates as:

$$|\Psi\rangle = \cos\left(\vartheta\right)|0\rangle + \exp^{i\varphi}\sin\left(\vartheta\right)|1\rangle \text{ where } \vartheta \in \left[0, \pi\right] \text{ and } \varphi \in \left[0, 2\pi\right[\tag{2.8}$$

where ϑ and φ are polar angle and azimuthal angle of a sphere. Using equation 2.8 as definition of $|\Psi\rangle$, any vector from the center of the sphere to its surface is a convenient way to represent any two-level system, which in our case is any qubit state. The spherical construction of a two-level system is called the Bloch sphere. Qubit gates can be seen as rotations on the surface of the Bloch sphere.

Spin qubits encode the two states that form the computational subspace in the electronic spin degree of freedom. Due to its nature, the spin can be controlled by an external magnetic field while being unaffected by external electric field fluctuations, leading to longer coherence times. The rest of this section is devoted to the introduction of three different spin-qubit platforms in quantum dot devices, the Loss-DiVincenzo qubit [8], the S-T_0 qubit [71], and the exchange-only qubit [72], which require one, two and three quantum dots, respectively.

2.2.1 The Loss-DiVincenzo qubit

The idea of a spin qubit was first proposed by Loss and DiVincenzo 1998 [8]. The so-called Loss-DiVincenzo (LD) qubit is based on a single electron trapped in a single quantum dot, as shown in Fig. 2.2.1(a). In the presence of an external magnetic field B_0, the two spin states split in energy forming the computational space given by $|\uparrow\rangle$ and $|\downarrow\rangle$, as shown in Fig. 2.2.1(b). The two states are separated in energy by the Zeeman energy $\Delta E_Z > k_B T$, as shown in Fig. 2.2.1(c). A Loss-DiVincenzo qubit can always be initialized to the fiducial state, since an electron loaded into the dot relaxes to the ground state $|\downarrow\rangle$, after waiting its relaxation time T_1.

Manipulation of the spin state can be performed using two similar approaches. The first method relies on the application of an oscillating magnetic field at the quantum dot position [73], a method known as electron spin resonance (ESR). This can be achieved by running an AC current in a microwave stripline antenna fabricated in close proximity to the quantum dot [73]. Single qubit addressability can be achieved using g factor modulation [32, 36]. The second

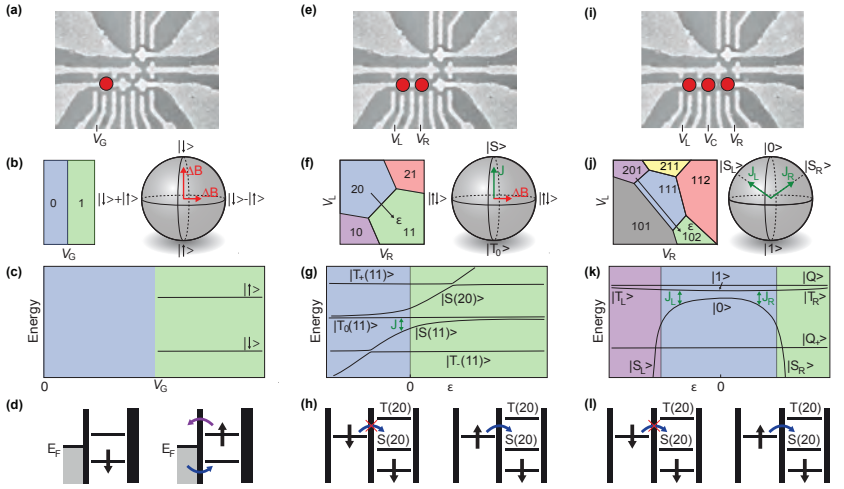


Figure 2.2.1 – **Spin-qubit architectures.** (a) Single quantum dot for the implementation of a Loss-DiVincenzo qubits. V_G controls the dot energy configuration. (b) Schematic charge stability diagram for a single dot on the left. Bloch sphere for a Loss-DiVincenzo qubit with $|0\rangle = |\downarrow\rangle$ and $|1\rangle = |\uparrow\rangle$ and the control axis on the right. (c) Energy diagram as a function of the control gate V_G. (d) Elzerman readout technique based on spin-to-charge conversion. (e) Double quantum dot platform for the implementation of S-T_0 qubits. V_L and V_R control the chemical potential of the left and right dot, respectively. (f) Schematic of a double quantum dot charge stability diagram, with ε being the detuning parameter. On the right, the Bloch sphere reporting the computational basis and the control axis for a S-T_0 qubit. (g) Energy diagram for a double quantum dot in the presence of a magnetic field as a function of the detuning parameter ε. (h) Pauli spin blockade readout technique for spin-to-charge conversion in double quantum dots. It relies on spin-selective charge tunneling. (i) Triple quantum dot system for implementation of exchange-only qubit. The three gates control the energy configuration of the respective dots. (j) Schematic charge stability diagram of a triple dot, where V_M is kept at a constant value. The detuning ε indicates the isoelectronic detuning direction. On the right side, Bloch sphere representation of the computational states and control axis. (k) Energy levels as a function of detuning in presence of an external magnetic field. Each state has a spin-split partner state with opposite spin projection (not shown). (f) Pauli spin blockade readout technique for spin-to-charge conversion in double quantum dots. It relies on spin-selective charge tunneling.

approach is based on the implementation of electron-dipole spin resonance (EDSR), which exploits the complementary mechanism compared to ESR. An

electron is moved back and forth within a constant gradient of magnetic field via an AC electric excitation. The field gradient can be generated from natural [25] or synthetic [23] spin-orbit interactions. The synthetic spin-orbit field is achieved by implementing micromagnets, which automatically enables single spin-qubit addressability in a multiqubit device. In fact, by creating a gradient of magnetic field, each electron at the i^{th} dot position is subjected to a distinct total magnetic field $B_{tot} = B_0 + \delta B_i$ [74]. Furthermore, valley-driven EDSR manipulation has been shown in foundry-fabricated devices [75]. Using this technique, spin rotations can be induced exploiting the valley degree of freedom, not requiring the presence of an additional stripline or micromagnet.
We now move toward the detection of the electronic spin. The magnetic moment of a single electron is $\sim$58 μeV/T, and its direct detection is possible but very sophisticated and not scalable yet [76]. Fig. 2.2.1(d) shows a scheme that allows the conversion of a single-electronic spin information into a charge signal, a much easier quantity to measure. The working principle of this scheme is explained in the following lines. As the manipulation step has been completed, the quantum dot energy levels are brought in close proximity to E_F, such that the chemical potential of the reservoir lies in between the two spin states. If the electron is in a $|\downarrow\rangle$, the electron is blocked inside the quantum dot owing to Coulomb blockade. Conversely, if the qubit ended being in $|\uparrow\rangle$, the electron tunnels out of the quantum dot, since this energy level is above E_F, and a new electron can tunnel in, reinitializing the qubit [77].
As introduced in chapter 1, beside single-qubit gates and readout capability, two-qubit gates are required to implement a universal quantum computer. Two-qubit gates using the Loss-DiVincenzo architecture can be performed by using the Heisenberg exchange interaction (J) between two electrons sitting in adjacent dots. The energy term is given by $H_H = J\vec{S_1} \cdot \vec{S_2}$, where the indices refer to the spin of each electron sitting in the quantum dots.
Over the past decade, many two-qubit gates have been implemented for Loss-DiVincenzo qubits, the CNOT gate [33], the SWAP gate [21] and the CPHASE gate [32]. Furthermore, using a programmable two-qubit processor the first implementation of Deutsch-Josza and the Grover search algorithms using LD

qubits has been demonstrated [35].
Recently, the demonstration of coherent spin shuttling has been fundamental to set the stage for the implementation of multiqubit experiment, enabling the information to be moved over micrometer distances [78, 79].

2.2.2 The single-triplet qubit

When implementing a LD qubit, a large external magnetic field B_0 is typically required to provide a Zeeman splitting that is large enough compared to the other energy scales in the system in order to reduce sources of decoherence. However, it has been shown that the relaxation time T_1 is decreased due to phonon scattering [80] and valley processes (for silicon) [81, 82] as the magnetic field increases. The S-T_0 qubit, an alternative qubit architecture, enables the implementation of spin qubits at lower magnetic field. The S-T_0 exploits the energy states of two electrons confined in a double quantum dot, as shown in Fig. 2.2.1(e) and (f). The computational basis states are $|S\rangle = (|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle))/\sqrt{2}$ and $|T_0\rangle \left(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle\right)/\sqrt{2}$. The states becomes $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ when the two electrons are localized in the two quantum dots. Additionally, the S-T_0 basis operates in the subspace $m_s = 0$, which makes the qubit insensitive to global magnetic field fluctuations. Furthermore, only small magnetic fields are required to perform the computation, of the order of a few hundred millitesla.
In a similar way to the LD qubit, the initialization can be performed by loading two electrons in the same quantum dot and waiting long enough for them to decay to the ground energy state, eventually relaxing to a singlet state $|S\rangle$ [21]. Manipulations along the two computational axis can be performed by the means of pure electric fields using the exchange interaction (J) to evolve between the $|S\rangle$ and $|T_0\rangle$ states as well as a gradient of a magnetic field to evolve the wavefunction between the two quantum dots as the exchange interaction is turned off (Fig. 2.2.1(f) reports a sketch of these two control parameters). To achieve universal control over the two axes, different methods have been implemented. Some examples of these methods are pumped polarization of the

atomic nuclei [83], synthetic spin-orbit coupling using micromagnets [84] and g-factor modulation [85] for control over ΔB. The strength of the exchange interaction is controlled by fast switching between the dot occupations (11) and (20) using fast gate pulses. For an experimentalist, control over the J axis can be seen as moving along the detuning axis of the double quantum dot. As can be seen in Fig. 2.2.1(g), working with an additional electron compared to the LD qubit increases the number of energy states present in the operating parameter space of the qubit: $|T_+\rangle = |\uparrow\uparrow\rangle$ and $|T_-\rangle = |\downarrow\downarrow\rangle$. The presence of additional states could cause leakage errors to states outside the computational subspace. However, it is possible to overcome this issue by operating the qubit in the proper energy window as well as moving diabatically across any transition that involves mixing with leakage states as the $|S\rangle - |T_-\rangle$ transition [21].

In order to readout the state of the system, spin-to-charge conversion has to be implemented. The technique that has been developed involves the spin-conditional tunneling of an electron onto a quantum dot that already hosts a second electron. Fig. 2.2.1(h) shows the working principle of such technique. Assuming an electron is prepared in the $|\downarrow\rangle$ state in the quantum dot on the left. The $|\downarrow\rangle$ electron is allowed to tunnel to the right dot if the second electron has the opposite spin state, since the triplet state $|T(20)\rangle$ lies higher in energy. Therefore, if the two electrons have the same spin the tunneling is blocked and the electrons remain localised on the two dots. This conditional-tunneling process is known as Pauli spin blockade, and relies on the same principles that govern the Pauli exclusion principle for atomic shell filling. Once the readout is performed, the system can be immediately reinitialized, and the qubit prepared to compute another operation, without the requirement of exchanging electrons with the leads. This is an advantageous property of the S-T_0 qubit over the previously discussed LD qubit. As an example, by removing the requirement of exchanging electrons with the reservoir, the double quantum dot could be completely decoupled from the reservoirs. Working with in a similar configuration the double quantum dot would be protected from the temperature broadening induced from the reservoirs, enabling the operation of the

$S\text{-}T_0$ qubit at a much higher temperature.
Two-qubit gates have been implemented using dipolar coupling between two double quantum dots, but since the coupling is purely electrical the two coupled double quantum dots are more likely to couple to charge noise, leading to fast dephasing [26].

2.2.3 The exchange-only qubit

One of the advantages of $S\text{-}T_0$ over to the Loss-DiVincenzo qubit comes from the electrical control of one rotation axis. Moving to a fully electrically controlled spin qubit would be highly beneficial for the implementation of a large scale spin-qubit computer. In fact, it would eliminate the requirement of gradients of magnetic fields and GHz frequency control signals to match the Zeeman splitting energies for EDSR manipulation. Furthermore, the exchange interaction is highly local and yields large on-off ratio using gate pulses only, compared to the slower ESR and EDSR manipulation sequences. Quantum gates implemented using electrical control would boost quantum gate timing, since electrical pulses can be controlled on a nanoseconds scale. Furthermore, a fully electrical spin-qubit quantum computer would be compatible with the moderate magnetic fields needed to integrate superconducting elements, both for readout [86, 87] and long range coupling [44, 45].
Unfortunately, the Heisenberg interaction alone does not provide a set of universal gates for the $S\text{-}T_0$ qubit implemented in a double quantum dot, since the Heisenberg interaction commutes with both the $\hat{S}$ and $\hat{S_z}$ operators, which represent the total spin number of the system and its projection. A possible solution is to implement a qubit which operates in a subspace which has $\Delta s = 0$ and $\Delta m_s = 0$, where the exchange interaction alone can be used for universal control [72]. This has been achieved by moving to a three-electrons system localised in three quantum dots as shown in Fig. 2.2.1(i). The addition of the third electron generates a computational subspace which conserves both the total spin and its projection along the z direction. Fig. 2.2.1(j) shows a schematic charge stability diagram representative of the qubit opera-

tion regime, in which each quantum dot contains one electron. The right side of Fig. 2.2.1(j) shows the Bloch sphere for the three-electrons quantum dots. The computational space is generated by $|0\rangle = \left(|\downarrow\uparrow\uparrow\rangle - 2\,|\uparrow\downarrow\uparrow\rangle + |\uparrow\uparrow\downarrow\rangle\right)/\sqrt{6}$ and $|1\rangle = \left(|\uparrow\uparrow\downarrow\rangle - |\downarrow\uparrow\uparrow\rangle\right)/\sqrt{2}$, both states having $s = 1/2$ and $m_s = 1/2$ [88, 89]. However, it is also important to consider that the addition of one more electron leads to an increase in the number of possible leakage states in the computational space as illustrated in Fig. 2.2.1(k), where $|Q\rangle$ refers to the quadruplet states with total spin s=3/2. In general, these high spin states can be neglected, since the system is initialized in one of the doublet states that define the computation subspace, and the total spin number is not changed during the operations.

The exchange-only qubit can be initialized in either the $|S_L\rangle$ or $|S_R\rangle$ states by performing Pauli spin blocked measurements as explained above for the S-T_0 qubit, since for either large positive or large negative detuning (c.f. Fig. 2.2.1(j)) the electrons are in an admixture of $|S\rangle$ and $|T\rangle$. The qubit is controlled by detuning the system from the (111) configuration to either the (201) or (102) configuration in order to increase either J_L or J_R, respectively. Experimentally this is achieved by applying fast square pulses along the detuning direction [90, 91]. The rotation axis offered by the two exchange interactions are separated by 120° from each other on the Bloch sphere, enabling universal control. The readout protocol makes use of Pauli spin blockade at both positive and negative detuning.

Several proposals for two-qubit gates using this platform have been proposed [92, 93], but extremely fine tuning of the multiple exchange interactions or long pulse sequences are required, making the implementation of these protocols challenging to be accomplished experimentally. The recent demonstration of coherent spin–photon coupling using an exchange-only qubit [94] represents an important milestone towards the implementation of a long-range two-qubit gate [95].

2.3 Silicon spin qubits

The last section of this chapter introduces the properties of quantum dots implemented in silicon, the material platform that is used in the following chapters. Silicon is a very attractive material for the implementation of spin qubits for several reasons: it has a reduced spinful nuclei concentration as well as a reduced spin-orbit coupling strength. These two parameters are related to how the crystal lattice of the semiconductor affects the spin state of the electrons during qubit operations.

Spin orbit interactions arises from a stretched lattice Coulomb potential seen by relativistic electrons moving in the conduction band, which experience an effective magnetic field [96, 97]. The spin-orbit interaction couples the electron orbital levels to the spin states, such that spin and orbital number are no longer good quantum numbers [68]. Therefore, for strong spin-orbit interactions, the spin of electrons can be very sensitive to electrical field noise. Spin-orbit interactions can arise from symmetries of the atomic lattice (known as Dresselhaus contribution) [98] as well as from gating effects (Rashba contribution) [99]. When spin-orbit interactions are present, phonons (which do not have a spin angular momentum) can now cause spin flip events. As a consequence, longer T_1 relaxation times are expected in silicon for Loss-DiVincenzo qubits and S-T_0 qubits compared to other materials having stronger spin-orbit interactions, such as gallium arsenide.

So far we only considered the spin of the electrons. However, when considering quantum dots, a single electron is surrounded by a vast amount of the nuclei that form the crystal lattice. When an external magnetic field is applied, the nuclei spins experience a Zeeman splitting which is a 1000 times smaller compared to Zeeman splitting of the electrons. At 20 mK, the thermal excitations are much bigger than the spin-split states of the nuclei, leading to a slowly drifting background magnetic field. Electrons can now couple to the spin nuclei via the hyperfine interaction, leading to short coherence times. Naturally occurring silicon is composed of 95% spinless nuclei (^{28}Si and ^{30}Si), and only 5% ^{29}Si which has a nuclear spin 1/2. Using isotopic purification processes, it

is possible to reduce the ^{29}Si concentration to a few parts per billion, achieving a "semiconductor vacuum" for spin qubits, further extending coherence time of spin qubits.

Another parameter that is usually considered when evaluating a material platform for the implementation of spin qubits is the effective electron mass m^*. The energy spacing in the quantum dot is proportional to $\left(Am^*\right)^{-1}$, where A is the area of the quantum dot. Therefore, a material with a high effective mass requires smaller quantum dot sizes in order to maintain a similar quantum dot level spacing compared to a material with lower m^*. This is the case for silicon, which has an effective mass of $m^* = 0.26\ m_e$, with m_e being the mass of the free electron, three times higher compared to GaAs or Ge.

When working with quantum dots in silicon, additional energy levels are present, known as valley states. They arise from a six-fold degenerate conduction band minimum in bulk silicon. In two-dimensional heterostructures, four of the valley states are separated in energy as a consequence of the z confinement [66]. The remaining two valleys states can be coupled to orbital states in SiGe or SOI nanodevices, giving rise to valley-orbit coupling terms [100]. Valley states are usually nearly degenerate in energy space, a feature that is detrimental when performing Pauli spin blockade. In fact, with reference to Fig. 2.2.1(h), we introduce the additional valley quantum numbers $|+\rangle$ and $|-\rangle$. Assuming the spin on the left belongs now to the energy state $|\downarrow,-\rangle$, whereas the right dot hosts $|\downarrow,+\rangle$. When moving the electron from the left dot to the right dot, even if the spin transition would be forbidden, the electron can now tunnel to the energy state $|\downarrow,-\rangle$, lifting Pauli spin blockade. Fabrication of material with valley states with an energy splitting larger than the Zeeman splitting would enable us to recover Pauli spin blockade for the transition (11)-(20). However, this seems to be complicated to achieve. Recovering of the spin blockade signal has been achieved by performing spin-to-charge conversion at the (13)-(04) transition for a double quantum dot [62]. At this configuration, the lower valley states are always filled with electrons, recovering the Pauli spin blockade signal for the upper valley states.

3

Experimental Techniques

In this chapter, we introduce the main experimental techniques that have been used in this thesis. In the first section we describe the experimental setup used in all of the three following chapters, mostly investigating the properties of the different electrical lines. Subsequently, we analyse the material platforms: Si/SiGe, used in chapter 4, and Si foundry-fabricated devices in chapters 5 and 6. The fabrication recipe for the single gate layer devices in Si/SiGe has been developed by C. Volk, and has been extended to the overlapping gate geometry by the author. The fabrication of CMOS devices has been performed by an external foundry, CEA-LETI in Grenoble. Lastly, we describe the two main readout techniques that have been exploited for this thesis, namely RF-reflectometry and gate-based dispersive readout.

3.1 Experimental setup and measurement techniques

As introduced in chapter 2, one of the key requirements for controlling and manipulating single electrons in quantum dots structures is a sufficiently low temperature, such that the thermal excitation k_BT is much smaller than the quantum dot level spacing. At room temperature, $k_BT = 25$ meV, but as the system is cooled at the base of a dilution refrigerator, around 20 mK, the thermal excitation becomes 10 μeV, a much smaller quantity compared to the typical energy scales for semiconducting quantum dots (above meV). The apparatus that has been used in this thesis, leading to the results presented in the next three chapters, is an Oxford Triton dilution refrigerator, equipped with a superconducting vector magnet with three axis control: 1 T along the X and Y directions, perpendicular to the fridge's main axis, and 6 T along the remaining direction. This system is shown in Fig. 3.1.1(a). Here, the magnet has been removed to access the interior of the fridge, but during measurement time it is anchored at PT2 (which thermalises at 4 K), such that it can be cooled down below its critical temperature. An extensive description of the wiring procedure can be found elsewhere [101] and here we only focus on characterizing the electrical lines according to their bandwidth as illustrated in Fig. 3.1.1(b). This analysis is useful to understand the calibration techniques and measurements performed in this and the following chapters. The PCB, shown in Fig. 3.1.1(c) and (d), is mounted inside a puck system (the frame is visible in Fig. 3.1.1(d)) anchored to the end-piece of the dilution unit, the mixing chamber (MC)[1]. Here the thermalised electrical lines are connected from the fridge to the PCB. The dilution system is also equipped with a load lock unit, which allows fast loading and unloading of devices, requiring only 9 hours to bring the newly loaded puck to base temperature. Cooling down from room temperature would require 48 hours.

In order to reject 50 Hz noise as much as possible, the frame that supports the

[1]The sample board presented is the one used for most of this thesis work; only in sections 4.1.2 and 4.2 a different board has been used, its specifications can be found in appendix B.

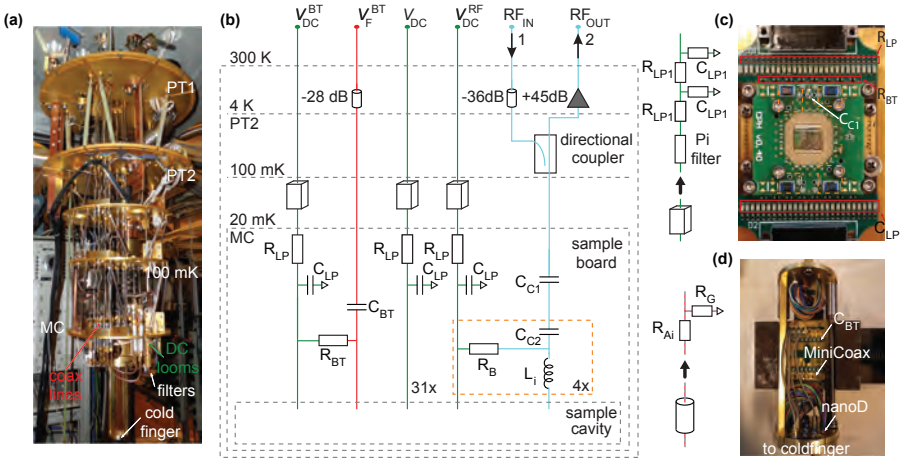


Figure 3.1.1 – Experimental setup. (a) Image of a cryo-free dilution refrigerator. The main cooling stages are indicated as well as most of the components to deliver voltages at the coldfinger. (b) Schematic of the wiring inside the dilution refrigerator. The green line indicates slow lines (green), carrying signals up to few kHz, fast lines (red), from few kHz up to GHz and reflectometry line (light-blue), carrying signals in the 100 MHz regime for readout. Additional electrical components that define the bandwidth of the lines are also reported (see appendix B for more informations). (c) Sample board system consisting of a mother and a daughter printed circuit board (PCB). See text for details.(d) PCB mounted inside a puck, shown from the back side.

fridge is isolated from the main ground, where most of the instrumentation is connected, and the fridge is grounded via a single point only, the magnet power supply ground, to avoid ground loops. Additionally, to reduce vibrational noise, the fridge frame is supported by compressed air springs, isolating the structure from building vibrations.

Low frequency electrical lines (DC - 10 kHz)

The fridge is equipped with 48 low frequency electrical lines, divided into 2 looms composed of 12 twisted pairs of constantan wire, a material which has a high thermal resistance. The looms are highlighted in green in Fig. 3.1.1(a) and (b) and are connected to the top of the dilution unit via Fischer connectors and

anchored at different stages of the dilution system for thermalisation purposes. These electrical lines are mostly used to perform current and conductance measurements, therefore requiring a very low noise environment, achieved by equipping them with two stages of filtering. The first consists of a series of pi filters and second order low pass filters with a cutoff frequency in the order of 100 kHz, in order to reject all the high frequency components, as reported on the right side of Fig. 3.1.1(b). At the coldfinger stage, the two looms are plugged in a single nanoD connector, that is subsequently connected to the puck. Additionally, the lines are filtered at the PCB level, as shown in Fig. 3.1.1(c), via a low pass filter with a 3 dB point of 100 kHz. As shown in the wiring schematic, some of the low-frequency lines are combined with high frequency lines via bias-tees, as explained in the next paragraph. Using the technique presented in section 3.1.1, a bandwidth of 10 kHz has been extracted, in agreement with the calculated RC rise-time.

High frequency electrical lines (10 kHz - 20 GHz)

The cryostat is also equipped with coaxial cables, meant to carry voltage signals up to several GHz, shown in red in both Fig. 3.1.1(a) and (b). Each coaxial line from room temperature to the coldfinger is divided into three sections: silver coated stainless steel (SS-SSS)[2] is used from room temperature down to the 4K stage and superconducting Niobium (Nb) coaxial lines are implemented from PT2 down to the MC, where, eventually, copper links connect to the puck (an exhaustive guide to thermal budgeting for coax lines can be found in [102]). In order to thermalise the incoming signal from room temperature, each line is anchored at the different stages via cryogenic attenuators, with a total attenuation of either 26 or 28 dB used for the experiments presented in the following chapters (the attenuation is distributed along the different stages of the dilution refrigerator). Mini-Coax connectors link the copper lines on the coldfinger to the PCB. No filters are installed inside the fridge for these lines, but they are combined with low frequency lines on the PCB via the

[2]Compared to SS-SS, the silver coating of the steel inner conductor increases the transmission properties of the coax.

previously mentioned bias tees. Using the technique presented in section 3.1.1, we extracted a 3 dB point for the high pass filter. The R_{BT} and C_{BT} SMD of the bias-tee are visible in Fig. 3.1.1(c) and (d), respectively. These lines are used to perform fast manipulation of the device, and the allowed bandwidth is fully compatible with the requirements imposed by the qubits introduced in section 2.2. Even if the coaxial lines used in this work are rated above 20 GHz, the sample board induces a heavy attenuation of the incoming signal for frequencies above 2 GHz.

Readout circuit (1 MHz - 1 GHz)

The readout circuit (in light-blue) is used to implement RF-reflectometry readout. As is discussed in section 3.3, the working principle of this technique consists in studying the reflected power from an LC oscillator loaded with the impedance of the device under study, with a resonator frequency typically in the order of hundreds of MHz. As shown in the wiring schematic, the circuit is composed of two coaxial lines coupled via a directional coupler anchored at the 100 mK plate. On the voltage-in line, the signal is heavily attenuated, and the reflected signal is amplified via a broadband cryogenic amplifier (Weinreb CITLF1 SN68) with an equivalent input noise of 4K. In order to readout multiple qubits at the same time, the circuit is equipped with a multiplexing circuit allowing the combination of up to four different readout tones (enclosed by an orange dashed line in Fig. 3.1.1(b) and (c)). Each multiplexing unit combines a low frequency signal, for DC biasing, with the RF carrier via a bias tee formed by R_B and C_C[3], with an RC rise time of 700 ns. The presence of both C_{C1} and C_{C2}, with $C_{C1} > C_{C2}$, is essential to reduce the amount of cross-talk between the reflected signals from the different L_iC circuits, since, as the signal is scattered back from the resonators, the lowest impedance path seen by the carrier is via the coupling capacitor C_{C1}, and not the other tank circuits.

[3] $C_C^{-1} = C_{C2}^{-1} + C_{C1}^{-1}$.

Printed circuit board

The printed circuit board implemented is composed of two parts, the main body (called a "motherboard") where the RC filters, bias tees, nanoD plugs for low frequency lines as well as Mini-Coax plugs for high frequency lines are placed. The motherboard is anchored to the frame of the puck and is intended to be non-interchangeable. The actual device is placed in the sample cavity of a second PCB (called a "daughterboard"), which hosts the multiplexing circuit; this board is intended to be interchangeable and facilitate sample changes without unbonding. The motherboard and daughterboard are interconnected via an interposer, an insulating layer equipped with metallic spring rods (called "fuzz buttons") that creates electrical contact between the two PCBs as they are tightened together [103]. Even if each fuzz button is rated for high transmission in the microwave regime, in practice the PCB combination cannot reach this regime, limiting the effective bandwidth of these lines. In fact, each fuzz button is used to carry an electrical signal and no proper coaxial-like configuration is implemented for high frequency transmission. Improvements can be made by designing additional fuzz buttons around the one carrying the high frequency signal, forming a shield-like structure, grounding them to the puck. Such an implementation would have required a much bigger and more expensive sample holder.

3.1.1 Calibration measurements

In order to perform the experiments presented in the following chapters, we performed an extensive calibration of the setup, both for low and high frequency measurements. To perform low frequency measurements, 50 Hz noise in the setup has been addressed and minimised. This has been achieved by connecting all the instrumentation in a star-like configuration, with respect to the dilution system frame reference and by removing all the instrumentation incorporating a voltage transformer as far as possible from the low noise elements (such as the DAC and breakout box) to avoid inductive noise pick-

up[4]. In order to be able to correctly perform high frequency manipulation, we monitored the effective in-situ waveform arriving at the sample.

High-pass corrections

First, we focus on the correction required to compensate for the RC time of the bias-tee (hpc). In the absence of such corrections, a square pulse will appear square at the device, but will drop in time. To implement the corrections, we identify a coulomb peak and apply a continuous square wave, as shown in Fig 3.1.2(a), using the blue pulse cycle in Fig 3.1.2(b), which yields the blue dataset in Fig 3.1.2(c). As can be seen, the detected voltage drops from the maximum intensity to 0 over a few hundreds of μs, approximatively corresponding to three times the RC time of the bias tee. Consequently, for a too long square waveform, the capacitor discharges and the pulse is not effectively applied to the sample. Analogously, this can be seen as the high pass filter removing all the low frequency components of the square waveform, below its cutoff frequency. Therefore, in order to apply longer waveforms, a linear correction[5] to the square pulse has to be applied, as shown in Fig. 3.1.2(b). As seen in Fig. 3.1.2(c), as the correction approaches the exact value (set to 80 μs for the implemented bias tees), the in-situ detected waveform approaches a square-like behavior. Once corrected, the rise time of the square wave enables to extract the full bandwidth of the demodulation circuit.

Square waveform detection

Next, we move towards the in-situ detection of the bandwidth of the two lines that are combined at the bias-tee, achieved by applying the correct waveform to a non-linear conductance feature, like a Coulomb peak, reported in Fig. 3.1.2(d). When applying a square waveform to the high-frequency input

[4] An acceptable 50 Hz noise intensity has been adapted from the value reported in section C.5.1 of Ref. [104].

[5] The high-pass filter behaves as a differentiator on the incoming wave. Therefore, in order to recover the original signal, it is necessary to apply the effect of an integrator. The integral function of a square wave is a linear ramp.

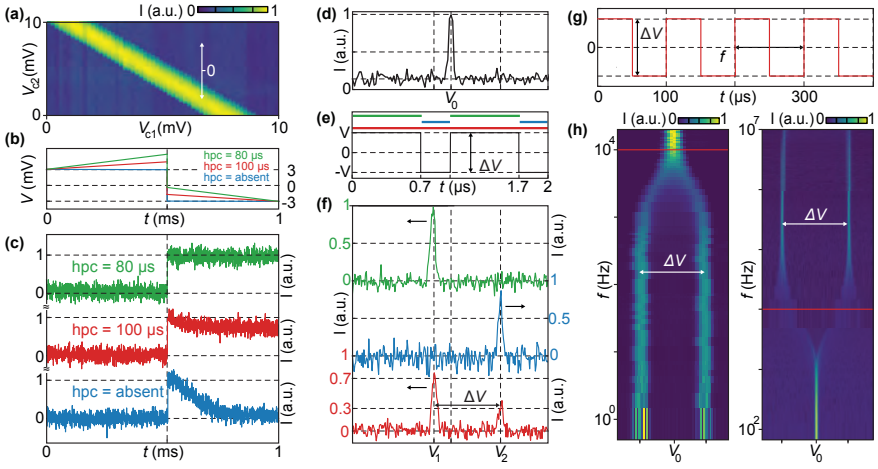


Figure 3.1.2 – Coaxial line characterization. (a) Coulomb peak as a function of two control parameters V_{c1} and V_{c2} coupled via C_{cv} (see chapter 2.1.1). Arrow indicates +/-3 mV pulse. (b) Sketch of a square pulse not corrected for the bias-tee rise time (hpc) (light-blue). Square pulse corrected the bias-tee rise time with 80 (green) and 100 (red) µs, respectively. (c) Effect of the non corrected (light-blue) square pulse shown in (a) as well as for a square pulse corrected for a 80 (green) and 100 (red) µs high pass filter. As shown, the green correction matches the RC time of the bias tee. (d) Coulomb peak as a function of a control parameter, set at position V_0. (e) 70/30 square pulse sequence with different integration periods. (f) Peak splitting of (d) as according to (e). Colour coding corresponds to (e). (g) 50/50 square pulse with a frequency of 10 kHz and amplitude ΔV. (h) Calibration of a low frequency (left) and high frequency (right) line. A coulomb peak, similar to the one in (d), splits according to the bandwidth of the investigated line. Shown in red the position of a 10 kHz square pulse.

of the bias-tee, the waveform crosses a capacitor (C_{BT} in Fig. 3.1.1(b)). As this happens, the effect of the capacitor is to average out any DC component carried by the square waveform. Fig. 3.1.2(e) reports a 70/30 duty cycle square wave at the output of an arbitrary waveform generator, which is then applied to a quantum dot via a bias-tee. We assume the pulse amplitude ΔV to be larger than the Coulomb peak FWHM. The DC component of the bias-tee is supplying a voltage V_0 which defines the position of the Coulomb peak. The capacitor affects the square wave such that the effective waveform delivered

at the device has an offset given by $O = -(+V * 0.7 - V * 0.3)$ compared to the waveform before the capacitor, and the resulting effects are reported in Fig. 3.1.2(f). Additionally, it induces a shift of the voltage axis, in the positive (negative) direction for the negative (positive) segment. Therefore, the single Coulomb peak splits into two copies, one at the position $V_1 = V_0 - (O + V)$ and the second at $V_2 = V_0 - (O - V)$. The intensity of each copy is proportional to the duty-cycle. If a digitizer is acquiring data continuously, the peaks intensity are given by the length of the high/low segment, which in this example leads to $0.7 * I / 0.3 * I$, respectively (red trace). As the digitizing instrument is integrating only during either the high or low segment, the intensity of each copy is as high as I in both cases (green and blue trace, respectively).

Electrical line bandwidth characterization

Eventually, the coaxial line bandwidths are characterized using a 50/50 duty-cycle pulse (for simplicity), as reported in Fig. 3.1.2(g). This enables us to calibrate the voltage division due to the presence of attenuators, which can be calculated as $V_g/V_i = (10^{A/20})/2$, where A is the total value of the attenuators in dB of the attenuators along the coaxial line, V_g is the voltage at the gate and V_i is the voltage at the input of the coax line. A suitable compensatory factor is then added in software such that the pulse voltage delivered at the sample is the expected one (ΔV, as shown in Fig. 3.1.2(h)). We then characterize the bandwidth of the line by varying the frequency of the square wave applied. As shown in Fig. 3.1.2(h), the low-frequency transmission is effective up to 2 kHz, where each copy shows half of the original intensity, and already at 10 kHz, the square pulse is completely filtered out, recovering original Coulomb peak. On the contrary, the high-frequency coaxial line covers the remaining part of the frequency spectrum, all the way up to a few GHz (not shown).

3.2 Silicon quantum dot devices

In the first part of this section we introduce the fabrication procedure developed in-house for Si/SiGe devices as well as the working principle of such

devices. Currently, Si/SiGe devices represent one of the best platforms for the development of a spin-qubit-based quantum computer, not only for the highly controllable formation and manipulation of quantum dots [53], but also for the high compatibility of these devices with on-chip elements such as micromagnets and coplanar waveguides[44].
These results have been enabled by scientists developing and fabricating quantum dot devices of rapidly increasing complexity, fully exploiting the capabilities of university cleanrooms. However, the field is reaching the critical mass of technological developments that can be adsorbed from university laboratory in order to produce smaller, denser and more scalable quantum dot devices, especially on the silicon platform. This technological gap can be filled by semiconducting foundries, which have been involved in the development of smaller and better-performing transistors over the last few decades, reaching nanoscale technological nodes such that further miniaturization is mostly limited by quantum effects (detrimental for classical transistors, but essential for the implementation of spin qubits).
In the second part of this section, the working principle of the fully-depleted silicon-on-insulator nanowire transistors (FDSOI) devices fabricated at the CEA-LETI foundry in Grenoble will be introduced. The recent demonstration of hole-based spin qubits in these foundry-fabricated silicon-on-insulator (SOI) devices [38, 43] has energized the pursuit of similar structures with additional functionalities, such as the introduction of split-gate electrodes [105] for local control and top gates for global control (as demonstrated in this work). Such advanced structures have been used to obtain the results in chapters 5 and 6.

3.2.1 Si/SiGe device fabrication

We now introduce the fabrication of both single-gate-layer and overlapping-gate geometry quantum dot structures, analysing their respective advantages and disadvantages.
The material used is an undoped Silicon Germanium heterostructure, where

the electrons are induced in a strained silicon channel which acts as a square quantum well (as shown in Fig 3.2.1(a)), embedded in two layers of $Si_{0.7}Ge_{0.3}$. The growth of the material stack was performed by an external company[6], which implemented standard industrial MODFET (Modulation Doping Field Effect Transistor) techniques using an MOCVD (Metalorganic Chemical Vapor Deposition) chamber.

The substrate is a high quality silicon wafer[7], which hosts a graded buffer layer used to reduce the lattice mismatch between the unit cells of Si and $Si_{0.7}Ge_{0.3}$. The buffer is obtained by stacking material slabs with a graded silicon and germanium concentration, until the ideal ratio is reached. Then, an homogeneously layer of $Si_{0.7}Ge_{0.3}$ is grown for hundreds of micrometers. With this technique, it is possible to improve the quality of the 2DEG, since the potential inhomogeneities arising from atomic dislocations are confined away from the Si well. The top stack is composed by the quantum well itself, where the Silicon channel is encapsulated between the two layers of $Si_{0.7}Ge_{0.3}$. Due to the different bandstructure compared to silicon, $Si_{0.7}Ge_{0.3}$ behaves as the potential barrier for the quantum well. An important aspect when designing the correct heterostructure for the experiment, is to reach the ratio between the thickness of the silicon channel and the top $Si_{0.7}Ge_{0.3}$ layer. In fact, the thickness of the quantum well defines the quality of the quantum well, therefore the mobility of the 2DEG. For too thick Si wells, threaded dislocations would arise in Si, inducing additional scattering sources, limiting the electron mobility. On the other hand, too thin Si channel would not lead to a homogeneous layer[8]. Analogously, the top buffer layer has to be chosen such that the thickness would still allow a sufficiently high gate lever arm (therefore a thin layer would be ideal). At the same time, the top buffer layer, has to offer a high quality potential barrier, in order not to allow the electrons to leak to the surface from the quantum well. Following these constraints, the community consensus has empirically settled on a Si/SiGe thickness around

[6] Lawrence Semiconductor.
[7] 4 in. wafers purchased from TOPSIL.
[8] An extensive discussion about strain engineering can be found in [106].

8-10/35-50 nm. In this section and in the next chapter, the material that has been used has a 12/40 nm Si/SiGe ratio .
The in-house fabrication flow that has been developed for quantum dots devices on Si/SiGe can be divided into two steps: the first one deals with the preparation of the substrate and the subsequent one with gate layer fabrication. The complete fabrication steps are shown in appendix A.

Substrate preparation

Most of the substrate preparation is aimed at the realisation of good ohmic contacts, essential to provide electrons from the external world to the devices, as a consequence of the undoped nature of the heterostructure. In order to realise ohmics, well defined windows designed using optical lithography are opened on the surface of the sample, forming the mask that is active during the exposure to a high energetic P^+ ion beam. Ion implantation aims to degenerately n-dope the silicon substrate in order to modify the band structure of the exposed area, such that the conduction band bends below the Fermi energy, resulting in the formation of a metallic area. In order to evaluate the right amount of ion dose required to obtain an ohmic contact, we simulated the process using the *SRIM* software[9] (simulations are reported in appendix A). For the material used in this work, we used at ion dose of 10^{15} cm–2 deposited at two intensities, 30 keV and 15 keV. The first deposition is aimed to generate a good ohmic region at the quantum well depth, whereas the second intensity creates good ohmic contacts at the surface of the material[10]. Subsequently, the implanted samples undergo an annealing step in a Rapid Thermal Annealer (RTA) at 700 °C in a nitrogen atmosphere, in order to enable the restoration of any damage to the Si lattice. An example of ohmic contacts are shown in Fig. 3.2.1(b), where they are clearly visible under a scanning electron microscope (SEM) due to increased number of free carriers in the area. Ohmics

[9] http://www.srim.org/.
[10] Implantation performed from an external company, Kroko Inc., based in the United States.

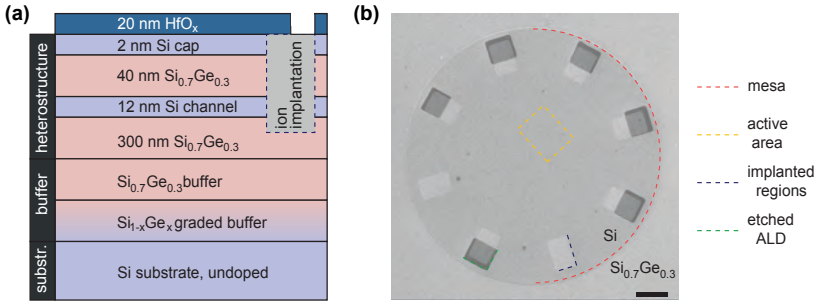


Figure 3.2.1 – Material platform and substrate preparation. (a) Si/SiGe heterostructure layers. The quantum well is formed in top Si channel, using band-gap engineering approach. (b) Fabricated substrate, ready for metal gate deposition. Scale bar 30 μm. The area presented shows one of the mesa regions on one chip, where eight P^+ implanted region are visible and 6 of them has been etched to host ohmic contact lines.

are designed to be confined to a small portion of the chip, close to the active area of the chip where the quantum dot structures are going to be fabricated. This minimises the additional capacitance induced from the accumulation top gates, which is detrimental for reflectometry-based readout, as it is discussed later.

After the ohmics step is completed, we define mesas on the chip, hosting the active area of the device as well as the ohmic regions. These regions are fabricated using dry argon (Ar) milling process in a high-vacuum chamber, removing approximatively 100 nm of material, as shown by the dashed red semi-circle in Fig. 3.2.1(b). This step allows to completely separate active device areas from each other, avoiding charge leakage between them. Simultaneously, it avoids the wire-bond breaching the bonding-pad to reach the underlying quantum well (which has been removed). This could otherwise induce intergate leakage. The last step is the deposition of a thin layer of high-quality insulator (either AlO_x or HfO_x) using an atomic layer deposition (ALD) process. This step is required to enable the accumulation of the electronic reservoir from the ohmic regions to the active area of the device, and the insulating layer has to partially overlap the ohmic region. We tried two different approaches: either

growing ALD in presence of a lithographic mask (adapted for the single-gate-layer devices) or uniformly growing the oxide layer, and subsequently etching it away around the regions of interest[11]. The first method allowed us to avoid the exposure of the substrate to additional chemicals, whereas higher quality oxide layers can be obtained using ALD deposition that is uniform across the chip.

Single-gate-layer geometry devices

The first generation of in-house developed devices is a single-gate-layer architecture, illustrated in Fig. 3.2.2. As shown, this geometry inherits its design features directly from gallium arsenide technology, where only one gate layer of depleting gates is required to from quantum dots, owning to the doped nature of the AlGaAs/GaAs heterostructure. The accumulation gates that are used to populate the quantum well are visible in Fig. 3.2.2(b) and (c), where they partially overlap the implanted regions and continue to the device, as visible in the four large-area leads Fig. 3.2.2(d) and (e). The two sides of the accumulation gate were intentionally disjointed in the design file in order to avoid electrostatic discharge (ESD) issues, while still allowing the accumulation of a single channel by applying a common voltage to the two gates. The thin gates in Fig. 3.2.2(d) and (e) are used as side gates in depletion mode, in order to fine-tune the chemical potential of the quantum dots as well as the tunnel coupling between the quantum dots. Finally, the elongated middle gate is used to tunnel-decouple the two sides of the device, such that the side with a single quantum dot can be exploited as a charge sensor, capacitively coupled to the qubit array on the facing side.

Gate fabrication is divided into two stages, both performed using Electron Beam Lithography (EBL)[12]. During the first step, the inner gates reported in Fig. 3.2.2(d) and (e) are fabricated using the cold-development technique[13] as

[11] We used buffered HF to etch HfO_x and transeneD to etch AlO_x.
[12] EBL was performed using ELS-F100, a 100 keV system from Elionix inc.
[13] This technique relies on PMMA development in water-IPA at low temperatures [107].

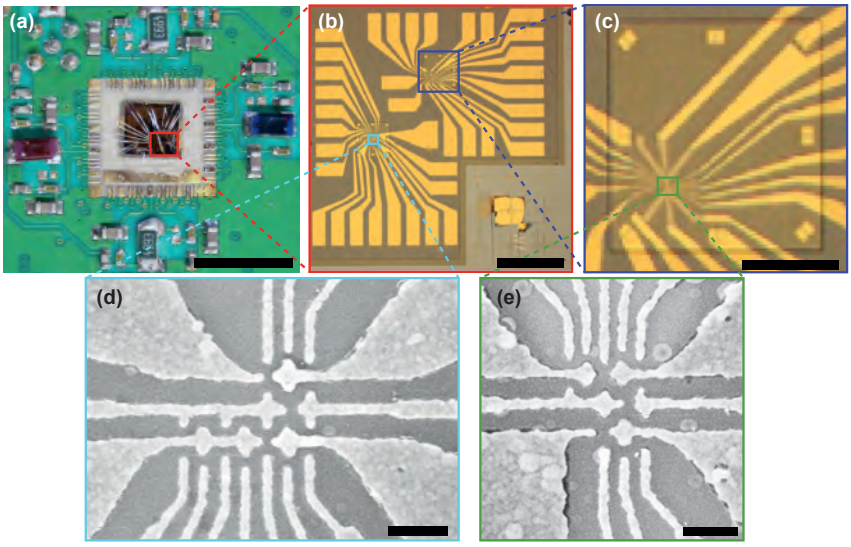


Figure 3.2.2 – Single-gate-layer geometry device fabrication. (a) Device chip wire-bonded to a PCB sample holder. The chip measures 4x4 mm and hosts eight independent device mesas. Scale bar 8 mm. (b) Optical micrograph showing two 250x250 μm device mesas, each connected to large rectangular wirebonding pads. Scale bar 500 μm. (c) Close-up of one mesa. Near the corners and edges of the mesa, eight regions of ion implantation are visible (gold double squares), which form ohmic contacts to the silicon channel. Scale bar 100 μm. (d) and (e) Scanning electron micrograph of a triple and double QD device, showing four large-area accumulation gates and skinny depletion gates, respectively. Scale bars 200 nm.

reported in appendix A, and metallized using a deposition of Ti/Au, where the Ti is used as sticking layer. Subsequently, the outer layer of gates (which starts where the gates change colour in Fig. 3.2.2(c)) is fabricated using standard development recipes. During the metallization of this step, a thicker layer of Ti/Au is deposited, in order to obtain an uniform film as the gates cross the mesa structure. Fig. 3.2.2(a) shows a typical chip that is fabricated, with a 4x4 mm^2 area, used to host single, double and triple dot devices (Fig. 3.2.2(d) and (e)).

Overlapping-gate geometry devices

The fabrication of these single-gate-layer devices has proven to be relatively easy to implement. While enabling fast turn around of devices (extremely useful in a university environment) as well as eliminating intergate leakage, single-gate-layer fabrication has not been fully effective in showing the reproducible formation of quantum dots with well-controlled tunnel-couplings, as discussed toward the end of chapter 4. In recent years, consensus has built over the need to gate the entire heterostructure surface in the active region to avoid non-uniform strain, as well as the need for dense gating due to the larger effective mass (and smaller required dot size) in silicon. Following state-of-art device fabrication advances [37, 53], we moved toward the implementation of overlapping-gate devices. Unlike the previous geometry, these new nanostructures are fabricated using three layers of overlapping Al gates, as shown in Fig. 3.2.3, in order to achieve a better confinement and control of the electronic wavefunction. Similar to the previous procedure, the fabrication is divided into two stages, but the order is now reversed. Initially, the outer gate layer is fabricated using standard EBL lithography processes, and metallized by depositing a layer of Ti/Au, thicker than the mesa height as before, as shown in Fig. 3.2.3(a) and (b). During metallization, the device is tilted with respect to the normal material evaporation direction as well as placed on a rotating substrate, in order to yield outer gates terminated with a slope instead of a sharp edge, such that the inner gates can be laid down as a single and uniform metallic gate. Furthermore, during the deposition of the outer gates, the pads are all shorted together in order to avoid charging of different gates during the fabrication process, avoiding ESD shocking of the devices during fabrication, bonding and loading into the sample holder[14] (the short is then removed using a grounded tungsten tip as the chip is bonded and grounded on the sample holder next to the fridge, just before loading). Despite the usefulness of this technique, the elongated parallel gold-lines might become source of unwanted

[14] This dramatically improved the yield of devices with no intergate leakage to 100%.

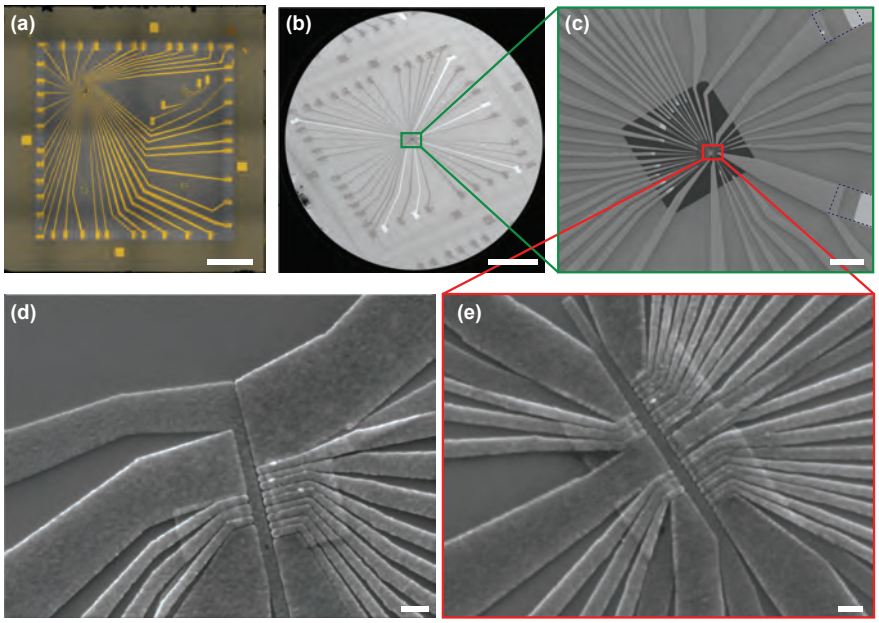


Figure 3.2.3 – Overlapping gate geometry fabrication. Device chip for overlapping gate geometry. The chip measures 5x5 mm and hosts only one device. The thin outer connectors are used as a short between all the gates to avoid blowing up of the devices due to ESD during fabrication. Scale bar 1 mm. (b) Scanning electron micrograph of similar device displayed in (a). Ohmic contacts are brighter due to the absence of ALD underneath them Scale bar 1 mm. (c) Zoom-in around the device region. The darker area represent the region where the ALD has been etched. Dashed blue area represent the implanted regions. (d) and (e) overlapping gate devices. (e) is a 4 QD + 1 sensor dot which is used as unit cell. In (e) two unit cell are connected via an ohmic that can be turned into a multielectron quantum dot.

cross coupling between different gates as fast pulses are implemented. Therefore, in future, proper engineering of the shorting fence has to be implemented. Fig. 3.2.3(c) shows a zoom-in of the active device region, where the oxide has been etched away in order to theoretically reduce the charge noise arising from the ALD layer[15].

[15]In doing so we would rely on the Schottky barrier between the gates and the quantum well, which could still be enough for sufficiently low gate voltages. Unfortunately we did not

During the second step the inner gate layers are fabricated, using the cold development technique previously mentioned. Two designs of the inner gate structure are reported in Fig. 3.2.3(d) and (e), with a 4 QD device and an 8+1 QD device, respectively. As previously mentioned, these devices are composed of three gate layers (corresponding to three different fabrication steps) that are aligned to 20 nm[16], as shown, since the gate pitch is 80 nm. In order to achieve these results, great care is taken in the positioning of the alignment markers, which are metallized with 5/100 nm of Ti/Au, offering enough contrast to enable the machine to perform automatic alignment, reaching a pixel reproducibility below 10 nm[17]. After each lithography step, the layer is metallized using aluminum (18 nm for the first layer and 35 nm for the remaining two) and the sample is heated up to 185 °C on a hotplate in a cleanroom environment in order to enhance the thickness of the native oxide. Using this technique, inter-gate leakage above 2 V has been reproducibly observed[18]. The working principle of these devices is very similar to the one presented in section 3.2.1, with the main difference lying in the top gating effect of the thin gates compared to the previous side gating effect. The first layer (shown in yellow in Fig. 3.2.4(a)), also called the screening layer, has two different functions: it is meant to screen the effect of the accumulation and plunger gates, in order to allow the formation of dots in the unscreened region only, and, at the same time, it is used to tunnel decouple the sensor dots (via the backbone gate) from the quantum dot array. Furthermore, it is also meant to release the strain at the surface of the device (given its flatness) avoiding the formation of unwanted trapping potentials that could lead to the presence of unwanted quantum dots. The second layer (shown in green in Fig. 3.2.4(b)) is the accumulation and plunger gate layer. The large-area leads fulfill the same task as for the previous gate architecture. The additional green thin gates are the

have the chance to test whether the barrier offered from our material would be high enough to allow accumulation avoiding leakage.

[16] The nominal alignment of the machine is 20 nm!

[17] Additional care is also taken by waiting for stage of the machine to thermalise and making sure that the chip is as flat as possible once positioned on the stage.

[18] However, we do not have any knowledge about the charge noise quality of this oxide.

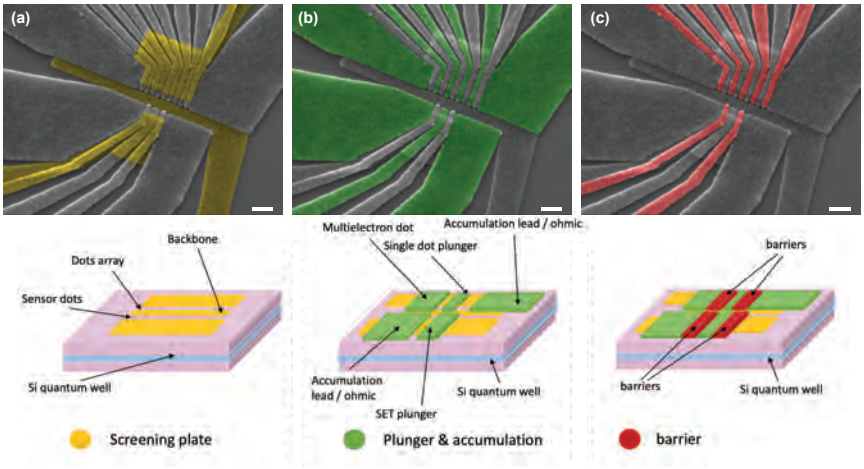


Figure 3.2.4 – Overlapping gate geometry devices. (a) The first layer (yellow) is the screening gate layer, meant to both screen the effect of the plunger gates away from the accumulation region as well as to tunnel decouple the sensor dot array from the single quantum dots channel. (b) The second layer (green) is the accumulation and plunger gate layer, which is used both to create an electrical contact between the implanted regions and the area where the device is located (via the bigger green leads) and to independently control the chemical potential of each QD (via the smaller gates). (c) The last layer (red) is the barrier gate layer, which allows to control the tunnel coupling between the quantum dots themselves as well as with the electronic reservoirs.

plunger gates, which control the chemical potential of each single dot. Finally, the last layer (shown in red in Fig. 3.2.4(c)) is intended as the barrier layer, and is used to control the tunnel coupling between the quantum dots themselves as well as between the external QD and the reservoirs.

3.2.2 Foundry-fabricated devices

The devices introduced in section 3.2.1, represent the most advanced silicon quantum dot device architecture that has been recently used to demonstrate the shuttling of a single-electronic charge across 9 quantum dots [51] as well as the control of single spins in a 4 dot device [79], an extremely important first step towards the implementation of many-qubit experiments in silicon quantum

dots. Despite these technological developments, the realisation of such devices has proven to be very challenging in university cleanrooms, especially if the infrastructure is not optimized for Si fabrication. Furthermore, the fabrication flows presented in section 3.2 are both based on liftoff techniques, processes that are highly non CMOS compatible and therefore not scalable. Exploring more scalable fabrication processes would be highly beneficial for the development of this platform.

Over the past decades, CMOS research has been developing denser, smaller and more scalable transistors in order to be able to supply the computing industry (and more) with increasingly powerful machines to satisfy consumer demand. Recently, finFET transistors have reached the 7 nm technological node [1], practically ending the evolution of Moore's law. In fact, trying to develop smaller transistors would lead to unwanted quantum phenomena, detrimental for the functioning of classical computers. Luckily, this represents an ideal playground for the spin-qubit community. Relying on the high quality and fully CMOS compatible silicon fabrication developed by the semiconducting industry, very compact quantum dots confined in the channel of nanoscale transistors can be produced using scalable processes, yielding an incredible number of devices in a single fabrication run (especially when implementing the 300 mm fabrication platform). Chapters 5 and 6 of this thesis are performed on foundry-fabricated devices, also known as fully-depleted silicon-on-insulator nanowire transistors (FDSOI), shown in Fig 3.2.5, produced at the CEA-LETI foundry in Grenoble[19] [105].

FDSOI device fabrication

The fabrication flow has been entirely developed at the LETI foundry, therefore only the necessary knowledge to understand the main structure of these

[19]These devices were measured within the European collaboration MOSQUITO. The author wishes to thank Silvano De Franceschi and Louis Hutin for having made this collaboration possible, as well as all the members of the consortium for useful discussions. The author wishes also to thank the CEA-LETI team for having developed the fabrication flow.

devices is given[20]. Fig 3.2.5(a) reports a schematic of such devices, which presents some advancements compared to the first generation of similar FD-SOI devices [108] as well as the main dimensions of interest when designing such devices. These devices consist of an undoped silicon nanowire channel

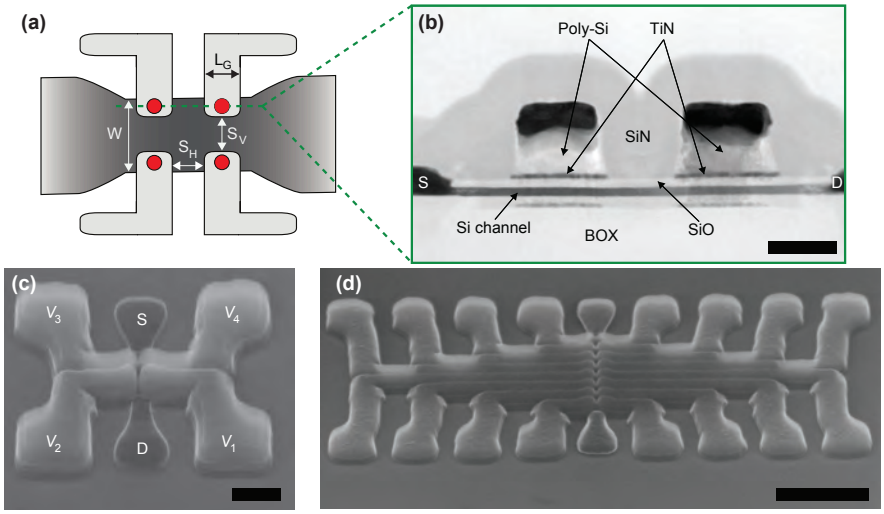


Figure 3.2.5 – Foundry FDSOI devices. (a) Schematic of a 2x2 split-gate device. Red dots indicate the position where quantum dots would expect to be accumulated. Arrows indicate the devices main geometrical dimensions. (b) Cross-sectional TEM image of a device similar to the measured in chapters 5 and 6, taken along the channel as shown from the dashed green line in (a). Scale bar 50 nm. (c) Tilted SEM image of a similar quadruple QD device after gate pattering and spacer deposition, similar to the one measured in chapters 5 and 6. Scale bar 200 nm. (d) Micrograph of a 16 quantum dot device fabricated using the same FDSOI technology. Scale bar 500 nm.

(in dark grey) with a thickness of 7 nm, connected to degenerate n^+ doped regions which act as ohmic contacts. Two pairs of split-gate electrodes (in light grey) are deposited on top of the device, and are used to control the quantum dots' potential, identically to the accumulation layer in Fig 3.2.4(b). For the

[20]The full fabrication flow, starting from the undoped silicon substrate, is composed from more than 200 steps.

device investigated in chapters 5 and 6, the effective dimensions as marked on Fig 3.2.5(a) are: W = 70 nm and $S_H = S_V = L_G = 32$ nm. Fig 3.2.5(b) reports a cross-sectional Transmission Electron Microscope (TEM) image (with inverted colours) along the axis of the silicon nanowire, highlighting the advanced technological fabrication. The QD gates are made of a thin layer of TiN in order to set a low threshold voltage, covered with highly doped poly-Si to ensure uniform behavior of the gates and separated from the Si channel by a thin layer of high-quality SiO_2. The ohmic contacts are shown on the further left and right of the image in darker colours. In order to protect the Si channel during the implantation processes, SiN spacers are deposited in the inter-gate regions as well as in between the gates and the ohmics. Finally, the silicon channel is sitting on top of a 145 nm thick silicon Buried Oxide (BOX), enabling the undoped silicon substrate to act as a backgate (in practice, below the silicon freeze-out temperature of around 22 K, this requires the shining of an LED). Fig 3.2.5(c) and (d) show SEM images of a quadruple and a 16 quantum dot device fabricated by CEA-LETI, respectively. The latter represents one of the most advanced semiconductor quantum dot devices ever fabricated, doubling the QD density for an area similar to state-of-the-art lateral quantum dot devices [53].

During a later fabrication stage, 300 nm of SiO_2 is deposited, allowing the evaporation of a metallic Cu gate, which, as discussed later, is used to further control the electronic wavefunction overlap in the quantum dots (similarly to the barrier layer in Fig 3.2.4(c)), as shown in Fig. 3.2.6(a). Finally, 2 µm of encapsulation oxide is deposited in order to protect the devices, inherited from the standard CMOS back end fabrication.

Foundry-quantum-dot control

Unlike the devices presented in section 3.2, the formation of quantum dots in FDSOI devices relies on the enhanced electric field that Poly-Si gates exert at the topmost corner of the Si nanowire, since they wrap around it [108]. This is also known as the “corner effect” in fin-FET transistors. In the devices studied

in this thesis the chemical potential of the expected quantum dots underneath each gate is controlled by the poly-Si gate voltage, whereas the TiN controls the threshold voltage. However, given the extent of the SiN spacers (thicker than TiN) it is possible to expect the presence of additional quantum dots forming underneath the spacers, induced by the effect of the Poly-Si gates.

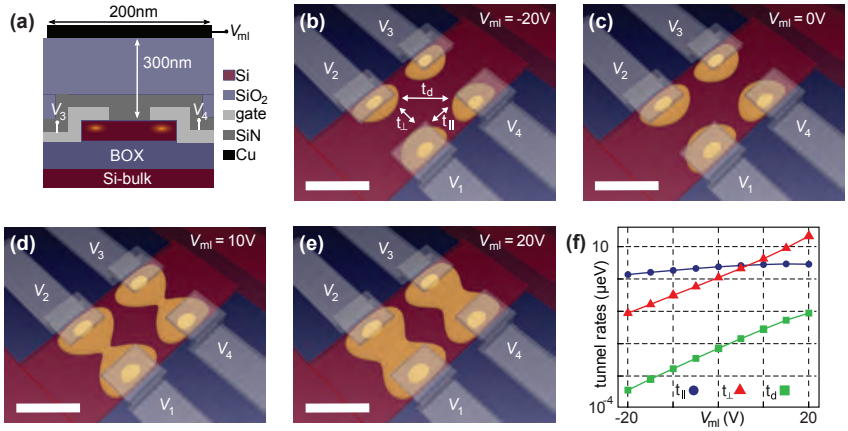


Figure 3.2.6 – Foundry FDSOI quantum dot tunability. (a) Schematic sketch of the back-end part of a split-gate FDSOI device, introducing the general metal line V_{ml}. (b)-(e) Simulated contour plots of computed ground-state electron wave function extension for V_{ml} = -20, 0, +15 and +20 V. Dark/light yellow colours represent iso-surfaces that correspond to 0.0025 and 0.5 of $|\psi|^2_{max}$ at $V_{ml} = 0$ V. See appendix B for more informations. Silicon in red ; TiN in gray ; BOX in blue ; other materials not represented. Scale bar 40 nm. (f) Simulated evolution of different tunnel rates as a function of V_{ml}.

Quantum dots obtained using these techniques have shown very high charging energies (three or four times higher compared to laterally defined quantum dots, in agreement with the assumption of small localized quantum dots), as well as very strong lever arms (in the order of 0.5) [43, 109, 110]. As already introduced, the FDSOI device studied in this thesis is reported in Fig. 3.2.5, and it is composed of a pair of split-gate electrodes, separated by spacers. Theoretically, the tunnel coupling between the quantum dots is dialed-in during fabrication, relying only on the spacers and the quantum dot separation (this

concept is further developed in the beginning of chapter 5). However, for this device, the presence of the additional Cu top metal line V_{ml}, enables the tuning of the tunnel coupling between the quantum dots as reported in Fig. 3.2.6(b) to (f).

Using a Poisson solver[21], the potential in the device is computed as a function of different V_{ml} in order to study the evolution of the quantum dot wavefunction for a single electron occupation for each single quantum dot (see appendix B for more informations). As reported, by moving the top metal line, the individual tunnel coupling strengths between the quantum dots are increased (in analogy to the concept introduced in section 2.1.3). The perpendicular tunnel coupling $t_\perp$ (with respect to the wire direction) as well as the diagonal coupling t_d show a "slow" but sizable dependence on V_{ml} due to the larger area covered by spacers. On the contrary, coupling between series dots $t_\parallel$ seems to be mostly unaffected, as a consequence of the strong screening of the metallic gates, much closer to each other along this direction. Furthermore, the absolute value of the tunneling strengths at $V_{ml} = 0$, where $t_\parallel \gg t_\perp > t_d$ is in agreement with a theory of the quantum dot wavefunction having a "cigar"-like shape [108], elongated in the direction of the nanowire, along the corner. The second inequality is accounted for by the longer distance between the perpendicular and diagonal quantum dots.

As a final remark, despite the powerful fabrication platform developed at CEA-LETI (and in general from semiconductor foundries), it is fair to acknowledge its limitations. As visible in all the devices presented above, and in literature [43, 75, 109, 110], only two types of device designs are available at the moment, the aforementioned split-gate design and the "pump" geometry, where the gates wrap around the channel in Ω-like shape [38]. These "catalog" limitations are imposed by the fact that foundry-fabrication processes are still not directly meant for such small devices, therefore devices have to be made by tweaking the already existing fabrication flows. As such, turnaround for these devices (especially if fabricated on a 300 mm platform) currently requires years,

[21] The author wishes to thank Yann-Michel Niquet and his group in Grenoble for useful simulations and discussions.

as well as large international consortia to fund these projects.

3.3 Readout techniques

As already introduced in section 2.2, decoding the state of a single spin has proved very challenging due to its small magnetic moment. Even though different techniques have been developed [76, 111], they do not meet the scalability criteria required to develop a fully functional spin-qubit quantum computer. The conversion of the spin texture to a charge signal has proven to be a simple, yet powerful, solution to readout the state of a spin qubit, building on decades of improvement in technology for electrical charge detections. However, despite the increased noise rejection performance that can be achieved using lock-in techniques, the minimum amount of current that can be detected is in the order of fA, which for quantum dot systems corresponds to tunneling rates in the order of 100 kHz. I most of the experiments, this corresponds to a regime where many electrons are allocated inside the quantum dot (for a reasonably long integration time). As the electronic occupation inside a quantum dot increases, the energy spectrum follows the same trend, increasing the leakage states for the qubit as well as hindering the application of the readout techniques introduced in section 2.2. Nevertheless, it is possible to make the barriers less opaque to access the few-electron regime, at the price of reduced performance of the qubit [22, 73]. On the other hand, similarly to filled electronic shells in atoms, filled electronic shells in quantum dots show an inert behavior. Consequently, the spin properties of the first additional electron to such filled shells and single electrons trapped in quantum dots are similar. This has enabled the coherent manipulation of spins in multielectron quantum dots, without directly adjusting the tunneling barriers [38].
In order to perform single electron control to implement the qubits introduced in chapter 2, it is necessary to reach total control over quantum dots in the few-electron regime. An optimal solution has been found in the implementation of proximal charge sensors to the qubit dots, nanostructures such as quantum point contacts [112] or single electron transistors (SET) [113, 114],

capacitively coupled to the qubit. These sensors rely on the sensitivity of their conductance to the nearby environmental charge distribution. The conductance of the SET can now be probed using lock-in techniques (since the SET works in the many electron regime), reaching high fidelity readout of quantum dots in the few-electron regime, since the technique is not directly sensitive to tunneling rates anymore, but absolute charge occupation only. Nevertheless, given the theoretical prediction of the channel conductance for these platforms of the order of 1 quantum of conductance [66], the RC rise times in these systems are limited to few kHz, a bandwidth too narrow for real-time monitoring of spin-qubit events [77] (especially in GaAs, where these techniques were first implemented). This has led to the development of higher-bandwidth readout techniques, such as RF-reflectometry, which combined with charge sensing offers an ideal readout platform for spin-qubit experiments [114, 115]. As discussed in the following paragraphs, they rely on the study of the reflected power from an LC oscillator (which has its resonance frequency typically in the MHz regime) loaded with the sensor impedance. Fig. 3.3.1 shows an electrical circuit as well as a lumped element circuit for the RF-SET in panel (a), as well as for gate-based dispersive readout in panel (b).

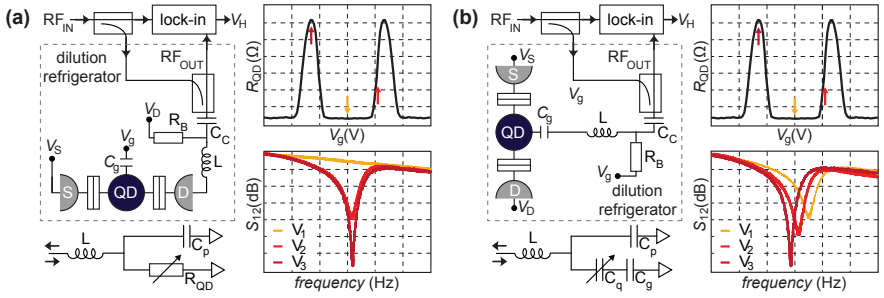


Figure 3.3.1 – Reflectometry setups. (a) and (b) Sketch of the electrical circuit for the implementation of the reflectometry setup (see Fig. 3.1.1(b) for component position inside the dilution system) as well as the lumped element circuit diagram for RF-reflectometry and gate-based dispersive readout, respectively. On the right sides, matching condition for the resonant circuit as a function of the impedance of the quantum dot (QD).

Nevertheless, it is worth mentioning that using charge sensing techniques, it has been recently demonstrated that the quality factor (number of coherent oscillations over gate time) of a Loss-DiVincenzo qubit operated in the 5-electron regime (therefore in the p-orbital for a 2D atom) is enhanced compared to operations using the last electron [116].

3.3.1 RF-reflectometry and charge sensing

Fig. 3.3.1(a) introduces the setup used to perform RF-reflectometry measurements. A drive signal propagating trough a series of directional couplers reaches an LC resonator circuit loaded with the impedance of a quantum dot (which can be assumed to be mostly a resistive element). The reflected power (dependent on the matching condition) is then recombined at RT with the original signal, enabling homodyne detection, yielding the DC signal V_H. The percentage of reflected power (Γ) at the LC resonator depends on the deviation of its impedance from the Z_0=50Ω of the coaxial line:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{3.1}$$

As emphasized in the formula above, if the impedance Z of the resonant circuit deviates too much from Z_0 the technique becomes insensitive to the loaded element, since the reflected power would be constant, independent of the value of Z. Therefore in order to optimize the working regime, it is necessary to evaluate the value of Z for the system under consideration. For quantum dot devices, as previously introduced, the loaded impedance associated to the resistive element is in the order of one quantum of conductance, R = 25 kΩ. As a general rules, these circuit are operated in the hundreds of MHz regime, where the effective dimensions of the resonator is very small compared to the drive wavelength, enabling a lumped element description and facilitating the realisation of the impedance matching condition[22]. In this limit, the resonant

[22]When considering resonators with dimensions comparable with the drive wavelength, a distributed element description has to be introduced, since the phase contributions are not negligible anymore, leading to non-constant voltages and currents across the circuit. This

circuit is formed from the inductor L and the parasitic capacitance of the circuit to any nearby ground, which, for the setup presented in Chapter 4, we estimated to be 1.5 pF. By evaluating the overall impedance of the circuit at the resonance frequency of the circuit ω_0, we extract the matching condition [114, 117]:

$$\Gamma = \frac{L}{RC_p} \text{ with } \omega = \omega_0 = \frac{1}{\sqrt{LC}} \tag{3.2}$$

yielding inductances between 300-1200 nH for the parameters previously specified. As reported on the right side of Fig. 3.3.1(a), when the circuit is driven at ω_0, the reflected power is strongly dependent on the impedance of the quantum dot, yielding a large variation of the reflected power for a small variation of the SET impedance. Inductors are surface mount devices (SMD) element [114, 118], which have dissipative components leading to a reduction of the quality factor of the resonator (visible in Fig. 3.1.1(c)). To obviate this inconvenience, superconducting spiral inductors have been developed, drastically increasing the quality factor of the resonator [119]. RF-readout circuit elements are usually loaded with the impedance of charge sensors, enabling nanoseconds-resolution measurements of spin-qubit systems in the few-electron regime, as reported in Fig. 3.3.2.

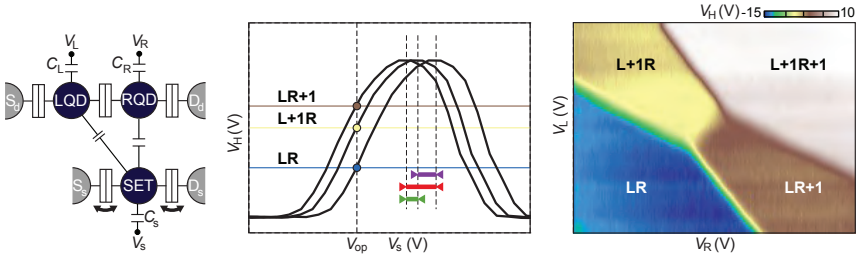


Figure 3.3.2 – Charge sensing. (a) Circuit diagram of a double quantum dot with a proximal capacitive coupled charge sensor. (b) Coulomb peaks of the SET as a function of the double quantum dot occupation. (c) Double quantum dot charge stability diagram read out via the demodulated voltage V_H from the charge sensor.

would be the case in the GHz regime.

In an experiment the SET is capacitively coupled to a DQD and tunnel coupled to its source and drain (the latter connected to the rf circuit), and the SET is biased on the side of one of its Coulomb peaks, as shown in Fig. 3.3.2(b). As the DQD is in a fixed charge configuration (L,R) (represented by the peak with the blue dot), the demodulated voltage V_H stays constant. As the electronic occupation is rearranged in the DQD, the Coulomb peak of the SET is shifted in gate voltage space due to capacitive effects, moving the readout point to either the yellow of brown dot, depending if an electron tunneled into the left or right dot. By moving the plunger gates in a small region across the interdot transition of the DQD (such that the cross capacitances do not move the readout point too far away from V_{op}), it is possible to obtain a charge stability diagram as in Fig. 3.3.2(c).
When positioning the charge sensor close to the device under study, it is necessary to arrange the overall capacitances between the sensor and each individual dot asymmetrically, such that tunneling between the two different QDs can be distinguished. For example, placing the sensor exactly in the middle of the two dots, would yield a charge sensor sensitive to overall charge inside the DQD, but unable to distinguish interdot charge movement.

3.3.2 Dispersive readout

RF-reflectometry charge sensing has proven to be a key technique to demonstrate many of the fundamental milestones necessary to lay the foundations for the development of a spin-qubit quantum computer [21, 26, 32, 33, 35, 77]. However, a fully functional quantum machine will require millions of qubits, which might translate to an even higher number of quantum dots, necessitating the presence of additional readout sensors. This translates into a huge overhead in terms of cooling power at the mixing chamber of the dilution unit as well as control electronics. Gate-based dispersive readout could harness the benefits of RF-SETs, while simultaneously reducing the overheads related to cooling power as well as control electronics [120, 121]. In fact, when implementing dispersive readout, the sensor becomes one of the quantum dots already

involved in the processor, without the requirement of additional ohmics and electrical control lines [43].

This readout technique has been successfully harnessed for many years by the superconducting qubit community [10], but only recently it has been demonstrated on the semiconducting platform [86, 122]. For these systems, dispersive readout is probed by embedding the plunger gate of a quantum dot into the resonant LC circuit, as showed in Fig. 3.3.1(b). However, as shown from the lumped element circuit, the resonant circuit is now loaded with the constant C_g, arising from the geometrical capacitance, as well as the variable capacitance C_q, which is dependent on the state of the quantum dot itself [123, 124]. By performing the calculations, it is possible to obtain that the quantum capacitance of the system is proportional to the second derivative of the density of states, as follows:

$$C_q = -(\alpha e)^2 \frac{d^2E}{d\varepsilon^2} \tag{3.3}$$

where α is the lever arm parameter and e is the electron charge. This can also be seen as the electromagnetic wave reflected at the quantum dot gate being modulated by the change in the electrical susceptibility of the quantum dot. In order to achieve strong response from the quantum dot, a relatively high lever arm of the gate is required, which has been achieved using silicon CMOS devices [61, 62], carbon nanotubes [125] and nanowires structures [126]. The right side of Fig. 3.3.1(b), reports the evolution of the reflected coefficient as a function of the variation of the admittance of the quantum dot. As displayed, and discussed later, the admittance variation in the matched regime has both a capacitive contribution, responsible for the shift in the resonance frequency of the oscillator, as well as a dissipative contribution. As it can be inferred, this readout method is sensitive to both interdot and quantum dot-to-lead transitions which directly involve only the dot embedded in the circuit.

Quantum and tunneling capacitance detection

The study of the polarizability of quantum dots has been extensively investigated in two and three dimensional systems and it has been well understood

in terms of the Sisyphus resistance as well as quantum and tunnelling capacitances [61, 127]. Considering a single quantum dot system at its highest polarizability point (i.e. where the electron level is aligned with the reservoir), the RF excitation is able to drive inelastic electronic tunneling, changing the average occupation of the quantum dot. Fig. 3.3.3(a) reports in detail the evolution of the two different charge states as a function of an external parameter (in this case the position of the DC voltage controlling the chemical potential in the dot, as shown in the inset of Fig. 3.3.3(b)). As the two levels

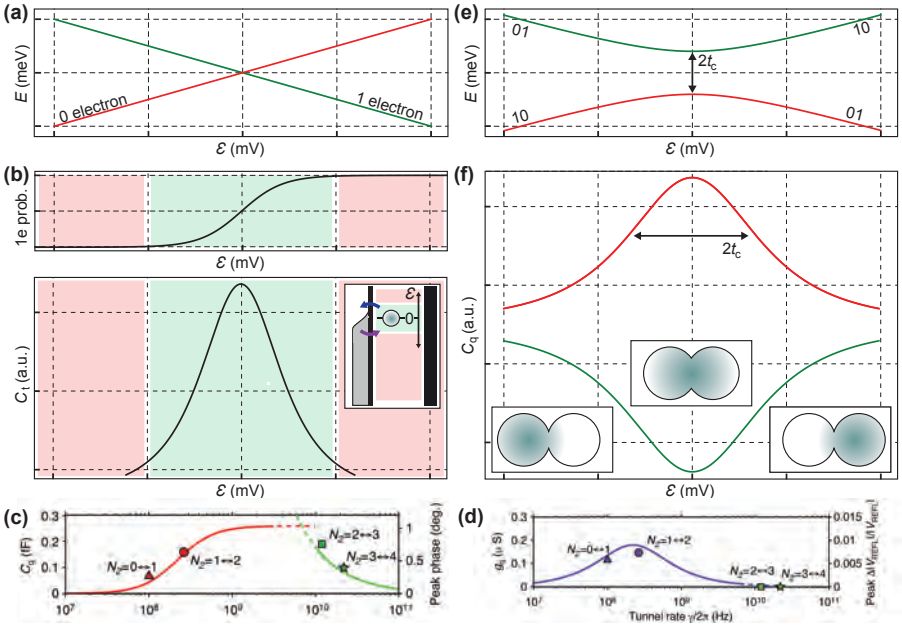


Figure 3.3.3 – Dispersive readout. (a) Energy diagram for a single electron being loaded into a quantum dot. (b) Density of states of the lead at a fixed temperature. It directly represents the probability of loading the electron into the dot. Quantum capacitance proportional to the tunneling capacitance of the electron. (c) Energy diagram for a double quantum dot in the occupation 01-10. (d) Quantum capacitance associated with (c) as well as double dot occupation as a function of detuning (in the insets). (e)-(f) Adapted from [128]. Quantum capacitance and quantum conductance of as a function of frequency.

are degenerate (at $\varepsilon = 0$), the polarizability of the system is the highest, which translates to a probability of the electron being 50% of the time in the lead and 50% of the time in the dot, as shown in Fig. 3.3.3(b), top panel. The excess dissipated energy drives the variation in the reflected power, which shows as additional tunneling capacitance C_t, which can be obtained by solving a master equation [129, 130], yielding:

$$C_t = -(\alpha e)^2 \frac{dP}{d\varepsilon} \tag{3.4}$$

where P is the probability of the electron being in either the lead or the dot. The result is reported in Fig. 3.3.3(b), bottom panel; a change is induced in the phase of the reflected signal, which can be evaluated as $\Delta\Phi \propto Q\Delta C/C_t$. The exact shape of the signal depends on the ratio between the tunneling rate of the electron (Γ) compared to he frequency of the excitation (ω_0), as well as the temperature of the system. Interestingly, in the limit of $k_B T \gg \hbar\Gamma$, the demodulated peak can be used as a on chip thermometer, since the lineshape is proportional to the temperature of the system. On the other hand, when the opposite limit is reached, the peak is broadened only by the lifetime of the transition, allowing to extract the elastic tunneling matrix element [129, 131]. As reported in Fig. 3.3.3(c) and (d), it is also possible to extract the evolution of the quantum capacitance and conductance starting from the admittance of the quantum dot, $Y = g_c + i\omega C_q$ [123, 128], yielding:

$$g_q = A\frac{q_e^2}{4k_B T_e}\Gamma\left(1+\frac{\Gamma^2}{\omega_0^2}\right)^{-1}\cosh^{-2}\left(\frac{\Delta\mu}{2k_B T_e}\right) \tag{3.5}$$

$$C_q = A\frac{q_e^2}{4k_B T_e}\left(1+\frac{\omega_0^2}{\Gamma^2}\right)^{-1}\cosh^{-2}\left(\frac{\Delta\mu}{2k_B T_e}\right) \tag{3.6}$$

where $\Delta\mu$ is the difference between E_F and the chemical potential of the dot and e is the electron temperature. As the formulas imply, the bandwidth of detection of the transitions is strongly conditioned by the ratio between ω_0 and

Γ. In fact, as the tunneling rate of the electron becomes much slower than the probing tone, the system does not show any sizable polarizability effects within one period of the excitation tone. In the other limit $\Gamma \gg \omega_0$, the contribution to the admittance is purely capacitive, meaning that the transition happens out-of-phase with respect to the drive. As a consequence, the tunneling is an elastic event and there is no dissipated power.
When considering interdot transition between two quantum dots, the working principle is similar. When considering a single electron in a double quantum well, the signal arising from the dispersive readout is at its maximum when the electron is delocalized between the two sites, as reported in Fig. 3.3.3(e) and (f). Fig. 3.3.3(e) shows the energetic state distribution for a double quantum dot in presence of tunnel coupling, and owning to equation 3.3, the maximum C_q is measured at detuning $\varepsilon = 0$ (with reference to Fig. 2.1.3(c)). A full mathematical derivation can be performed using the Jaynes-Cummings Hamiltonian, as done in [117]. This technique proves itself to be very powerful also when investigating Pauli spin blockade. In fact, as the magnetic field is increased, the triplet state becomes the ground state of the system, leading to the vanishing of the dispersive signal, owing to equation 3.3, where E is now linear in ε [109, 128]. In general, this technique being sensitive to only the electrons that are polarizable, is not directly sensitive to the charge occupation of the quantum dot, but only to the tunneling events that happens into and out from the dot.
Recently, a huge effort has been applied by the spin-qubit community in realising hybrid circuit quantum electrodynamics (cQED) systems, where semiconductor and superconductor technology are merged together, to overcome some of the limitations of spin qubits, such as the extreme locality of the qubit. Coplanar waveguide (CPW) cavities have been harnessed to developed readout schemes where the CPW is used to investigate the occupation of the quantum dots, by exploiting the same polarizability principle introduced above [126, 132]. Recently, a strong coupling between a photon and the spin degree of freedom of the electron has also been demonstrated [44, 45, 47, 94].
In the beginning of this section, we stated that the power of this technique relies

on its compactness. However, by analysing its characteristics, it emerged that dispersive readout has some limitations as well: the reduced readout bandwidth with respect to electron tunneling rates, the insensitivity to the absolute charge in the quantum dot as well as the locality of the technique, being limited to the density of states of the quantum dot embedded in the resonator. Chapter 5 describes the development of a dispersive readout technique that overcomes some of these limitations.

4

Radio-Frequency Readout in Si/SiGe

In this chapter we are going to introduce the results obtained for quantum dots fabricated on the Si/SiGe platform. Initially, we discuss the performance of single-gate-layer devices using the fabrication introduced in section 3.2.1, analysing the ability to form single, double and triple dots. Subsequently, we analyse the ability to perform single shot readout of a single-electron spin, exploiting radio-frequency (RF) techniques, an essential element for the implementation of Loss-DiVincenzo qubits. We demonstrate the capability to resolve single events at 24 µs integration times. Despite the capabilities of such devices, they still lack reproducibility of quantum dot properties across different devices. In order to overcome these limitations, in the second part of the chapter, we introduce the results obtained on the fabrication of overlapping-gate devices, with the aim of obtaining more reproducible and controllable quan-

tum dots. The results presented in the first half of this chapter, have been published in the following scientific article: Fast Charge Sensing of Si/SiGe Quantum Dots via a High-Frequency Accumulation Gate, C. Volk *et al.*, *Nano Letters*, **19**, 8, 5628 (2019).

4.1 Single-gate layer Si/SiGe devices

As introduced in section 3.2, an important quantity which defines the quality of the Si/SiGe heterostructure is given by the ratio of the thickness of the top buffered SiGe layer and the quantum well. In order to quantify the quality of the material used in this study, we initially performed Hall bar characterizations, using a single-gate-layer device, as reported in Fig. 4.1.1(a) and (b). After some iterations, it turned out that for our platform, mesa etched Hall bars with ratio L/W=4 and fabricated using the same procedure introduced in section 3.2.1, equipped with a single metallic Ti/Au layer gave the best results. The results are reported in Fig. 4.1.1(c), yielding low-temperature mobilities of up to 10^5 cm^2/(Vs) at 20 mK, achieved for charge carrier densities around $5 \cdot 10^{11}$cm^{-2}. The sheet resistivity has been extracted to be approximately 1.6 kΩ/□. In order to perform these measurements, we optically populated

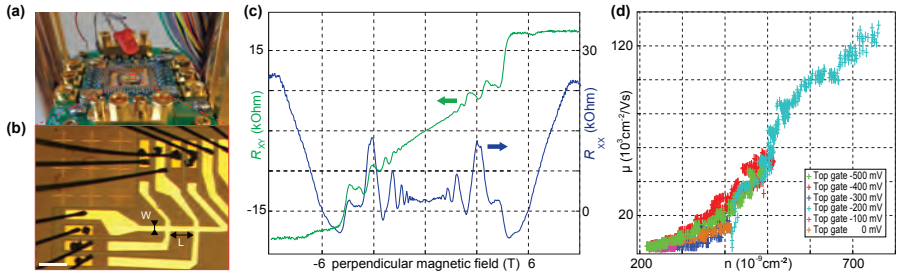


Figure 4.1.1 – Hall bar characterization. (a) Optical micrograph of the sample board hosting the Hall bar device. (b) Image of the Hall bar used to characterize the mobility of the electrons in the quantum well. Scale bar 250 μm and W/L=4. (c) Hall (green) and longitudinal (blue) resistance measured as a function of magnetic field at a fixed magnetic field. (d) Hall bar mobilities for different top gate voltages during the illumination process.

the quantum well using a red LED, visible in figure Fig. 4.1.1(a), which was activated for a short time, typically 10 seconds, at a fixed top-gate voltage at base temperature. Applying a negative top-gate voltage during the illumination step was found to move the accumulation threshold voltage to negative values, after the LED was turned off. Fig. 4.1.1(d) reports Hall bar mobilities for different electron densities in the quantum well, showing that their proportionality relation is unaffected by the top gate configuration during the illumination step.

4.1.1 RF-reflectometry setup

The strong capacitive coupling of the accumulation gate to the 2DEG changed the matching condition of the resonant circuit significantly and, in conjunction with the relatively large 2DEG resistance, impeded RF readout via the sensor's ohmic contacts, as commonly implemented in nanowires [133] and GaAs heterostructures [113].The reflectometry circuit is galvanically isolated from the heterostructure, by wirebonding the LC tank circuit to the accumulation gate of the sensor dot (L=1200 nH and C given by the stray capacitance as illustrated in Fig. 4.1.2. By decoupling the sensor's ohmic from the RF ground of the sample board, the reflected RF signal effectively becomes sensitive to the sensor's conductance, rather than only its quantum capacitance. To prevent the RF excitation from directly shunting to the RF ground of the sample holder, the sensor ohmic underneath the accumulation gate is connected via a high-impedance decoupling resistor to a DC gate voltage line (R=500 kΩ, see Fig. 4.1.2).

It is worth mentioning that by optimizing the device geometry, for example moving the implantation region closer to the device as well as reducing the dimensions of the accumulation top gate (i.e. reducing the additional capacitance), it is also possible to implement RF-reflectometry readout on the ohmic of a charge sensor placed near the qubit [31, 134, 135]. The PCB used in this experiment (reported in Fig. 4.1.2(a)) has some differences compared to the one described in section 3.1, such as the absence of a separable mother-/daughter-

board configuration. However, the reflectometry as well as bias-tee circuits

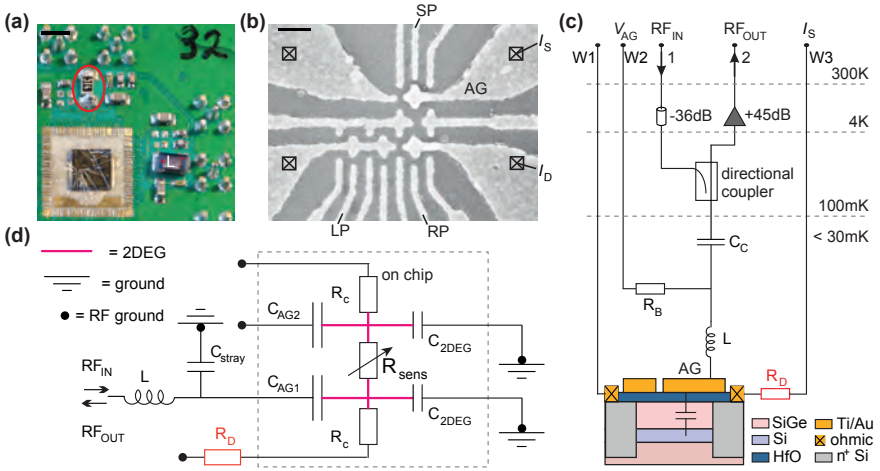


Figure 4.1.2 – Reflectometry circuit. (a) Silicon-germanium chip wirebonded to a PCB-mounted inductor (L), a decoupling resistor R_D (red circle), and conventional slow and fast signal lines. Scale bar 3 mm. (b) Scanning electron micrograph of a representative triple dot (plunger gates LP and RP indicated) with proximal charge sensor (plunger gate SP indicated). The accumulation gate AG is used for reflectometry, whereas four ohmic contacts (crosses) to the 2DEG allow measurements of sensor current (I_S) or device current (I_D). Scale bar 200 nm. (c) Simplified reflectometry schematic, showing how a RF carrier applied to the cryostat (port 1) excites the L-AG resonator. R_D decouples the RF from low impedance ground under the AG ohmic line. (d) Circuit schematic of the effective RF path on the PCB and on the chip, with RF grounds indicated by dots.

are the same as the schematic presented in Fig. 3.1.1(b) (see appendix B for a more detailed schematic, as well as part numbers). Fig. 4.1.2(b) shows an SEM image of the device studied in this chapter, which has been fabricated following the process presented in section 3.2.1. The AG gate indicates the accumulation top gate that is embedded into the RF circuit, and it was chosen to be the gate overlapping with the quantum dot's expected position (for the RF, the choice of a continuous AG gate from ohmic region to ohmic region, as well as the choice of the other accumulation top gate would have probably not led to the same result). A simplified schematic of the reflectometry readout circuit

is shown in Fig. 4.1.2(c), where, the surface-mount inductor (L) is wirebonded to the accumulation gate (AG) of the sensor, forming the tank circuit with the effective stray capacitance $C_{stray} = 1.2$ pF, summarizing contributions from PCB tracks, bond wire and metal tracks on the chip. The signal couples via the capacitance of the accumulation gate ($C_{AG1} \approx 2$–5 pF based on geometric estimation) to the underlying 2DEG. The 2DEG has a small unknown capacitance ($C_{2DEG} \ll 1$ pF) to nearby ground tracks, and a resistive connection to effective RF grounds (black dots in Fig. 4.1.2(d)) via the sensor quantum dot ($R_{sens} \approx 0.1$–0.5 MΩ) and a contact resistance ($R_C \approx 20$ kΩ, including contributions from the finite 2DEG resistivity and imperfect ohmic contacts). If the decoupling resistance R_D is chosen sufficiently high (in this experiment 0.5 MΩ), and if the admittance $2\pi f C_{AG2}$ is sufficiently high (where f is the carrier frequency and by design $C_{AG2} \approx C_{AG1}$), then the 2DEG RF excitation reaches the RF ground predominantly via the sensor dot resistance (i.e. the 2DEG part underneath the low-pass filtered accumulation gate, AG2, serves as a RF ground). Overall, this makes the reflected signal RF_{OUT} sensitive to changes in R_{sens}.

4.1.2 Single, double and triple quantum dots

Initially, a sensor dot is tuned up in the top half of the device shown in Fig. 4.1.2(b), using conventional DC transport measurements via wires W1 and W3. We increase the accumulation gate voltage until a conductive channel is formed, and then operate the barrier gates close to their pinch-off voltage to confine a quantum dot. Figure 4.1.3(a) shows a transport measurement of a Coulomb resonance of the sensor dot as a function of the plunger gate voltage. (In this configuration, we estimate that the resistance between one of the dot's barriers and the respective wirebonding pads is 20 kΩ, including ohmic contact resistance and finite resistivity of the 2DEG, i.e. a significant fraction of the applied bias voltage drops over the decoupling resistor.) Simultaneously, the demodulated voltage of the reflectometry circuit has been measured as a function of the applied RF frequency (Fig. 4.1.3(b)). The reflected RF power is

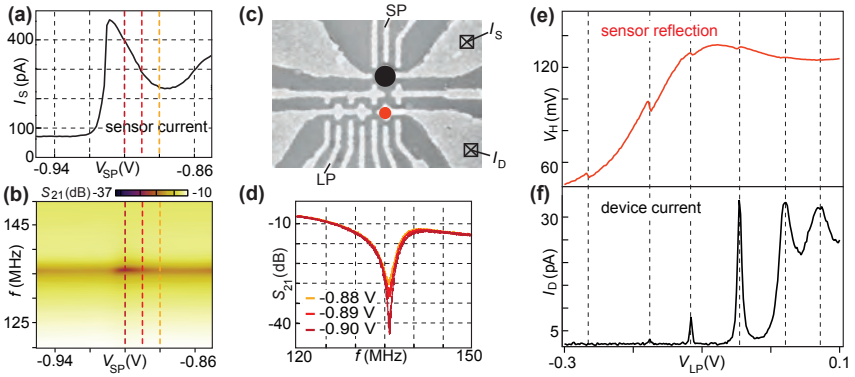


Figure 4.1.3 – Transport and reflectometry features of a single quantum dot. (a) Sensor dot current as a function of the plunger gate voltage V_{SP}, for fixed ohmic bias of 500 μV. (b) Scattering parameter from port 1 to port 2, S_{21}, as a function of V_{SP} and carrier frequency f. (c) Electron micrograph of the single quantum dot device. (d) $S_{21}(f)$ for the gate voltages indicated in (b), demonstrating near the 136-MHz resonance a sensitivity of the reflected RF signal to changes in sensor conductance. (e) Demodulated voltage V_H from homodyne detection at 136 MHz, as a function of the left-plunger voltage V_{LP}. (f) Simultaneous I_D measurements in the device's Coulomb-oscillations regime indicate that kinks in V_H result from charging events in the device.

strongly modulated by the conductance of the sensor dot. The minimum, where the resonant circuit is matched best, approximately aligns with the Coulomb peak. The resonance frequency stays constant indicating that the capacitive and inductive contributions to the readout circuit are not affected. Fig. 4.1.3(c) compares cuts through (b) at selected gate voltages, showing a resonance dip at 136 MHz. The reflected power at resonance changes by 12 dB, while the current of the sensor dot changes by 170 pA. By tuning the sensor dot to the flank of a Coulomb peak, the reflected RF amplitude becomes sensitive to the charge within the triple-dot channel. The RF frequency, power and phase are optimized for the best readout contrast. First, we tune up a single QD in the triple-dot channel (bottom half of Fig. 4.1.3(c)). A measurement of the sensor reflection demodulated voltage (V_H) as a function of the triple-dot plunger gate voltage is shown in Fig. 4.1.3(e). The signal shows steps in amplitude

that align well with the Coulomb peaks of the triple-dot device measured simultaneously in DC transport (Fig. 4.1.3(f)). Next, we demonstrate fast device characterization that takes advantage of the high bandwidth of our reflectometry technique. Figure 4.1.4(a) shows the charge stability diagram of a double QD in the low-electron regime (the device is shown in inset of the same figure). To speed up this acquisition, a 2-kHz saw-tooth pulse is applied to one of the plunger gates while stepping the other. The frequency is chosen to be larger than the cut-off frequency of the bias tee, but smaller than typical tunnel rates to avoid electron latching effects. This technique allows a high-resolution scan of charge stability regions within one second (for example Fig. 4.1.4(b) shows the (12), (22), (13), and (23) ground state regions), compared to acquisition times of several minutes using conventional DC transport measurements. At reduced resolution, video rate scans are possible, which facilitates the measurements significantly, especially allowing a "real-time" tuning procedure [136]. The charge stability diagram can be continuously monitored while adjusting other parameters, such as the tunnel couplings.

Detection of Pauli Spin Blockade

Our reflectometry technique also allows pulsed-gate measurements typically used in time-domain spin-qubit experiments, such as the determination of spin and charge dynamics. In order to determine spin life times directly, nanosecond-to-microsecond-long gate pulses are used, along with spin-to-charge conversion based on Pauli spin blockade, a common readout technique to distinguish between singlet and triplet states [109, 113, 137, 138]. To probe these effects in our devices, we apply a three-step pulse cycle to the plunger gates. First, the double QD is initialized in the (0,1) occupation (position I in Fig. 4.1.4(c)), followed by a pulse to the separation point (S) where an electron of random spin state is loaded from the reservoir. Readout takes place at the measurement point (M), located in the (02) ground state region. A (11) singlet state can relax into the energetically favorable (02) singlet state, whereas a (11) triplet state remains in (11) until a spin flip takes place, due

to Pauli spin blockade. By applying the RF readout tone only during the M step, the resulting (averaged) reflectometry signal distinguishes between the (02) and (11) charge states selectively during the M step, and thus provides information about triplet-to-singlet relaxation rates [113]. In Fig. 4.1.4(c), we

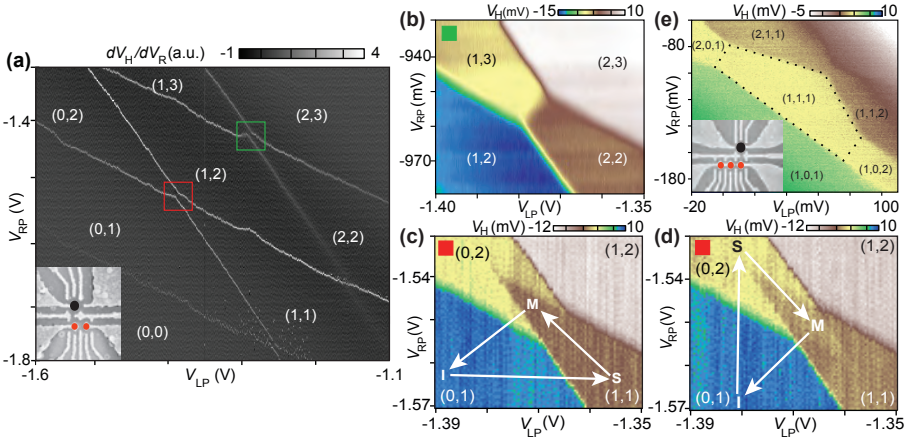


Figure 4.1.4 – Double and triple dot. (a) Charge stability diagram of a few-electron double dot device (derivative $\mathrm{dV_H/dV_{RP}}$ plotted for clarity). Numbers (n,m) indicate occupation of the left and right dot, respectively. (b) High-resolution zoom on the charge transition highlighted in (a), after tuning. Total acquisition time 1 s. (c-d) Three-step voltage pulses (arrows) are repeatedly applied to the left and right plunger gate, while slowly changing the DC voltages $\mathrm{V_{LP,RP}}$ such that $\mathrm{V_H}$ represents the average over many pulse repetitions. The M/I/S segments of the pulse are 5/1/1 µs long, with the RF carrier applied only during the M segment. (c) For counterclockwise pulse trajectories, a pulse triangle of (11) character appears in the region near "M", indicating that relaxation from Pauli-blocked (11) states to the (02) ground state exceeds 5µs. (d) For clockwise pulse trajectories, no reversed pulse triangle is visible, indicating the relaxation between (02) and (11) occurs at much shorter time scales. For better charge visibility in panels b, c, d, a plane fitted to (12) or (23) regions has been subtracted from $\mathrm{V_H}$. (e) $\mathrm{V_H}$ as a function of the left and right plunger gates, revealing the charge stability diagram of the triple dot device. Single-electron occupation of the three dots is indicated by a dotted line. A plane fit to the central region of (111) has been subtracted from $\mathrm{V_H}$.

record a charge stability diagram while repeatedly applying the pulse cycle described above. The brown region extending from the (11) ground state region

into the (02) ground state region (pulse triangle) shows that the system cannot immediately relax into the (02) ground state, indicating the presence of Pauli spin blockade. Thus, the duration of the M step (5µs) gives a lower bound for the spin relaxation time. In Fig. 4.1.4(d), we show a control measurement with an inverted gate pulse trajectory. Here, no such pronounced pulse triangle is visible, in agreement with the expectation that no spin blockade is present in the charge transition from (02) to (11). Instead, a faint rhombus-shaped region with an average charge occupation between (02) and (11) appears, likely related to averaging over intrinsic metastabilities within the double dot [139]. In addition, the sensor reflection is sufficiently sensitive to resolve charge transitions in regimes where the DC current through the triple-dot device is below the detection limit (for instance, see the left most charge transition in Fig. 4.1.3(f)). This is especially relevant for tuning up quantum dot arrays with single-electron occupations, appropriate for many spin-qubit experiments. As an example, we tune up a triple QD configuration where each of the QDs is filled with one electron. The charge stability diagram (Fig. 4.1.4(e)) shows the typical pattern of a triple QD. The demodulated voltage is plotted as a function of the left and right plunger gates, as labeled in Fig. 4.1.2(b).

4.2 Single shot readout

For these measurements, a triple-dot device is tuned up as a double-dot device. The double dot (0,0)-(1,0) charge transition is first identified using a charge stability diagram (Fig. 4.2.1(a)). We then apply the three sequence pulse sequence for spin-selective readout to the left plunger gate [77], while we step its DC gate voltage (Fig. 4.2.1(b)). During the pulse cycles, the applied magnetic field is large enough, such that the Zeeman splitting is larger than the thermal excitations. If the gate voltage is far too low ($\lessapprox$ –468 mV) or far too high ($\gtrapprox$ –457 mV), no tunneling events are observed, indicating that the pulse never crosses the charge addition line and the system remains always either in the (0,0) or (1,0) state. In the range –468 $\lessapprox$ V_{LP} $\lessapprox$ –462 mV, the gate voltage

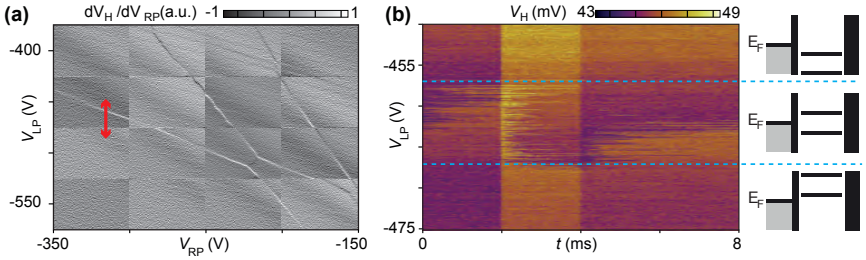


Figure 4.2.1 – Readout position for spin-selective readout. (a) Charge stability diagram of a device as in Fig. 4.1.2(b), but tuned up as a double QD. The arrow indicates the voltage trajectory of the left plunger gate as the left dot is pulsed across the (0,0)-(1,0) in order to identify the position of the Zeeman-split states. (b) At each DC value of V_{LP} the pulse cycle for spin-selective readout is applied (see Fig. Fig. 4.2.2(d) of the main text), with each row showing one single-shot readout trace. The dashed line defines the area where the readout position is aligned with the charge transition in such a way that the Zeeman-split spin states of the quantum dot straddle the Fermi level of the left reservoir.

is too low and the electron can always tunnel out to the reservoir during the readout step, independent of its spin. In the range $-462 \lessapprox V_{LP} \lessapprox -457$ mV, the electron cannot tunnel out during readout. Only in a small voltage range set by the Zeeman splitting, the spin-split states of the QD straddle the Fermi level of the reservoirs, such that only spin-up electrons can tunnel out from the dot during readout step. This phenomenological procedure was used to determine the readout point for spin-selective readout. The measurements presented so far were obtained by averaging over multiple pulse cycles. To gain a deeper insight into the dynamics of a system, single-shot measurements are an important technique [77, 140, 141]. To show single-shot readout, we apply the RF carrier continuously, and first characterize single-electron charge transitions between a QD and an adjacent reservoir, and focus on spin effects later. For that purpose, we apply a square pulse to the left plunger gate of a triple QD, periodically pulsing the left dot across the 0-1 charge transition to load and unload one electron within each period (see Fig. 4.2.2(a)).

4.2.1 Charge and spin detection

Fig. 4.2.2(a) illustrates the applied pulse cycle for single-shot charge readout together with the expected response of the charge sensor signal. The electrostatic effect of one electron entering or leaving the QD manifests itself as a step in the demodulated voltage V_H, as indicated by the arrows. In order to not miss transitions, the pulse period needs to be sufficiently long compared to the characteristic tunneling time. Due to unintentional capacitive coupling between the plunger gates of the triple dot and the sensor dot, V_H also shows steps whenever the plunger voltage changes (black dashed lines). Fig. 4.2.2(b) shows a representative single-shot readout trace from one such pulse cycle, using a pulse period of 3.6 ms and an integration time of 24 µs per data point. The arrows highlight the charge sensor response to an electron tunneling in and out from the dot. (Single-shot traces with integration times as small as 2.4 µs are discussed in section 4.2.2). Repeated acquisition of many single-shot traces as in the lower part of Fig. 4.2.2(b) provide statistics of single-electron tunneling times. For example, the average over 200 single-shot traces is shown in Fig. 4.2.2(c), yielding tunnel in (out) times of 0.41 (0.69) ms from exponential fits for this particular tuning. Alternatively, software detection of tunneling events based on wavelet analysis[142] yields tunnel rates in good agreement with those obtained from the exponential fits, as discussed in section 4.2.2.

Finally, we apply a pulse cycle designed to detect spin-dependent tunneling from the QD to the reservoir. The spin degeneracy is lifted by an in-plane magnetic field of 800 mT. We apply a three-step pulse cycle consisting of an empty, initialization and readout step [77], as illustrated in Fig. 4.2.2(d). First, the energy of both spin states is raised above the Fermi level of the reservoir to empty the QD. Then, the initialization step pulses both states below the Fermi level to load an electron of random spin orientation. Subsequently, spin-selective tunneling is achieved if the readout pulse places the Fermi level just between the Zeeman-split spin states of the QD: A spin-down electron will remain on the QD, while a spin-up electron can tunnel out to the reservoir before a spin-down electron repopulates the QD. The characteristic “electron

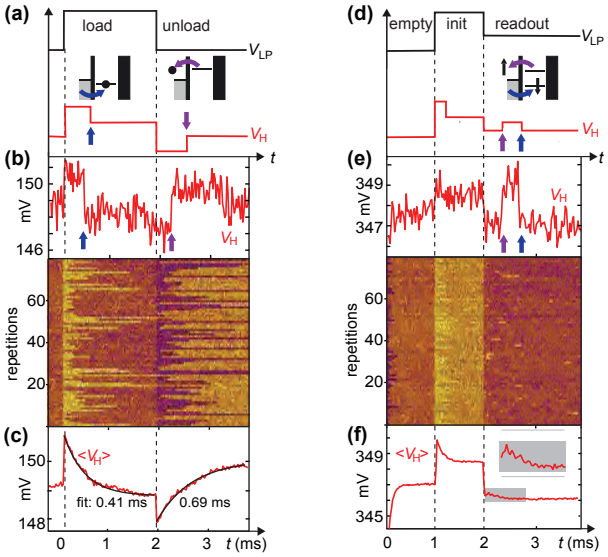


Figure 4.2.2 – Single-shot readout of a quantum dot. (a) Square pulse (black) repeatedly applied to the left plunger gate of a triple dot, pulsing across the 0-1 charge transition of the leftmost QD. Charge sensor response (red) expected for detection of an individual electron tunneling onto or off the dot (arrows). (b) Single-shot trace $\mathrm{V_H(t)}$ acquired during one representative pulse cycle of (a), along with 80 repetitions (lower panel). (c) Average of 200 single-shot traces (red) with 1/e time from exponential fit to selected ranges (black). (d) Three-level pulse (black) for single-shot spin readout [77] repeatedly applied across the 0-1 charge transition. Expected charge sensor response (red) for a spin-up electron, with arrows indicating the characteristic out-in tunnel event during the readout step. This event is absent for spin-down electrons, provided the two spin states straddle the chemical potential of the left reservoir (gray). (e) Single-shot trace $\mathrm{V_H(t)}$ acquired during one pulse cycle of (d), along with 80 repetitions (lower panel). (f) Average of 1000 single-shot traces. The inset highlights the presence of a bump, indicative of an ensemble of spin-up events with stochastically distributed tunneling times.

out electron in" tunneling events associated with spin up show up as a temporary change in the sensor response, as illustrated with arrows in Fig. 4.2.2(d). Spin-selective tunneling requires the plunger gate voltage in the readout step be chosen correctly, such that spin-split QD states straddle the Fermi level. We tuned to this readout position by repeatedly applying the three-step pulse

cycle while slowly stepping the DC gate voltage of the plunger gate until the readout characteristics were observed (see Fig. 4.2.1(b)). For this procedure to work, the Zeeman splitting (≈ 90 μeV) needs to exceed the thermal energy (< 10 μeV), a condition which is fulfilled in the experiment.

Figure 4.2.2(e) shows a single-shot trace representative for a spin-up electron, with the readout step beginning at 2 ms. The out-in tunneling events can be clearly seen in the charge sensor response (arrows). With an rms noise level of 0.42 mV in V_H and a step height of 2.0 mV, the signal-to-noise ratio associated with a 24-μs integration time is SNR $= \frac{2.0}{\sqrt{2}\cdot 0.42} = 3.4$, corresponding to an effective charge sensitivity of $1.5 \cdot 10^{-3} e/\sqrt{Hz}$. Assuming that the power signal-to-noise ratio (SNR^2) scales linearly with the integration time, we estimate a minimum integration time $t_{min} = 2.1$ μs to achieve SNR = 1 [132]. The 2D plot shows data for 80 repetitions of the same pulse cycle; as expected, some shots show no in-out tunneling events and some of them do. The analysis of spin-down and spin-up traces can be automated using simple thresholding methods, leading to reliable results only at sufficiently high signal-to-noise ratios. An alternative technique, which has been found to be more robust against low-frequency noise and signal drift, is based on wavelet edge detection [142]. Alternatively, the presence of spin-up occupations shows up as a "spin bump" when averaging over many single-shot traces (see inset to Fig. 4.2.2(d)), with the shape of the spin bump governed by the tunneling rates [134, 143].

4.2.2 Wavelet edge analysis

Figure 4.2.3 shows the application of a wavelet edge analysis algorithm to data of Fig. 4.2.2, allowing automated detection of single-electron-tunneling events as outlined by Prance et al. [142]. The technique is based on Canny's edge detection algorithm [144], used for the recognition of edges in images, and is well suited to detect sharp edges associated with sensor signals. In order to obtain the function *W(t,s)*, the signal V_H (black trace in 4.2.3(a) is convolved with a scaled mother wavelet, namely the derivative of a Gaussian function of first order, for different scaling factors s of the wavelet function. During the

second step, shown in the fourth row of Fig. 4.2.3(a), the algorithm identifies the track weight for every local minima and maxima at the smallest wavelet scaling factor. The final weight is obtained by summing over the single weights obtained for increasing scaling s, for each trace point. The weight is defined as $W(t,s)^2$ normalized by the median value of $W(t,s)^2$ at a fixed scale. When the

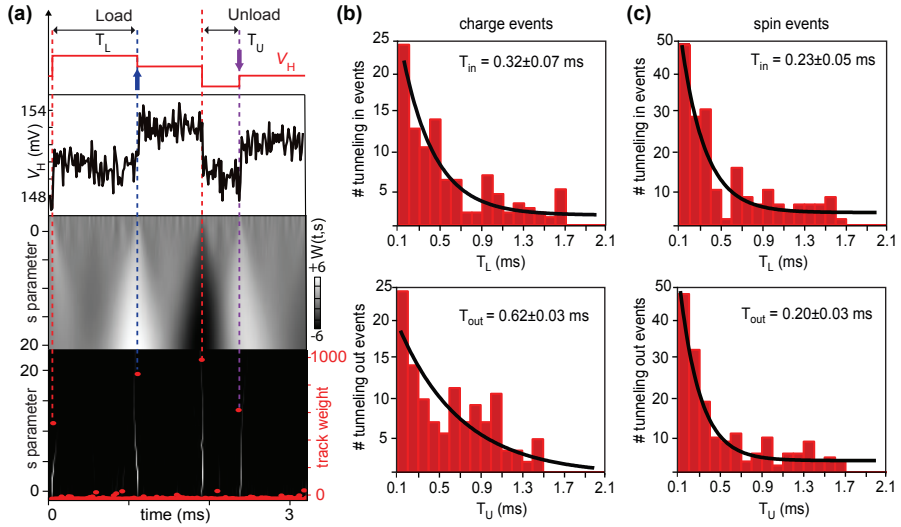


Figure 4.2.3 – Wavelet analysis.(a) One single-shot trace from the two-dimensional panel in Fig. 4.2.2(b) (black), along with the conceptual definition of event durations for loading (T_L) and unloading (T_U) of an electron. In the presence of noise, tunneling events can be extracted by means of wavelet edge analysis as shown in the lower two panels, based on calculating, weighting, and thresholding tracks using a scaling parameter s (see text). (b) Histogram of the $T_{L,U}$ charge events associated with 200 single-shot traces associated with Fig. 4.2.2(b), extracted using the edge detection algorithm exemplified in (a). Exponential fits (black) yield tunneling times consistent with those obtained from the averaged single-shot traces in Fig. 4.2.2(c). (c) Histogram of the $T_{L,U}$ spin events associated with 1000 single-shot traces associated with Fig. 4.2.2(e), extracted by modifying the definitions in (a) appropriate for the spin detection events: T_U is defined as the time elapsed between the beginning of the readout pulse and the tunnel-out event (purple arrow in Fig. 4.2.2(d)), whereas T_L corresponds to the time elapsed between the tunnel-out event and the tunnel-in event (blue arrow). Exponential fits (black) yield tunneling times T_L and T_U that are approximately identical.

track weight rises above a certain threshold value, here defined as seven times the standard deviation from the average track weight, the event is classified as an edge event. The algorithm is implemented in Igor, with wavelet transformation performed using the Igor CWT function, while the main code is based on MATLAB routines found in the WaveLab850 library[1]. Panels 4.2.3(b) and (c) show the tunneling times obtained by applying the wavelet edge detection to the repeated acquisitions presented in the Fig. 4.2.2(c) and (f), for charge and spin events respectively. In order to determine the charge tunneling rates, each single-shot trace is split into two segments, one for each pulse segment. If only one edge is detected within each of these segments, it is recorded as a tunneling event, i.e. either as a loading time (T_L) or unloading time (T_U), depending on whether it occurs in the load or unload segment. The tunneling times are then binned into histograms, using a bin size of 0.1 ms and binning range of 0-2.1 ms (Fig. 4.2.3(b)). Fitting exponentials to the histograms (black trace) yields tunneling times consistent with the tunneling times obtained from averaged single-shot traces in Fig. 4.2.2(c). The experiment in Fig. 4.2.2(b) was performed at high magnetic field (2 T), suggesting that the difference of tunneling times may either be caused by an accidental (near) degeneracy of two orbitals, or by occupation-dependent and gate-voltage-dependent tunneling barriers. For the extraction of the spin tunneling times, T_L or T_U are defined slightly differently: referring to the pulse cycle of Fig. 4.2.2(d), T_U is defined as the time elapsed between the beginning of the readout pulse and the tunnel-out event (purple arrow), whereas T_U corresponds to the time elapsed between the tunnel-out event and the tunnel-in event (blue arrow). The result of the wavelet analysis is binned to extract the tunneling times only if two edges are detected during the measurement step (Fig. 4.2.3(c)). In this case, comparable tunneling times are found for T_L or T_U, as expected for singly-degenerate levels in the Zeeman-split quantum dot. Though both experiments were performed for the 0-1 transition of the left dot, we obtained differing transition rates for charge and spin events, possibly due to a small effective

[1] https://statweb.stanford.edu/~wavelab/.

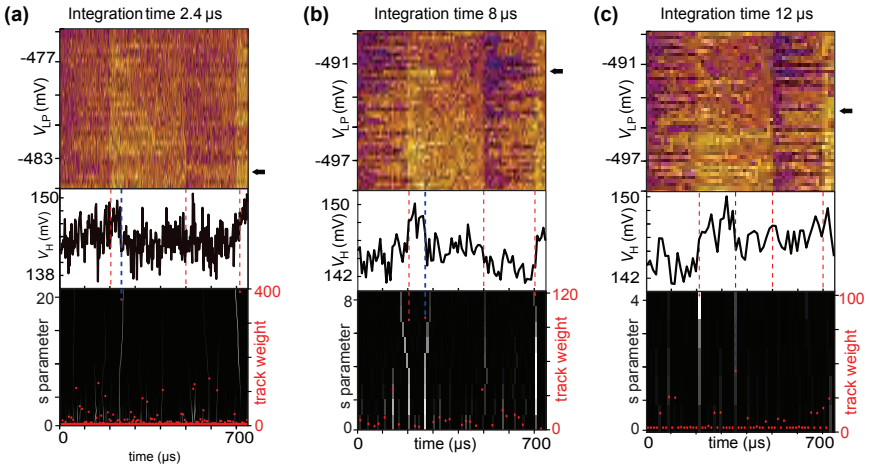


Figure 4.2.4 – Wavelet edge detection for noisy single-shot traces. A square pulse (with pulse segments of 200/300 µs) is repeatedly applied to the left plunger gate to cross the (0,0)-(1,0) charge transition, inducing a cycle similar to that in Fig. 4.2.2(a). Single-shot traces have been acquired with integration times of 2.4 µs (a), 8 µs (b) and 12 µs (c) per pixel, resulting in ensembles with increasing signal-to-noise ratio. Wavelet edge analysis is used to detect tunneling events into the dot, exemplified by one representative single-shot trace (black arrow and black trace) for each integration time. Dashed lines mark the sudden variation of V_H during the acquisition, as detected by the wavelet edge analysis: In red, we mark the steps in V_H arising from direct capacitive coupling between the left plunger gate and the sensor dot (as discussed in Fig. 4.2.2(a)). In blue, we mark steps due to tunneling events, as identified by a large track weight.

shift in tuning voltages and associated tunneling barriers (data in Fig. 4.2.2(b) and 4.2.2(e) were taken several weeks apart). In addition, the rates obtained in this way have a significant uncertainty, which can be improved by increasing the statistics within the histograms. As a consequence of the conservative thresholding criterion for identifying edge events, only 10% (2%) of the single-shot traces were identified with charge (spin) events. This set can likely be increased by optimizing the thresholding criterion. To determine the minimum integration time needed to resolve single-electron-tunneling events, we applied a square pulse to repeatedly induce the 0-1 charge transition, using different settings for the integration time associated with the sampling of single-shot V_H

traces (Fig. 4.2.4). For an integration time as short as 2.4 µs, tunneling events are hard to detect in the raw data by eye (consistent with our estimation of SNR ∼1 for an integration time of 2.1 µs), yet the wavelet edge analysis still yields useful quantitative results.

4.3 Overlapping gate geometry SiGe devices

Despite the impressive results obtained in the previous section, the actual control over these single layered devices has not always proven to be ideal for their application as spin-qubit platforms. In fact, quantum dots belonging to different batches of devices (despite having the same geometry) yielded different properties. Furthermore, as visible from Fig. 4.1.4(e), when the triple dot is tuned in the few-electrons regime, the charge sensor is not able to distinguish between the isoelectronic charge occupations (201), (111) and (102). This drawback would prevent us, for example, from using this device for the implementation of an exchange-only qubit, since it would not offer the readout signal required, as explained in section 2.2.3. We associate the lack of reproducibility of this type of device to mainly two issues: the side gating effect as well as the strain induced from the finger gates at the interface with the substrate. Side gating has a far weaker lever arm compared to top gating. Despite these limitations, the fabrication of the single-gate-layer devices has proven to be "quick", reducing the total number of steps involved. Furthermore, it allows us to avoid low yield due to gate leakage, given the distance between the finger gates. Regarding the inhomogeneous strain induced by the gates at the surface of the material, it contributed to an uneven potential in the quantum well, compounding the effect of the presence of unwanted dopants and other elements [145, 146], which tend to form charge pockets. Recent efforts have been devoted to studying the presence of these charge pockets using gate based readout [147], as well as using optical spectroscopy [148]. The presence of these pockets might be highly detrimental for spin qubits, reducing their performance.

A solution to these multiple issues has been engineered by groups from Prince-

ton [37, 53] and New South Wales [36, 149], where the use of an overlapping gate geometry, could allow in principle to compensate for the inhomogeneous potential in the quantum well, as well as to release the strain due to the finger gates. Additionally, the device would be controlled using a top-gating approach, as extensively explained in section 3.2.1, and it should be possible to induce smaller dots. However, the improved control comes at a cost: the technology required to fabricate such devices is usually beyond the ability of common university cleanrooms (where the yield is still low), and more advanced facilities are required, a luxury that not all research group can access. In the next section we are going to discuss the measurement results we obtained for these devices, as well as possible improvements.

4.3.1 Measurement results

Fig. 4.3.1(a) reports a device fabricated using the recipe presented in section 3.2.1, with a gate pitch of 80 nm. The DC characterization that is going to be presented in this section is from three different devices[2], identified from different heat maps in Fig. 4.3.1 and Fig. 4.3.2. As a first step, a 2DEG is accumulated underneath the left SET presented in Fig. 4.3.1(a), using the general accumulation top gate $V_T = V_{A1} \bigcup V_{AG2} \bigcup V_{SC} \bigcup V_P$, where some minimal hysteretic behavior is observed, as reported in Fig. 4.3.1(b), possibly an indication of two level systems trapped in the ALD oxide layer. The current was biased to flow from the reservoir under V_{A1} to the reservoir under V_{A2} Additionally, the 2DEG shows a metal-like behavior as reported in the inset, yielding a resistance of 1 k$\Omega/\square$ (taken at a V_T=2 V), comparable with the results presented in section 3.2.1. In order to test the effect of the screening plate, we proceeded to the formation of an elongated quantum dot, extending underneath the three gates labeled V_P. The idea behind this tuning procedure is to slowly reduce the extension of the 2DEG from underneath the screening layer, as well as remove inhomogeneous potentials from the surroundings of the

[2]Fig. 4.3.1(c)(d) : device SiGe1240-TURNOV15-CHIP1-32. Fig. 4.3.1(e): device SiGe1240-Ansa12-device4. Fig. 4.3.2: device SiGe1240-TURNOV15-CHIP1-33.

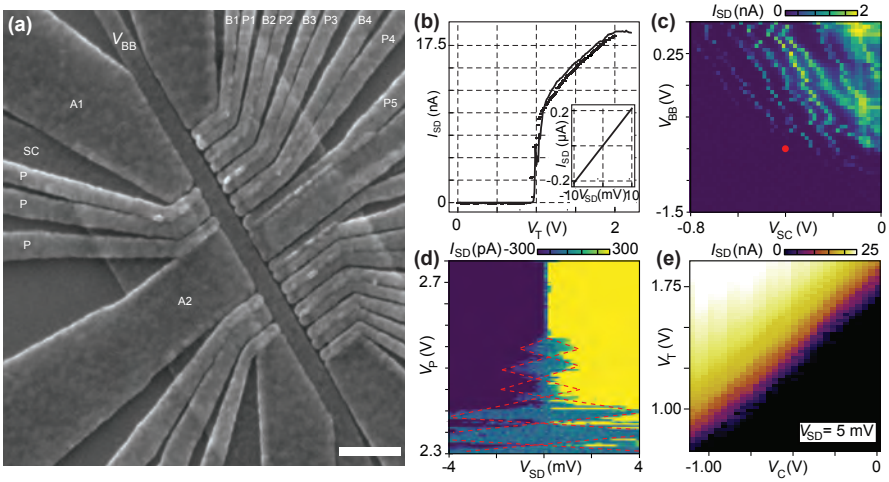


Figure 4.3.1 – **Sensor dot formation.**(a) Scanning electron micrograph of an 8 quantum dot device, including a multielectron quantum dot and equipped with two charge sensors. Scale bar 300 nm. (b) Accumulation curve with a fixed 1 mV bias using a compound V_T gate (see main text). Inset, I-V characteristic at $V_T = 2$ V. (c) Formation of an elongated dot underneath the three gates V_P using the screening plate and the backbone. (d) Coulomb diamonds for the previously mentioned peak, acquired with the gate configuration indicated by the red dot in (c). (e) Effective reduction of the threshold voltage shown in (b), by reducing the bias gate voltage $V_T = V_S \bigcup V_D$, while still maintaining an effective V_{SD}=5 mV. This acquisition belongs to a different device, see main text for more information.

quantum dot channel. As visible in Fig. 4.3.1(c), by using the backbone V_{BB} as well as the screening layer V_{SL}, an elongated single dot could be induced in the channel. Eventually, by moving the potential of the plunger gates, we observed sharp Coulomb diamonds, meaning that the quantum dot was indeed formed in the expected channel, as reported in Fig. 4.3.1(d). The presence of only a few diamonds could be associated with the weakness of the tunneling barrier to the reservoirs.

We now present data belonging to a different device, where we tried to form a quantum dot on the qubit array side of the device (using the labeled gates in Fig. 4.3.1(a)). First, we carefully monitored the gate leakage for each of

the finger gates on the left side of the device, which showed good results as reported in Fig. 4.3.2(a), considering that the insulating layer is obtained solely from the native Al gate oxide (as explained in section 3.2.1). Subsequently, we accumulated an electron channel using all the finger gates and the large accumulation gates, obtaining a curve similar to Fig. 4.3.1(b). Then we pinch off each gate one by one as reported in 4.3.2(b), proving the effectiveness of the single finger gates, despite their reduced dimension (they are partially screened by the overlap with the neighbouring gates). As visible from the SEM image, the gates that show a stronger lever arm, are the ones with reduced screening due to overlap. We also monitored the gate leakage of V_{B3} which reported -140 pA at -3 V (not shown). As for the sensor dot, we could show the accumulation of an elongated quantum dot underneath the electrodes extending between V_{B4} and V_{P1}, as reported in Fig. 4.3.2(c). Selecting suitable V_{B4} and V_{P1}, we obtained the Coulomb diamond data presented in Fig. 4.3.2(d). Despite the

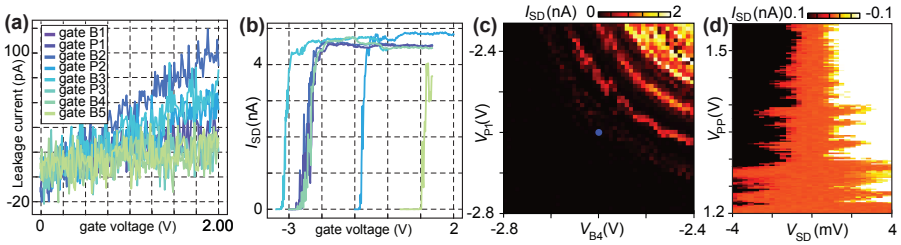


Figure 4.3.2 – Qubit array study. (a) Gate leakage for the leads indicated in Fig. 4.3.1(a). (b) Pinch-off curves for individual gates, with the neighbouring gates at 1.35 V and the screening layer at negative gate voltages. (c) Barrier-barrier scan for the quantum dot sitting underneath the gate $V_{PP} = V_{B2} \bigcup V_{P2} \bigcup V_{B3} \bigcup V_{P3}$, showing Coulomb blockade. (d) Coulomb diamond for the aforementioned quantum dot, with the gate configuration indicated from the blue dot in (c).

promising results obtained, we could not measure the devices further, due to the sudden appearance of gate leakage, related to the quality of the native oxide of the finger gates, which is not sufficient to sustain high potential differences (more than 2V) for prolonged periods of time. Therefore, in a subsequent device, we tried to release the constraints on the potential difference between

the finger gates, redistributing most of the potential drop on the capacitor formed by the ALD oxide in the overlapping area of the accumulation gate and the implantation region. In fact, for a comparable amount of oxide thickness, a higher breakdown voltage for ALD oxide would be expected. The idea consists in using the source-drain voltage as an effective gate voltage in order to activate the channel already at zero top gate voltage, similar to the results obtained in section 4.1, but without the requirement of an LED. The results are reported in Fig. 4.3.1(e), where the the common bias mode $V_C = V_S \bigcup V_D$ is swept as a function of V_T while still maintaining an effective V_{SD}=5 mV. As expected, the threshold voltage scales linearly as a function of V_C. The explanation simply resides in the fact that the 2DEG layer and the top gates are two plates of the same capacitor, and conventionally one of them has always been biased around 0 V, relying on the presence of a higher potential on the other one. However, nothing would prevent, in principle, the accumulation of the 2DEG with all the top gates grounded and a very negative V_C gate voltage. This could be highly beneficial since it would allow to operate the finger gates in a reduced gate voltage space, especially for spin qubits which are typically operated in the few-electron regime. Of course, there is still going to be a relative voltage drop between neighbouring gates. This might allow a thinner AlO_x layer on the finger gates, reducing charge noise arising from TLS [150], as well as a reduced range for digital-to-analog (DAC) sources, an extremely useful requirement for 4K CMOS technology, where lower power consumption strongly limits the bit resolution available [151]. Eventually, reduced ALD thickness would translate to stronger gate lever arms.

However, this technique has proven to be detrimental for our devices, due to a very bad quality of the ALD oxide, where 10 nm of material (for either AlO_x and Hf_x) resulted in gate leakage below 2 V at the region with ohmic-top gate overlap. We attributed this effect to an ineffective treatment of the silicon surface before ALD deposition. We believe, that the optimal way to proceed could be the following: native SiO capping layer removal with subsequent re-oxidation of the surface using a mixture of sulfuric acid and hydrogen peroxide (commonly known as the Piranha solution) for a few cycles, to obtain a high

quality passivated silicon oxide, an ideal layer for the growth of a high quality ALD oxide [152]. Nevertheless, it is important to perfectly calibrate the SiO capping layer removal procedure, such that the silicon capping layer is not fully removed, in order to not expose the underlying $Si_{0.7}Ge_{0.3}$ to air, which could form a very poor quality GeO_x.

5

A 2x2 Array of Quantum Dots in Silicon

In this chapter we characterize a 2x2 array of quantum dots, implemented in a foundry-fabricated device similar to those introduced in section 3.2.2. We use gate-based dispersive RF-reflectometry readout as main investigation tool. We develop techniques to overcome some of the limitations of this technique, demonstrating its compatibility with charge-sensing. We show the capability to control the interdot capacitances using a general top gate and the ability to perform fast single-shot readout measurements. The development of readout techniques for one- and two-dimensional arrays of quantum dots is fundamental to enable to investigation of mid- and long-range interaction between spin qubits implemented in semiconducting quantum dots.

5.1 A new generation of devices

Overlapping-gate devices represent the state-of-the-art for university cleanrooms, and have enabled an incredible advancement of the field for the GaAs [78], SiGe [44] as well as CMOS [153] platform. The tight design constraints have enabled a higher degree of control for the single electron trapped in the quantum dots as well as an increased reproducibility of quantum dot properties (such as charging energies and lever arms). This has set the stage for multiqubit experiments and shown a path towards a fully scalable quantum computer. However, this comes at a high price: as showed at the end of the previous chapter, fabrication is still highly demanding, even for the most advanced university cleanrooms, in terms of facilities as well as skilled scientists[1]. Additionally, almost all the devices used to perform proof-of-principle experiments rely on "quick-and-dirty" lift-off processes incompatible with etched CMOS fabrication carried out in industrial foundries, which are eventually going to take over the mass production of quantum dot devices.

In this chapter, we discuss results obtained on fully CMOS compatible devices, produced at CEA-Leti in Grenoble (already introduced in section 3.2.2). Foundries such as CEA-Leti have been harnessing the knowledge acquired from decades of transistor fabrication, as the production of ultra-thin yet extremely high quality gate dielectric as well as reduced gate pitch and dimension. These two capabilities alone set the stage for the development of extremely efficient silicon devices comparable to the state-of-the-art. Furthermore, these devices can be mass-produced, overcoming the fear of low device yield[2]. However, the potential of these devices rely on the reduced number of knobs for controlling a single qubit. The superconducting qubit community has developed single-knob controlled qubits (via properly engineering the Josephson junction itself), enabling them to achieve unprecedented results in the fabrication and operation

[1] Furthermore, being fabrication expert is an appreciable complementary skill for physicists, but simultaneously it requires a lot of trainings and trail-and-errors. Handing this over to specialized engineers would enable physicists to focus more on research.

[2] This would be extremely important, especially for the university environment, where short device lifetime can be an issue, due for example to power cuts or other events not in direct control of the research group.

of two-dimensional arrays of qubits [16]. Analogously in these silicon devices, a desirable tunnel coupling between the quantum dots could already be dialed into the device during fabrication (depending on gate pitch and spacers). If such devices then turn out to host spin qubits that meet all of the DiVincenzo criteria, they would largely reduce the constraints on the required control electronics (consider the number of AWG or DAC channels required to operate one gate per qubit as opposed to two or three), a possible bottleneck for the realisation of a fully scalable quantum computer. Additionally, a reduced number of knobs would move toward a simplified device design required for scalable 3D integration proposals such as crossbar networks [120, 121]. As is shown later in the chapter, the dense packing of qubits, due to fewer adjacent ohmic reservoirs, requires the implementation of novel readout techniques compared to facing or side-by-side stand-alone charge sensors, namely gate-based dispersive readout (section 3.3.2). This technique repurposes the quantum dots hosting the qubits as sensors for the nearby environment, further reducing the control electronics required. Furthermore, by removing the additional charge sensor, the extension to two dimensional networks can be more easily investigated.

In more general terms, a two-dimensional network is attractive because the scalability of a quantum computation platform is in part predicated by the ability to form one- and two-dimensional arrays of coherent qubits coupled controllably to one another [50, 51, 55, 56, 58, 154, 155]. Silicon spin qubits have recently achieved high-fidelity one- and two- qubit gates [30, 32–35, 156], above error-correction thresholds [31] and are a promising approach to fault-tolerant quantum computation. A significant next step is the coherent operation and readout of these qubits in nearest-neighbour tunnel-coupled two-dimensional arrays. One-dimensional arrays in Gallium Arsenide have led to the demonstration of electron shuttling [50, 154] as well as small-scale quantum simulation [157], which has been successfully extended to the second dimension [57]. Similar results for one dimensional arrays of quantum dots in Silicon devices have been recently demonstrated [51]. The exploration of two-dimensional networks in group IV materials has been limited to the many electron regime in silicon [60]. Recently, Ge two-dimensional arrays have been harnessed to

demonstrate single-hole manipulation for spin-qubit implementation [29]. In this chapter, we demonstrate a two-dimensional plaquette of single-electron quantum dots in silicon with an integrated gate-based fast charge sensor. We show the ability to form reconfigurable single, double, and triple quantum dots with tunable tunnel couplings in this array, presented in Fig. 5.1.1. Compared to previous charge sensing geometry, the charge sensor we implement is strongly coupled with the nearby qubits, and it can be additionally used as a multielectron coupler element for spin qubit, where on-site exchange interactions can also exploited. We believe that these densely-packed architectures could pave the way for densely-packed two-dimensional silicon arrays for quantum computation and simulation[120].

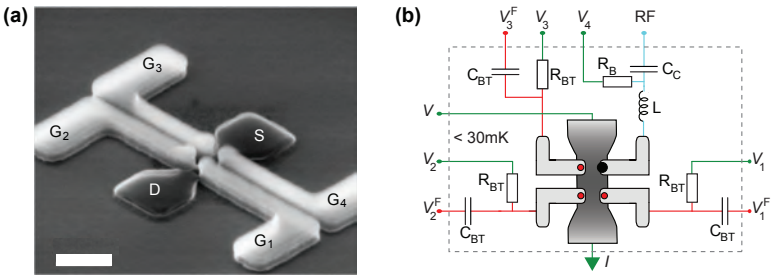


Figure 5.1.1 – 2x2 Device device. (a) SEM image before encapsulation of a device similar to the one studied, showing the Si channel and reservoirs (dark grey) along with four poly-Si gates G_1-G_4 (light grey). Scale bar 200 nm. (b) Device plus PCB configuration. Low pass filters are omitted in the schematic, but present on each low frequency (green) line. See section 3.1 for more informations.

5.1.1 Transport characterization

A scalable architecture requires homogeneity across all the copies that are produced. However, due to the large 300 mm wafer size, as well as the requirement of low temperatures to extract quantum dot properties, fast characterization to improve and validate fabrication flows for such devices is not always accessible to foundries. Nevertheless, there exist links between RT and mK behavior.

As an example, it has been experimentally observed that the quality of the subthreshold swing behavior at room temperature could be directly linked to the strength of the gate lever arm at low temperature [158, 159]. Despite these limitations, high reproducibility for quantum dot properties has been obtained from in-house transport characterization at mK temperature for three different devices (with very similar dimensions), as reported in table 5.1.1. Devices 1S11-1 and 1S11-2 are single split-gate, hosting two quantum dots each (data and more information about the devices can be found in appendix B. 2S29-2 is the double split-gate device that is going to be investigated in this and the following chapter, hosting four quantum dots. The results obtained show an

	1S11-1 RG	1S11-1 LG	1S11-2 RG	1S11-2 LG	2S29-2 G1	2S29-2 G1	2S29-2 G3	2S29-2 G4
E_C (meV)	21.8	22.2	22.4	22.8	15.7	16.5	22	21.3
α (eV/V)	0.5	0.57	0.52	0.51	0.53	0.41	0.35	0.5

Table 5.1.1 – Foundry devices charging energies and lever arms. Devices 1S11-1 and 1S11-2 are single split-gate devices, hosting only two quantum dots each. For more information see appendix B. Device 2S29 is a double split-gate device which is presented in this and the next chapter, and it hosts 4 quantum dots. Wafer T18S0063-W15-D58.

average charging energy in the order of 20 meV, which is in agreement with an electronic wavefunction extension of 500 nm[2][3], an acceptable value given the geometric dimensions of the gates. High charging energies are highly beneficial for "hot" qubit operation, which has been recently demonstrated at a temperature above 1 K [39, 40] as the dots are decoupled from the reservoirs. Interestingly, here the charging energies are roughly comparable to RT thermal excitations (25 meV), a property that could propel the development of a quantum computer with high-fidelity operations at temperature above 1.5 K, the lowest temperature reachable with only He^4, highly reducing opera-

[3]This number represent an upper boundary for the wavefunction extent and it is based under the assumption of a circular shape of the quantum dot.

tional costs. Furthermore, very strong lever arms of the order of 0.5 has been extracted, roughly five times higher compared to state-of-the-art lateral quantum dot devices [53]. In general, such α and E_C results indicate low local disorder, and few defects or residual dopants in the channel, which can affect quantum dot properties and cause irregularities. Finite bias spectroscopy data, used to extract the charging energy E_C as well as the lever arm α are reported in Fig. 5.1.2 for the 2S29-2 device. As shown, each acquisition shows a modulation superimposed on the diamonds, which we associate to the presence of unintentional quantum dots present during the measurements, capacitively coupled to the quantum dot under investigation[4].

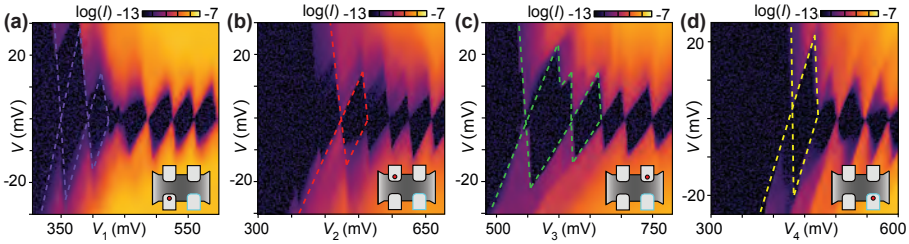


Figure 5.1.2 – DC transport characterization.(a)-(d) Coulomb diamond for each single quantum dot in the 2S29-2 device. Plunger labeling follows the nomenclature introduced in Fig. 5.1.1(a). We estimated an average charging energy in the order of 20 meV as well as an average lever arm of 0.5.

Subsequently, we move to the effect of the metal top gate situated 300 nm above the silicon nanowire, as illustrated in Fig. 5.1.3(e). We tuned the system such that the double dot underneath the gates G_2 and G_3 merged into a single one, and we measured differential conductance using standard locking techniques varying the effective biasing of the top metal line. It is worth noticing that the plunger gates alone can control the tunnel coupling between the quantum dots,

[4]In fact, in order to measure transport, the device was biased such that the dots in series to the one measured to extract the Coulomb blockade pattern were in the few-electron regime, in order to allow tunneling to the reservoirs and simultaneously to block co-tunneling through the other side of the device. As a consequence, the plunger that is swept is slowly modulating the diamond of the neighbouring quantum dot.

by extending the quantum dot wavefunction; as more and more electrons are added, it eventually merges into a single object. As reported in Fig. 5.1.3(a)-(d), by increasing the biasing of the top metal line, it is possible to observe that the merged single-quantum-dot features arise at less and less positive plunger gate voltages. This is in agreement with an interaction mechanism where the top metal line directly affect the potential barrier in between the quantum dots and the reservoirs, reducing the barrier heights as the voltage is made more and more positive. During these acquisitions, the gate voltage applied to the remaining plunger gates were set to zero.

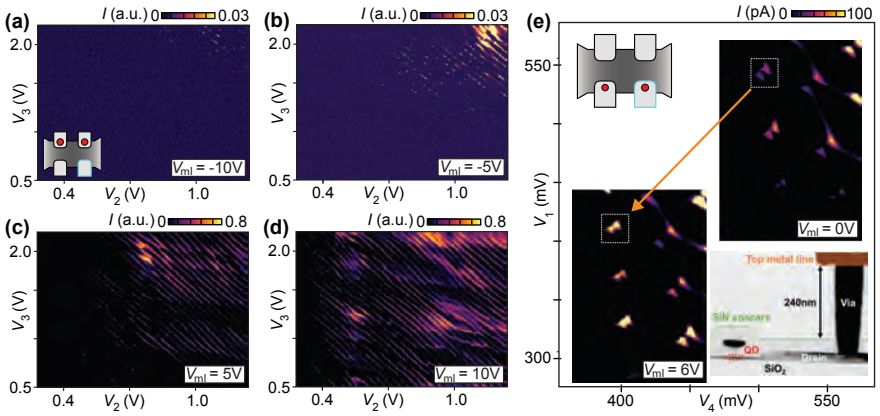


Figure 5.1.3 – Top metal line modulation. (a)-(d) Charge stability diagram of a double dot. The current is shown as a function of the gate voltages V_2 and V_3 measured at different V_{ml} as indicated in each panel. As V_{ml} is made more and more positive, less and less voltage is required to observe transport features of a single extended double dot in the top channel. Effective reduction of the potential barrier between the extended dot and the reservoirs is visible. (e) Double quantum dot modulation as a function of the V_{ml}. Movement of the last triple point visible in transport is in agreement whit a lever arm of 0.017 (extracted from different measurements). As visible the current for the same pair of triple points is enhanced, in agreement with an increased tunnel coupling between the quantum dots.

From more accurate measurements using gate-based dispersive readout, we extracted a lever arm of this top gate on the quantum dots of the order of 0.017.

However, in order to extract the effectiveness of this gate when addressing the interdot tunnel coupling, we focused on the study of the system in the double dot regime as reported in Fig. 5.1.3(e). These two acquisitions present the last set of triple points visible for this double quantum dot (DQD) with a source-drain bias of V= 3mV with reference to Fig. 5.1.1(b). As shown, the intensity of triple points is overall enhanced for V_{ml}=6 V, in agreement with a description were the tunnel coupling between the two dots is increased, hence a faster RC time is expected for tunneling events. This translates into an overall increased number of electrons reaching the drain lead during the same amount of time, in agreement with the trend presented in section 3.2.2. As in the previous acquisition, the gate voltages of the quantum dots not involved in the measurements were biased to zero.
In conclusion, a preliminary transport characterization of these devices has shown that despite the simple design, a high degree of control of each quantum dot can be obtained, using the plunger gates to control dot occupation and the tunnel coupling with the top metal line. This makes these devices promising candidates for further in-depth investigation using gate-based readout.

5.1.2 Gate based dispersive readout

Reaching the last electron occupation using direct transport is not straightforward, and hours of tuning would be required, always with the uncertainty related to this technique (also involve infeasibly long integration times). As a consequence we moved to gate-based dispersive readout in order to fully characterize the device. The resonant circuit consisted of a surface-mounted 820 nH inductor and the stray a capacitance to ground. The reflected signal is demodulated at RT using standard homodyne techniques. V_H is then read-out using a digital multimeter with an integration time of 400 μs (unless otherwise specified).
We started by investigating the properties of the parallel as well as series DQD systems involving the sensor G_4, reported in Fig. 5.1.4(a) and (b), respectively. As shown in both the acquisitions, as the sensor gate voltage is made more and

more positive, while keeping the other gate voltage at zero, intense dot-to-lead transitions appear, related to the increase in the tunnel coupling of the sensor dot with its lead. As the strength of the tunnel coupling reaches a value that matches the resonant frequency of the tank circuit, the polarization signal becomes detectable in the demodulated voltage V_H, as shown in Fig. 3.3.3. Therefore, by biasing the device on any Coulomb peak of the sensor dot, the system is in a configuration where the sensor dot is continuously exchanging electrons with the lead.

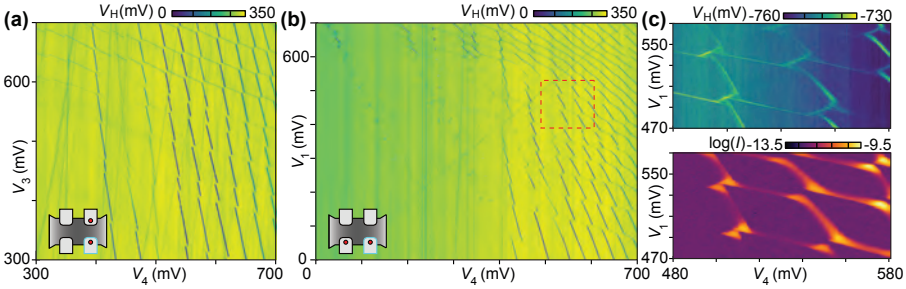


Figure 5.1.4 – Gate-based dispersive readout. (a) Parallel double quantum dot formed between the sensor and the dot facing it. In the overall region explored, double quantum dot feature are visible with increasing tunnel coupling as gate voltages are increased. G_1=G_2=0 V(b) Series double quantum dot formed between the sensor dot and the G_1. Similarly to the previous acquisition, increasing the plunger gate voltages increases the coupling between the dots as well as with the leads, driving the system from a double dot weakly interacting with the leads to a single dot strongly interacting with the reservoirs. G_3=G_2=0 V(c) Comparison between transport and dispersive readout for a double quantum dot strongly interacting with the ohmics, highlighted in (b) by the red dashed region. A bias of -3 mV was applied.

Analogously, a similar behavior is observed if the other plunger gate, namely either G_1 or G_3, is made more and more positive, keeping G_4 at zero gate voltage. Interestingly, this is a peculiarity of these devices, and not commonly observed in lateral quantum dots that are read out dispersively [126, 128]. We believe this effect is related to the strong cross coupling between the sensor dot and these two neighbouring dots. In fact, the RF signal exciting the gate couples directly to the dots in G_1 or G_3, becoming directly sensitive to their

density of states (i.e. their polarizability) when they exchange electrons with their reservoirs. This already introduces one of the peculiarities obtained from the combination of such devices with gate-based dispersive readout: the overcoming of the strong locality of the readout technique, which is now directly sensitive to surrounding environment. Furthermore, for both systems, anytime an electron is moved across any of the two quantum dots, the dot-to-lead transition of the remaining quantum dot experiences a capacitive shift, analogously to the principle used to implement charge sensing, as explained in section 3.3.1. Focusing on Fig. 5.1.4(a), moving along the axis defined as δ=$V_4 + V_3$ we observe the appearance of a regular honeycomb pattern, directly related to the presence of a DQD system. It evolves from being weakly coupled (as visible from the absence of the interdot transitions in the demodulated signal), to a strongly interacting system in the upper right corner, where an ICT appears. Conversely, the series configuration shows many more quantum dot regimes, when the same gate space is investigated, as shown in Fig. 5.1.4(b). Already in the few-electron regime reduced gate space regions show non-zero signals. This is associated with a strongly interacting DQD weakly coupled with the electronic reservoirs. The absence of the dot-to-lead transitions is related to their frequency being slower than the resonant frequency of the readout circuit. Moving along the δ direction, a double quantum dot configuration similar to the one presented in Fig. 5.1.4(a) becomes visible, eventually evolving to a single-quantum-dot configuration for strongly positively biased plunger gate voltages, reproducing the evolution of a double quantum dot for increasing mutual capacitances reported in the sketches of Fig. 2.1.3(c) and (d).
The results obtained in this section are strongly in agreement with the wavefunction distribution already hypothesized in section 3.2.2, where the shape of the electronic clouds is elongated along the channel direction, favoring a strong longitudinal coupling compared to the perpendicular one for low V_{ml} voltages, in agreement with the simulation in Fig. 3.2.6(f). Finally, Fig. 5.1.4(c) reports the comparison between transport and V_H for a stability diagram in the region highlighted by the red dashed square in Fig. 5.1.4(b), in the presence of a V=-3 mV. It shows bias triangles arising in the lowest electron occupation. Co-

tunneling lines appear at higher electron occupancy in transport, highlighting the typical hexagonal DQD pattern and access to both reservoirs. Concurrently, V_H shows an identical hexagonal pattern with clear visibility over all expected transitions. Furthermore, bias triangles are observable in reflectometry as well, with finer features that possibly indicate the presence of excited states and a complex orbital structure.

However, in order to demonstrate suitability for spin-qubit operations, reaching the single-electron occupation is required, similarly to the results obtained in chapter 4. This is achieved by exploiting the capacitive shift induced from a loading event in the neighbouring dots onto the dispersive signal of G_4. The results are presented in Fig. 5.1.5. The sensor is biased in the many electron

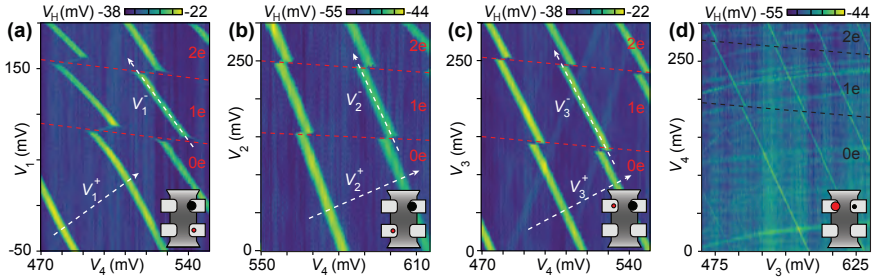


Figure 5.1.5 – Last electron occupation in single dots. (a)-(c) Last electron occupation for G_1,G_2 and G_3, respectively. The sensor dot is biased in the many electron regime, and capacitive shifts indicate the electronic occupancy. V_i^+ and V_i^- arrows indicate the direction of positive and negative compensated sensor gates, respectively. (d) Last electron occupation on G_4 detected using back-sensing action from G_3, see main text for more information.

regime, indicated by the black dot in the inset schematic, and it is swept as a function of the other gate voltages (during each acquisition the idling quantum dots are kept at zero voltage). As shown, anytime an electron is loaded, the Coulomb peaks of the sensor undergo a capacitive shift, indicating the presence of a charging event, revealing the gate-space position of the last electron. The appearance of the first electron at a lower plunger gate voltage for G_1 is in agreement with a stronger lever arm α_{41} compared to the acquisition in

Fig. 5.1.5(b) and (c), effectively reducing the absolute gate voltage required on G_1 to load an electron. Owning to the high cross-coupling between the sensor dot and G_3, α_{43}, we can now access the last electron occupation on the sensor itself, as reported in Fig. 5.1.5(d). By biasing G_3 in the many electron regime, we can "back-sense" the occupation on G_4, exploiting the same charge sensing principle. The reduced FWHM of the sensing peak is most likely related to the absence of power broadening, similar to G_4 in the low power regime (for example when -100 dBm are shown on the gate). From the data presented in Fig. 5.1.5 and other acquisitions, we extracted the following capacitance matrix for the single-electron occupation, when possible. Rows and columns has to be read with input from the vector $\vec{V} = (V_1, V_2, V_3, V_4)$.

$$\hat{C}_{cv} = \begin{pmatrix} 2.14 & 0.33 & 0.25 & 0.73 \\ 0.3 & 1.69 & 0.22 & 0.17 \\ 0.32 & 0.6 & 1.41 & 0.26 \\ 0.79 & 0.34 & 0.47 & 2.00 \end{pmatrix} \tag{5.1}$$

All the capacitances are expressed in attofarad. From this matrix we also define the lever arm factors as $\alpha_{ij} = C_{ij}/C_{jj}$.

5.2 Dispersive charge sensing

Despite these results, dispersive sensing is cumbersome for the identification of ICTs of double-dots not directly involving G_4. In fact, fine tuning would be required to bring the sensor Coulomb peak in resonance with the interdot feature. Furthermore, as the position of the ICT is highlighted, the sparseness of the G_4 Coulomb peaks would barely allow the identification of the contours of the charge state of interest. In this section we introduce two complementary techniques involving virtual gates, which allow to overcome these limitations. Virtual gates are linear combinations of real gates $\vec{v} = \hat{M}\vec{u}$, where either $\hat{M} = \hat{C}_{cv}$, if the requirement is to correct for cross-compensation [51, 55], or any set of linearly independent vectors, if the aim is to rotate the reference

frame [21, 90]. The first set of virtual gates can be used to control what could be called "physical" gates, where each single parameter or "gate" controls one and only one physical quantity in the system, for example the chemical potential of a single quantum dot, or a well-determined tunnel barrier. Such gates have proven to be fundamental for the manipulation of extended quantum dot devices, where cross-talk plays an important role; for example achieving the shuttling of a single charge across nine quantum dots [51] as well as the loading of an eight-dot qubyte register [55].

In this section we are going to introduce compensated gates, which rely on a geometrical transformation dependent on $\hat{C}_{cv}$, similarly to "physical gates". The aim is to correct for cross-capacitances in order to make the chemical potential of the sensor dot sensitive only to the rearrangement of electronic charges in the plaquette. A visual example of such virtual gates is shown in Fig. 5.1.5. By following the white dashed arrows labeled V_i^-, the demodulated voltage would remain constant as long as the electron occupation in the i^{th} dot remains constant. Nevertheless, differently from the results reported in Fig. 4.1.4(b) and (e), due to the very strong dot-to-dot capacitive coupling, the shifts in all the three cases is larger than the FWHM of the Coulomb peak, leading to a very high charge sensitivity at the cost of reduced visibility to only one charge state at the time. As a consequence, differently from the sketch in Fig. 3.3.2, the most sensitive point corresponds now to a biasing on top of the G_4 sensor Coulomb peak. We therefore define the negatively compensated gate as:

$$V_4^- = V_4^o - \alpha_{i4} V_i \text{ with } i = 1, 2, 3 \tag{5.2}$$

α_{i4} is the cross-capacitance matrix element of G_i on G_4, and V_4^o is the sensor biasing point.

5.2.1 Device tuning

In order to apply this technique, we need to have an overview of the charge states disposition, since we are going to be able to highlight only one of them at the time. To increase the density of the peaks per unit area of gate space ex-

plored, we implement positively compensated gates as $V_4^+ = V_4^o + k(V_i + V_j)$, where k now could be any value, depending on the density required. The behavior of these gates can be visualized following the white dashed arrows labeled V_i^+ in Fig. 5.1.5. An example is reported in Fig. 5.2.1(a), where we investigate the double dot V_1-V_2, and we extrapolate the dot-to-lead transition by analysing the capacitive events. Despite the utility of this acquisition technique it suffers from a drawback, namely a reduced sensitivity to latched transitions, as can be observed from the absence of the capacitive shift for the first electron loaded into G_2, at a low biasing of G_1. As the charge state of interest has been identified, in this case the (110) state, we proceed to the implementation of negatively compensated gates, by extending equation 5.2 to two gates, as $V_4^- = V_4^o - \alpha_{14}(V_1 - V_1^b) - \alpha_{24}(V_2 - V_2^b)$, where $\vec{V}^b$ indicates the reference coordinates of any point inside the charge state. The result is reported in Fig. 5.2.1(b). As expected, the first electron transition on G_2 shows latching effects in agreement with Fig. 5.2.1(a), although the identification of the charge state is not significantly hampered by it. Furthermore, as discussed above, the strong dot-to-dot coupling leads to the adjacent charge states being indistinguishable, where V_H lies consistently in the coulomb blockade region of the sensor. As the position of the interdot charge transitions are correctly identified in gate parameter space, it is now possible to separately highlight the four different charge configurations around it using uncompensated gates (Fig. 5.2.1(c)-(d)) as well as sweeping negatively compensated gates (Fig. 5.2.1(e)-(h)), depending on the experimental requirements. In order to obtained the aforementioned result, the biasing point of the charge sensor during the four different acquisitions is adjusted accordingly to the total number of electrons present in the double dot.

Working principle

To gain an understanding of this type of acquisition, we focus now on the study of the double dot G_1 and G_3. Fig. 5.2.2(a) reports a sketch of the main capacitances playing an important role when measuring the aforementioned

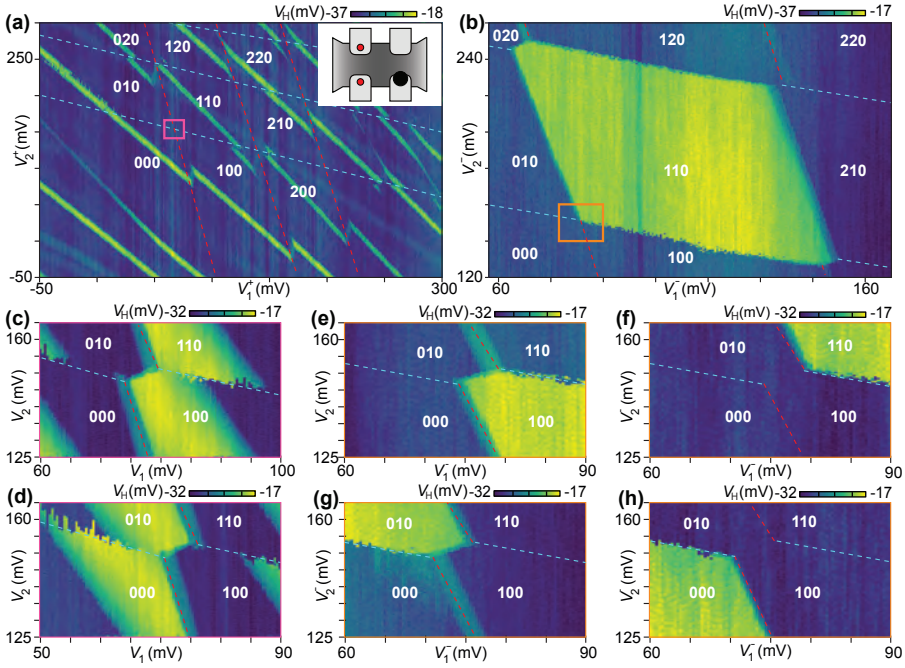


Figure 5.2.1 – Device tuning. (a) charge stability diagram of the double dot formed by G_1 and G_2, as indicated by the two small red dots in the inset. The sensor G_4 is operated in the many electron regime and used as a sensor (big black dot in the inset). In order to improve the sensitivity, positive compensation has been implemented on the sensor. (b) (110) charge state for the same double dot as in (a) acquired using negative cross compensation on the sensor. See main text for more details. (e)-(d) zoom-in on the highlighted ICT in (a), measured by bringing the sensor peak in degeneracy with them, without applying any compensation. By properly tuning, any charge state can be lightened up. (e)-(h) zoom-in on the highlighted region in (b), showing the ability of using cross-compensation to light up any charge state, by opportunely tuning the bias point of V_4^o of the sensor. All the acquisition were performed at V_{ml} =12 V.

double dot, either in real gate space or in the negatively compensated one. The blue lines indicate the capacitances of plunger G_4 on the neighbouring gates whereas, in yellow, we highlight the reciprocal capacitance. As a first step, we developed a simulator able to solve the electrostatic ground state of a quadrupole quantum dot plaquette, with real-valued dot-to-dot and dot-to-

gate capacitances [160, 161]. Fig. 5.2.2(b) reports the simulation of a triple dot charge state in real gate space, involving the three dots introduced in (a). Interestingly, taking a cut through the volume of the charge state for a fixed V_4 yields the expected honeycomb pattern, as reported in (d). This configuration corresponds to keep the sensor dot biased in its Coulomb valley, while sweeping the other plunger gates. However, by taking the same cut with V_4 biased on

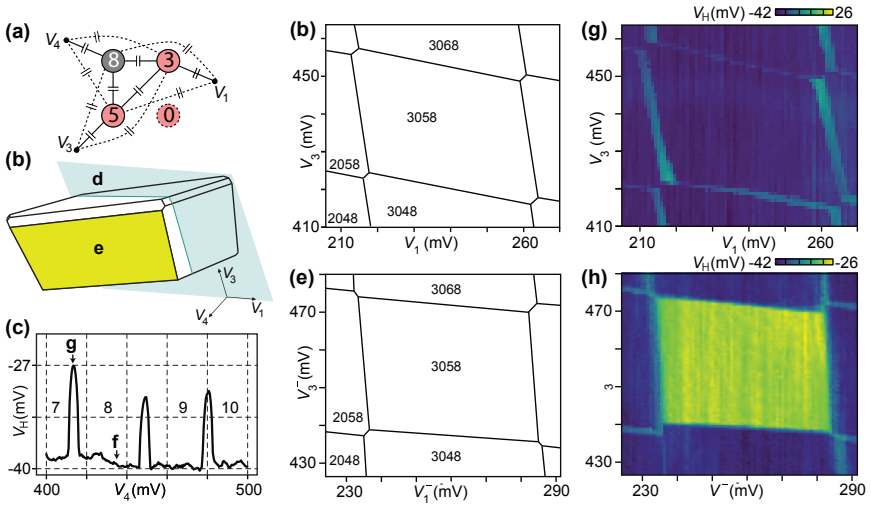


Figure 5.2.2 – Dispersive charge sensing. (a) Sketch of the main important capacitances in the device, when considering a double dot formed by G_1 and G_3 plus the sensor dot (in black). In blue C_{41} and C_{43}, and in yellow C_{14} and C_{34}. (b) Simulated charge stability diagram for the triple dot formed by the three dots presented in (a). (c) Sensor G_4 Coulomb peaks. (d) Simulated charge stability diagram for G_1 and G_3 double dot, for G_4 deep in Coulomb blockade. This corresponds to a two-dimensional cut along the volume of the triple dot in (b). (e) Simulated charge stability diagram for G_1 and G_3 double dot, for G_4 biased on top of a Coulomb peak. This corresponds to the facets highlighted in (b). (g) Acquired charge stability diagram for the same configuration as in (d). The lines visible belongs to the dispersive signal of G_1 and G_3 dot-to-lead transitions. (h) Acquired data using negatively compensated gates for the same configuration as in (e). The sensor peak is biased to the position reported in (c).

its own Coulomb peak, the stability diagram becomes distorted, reshaping into

a rectangle, as confirmed from the simulations in (e). Just like the facets of a double dot are lines of different length, the facets of a triple dot are areas of different shapes, as the tetragon and hexagons previously showed. The actual shape depends on the capacitance ratios between the different quantum dots. This behavior seems to be supported by the experimental data reported in Fig. 5.2.2(g) and (h). The first acquisition is taken with the sensor peak biased deep in blockade. As a consequence, the only signals visible in the acquisition are associated to the big capacitance existing between G_4 and any of the first-order neighbouring gates, making the RF signal directly sensitive to G_1 and G_3 density of states (blue lines in (a)). Unfortunately, due to the weak diagonal tunnel coupling, the interdot charge transitions are not visible, but the overall shape of the acquisition resemble an hexagon, as in the simulation. In the last panel, the sensor is kept biased on the top of its Coulomb peak (see Fig. 5.2.2(c)), recovering the rectangular yellow facet highlighted in (b), as negatively compensated gates are implemented (yellow lines in Fig. 5.2.2(a)). In conclusion, given the readout method for these devices and their properties, anytime we investigate a N-dimensional charge configuration using the negatively compensated gates, we are actually studying the projection of the same charge state on the facet of an N+1 dimensional charge state, where the additional dimension is given by the occupation of the charge sensor.

5.2.2 Charge sensing of double and triple dots

In Fig. 5.2.3(a) to (c), we map out the single-electron occupation of the three different double quantum dot combinations (series, facing, and diagonal). This is the first time that reconfigurable last-electron occupancy has been demonstrated on such two-dimensional devices, mainly due to the limitations of purely dispersive gate-based readout. By implementing the "dispersive charge sensing" technique, we managed to overcome two of these limitations: first, we are now able to probe non-local transitions that have a tunnel rate much slower than the readout tone (∼200MHz), and second (and most importantly) this technique is now sensitive to charge and not to charge motion anymore, en-

abling a direct comparison with traditional charge sensing techniques. It therefore enables the study of spin qubits exploiting many techniques developed over the past two decades, as shown in the next section. In Fig. 5.2.3(d) we report

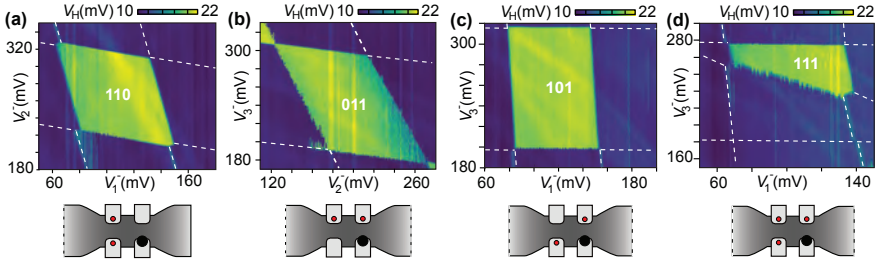


Figure 5.2.3 – Charge sensing of double and triple dots.(a)-(c) Single-electron double-dot charge states for different quantum dot configurations (above) with a schematic showing the corresponding electron occupation within the array (below). (d) Above, the (111) charge state of a triple dot, with one electron in each of the three dots under G_1-G_3 as shown in the schematic below. The charge state is obtained by starting from (c) and slowly raising the plunger voltage V_3 until an electron populates the corresponding dot. All acquisitions are performed by compensating V_4 against direct capacitive coupling between $G_{1,2,3}$ and the chemical potential of dot 4. In (a)-(d) the top gate voltage is set to 6 V.

the formation of a triple quantum dot, where each dot hosts a single electron. This has been obtained by starting from the configuration in (c), and slowly increasing the plunger gate voltage of G_2 until one electron is trapped inside the dot. The identification of the (111) state is useful for the implementation of the exchange-only qubit, which obviates the need for micromagnet or ESR line fabrication [89, 90]. A purely dispersive signal arising from the dot-to-lead transition of the G_1 dot is also visible, in a regime where in real gate space this signal would be absent, as seen in Fig. 5.2.1(a). A likely explanation could rely on the fact that the sensor dot is tuned at the highest hybridization point with its own lead, where an electron is continuously exchanged with the source, possibly"pumping" the G_1-to-lead transition. However, further investigations are required, studying, for example, the evolution of such an effect as a function of the sensor gate bias point.

5.3 Single-electron control

The last section of this chapter concerns the study of the tunneling times for single-electron occupations, for the double dots presented in Fig. 5.2.3. Similar results have not previously been reported for such devices due to the limitations imposed by gate-based dispersive readout. They provide a first insight at the suitability of the current geometry and architecture for qubit implementation, since the ability to perform non-equilibrium studies for single electrons in a quantum dot is a fundamental requirement in a gate-defined spin-qubit toolbox.

The technique that we implemented, as shown in Fig. 5.3.1, has been developed and improved over the last two decades from the lateral quantum dot seminconducting community [68, 162]. In (a) we show the charge stability diagram acquired for the double quantum dot formed underneath gates G_2 and G_3, highlighted as two small red dots in the inset, with the sensor dot in uncompensated mode. The orange arrow in the inset, as well as superimposed on the stability diagram shows the dot-to-lead transition studied, taking the electronic state from (000) to (010). The arrow is marked V_2^F, indicating a pulse of 2mV amplitude applied to G_2. To perform the measurement in Fig.5.3.1(b), we apply the square pulse, as shown in the inset, and acquire traces while changing the DC biasing point V_2, with a sample rate of 1 MSa/s, measurement time τ_M, and 5000 averages, corresponding to an overall bandwidth of 200 Hz[5]. In an approximately 2mV window around the degeneracy point between the (000) and the (010) dot-to-lead transition, we observe the sensor signal decaying from the value corresponding to the (000) state (green in the stability diagram) to the (010) state (blue), as expected. Fig.5.3.1(c) reports three linecuts corresponding to different negative detuning positions with respect to the charge transition point indicated in (a). The signal has been normalized to the unitary value for the zero occupation, yielding $\overline{V}_H$, and it

[5]All the fast data acquisition in this section have been performed using a fast digitizing card, Alazar 9360.

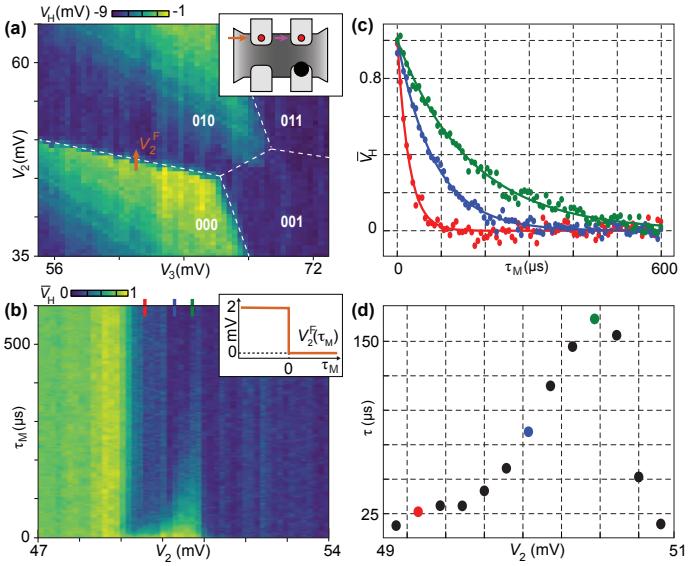


Figure 5.3.1 – Tunneling rate analysis. (a) Stability diagram of a DQD formed under G_2 and G_3 with $V_{ml} = 12$V. The orange arrow indicates the fast pulse V_2^F of amplitude 2mV used to explore the tunnel rate dynamics of dot-to-lead transitions for the dot under G_2, as shown in the inset schematic. (b) Time-domain measurement of sensor response vs τ_M, where the 2mV pulse (see inset) is applied to G_2, while its DC voltage is varied via the bias tee. The measurements were performed at a sample rate of 1 MSa/s. The data show the (000) state (green) decaying into the (010) state as the degeneracy point is approached. The three bars (red, blue, green) show three cuts near the degeneracy point. (c) Normalised red, blue and green traces taken at the three corresponding points indicated in (b), showing the variation of tunnel rates near the degeneracy point. (d) Tunneling times extracted from the traces in (b) shown against the DC biasing point of G_2, with the three traces in (c) shown with solid circles of the corresponding colour. The green circle is the one with the maximum tunnel rate

has been fitted using an exponential decay function, extracting the characteristic tunneling time. The extracted non-zero tunneling rates have been reported in Fig.5.3.1(d), where the colour code corresponds to the traces presented in Fig.5.3.1(c). Interestingly we notice a strong dependence of the characteristic tunneling time as a function of the detuning value. We associate this effect with the presence of singularities in the density of states, since such structures

would not be generated from a flat two-dimensional metallic density of states. A further study of this effect along the dot-to-lead transition of G_2, for different pulse amplitudes, would enable us to disentangle the density of states of the reservoirs and the orbital structure of the quantum dots. Such information could allow a deep understanding of the origin of the non-constant density of states in the leads, such as isolated dopants, providing useful feedback to the fabrication team. In order to perform such an experiment, we believe that the implementation of negatively compensated gates would be highly beneficial, providing visibility over an extended area in gate space.

5.3.1 Time domain analysis

We now perform time domain analysis employing fast pulses on G_1-G_3, combined with high-bandwidth readout, similarly to recent scientific results obtained from the international community [62, 110, 118, 132, 163]. In Fig. 5.3.2(a) the device schematic is superimposed with the dot-to-lead (blue and green) as well as interdot (magenta and orange) transitions under investigation, probing their tuneability as a function of the metallic top gate. We study the system without sensor cross-compensation, using the capacitive shift of the sensor peak to identify the interdot charge transition of interest, as reported for one of the double dot in Fig. 5.3.2(b). As illustrated in Fig. 5.3.2(c), the pulse sequence is composed of two steps in all cases. During the preparation step (P), the system is initialized to the charge configuration of interest, whereas during the measurement step (M), lasting for a time τ_M, the single electron is non-adiabatically pulsed into either the neighbouring lead ((d) and (e)) or quantum dot ((f) and (g)). V_H is continuously recorded and digitized at 500 kS/s with an integration time of 11 µs. Fig. 5.3.2(d)-(g) report the results on the investigation of the characteristic tunneling time as a function of the metal gate line, where the colour code matches the transitions indicated in panel (a). The value of the metal line is indicated by the shape of the marker used to plot each of the tunneling events. As observed, the overall effect of the metal line is to reduce the height of the tunneling barrier between the dots and the leads.

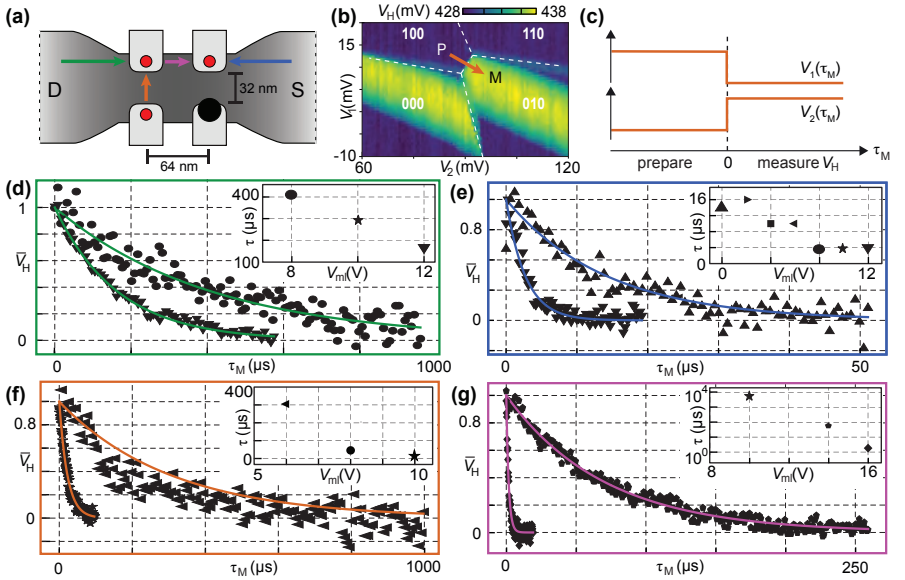


Figure 5.3.2 – Tunneling time modulation. (a) Device schematic indicating the dot-to-lead (green and blue arrows) and interdot (orange and magenta arrows) transitions for a single electron. The arrowhead orientation indicates the directionality of the tunneling event studied. (b) Charge stability diagram for the plunger voltages V_1 and V_2. P and M indicate the preparation and measurement points respectively for a square pulse used to study the G_1 to G_2 single-electron interdot transition. (c) Representative square pulse used to probe the interdot charge transition in (b), with the DC point chosen to be in the middle of the transition. (d)-(g) Average characteristic tunnel rates for the single-electron transition indicated in (a), for the last electron occupation. The colour of the bounding box corresponds indicates the transition studied, in analogy with the arrows in (a). The shape of the marker represent a well defined V_{ml} voltage. The insets report the tunneling time dependence on V_{ml}.

Regarding the dot-to-lead transition we observe a slower tunneling rate of G_2 with its own lead compared to G_3, which is in agreement with the measured latched behavior for the last electron under G_2, reported in Fig. 5.2.1(a). A similar modulation is reported for the interdot transitions, which tend to become faster as V_{ml} becomes more and more positive. This description is partly in agreement with the simulations presented in section 3.2.2, where the overall

effect of the metal line follows the same trend regarding the evolution of the interaction. However, from the extracted data it seems that the modulation is much stronger for the quantum dot in series, as compared to the perpendicular configuration. This discrepancy between simulation and experiment could be due to different configurations of the sensor G_4, being biased to the one-electron regime in the simulation, whereas it was kept in the many-electron regime during the experiment. Furthermore, it is necessary to acknowledge that the simulated points are extracted from the elastic tunneling matrix elements, whereas the τ we report arise from the inelastic tunneling of an electron from the excited state to its ground state. Experimentally, elastic tunneling matrix elements could be extracted from the FWHM of the dispersive signal of the interdot, which is not available for this biasing of the device.
The lack of tunnel coupling tunability has been a concern for foundry-fabricated device with only one gate per device. These results show that the common top gate fabricated using the third dimension can alleviate this concern while maintaining foundry-compatibility and a simple gate structure. Furthermore, in future iterations it might be possible to place V_{ml} closer to the device as well as implementing a higher quality oxide, reducing hysteresis effects that are sometimes observed as V_{ml} is moved.

5.3.2 Single-shot readout

Eventually, we move to the demonstration of single-shot measurement capability, an essential property to perform qubit readout as explained in section 2.2. For this purpose, we select the spinful, or even-parity, (040)-(031) transition which has been shown to be useful for spin-qubit operation due to the filled lower-valley structure [62], for the double quantum dot presented in Fig. 5.3.1(a)[6]. The stability diagram, with the sensor dot under G_4, biased to maximise contrast between the states of interest, is shown in the inset of Fig. 5.3.3(a). The top gate is lowered to $V_{ml} = 6V$ to achieve lower tunnel rates, expected to be in the order of ms in analogy with the results in

[6]We note that we are not performing spin readout, but demonstrating the ability to perform single-shot charge measurement at this interesting transition.

Fig. 5.3.2(f). The triangular pulse sequence (load, initialise and measure) is

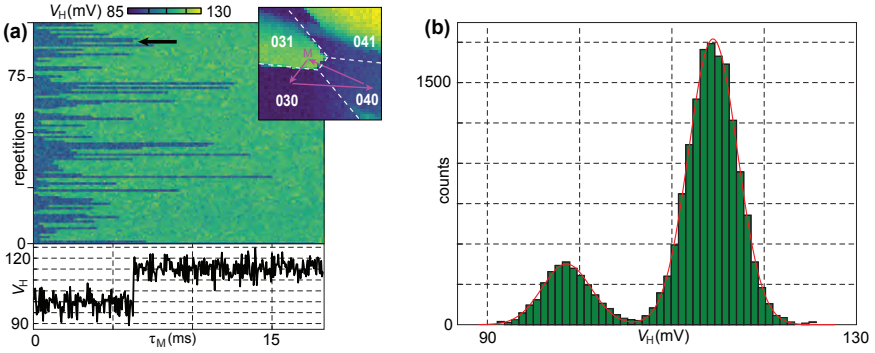


Figure 5.3.3 – Single shot readout.(a) Single shot measurements and characterization. 100 single-shot traces are shown, taken at $V_{ml} = 6V$, shown in the inset along with the pulse performed. The measurement point is indicated by the letter M. The (031)-(040) state is chosen since it is a region where spin-qubit operation is possible, and requires high-fidelity single-shot readout. The change in the sensor signal from blue (040 state) to green (031 state) is clear. The arrow in the top panel of (a) indicates the single trace which is plotted in the bottom panel. The data are post processed using the decimate function from python-scipy library. (b) Histogram analysis of the ensemble of single-shot traces, with a double-gaussian fit measured using an integration time of 10μs. The post-processed data yields an of SNR=4.23.

superimposed on the stability diagram, with the measurement point marked by the letter "M". Panel (a) shows 100 single-shot traces, taken at a sample rate of 100 KSa/s. The effective integration time of the measurement was set to be roughly 10 μs via a 30 kHz low-pass filter. In the bottom part of the same panel, a particular trace from the heat map (indicated by the black arrow) is shown to highlight the sharp jump in the sensor signal when the electron tunnels from one dot to another. In post-processing we apply a digital filter[7]. In panel Fig. 5.3.3(b) we histrogram the filtered traces obtaining an SNR $= \frac{15.9}{\sqrt{2}\cdot 2.65} = 4.23$. This yields a charge sensitivity of 0.7 $me/\sqrt{\text{Hz}}$, in agreement with state of the art single-shot results, ranging from

[7]We applied the decimation filter from the python-scipy library.

hundred of nanoseconds [132, 134] for highly tuneable Si/SiGe devices to milliseconds [62, 110] for CMOS devices. The histogram of the not post-processed single-shot traces yields an SNR of 1.43. While already comparable to recent single-shot SNR results in the field of silicon quantum dots, we anticipate that this SNR, measured using standard reflectometry techniques and surface-mount inductors, could be significantly improved using specialised amplifiers [163], a Josephson Parametric Amplifier [164] or by moving to superconducting inductors [132] or a different tank circuit configuration [165].
In conclusion, we have developed a gate-based dispersive readout technique that is sensitive to absolute charge occupation in the quantum dot array, and not only to quantum and tunneling capacitances. We have made use of this technique to demonstrate the capability of these foundry-fabricated devices, showing the ability to form single, double and triple dots, performing time domain measurements of tunneling rates and single shot readout of electron charges. These results are comparable to state-of-the-art university cleanroom devices as presented in chapter 4. In the 2x2 array which we presented, the sensor dot can be driven into a strong interacting regime with the qubits dots, differently from the device in chapter 4, where the sensor was only weakly capacitively coupled to the qubit array. This configuration could be beneficial, since the sensor can now be embedded in the quantum circuit itself. For example it can be used as a multielectron coupler that mediates the interaction between distant qubits, using onsite exchange interactions [166].

6

Electron Shuttling and Adaptive Data Acquisition

In this chapter we present two experiments performed using the device and acquisition techniques presented in chapter 5. The first experiment concerns the shuttling of electrons within the array. By exploiting the two dimensionality of the array, we interchange the position of two electrons within the array, without exchanging them with the leads. This demonstration of charge shuttling might be useful in future experiments for realizing protected gates in quantum permutation algorithms [167] and, on an operational level, for braiding experiments based on non-abelian particles [168]. The second experiment concerns the implementation of a semi-automated sparse data acquisition for the investigation of high-dimensional charge states. We show the working prin-

ciple for a two-dimensional and three-dimensional acquisition, demonstrating a dramatic reduction of measurement samples and a speed-up in acquisition time compared to standard acquisition. This approach does not depend on the dimensionality of the array, but can be extended to an N-dimensional charge state. If applied to the (1111...1) state of a large array, this procedure could also be seen as a semi-automated method for the booting of a Loss-DiVincenzo simulator.

6.1 Shuttling of two electrons in two dimensions

In the previous chapter we have demonstrated the ability to populate each quantum dot with one single electron. Furthermore, in Fig. 5.2.3(d) we showed the capability to form triple dots, an useful platform to avoid the implementation of micromagnets and striplines for qubit control. In Fig. 6.1.1(a) we report a similar triple-dot configuration, in which we tuned the occupation in the (111) regime, corresponding to (G_1,G_2,G_3), using negatively compensated gates. Despite the high states visibility offered from the negatively compensated technique, it requires time to be initialized when moving between many charge states. In order to speed up this process, we introduce a new control parameter, which we indicate as common mode (CM). When sweeping the common mode voltage V_{CM}, the plunger gate of dots G_1, G_2 and G_3 are swept simultaneously. An example is reported in Fig. 6.1.1(b), where the common mode is swept as a function of the sensor dot voltage. In this acquisition, V_{CM} origin is set at the purple circle in Fig. 6.1.1(a). By decreasing V_{CM} and following the right peak (the same V_4 peak used to obtain the negatively compensated map in Fig. 6.1.1(a)), we observe only three capacitive shifts, G_1, G_2 and G_3, corresponding to the three transitions highlighted in Fig. 6.1.1(a). The capacitive shifts observed are in agreement with the dot-to-dot coupling observed in Fig. 5.1.5. No transitions are observed below 50 mV for over 250 mV, a gate space extension bigger than the individual charging energies of each single quantum dot, confirming that the system reached the (000) state. The

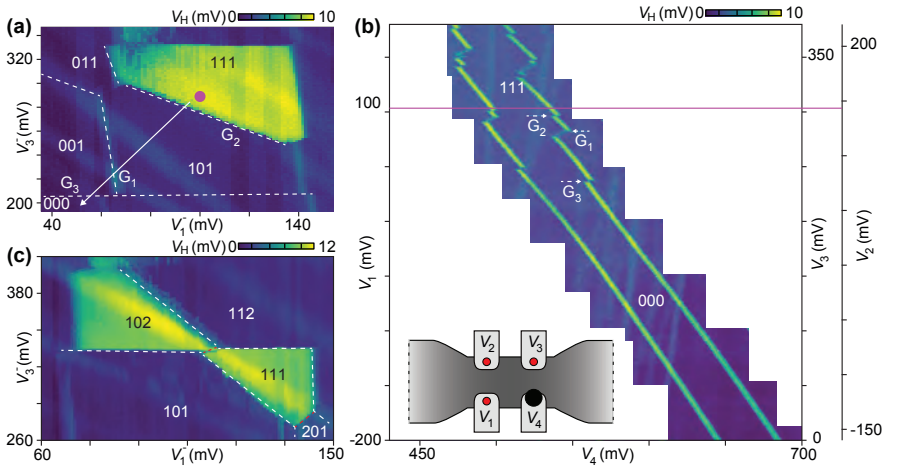


Figure 6.1.1 – Triple-dot occupation. (a) (111) state configuration acquired using negatively compensated G_4 gate for the (G_1,G_2,G_3) dots. The G_4 dot containing 8 electrons serves as a sensor. Arrow represents one possible path to empty the array, reaching the (000) configuration. (b) By sweeping V_1, V_2, V_3 simultaneously (see three vertical axes) versus V_4, the presence of three electrons in the (111) region (violet markers in (a) and (b)) is confirmed by three discrete jumps in the V_4 position of the sensor's Coulomb peaks. We associate each jump with a particular dot, s indicated by G_1, G_2 and G_3. (c) (111) charge state biased in the so-called "house" configuration required for the implementation of the exchange only qubit.

white arrow in Fig. 6.1.1(a) reports a two-dimensional representation of the common mode voltage sweep.

The boundaries of the (111) state in Fig. 6.1.1(a) are not the ones of the so-called "house" configuration desired for the implementation of Pauli spin blockade readout at the extrema of the state [90]. In fact by moving from the center of the state to the left, we cross from (111) to (011). By changing the potential of G_2 during the two-dimensional sweep, we managed to recover the familiar structure for the implementation of the exchange only qubit, reported in Fig. 6.1.1(c). In Fig. 6.1.1(c), the contrast between (102) and (111) is low, indicating that charge movements between G_2 and G_3 affect the sensor signal very little. This could be improved by reducing the power broadening

of the sensor peak, or by optimizing the cross compensation parameters. In order to realize the exchange-only qubit, the visibility of the (111) state with respect to the (102) and the (201) states alone is enough to perform all the operations required to implement qubit gates (in the presence of the right tunnel couplings).

6.1.1 The 111 state

In order to understand the three-dimensional shape of the (111) charge configuration, we acquired several tomographic two-dimensional cuts of the state, as reported in Fig. 6.1.2. Fig. 6.1.2(a) reports a sketch of the state in the negatively compensated gate space, along with one two-dimensional cut (V_1^- vs V_3^-) for a fixed value of V_2^-. In Fig. 6.1.2(b), we show five two-dimensional cuts, for five different choices of V_2^-[1]. The state evolves from a pentagonal shape in the upper cut, through different polygons, to a reversed (111) pentagonal shape. The volume in Fig. 6.1.2(b) does not represent the (111) ground state region. In fact, it represents only the gate-space region (V_1,V_2,V_3,V_4) where the state (1116) and (1117) are degenerate. In other words the triple dot charge state we have investigated corresponds to a facet of the four-dimensional state formed with the sensor dot. This is analogous to how the double dots reported in Fig. 5.2.3(a),(b) and (c) were representing one particular facet of the triple dot they formed with the sensor dot. As a consequence, the state can assume different shapes as compared to the ones obtained for a three quantum dots only triple dot, as the one reported in Fig. 5.2.2 and in triple dot literature [169–171].

6.1.2 Virtual gate space

In this section we describe a specific cut in a virtual space which enables us to implement the two-dimensional shuttling protocol described later in this chapter. As previously introduced, any triple dot charge state cut in two dimensions

[1] due to a different biasing of the phase shifter, the Coulomb peaks of the senor are detected as dips.

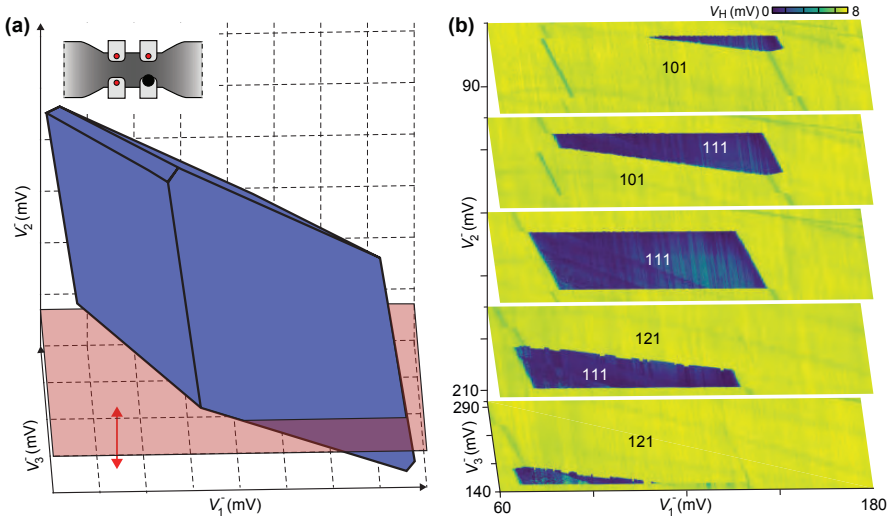


Figure 6.1.2 – Triple-dot tomography. (a) Sketch of the (111) region of a triple dot (blue) in the coordinate system of the negatively-compensating gates V_1^-, V_2^- and V_3^-. The red plane indicates the two-dimensional cut for fixed value of V_2^-. (b) 2D data acquired for five choices of V_2^-, as indicated by minor tickmarks.

assumes different shapes depending on the exact gate voltage configuration. For example, in Fig. 6.1.2(b) it evolved between pentagons and tetragons, but many more shapes might be present. By measuring the triple dot along the direction reported in Fig. 6.1.3(a), it is possible to recover a triangular-like shape, as represented in the sketch. In order to correctly identify the direction of the line-cut, we define the following set of virtual gates, which we operate in the negatively compensated regime:

$$\begin{pmatrix} \varepsilon_1^- \\ \varepsilon_2^- \\ \varepsilon_3^- \end{pmatrix} = \begin{pmatrix} 1/\sqrt{3} & 1/\sqrt{3} & 1/\sqrt{3} \\ 0 & -1/\sqrt{2} & 1/\sqrt{2} \\ -2/\sqrt{6} & 1/\sqrt{6} & 1/\sqrt{6} \end{pmatrix} \begin{pmatrix} V_1^- \\ V_2^- \\ V_3^- \end{pmatrix}, \tag{6.1}$$

This set of virtual gates is representing a rotation of the gate-parameter space, as indicated in Fig. 6.1.3(b).

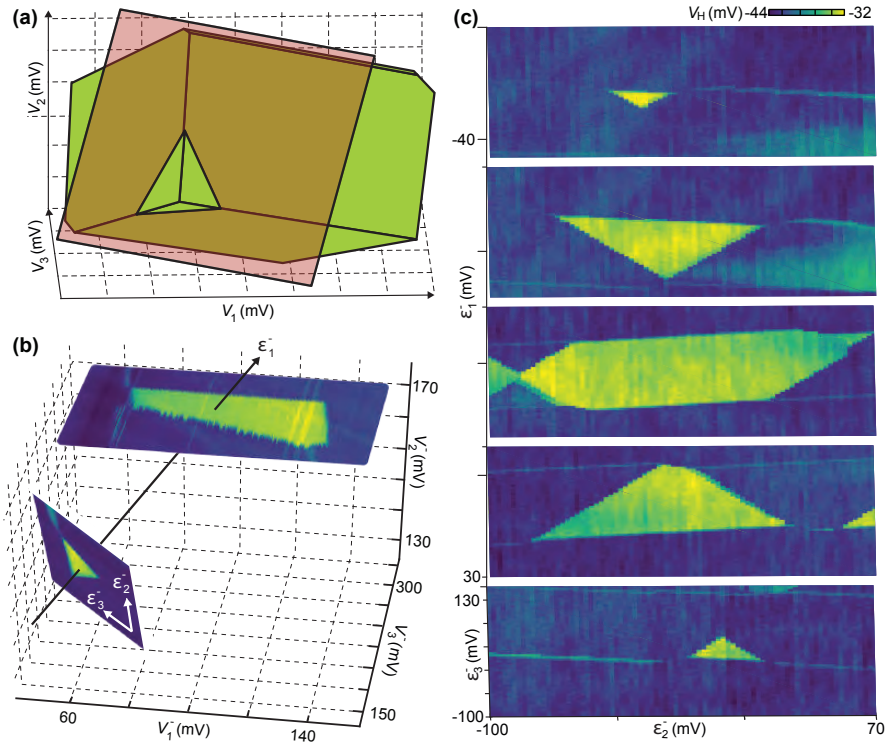


Figure 6.1.3 – Symmetry-adapted coordinate system. (a) Sketch of the (111) state of a triple dot in parameter space spanned by V_1^-, V_2^- and V_3^-. Within a particular two-dimensional cut spanned by detuning parameters ε_2, ε_3 (see equation 6.1), the (111) region appears as a triangle. (b) Visualization of ε_1^- (a common mode voltage for V_1^-, V_2^- and V_3^- which adds electrons to the overall array) and ε_2^- and ε_3^- (detuning voltages, which polarize charge distribution within the array along and perpendicular to the Si channel). Note that the same (111) state appears very differently on (V_1^-, V_3^-) and (ε_2^-, ε_3^-) 2D maps. The (V_1^-, V_3^-) is identical to Fig. 5.2.3(d). (c) 2D maps ε_2^- vs ε_3^- for different choices of ε_1^-, revealing five tomographic cuts of the (111) region (yellow).

The rotated reference frame can be interpreted as follows: ε_1^- approximates the common mode direction that propagates along the diagonal of the 111 charge state (it is the normalized representation of V_{CM} previously introduced). ε_2^- describes the detuning potential along the longitudinal direction of the quan-

tum dot array and ε_3^- represents the detuning between the left and right side of the array, similarly to [90]

In Fig. 6.1.3(b), the bottom state highlights the (111) configuration acquired using the compensated virtual coordinates $\vec{\varepsilon}$, unveiling the triangular shape. Moving to more negative ε_1^- values, the (111) state shrinks to a single point; at this point the charge configurations (110), (101), (011) and (111) are degenerate, forming a quadrupole point [170, 172]. It is interesting to notice that points with six-fold degeneracy have been observed, depending on the dot-to-dot capacitances, for triple dot systems [54]. On the other hand, the upper cross-section of 6.1.3(b) shows the same charge state as the acquisition reported in Fig. 5.2.3(d), recovering the more commonly observed (111) shape for a triple dot. Fig. 6.1.3(c) reports a tomographic study of the triple dot charge state, similarly to Fig. 6.1.2(b), by exploring the rotated gate parameter space. As visible, by moving along the ε_1^- direction, the system evolves between a couple of quadruple points, where the one situated at positive detuning is degenerate between the energy states (111), (211), (121) and (112). For intermediate ε_1^- values we observe previously unreported number of facets of the (111) state. In addition to the triangular, tetragonal, pentagonal and hexagonal shapes, the (111) assumes a maximum extension of nine facets around the coordinate $\varepsilon_1^- = 0$.

Some of these facets might border with charge states which involve more than one charge rearrangement process when crossing the state boundary. These effects are often associated with quantum cellular automata (QCA) [169, 170, 172], due to their similar signature. More in general, QCA processes are related to arrays of quantum dots with a number of interdot capacitances higher than one. Therefore they are not limited to two-dimensional arrays, but they have been observed in a linear triple quantum dot array [173]. QCA transitions have been proposed as one of the alternative technologies to replace classical CMOS technology [174].

6.1.3 Electron shuttling

An important milestone for the implement of a spin-qubit quantum computer is the ability to enable mid- and long-range interactions. One possible solution is the implementation of coherent shuttling of single electrons within a quantum dot array. We previously introduced the existence of the quadruple point where the states (111), (011), (101) and (110) are degenerate. As it is shown later in the chapter, it is possible to individuate a two-dimensional cut in gate space where the three configurations (011), (101) and (110), each holding two electrons, are separated from each other by direct interdot charge transitions only.

As a consequence, it might be of interest to investigate the charge states surrounding the triangular (111) state reported in Fig. 6.1.3(b). Due to the reduced visibility of a single-charge state at the time using negatively compensated gates, we implemented another tomographic study. As Fig. 6.1.4(a) shows, for this series of acquisition, we fixed the value of ε_1^-, and we moved the biasing point of the sensor peak used in the compensation formula 5.2. By starting at high V_4^o detuning (the most right acquisition in Fig. 6.1.4(a)), the sensor peak is biased such that only the (111) state is highlighted, similarly to the acquisition presented in Fig. 6.1.3(b). In this gate-space two-dimensional plane, the (111) is the highest occupational configuration. In order to highlight the neighboring states, it is necessary to move the sensor biasing point V_4^o in equation 5.2 to lower values, due to the reduced total charge capacitively coupled to the sensor.

Moving from right to left in Fig. 6.1.4(a), we show that each charge state can be highlighted individually. The charge states occupation are labeled in agreement with simulations reported elsewhere [160, 161] as well as with the definition of the virtual gates introduced in previous section. In agreement with the reported dot-to-dot capacitances in Fig. 5.1.5, we observe that the least change in V_4^o is induced by the removal of an electron from G_2, the weakest dot coupled to the sensor dot. Following the same reasoning, the third acquisition in Fig. 6.1.4(a) shows a change in the removal of an electron in G_3. Further

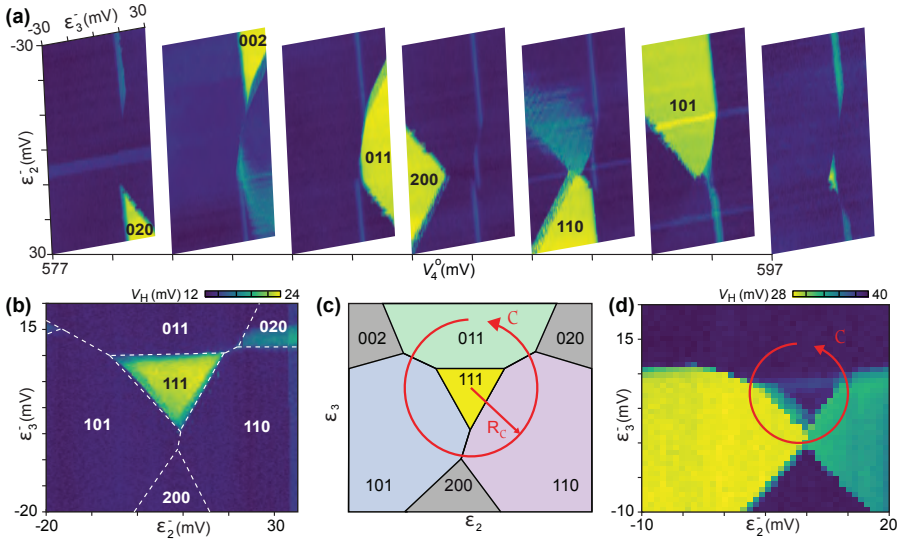


Figure 6.1.4 – (111) charge state configuration. (a) Tomographic acquisition for a fixed ε_1^- value. The horizontal axis represents the value of the sensor biasing point, V_4^o in formula 5.2. This allow us to highlight neighboring two-electron charge configurations, such as (011), (101) and (110). (b) Guides to the eye indicating different ground state configurations within one particular detuning plane. For this choice of sensor operating point, V_H does not discriminate between different two-electron configurations. (c) Sketch of the charge stability diagram for the same fixed ε_1^- configuration used in (a). C indicates a control-voltage path traversing two-electron ground states such that two isolated electrons are exchanged within the array, by sequentially relocating one electron at a time, without exchanging electrons with the leads. R_C is the radius of the control path. (d) Acquisition as in (b), but with different choice of sensor operating point. The resulting different intensities of of V_H allow the control experiment in Fig. 6.1.5.

moving to the left, we observe that the state (200) is highlighted before (011), meaning that the movement of an electron in G_1 has a less strong capacitive coupling compared to a pair of electron loaded in G_2 and G_3. This might be associated to the additional mutual capacitance, when the (011) state is occupied. The last two acquisitions at the lowest values of V_4^o agree again with the capacitive coupling configuration. Two electrons occupying G_3 induce a weaker potential shift on the sensor dot compared to the (020) configuration.

By combining the results just described, we report the charge stability diagram in Fig. 6.1.4(b).
With reference to Fig. 6.1.4(c) we report a sketch of the charge stability diagram, where we highlight one of the possible paths (a fixed circumference with radius R_C) to enable cyclic shuttling of two electrons within the array without exchanging them with the leads. In particular, by moving across the highlighted path, the initial position of two electrons is swapped within the array, as a single circular path is completed. By optimizing the readout point on the sensor, in Fig. 6.1.4(c) we report an optimal configuration to discriminate between the three different charge configurations [155].
In order to find the correct circular path that enables the shuttling of the two electrons, we perform a sweep as a function of the circumference radius R_C, as reported in Fig. 6.1.5(a). In this acquisition, we highlight three different shuttling regions. For small radius R_C, the system does not explore the (110) state. From the demodulated voltage we infer that the triple dot evolves between the states (011),(101) and (111), therefore exchanging electrons with the leads. On the contrary for too large radius R_C, we identify the presence of dark blue regions in between the evolution from (101) to (110), which we associate with the system exploring the charge state (200) therefore exchanging electrons with the leads once again. For intermediate values of R_C, in the order of 7.5 mV, we explore only the states of interest. As a consequence, we observe sharp jumps in the demodulated signal between blue-yellow and green.
In Fig. 6.1.5(b), we report the gate voltages sweeps applied to each individual gate in the quantum dot to perform the 7.5 mV circular sweep in negatively compensated parameter space, and the corresponding demodulated detected voltage in Fig. 6.1.5(c). This latter acquisition, reproduces a scenario in which two electrons are initialized in the quantum dots G_2 and G_3, then, as the demodulated voltage evolves to yellow, the electron underneath G_2 is moved to G_1. As the system explores the green region, the electron from G_3 is moved to G_1, and eventually the initial demodulated voltage is detected again, meaning that the same charge configuration has been reached again. In the actual

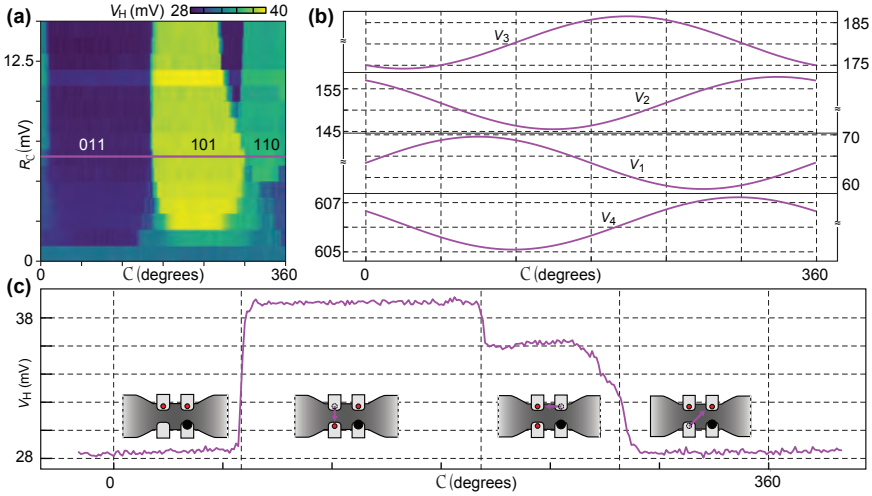


Figure 6.1.5 – Exchange of two electrons within a triple dot array. (a) Paramter sweep of the circumference radius R_C as a function of the circumference path in order to identify the correct path to shuttle the two electrons. The acquisition is performed in virtual negatively compensated gates, biased as shown in Fig. 6.1.4(d). For R_C values chosen too large or too small, leakage into undesired states is clearly visible by a change in V_H. (b) Gate voltage waveform used to perform the electron shuttling at the radius value indicated by the violet line in (a). (c) The charge sensor signal acquired during one cycle of the shuttling path C. V_H reflects the different arrangements of the two electrons in the array, as shown by red dots in the illustrations. At the end of the cycle C, the position of the two electrons in the array has been swapped without the need for the Heisenberg exchange interaction.

configuration the two electrons have been swapped. This charge shuttling might have induced a geometrical phase in the overall electronic wavefunction. However, the acquisition of a geometrical phase cannot be measured with the described setup. More advanced device geometries enabling interference experiment are could facilitate the observation of a geometrical phase after a single charge shuttling. Furthermore, the trajectory $f(V_1, V_2, V_3, V_4)$ is not only limited to the circular path C, but the same shuttling can be induced using a triangular C curve, or indeed arbitrary trajectory. The only requirement that the f function has to satisfy, is the condition of intersecting the

interdot lines, ensuring electron shuttling with protection against charge noise and software "error". This protection is intrinsic in the system, and it is owed to the presence of Coulomb blockade.

6.2 Detection of N-dimensional charge states

The knowledge of charge states in a multiple quantum dot system is essential to perform spin qubit experiments as well as to investigate the quantum dots electrostatic properties. Single and double quantum dots have been deeply investigated in the past two decades unveiling most of their electrostatic properties, enabling the implementation of LD and S-T_0 qubits. Already the addition of a third quantum dot has shown to drastically increase the complexity in the understanding of the charge ground states, due to the three-dimensional nature of the charge state. The understanding of higher dimensional charge states becomes more complicated as larger quantum dot arrays are investigated, since two-dimensional projections become less useful to disentangle the arrangement of charge states.
These considerations hold true for any array of quantum dots, both in one- and two dimensions. In the pathological case of eight completely uncoupled quantum dots, the full charge state (1111111) could be easily investigated with the use of one-dimensional acquisitions. In fact, in this limit, the charge state could be seen as the eight-dimensional hypercube. The situation becomes more complicated when the capacitance matrix of the array becomes non-negligible, both for dot-to-dot and dot-to-gate capacitance elements.
One solution might be found in the exploration of charge states using ad hoc virtual gates, as we implemented in Fig. 6.1.4(b). However, this technique relies on an intuitive extension of the charge distribution, accessible in three dimensions, but hard to picture as soon as a higher dimension is entered. Studying four dimensional charge spaces might be possible implementing tomographic investigations, similarly to in Fig. 6.1.2. However, each single acquisition would be a three dimensional object and many of them should be acquired and combined into a four dimensional object. Despite being not easy

to be visualized from the human mind, it would also require the storing of a tremendous amount of data. This sets an important problem that has to be addressed in order to perform multiqubit experiments, where more than three quantum dots are involved.

So far, the scientific community has found a solution by sequentially loading with one electron at the time the array of quantum dots. By using virtual gates to control "physical" parameters, raster acquisitions have been enough to load the (11....1) state in these arrays [51, 55]. In the following two paragraphs we propose an alternative solution: a semi-automated method that enables the study of the distribution for the (111) manifold of the four quantum dot parameter space. By using a sparse acquisition we demonstrate that we dramatically reduce the number of acquired data points, enabling an overall speed-up of the acquisition procedure. Moreover, this technique is compatible with ray-based approaches implemented in machine learning techniques for automated tuning [175].

This technique can be straightforwardly extended to the (11111) state in a six quantum dot plaquette and eventually applied to a 3x3 array, with the sensor dot sitting in the middle (if a similarly strong capacitive coupling can be maintained in such a new platform). The understanding of these higher-dimensional charge states would then be limited to the classical computer controlling the quantum hardware, which can handle a N-dimensional charge boundary information more easily than a human brain. Such information might be useful to avoid the leakage and loading of unwanted electrons during the booting of a quantum simulator, where the working regime would be the (1111..1) state. This state is of particular interest for gate based spin qubits. For the LD qubit, the (11...11) state enables the implementation of the Heisenberg exchange interaction to perform two-qubit gates. Additionally it enables the quantum dot array to be initialized for the implementation of the S-T_0 architecture, enabling also the implementation of the Pauli spin blockade readout technique. Furthermore it also enables to inizialise and operate an array of exchange-only qubits.

We define this method semi-automated since the state detection is governed

by the device itself, depending on its response to the external stimulus.

6.2.1 Measurement setup

In this section we explain how we use the sensor dot G_4 to trigger the acquisition of the (111) charge state boundaries when a charging event changes the occupation of the triple dot G_1, G_2 and G_3. In Fig. 6.2.1(a) we report the setup for the semi-automated adaptive acquisition. The demodulated voltage obtained from the homodyne detector is amplified a thousand times via a voltage preamplifier. The amplification enables us to increase the maximum demodulated V_H, covering an extension of about 5 V. By exploiting the negatively compensated gates, the demodulated voltage is going to to be 0 V when the system is configured within the (111) state, jumping to 5 V when electrons are rearranged within the triple dot array, moving the sensor demodulated voltage from a Coulomb peak to a valley. As a consequence, the time evolution of the signal looks like a sharp step-function, anytime the boundary of the (111) charge state is crossed. V_H can then be can be used as a trigger-input signal to arm an instantaneous acquisition of a digital instrument, which in our case is a digital multimeter Keysight 34456A, with a sample rate of 50 kSa/s. The device gates are supplied with four ramp-like signals synced together and produced by a Qdevil DAC. Additionally, a fifth ramp, with range from 0 to 1 V, synced with the device ramps, is supplied to the input port of the digital multimeter.

As a first step, we identify a gate parameter space point positioned in the middle of the (111) state, extracted from measurements presented in Fig. 6.1.1. Subsequently, we have to identify a volume in parameter-space that is going to contain the full extension of the (111) charge state. In order to achieve this task, we decide to enclose the volume explore by the DAC ramps in a sphere. Since it is not trivial to evenly distribute points on the surface of a sphere, we make use of the Fibonacci series which enables to distribute points as reported in Fig. 6.2.1(b). We can define sets of four voltage ramps that can be used to explore the volume of the sphere as reported in Fig. 6.2.1(c). While the

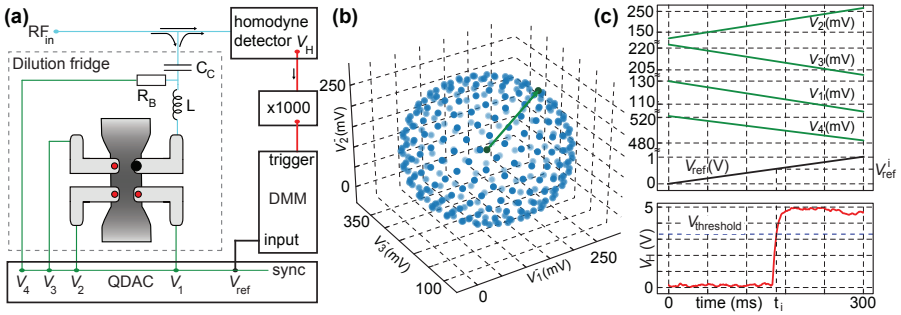


Figure 6.2.1 – Triggered acquisition setup. (a) Setup for the acquisition of high dimensional charge states. Abrupt changes in the demodulated signal V_H are used as a trigger to acquire time stamps (V^i_{ref} values). The input of the multimeter is a reference voltage ramp which is synced with the gate channels. (b) Scanning of a high-dimensional sphere in parameter space (here V^-_1, V^-_2, V^-_3) by a large number of automatically generated 1D rays (arranged here on a Fibonacci grid). Each ray results in the acquisition of only one time stamp, thereby resulting in a sparse acquisition (c) Execution of one ray. The QDAC generates five linear ramps $V_i(t)$; $V_1, .., V_4$ are applied to the cryostat, while V_{ref} is applied to the input of the DMM and encodes the time stamp. When the DMM receives the trigger *i*, it acquires one measurement $V^i_{ref} = V_{ref}(t = t_i)$, which serves as a time stamp. After the acquisition of many time stamps, data points $V^-_{1..4}(t = t_i)$ can be reconstructed numerically. For illustrative purposes, $V_H(t)$ was also recorded, illustrating how its crossing of a user-defined threshold triggers one time stamp.

first three ramps move the system inside the sphere, the fourth one on V_4, is used to perform negative compensation on the sensor gate, such that the demodulated signal would be 0 V as long as the charge state is biased in the (111) configuration. An example of the acquisition performed is reported in the bottom panel of Fig. 6.2.1(c). The demodulated voltage stays constant at 0 V as long as the triple dot hosts one single electron per quantum dot, and it suddenly jumps to 5 V, as soon as the charge is rearranged. As the jump happens, the multimeter is triggered to acquired one single point V^i_{ref}, corresponding to the time stamp of the (111) boundary $V^-_{1..4}(t = t_i)$. In our case the threshold voltage of the multimeter is set to 3.3 V (blue line in Fig. 6.2.1(c) bottom panel).

We define the technique semi-automated since the user has to manually bias

the system somewhere within the charge state. It is possible to fully automate the procedure, where for example we could use the V_{CM} gate introduced in Fig. 6.1.1(b) to automatically find a point inside the charge state, or use machine learning techniques [176, 177].

6.2.2 Triple dot charge state in three dimensions

Initially, we applied this method to the acquisition of a two dimensional charge stability diagram using negative compensated gates, as reported in Fig. 6.2.2(a) and (b). As the compensation has been optimized, the system is biased at the center of the (111) charge state, identifying its maximum extensions using a coarse raster scan. Subsequently, we defined 300 points belonging to the surface of a circle enclosing the state (following the same process used for a sphere in three dimensions) and started the triggered acquisition using a procedure similar to the one explained in the previous section. As explained in the previous section, we would expect the setup to be trigger for any point along the red line manually sketched in Fig. 6.2.2(a). The results are reported in Fig. 6.2.2(b) and, as visible, the state be unequivocally traced back to Fig. 6.2.2(a).
The acquisition presented in (a), consists of a two-dimensional map that has been acquired with 80x50 points. However, only 2x50 points are of interest in order to perform spin qubit experiments, which represent the boundary of the charge state (within the blue area, the array is in a Coulomb valley ground state). The total acquisition time was 180s. Therefore, roughly 97% of the acquisition can be regarded as not useful, leading to an unnecessary acquisition overhead time (the overhead increases as higher resolution acquisitions are required). On the contrary, the triggered acquisition mode is only sensitive to non-equilibrium points, where the number of electron changes within the array, avoiding the integration of points in region of constant charge. By using this method, the 300 points on the surface of the charge state has been acquired in 76 s, using ramp-like waveforms with a 300 ms period. On a single two-dimensional map, the speed-up is not as significant, but it starts to become more sizable for the full three-dimensional (111) charge state. In fact, in order

to have the same resolution as Fig. 6.2.2(a) extended to the third dimension, 80 more heat maps should be acquired, increasing the acquisition. However, already in two dimensions the number of acquired points is reduced by a factor of 40, freeing memory in the quantum dot array classical control unit.

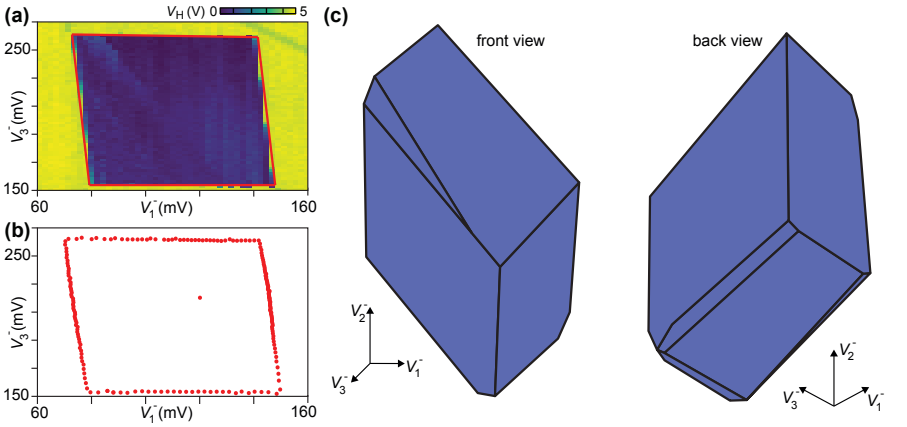


Figure 6.2.2 – Sparse acquisition for double and triple dots. (a) Conventional raster acquisition of the (111) charge stability diagram in two-dimension using negatively compensated gates, number of points: 40000. The red line indicates the data points of interest to perform spin-qubit experiments, number of points: 100. (b) Sparse acquisition in the same region of parameter space using technique described in Fig. 6.2.1. Number of acquired time stamps: 100. (c) Sparse acquisition of the (111) state using negatively compensated gates in three dimensions. Number of acquired time stamps: 100000. Each time stamp has been converted to a three-dimensional coordinate (V_1^-, V_2^-,V_3^-). For illustrative purposes, surfaces have been generated using convex hull, and measured manifold is shown from front and back.

Therefore, we mapped out the surface of a sphere containing the (111) surface and we performed the triggered acquisition with ramps rate set to 300 ms. The result is reported in Fig. 6.2.2(c), and the acquisition of 10^5 points on the facets of this state took 6 hours. In comparison, the same resolution of the (111) state boundaries using a raster tomographic acquisition of two-dimensional heat maps would have required 83 hours. Furthermore, due to hardware limitation, the ramps frequency was limited to 3.3 Hz. However,

the bandwidth of the low frequency lines is 2 kHz and therefore we expect to significantly improve the acquisition time, which we estimate to reach 15 minutes at full bandwidth. This sparse acquisition method has the additional advantage of drastically reducing the number of acquired data points. In fact, the same amount of information contained in the 10^5 points sparse acquisition, would have required the storing of 10^7 points using raster scans.

The acquired charge state is reported in Fig. 6.2.2(c) and presents differences from a simulated triple dot charge state, as the one reported in Fig. 5.2.2(b). Interestingly, it seems that the corners of the state have mostly cusp shapes (compare with the sketch of a triple dot charge state in Fig. 5.2.2(b)). This effect could be analogous to how a pure double dot evolves from an hexagon to a tetragon, when it is projected on the surface of a triple dot, as reported in the comparison of Fig. 5.2.2(g) and (h). Some of the facets of a triple quantum dot still appears in an hexagonal-like shape, recalling the shape of a double quantum system (reference to the simulated three-dimensional charge state in Fig. 5.2.2(b)). Analogously, one of the facets of the (1117) state might be a similar copy of the (1110) ground state. However, we cannot prove this hypothesis yet, since we do not have the capability to compensate on any other dot-to-lead transition in this configuration, but for G_4.

Further work is required to obtain a higher resolution of the charge state we presented in Fig. 6.2.2(c), especially for the corners. From electrostatic simulations, corners seem to host regions where most of the QCA transitions happen. Possible solutions involve the implementation of more advanced algorithms for edge detection. For example one could imagine to proceed as follows: the first step is to use a ray to find one point on the surface of the charge state. Subsequently, the algorithm controls the gates in such a way that they move along the surface of the charge state, instead of restarting each time from the center of the charge state.

Moving in this direction, we have already implemented a first step toward a more advanced code which aims at speeding-up the acquisition time. It works as follows. An initial ray finds one point on the surface of the charge state. Subsequently, the second ray investigates a parameter space reduced to +/-

10% of the previously identified $\vec{V}^{-}$ triplet of points along the radial direction, instead of exploring the full radius. For the following rays, the central point of the investigated window is updated each time a new $\vec{V}^{-}$ is acquired.
As the plaquette is extended to six quantum dots in a 3x2 array, the sensor is able to detect the charge rearrangement of a quintuple quantum dot system. In order to individuate the state, the computer would define the surface of a five-dimensional hypersphere and subsequently sweep six-dimensional rays in order to identify the boundary of the charge state. As the parameter space which loaded the (11111) state is individuated, the boundary of such charge state would only be saved within the classical controller of the array, defining the working hypervolume of the computation.

7

Conclusion and Outlook

In this thesis we analyzed two valuable platforms for the implementation of a spin-qubit quantum computer: university fabricated Si/SiGe quantum dot devices as well as fully CMOS compatible foundry-fabricated quantum dot devices.

In chapter 4 we investigated the properties of a single-layered triple quantum dot device fabricated on Si/SiGe heterostructures. Exploiting an rf-SET charge sensor in the close proximity to the quantum dots device, we demonstrated the ability to form single, double and triple quantum dots, reaching the single electron occupation. Using the single quantum configuration, we demonstrated single-shot readout of a single spin using the Elezerman protocol at an integration time of 24 μs with SNR = 3.4, comparable with state-of-the-art results. Single-spin readout is essential for the implementation of

Loss-DiVincenzo qubits. Despite the results obtained, these devices showed reduced control over the tunnel coupling and reproducibility of the quantum dots. In order to overcome these limitations, we demonstrated first results toward the implementation of more advanced quantum dot devices, using the overlapping-gate geometry. Using superimposed aluminum gates with a reduced gate pitch, such a geometry enables a higher degree of control of the quantum dots, leading to more reproducible quantum dot devices over many fabrication runs. Despite a seemingly working fabrication recipe, the formation of quantum dots has proven complicated, especially due to the low quality of the oxide interface between the ohmic regions and the accumulation top gates, leading to leaking devices. We associated such behavior to a non-ideal treatment of the silicon surface before the deposition of the ALD oxide layer.
In chapter 5 we investigated the properties of a 2x2 array of quantum dots in a fully CMOS compatible foundry-fabricated quantum dot device. The four quantum dots showed similar charging energies as well as similar lever arms. The device was investigated using gate-based dispersive readout, a technique that would enable to operate qubit arrays without the need for additional charge sensors, drastically reducing the number of control lines for a spin-qubit quantum computer. We demonstrated the ability to reach the single occupation for each single quantum dot. Implementing charge sensing using a dispersive readout technique, we demonstrated the ability to form double and triple dots in the last occupation regime, overcoming the limitations of a readout technique solely based on dispersive signals. Exploiting the presence of a general top gate, we demonstrated the ability to tune the interdot and dot-to-lead tunneling rates for single electrons within the array over few order of magnitude. We also demonstrated the ability to perform single-shot readout of a charge state with 10 μs integration time with SNR = 1.43, comparable with state-of-the art results.
In chapter 6, implementing the readout techniques developed in chapter 5 we showed the study of the three-dimensional (111) triple dot charge state, being one of the facets of a higher dimensional four charge state. Implementing virtual gates, we individuated a line-cut in the three-dimensional charge state

that enabled us to shuttle two electrons within the the 2x2 plaquette without exchanging the electrons with the electronic reservoirs. Furthermore, using the charge sensing technique, we showed a semi-automated procedure for the acquisition of the (111) state which drastically reduced the acquisition as well as the number of stored data points compared to traditional two-dimensional raster acquisitions. This technique is compatible with ray-based approaches implemented in machine learning techniques for automated tuning.

The work described in this thesis opens up opportunities for many new experiments.

The demonstration of single-electron control in a 2x2 plaquette of quantum dots in foundry-fabricated devices has been reported for the first time. The next step will move toward the identification of spin signatures. In fact all the data presented in both chapters 5 and 6 were taken in the absence of a magnetic field. The most straightforward demonstration of spin-qubit capabilities for such a device would be the implementation of an exchange-only qubit, given the ability to form triple dots in the (111) configuration and the readout visibility offered by the negatively compensated gates technique.

Another direction could be the implementation of Loss-DiVincenzo qubits. Firstly, we would demonstrate the ability to perform Elezerman readout in these devices, similarly to the results reported in chapter 4. Regarding the control of the single-electronic spin, we will work toward the implementation of micromagnet technology for EDSR manipulation. Micromagnets could be deposited either in-house using ferromagentic materials as Co or outsourced to the foundries (for example using CMOS compatible permalloy materials). Alternatively, the investigation of spin-orbital-valley interactions to induce spin rotations would be an interesting route to develop LD qubit gates.

As qubit functionalities will be demonstrated, the following step would deal with the implementation of two-qubits gates. Working with LD qubits, it might be of interest to explore the capabilities of the sensor dot as a coupling element. For example, by fast pulsing two LD into the sensor dot we could activate the onsite exchange interaction to boost quality factor of the gate. In order to investigate mid-range interactions, charge- and spin-shuttling exper-

iments can be performed in longer arrays. Such advanced devices have been already fabricated by the foundry CEA-LETI, as shown in the back cover of this thesis. Eventually, long-range interactions might be investigated using superconducting coplanar waveguide resonators. The strong lever arms measured in these devices would be highly beneficial to obtain elevated visibility.
Regarding material improvement, the implementation of isotopically purified SOI wafers for the fabrication of the silicon nanowire transistors would boost the coherence times of spin qubits in these foundry-fabricated devices. Such a technology is already available in the foundry at CEA-Leti.
On a more fundamental research direction, further development of the shuttling experiment presented in chapter 6 will be required to understand either the presence or the absence of a geometrical phase acquired by two electrons as their position is swapped within the array. We believe that these experiments will require more advanced architecture, as 2x4 arrays of quantum dots. In these devices, by embedding the reflectometry circuit on the outer-most pairs of split-gates, the inner 2x2 plaquette could be used as a platform to perform interference experiments. This might help to disentangle the effective electronic wavefunctions of the electrons.
The same device could be used to investigate the study of higher dimensional charge states, where a five quantum dot can be initialised in the state (11111) using negative compensated gates. Interesting experiment can be devoted to the development of techniques for automated tuning using machine learning, exploiting the ray-based approach.
More in general, investigating higher dimensional charge states could shed light on more exotic charge transitions where groups of electrons are loaded and moved simultaneously within the array. These effects would represent signatures of quantum cellular automata transitions, predicted to enable logic operations.

A

Fabrication Notes

The following pages describe the fabrication implemented for the single gate design as well as the overlapping gate geometry Si/SiGe devices presented in chapter 3.

A.1 Substrate preparation

NbTiN Marker - Elionix 100 keV

- Spinning double layer resist, EL9 at 4000 rpm and baking for 1 minutes at 185°C, then A4 at 4000 rpm and baking for 2 minutes at 185°C
- Exposure using parameters : 20000 px and 600 µm writing field, with a current of 5 nA (120 um aperture) and a dose of 900 µC/cm^2

- Development in MIBK-IPA:1-3 for 60 seconds and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 1 minute
- DC plasma sputtering of NbTiN. The holder oriented 20° with respect to the horizontal position. Pressure during the DC sputtering is 4 mTorr of N/Ar mixture, with a power of 200 W. Run twice the 10 minute program. Deposition of around 200 nm for good contrast with silicon during EBL alignment step.
- Lift-off in NMP at 85° for 30 minutes and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 4 minute

Mesa etching - Heidelberg μPG501

- Spinning single layer resist, Az1505 at 4000 rpm and baking for 2 minutes at 115°C
- Exposure with using 21 ms exposure time and -2 defocusing.
- Development in MF321 for 35 seconds slowly moving the sample and rinsing in milliQ for 60 seconds
- Ashing in oxygen plasma for 4 minute
- Etching process using Kauffman milling. Set the Ar flow at 15 sccm and pressure of 1 mBar. Set the beam voltage to 600 V and the other parameters to the default value. Warm ups 2 min and put the stage 45 °C with respect the source, with rotation. Sputtering for 5:30 minutes (around 80-90 nm etch)
- Lift-off in NMP at 85° for 30 minutes and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 4 minute

Implantation regions - Heidelberg μPG501

- Spinning single layer resist, Az1505 at 4000 rpm and baking for 1 minutes at 115°C, then Az1505 at 4000 rpm and baking for 2 minutes at 115°C

- Exposure with Heidelberg writer, using 21 ms exposure time and -2 defocusing.
- Development in MF321 for 35 seconds slowly moving the sample and rinsing in milliQ for 60 seconds
- Ashing in oxygen plasma for 4 minute
- Baking for 2 minutes at 120 °C.

Implantation regions

The implantation process has been outsourced to an external company, Kroko inc. in the United States. We first simulated the dose and energy of phosphorus atoms using SRIM software, with the following results: We then implemented

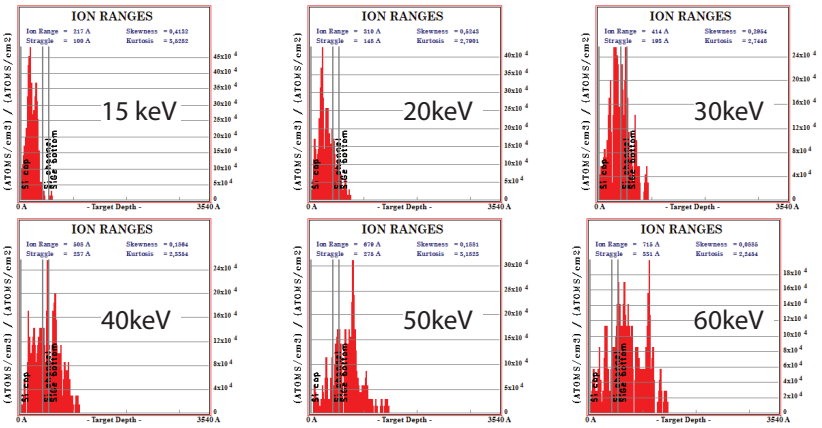


Figure A.1.1 – SRIM simulation for 12/40 Si/SiGe substrate.

the following parameters:

- 1st step: 30 keV, deposition of 1x10^{15}cm^{-2}
- 2nd step: 15 keV, deposition of 1x10^{15} cm^{-2}

Activation

- Lift-off in NMP at 85° for 30 minutes
- Ashing in oxygen plasma for 4 minute
- Activation using the room temperature annealer. Anneal at 700 °C for 3 minutes in nitrogen atmosphere.

Au Marker - Elionix 100 keV

- Spinning double layer resist, EL9 at 4000 rpm and baking for 1 minutes at 185°C, then A4 at 4000 rpm and baking for 2 minutes at 185°C
- Exposure using parameters : 20000 px and 600 µm writing field, with a current of 5 nA (120 um aperture) and a dose of 900 µC/cm^2
- Development in MIBK-IPA:1-3 for 60 seconds and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 1 minute
- Metalization with Ti/Au - 5/100 nm. Ti deposited with a rate of 1 Å/s and Au with 3 Å/s.
- Lift off in dioxolane at RT and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 4 minute

A.2 Single-layered devices

ALD deposition and liftoff procedure- Elionix 100 keV

- Spinning double layer resist, EL13 at 4000 rpm and baking for 1 minutes at 185°C, then CSAR4 at 4000 rpm and baking for 2 minutes at 185°C
- Exposure using parameters : 20000 px and 600 µm writing field, with a current of 40 nA (240 um aperture) and a dose of 335 µC/cm^2
- Development in oxylane for 60 seconds and MIBK-IPA:1-3 for 30 seconds at room temperature.

- Ashing in oxygen plasma for 60 seconds
- ALD deposition of 20 nm of HfOx at 90 °C, pulsing Hf precursor for 0.4 s and waiting 100s and then pulsing milliQ for 0.03 s and waiting 300s. 200 cycles.
- Lift-off in NMP at 85° for 30 minutes and subsequent dioxolane at RT. Rinsing in IPA for 60 seconds. Sonication at 80 kHz.
- Ashing in oxygen plasma for 4 minute

Inner gates - Elionix 100 keV

- Spinning single layer resist, A2 at 4000 rpm and baking for 10 minutes at 185°C
- Exposure using parameters : 240000 px and 150 μm writing field, with a current of 100 pA (40 um aperture) and a dose of 1500 μC/cm^2
- Development in IPA-milliQ : 7-3 for 2:30 minutes at -5°C. (Half an hour for temperature thermalization of the bath)
- Ashing in oxygen plasma for 20 seconds
- Metalization with Ti/Au - 3/17 nm. Ti deposited with a rate of 0.7 Å/s and Au with 2.1 Å/s.
- Lift-off in NMP at 85° for 30 minutes and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 4 minute

Outer gates and pads - Elionix 100 keV

- Spinning double layer resist, EL9 at 4000 rpm and baking for 1 minutes at 185°C, then CSAR9 at 4000 rpm and baking for 2 minutes at 185°C
- Exposure using parameters : 20000 px and 600 μm writing field, with a current of 40 nA (240 um aperture) and a dose of 335 μC/cm^2
- Development in oxylane for 30 seconds and MIBK-IPA:1-3 for 30 seconds at room temperature.

- Ashing in oxygen plasma for 20 seconds
- Metalization with Ti/Au - 5/250 nm. Ti deposited with a rate of 0.7 Å/s and Au with 3.5 Å/s.
- Lift-off in NMP at 85° for 30 minutes and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 4 minute

A.3 Overlapping gate geometry devices

ALD deposition and etching procedure

- BHF dip for 30s and rinsing in milliQ for 2 minutes
- ALD deposition of 10 nm of HfOx at 150 °C, pulsing Hf precursor for 0.2 s and waiting 90s and then pulsing milliQ for 0.5 s and waiting 90s. 150 cycles.
- Spinning single layer resist, Az1505 at 4000 rpm and baking for 2 minutes at 115°C
- Development in MF321 for 35 seconds slowly moving the sample and rinsing in milliQ for 60 seconds
- Ashing in oxygen plasma for 4 minute
- Post baking for 2 minutes at 120°C
- Etching in BHF for 5 minutes and after rinsing in milliQ for 2 minutes in room temperature water
- Lift off in dioxolane at RT and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 4 minute

Outer gate layer - Elionix 100 keV

- Spinning double layer resist, EL13 at 4000 rpm and baking for 1 minutes at 185°C, then A4 at 4000 rpm and baking for 2 minutes at 185°C

- Exposure of the inner gates using parameters : 20000 px and 600 μm writing field, with a current of 5 nA (60 um aperture) and a dose of 1200 μC/cm^2. Exposure of the outer gates using parameters : 20000 px and 600 μm writing field, with a current of 40 nA (250 um aperture) and a dose of 1200 μC/cm^2. In this layer the overlapping area between top gates and implanted region is not exposed
- Development in MIBK-IPA:1-3 for 80 seconds and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 1 minute
- Kaufmann milling for 1 minute with default settings, but beam voltage at 600V. 15 sccm Argon flow and 1 mTorr pressure. Inclination 45 depress with rotation and warming up 2 minutes.
- Metalization with Ti/Au - 5/160 nm. Ti deposited with a rate of 1 Å/s and Au with 3 Å/s. During the evaporation is tilted 20° with respect to the crucible and the stage is rotating at constant speed
- Lift off in dioxolane at RT and rinsing in IPA for 60 seconds
- Ashing in oxygen plasma for 2 minute

Screening gate layer - Elionix 100 keV

- Spinning single layer resist, A2 at 4000 rpm and baking for 10 minutes at 185°C
- Load the sample, settle the current and then let the system at rest for 30 mins (T and beam current settling). Exposure using parameters 240000 px X 600 μm writing field, with 300 pA current (40 um aperture) and dose fo 1600 μC/cm2. The CAD file was biased -10nm in beamer. Aligned using automatic alignment.
- Development in IPA-milliQ : 7-3 for 2:30 minutes at -5°C. (Half an hour for temperature thermalization of the bath)
- Development in MF321 for 35 seconds slowly moving the sample and rinsing in milliQ for 60 seconds

- Ashing in oxygen plasma for 45 seconds
- Metalization with Al 18 nm deposited with a rate of 2 Å/s
- Lift off in dioxolane at RT and rinsing in IPA for 60 seconds. Sonication at 80 kHz
- Ashing in oxygen plasma for 2 minute
- Post baking for 15 minutes at 185°C

Plunger gate layer - Elionix 100 keV

- Spinning double layer resist, A2 at 4000 rpm and baking for 2 minutes at 185°C, then A2 at 4000 rpm and baking for 10 minutes at 185°C
- Load the sample, settle the current and then let the system at rest for 30 mins (T and beam current settling). Exposure using parameters 240000 px X 600 μm writing field, with 300 pA current (40 um aperture) and dose of 1600x1.125 μC/cm2. During this lithograohy step, we also exposed the overlapping area between top gates and ohmic regions (see Fig. 3.2.3(a)). The CAD file was biased -10nm in beamer. Aligned using automatic alignment.
- Development in IPA-milliQ : 7-3 for 2:30 minutes at -5°C. (Half an hour for temperature thermalization of the bath)
- Development in MF321 for 35 seconds slowly moving the sample and rinsing in milliQ for 60 seconds
- Ashing in oxygen plasma for 45 seconds
- Metalization with Al 35 nm deposited with a rate of 2 Å/s
- Lift off in dioxolane at RT and rinsing in IPA for 60 seconds. Sonication at 80 kHz
- Ashing in oxygen plasma for 2 minute
- Post baking for 15 minutes at 185°C

Barrier gate layer - Elionix 100 keV

- Spinning double layer resist, A2 at 4000 rpm and baking for 2 minutes at 185°C, then A2 at 4000 rpm and baking for 10 minutes at 185°C
- Load the sample, settle the current and then let the system at rest for 30 mins (T and beam current settling). Exposure using parameters 240000 px X 600 μm writing field, with 300 pA current (40 um aperture) and dose of 1600x1.2 μC/cm2. The CAD file was biased -10nm in beamer. Aligned using automatic alignment.
- Development in IPA-milliQ : 7-3 for 2:30 minutes at -5°C. (Half an hour for temperature thermalization of the bath)
- Development in MF321 for 35 seconds slowly moving the sample and rinsing in milliQ for 60 seconds
- Ashing in oxygen plasma for 45 seconds
- Metalization with Al 35 nm deposited with a rate of 2 Å/s
- Lift off in dioxolane at RT and rinsing in IPA for 60 seconds. Sonication at 80 kHz
- Ashing in oxygen plasma for 2 minute

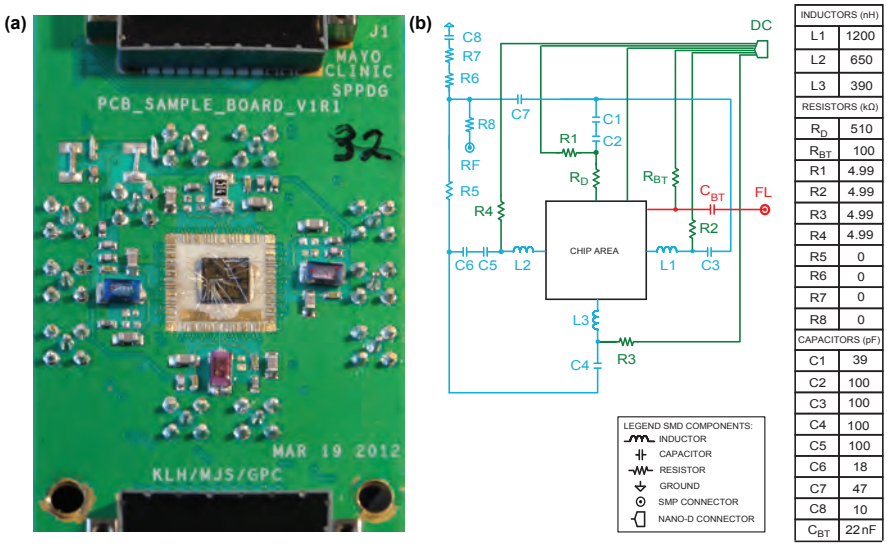
B

Measurement Notes

In this appendix we illustrate the components of the sample holder used in this thesis work, supplementary data for the characterization of single split gate devices introduced in table 5.1.1 as well as the theory used in the simulations presented in section 3.2.2.

B.1 Sample boards

In Fig. B.1.1 we report the sample holder configuration for the Elzerman readout experiment performed in chapter 4. The component for this sample holder are all non-magnetic.



INDUCTORS (nH)	
L1	1200
L2	650
L3	390
RESISTORS (kΩ)	
R_D	510
R_{BT}	100
R1	4.99
R2	4.99
R3	4.99
R4	4.99
R5	0
R6	0
R7	0
R8	0
CAPACITORS (pF)	
C1	39
C2	100
C3	100
C4	100
C5	100
C6	18
C7	47
C8	10
C_{BT}	22 nF

Figure B.1.1 – Mayo board configuration. (a) Photograph of the PCB sample holder connecting to the cryostat via two low-frequency nanoD connectors (top and bottom) and eleven SMP high-frequency connectors (each mounted from the back side via five through-holes). Three inductors (purple and blue SMDs), one decoupling resistor (black SMD marked 514), as well as some of the bias tees (smaller SMDs) can be identified. Some components are positioned on the back side of the PCB. (b) Simplified circuit schematic of the PCB, showing signal paths associated with low-frequency control voltages (green), high-frequency control voltages (red), and rf reflectometry signals (blue). Isolated crossings are achieved by using a multilayer PCB. For clarity, only one high-frequency (low-frequency) bonding pad in red (green) is shown in the upper right corner of the chip area. Symbols are specified in the legend. SMD values are specified in the table.

In table B.1.1 we report th values for the sample holder used for the study of the Si/SiGe overlapping gate geometry device presented in chapter 4 as

well as the characterization of the 2x2 CMOS quantum dot array presented in chapter 5 and chapter 6. The labeling of the electrical components are referred to Fig. 3.1.1. The component for this sample holder are all non-magnetic.

C_{LP}	R_{LP}	C_{BT}	R_{BT}	C_{C1}	C_{C2}	R_B	C_{LP1}	R_{LP1}	L_1	L_2	L_3	L_4
1 nF	1.2 kΩ	25 nF	50 kΩ	100 pF	22 pF	5 kΩ	5.1 nF	2 kΩ	1200 nH	820 nH	560 nH	390 nH

Table B.1.1 – Copenhagen motherboard and daughterboard configuration. Copenhagen board stuffing with reference to Fig. 3.1.1.

In the following list we report the manufacturer part number for the Mayo board electronic components: L_1: 1206CS-122XJL, L_2: 1206CS-621XGLB, L_3: 1206CS-391XJL, R_{BT}: RR0510P-104-D, R_1: RR0510P-4991-D, R_2: RR0510P-4991-D, R_3: RR0510P-4991-D, R_4: RR0510P-4991-D, C_1: VJ0402A390JNAAJ, C_2: VJ0402A101JNAAJ, C_3: VJ0402A101JNAAJ, C_4: VJ0402A101JNAAJ, C_5: VJ0402A101JNAAJ, C_6: VJ0402A180JNAAJ, C_7: VJ0402A470JNAAJ, C_8: VJ0402A100JNAAJ and C_{BT}: GCM21B5C1H223JA16L.
In the following list we report the manufacturer part number for the Copenhagen sample holder electronic components: R_{LP}: RG1005P-122-B-T5, C_{LP}: 720-1229-2-ND, C_{BT}: GRM21B5G1H223FA012, R_{BT}: RG1005P-4992-B-T5, C_{C1}: VJ0402A220JNAAJ, C_{C2}: VJ0402A101JNAAJ, R_B: NRG1005P-502D, L_1: 1206CS-122XJL, L_2: 1206CS-821XJL, L_3: 1206CS-561XJL and L_4: 1206CS-391XJL.

B.2 Simulation of the foundry devices

The thickness of the SOI channel is $t_{Si} = 7$ nm, and the thickness of the BOX is $t_{BOX} = 145$ nm. The top metal line sits 300 nm above the channel. The front gates stack is made of 6 nm of SiO_2 , 5 nm of TiN, and 45 nm of n-doped poly-silicon (N_d= 2x10^{19} cm^{-3}). The same 6 nm thick layer of SiO_2 separates

the Si channel from the nitride (Si_3N_4) in the spacers. The source and drain are raised by 20 nm beyond "spacer0" and are also n-doped ($N_d = 10^{20}$ cm^{-3}). The density of donors under "spacer0" decreases at a rate of 1 decade every 4 nm. The silicon substrate below the BOX is assumed to be slightly p-doped ($N_a = 10^{15}$ cm^{-3}). The dielectric constants of the materials are $\varepsilon_{Si} = 11.7$, $\varepsilon_{SiO2} = 3.9$, and $\varepsilon_{Si3N4} = 7.5$. The potential in the device is computed with a Poisson solver. The source, drain, polysilicon gate and substrate are dealt with self-consistently in the Thomas-Fermi approximation. Namely, the density of carriers in these areas is computed from the local relations:

$$\begin{aligned} n(\vec{r}) &= N_c(T) F_{1/2}\left[-(E_c) - eV(\vec{r}) - \mu)/(k_B T)\right] \\ p(\vec{r}) &= N_c(T) F_{1/2}\left[+(E_c) - eV(\vec{r}) - \mu)/(k_B T)\right] \end{aligned} \tag{B.1}$$

where μ is the chemical potential (that may be different in the source/drain, gate and substrate), T is the temperature, and $F_{1/2}$ is a Fermi integral. The density of ionized impurities is computed with an incomplete ionization model valid at low temperatures and above the Mott transition [178].

We account for the formation of a ~ 0.25 eV high Schottky barrier at the poly-silicon/TiN interface, as suggested by the threshold voltage shifts measured at room temperature in similar transistor devices with a pure poly-silicon gate (missing TiN). As a consequence, the electrostatic potential is about 0.225 eV larger in poly-silicon than in TiN at a given electro-chemical potential in a front gate.

For numerical convenience, the above equations are solved at T = 4.2K (but there is no significant change in the electrostatics below at least 20K). The one-electron states in the resulting potential are computed in the anisotropic effective mass approximation. The low-energy states belong to the Z valleys (the valley splitting is not accounted for in the present approximation). We then map the energies and wave functions of the four lowest-lying states of the

+Z valley onto the following Hamiltonian:

$$H = \begin{pmatrix} E_{Q1} & t_{\parallel} & t_d & t_{\perp} \\ t_{\parallel} & E_{Q2} & t_{\perp} & t_d \\ t_d & t_{\perp} & E_{Q3} & t_{\parallel} \\ t_{\perp} & t_d & t_{\parallel} & E_{Q4} \end{pmatrix} \tag{B.2}$$

where E_{Qi} are the energies of the (isolated) dots, $t_{\parallel}$ is the tunnel coupling between neighbouring dots along the wire, $t_{\perp}$ is the tunnel coupling between opposite face-to-face dots, and t_d is the tunnel coupling between dots in diagonal positions. In particular, at resonance $E_{Q1} = E_{Q2} = E_{Q3} = E_{Q4} = E_0$ the eigenenergies and parity of the wave functions within the dots are:

$$\begin{aligned} E_1 &= E_0 + t_{\parallel} + t_d + t_{\perp}; \psi_1 = [1,1,1,1] \\ E_2 &= E_0 - t_{\parallel} - t_d + t_{\perp}; \psi_1 = [1,-1,-1,1] \\ E_3 &= E_0 + t_{\parallel} - t_d - t_{\perp}; \psi_1 = [1,1,-1,-1] \\ E_4 &= E_0 - t_{\parallel} + t_d - t_{\perp}; \psi_1 = [1,-1,1,-1] \end{aligned} \tag{B.3}$$

which allows for a straightforward fit of $t_{\parallel}$, t_d and $t_{\perp}$ on the simulation data. Resonance is simply achieved in the present (highly symmetric) device by applying the same voltage on all four front gates.

B.3 Single split-gate devices

We present the acquisition that were used to extract the charging energy and lever arm for the two additional devices described in table 5.1.1. These two devices belong to the same wafer of device 2S29-2 introduced in chapter 5 and 6. With reference to the device dimension reported in Fig. 3.2.5, the devices have the following dimensions:

- Device 1S11-2 in Fig. B.3.1: W= 90nm, L_G=50 nm and S_V=60 nm
- Device 1S11-1 in Fig. B.3.2 : W= 90nm, L_G=50 nm and S_V=60 nm

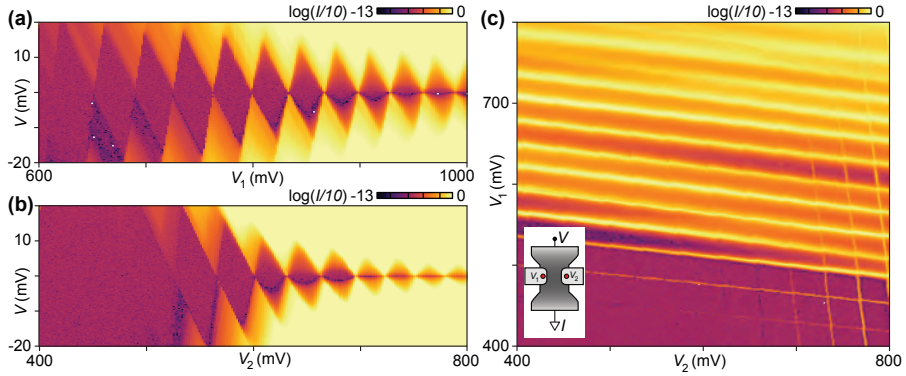


Figure B.3.1 – Device 1S11-2 characterization. (a) Coulomb diamond for the quantum dot sitting underneath gate V_1 with reference to the sketch in (c). (b) Coulomb diamond for the quantum dot sitting underneath gate V_2. (c) charge stability diagram measured in transport for the parallel double dot formed from V_1 and V_2 at a 1 mV bias.

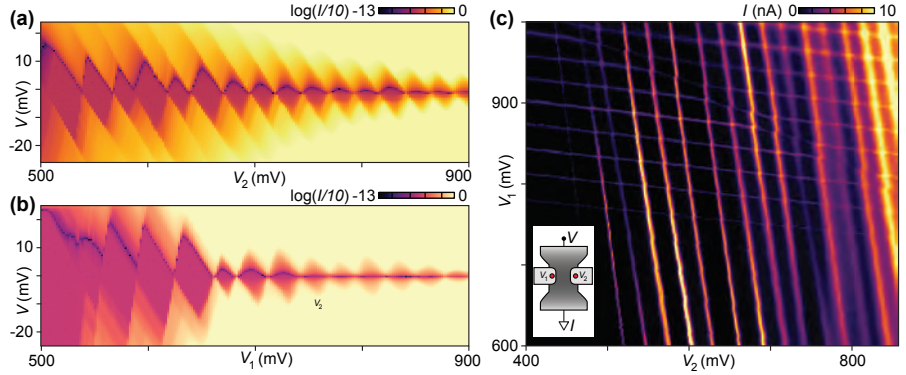


Figure B.3.2 – Device 1S11-1 characterization. (a) Coulomb diamond for the quantum dot sitting underneath gate V_1 with reference to the sketch in (c). (b) Coulomb diamond for the quantum dot sitting underneath gate V_2. (c) charge stability diagram measured in transport for the parallel double dot formed from V_1 and V_2 at a 1 mV bias.

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Colophon

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