



Development of superconducting gatemon qubits based on selective-area-grown semiconductors

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Abstract

Currently much experimental effort at universities and companies focuses on the development of large scale quantum computers. Quantum computers are believed to enable solving certain computational problems faster than classical computers, thus revolutionizing many fields in science. Many different technologies are competing to overcome challenges in scaling today's small quantum processors to practically useful fault tolerant quantum computers. Superconducting qubits – in particular transmon-type qubits – are a leading technology in the field and the subgroup of gate-tunable transmons has recently shown strong potential to become a platform for low crosstalk and low dissipation qubit systems.

This thesis presents novel material platforms for scalable voltage-controlled semiconductor-based superconducting transmon qubits (gatemons). These gatemons are based on selective-area-grown InAs/Al hybrid structures which are monolithically integrated into a high resistivity silicon substrate (Si SAG) or InP substrate (InP SAG).

Starting with proof-of-principle demonstrations, the InP SAG material system is introduced and the gatemon fabrication is outlined. Coherent oscillations are demonstrated and coherence times $T_1 \approx 180$ ns and $T_2^* \approx 10$ ns are measured. To improve coherence times, an alternative growth sequence is explored and the electric properties of the material are characterized.

Moving towards gatemons on silicon, the electrical properties of Si SAG at millikelvin temperatures are characterized where we observe a high average field-effect mobility of $\mu \approx 3200$ cm²/Vs for the InAs channel, a hard induced superconducting gap, high transparency Josephson junctions $\mathcal{T} \approx 0.75$ and signatures of multiple Andreev reflections. Josephson junctions exhibit a gate voltage tunable switching current with $I_C R_N \approx 83$ μ V.

Finally, we discuss the RF properties of Si SAG and demonstrate that high quality resonators can be fabricated on the silicon substrate. After detailing the gatemon device fabrication, we describe the measurement of coherent oscillations and coherence times $T_1 \approx 380$ ns and $T_2^* \approx 15$ ns are measured. Possible steps towards increased coherence times are outlined.

In summary, the work presented in this thesis presents a novel and promising material platform for scalable voltage-controlled qubit circuitry.

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List of Publications

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1. **Albert Hertel**, Laurits O. Andersen, David M. T. van Zanten, Michaela Eichinger, Pasquale Scarlino, Sachin Yadav, Karthik Jambunathan, Sergei Gronin, Geoff C. Gardner, Michael J. Manfra, C. M. Marcus, Karl D. Petersson

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2. **Albert Hertel** et al.

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1

Introduction

Currently the world is eagerly awaiting the arrival of the first large scale quantum computer. Inspired by the possibility that quantum computers could revolutionize certain fields in science by solving specific computational problems significantly faster than classical computers [1–4], many research groups and companies are working towards the first quantum computer. The media is closely following the efforts and documenting major breakthroughs in the field, such as the recent demonstration of quantum speed up [5], commenting on how a concept once considered science-fiction slowly becomes reality.

The essential building block of a future quantum computer is the quantum bit (short: qubit), which is built from a quantum two-level system [6]. In contrast to the classical bit, a qubit can be in a superposition of the ground and excited state. A system with N qubits can therefore be prepared in 2^N states, leading to an exponential growth of available states with each additional qubit [7]. Further, quantum states can be entangled, which can be harvested as computation speed up by parallelizing computations [7].

The challenges to building a real quantum computer are manifold. Focusing on the hardware aspect, highly coherent and controllable qubits are required. To readout the qubit states, qubits must inevitably be coupled to the environment and thus to noise sources, causing qubit decoherence. Tremendous progress has been made in the last decade to increase coherence

times, reliably reaching coherence times above ~ 100 ms in superconducting qubits [8,9]. Adding to this challenge, even the simplest quantum algorithms require several qubits [4], meaning qubit-qubit interactions are an essential part of quantum computing. Interconnecting qubits creates parasitic crosstalk between qubits and is a potential source of decoherence. Due to the limited coherence and control of qubits, quantum error detection and correction is assumed to be a necessary ingredient for quantum computers [4,10,11]. Most suggested error corrections schemes, such as the surface code [12], utilize many physical qubits to build one logical qubit. Depending on the assumed error rates, it is estimated that $10^5 - 10^6$ physical qubits will be needed for useful large scale quantum computers [13].

Scaling up to a large number of interconnected qubits sets challenges beyond the device level. Examples are (a) the relatively large footprint of most qubit systems in combination with the limited volume of dilution refrigerators, which are used to cool down many types of qubits to their operation temperature at millikelvin temperatures, and (b) that data acquisition and processing must be performed using classical computers. With these requirements in mind, several qubit platforms have been developed. Some of these are superconducting qubits [9,14,15], electrons confined in quantum dots [16–18] and trapped ions [19,20]. All platforms have their own advantages and disadvantages and compete to be the foundation for future qubit architectures. In parallel, much experimental effort is put into the development of alternative platforms that have the potential to alleviate the challenges of scaling up quantum computers. The work presented in this thesis is part of this experimental effort.

This thesis focuses on the development of a new scalable platform for superconducting qubits using semiconductor-superconductor hybrid systems. These qubits can be classified as gate-voltage controlled transmons, called "gatemons" [21,22]. A transmon uses a Josephson junction to create an anharmonic oscillator [23,24]. In the 'standard' transmon, the Josephson junction is almost exclusively made as an insulating tunnel junction, using aluminium oxide sandwiched between two aluminium electrodes. Transmons are usually controlled using magnetic flux generated at the device level by milliampere currents, which can lead to heating or crosstalk between qubits [22]. Due to the voltage tunability of the junction, the qubit frequency can be voltage controlled, removing the need for large currents and potentially reducing crosstalk. Al-

though a promising new platform, gatemons [25,26] have not reached the high coherence times typically achieved with state-of-the-art transmons [9]. Additionally, current gatemon platforms have either poor scalability [21,27] or poor coherence times due to losses in the underlying III-V substrate [28]. In this work we develop a gatemon platform using selective area growth techniques that has the potential to overcome current limitations and combine scalability and high coherence.

1.1 THESIS OUTLINE

This thesis reports the experimental efforts and progress in creating gatemons using selective-area-grown InAs/Al structures.

Chapter 2 introduces the basics of circuit quantum electrodynamics and discusses the implication of a semiconducting Josephson junction for a superconducting qubit, providing the necessary theoretical framework to understand the experimental data presented in Chapters 5 and 7.

Continuing the discussion about semiconductor-superconductor hybrid systems, Chapter 3 presents the theoretical framework for these systems in term of Andreev reflections. The chapter introduces the BTK theory, the SNS junction, the RCSJ model, the $I_C R_N$ product and OBTK theory, which are necessary to understand the experiments presented in Chapter 6.

Chapter 4 presents our requirements for a platform for scalable and highly coherent gatemons. Further, it details the device fabrication, measurement setups and measurement techniques used in this work.

Chapter 5 introduces the InP SAG material system, outlines gatemon fabrication and presents proof-of-principle measurements showing that selective-area-grown structures can be used to make gatemons. Possible sources of decoherence are discussed and the growth adjusted for it. Material with the adjusted growth is characterized in DC transport, where a sufficiently high field-effect mobility and hard induced superconducting gap is found, leading to the decision to continue with qubit fabrication. These devices showed a gate response but no coherent oscillation, which can be explained by short lifetimes.

Chapter 6 introduces the Si SAG material system and characterizes its DC transport properties in terms of requirements for cQED applications. The measured properties are the field-effect mobility of the InAs channel, the induced

superconducting gap, the Josephson junction transparency and signatures of multiple Andreev reflections. Based on these results, we concluded that the material system is a suitable candidate for scalable gate voltage tunable transmon devices and other superconductor-semiconductor hybrid devices fabricated directly on Si.

Chapter 7 presents the RF properties of Si SAG and demonstrates that high quality (low loss) resonators can be fabricated on the Si substrate. This chapter details the device fabrication and presents coherent oscillations and measurements of the coherence times in these devices. Further, the junction characteristics are probed using the qubit anharmonicity measurements. The chapter concludes with an outline of possible modifications to the device fabrication to improve the device performance.

Chapter 8 summarizes the results of this thesis and gives an outlook on possible future experiments using the Si SAG platform that would benefit and advance the field.

2

Circuit Quantum Electrodynamics

Circuit quantum electrodynamics (circuit QED, or in short cQED) describes the light-matter interaction of a quantum system interacting with microwave photons [15, 24]. In particular, cQED describes superconducting systems as artificial atoms coupled to photons. Based on this successful theoretical framework, superconducting qubits have played a key role in quantum information experiments and the exploration of fundamental laws of quantum mechanics [9, 24]. In this work, only a brief overview of basic concepts of cQED will be given. Understanding cQED is fundamental to superconducting qubits and provides the building blocks for qubits with novel material systems such as the systems presented in this thesis. These concepts are crucial for understanding the measurements presented in Chapters 5 and 7. Section 2.1 introduces the concept of the quantum LC oscillator. Hereafter, the anharmonic quantum oscillator and transmon qubit are described in Sections 2.2 and 2.3. This is followed by the discussion of qubit readout and manipulation in the framework of the Jaynes-Cummings model in Sections 2.4 and 2.5. The final section of this chapter discusses the implication of building a superconducting qubit with a semiconductor-based Josephson junction.

2.1 QUANTIZED LC OSCILLATOR

One of the simplest quantum circuits that can be experimentally realized is the LC oscillator, which consists of an inductor with inductance L , and capacitor, with capacitance C . The corresponding circuit diagram is shown in Fig. 2.1(a). This circuit does not contain any resistors or dissipative elements and is therefore undamped. This is a good approximation to experimental superconducting circuits as the current flow in a superconductor is dissipationless [29]. This can be explained as a consequence of the superconducting gap 2Δ [30] that originates from electrons with opposite spin pairing up to form Cooper pairs [31]. These Cooper pairs condense into a resistance-free ground state, where 2Δ is the energy needed to break a Cooper pair and create single particle excitations. This means that single-particle excitations are effectively suppressed as they require the breaking of a Cooper pair, which is energetically expensive. Collective excitations are lifted to optical frequencies by the long-range Coulomb interaction [24]. Optical frequencies are several orders of magnitude higher than the eigenfrequencies of the LC circuit. Choosing the capacitance charge q as coordinate, the Lagrangian \mathcal{L} of the LC oscillator can be written in terms of a single degree of freedom as follows:

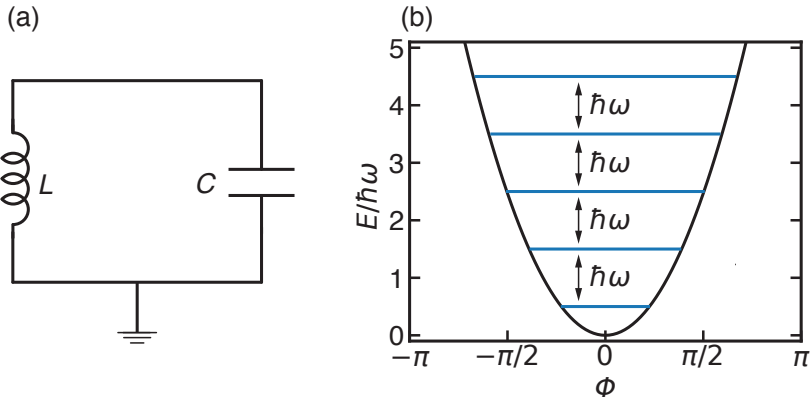


Figure 2.1: Quantum LC oscillator circuit and potential. (a) Circuit diagram of an oscillator with an inductance L and a capacitance C in parallel. (b) Harmonic potential of the quantum LC oscillator with energy levels $E = \hbar\omega(\frac{1}{2} + n)$, where $n \geq 0$.

$$\mathcal{L} = \frac{L}{2} \dot{q}^2 - \frac{q^2}{2C}. \quad (2.1)$$

The time derivative of the charge, $\dot{q} = I$, is the current through the capacitor. The flux through the inductor, Φ , can be expressed as the momentum conjugate to the charge by

$$\frac{\partial \mathcal{L}}{\partial \dot{q}} = L\dot{q} = LI = \Phi. \quad (2.2)$$

Using the equations above, the Hamiltonian can be written as

$$H = \Phi\dot{q} - \mathcal{L} = \frac{\Phi^2}{2L} + \frac{q^2}{2C}. \quad (2.3)$$

This Hamiltonian corresponds to a classical harmonic oscillator with mass L , a spring constant $1/C$ and a resonance frequency $\omega = 1/\sqrt{LC}$. In order to treat the system quantum mechanically the coordinate and conjugate momentum can be promoted to quantum operators \hat{q} and $\hat{\Phi}$. By definition these fulfill the canonical commutation relation

$$[\hat{q}, \hat{\Phi}] = i\hbar. \quad (2.4)$$

This allows us to rewrite the Hamiltonian as

$$\hat{H} = \hbar\omega \left(\hat{a}^\dagger \hat{a} + \frac{1}{2} \right) \quad (2.5)$$

in terms of the raising and lowering operators

$$\hat{a}^\dagger = \frac{1}{\sqrt{2\hbar\omega C}} \hat{q} + i \frac{1}{\sqrt{2\hbar\omega L}} \hat{\Phi} \quad (2.6)$$

$$\hat{a} = \frac{1}{\sqrt{2\hbar\omega C}} \hat{q} - i \frac{1}{\sqrt{2\hbar\omega L}} \hat{\Phi}, \quad (2.7)$$

which obey the commutation relation

$$[\hat{a}, \hat{a}^\dagger] = 1. \quad (2.8)$$

As a consequence of the choice of q as coordinate the energy stored in the

capacitance represents the potential energy. The energy stored in the inductance corresponds to the kinetic energy. The same system could equally well be described using the node flux, Φ , which is defined as the time integral

$$\Phi(t) = \int^t d\tau V(\tau), \quad (2.9)$$

where $V(\tau)$ is the voltage across the two lumped elements in Fig. 2.1(a). While the physical properties of the system are independent of the coordinate choice, describing using Φ as coordinate is more convenient when the inductor is replaced with a non-linear element such as a Josephson junction (see Section 2.2). The consequence of Eq. 2.9 is that $V(t) = \dot{\Phi}$. The energy stored in the inductor can be written as

$$U = \frac{\Phi^2}{2L} \quad (2.10)$$

and takes the form of the potential energy. In contrast to the original coordinate choice this results in the energy stored in the capacitor corresponding to kinetic energy

$$T = \frac{1}{2}C\dot{\Phi}^2, \quad (2.11)$$

resulting in the Lagrangian

$$\mathcal{L} = \frac{1}{2}C\dot{\Phi}^2 - \frac{1}{2L}\Phi^2. \quad (2.12)$$

The momentum conjugate to the flux is given by

$$Q = \frac{\partial \mathcal{L}}{\partial \dot{\Phi}} = C\dot{\Phi}. \quad (2.13)$$

This definition requires that $\hat{Q} = -\hat{q}$ and ensures the canonical commutation relations $[\hat{q}, \hat{\Phi}] = [\hat{\Phi}, \hat{Q}] = +i\hbar$ can be maintained consistently between both coordinate systems discussed in this section. The Hamiltonian can be written in the same form as in Eq. 2.5,

$$\hat{H} = \hbar\omega \left(\hat{a}^\dagger \hat{a} + \frac{1}{2} \right), \quad (2.14)$$

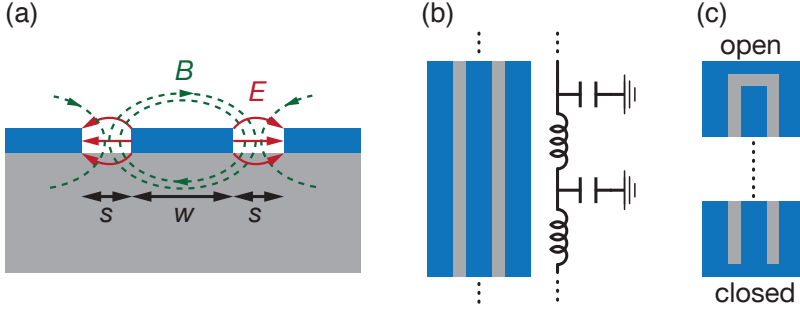


Figure 2.2: Coplanar waveguide geometry (a) Schematic cross section of a coplanar waveguide geometry (CPW). A CPW consists of a conductor (blue) on a substrate (grey) that forms a central conductor with width w and distance to the ground planes s . A schematic representation of the electric and magnetic field distribution of a propagating signal are added. (b) Top view schematic of a CPW structure with the corresponding circuit model. (c) Top view schematic of an open and closed end in the CPW structure. A quarter wave resonator with wavelengths $\lambda_n = 4L'/(2n + 1)$ can be build by connecting both ends with a segment like in (b) with length L' .

but the raising and lowering operators take on the new form

$$\hat{a}^{\dagger} = \frac{1}{\sqrt{2\hbar\omega C}}\hat{\Phi} + i\frac{1}{\sqrt{2\hbar\omega L}}\hat{Q} \quad (2.15)$$

$$\hat{a} = \frac{1}{\sqrt{2\hbar\omega C}}\hat{\Phi} - i\frac{1}{\sqrt{2\hbar\omega L}}\hat{Q}. \quad (2.16)$$

The solutions to the Hamiltonian (Eq. 2.14) are shown in Fig. 2.1(b), where energy levels are evenly spaced and separated by $\hbar\omega$.

The LC oscillator is an important building block cQED measurements, typically used to control and read out the state of a qubit [14,15]. It is most commonly made as a two-dimensional structure in the form of coplanar waveguides (CPW) [32].

Figure 2.2 shows the schematic of a (CPW) geometry, which is also used in this work. A CPW consists of a central conductor with width w that is separated from two ground planes by a gap of width s . The conductor sits on a substrate with permittivity ϵ . It is usually described by its capacitance per unit length $c(k, \epsilon)$, its inductance per unit length $l(k, \epsilon)$, and its impedance $Z(k, \epsilon)$,

where $k = s/(s + 2w)$ [†]. The phase velocity with which a signal propagates through the CPW structure is given by $v_p = 1/\sqrt{\epsilon}c$. Without any boundary conditions, signals with a wide frequency range can propagate through a CPW structure. Extended CPW structures are therefore used as transmission lines. To limit the number of possible modes that can propagate through a CPW, boundary conditions must be introduced. These are usually breaks in the central conductor (open ends with $Z = \infty$) and shorts to the ground plane (closed ends with $Z \rightarrow 0$) as shown in Fig. 2.2(c). No current can flow at the open ends which leads to voltage anti-nodes and current nodes. The opposite configuration is true for closed ends as the voltage relative to ground must be zero. The voltage and current profiles that respect these boundary conditions are the harmonic oscillator modes of the distributed resonator, which is formed. The resonators used in this work are quarter-wave resonators, meaning they have one open and one closed end. The boundary conditions of such a quarter-wave resonator with length L' result in a wavelength $\lambda_n = 4L'/(2n + 1)$, where n denotes the mode number with $n \geq 0$. The corresponding resonance frequencies are $\omega_n = v_p(2n + 1)/(4L')$. In many experiments a resonator can be treated as having a single mode with resonance frequency ω_0 as higher modes are far detuned from any relevant parts of the circuit.

2.2 ANHARMONIC QUANTUM OSCILLATOR

Harmonic LC oscillators play a central role in cQED applications as discussed above but they cannot be used as a qubit while they remain completely harmonic. A qubit needs a non-linear element to enable full control over the computational subspace. If an LC oscillator is in the ground state, energies with $\hbar\omega$ could excite the qubit to the first excited state but also lead to excitations to the second state as $\omega_{01} = \omega_{12}$. This can be avoided by using a non-linear element to change the energy potential from harmonic to (weakly) anharmonic, which has the effect that $\omega_{01} \neq \omega_{12}$. The non-linear element that is used to build superconducting qubits is the Josephson junction [33]. A Josephson junction (JJ) consists of two superconductors that are separated by a weak link and has a non-linear inductance L_J associated to it. In the context of superconducting qubits, JJs most often consist of an insulator that

[†]This is oversimplified since for many applications other important effects such as the kinetic inductance of the superconductor have to be taken into account.

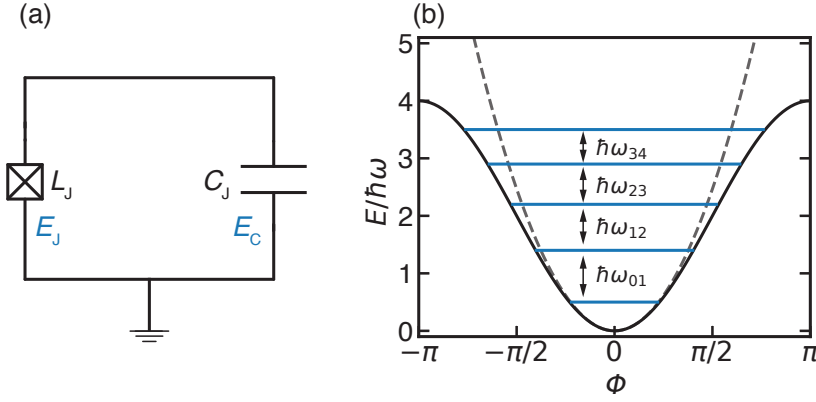


Figure 2.3: Quantum anharmonic oscillator circuit and potential. (a) Circuit diagram of a Josephson Junction (JJ) with Josephson inductance L_J with the associated Josephson energy E_J and capacitance of the Josephson junction C_J with the associated charging energy E_C . (b) Anharmonic potential of the JJ with sinusoidal current phase relation (solid line) and potential of the harmonic oscillator (dashed line). The energy scale is normalized to the harmonic transition energy $\hbar\omega = \hbar/\sqrt{L_J C_J} = \sqrt{8E_J E_C}$. Compared to the harmonic oscillator the spacing between energy levels $|n\rangle$ is not equal and decreases with increasing state index n .

is sandwiched by two superconductors (SIS JJ) [14]. A Josephson junction is described by the two basic Josephson equations

$$I_s = I_c \sin(\phi) \quad (2.17)$$

$$\frac{d\phi}{dt} = \frac{2eV}{\hbar}, \quad (2.18)$$

where I_s is the dissipationless supercurrent across the JJ, ϕ is the superconducting phase difference across the superconducting leads of the JJ, and V is the voltage difference across the JJ. I_c denotes the critical current that is the largest supercurrent that the system can sustain before turning normalconducting. Equations 2.17 and 2.18 are known as DC Josephson effect and AC Josephson effect, respectively [29]. Combining both equations, the time evolution of the

supercurrent can be written as

$$\frac{dI_s}{dt} = \frac{d}{dt} I_c \sin(\phi) = I_c \cos(\phi) \frac{d\phi}{dt} = I_c \cos(\phi) \frac{2eV}{\hbar}. \quad (2.19)$$

This in turn allows us to use the current-voltage relation of an inductor to find an expression for the Josephson inductance

$$L_J = V \left(\frac{dI_s}{dt} \right)^{-1} = \frac{\hbar}{2eI_c \cos(\phi)}. \quad (2.20)$$

Thus, the inductance L_J of this element is non-linear and its use in conjunction with a capacitor results in an anharmonic potential, as required. Figure 2.3(a) shows the circuit diagram for a JJ, with the geometrical (and linear) capacitance C_J of the JJ taken into account. To solve the Hamiltonian, we need an expression for the energy that is associated with the current flow across the JJ. An expression can be obtained by evaluating the time integral over the power,

$$\begin{aligned} E(\phi) &= \int P dt' = \int I_s(\phi) V(\phi) dt' = \int I_c \sin(\phi) \frac{\hbar}{2e} d\phi \\ &= -\frac{\hbar I_c}{2e} \cos(\phi) = -E_J \cos(\phi) \end{aligned} \quad (2.21)$$

where $E_J = \hbar I_c / 2e$ is the characteristic Josephson energy. To compare the quantum LC oscillator and the anharmonic oscillator we have to map the coordinate ϕ to the node flux Φ and promote it to an operator. While Φ is a continuous variable, ϕ is a periodic coordinate in the range $[-\pi, \pi]$. It can be shown that Φ is directly proportional to ϕ and,

$$\hat{\phi} = \frac{\hbar}{2e} \hat{\Phi} = \frac{\Phi_0}{2\pi} \hat{\Phi}, \quad (2.22)$$

where $\Phi_0 = h/2e$ is the superconducting flux quantum [24]. Another aspect that has to be considered is that a JJ will always transfer one Cooper pair across the junction. The energy associated with the transfer of a single electron is given by $E_C = e^2/2C_J$ [24]. The energy needed for the transfer of a Cooper pair is then given by $E = (2e)^2/2C_J = 4E_C$. Using the number operator $\hat{n} = -\hat{q}/2e$ for the number of Cooper pairs on the capacitor, the Hamiltonian for the JJ

can be written as

$$\hat{H}_{\text{JJ}} = 4E_C \hat{n} - E_J \cos(\hat{\phi}). \quad (2.23)$$

The $\cos(\hat{\phi})$ -term leads to the anharmonic potential. To further emphasize the difference from the *LC* oscillator, the Hamiltonian (Eq. 2.5) can be expressed in terms of the operators $\hat{\phi}$, \hat{n} as

$$\hat{H}_{\text{LC}} = 4E_C \hat{n} + \frac{E_L}{2} \hat{\phi}^2, \quad (2.24)$$

where $E_L = (\Phi_0/2\pi)^2/L$ is the inductive energy. This Hamiltonian only contains linear terms. Figure 2.3(b) shows the solutions to the Hamiltonian of the anharmonic oscillator (2.23), where the energy levels are not equally spaced, enabling the isolation of the two lowest energy levels. By utilizing the lowest levels one can already build a qubit system. To implement a useful qubit, we have to include circuit elements for both qubit control and qubit readout into our model, as well as take into account the environment of the qubit.

2.3 TRANSMON

In the following chapter, we will focus on superconducting charge qubits, the *Cooper pair box* (CPB) [34,35] and the *transmon* [23], where the transmon can be viewed as a charge-insensitive version of the CPB and is the qubit design used throughout this work.

To describe the CPB we can start from the Hamiltonian and circuit diagram of a single Josephson junction and increase the complexity. In a CPB a superconducting island is connected to a superconducting reservoir via a Josephson junction. The capacitance between the island and the reservoir is described by C_S . As shown in Fig. 2.4 this can be modeled as a Josephson junction with inductance L_J in parallel with a total capacitance $C_\Sigma = C_J + C_S$. The qubit will be affected by random charges in the environment or a voltage bias might be intentionally applied to the qubit to control it. Both cases can be modeled as a voltage source that is capacitively coupled to the qubit as shown in Fig. 2.4(c). The consequences of this are twofold. First, the charging energy for this system is given by $E_C = e^2/2C'_\Sigma$, where $C'_\Sigma = C_\Sigma + C_G$. Further, the

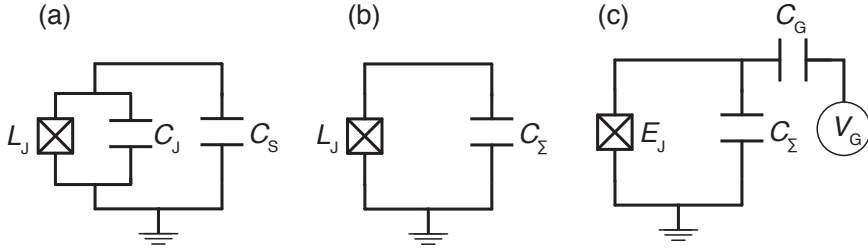


Figure 2.4: Cooper pair box circuit. (a) Circuit diagram of a Josephson junction in parallel with a shunt capacitor C_S . (b) Equivalent circuit to the circuit in (a), where the capacitances are combined to $C_\Sigma = C_J + C_S$. (c) A Josephson junction in parallel with a capacitor and a voltage source coupled capacitively to the circuit via C_G . This circuit diagram corresponds to the Cooper pair box discussed in the main text.

offset charge on the superconducting capacitor,

$$n_g = -\frac{C_G V_G}{2e}, \quad (2.25)$$

has to be considered. It is a continuous variable and represents either the effect of an externally applied electric field or some microscopic junction asymmetry that breaks the degeneracy between positive and negative charge transfer [37]. Taking this into account leads to the CPB Hamiltonian

$$\hat{H} = 4E_C (\hat{n} - n_g)^2 - E_J \cos(\hat{\phi}). \quad (2.26)$$

This Hamiltonian can be solved numerically in the charge basis with $\hat{n} |n\rangle = n |n\rangle$ and $\cos(\hat{\phi}) = 1/2 \sum (|n\rangle \langle n+1| + |n+1\rangle \langle n|)$ [37]. The solutions to the Hamiltonian are plotted in Fig. 2.5 for different ratios of E_J/E_C . These were calculated using a truncated charge space*. In the initial experiments [35, 39] the CPB was operated in the regime $E_J \approx E_C$, where the transition frequency $E_{01}(n_g) = E_1(n_g) - E_0(n_g)$ between the two lowest energy levels has a strong dependence on n_g . The dependency on n_g increases for transitions involving higher levels. As a consequence, CPBs are sensitive to charge noise [35, 39, 40]. To increase coherence times they are typically operated at the sweet spot with

*The code for the numerical solutions can be found in Ref. [38]

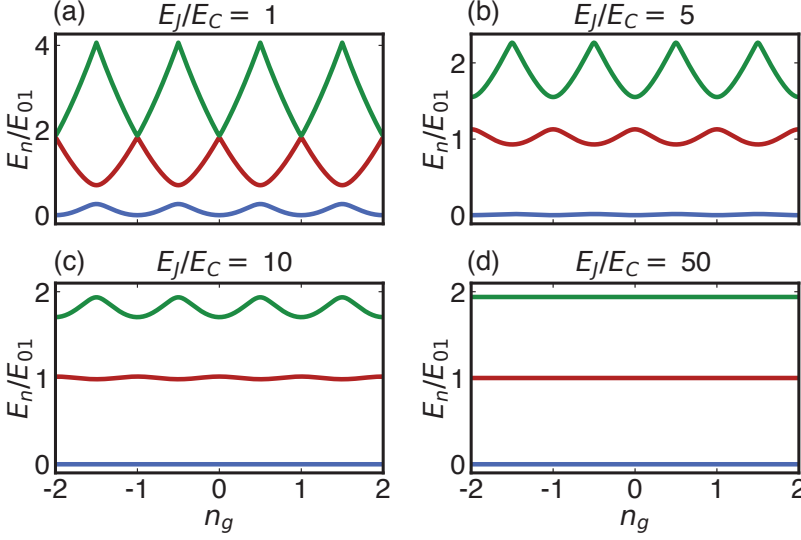


Figure 2.5: Numerical solutions to transmon Hamiltonian (Eq. 2.26) for four different values E_J/E_C showing the three lowest energy levels E_0 (blue), E_1 (red) and E_2 (green) as a function of offset charge n_g . As the ratio E_J/E_C is increased from panels (a) to (d), the charge dispersion, defined as the amplitude of energy deviation as function of n_g , is substantially reduced. This figure is inspired by Ref. [23, 36]. Energies E_n are normalized with respect to $E_{01} = E_1 - E_0$ at $n_g = 0.25$.

$n_g = 1/2$, at which point the system is less sensitive to charge noise as the first order perturbation term $\partial E/\partial n_g$ is zero. Even at the sweet spot, coherence times were limited by charge noise, leading to a shift of experimental efforts in the superconducting qubit community towards charge insensitive qubits such as the transmon [14].

The transmon was first proposed in Ref. [23] and can be described as a Cooper pair box that is operated in the regime $E_J \gg E_C$. In this regime the charge dispersion decreases exponentially while the anharmonicity decreases algebraically. As shown in Fig. 2.5 the energy levels become -almost- independent of the offset charge n_g for large ratios of E_J/E_C . The charge insensitivity can be understood based on the description of the anharmonic oscillator laid out in Section 2.2. In this description the qubit system can be mapped onto a particle with mass m in the anharmonic potential. In this description, $m \propto E_J$

and the kinetic energy corresponds to E_C . Since $E_J \gg E_C$, the particle oscillates around $\phi \approx 0$ and the position of the particle in phase space is localized. Due to the uncertainty principle the kinetic energy of the system, given by the charge, is no longer well defined. As a result external charge fluctuations cannot change the energy of the qubit systems and charge dispersion is reduced. Experimentally this regime is achieved by using a large shunting capacitor $C_S \gg C_J$ (see Fig. 2.4).

The experimental drawback of the transmon compared to the CPB is a reduced anharmonicity $\alpha = (E_{21} - E_{10})$ which increases leakage errors taking the qubit out of the computational subspace [14]. To calculate the anharmonicity we can expand the $\cos(\phi)$ -term of the CPB Hamiltonian around $\phi \approx 0$

$$E_J \cos(\hat{\phi}) = E_J - \frac{E_J}{2} \hat{\phi}^2 + \frac{E_J}{24} \hat{\phi}^4 + O(\hat{\phi}^6). \quad (2.27)$$

This approximation is valid in the regime $E_J \gg E_C$. Further, we can neglect n_g in the transmon regime as the charge dispersion is exponentially suppressed. Omitting constant terms and inserting Eq. 2.27 into Eq. 2.26 leads to the Hamiltonian

$$\begin{aligned} \hat{H} &= 4E_C \hat{n} - E_J \cos(\hat{\phi}) \\ &\approx 4E_C \hat{n} + \frac{E_J}{2} \hat{\phi}^2 - \frac{E_J}{24} \hat{\phi}^4 = \hat{H}_0 + V'(\hat{\phi}), \end{aligned} \quad (2.28)$$

where $\hat{H}_0 = 4E_C \hat{n} + \frac{E_J}{2} \hat{\phi}^2$ takes the form of the Hamiltonian of the harmonic oscillator. The corresponding plasma frequency is given by $\hbar\omega_r = 1/\sqrt{L_J C_\Sigma} = \sqrt{8E_J E_C}$, where C_Σ is the sum of all capacitances in the system [see Fig. 2.6(c)]. The term $V'(\hat{\phi}) = E_J \hat{\phi}^4/24$ can be treated as perturbation to \hat{H}_0 , which enables us to calculate the anharmonicity. In order to do so we can express the operators \hat{n} and $\hat{\phi}$ in terms of ladder operators of the Harmonic oscillator (see Section 2.1).

$$\hat{a}^\dagger = \sqrt{\frac{E_J}{2\hbar\omega}} \hat{\phi} + 2i\sqrt{\frac{E_C}{\hbar\omega}} \quad (2.29)$$

$$\hat{a} = \sqrt{\frac{E_J}{2\hbar\omega}} \hat{\phi} - 2i\sqrt{\frac{E_C}{\hbar\omega}}. \quad (2.30)$$

This, in turn, enables us to express $\hat{\phi}$ and \hat{n} in terms of ladder operators and relevant energy scales as

$$\hat{\phi} = \left(\frac{2E_C}{E_J} \right)^{1/4} (\hat{a} + \hat{a}^\dagger) \quad (2.31)$$

$$\hat{n} = \left(\frac{E_J}{2E_C} \right)^{1/4} (\hat{a} - \hat{a}^\dagger). \quad (2.32)$$

Inserting this back into the Eq. 2.28 yields

$$\hat{H}_0 = \hbar\omega \left(\hat{a}^\dagger \hat{a} + \frac{1}{2} \right) \quad (2.33)$$

$$V'(\hat{\phi}) = -\frac{E_J}{12} \left(\hat{a} + \hat{a}^\dagger \right)^4. \quad (2.34)$$

Applying the rotating wave approximation, by neglecting all terms with an uneven number of raising and lowering operators, the perturbation can be written as

$$V'(\hat{\phi}) = -\frac{E_J}{12} \left(\hat{a} + \hat{a}^\dagger \right)^4 = -\frac{E_C}{2} \left(\hat{a}^\dagger \hat{a}^\dagger \hat{a} \hat{a} + 2\hat{a}^\dagger \hat{a} \right). \quad (2.35)$$

This leads to corrections for the first three energy levels relative to the harmonic oscillator solutions

$$\langle 0 | V'(\hat{\phi}) | 0 \rangle = 0 \quad (2.36)$$

$$\langle 1 | V'(\hat{\phi}) | 1 \rangle = -E_C \quad (2.37)$$

$$\langle 2 | V'(\hat{\phi}) | 2 \rangle = -3E_C, \quad (2.38)$$

leading to the transition energies

$$E_{10} \approx E_1 - E_0 = \sqrt{8E_J E_C} - E_C \quad (2.39)$$

$$E_{21} \approx E_2 - E_1 = \sqrt{8E_J E_C} - 2E_C, \quad (2.40)$$

and an anharmonicity

$$\alpha = E_{21} - E_{10} \approx -E_C. \quad (2.41)$$

2.4 QUBIT READOUT

In the previous sections we described the transmon qubit and introduced an element of control in the form of an external voltage which can be used to set the offset charge. However, any useful quantum algorithm requires a way to manipulate and effectively read out the qubit state. Additionally, many proposed quantum algorithms rely on active error correction, requiring quantum non-demolition measurements that preserve the qubit state [24]. As we will discuss in this section, both qubit manipulation and qubit readout can be performed via an LC oscillator that is coupled to the qubit.

Figure 2.6 shows the circuit diagram of a circuit that is typically used to measure a voltage-controlled transmon qubit. Here, the transition frequency ω_{01} - henceforth only referred to as qubit frequency ω_q - can be controlled by changing E_J via the gate voltage V_G . The qubit is coupled to a distributed LC resonator with a total capacitance C_r , total inductance L_r , and resonance frequency $\omega_r = (2\pi)/\sqrt{L_r C_r}$ (see Fig. 2.6). The resonance frequency is chosen such that only the lowest mode of the resonator is close to the qubit frequency. Higher resonator modes can be neglected. The resonator is coupled inductively to a transmission line. The system can be described by the Hamiltonian

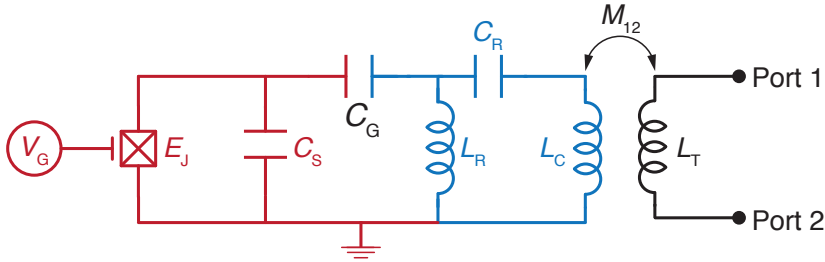


Figure 2.6: Coupled transmon circuit. Circuit diagram representing a voltage-tunable transmon (red) that is capacitively coupled to a readout resonator with inductance L_R and capacitance C_R (blue). The qubit and resonator are coupled by capacitance C_G . The readout resonator with coupling inductance L_C is inductively coupled to a transmission line with inductance L_T (black) by the mutual inductance M_{12} . The qubit frequency can be controlled via a gate voltage V_G that is applied to the Josephson junction to modulate E_J .

$$\hat{H} = 4E_C \hat{n} - E_J \cos(\hat{\phi}) + \hbar \omega_r \hat{a}^\dagger \hat{a} + 2\beta e V_{\text{rms}}^0 \hat{n} (\hat{a} + \hat{a}^\dagger), \quad (2.42)$$

where $\beta = C_G/C_\Sigma$ and $V_{\text{rms}}^0 = \sqrt{\hbar \omega_r / (2C_r)}$ is the root mean square voltage of the resonator at the point where it couples to the shunting capacitor [23]. Here, the first two terms correspond to the uncoupled CPB Hamiltonian (Eq. 2.28). The third term represent the lowest mode of the resonator. The fourth term describes the resonator-qubit coupling. Rewriting the Hamiltonian in the basis of the uncoupled transmon states $|i\rangle$, one obtains the generalized Jaynes-Cummings Hamiltonian

$$\hat{H} = \hbar \omega_r \hat{a}^\dagger \hat{a} + \hbar \sum_i \omega_i |i\rangle \langle i| + \hbar \sum_{i,j} g_{ij} |i\rangle \langle j| (\hat{a} + \hat{a}^\dagger), \quad (2.43)$$

where the coupling strength g_{ij} between is levels i and j are given by the expression

$$\hbar g_{ij} = 2\beta e V_{\text{rms}}^0 \langle i | \hat{n} | j \rangle. \quad (2.44)$$

Equation 2.43 can be significantly simplified when analyzing the matrix elements and using the rotating wave approximation. The only matrix element with a significant contribution is the element $\langle i+1 | \hat{n} | i \rangle$ as all other matrix elements asymptotically approach zero in the transmon limit $E_J/E_C \rightarrow 0$. Employing the rotating wave approximation, terms that do not conserve the number of excitations in the system can be eliminated. This leads to the effective generalized Jaynes-Cummings Hamiltonian

$$\hat{H} = \hbar \omega_r \hat{a}^\dagger \hat{a} + \hbar \sum_i \omega_i |i\rangle \langle i| + \hbar \sum_i g_{i,i+1} (|i\rangle \langle i+1| \hat{a}^\dagger + |i+1\rangle \langle i| \hat{a}). \quad (2.45)$$

Simplifying further, the qubit system can be approximated as an effective two-level system. Rewriting the Hamiltonian in terms of the qubit frequency ω_q , the spin Pauli operators $\hat{\sigma}_z$ and the spin ladder operators $\hat{\sigma}_\pm = \hat{\sigma}_x \pm i\hat{\sigma}_y$, leads to the original Jaynes-Cummings Hamiltonian [41, 42]

$$\hat{H} = \hbar \omega_r \hat{a}^\dagger \hat{a} + \frac{\hbar \omega_q}{2} \hat{\sigma}_z + \hbar g_{01} (\hat{a}^\dagger \hat{\sigma}_- + \hat{\sigma}_+ \hat{a}). \quad (2.46)$$

The Jaynes-Cummings Hamiltonian has two distinct regimes. In the resonant regime, $\omega_r \approx \omega_q$ the qubit and resonator hybridize into new states that are

superpositions of the qubit excitation states and the resonator photon states. These new states are split by the vacuum Rabi splitting $2\hbar g_{01}$. In order to achieve quantum non-demolition (QND), the qubit is operated in the dispersive regime that allows for quantum non-demolition measurements [42]. In this dispersive limit the detuning between qubit and resonator Δ_0 is large compared to the coupling ($|\Delta_0| = |\omega_r - \omega_q| \gg g$). Expanding around g/Δ_0 and restricting the Hilbert space to the lowest two levels leads to the effective Hamiltonian

$$\hat{H}_{\text{eff}} = \frac{\hbar\omega'_q}{2}\hat{\sigma}_z + \hbar(\omega'_r + \chi\hat{\sigma}_z), \quad (2.47)$$

where $\omega'_q = \omega_q + \chi$ and $\omega'_r = \omega_r - \chi_{12}/2$ are the renormalized qubit and resonator frequencies, respectively [23]. The harmonic frequency shifts are defined as

$$\chi_{ij} = \frac{g_{ij}^2}{\omega_q - \omega_r} \quad (2.48)$$

$$\chi = \chi_{01} - \frac{\chi_{12}}{2}. \quad (2.49)$$

The key feature in this regime is that the resonator frequency shifts by $\pm\chi$ depending on the qubit state, meaning the qubit state can be inferred from a resonator measurement. The other crucial aspect here is that the qubit remains in the measured state after readout. Therefore a resonator measurement constitutes a quantum non-demolition measurement of the qubit. Using $\omega_{12} = \omega_{01} + \alpha/\hbar$ and $g_{12} = \sqrt{2}g_{01}$, the frequency shift can be written as

$$\chi = \chi_{01} - \frac{\chi_{12}}{2} = \frac{g_{01}^2}{\Delta_0} - \frac{g_{01}^2}{\Delta_0 + \alpha/\hbar}. \quad (2.50)$$

As highlighted by Eq. 2.50 a sufficiently large anharmonicity is needed for a resonator shift that is large enough to be detected. Ideally, a large coupling strength g_{01} would be chosen in most experiments if it would not cause adverse effects. For instance, the spontaneous decay rate of the qubit is modified by the decay rate of the resonator κ , which is known as the Purcell effect [43,44].

The Purcell decay rate is given by

$$\gamma_\kappa = \kappa \frac{g_{01}^2}{\Delta_0^2}. \quad (2.51)$$

Without the aid of measures such as the use of a Purcell filter to mitigate losses [45], we choose a trade off that enables a large enough resonator shift while keeping the Purcell decay rate below the qubit state decay rate.

2.5 QUBIT MANIPULATION

In the previous section we described the qubit as a quantum mechanical two-level system. In order to realize the potential of such a system for quantum computation it is fundamentally important to be able to control it, starting from the ability to prepare a qubit in any linear combination of the ground state $|0\rangle$ and the first excited state $|1\rangle$. As illustrated in Fig. 2.7, any state can be visualized as a vector on the Bloch sphere $|\Psi\rangle = \cos(\theta/2)|0\rangle + e^{i\phi}\sin(\theta/2)|1\rangle$.

Any single qubit operation can be visualized as a series of rotations of the qubit state around the x and y axes. In our experiment these rotations are generated by microwave tones that are coupled to the qubit, either through a drive line or the readout resonator. The Hamiltonian in Eq. 2.47 can be expanded to account for an external time-dependent drive of the kind $V_d(t) = v_R \cos(\omega_d t) + v_I \sin(\omega_d t)$, where v_R and v_I denote the in-phase and out-of-phase part of the drive signal, respectively, and ω_d is the drive frequency. In the rotating frame of the drive the Hamiltonian can be written as

$$\hat{H} = \hbar(\Delta_r + \chi \hat{\sigma}_z) \hat{a}^\dagger \hat{a} + \frac{\hbar \Delta_q \hat{\sigma}_z}{2} + \frac{\hbar}{2} (\Omega_R(t) \hat{\sigma}_x + \Omega_I(t) \hat{\sigma}_y), \quad (2.52)$$

where $\Delta_r = \omega_r - \omega_d$, $\Delta_q = \omega_{01} - \omega_d$ and $\Omega_{R,I} = 2e\beta \langle 0 | \hat{n} | 1 \rangle v_{R,I}$. In this description $\Omega_{R,I}$ are Rabi frequencies, the frequencies of the driven system with which the state rotates around the x -axis (with frequency Ω_R) and y -axis (with frequency Ω_I). Equation 2.52 describes a superconducting transmon, which is coupled to a readout resonator and can be manipulated with an external drive, enabling full qubit control and readout. This Hamiltonian describes the qubit devices that are the focus of this work and discussed in Chapters 5 and 7. The experimental implementation of Eq. 2.52 will be

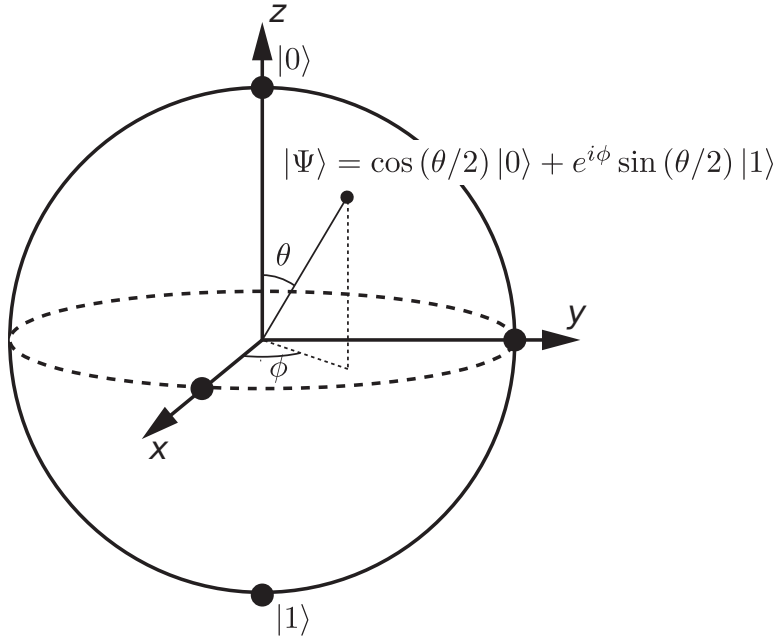


Figure 2.7: Bloch sphere representation of a qubit state $|\Psi\rangle$ as a unit vector anywhere on the surface of the sphere. The state $|\Psi\rangle$ can be described using the angles θ and ϕ .

discussed in Section 4.7.

2.6 SEMICONDUCTOR-BASED SUPERCONDUCTING QUBITS

In the previous sections we assumed two properties of the Josephson junction (JJ). Firstly, that the critical current and therefore E_J is tunable with an external voltage and secondly, that the current-phase relationship (CPR) of the junction is sinusoidal (Eq. 2.17). However, most state-of-the-art transmons are not gate-tunable. The JJs in these transmons are commonly realized by a material stack that is made out of $\text{Al}/\text{Al}_2\text{O}_3/\text{Al}$, where the insulating Al_2O_3 layer is only a few nanometers thick [14]. Two junctions are built in parallel to form a superconducting quantum interference device (SQUID [46]. The critical current I_C (hence E_J) of the SQUID is controlled via an magnetic flux that is

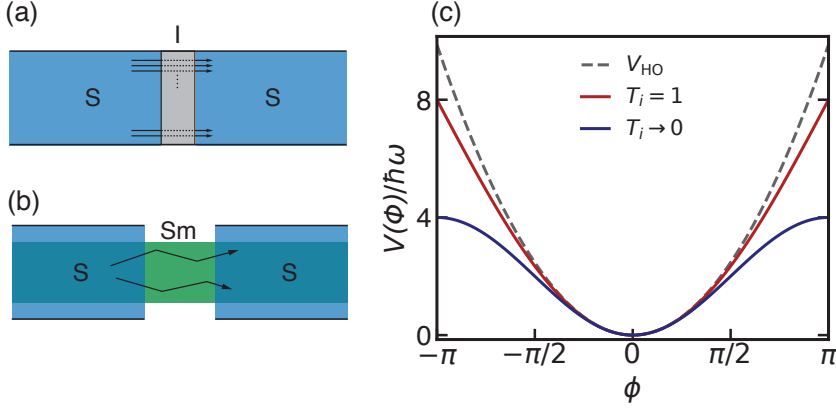


Figure 2.8: Short junction potential. Comparison of an (a) SIS and (b) SSmS Josephson junction. The SIS junction has many low transmitting channels while the SSmS junction has few highly transmitting channels. (c) Short junction Josephson potential $V(\phi)$ (Eq. 2.53) in the limits $T_i \rightarrow 0$ (blue) and $T_i = 1$ (red). For comparison the potential of the harmonic oscillator V_{HO} is plotted as a dashed line. The potentials are normalized to the harmonic resonance frequency ω and offset to all equal 0 at $\phi = 0$.

threaded through the SQUID loop.

Gate-tunable junctions and qubits have been realized with superconductor-semiconductor-superconductor (SSmS) junctions [21, 22], where I_C can be tuned by tuning the semiconductor segment of the junction. The CPR of a SSmS junction is not sinusoidal[†].

Figures 2.8(a) and (b) show a schematic representation of an SIS and SSmS junction. In the case of an SIS junction, the junction has many low-transmitting channels and the current-phase relationship is well described by Eq. 2.17. In contrast, SSmS junctions have a few highly transmitting channels [47]. The charge is transferred via so-called Andreev bound states that will be discussed in more detail in Section 3.3. In the ballistic limit where the superconducting coherence length is much larger than the junction length, the Andreev bound

[†]A sinusoidal CPR can be retrieved in the tunnel limit where the semiconductor is effectively depleted but otherwise not present (see Eq. 2.57).

states lead to a Josephson potential of the form

$$V(\hat{\phi}) = -\Delta \sum_i \sqrt{1 - T_i \sin^2(\hat{\phi}/2)}, \quad (2.53)$$

where Δ is the superconducting gap and T_i is the transmission probability of the i_{th} channel [48]. In the case $T_i \rightarrow 0$ the potential $V(\hat{\phi})$ approaches a $\cos(\phi)$ -potential. This is the potential used previously to describe the anharmonic oscillator in Section 2.2. It is illustrated in Fig. 2.3(b) and described by Eq. 2.21. For $T_i = 1$ the potential is still weakly anharmonic but more closely resembles the potential of a harmonic oscillator [see Fig. 2.1(b)]. A comparison of all three potentials is shown in Figure 2.8(c). As a consequence the anharmonicity depends on the transmission of the single channels. To calculate the anharmonicity we can follow the procedure described in Section 2.3 and expand $V(\hat{\phi})$ to the fourth order in $\hat{\phi}$. A more detailed derivation can be found in Ref. [36]. For $E_J \gg E_C$ and $\phi \approx 0$ the potential can be written as

$$V(\hat{\phi}) = E'_J \frac{\hat{\phi}^2}{2} - E'_J \left(1 - \frac{3 \sum T_i^2}{4 \sum T_i} \right) \frac{\hat{\phi}^4}{24} + \mathcal{O}(\hat{\phi}^6) \quad (2.54)$$

$$\text{with } E'_J = \frac{\Delta}{4} \sum T_i. \quad (2.55)$$

With the definition of E'_J the harmonic part of the potential can be written as $V_0(\hat{\phi}) = \frac{E'_J}{2} \hat{\phi}^2$. Treating the rest of the potential as perturbation

$$V'_0(\hat{\phi}) = -E'_J \left(1 - \frac{3 \sum T_i^2}{4 \sum T_i} \right) \frac{\hat{\phi}^4}{24} \quad (2.56)$$

and applying the rotating wave approximation, the transmission dependent anharmonicity can be expressed as

$$E_{12} - E_{01} = \alpha \approx -E_C \left(1 - \frac{3 \sum T_i^2}{4 \sum T_i} \right) \quad (2.57)$$

as shown in Ref. [36]. This result demonstrates that the anharmonicity can be

reduced to $\alpha = -E_C/4$ in the limit of $T = 1$. In the tunnel limit $T_i \rightarrow 0$ the result $\alpha = -E_C$ of a transmon with an SIS junction is recovered.

In this chapter we discussed the LC oscillator, the SIS Josephson junction, and the transmon in the framework of cQED. Additionally, we described the coupled system of a transmon and an LC oscillator for qubit manipulation and readout. This formulation is the basis of quantum computing with superconducting qubits and necessary to understand the qubit characterization in Chapter 5 and 7. Further, we have discussed the difference between the standard insulator-based transmon and the gate-voltage tunable semiconductor-based transmon, often referred to as a gatemon [21,22]. Here, the qubit system was described using macroscopic degrees of freedom, such as inductance, capacitance and critical current. In Chapter 3 we will give a microscopic description of the processes that appear at the interface between semiconductor and semiconductor, namely Andreev reflections, and the Josephson effect in terms of Andreev bound states.

3

Superconductor-Semiconductor Hybrid Systems

In the previous chapter, we have described superconductor-semiconductor-superconductor Josephson junction as a building block for a transmon in the framework of cQED. In this chapter, we will focus on the microscopic description of the electric properties of superconductor-semiconductor hybrid systems in terms of Andreev reflections. These are introduced in Section 3.1. Section 3.2 gives a brief summary of the Blonder-Tinkham-Klapwijk (BTK) formalism for the charge transport across an NS interface and the proximity effect. This is followed by the description of an SNS junction in terms of Andreev reflections and within the resistively shunted junction model in Sections 3.3 and 3.4, respectively. Section 3.5 discusses the $I_C R_N$ product for different junction limits. Lastly, Section 6.6 presents the concept of multiple Andreev reflections. These concepts are necessary to understand the measurements presented in Chapter 6.

3.1 ANDREEV REFLECTIONS

To understand the properties of a semiconductor in the proximity of a superconductor, it is crucial to understand the processes at the material interface.

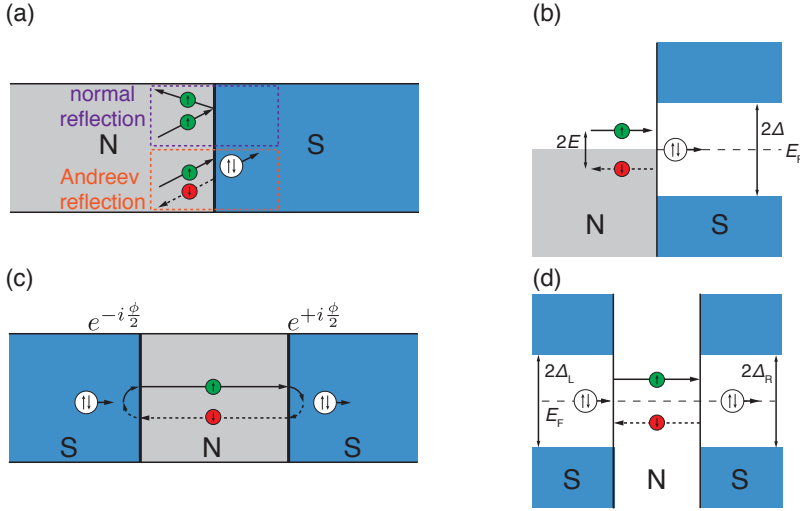


Figure 3.1: Andreev reflections in real and energy space. (a) Real space schematic of a normal reflection and Andreev reflections at an NS interface. In this example an electron (green) with spin up (\uparrow) is Andreev reflected, meaning being retroreflected as a hole (red) with spin down (\downarrow) and retracing the trajectory of the incident electron. As result a Cooper pair in the superconductor is created. (b) Energy schematic of Andreev reflections. (c) Real space schematic representation of an Andreev bound state in an SNS junction with phase difference ϕ between the superconducting regions. (d) Energy space representation of an Andreev bound state in an SNS junction.

When the semiconductor, which is modeled as a normal conductor, and superconductor are in contact, the Fermi energies E_F of both materials are aligned. While electron states in the normal conductor (N) with energies $E \leq E_F$ are occupied, no single particle states with $E_F - \Delta < E < E_F + \Delta$ exist in the superconductor (S), where Δ is the superconducting gap.

Figure 3.1(a) shows the two ways an electron can reflect at an NS interface for $E < \Delta$. First, it could normal reflect, where the electron is reflected back into the normal conductor. As we will see in Section 3.2.1, normal reflections only occur if the interface is imperfect or the incident electron has an energy $E > \Delta$. In case of a perfect interface and $E < \Delta$, *Andreev reflections* will occur [49], meaning the incident electron with momentum \vec{k} and spin up (\uparrow) propagates into the superconductor and the normal conductor donates an

additional electron with $\vec{k} \downarrow$ and energy $-E$. As a results. the superconductor accepts a Cooper pair ($\vec{k} \uparrow, -\vec{k} \downarrow$) with energy E_F . This process can equally well be represented as the incident electron being retroreflected as a hole with momentum $-\vec{k}$ [see Figs. 3.1(a)-(b)].

The qualitative description above can be generalized for imperfect interfaces to describe electrical transport across an NS interface quantitatively. Interfaces will always be degraded due to sample processing or imperfect materials. Further, the Fermi velocity mismatch between semiconductor and superconductor is taken into account.

3.2 TRANSPORT ACROSS NS INTERFACE

3.2.1 THE BLONDER-TINKHAM-KLAPWIJK FORMALISM

The Blonder-Tinkham-Klapwijk formalism describes the electrical transport across an imperfect NS interface [50]. The system is modeled with the potential shown in Fig. 3.2(a), where the interface between semiconductor and superconductor is described with the potential $H\delta(r)$, where $\delta(r)$ is the Dirac delta function. Instead of H , the dimensionless unit

$$Z = H \frac{m_e}{\hbar v_F}, \quad (3.1)$$

is typically used to describe the interface, where v_F denotes the Fermi velocity and m_e is the electron mass. This Z -parameter is often used synonymously with the interface quality, where $Z = 0$ correspond to a perfect interface with-

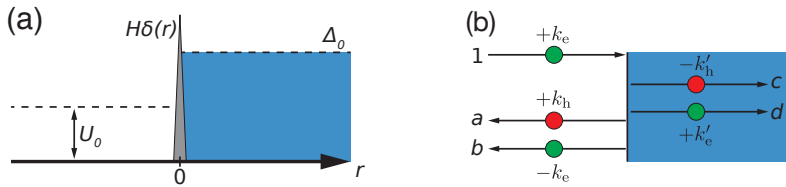


Figure 3.2: Schematic NS interface in the BTK model. (a) The potential between normal conductor (white) and superconductor (blue) is modeled using the conduction band offset U_0 , the pairing potential Δ_0 , and a Dirac δ -function with height H at the interface. (b) Definition of the plane-wave coefficients used in the BTK analysis.

out barrier. Additionally, different charge carrier densities in both materials lead to a difference in E_F , which lifts the conduction band of the semiconductor relative to the superconductor by U_0 . The Fermi velocity mismatch is modeled by a potential step across the interface, leading to the potential

$$U(r) = U_0\theta(-r) + H\delta(r), \quad (3.2)$$

where $\theta(r)$ is the Heaviside step function. Further, the pair potential increases in a step-like manner $\Delta(r) = \Delta_0 e^{-i\phi} \theta(r)$ as shown in Fig. 3.2(a). In order to calculate the particle transfer across the interface, the Bogoliubov-de Gennes equations are utilized [29]. The corresponding Hamiltonian is

$$H(r) = \frac{\hbar^2}{2m^*} \nabla_r^2 - \mu + U(r), \quad (3.3)$$

where m^* corresponds to the effective mass of the electrons in the semiconductor and μ denotes the chemical potential. Fig. 3.2(b) illustrates the possible outcomes of a scattering event at the interface. An incident electron at the interface can be scattered in four different ways: as a reflected electron (normal scattering), as a retroreflected hole (Andreev reflection), be transmitted as a quasi-electron or be transmitted as a quasi-hole. Using the plane-wave ansatz this can be expressed by three wave functions

$$\Psi_{\text{incoming}} = \begin{pmatrix} 1 \\ 0 \end{pmatrix} e^{ik_e r} \quad (3.4)$$

$$\Psi_{\text{reflected}} = a \begin{pmatrix} 0 \\ 1 \end{pmatrix} e^{ik_h r} + b \begin{pmatrix} 1 \\ 0 \end{pmatrix} e^{-ik_e r} \quad (3.5)$$

$$\Psi_{\text{transmitted}} = c \begin{pmatrix} u \\ v \end{pmatrix} e^{ik'_e r} + d \begin{pmatrix} u \\ v \end{pmatrix} e^{-ik'_h r}. \quad (3.6)$$

The wavenumbers can be found considering the eigenenergies of the Bogoliubov-de Gennes equations

$$\begin{aligned}
 k_e &= \sqrt{k_{F,N}^2 + \frac{2m^*}{\hbar^2} E} \\
 k_e &= \sqrt{k_{F,N}^2 - \frac{2m^*}{\hbar^2} E} \\
 k_e &= \sqrt{k_{F,S}^2 + \frac{2m^*}{\hbar^2} \sqrt{E^2 - \Delta_0^2}} \\
 k_e &= \sqrt{k_{F,S}^2 - \frac{2m^*}{\hbar^2} \sqrt{E^2 - \Delta_0^2}},
 \end{aligned} \tag{3.7}$$

where $k_{F,N}$ and $k_{F,S}$ are the Fermi wave vectors of the normal and superconductor, respectively. These equations can be solved by evaluating the boundary condition at $r = 0$ to find an expression for the probability of Andreev reflections $A(E) = |a|^2$, the probability of normal reflections $B(E) = |b|^2$ and the probability for transmission $T(E) = 1 - A(E) - B(E)$ [50]. These probabilities are summarized in Table 3.1 and plotted in Fig. 3.3(a)-(c). The factors in Table

		$A(E)$	$B(E)$
$Z = 0$	$E < \Delta$	1	0
	$E > \Delta$	$\frac{v_0^2}{u_0^2}$	0
$Z > 0$	$E < \Delta$	$\frac{\Delta^2}{E^2 + (\Delta^2 - E^2)(1 + 2Z_{\text{eff}}^2)^2}$	$1 - A(E)$
	$E > \Delta$	$\frac{u_0^2 v_0^2}{u_0^2 + (u_0^2 - v_0^2)Z_{\text{eff}}^2}$	$\frac{(u_0^2 - v_0^2)^2(1 + Z_{\text{eff}}^2)Z_{\text{eff}}^2}{u_0^2 + (u_0^2 - v_0^2)Z_{\text{eff}}^2}$

Table 3.1: Probability of Andreev reflection $A(E)$ and normal reflections $B(E)$ for $Z = 0$ and $Z > 0$ in the regimes $E > \Delta$ and $E < \Delta$. The transmission probability is not explicitly listed here but is given by $T(E) = 1 - A(E) - B(E)$.

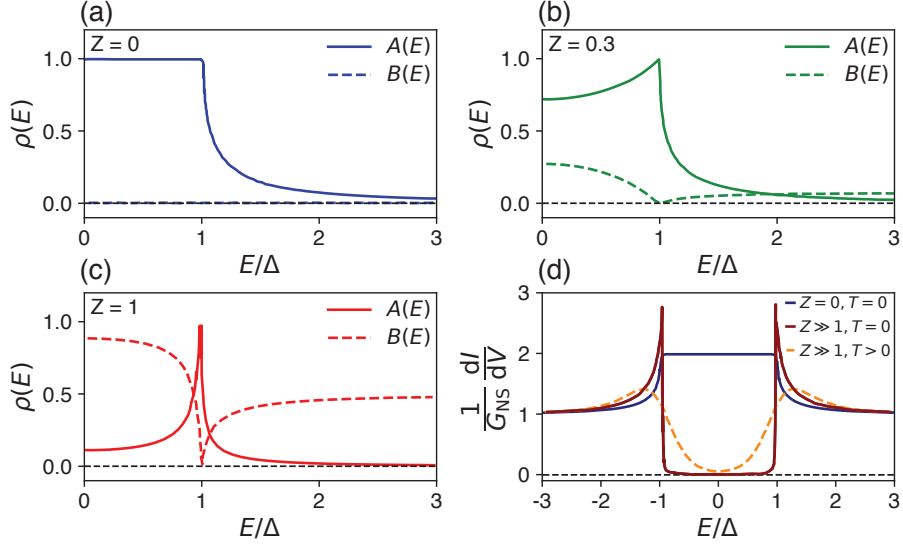


Figure 3.3: BTK model solutions. (a)-(c) Probabilities for Andreev reflections (AR) and normal reflections (NR) as function of the normalized energy E/Δ for different values of Z at temperature $T = 0$. (d) Differential conductance across an NS interface normalized by the normal state resistance $G_{NS} = dI/dV|_{eV \gg \Delta}$ for different limits of Z and T .

3.1 are defined as

$$u_0 = \frac{1}{2} \left(1 + \frac{\sqrt{E^2 - \Delta^2}}{E} \right) \quad (3.8)$$

$$v_0^2 = 1 - u_0^2. \quad (3.9)$$

The Fermi velocity mismatch $r_F = v_{F,N}/v_{F,S}$ is taken into account by replacing the Z -parameter with

$$Z_{\text{eff}} = \sqrt{Z^2 + \frac{(1 - r_F)^2}{4r_F}}. \quad (3.10)$$

For the remainder of this thesis, Z_{eff} will be referred to as Z -parameter. *

Figure 3.3(a) shows the solution for a perfect interface with $Z = 0$. In the

*This usage is consistent with existing literature (e.g. the original BTK-paper [50] and Ref. [51]).

case $E < \Delta$ only Andreev reflections occur. Andreev reflections also occur for energies $E > \Delta$, i.e. change the normal state transmission across the interface. Andreev reflections occur for energies $E > \Delta$ for $Z \lesssim 1$ and are suppressed for increasing Z . Figure 3.3(b) and (e) show the solution for $Z = 0.3$ and $Z = 1$, respectively. As exemplified here $B(E)$ increases monotonically with Z for any given value of E . For large values of $Z \gg 1$, Andreev reflections only contribute to transport for $E \approx \Delta$.

The probabilities of Andreev reflections at an NS interface can be measured using tunneling spectroscopy. When a voltage V is applied across the NS interface the corresponding current is given by

$$I = \frac{G_0}{e} \int_0^\infty dE [f(E) - f(E - eV)] [1 + A(E) - B(E)], \quad (3.11)$$

where $f(E)$ denotes the Fermi distribution and $G_0 = 2e^2/h$. The second bracket represents the probability to transmit an electron across the interface. This equation can be simplified in the limit $T = 0$ to calculate an experimentally accessible key result of the BTK formalism. For $T = 0$ the Fermi distributions can be approximated by a step function. The differential conductance G is given by the voltage derivative of the current

$$\begin{aligned} G|_{T=0} &= \frac{dI}{dV} = G_0 \int_0^\infty \delta(E - eV) [1 + A(E) - B(E)] dE \\ &= G_0 [1 + A(E) - B(E)]. \end{aligned} \quad (3.12)$$

Figure 3.3(f) shows the differential conductance based on Eq. 3.11 and Eq. 3.12. In the limit $eV \gg \Delta$ Eq. 3.12 reduces to the normal state resistance $G_{NS} = G_0/(1 + Z^2)$. For $eV < \Delta$ the subgap conductance is twice the normal state resistance as Andreev processes transfer a charge $2e$ across the interface. In the limit $Z \gg 1$ Eq. 3.12 can further be simplified to

$$G(E) = G_{NS} \frac{E}{\sqrt{E^2 - \Delta^2}} = \frac{G_{NS}}{D_N} D_S(E), \quad (3.13)$$

where D_N is the normal state density of state [29]. Here, we used $D_S = D_N \cdot E/\sqrt{E^2 - \Delta^2}$ to relate the superconducting density of states D_S to D_N . As illustrated by Eq. 3.13, G can be used to probe D_S as $G(E) \propto D_S(E)$.

3.2.2 PROXIMITY EFFECT

The step-like potential shown in Fig. 3.2(a) is an oversimplification. As demonstrated in experiments, the properties of a superconductor extend into the N-region, known as the *proximity effect* [52]. An example of this is an induced superconducting gap in a semiconductor in semiconductor-superconductor hybrid systems, as discussed in Chapter 6. This effect can be understood by considering pairing between electrons and retroreflected holes near the NS interface. The electron and hole only follow the exact same path if the incident electron has an energy $E = 0$. For energies $|E| > 0$, the respective paths deviate from each other, meaning the particles acquire a phase difference $\Delta\phi$ and a difference in momentum $\delta k = k_e - k_h = E/(\hbar v_F)$. The pair of particles becomes out of phase after the particles have traveled the distance $L = \Delta\phi/\delta k = \pi/\delta k$ [53]. The largest electron energy that will lead to Andreev reflection is $E = \Delta$, giving a coherence length

$$\xi_N = \frac{\hbar v_F}{\pi \Delta}, \quad (3.14)$$

which is the same results as the BCS coherence length, except v_F corresponds to the Fermi velocity inside the N-region.

3.3 SNS JUNCTION

A semiconductor Josephson junction as previously introduced in Section 2.6), can be described as an SNS junction in the framework of Andreev reflections, where the semiconductor junction is modeled as a thin N-region that is confined by two S-regions. Andreev reflections occur at both interfaces and obtain an additional phase as depicted in Fig. 3.1(c)-(d). An electron is retroreflected as a hole at one of the NS interfaces. The retroreflected hole moves through the constriction with length L and is retroreflected as an electron. This process repeats itself. The electron obtains a phase in each cycle and Andreev bound states (ABS) form when the total phase is a multiple of 2π . In this case, the energy eigenvalues can be expressed in terms of the phase difference between superconducting regions ϕ [see Fig. 3.1(c)]. They are given by

$$\frac{E}{\Delta} \frac{L}{\xi_N} = 2 \arccos \left(\frac{E}{\Delta} \right) \mp \phi - 2\pi n, \quad (3.15)$$

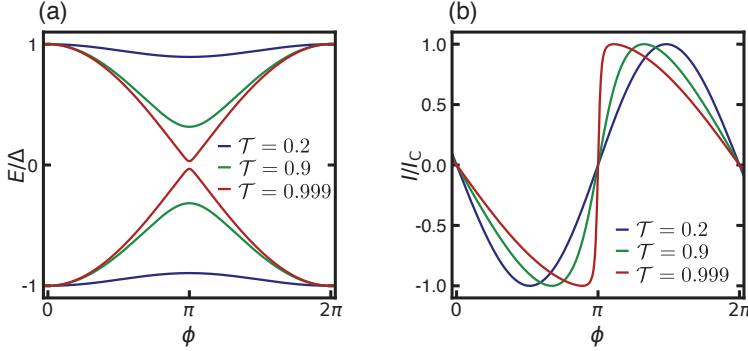


Figure 3.4: Andreev bound state energies. (a) Energy of Andreev bound states for different values of transmittivity \mathcal{T} . (b) Current-phase relationship (Eq. 3.18) of the lower bands, normalized by the critical current $I_C = |\max_{\phi}(I(\phi))|$.

where $\xi_N = (\hbar v_F)/(2\Delta)$ is the BCS coherence length [54]. The term on the left-hand side represents the dynamic phase that the electron acquires by traversing the N region. In the short junction limit ($L \ll \xi_N$) the dynamic phase can be approximated as zero and the lowest eigenvalues of the ABS are given by

$$E_{\pm} = \pm\Delta \cos\left(\frac{\phi}{2}\right). \quad (3.16)$$

Equation 3.16 describes ABS with a perfect interface. An imperfect interface can be modeled with the Z-parameter as previously described in Section 3.2.1 [55], leading to a more general expression for ABS energies

$$E_{\pm} = \pm\Delta \sqrt{1 - \mathcal{T} \sin^2\left(\frac{\phi}{2}\right)}, \quad (3.17)$$

where $\mathcal{T} = (1 + Z^2)^{-1}$ is the transmittivity of the junctions. The value of the supercurrent I depends on the phase difference between the two superconductors and is given by

$$I = \frac{2e}{h} \frac{dE}{d\phi}. \quad (3.18)$$

Equations 3.17 and 3.18 are plotted in Fig. 3.4. The Andreev levels can be un-

derstood as energy bands $E(\phi)$ with the Andreev band dispersion determining the current-phase relationship of the supercurrent.

The above discussion enables the theoretical description of an SNS junction as a building block for a transmon from the viewpoint of Andreev bound states. In this section, Eq. 3.17 was derived, which was the starting point for the discussion in Section 2.6*. The reason for this is that the Josephson current from each channel is the result of two Andreev bound states lying inside the N(Sm) region.

3.4 RCSJ MODEL

In this Section, we introduce the resistively shunted junction model (RCSJ model) [56,57]. Although Andreev bound states describe the charge transfer across a Josephson junction, a more complete (macroscopic) model is needed to describe a Josephson junction in finite-voltage situations [29]. In the RCSJ model the physical junction is modeled by the circuit shown in Fig. 3.5. The junction is modeled as an ideal Josephson junction, which is shunted by a resistance R and capacitance C . Here, C describes the capacitance between the two superconducting electrodes and introduces a displacement current. The resistance R describes the sum of quasi-particle and insulator leakage in the finite-voltage regime without affecting the dissipationless regime [29,33]. The circuit is assumed to be current biased as the device impedance is usually much smaller than the source impedance [33].

The current balance equation for this circuit is:

$$I = I_C \sin(\phi) + V/R + C \frac{dV}{dt}. \quad (3.19)$$

Replacing V with the second Josephson equation (Eq. 2.18) allows us to rewrite Eq. 3.19 into the second order differential equation

$$\frac{I}{I_C} = \sin(\phi) + \frac{1}{Q} \frac{d\phi}{d\tau} + \frac{d^2\phi}{d\tau^2}, \quad (3.20)$$

where $\tau = \omega_p t$ is a dimensionless variable and the other parameters are

*Equation 3.17 in this section corresponds to Eq. 2.53 for a single channel from Section 2.6 with different notation ($\mathcal{T} \rightarrow T, E(\phi) \rightarrow V(\hat{\phi})$).

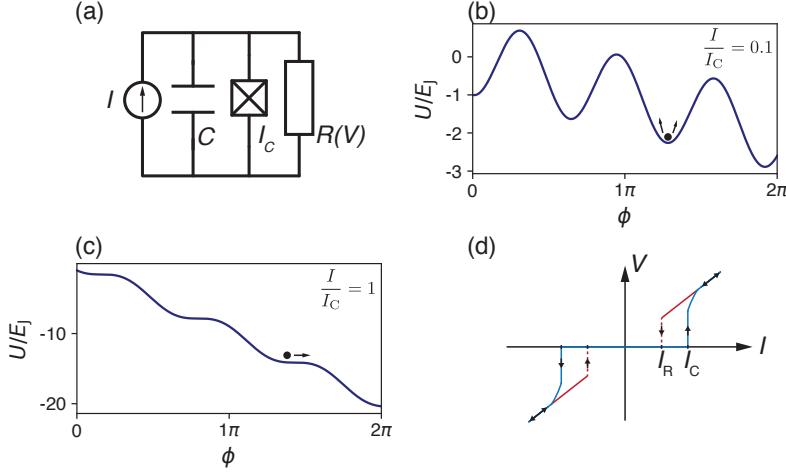


Figure 3.5: RCSJ model. (a) Equivalent circuit of a Josephson junction in the RCSJ model. The junction is current biased with a current I and consists of an ideal Josephson junction with critical current I_C , a resistance R and a capacitance C . Corresponding tilted washboard potential for (b) a situation where $I < I_C$ and (c) $I = I_C$. (d) Schematic of a hysteretic I-V curve with the critical current I_C and retrapping current I_R labeled and arrows indicating the current sweep direction.

defined as:

$$\omega_p = \sqrt{\frac{2eI_C}{\hbar C}}, \quad (3.21)$$

$$Q = \omega_p RC. \quad (3.22)$$

The parameters ω_p and Q are called the plasma frequency and the quality factor of the junction, respectively. Their meaning can be illustrated with the *tilted-washboard potential*, an illustration of the RCSJ model that is often used to explain and visualize the dynamics of a Josephson junction [29,33].

The differential equation Eq. 3.20 can be solved, where the solution is analogous to a particle with mass $(\hbar/(2e))^2 \cdot C$ moving along the ϕ -axis in a potential

$$U(\phi) = -E_J \cos(\phi) - \frac{\hbar I}{2e} \phi, \quad (3.23)$$

where $E_J = (\hbar I_C)/(2e)$ is the characteristic Josephson coupling energy we introduced in Chapter 2. Further, the particle is subject to a viscous drag force $(\hbar/(2e))^2(1/R)d\phi/dt$. Figures 3.5(b) and (c) illustrate different configurations of the tilted washboard potential. For current $I < I_C$ [Figure 3.5(b)] the particle is confined in a local minimum and oscillates around its equilibrium position with frequency ω_p . As the average ϕ does not change, no voltage builds up across the junction. When $I \geq I_C$ [Figure 3.5(c)] the local minima disappear and the potential turns into a downwards slope. The particle will move down the potential and change its coordinate ϕ continuously. A change in ϕ corresponds to a voltage built up across the junction (see Eq. 2.17).

The above description only describes a fluctuation-free junction and is independent of the quality factor Q . The quality factor Q is often used to classify a Josephson junction as *underdamped* ($Q \gg 1$) or *overdamped* ($Q \ll 1$) [29, 33]. Both junction types have different $I - V$ characteristics. Here, we will only focus on the underdamped regime as it is relevant for this thesis (see Chapter 6). To consider fluctuation, the position of the particle along the vertical axis can be understood as its total energy. With additional energy, e.g. thermal energy, a particle can already escape the minima, meaning the junction switches to a dissipative state with a switching current $I_{sw} < I_C$. When the junction is in the resistive state with $I > I_C$ and the current bias is reduced towards $I = 0$, the junction will switch back to the dissipationless state at a finite retrapping current I_R . When the junction is in the resistive state $I > 0$ the washboard potential is slightly tilted and the trajectory of the particle lies above all maxima, where the vertical position of the particle is given by the kinetic energy $\frac{1}{2}CV^2$. The particle will be trapped in a minimum as soon as the kinetic energy is not sufficient to move from one maximum to the next, which is the case for $\frac{1}{2}CV^2 = E_J(1 + \cos(\phi))$. This expression can be evaluated to yield

$$I_R = \frac{4I_C}{\pi Q}. \quad (3.24)$$

Considering thermal fluctuation, the measured I_R will be equal or greater than described in Eq. 3.24. When the particle is still above the local maxima a single downward fluctuation in energy leads to a trajectory that hits the potential and spirals down to a local minimum. The resulting $I - V$ characteristic of an underdamped junction is exemplified in Fig. 3.5(d). Due to the stochastic nature of fluctuations there is no single value for I_{sw} or I_R , but both are best

described by a distribution function. The exact distribution depends on the dissipative processes in the junction [58,59].

3.5 SHORT VS. LONG JUNCTION

Josephson junctions can be built in many different ways, for example by using different superconducting materials. A useful parameter to compare different junction types is the $I_C R_N$ -product, where R_N is the normal-state resistance of the junction. It is often used as a measurement of the similarity of a real Josephson junction and an ideal junction. The (theoretical) limit of the $I_C R_N$ product and its temperature dependence depend on the characteristic length scales inside the junction. Relevant for an SNS junction are:

- The length of the junction L , which is the distance between superconducting electrodes,
- The electron mean free path $l_e = \mu m^* v_F / e$ of the N-region, where μ is the mobility of an electron,
- The superconducting coherence length ξ_N inside the N-region,
- The Thouless energy E_{Th} , that is a measure of sensitivity of the system to boundary conditions [60].

The expressions for the length scales are different in the limits of ballistic transport ($l_e \gg L$) and diffusive transport ($l_e \ll L$) and are summarized in Tab. 3.2. Different expressions for the $I_C R_N$ product were derived in the short junction limit ($L \ll \xi_N$) and long junction limit ($L \gg \xi_N$).

	ξ_N	E_{Th}	short	long
ballistic	$\frac{\hbar v_F}{\pi \Delta}$	$\frac{\hbar v_F}{L}$	$L < l_e, \xi_N$	$\xi_N < L < l_e$
diffusive	$\sqrt{\frac{\hbar D}{2\Delta}}$	$\frac{\hbar D}{L^2}$	$l_e < L < \xi_N$	$l_e, \xi_N < L$

Table 3.2: Expressions for the characteristic length scales of an SNS junction in the ballistic and diffusive regime as well as the relationships between length scales that define the short and long junction limit [33,61].

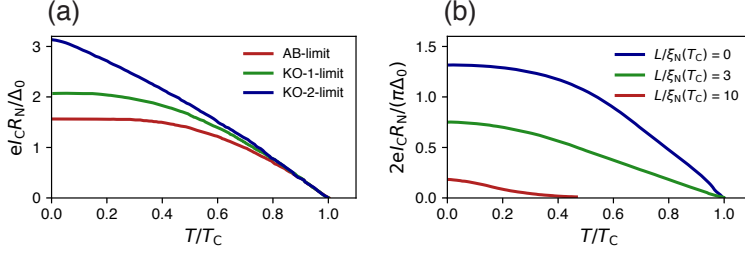


Figure 3.6: $I_C R_N$ product temperature dependence. Theoretically predicted temperature dependence of the normalized $I_C R_N$ product of (a) a short junction and (b) a long junction for different limits adapted from Ref. [61] with Δ_0 corresponding to the superconducting gap at $T = 0$ and $\xi_N(T_C)$ being the effective coherence length of the normal conducting material, if taken at the critical temperature of the electrodes.

Figure 3.6(a) shows solutions to the temperature dependence of the $I_C R_N$ in the short junction limit. The AB-limit is the solution in the tunnel limit (i.e. an SIS junction) derived by Ambegaokar and Baratoff [63]. Both solutions derived by Kulik and Omelyanchuk, namely the solutions for the KO1 limit ($l_e \ll L < \xi_N$) [64] and the KO2 limit ($L \ll l_e, \xi_N$) [65], describe short SNS junctions. The solutions for the long junction limit shown in Fig. 3.6(b) take the form

$$\frac{eI_C R_N}{2\pi T_C} = V^* \frac{L}{\xi_N^*} e^{-L/\xi_N^*}, \quad (3.25)$$

where the effective coherence length ξ_N^* and the factor V^* depend on the normalized temperature T/T_C [66].

3.6 FINITE-VOLTAGE REGIME OF AN SNS JUNCTION

Figure 3.7(a) shows an experimentally measured $I - V$ curve of a Josephson junction that is studied in Chapter 6. As discussed in Section 3.4, the current-biased Josephson junction switches into dissipative state when the current bias I_{SD} exceeds its critical current I_C^\ddagger . As evident in Fig. 3.7(a), the charge transport across the SNS junction in the dissipative state depends on the voltage drop across the junction V_{SD} . If $eV_{SD} \geq 2\Delta$, the junction is in the normal-

[‡]For simplicity we neglect the differences between the critical current I_C , the switching current I_{sw} and the retrapping current I_R here.

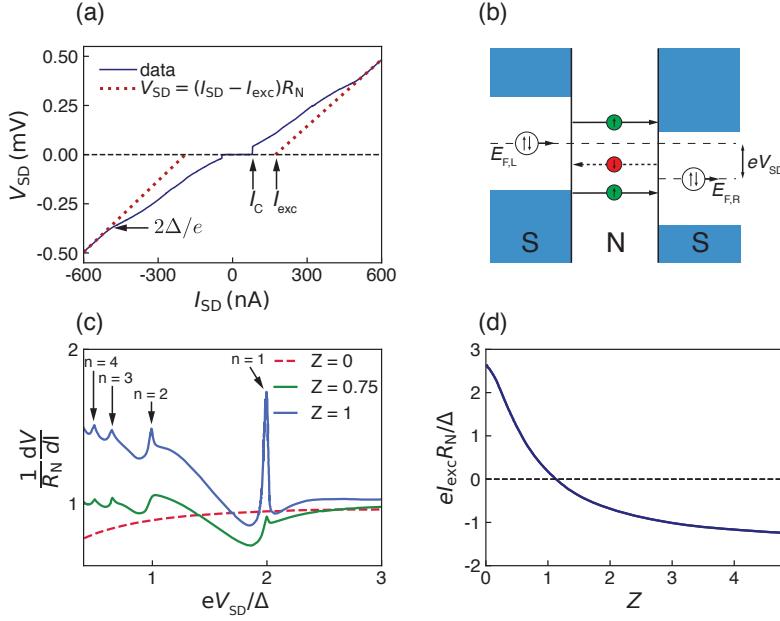


Figure 3.7: OBTK model predictions. (a) Measured I – V curve for an SNS junction that is characterized in Chapter 6. The current bias I_{SD} is swept from negative to positive values and the voltage drop V_{SD} is measured. The junction switches to a resistive subgap regime at I_C and to a normal conducting state at $e\Delta V_{SD} = 2\Delta$. The excess current I_{exc} can be extracted from a linear fit to the normal conducting state. (b) Energy space schematic of a third order multiple Andreev reflection. (c) Differential resistance dV/dI normalized by R_N of an SNS junction as a function of normalized voltage drop eV_{SD}/Δ for different values of Z -parameter adapted from Ref. [62]. Arrows indicate peaks that correspond to the positions of multiple Andreev reflection peaks with order n (Eq. 3.26). (d) Normalized excess current $eI_{exc}R_N/\Delta$ as a function of Z -parameter adopted from Ref. [62].

conducting state and exhibits an ohmic voltage characteristic that is described by $\Delta V_{SD} = \Delta I_{SD} R_N$. If $eV_{SD} < 2\Delta$, quasiparticles cannot tunnel across N-region in the subgap regime as the energy bands of both superconductors are not aligned. The potential difference is overcome by the process called *multiple Andreev reflections* (MAR), which transfers charge across the junction. When a quasiparticle Andreev reflects a single time the retroreflected particle has an energy that is mirrored around E_F . This process is repeated n times until

$n\Delta V_{SD} \geq \Delta I_{SD} R_N$. Figure 3.7(b) depicts the schematic of the MAR process with $n = 3$.

The OBTK theory [51], an extension of the BTK theory presented in Section 3.2.1, gives a quantitative description of the subgap regime. It assumes MAR processes across the junction and an imperfect barrier that can be described by the same Z -parameter as in the BTK theory. This result was later corrected in Ref. [62] to yield a better quantitative agreement between theory and experiment. Figure 3.7(c) shows the differential resistance dV/dI of an SNS junction as a function of voltage drop for different values of Z . The peaks in dV/dI are a signature of MAR and appear at voltages

$$eV_{SD} = \frac{2\Delta}{n}. \quad (3.26)$$

Further, the OBTK model relates the Z -parameter to the excess current I_{exc} . The excess current can be considered to be an additional current that is carried by the superconducting state of the junction and is defined by the equation $V_{SD} = (I_{SD} - I_{exc})R_N$ in the normal conducting state [see Fig. 3.7(a)].

4

Experimental Methods

In this chapter, device fabrication, experimental setups and experimental methods are discussed. Section 4.1 summarizes the requirements and considerations for the material systems developed in this work. Section 4.2 presents the concept of selective area growth. In Section 4.3, the design parameters and basic fabrications steps for qubit devices are described. Since the device fabrication varies greatly between different qubit devices, detailed descriptions of the fabrication steps will be given in the relevant chapters. Section 4.4 presents the mounting procedure used for loading samples into the cryogenic measurement setup described in Section 4.5. The measurement equipment used for DC transport and cQED measurements – including room temperature electronics – are discussed in Section 4.6 and Section 4.8, respectively. Section 4.7 presents the cQED measurement techniques used in this work.

4.1 cQED REQUIREMENTS FOR MATERIAL SYSTEMS

In order to be a suitable platform for scalable, gate-tunable transmons (gatemons) with long coherence times, a potential material system must fulfill several requirements:

- The substrate used to build the superconducting circuit should have a low dielectric loss-tangent at radio frequencies. Dielectric losses will

limit the qubit coherence times as well as the signal-to-noise ratio of the qubit readout. Substrates that are most commonly used for superconducting qubits are high-resistivity silicon and sapphire [9].

- The superconductor should induce a hard superconducting gap into the semiconductor, without any disorder-related subgap states [67]. Subgap states can be the result of a disordered interface [68] that gives rise to two-level systems (TLS) [69,70]. Two-level systems arising from disorder-related sub-gap states can lead to qubit decoherence [71].
- The Josephson junction (JJ) built with the superconductor-semiconductor system must have a gate-tunable critical supercurrent I_C . The precise range of numerical values depends on the desired qubit operation frequencies and the charging energy E_C . Given the standard design used in this work (same design as Ref. [28]), a qubit frequency $f_Q = 4 - 6$ GHz is achieved by tuning the critical current to $I_C = 20 - 45$ nA.
- The method by which the Josephson-junction is integrated into the superconducting circuit will determine the potential for scale up from a single qubit system to large scale quantum processors. Here, it is preferential that the active semiconductor component is monolithically integrated into the substrate during growth. This ensures that subsequent circuit design can be performed deterministically and that industry standard lithography techniques can be used for device fabrication [28].

Gatemons were first realized by Larsen et al, using InAs/Al epitaxial nanowires [21]. InAs was chosen due to low resistance ohmic contacts between InAs and metallic/superconducting electrodes [73], a high electron mobility [74] and an experimentally demonstrated induced hard superconducting gap [67]. However, the two structures used so far – VLS-grown nanowires and 2DEGs – cannot fulfill all the requirements listed above. In the case of VLS-nanowire gatemons [21] the nanowires were integrated into the cQED circuit by manually detaching individual nanowires from the growth wafer and placing them on the device chip. Such a serialized approach makes it prohibitively time consuming to integrate hundreds to millions of nanowires into a single circuit. While this problem could be overcome with technological developments like the placement of nanowires into a circuit using electrophoresis [75], selective area growth offers a deterministic placement of planar nanowires by

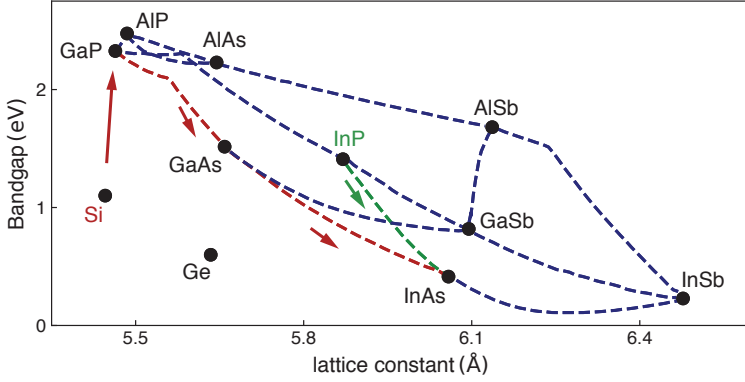


Figure 4.1: Lattice constant vs. bandgap diagram of commonly used semiconductors adapted from Ref. [72]. Dashed lines indicate ternary materials between materials AC and BC of the form $A_xB_{1-x}C$. The growth sequences used to achieve selective-area-grown InAs (SAG) on the substrate are highlighted in green for SAG on InP (see Chapter 5) and red for SAG on Si (Chapters 6 and 7).

direct growth on the the substrate. Gatemons with two-dimensional electron gas (2DEG) on InP [28] offer an relatively easy way to scale up as the mesa is defined via top-down fabrication methods. The limitation is that the lossy Fe-doped InP substrate limits qubit lifetimes to $T_1 \approx 2 \mu\text{s}$ [28].

The reason that high quality InAs-based 2DEGs have so far not been realized on e.g. low-loss Si substrates is linked to one long standing problem in solid state devices. That is, the large lattice mismatch between these materials. It has long prevented the large-scale incorporation of III-V semiconducting materials on Si substrates and is an active field of research for many applications such as solar cells [76] and other opto-electronic applications [77]. Figure 4.1 shows a lattice constant vs. band gap plot of commonly used semiconductor materials. When grown onto each other, any lattice mismatch between materials in a heterostructure produces some level of strain [78]. Large strain will cause defects that will limit the transport properties of the material - e.g. reduce the field-effect mobility [79–82]. It may even cause the material to break [83]. Instead of attempting a direct growth of InAs on Si, we gradually step through materials from left to right on the x -axis in Fig. 4.1. This method is commonly used to combine different semiconductor materials [84–86]. It is

aided by the use of ternary materials – e.g. $\text{In}_x\text{Ga}_{1-x}\text{As}$ – where the composition can be gradually changed during growth, facilitating effective strain compensation. Additionally, we use selective area growth techniques to reduce the lateral dimensions of the heterostructure [87]. This approach increases the ability of the heterostructure for strain compensation and enables the use of thinner layers [87]. The simplified growth sequences chosen in this work to build gatemons on InP and Si are highlighted in green and red in Fig. 4.1, respectively. For growth of InAs on InP, ternary materials along the green path are grown. For InAs on Si, first, GaP is grown directly on Si, due to the close lattice match. Thereafter, a thick GaAs layer is grown to until a certain material quality is reached (RMS surface roughness below 2 nm). From GaAs, InAs is grown directly, or by following the ternary InGaAs path. Specific growth parameters are given in Sections 5.1, 5.2 and 6.1.

4.2 SELECTIVE AREA GROWTH TECHNIQUE

Figure 4.2 shows the concept of selective area growth (SAG) [87]. A global dielectric layer is deposited on a semi-insulating substrate. Openings in the dielectric mask are created using standard electron beam lithography and etching techniques. A semiconducting, spatially confined channel is grown on the crystalline substrate in the dielectric opening using molecular beam epitaxy (MBE). Control over the material flux and growth temperature ensures that growth proceeds selectively on the substrate and not on the dielectric [87,88]. This enables the large scale bottom-up fabrication of a large number of complex structures after the initial mask preparation. The crystal orientation of the underlying substrate and orientation of the mask opening influence the selectivity, crystal quality and faceting of planar nanowire [87]. Buffer layers between the transport channel and substrate surface can be used to promote strain relaxation and thus improve transport properties of the nanowire. Al can be grown in-situ in the MBE as in Chapters 6 and 7 or at a later step as demonstrated in Chapter 5.

4.3 DEVICE LAYOUT

Progressing from the epitaxial nanowire Al/InAs growth to functional qubits requires integration in a cQED circuit by means of several lithography steps.

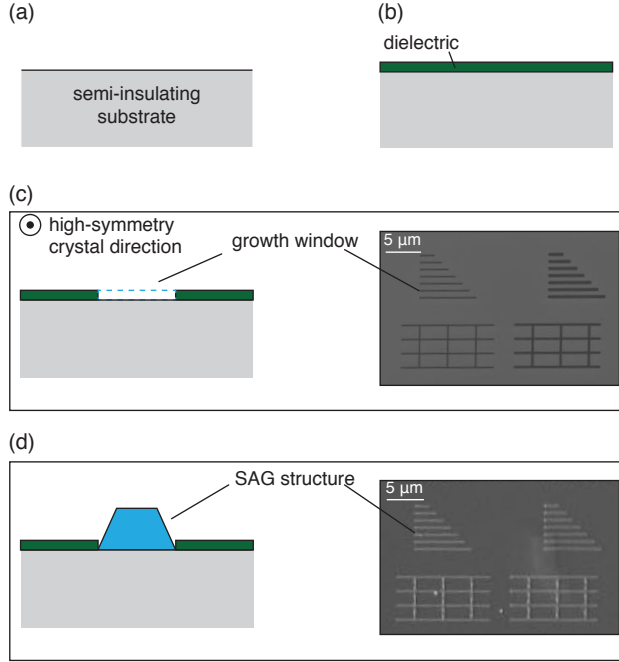


Figure 4.2: Schematic of selective area growth principle. (a) A blank substrate is prepared for growth by (b) depositing a dielectric layer and (c) patterning an opening using top-down lithography techniques. (d) The material is grown selectively in the mask opening while growth on the dielectric is suppressed by the choosing growth parameters within the selectivity window [87,88]. Scanning electron micrographs after the respective step are added in (c) and (d).

The standard design used in this thesis contains six qubits that can be simultaneously read out and controlled during the same cooldown. While the detailed process descriptions for InP SAG and Si SAG will be presented in Sections 5.1, 5.2 and 7.2 due to many important differences in the precise processing details, a brief overview of the processing is given here. At the start of fabrication, the entire chip is covered with a 40 nm thick Al film. The primary purpose is that this Al serves as the epitaxial Al layer in the InAs/Al hybrid, but also conveniently can be used to define many components of the cQED

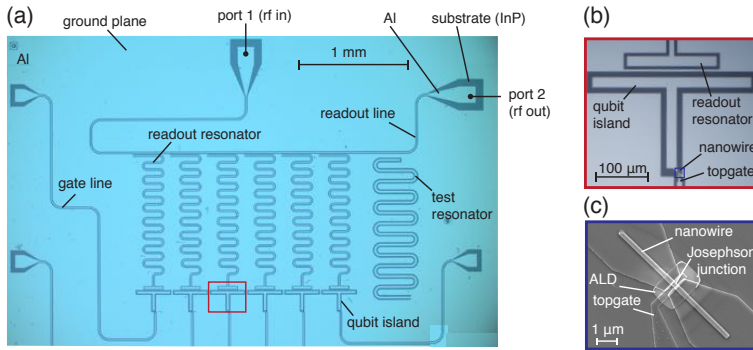


Figure 4.3: Qubit device layout. (a) Optical micrograph of a typical 6-qubit device. The patterned Al overlayer shows as light blue, with the underlying substrate showing as dark blue. Each qubit is controlled using an individual gate line and read out by an individual readout resonator. Each readout resonator and a test resonator are coupled to a common transmission line. (b) Zoomed in optical micrograph of a qubit island that is shunted to the ground plane using a gateable Josephson junction. (c) Scanning electron micrograph of a nanowire. The Josephson junction is formed by removing a $\sim 150 - 200$ nm long segment of Al. The junction and topgate are isolated by a 15 nm dielectric layer of HfO_2 .

circuit by selectively removing certain regions. The resonators and Josephson junctions are defined using electron-beam lithography (EBL) as shown in Fig. 4.3. Etched areas are defined by depositing a thin (~ 400 nm) film of PMMA (polymethyl methacrylate) and exposing this to a high energy (100 – 125 keV) electron beam, which is scanned over the substrate in the desired pattern. The exposed resist is removed via a solvent-based developer (methyl isobutyl ketone:2-propanol in 1:3 solution). Next, Al is selectively removed using a wet-etch solution (Transene Al Etchant Type D at 50°C). This defines the larger features visible in Figs. 4.3(a)-(b): the transmission line, readout resonators, qubit islands, a test resonator and gate lines. The gate-tunable JJs are formed by removing a ~ 150 nm long segment of Al from the InAs nanowire. The gate dielectric consists of 15 nm HfO_2 deposited by atomic layer deposition in lithographically pre-defined regions [see Fig. 4.3(c)]. Topgates (50 nm thick Al) are evaporated on top of the HfO_2 , and are used to tune the critical currents of the single JJs and thereby the qubit frequencies. In the final step, the topgates are

electrically connected to the gate lines with additional Al-patches. This step is preceded by RF Ar-milling to remove the AlO_x that develops on the topgate and gate lines due to exposure to atmosphere, and ensure a metallic contact.

The transmission line, resonators for qubit readout, and a test resonator for the measurement of dielectric losses are designed as coplanar waveguides (CPWs) [32]. The impedance of the CPW is set by only the dielectric constant of the underlying substrate and the ratio of the central conductor and gap. Therefore, the impedance of the readout line Z_{readout} can easily be matched to the impedances of the rest of the experimental setup, usually $50\ \Omega$ as discussed in Section 2.1. For CPWs the electrical fields are mainly contained in the gap such that radiation losses are reduced [32]. The dense packing of neighboring resonators is possible as the electrical fields in ground planes reduce exponentially with the distance to the central conductor. The readout resonators are designed as distributed quarter wave resonators ($\lambda/4$) [89] that are coupled inductively to the transmission line and capacitively to the qubit island. The coupling to the transmission line can be expressed using the coupling quality factor Q_{ext} . Most devices are designed with $Q_{\text{ext}} \approx 10^4$. Typical resonance frequencies f_r for the readout resonator are 6 GHz – 7.5 GHz. Qubits are usually operated at 4 – 6 GHz. The qubit islands geometry is chosen to set the charging energy to $E_C/h = e^2/(2C_\Sigma) \approx 230\text{ MHz}$, where C_Σ is the sum of all capacitances of the qubit system and to set the coupling between qubit and resonator to $g/h \approx 80\text{ MHz}$. The coupling g is given by the ratio $\beta = C_g/C_\Sigma$ (see Section 2.4). All the capacitances have been estimated using electrostatic simulations [90].

4.4 MOUNTING THE DEVICES

After the qubit devices are fabricated they are loaded in the dilution refrigerator and cooled down to millikelvin temperatures. In a first step, the qubit device is glued to a printed circuit board (PCB) with a droplet of PMMA. After the PMMA has dried, bond wires are placed to connect the lines of the qubit chips to the lines of the PCB as shown in Fig. 4.4(a). The aspect ratio of the lines of the PCB is designed to match the impedance $Z = 50\ \Omega$ of the rest of the setup. To avoid unwanted modes on the chip a dense pattern of bonds is used to connect the ground planes of the PCB and qubit chip [91]. For further suppression of unwanted electromagnetic modes on-chip bonds are placed to

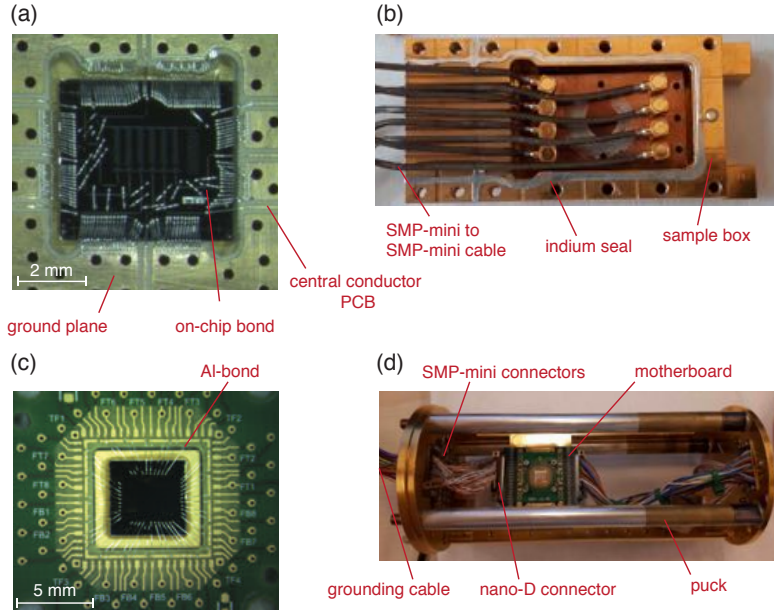


Figure 4.4: Device packaging. (a) Example of a qubit device glued and bonded to a PCB. The transmission line and gate lines are connected to the striplines of the PCB, which are connected to SMP-mini connectors that are soldered to the PCB. The sample is mounted to an indium-sealed CuBe box and RF cables are connected as shown in (b). (c) Device packaging for DC transport devices and devices operated at RF frequencies. Example of a DC transport device glued and bonded to a PCB daughterboard. The bonded device is then loaded into the motherboard and puck as shown in (d).

connect parts of the ground plane on different sides of the gate lines and the transmission line. In practice, placing on-chip bonds reliably is not always possible for devices fabricated on InP-substrates due to bad adhesion of the Al-layer on the substrate. As a consequence, no on-chip bonds were placed for most InP-based devices.

Careful sample packaging of qubit devices is necessary to achieve long qubit coherence times for several reasons. Superconducting qubits are very sensitive to a wide radiation spectrum from radio-frequencies [92] to frequencies in the infrared spectrum [93,94]. Further, relaxation times can be reduced if the qubit is insufficiently thermalized, leading to thermally generated quasi-

particles [95]. In addition, readout fidelities are reduced by a thermal residual excited-state population [96]. To avoid these relaxation mechanisms, the bonded device is placed in a CuBe-box that is coated with light absorbing paint and covered with a CuBe-lid. The CuBe-lid on top of the box additionally suppresses box resonances at qubit frequencies. CuBe is used to enable effective qubit thermalization through its relatively high thermal conductivity at low temperature. Further, heating from eddy currents is reduced by the relatively low electric conductance when operating devices in large magnetic fields. Trenches in the box ensure that flexible cables that connect the device with SMP-mini connectors in the puck are not damaged and squeezed when the box is closed. The SMP-mini connector in the puck will engage with the counterpart of the cold finger plate inside the dilution refrigerator, where the sample connects to the cables inside the setup. This enables the control of the qubit devices from room temperature using the electronics inside the cryostat. Due to the large size of the soldered SMP-mini connectors on the PCB the amount of lines per device is limited to eight lines. Indium is used to seal the box [Fig. 4.4(b)] from infrared black body radiation originating from warmer stages of the fridge.

A different PCB is used for transport measurements [see Fig. 4.4(c)]. Losses at high frequencies are no concern for most transport measurements and ground planes between conductors are not needed. Therefore, more lines can be put on a PCB of the same size. The PCB shown in Fig. 4.4(c) has 48 DC lines to which the sample leads can be bonded to, and is known as a 'daughterboard'. The corresponding 'motherboard' to which the 'daughterboard' can fit to is placed in the puck as shown in Fig. 4.4(d) and connected with a nano-D connector. The motherboard has two nano-D connectors for connection to external electronics. Two connectors are used to ensure that one side of the device can always be grounded during the loading procedure. Devices are grounded at all times as electrostatic discharge could damage or break devices. When loaded the nano-D connector of the puck connects to a counterpart in the cold finger plate inside the dilution refrigerator.

4.5 DILUTION REFRIGERATOR

Most of the measurements were taken in a cryofree dilution refrigerator [97] to reach low temperatures below the critical temperature of Al, $T_{C,Al} \sim 1.2$ K.

Figure 4.5(a) shows the interior of the dilution refrigerator. The cryofree dilution refrigerator uses a pulse tube cooler to precool the system to $PT2 \approx 4$ K. To cool down the sample further to millikelvin temperatures a $^3\text{He}/^4\text{He}$ mixture in a closed circuit is used. Below a critical temperature, the mixture separates into a ^3He -rich and ^3He -dilute phase, separated by a phase boundary. The ^4He composing the bulk of the dilute phase is superfluid and can be considered noninteracting. The ^3He -rich phase is lighter than the ^3He -dilute phase that is rich in ^4He and the ratio of ^3He and ^4He in both phases are fixed at any given temperature. Since the enthalpy of ^3He in the two phases is different, the crossing of ^3He across the phase boundary from the ^3He -rich into the ^3He -dilute phase may provide highly effective cooling. To use this cooling effect, the refrigerator is constructed in a way that the phase boundary occurs in the mixing chamber. The more dense ^3He -dilute phase resides below the ^3He -rich phase. A pipe leading to a chamber called the still sits below the this boundary. When ^3He is removed from the ^3He -dilute phase via pumping, ^3He will cross the phase boundary and cool the environment. Inside the fridge, the ^3He is continuously circulated and the cold, outflowing ^3He is used to cool the relatively warm inflowing ^3He via heat exchangers. This process works even at the lowest temperatures since the equilibrium concentration of ^3He in the dilute phase is finite even at zero temperature. One of the advantages of a cryofree dilution refrigerator are that devices can be loaded into the setup while the dilution refrigerator is fully precooled (but the mixture is not circulating), enabling the exchange of samples on a daily basis.

Performing cQED measurements demands low-noise instrumentation, and as such many electronic components are mounted inside the dilution refrigerator to cool and shield them. A significant part of my work was to continually modify and optimize the setup to make it suitable for high quality cQED measurements. Fig 4.5(a) shows the fridge in an intermediate state after some of these upgrades, and was used in this state for the measurements in Chapter 7. Earlier measurements did not benefit from all of the modifications. This setup is designed to load two separate gate controlled 6-qubit devices together and measure them simultaneously. Several considerations are taken into account preparing and assembling the setup, such as ensuring the thermal load remained within the $200 \mu\text{W}$ cooling power of the cryostat, sufficient thermal anchoring for all components, the limited space between the bottom of the mixing plate at the shielding, ensuring DC signals and RF signals are filtered

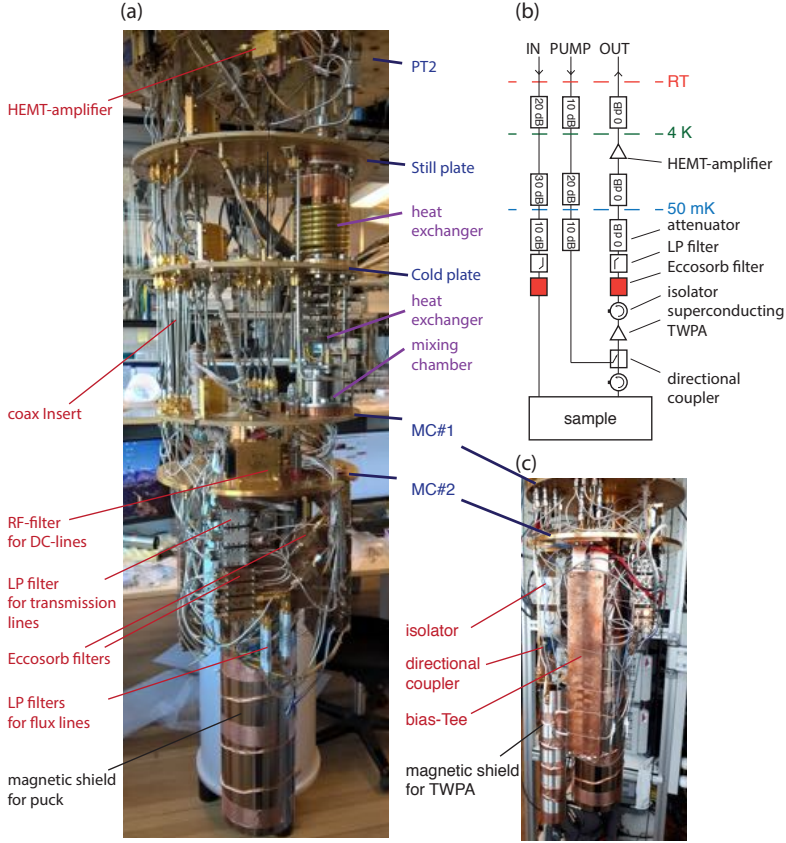


Figure 4.5: Dilution refrigerator setup. (a) Photograph of the dilution refrigerator with the shields of all temperature stages removed. The electrical components (red), temperature stages (blue), cryogenic components (purple) and magnetic shields (black) are labeled. All electrical components below the mixing chamber plate (MC) are attached to mounting brackets that were specifically designed for the setup. The magnetic shield for the traveling wave parametric amplifier (TWPA) is closed on the bottom. The superconducting shield for the puck is open to enable bottom-loading. Below the MC, flexible non-magnetic coaxial cables are used to connect different parts of the circuit. (b) Simplified schematic of the readout circuit. (c) Close-up of the bias tee and TWPA.

sufficiently before reaching the sample.

Considering the suppression of readout noise, an important aspect is to limit the amount of thermally induced noise by ensuring the inner conductors of all coaxial lines are properly thermalized. This is achieved by attenuating the single lines at different stages as shown in Fig. 4.5(b). On the return side, 0 dB attenuators are used to achieve the highest possible readout signal. In an attenuator both inner and outer conductor are galvanically connected with each other, enabling cooling of the inner conductor via the outer conductor. In all other components, the presence of low thermal conductance electrical insulation between inner and outer conductor prevents thermalization of the inner conductor. While the attenuators also reduce the power of ingoing signals, the only purpose on the return side is the thermalization of the coaxial lines. The mounting brackets further help thermalizing the coaxial lines. Below the mixing chamber plate, flexible coaxial cables are used instead of rigid cables as they offer an additional degree of freedom and allow denser cable packing. All filters are attached to the mixing chamber plate (MC #2) via brackets with a large contact area for sufficient thermalization. In-house made bias tees shown in Fig. 4.5(c) are used to combine DC and RF signals for qubit control. The DC signal is used to apply a gate voltage to the Josephson junction and control the qubit frequency (see Section 2.4), while the RF signal drives the qubit at frequencies between 4 and 6 GHz. To reduce frequency dispersion, the bias tees contain a series of filters that result in a flat attenuation in this frequency range. A cylindrical Mu-metal shield is attached to the mixing chamber to shield the sample from external magnetic fields. This shield is open on the bottom-end to enable sample loading. When operated, multiple shields are anchored to the different plates to shield the interior from radiation and an outer vacuum can is attached to enable the system to be pumped to ultra-high vacuum. The second Mu-metal shield visible in Fig. 4.5(a) screens an important part of the readout circuit - the superconducting traveling wave amplifier (TWPA) [98] - which we discuss as part of the readout circuit below.

A schematic of the readout circuit is shown in Fig. 4.5(b). The ingoing signal is attenuated by ~ 60 dB before reaching the sample and amplified by ~ 60 dB after the sample. The high attenuation is needed to perform the experiments in the single photon/excitation regime [39]. A low power is also essential to ensure the qubit components remain in the superconducting state. In addition, low-pass filters and in-house made Eccosorb CR-110 filters are

used for filtering. The Eccosorb material filters infrared radiation from the warmer cryostat stages that propagate through the inner conductor of the coaxial cables. On the return side the signal is amplified at two stages, using the TWPA at base temperature and a high electron mobility transistor (HEMT) amplifier at ~ 4 K. The amplification process of the TWPA is based on the principle of 3-wave mixing and requires a pump signal that is supplied via a directional coupler. The TWPA offers a gain of ~ 20 dB with a high dynamic range 4 – 8 GHz [98] with a maximum input power of ~ -100 dBm. The Isolators before and after the TWPA are used to prevent reflected signals from amplifiers to reach the sample or TWPA and reduce noise in the readout signal. The HEMT amplifier is powered with a voltage supply at room-temperature and offers an amplification of 40 dB over a range from 4 – 8 GHz.

4.6 DC TRANSPORT SETUP

Figure 4.6 shows a schematic of the room temperature electronic circuit used in DC transport measurements (Chapter 6). DC characterization focused on current biased, four-terminal measurements of differential resistance, dV/dI . dV/dI was measured directly using a combination of AC and DC signals, relying on the principle that if the AC currents and voltages are small compared to the DC currents and voltages, they represent dI and dV [78]. To achieve this signal, the AC voltage output of a lock-in amplifier was combined with the DC output of a source meter using a voltage divider/adder circuit with a common ground resistor $100\text{ k}\Omega$. The AC (DC) signal was reduced by approximately 10^{-4} (10^{-2}) before being fed to a $100\text{ k}\Omega$, with the resistance chosen to be a factor of 100 larger than the sample resistance to ensure a constant current bias. On the measurement side, the outgoing current was converted to a voltage signal using a transimpedance amplifier, while the potential difference across the sample was converted into a voltage-to-ground using a differential amplifier. Each of these signals was split again to enable four simultaneous measurements: the two AC components (voltage and current) were measured using two separate, phase aligned lock-in amplifiers to give dV and dI . The two DC components were measured using multimeters after filtering each signal to remove the AC components. The settings for each instrument are given in Appendix E. The gate voltage V_G was supplied using the second channel of the dual-channel source meter. Two sets of RC and RF filters - one

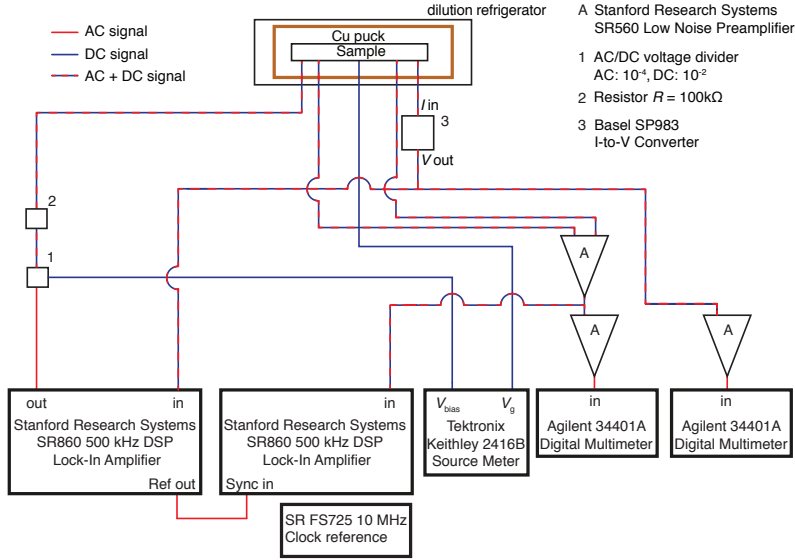


Figure 4.6: Schematic of the DC measurement setup used for four-terminal, current biased, DC transport measurements (Chapter 6). Red lines indicate cables that carry an AC signal, blue lines indicate lines that carry a DC signal and blue-red dashed lines indicate cables that carry both components. All instruments are synchronized with a 10 MHz clock reference. To measure the device in a two-terminal voltage-bias configuration the bias resistor ($R = 100 \text{ k}\Omega$) is removed and only the signal after the transimpedance amplifier (Basel SP983) is measured with the lock-in amplifier to obtain dI/dV .

set on the MC plate and the other on the motherboard - were used to enhance the signal-to-noise ratio.

A similar setup is used to measure in a two-terminal, voltage bias configuration. For this, the bias-resistor is removed and all instruments that are used to measure the voltage drop are disconnected. The AC voltage that is measured with the remaining lock-in amplifier is directly proportional to the differential conductance, dI/dV .

4.7 cQED MEASUREMENT TECHNIQUES

This section presents the different types of cQED measurements techniques for the characterization of gatemons. The key aspect of all measurements is that the resonance frequency of the readout resonator f_r depends on the qubit state as described in Section 2.4. A vector network analyzer (VNA) enables fast measurements with a wide dynamic range, making it well suited for initial measurements of f_r and the qubit frequency f_q . The VNA mixes the incoming signal with a reference tone and thereby measures the transmission between ports 1 and 2, S_{21} , directly. Figure 4.7(a) presents typical measurements of a readout resonator as a function of readout signal power at the device, P_{rf} . At high input powers, the resonator is at its bare resonance frequency $f_{r,bare}$, where it is unaffected by the qubit [99]. At lower power the resonator and qubit hybridize and the resonator shifts relative to $f_{r,bare}$ by $\chi_{01} = g^2/\Delta$, where g is the coupling between qubit and resonator and $\Delta = 2\pi(f_r - f_q)$. The evolution

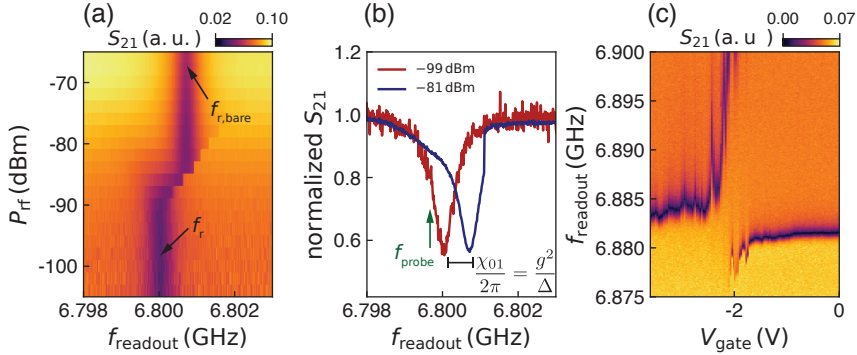


Figure 4.7: Examples of continuous readout measurements acquired with the VNA. **(a)** Transmission S_{21} near the resonance frequency f_r of a readout resonator as a function of probe power at the device P_{rf} . **(b)** Two linecuts from (a) with the transmission normalized with respect to the transmission coefficient far off resonance. The difference between the resonance frequency of the bare cavity (blue) and the hybridized cavity (red) χ_{01} is given by the coupling between qubit and readout resonator g and the frequency difference $\Delta = 2\pi(f_r - f_q)$. The green arrow indicates the frequency f_{probe} that would be used for two-tone spectroscopy. **(c)** Readout resonator as a function of applied topgate voltage at the qubit Josephson junction V_G . The qubit frequency passes through f_r around $V_G = -2$ V.

of f_r away from f_q is demonstrated in Figs. 4.7(a)-(b). Figure 4.7(c) shows a measurement where f_q is modulated by applying the gate voltage V_{gate} at the Josephson junction. The qubit passes through the readout resonator at around $V_G = -2\text{ V}$, where the readout resonator shows an avoided crossing.

In addition to the resonator tone f_r , a second drive tone, f_{drive} , is necessary in order to manipulate the qubit. In this thesis, the qubit is operated in the dispersive regime ($2\pi|f_r - f_q| \gg g$), where f_r shifts by $\chi = \chi_{01} - \chi_{02}/2$ de-

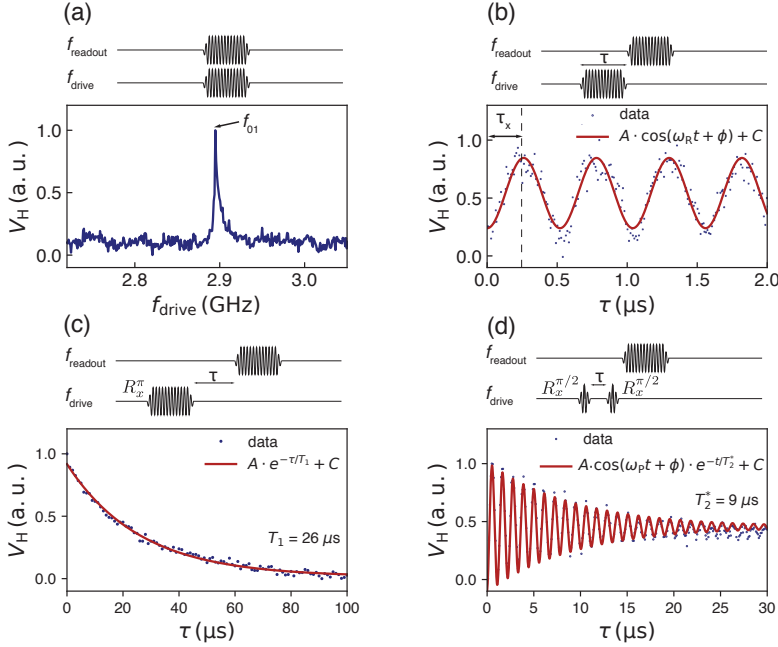


Figure 4.8: Examples of pulsed readout measurements acquired for a qubit with corresponding pulse schemes. Fits and equations are added to the data in panels (b)-(d). These qubit are standard transmons with Al/AlO_x/Al junction [23] that were fabricated by Kyle Serniak and Greg Calusine from Will Oliver’s group at the Lincoln Laboratory, Massachusetts Institute of Technology. These measurements were used to calibrate the cryogenic setup and room-temperature electronics after the most recent upgrade. **(a)** Continuous drive two-tone spectroscopy. **(b)** Coherent (Rabi) oscillations for $f_{\text{drive}} = f_q$. The duration τ_x for a R_x^π pulse is extracted from these oscillations. **(c)** T_1 -measurement of the qubit. **(d)** Ramsey-like measurement of the qubit to extract T_2^* .

pending on the qubit state (see Section 2.4). Further, all measurements of the qubit state in this thesis utilize this state-dependent shift, with typical values $\chi \approx 10 - 100$ kHz, and is measured by monitoring the transmission at a fixed frequency f_{probe} . The frequency f_{probe} is chosen such that it coincides with a steep region of the resonator feature, effectively amplifying the transmission change when the qubit is excited [see Fig. 4.7(b)]. Representative measurements are shown in Fig. 4.8. In Fig. 4.8(a) f_{drive} is swept around f_q and the transmission changes considerably when $f_{\text{drive}} = f_q$, resulting in a peak or dip depending on the relative position of f_{probe} to f_r and f_q to f_{probe} . The single peak in the amplitude of the readout tone V_H in Fig. 4.8(a) corresponds to the transition between the $|0\rangle$ and $|1\rangle$ states. At increased drive powers, other multi-photon transitions such as transitions between states $|0\rangle$ and $|2\rangle$ states become measurable using two-tone spectroscopy. Two-tone-spectroscopy is useful for both measuring the qubit frequency and estimating the dephasing time [100] but is limited to continuous drive schemes where the drive and readout tone are applied simultaneously.

A continuous drive does not offer the degree of the qubit control that would be necessary for universal quantum computing [101]. Instead, time resolved pulse schemes are needed, where pulse durations and timing between different pulses can be controlled. Figure 4.8(b) shows Rabi oscillations, where the qubit is driven for a time τ and oscillates between the $|0\rangle$ and $|1\rangle$ state with the Rabi frequency ω_R . This measurement is used to calibrate the gate R_x^π that rotates the qubit state by π around the x -axis, preparing the qubit in the $|1\rangle$ state. The gate is simply realized by a pulse with the period τ_x . Figure 4.8(c) shows a measurement of the relaxation time T_1 . First, the qubit is prepared in the $|1\rangle$ state. The qubit is allowed to relax into the ground state for a variable time τ before it is read out via the resonator. T_1 is extracted from a fit to the exponential decay. To extract the dephasing time T_2^* two $R_x^{\pi/2}$ pulses with a waiting time τ between them are used. The first pulse rotates the qubit state on the equator of the Bloch sphere, where the qubit state is allowed to process around the z -axis with frequency ω_p until the second pulse is applied. The probability that the qubit is in the excited state oscillates periodically within an exponentially decaying envelope due to dephasing. T_2^* is extracted by fitting a coherent oscillation with an exponential decay as shown in Fig. 4.8(d).

The time-domain measurements described above cannot be made using a VNA. Instead, an arbitrary waveform generator (AWG), a field-programmable

gate array (FPGA card), and IQ mixer are used for single-sideband mixing (SSB), data processing and pulse generation. Figure 4.9 shows a schematic of a setup that can be used for this purpose. Time-dependent waveforms are uploaded to the AWG that in turn modulate the output of two RF sources, effectively generating the pulse sequences illustrated in Fig. 4.8. This is achieved by applying the pulses to the IQ mixer port of the RF source. I and Q represent the real, $I(t)$, and imaginary, $Q(t)$, components of the signal generated by the AWG - also known as "in-phase" and "quadrature", respectively. The resulting modulated voltage signal at the RF output is then given by:

$$V(t) = I(t) \cos(\omega_{\text{rf}} t) + Q(t) \sin(\omega_{\text{rf}} t), \quad (4.1)$$

where ω_{rf} denotes the set signal frequency of the RF source. Typically, a rectangular pulse with pulse duration τ is used for the qubit drive [see Fig. 4.8]. For simplicity, we define the rotation of the qubit state as rotation around the x-axis of the Bloch sphere, when the rectangular pulse is only applied as $I(t)$. The consequence is that rotation around the y-axis can simply be realized by only uploading the pulse as $Q(t)$. More elaborate waveforms are usually used in the field of quantum computing to perform operations other than simple rotations or to increase the gate fidelity [14]. Heterodyne detection is used for readout, whereby a reference signal and readout signal with different frequencies are mixed to create a third signal at a lower frequency, called intermediate frequency (IF). In the schematic in Fig. 4.9, the RF source outputs two signals; the reference signal – often referred to as local oscillator (LO) –

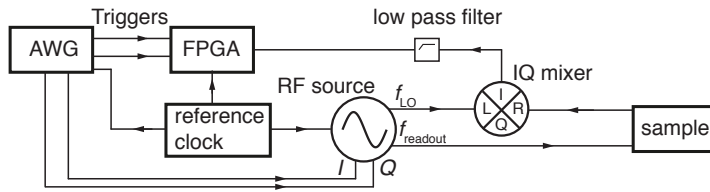


Figure 4.9: Schematic of a demodulation circuit for single sideband demodulation with a single RF source. Arrows indicate the direction of the signal. In order to manipulate the qubit a second RF source is added and modulated with the AWG. The FPGA is controlled via triggers from the AWG. The reference clock synchronizes all instruments.

at f_{LO} and the readout tone/input signal at f_{readout} . In order to offset the output of both ports waveforms of the form $I(t) = \cos(\omega_{\text{demod}}t)$ and $Q(t) = \mp \sin(\omega_{\text{demod}}t)$ are applied to the I and Q ports of the RF source, respectively. The generated signal is given by:

$$\begin{aligned} V(t) &= I(t) \cos(\omega_{\text{LO}}t) + Q(t) \sin(\omega_{\text{LO}}t) \\ &= \cos(\omega_{\text{demod}}t) \cos(\omega_{\text{LO}}t) \mp \sin(\omega_{\text{demod}}t) \sin(\omega_{\text{LO}}t) \\ &= \cos[(\omega_{\text{LO}} \pm \omega_{\text{demod}})t]. \end{aligned} \quad (4.2)$$

The signal with the lower frequency is chosen as readout frequency $\omega_{\text{readout}} = \omega_{\text{LO}} - \omega_{\text{demod}}$, where $\omega_{\text{demod}}/(2\pi) = 10 - 100 \text{ MHz}$ is typically used. The returning signal with frequency ω_{R} is down-converted to ω_{demod} with the IQ mixer to

$$\begin{aligned} V(t) &= A_{\text{readout}} \cos(\omega_{\text{readout}}t + \phi) \cdot A_{\text{LO}} \cos(\omega_{\text{LO}}t) \\ &= \frac{A_{\text{readout}}A_{\text{LO}}}{2} [\cos((\omega_{\text{readout}} - \omega_{\text{LO}})t + \phi) + \cos((\omega_{\text{readout}} + \omega_{\text{LO}})t + \phi)], \end{aligned} \quad (4.3)$$

where A_{readout} and A_{LO} are the amplitudes of the readout signal and the LO, respectively, and ϕ is the phase difference between the reference signal and transmitted signal. The high frequency component of the signal is removed using low pass filters such that only a low frequency signal with ω_{demod} reaches the FPGA card for readout. Due to the probabilistic nature of qubits, as well as noise in the readout chain, a measurement with a specific set of parameters must be repeated many times. Typically, $10^3 - 10^4$ single measurement are averaged to obtain a single data point. For example, each data point in Fig. 4.8(b) is the result of $2 \cdot 10^3$ averages. In order to reduce the time for an actual measurement, all waveforms that should be measured are uploaded to the AWG before the measurement. Alongside the waveforms for readout and qubit manipulation, the AWG sends two triggers to the FPGA to initialize measurements. The first trigger indicates the start of a sequence, the second trigger the start of each measurement cycle. The digitized signal contains both the amplitude and phase of the return signal.

4.8 cQED SETUP

Figure 4.10 shows a schematic of the setup used for the cQED measurements presented in Chapter 7. An RF switch was used to redirect signals to perform both measurement techniques that are discussed in Section 4.7, frequency-domain (continuous readout) and time-domain measurements (pulsed readout) without the need for rewiring the setup. For frequency-domain measurements, a vector network analyzer (VNA) was used for both signal generation and readout, since it is capable of rapidly switching between frequencies over a range 10 kHz - 20 GHz. For pulsed readout, the input signals were generated by using an AWG to modulate the output of RF sources (component A). The

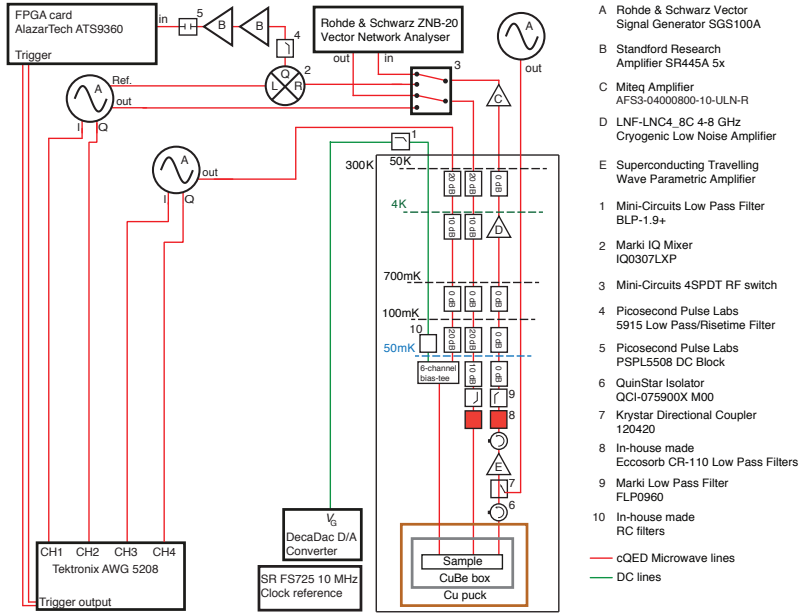


Figure 4.10: Schematic of the cQED measurement setup used in Chapter 7. The red lines represent cables that carry RF signals. Green lines represent cables that are used for applying DC voltages (qubit frequency control). All instruments are synchronized via a 10 MHz clock reference. The setup is designed to switch between frequency-domain and time-domain measurements effectively. Both techniques are discussed in detail in Section 4.7

input signal was attenuated and filtered before reaching the device. On the measurement side the signal was amplified, demodulated with a mixer and digitized with a FPGA card. Filters and amplifiers with a low cut-off frequency ensured that only the lower-sideband is recorded (see Section 4.7). For most measurements the demodulation frequency was set to $f_{\text{demod}} = 15$ MHz by offsetting the local oscillator signal (LO) by 15 MHz relative to the readout tone. A detailed description the electrical components inside the dilution refrigerator can be found in Section 4.5.

The qubit frequencies were controlled via the gate voltage V_G that was sourced by a digital-to-analog converter (DAC), where the DC signal was filtered at two stages, with a LP filter at room-temperature and inside the bias tee. The multi-channel bias tee was used to combine V_G with the qubit drive at the MC stage. By driving the qubit through the bias tee, meaning effectively driving it through the gate line, higher signal power could be applied since the gate lines in the setup are less attenuated and filtered than the readout lines. Alternatively, the qubit could be driven through the readout resonator. This approach limits power that can be applied to the qubit as, in practice, a very high drive power will lead to additional reflections that increase the difficulty of measurements.

The setup used in Chapter 5 for cQED measurements differed from the setup presented in this section. The main differences are that different bias tees were used and an additional RF source was used to generate the LO-signal. The resonator tone and qubit drive tone were combined with a power splitter. This way the qubit was driven the transmission line. A detailed schematic can be found in Appendix C.

5

The InP SAGmon

In this chapter, we show proof-of-principle measurements which demonstrate that gatemons can be made with selective-area-grown (SAG) Al/InAs material systems. For this demonstration SAG structures on InP substrates are used. The results are discussed in two large sections, reflecting that the project went through two distinct phases. Section 5.1 presents the results from the first phase, encompassing growth mask fabrication, first generation material growth, gatemon fabrication and gatemon measurements. Section 5.2 summarizes the second phase, including second generation material growth, device fabrication, material characterization using DC-transport and gatemon measurements.

5.1 FIRST GENERATION DEVICES

The first gatemon devices using selective-area-grown structures were made on Fe-doped InP for two reasons: the availability of the technology and the relatively low radio frequency losses. Selective-area-grown InAs on InP had already been reported in Ref. [87]. Additionally, resonator tests that led to the development of the 2DEG gatemon [28] had previously identified Fe-doped

InP as substrate with the lowest dielectric loss among the tested substrates.*

5.1.1 PRE-GROWTH FABRICATION

As the general principle of selective area growth has already been discussed in Section 4.2, only the important process details will be presented in this Section. An overview of the process parameters can be found in Appendix A. The dielectric growth mask consisted of thin SiO_x (10 nm), deposited using plasma-enhanced chemical vapor deposition (PECVD). The mask was etched with ammonium fluoride, followed by a cleaning step including acetone, 2-propanol, MQ and oxygen plasma cleaning. The nanowires for qubit devices were defined by openings in the mask with a length of $10\text{ }\mu\text{m}$ and a width varying from 100 – 500 nm. Additionally, openings for small test structures and larger alignment mark structures were patterned.

5.1.2 MATERIAL GROWTH

Figure 5.1 illustrates the different growth steps. First, 20 nm InP was regrown on the InP substrate using chemical beam epitaxy (CBE), followed by the growth of 17 nm of InAs. The regrowth was integrated to increase the InP/InAs interface quality and thus increasing the overall crystal quality. Due to the regrowth InAs can be grown on a pristine InP surface instead of a surface that was damaged by etchant and exposed to air. As the CBE system did not contain an Al-source, Al was grown in a second growth chamber using molecular beam epitaxy (MBE). Preferably, Al would have been grown in-situ as previous works had already demonstrated that in-situ growth of Al on InAs nanowires leads to a hard superconducting gap in the semiconductor, without any disorder related states [67, 102]. Instead, the wafer was dipped into diluted hydrofluoric acid (HF) before loading it into the growth chamber to clean the surface, followed by hydrogen assisted plasma cleaning [103] and the deposition of 40 nm of Al in the MBE. The HF dip also removed the SiO_x mask, which simplified the consecutive device fabrication. The removal of SiO_x is important as its presence can cause dielectric losses and limit qubit coherence times. Based on resonator tests made with MBE Al on SiO_x , we extracted an internal quality factor $Q_i \approx 10^3$. Assuming the same value for the qubit island

*InAs on GaAs had also been demonstrated in Ref. [87] but significantly higher losses had been measured on GaAs substrates [28]

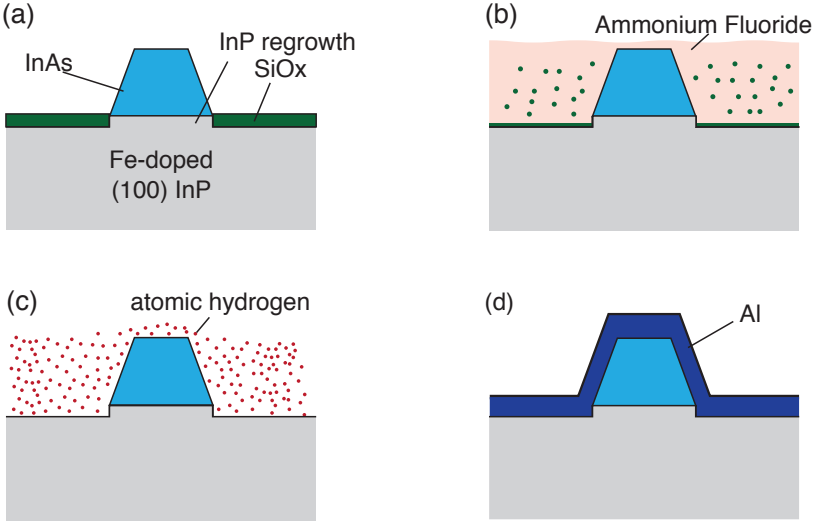


Figure 5.1: First generation InP SAGmon growth sequence. (a) InP and InAs are grown selectively using chemical beam epitaxy. (b) The SiO_x film is removed with ammonium fluoride. (c) The wafer is loaded into the molecular beam epitaxy system and cleaned using hydrogen assisted plasma cleaning before (d) depositing Al in the same system.

capacitor, the coherence time of a qubit with frequency $f_q = 6 \text{ GHz}$ would be limited to $T_1^{\text{diel}} \approx Q_i / (2\pi f_q) \approx 250 \text{ ns}$ [28].

5.1.3 POST-GROWTH FABRICATION

Prior to the qubit device fabrication, the wafer was cleaved into smaller pieces, typically with dimension $10 \text{ mm} \times 9.2 \text{ mm}$. A total of four devices with six gatemones each were made in parallel on these chips. Figure 5.2(a) shows a micrograph of the qubit of one of the finished devices. A close-up up the junction region can be seen in Fig. 5.2(b). The design and fabrication flow were similar to the ones described in Section 4.3, with two minor deviations, introduced to increase the low yield that was caused by poor surface adhesion. First, topgates were evaporated with a 2 nm Ti sticking layer below the 50 nm of Al. Second, the Josephson junction and all other large features

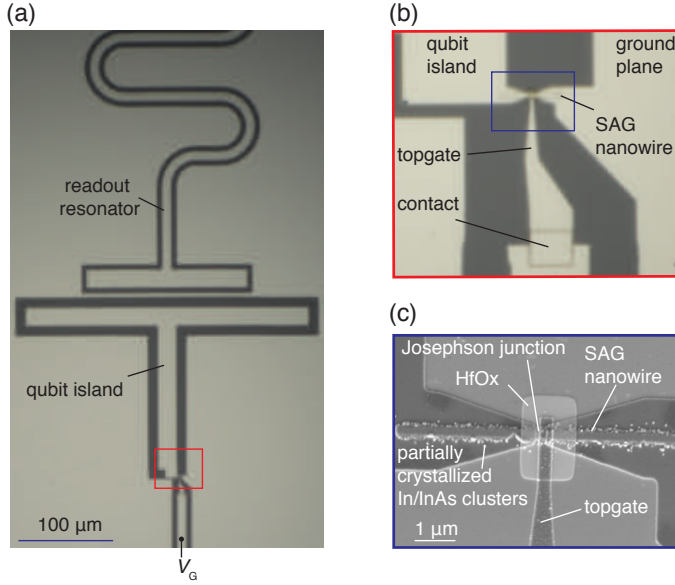


Figure 5.2: First generation InP SAGmon devices. (a) Micrograph of the T-shaped qubit island and the readout resonator. The patterned Al overlayer shows as light grey, with the underlying substrate showing as dark grey. (b) Zoom in on the junction region with the topgate deposited on the Josephson junction. (c) Scanning electron micrograph of the junction region with partially crystallized In/InAs clusters visible near the nanowire. These clusters form when the growth parameters are no within the selectivity window [88].

such as the transmission line, readout resonators, the test resonator and gate lines, were defined in the same etch to reduce the number of fabrication steps. The adhesion problems resulted in an uncontrollable running of the Al etchant, which etched into the ground plane and interrupted the center conductor for some resonators and the transmission line. The etch run was randomly distributed across the device. Although the mechanism that causes the poor adhesion is not understood, the insufficient adhesion could be shown to be correlated to the hydrogen assisted cleaning step preceding the MBE Al deposition. For consecutive growths with a shorter hydrogen assisted cleaning duration, significantly fewer etch runs were observed, which were also

limited to smaller areas. No uncontrolled etch runs were observed for test samples without any hydrogen assisted cleaning, where the etch process between samples was identical. Small grains were present around all nanowires [see Fig. 5.2(c)]. These were likely partially crystallized In/InAs clusters that formed because the material was not grown with process parameters within the selectivity window [88]. This hypothesis is supported by the fact that an optimization of the growth parameters led to a reduced amount of grains until only few or no grains were visible close to the nanowires. A detailed fabrication flow and process parameters can be found in Appendix B.

5.1.4 QUBIT DEVICES

After qubit device fabrication, the devices were bonded up and loaded into the setup as described in Section 4.4. In this section, we will focus on the results for qubit 1 (Q1)[†]. We used the measurement techniques and the setup described in sections 4.7 and 4.8, respectively. Figure 5.3(a) shows a power sweep of the readout resonator with resonance frequency f_r that was coupled to Q1, where zero volts were applied to the qubit Josephson junction. Due to the presence of the qubit the resonator experienced a dispersive shift χ_{01} (see Section 2.4) at low input powers. From the dispersive shift $\chi_{01}/2\pi = g^2/\Delta = -6$ MHz we can estimate the qubit frequency $f_q \approx 8$ GHz, where we used $g/2\pi = 80$ MHz and $\Delta = 2\pi(f_r - f_q)$. Assuming $E_C/h = 230$ MHz (obtained from electrostatic simulations), we estimate Josephson energy $E_J/h \approx 35$ GHz and a critical current $I_C \approx 70$ nA, values comparable to similar devices with VLS nanowires [21]. Figure 5.3(b) shows the transmission coefficient S_{21} near f_r as a function of gate voltage V_G applied to Q1 at a low readout power, where the resonator showed a dispersive shift ($P_{\text{readout}} = -30$ dBm). By applying a negative gate voltage, E_J , and thereby f_q , was reduced. Starting from $f_q > f_r$ at $V_G = 0$ V, the qubit frequency was reduced to $f_q < f_r$ for $V_G < -1.5$ V. An avoided crossing was observed between both regimes for $f_q \approx f_r$ for -1.2 V $< V_G < -1.5$ V. The non-monotonic change in f_r follows the monotonic change in f_q , which is typical for superconductor-semiconductor based junction and has previously been reported in References [21, 26–28, 47, 104]. It can be explained by a non-monotonic function $I_C(V_G)$ due to mesoscopic conductance fluctuations

[†]Resonators of qubits 2, 3 and 4 showed a gate response but could not be measured using two-tone spectroscopy. Qubits 5 and 6 had an interrupted readout resonator due to an etch run such as described in Section 5.1.3

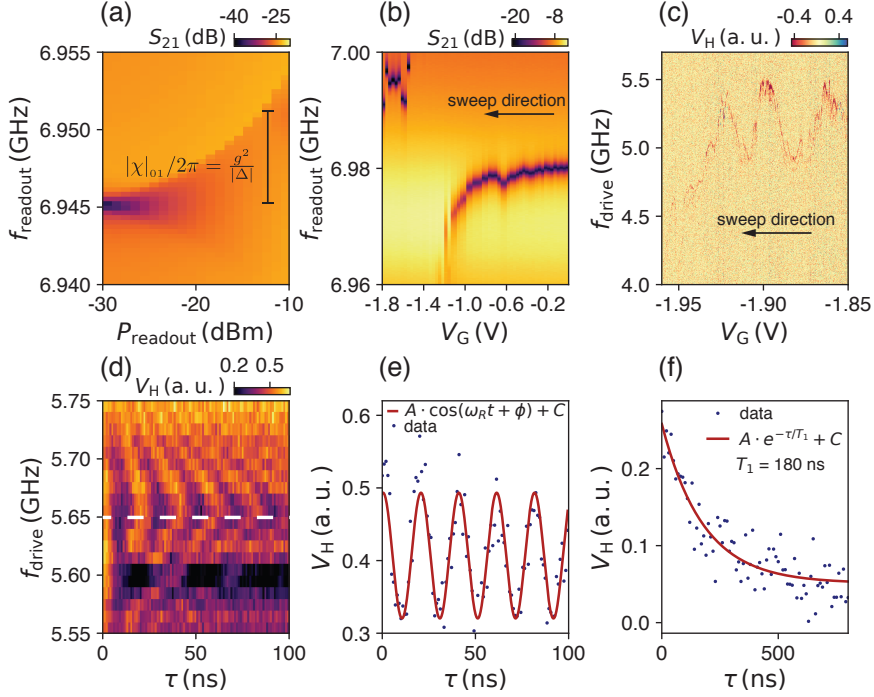


Figure 5.3: InP SAGmon qubit measurements. (a) Transmission amplitude S_{21} as a function of resonator drive frequency f_{readout} and readout power P_{readout} . The resonator shows a dispersive shift χ_{01} at low powers. (b) Transmission amplitude S_{21} as a function of resonator drive frequency f_r and gate voltage V_G with an avoided crossing for $-1.7 \text{ V} \leq V_G \leq -1.2 \text{ V}$. (c) Two-spectroscopy signal of the qubit as function of gate voltage V_G and qubit drive frequency with the average signal amplitude per gate voltage subtracted for each line. The colorbar is chosen such that the signal oversaturates in order to highlight the qubit frequency which is visible in red and shows a non-monotonic behavior and overall decrease as V_G is lowered. (d) Rabi oscillations as a function of drive time and qubit drive frequency. (e) Line cut from (d) for a frequency 5.65 GHz fitted to a sinusoidal oscillation. (f) Lifetime measurement with varying wait time τ between an R_X^π pulse with duration 20 ns and readout. An exponential fit is used to extract the relaxation time $T_1 = 180$ ns.

caused by electrons scattering across the junction. Scattering appears as the mean free path of electrons is typically shorter than the superconducting coherence length in these devices [21]. The qubit frequency was also measured

in the dispersive regime ($|f_r - f_q| \gg g$) with $f_q = 4 - 6 \text{ GHz} < f_r$ using two-tone spectroscopy. Figure 5.3(c) shows resonator transmission amplitude V_H as a function gate voltage and qubit drive frequency, where the observed dip (red color) corresponds to the qubit frequency. The qubit frequency changed non-monotonically as discussed before. Due to the relatively low drive power only one dip corresponding to the $|0\rangle \rightarrow |1\rangle$ transition was measured.

To perform qubit rotations, we fixed the gate voltage at $V_G = -1.838 \text{ V}$ to fix the qubit frequency at $\sim 5.6 \text{ GHz}$. We pulsed the qubit for a variable duration τ to rotate the qubit around the x -axis and read out the amplitude of the readout tone V_H , which reflects the probability of the qubit to be in the $|1\rangle$ state. The measurement of V_H as function of qubit drive frequency and pulse duration is shown in Fig. 5.3(c), where coherent oscillations forming a chevron pattern are observed. Next, we fit to a line cut at $f_{\text{drive}} = 5.65$ [see Fig. 5.3(e)] to extract the duration τ_π of an R_x^π pulse. After some additional readout optimization, the qubit relaxation time $T_1 = 180 \text{ ns}$ was measured. Figure 5.3(f) shows the measurement and the exponential fit that was used to extract T_1 . For this measurement, the qubit in the $|1\rangle$ state using a R_x^π pulse and V_H after a variable wait time τ . Attempts to measure the dephasing time T_2' were unsuccessful.

Instead, we estimate the dephasing time from the power dependence of the line width of the qubit in two-tone spectroscopy. As shown in Fig. 5.4(a) the line width of peak decreases with decreasing drive power. The measured line have a Lorentzian line shape with half width at half maximum δ_{HWHM} [see Fig. 5.4(b)]. Following Ref. [100], we estimate T_2^* from fitting $2\pi\delta_{\text{HWHM}} = 1/T_2^* = (1/T_2^* + n_s\omega_{\text{vac}}^2 T_1/T_2^*)^{1/2}$ to the data as illustrated in Fig. 5.4(c), where we assume $n_s\omega_{\text{vac}}^2 T_1$ to be a power independent prefactor that is proportional to $P_{\text{drive},s}$, the drive power on-chip[‡]. We extract $T_2^* = (7.4 \pm 0.8) \text{ ns}$, which is an order of magnitude lower than T_1 . Due to poor signal-to-noise ratio (SNR) of the signal T_2^* has a large uncertainty. Other measurements with better SNR but higher drive power exist. These were not used to extract T_2^* as the peak is power broadened and no power dependents was measured.

The coherence time is an order of magnitude shorter than state-of-the-art gatemons on InP substrates [28]. The relatively short coherence times could have been caused by a relatively low material quality. Partially crystallized

[‡]We assume $P_{\text{drive},s} = P_{\text{drive}} - 30 \text{ dB}$ to account for used cryogenic attenuators, line line attenuation and filtering.

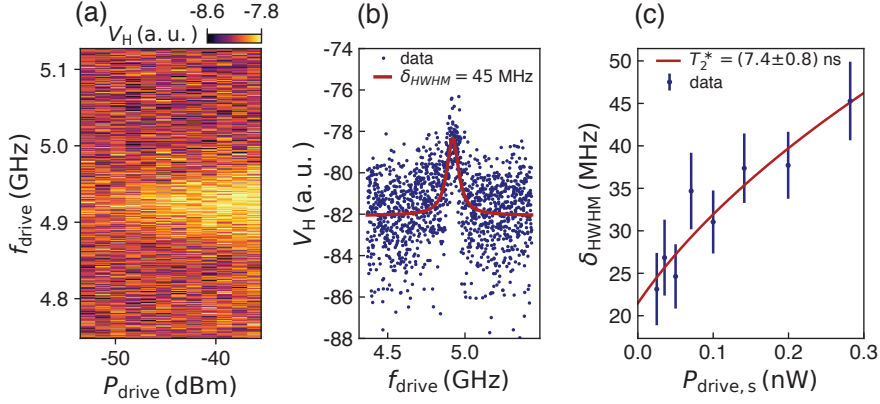


Figure 5.4: nP SAGmon T_2^* measurements. (a) Amplitude of the read out tone V_H as a function of drive frequency f_{drive} and drive power P_{drive} at room temperature. The qubit line width decreases with decreasing drive power. (b) V_H as a function of f_{drive} at $P_{\text{drive}} = -35.5$ dBm with a fit of a Lorentzian line shape to extract the half width at half maximum δ_{HWHM} . (c) Extracted δ_{HWHM} as a function of power at the sample $P_{\text{drive,s}} = P_{\text{drive}} - 30$ dB with a fit $2\pi\delta_{\text{HWHM}} = 1/T_2 = (1/T_2^* + n_s\omega_{\text{vac}}^2 T_1/T_2^*)^{1/2}$.

In/InAs clusters were observed near the nanowire [see Fig. 5.2(c)] and the Al layer was not deposited in-situ. To study the interface quality between Al and InAs we extract the qubit anharmonicity following Ref. [47] and using the theoretical description of an SSmS junction from Section 2.6.

Figure 5.5(a) shows the two-tone spectroscopy signal of Q1 as a function of gate voltage at relatively high qubit drive power, where the two-photon $|0\rangle \rightarrow |2\rangle$ transition became measurable. The peak position $f_{02}/2$ is used to calculate the anharmonicity $\alpha/h = 2(f_{02}/2 - f_{01})$. Here, the frequencies $f_{02}/2$ and f_{01} are extracted by numerically fitting two independent Lorentzian line shapes to the signal and using the position of peak maxima as transition frequencies [see Fig. 5.5(b)]. We calculate the set of channel transmission $\{T_i\}$ for each value of gate voltage using $\Sigma T_i = (hf_{01})^2/(2\Delta E_C)$ as shown in Fig. 5.5(c). Here, we used $\Delta = 190 \mu\text{V}$, a value typically measured for InAs/Al hybrid systems [67, 105]. The value of Δ was not verified and could be smaller. For example, Ref. [67] reports $\Delta \approx 140 \mu\text{V}$ for InAs nanowires with evaporated Al. However, a smaller value of Δ does not change the qualitative statement derived from a comparison of the anharmonicity to model calculations. Assum-

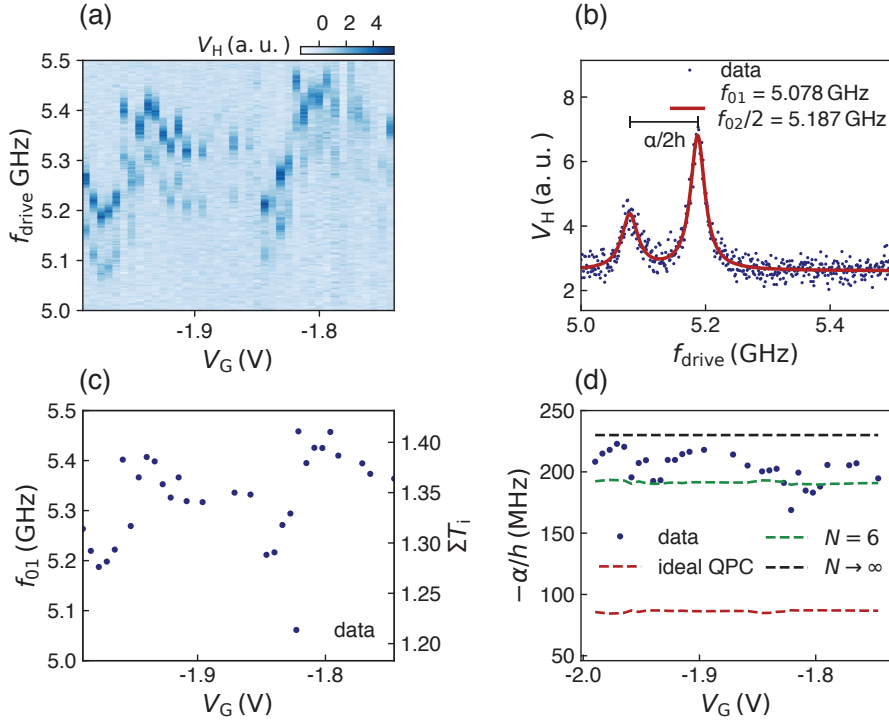


Figure 5.5: Anharmonicity analysis InP SAGmon. (a) Two-tone spectroscopy of Q1 as a function of gate voltage V_G with the transitions f_{01} and $f_{02}/2$ being measured. (b) Example fit of two Lorentzian line shapes to the spectroscopy signal at $V_G = -1.977$ V, giving the anharmonicity $\alpha/h = 2(f_{02}/2 - f_{01})$. (c) Extracted transition frequency f_{01} and sum of transmission channels ΣT_i as a function of gate voltage. (d) Anharmonicity over the entire gate range in (a). The dashed lines indicate the expected anharmonicity for different models as discussed in Ref. [47] - an ideal QPC, six equally transmitting channels ($N = 6$) and the tunneling regime ($N \rightarrow \infty$).

ing N transmitting channels with equal transmission probability T , the model gives $\alpha/h = -E_C[1 - 3E_J/(\Delta N)]$. Figure 5.5(d) shows that the anharmonicity lies between the predicted value for $N = 6$ and $N \rightarrow \infty$. In contrast, an ideal QPC, that is assuming channels are filled in a staircase with at most one partially transmitting channel, would predict an anharmonicity of $-\alpha/h \approx 85$ MHz [see Fig. 5.5(d)]. This indicates that the transparency of the junction was well

below 1. We find an average sum of transmissions $\Sigma T_i \approx 1.35$. Assuming $N = 6$, each channel would have a transmission $T_{\min} = 0.22$, which is a lower estimate the junction transmission. In contrast, studies on gatemons with VLS InAs/Al nanowires with in-situ grown epitaxial Al in Ref. [47] reported $\alpha \approx 100 - 150$ MHz and the presence of 2-3 channels with transparencies up to $T_{\min} \sim 0.9$. DC-transport measurements with state-of-the-art III-V materials report a junction transparency of more than 0.9 [106,107]. The relatively large anharmonicity in our devices is likely related to a relatively poor InAs/Al interface. The poor interface probably originates from the two step growth process that exposes the InAs to air before the Al evaporation. The low transmission probability could also be caused by scattering processes in the junction caused by a poor material quality, meaning that the junction is not in the short junction limit.

5.1.5 DISCUSSION

The extracted relaxation time $T_1 = 180$ ns is significantly lower than lifetimes found in state-of-the-art gatemons built with VLS InAs nanowires on a Si substrate [25,26] or 2DEG on an InP substrate [28] but larger than the coherence times reported for graphene-based gatemons [27] and carbon-nanotubes based gatemons [108]. The coherence times could be limited by loss mechanisms that are related to the material growth process. As discussed above, the relatively large anharmonicity indicates a relatively low junction transparency, probably originating from a low quality Al/InAs interface or a poor semiconductor quality. Disorder at the interface can give rise to subgap states that in turn can couple to the qubit and cause relaxation and decoherence [71]. Further, the presence of parallel conduction channels near the InP/InAs interface in selective-area-grown structures has been reported in Ref. [87]. The authors demonstrated that a GaAs(Sb) buffer can be used to promote elastic relaxation and thus avoid parallel conducting channels and improve transport properties of the nanowire. The regrowth of InP for the material grown in this work does not have the same effect as a GaAs(Sb) buffer since it does not enable strain relaxation. The gatemon could also couple to the partially crystallized In/InAs clusters near the nanowire, which could potentially act as charge traps or normal conducting islands. Further, measurement of quality factor of the test resonator (see Fig. 4.3) indicate a poor substrate surface quality.

The extracted quality factor $Q_{\text{internal}} = 5 \cdot 10^3$ is significantly lower than a quality factor of the order $5 - 6 \cdot 10^4$ that is typically achieved on Fe-doped InP substrates. This can be attributed to the hydrogen assisted plasma cleaning step since resonators with a relatively high internal quality factor ($Q_{\text{internal}} \sim 5 \cdot 10^4$) were made on consecutive growth wafers with shorter cleaning steps.

The origin of the relatively short relaxation time of $T_1 = 180$ ns cannot be answered conclusively without further measurements. However, limits for coherence times associated with the substrate and readout circuitry can be estimated. A test resonator was placed on the device chip to extract dielectric losses [see Fig. 4.3(a)]. To ensure a meaningful mapping of the dielectric losses of this test resonator to the dielectric losses of the qubit capacitor, both structures were designed with the same inner conductor width and gap size. The extracted internal quality factor $Q_i \approx 1.5 \cdot 10^4$ is extracted at low input powers, where dielectric losses are the dominant loss mechanism [109]. This corresponds to a relaxation time of a qubit with $f_q = 5.65$ GHz of $T_1^{\text{diel}} \approx Q/(2\pi f_q) \approx 420$ ns, higher than the measured lifetime of 180 ns. Purcell decay, which is discussed in Section 2.4, can be excluded as dominant loss mechanism since the estimated decay rate is several orders of magnitude smaller than the observed relaxation rate. Using the measured coupling of the readout resonator to the transmission line $Q_{\text{coupling}} = 5 \cdot 10^3$, the decay rate of the resonator can be estimated to be $\kappa = 2\pi f_r/Q_{\text{coupling}} \approx 90$ MHz, giving a Purcell limit $T_1^{\text{Purcell}} = \Delta^2/g^2 \cdot 1/\kappa \approx 13$ μ s. Setup and sample packaging related loss mechanisms are unlikely as longer coherence have been measured for other qubit in the same setup, both before and after the qubit measurements discussed in this section.

The measurements in this section are, to the best of our knowledge, the first demonstration of a gatemon utilizing a selective-area-grown material system. In order to improve the device performance of future devices we decided to change the growth sequence, fabrication scheme and perform a DC-transport characterization of the new material. All of these aspects are summarized in Section 5.2.

5.2 SECOND GENERATION DEVICES

After coherent oscillation were demonstrated with the first generation material, the growth process was changed to improve the material quality. The growth

of a ternary buffer layer between InP and InAs layers as well as the growth of an As-capping layer after the InAs growth were introduced into the process. The pre-growth steps were identical to the ones described in Section 5.1.1.

5.2.1 GROWTH

Figure 5.6 shows a schematic of the growth sequence for the 2nd generation devices. In a first step, 8 nm InP, 16 nm $\text{InP}_{0.7}\text{As}_{0.3}$, 29 nm InAs and an As capping layer were grown. The purpose of the additional buffer was to help bridge the lattice mismatch between InP and InAs, thereby improving the crystal quality of the top InAs layer. The As layer protected the InAs surface between growth steps and was removed in the second growth chamber by thermal annealing at $\sim 800^\circ\text{C}$ and applying an As overpressure. The overpressure was applied to avoid As from the growth layers being evaporated during the annealing step, which would result in defects in the nanowires. In the final step Al is

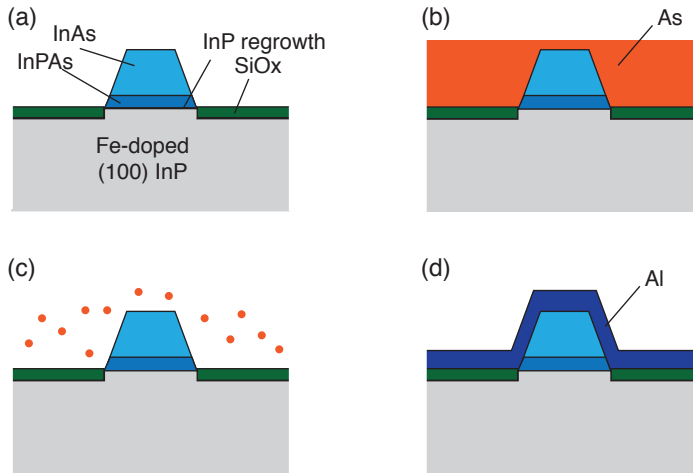


Figure 5.6: Second generation InP SAGmon growth sequence. (a) InP, InPAs and InAs are grown selectively on the substrate using chemical beam epitaxy (CBE). (b) The entire wafer is capped with As before it is taken out of the CBE system. (c) The As-capping is removed inside an molecular beam epitaxy (MBE) growth system using thermal annealing. (d) Al is evaporated on the entire wafer in the MBE system, resulting in SiO_x below the Al.

evaporated.

While this new As capping procedure replaced the hydrogen assisted cleaning step and solved the etching problems associated with it, it required major changes in the device fabrication. Since the As layer was protecting the SiO_x layer, the SiO_x layer was not removed before the Al deposition but selectively etched in the consecutive device fabrication. As discussed in Section 5.1.2, the presence of SiO_x would lead to dielectric losses of qubit capacitor and short qubit coherence times.

5.2.2 DC-TRANSPORT

To characterize the new material system, test devices were made using standard electron beam lithography and etching techniques. These devices were fabricated to test material properties in DC transport that are otherwise inaccessible in cQED measurements – the semiconductor quality of the nanowire and the induced superconducting gap. These DC transport were made on wires with the same dimensions as wires used for gatemon devices.

Figure 5.7(a) shows a scanning electron micrograph of a field-effect transistor device. The growth sequence for this material was stopped after the InAs growth, meaning the wafer was not capped with As and no Al was evaporated. In a first step, the wire was contacted on both ends with Ti/Au (5 nm Ti, 100 nm Au). This step was preceded by RF-milling on the InAs surface to ensure a metallic contact. The gate dielectric that consists of 15 nm HfO_2 was deposited globally by atomic layer deposition. Ti/Au topgates (5 nm Ti, 100 nm Au) were evaporated to tune the $L_{\text{FET}} = 6 \mu\text{m}$ long segment of the nanowire. A detailed fabrication description of the single fabrication steps can be found in Appendix B.

The devices were measured at a temperature of 4 K with the setup that is illustrated in Appendix C. The measurements focused on voltage biased, two-terminal measurements of the differential conductance, dI/dV . The AC voltage output was sourced by a lock-in amplifier to apply a voltage signal with amplitudes $V_{\text{AC}} \sim 100 \mu\text{V}$. On the measurement side, the drain current was converted to a voltage signal using a transimpedance amplifier and dI/dV measured with the lock-in amplifier.

Figure 5.7(b) shows the pinch-off curve of a device with a wire width of 170 nm. The wire pinched off for gate voltages $V_G < 1 \text{ V}$, indicating relatively

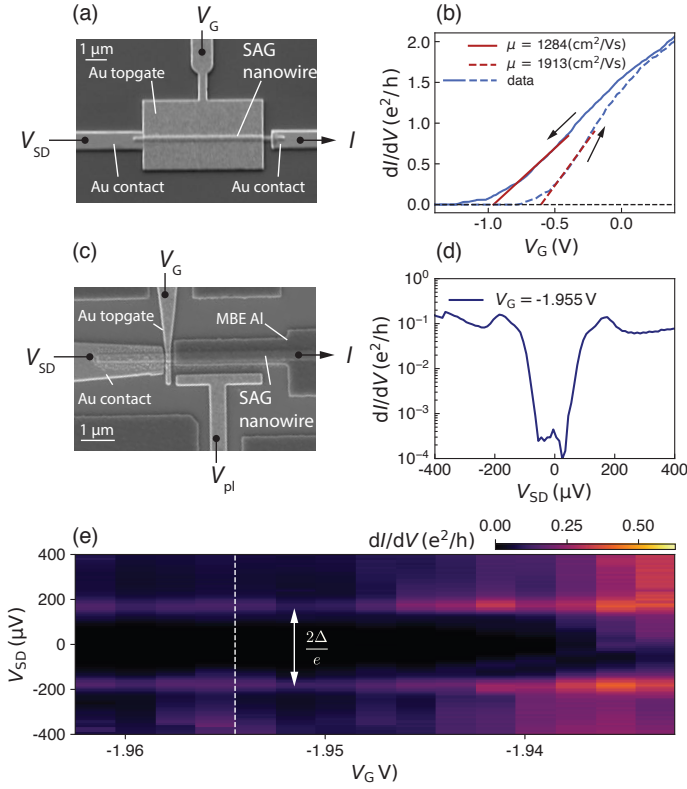


Figure 5.7: Second generation InP SAG DC transport. (a) Scanning electron micrograph of field-effect transistor device used to extract the field-effect mobility μ . (b) Differential conductance dI/dV as a function of topgate voltage V_G of a device similar to the device shown in panel (a). The arrows indicate the gate sweep direction. The fit of the linear region of the pinch-off curve is used to extract μ . (c) Scanning electron micrograph of the device used for NIS tunneling spectroscopy. (d) dI/dV as a function of voltage bias V_{SD} of NIS spectroscopy device in the tunneling regime. dI/dV is proportional to the induced superconducting gap and a line cut from the dataset shown in panel (e) (white line). (e) dI/dV as a function of V_G and V_{SD} .

good interface qualities between InP substrate and buffer as well as buffer an InAs. Pinch-off curves for increased wire widths look similar to the pinch-off curve shown in Fig. 5.7(b). Based on the fit to the linear region of the curves,

we extract the field-effect mobility

$$\mu = \frac{L_{\text{FET}}^2}{C} \frac{dG}{dV_G}, \quad (5.1)$$

where C represents the capacitance between topgate and the InAs transport channel and dG/dV_G is the slope of dI/dV . The capacitances for all wire widths are acquired from electrostatic finite-element simulations as shown in Appendix D. The average field-effect mobility over all five nanowires is $\mu = (1190 \pm 290) \text{ cm}^2/(\text{Vs})$. Here, we extracted mobilities for up and down sweeps and averaged them. This value is lower but comparable to the field-effect mobilities for selective-area-grown nanowires on GaAs with GaAs(Sb) reported in Ref. [87] in the order of $5600 \text{ cm}^2/(\text{Vs})$. This indicates a lower crystal quality of the nanowires in this work since the low-temperature field effect mobility of undoped III-V nanowires is typically limited by crystal defects [79, 82] or surface effects [80, 81]. The transport properties of the material system could potentially be improved by a continued optimization of the growth, in particular the buffer layer.

Based on the relatively high field-effect mobility and the successful pinch-off of the nanowires we proceeded with characterizing the Al/InAs hybrid material after the full growth sequence. Figure 5.7(c) shows a device for NIS spectroscopy that was made on material which was capped with an As layer between growth steps. At the start of the fabrication, the entire chip was covered with a 40 nm thick Al film. First, Al was selectively removed using wet-etch solution (Transene Al Etchant Type D at 50°C) to remove Al from one end of the nanowire [see Fig. 5.7(c)] and remove Al to define a superconducting contact on the other end. Additionally, Al was etched to create openings for ohmic contacts and topgates. In a second step, the nanowire was contacted at the semiconducting end with Ti/Au (5 nm Ti, 100 nm Au), using RF-milling on the InAs surface prior to the metal deposition to ensure an ohmic contact. The Au contacted part of the nanowire (N-region) and the Al covered part of the nanowire (S-region) were separated by a $\sim 200 \text{ nm}$ long segment of bare nanowire (I-region), forming an NIS junction. Next, the gate dielectric consisting of 15 nm HfO_2 was deposited globally using atomic layer deposition. Then, the Ti/Au topgate to control the I-region and a Ti/Au topgate plunger gate were evaporated in lithographically pre-defined regions. The plunger

gate, which could have been deposited to enable tuning of the chemical potential in the nanowire, was not used in the experiments. A detailed description of the single fabrication steps can be found in Appendix B.

The NIS spectroscopy device was measured inside a dilution refrigerator at a temperature $T \sim 30$ mK with the setup illustrated in Appendix C. The measurements focused on voltage biased, two-terminal measurements of differential resistance, dV/dI . The AC voltage output of a lock-in amplifier and DC output of the source meter were combined using a voltage divider that reduced the AC (DC) signal by 10^{-4} (10^{-2}) before being applied to the sample to apply voltages $V_{AC} = 5 - 20 \mu\text{V}$ and $V_{DC} = 0 - 1$ mV at the sample. On the measurement side, the outgoing current was converted to a voltage signal using a transimpedance amplifier and measured with the lock-in amplifier to measure dI/dV .

Figures 5.7(d) and (e) show measurements of the differential conductance as a function of voltage bias V_{SD} , where the semiconductor is depleted to form an insulating barrier. As discussed in Section 3.2.1 the differential resistance is proportional density of states inside the S-region, where the S-region refers to the proximitized InAs layer. Therefore the induced superconducting gap can be estimated from the distance of the coherence peaks to be $\Delta_{\text{InAs}} \approx 180 \mu\text{V}$, which is close to the nominal superconducting gap of bulk Al, $\Delta_{\text{Al}} \approx 200 \mu\text{V}$, indicating a high quality interface. As shown in Figs. 5.7(d) and (e), the subgap conductance is two orders of magnitude smaller than the normal state resistance for gate voltage $V_G < -1.94$ V and was sustained for lower voltages. The presence of the induced hard superconducting gap and the large value of the induced superconducting gap indicate a high interface quality between InAs and Al.

5.2.3 QUBIT DEVICES

The qubits were fabricated using additional steps compared to the qubit fabrication described in Sec. 5.1.3 as the SiO_x layer was removed. A finished device is shown in Fig. 5.8(a). In a first step the global SiO_x layer and Al layers were removed from the chip, except for a small region near each nanowires. First, the Al layer was selectively removed. Then, SiO_x was removed using the same resist stack and reactive-ion etching with process gases CHF_3 and O_2 . To form the qubit islands and resonators, 100 nm thick Al was deposited with

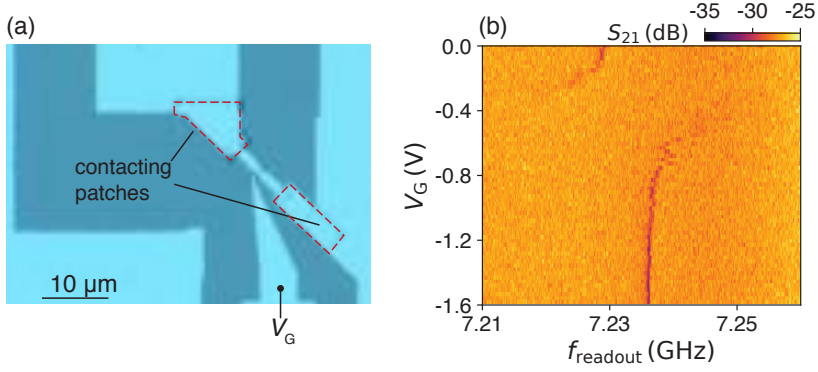


Figure 5.8: Second generation InP SAGmon devices. (a) Optical micrograph of a qubit device with contacting Al patches between the MBE Al and evaporated Al highlighted by red boxes. (b) Avoided crossing visible in the transmission amplitude S_{21} of a readout resonator as a function of readout frequency f_{readout} and applied gate voltage V_G to the junction.

a lift-off process, where the nanowire was protected from the evaporated Al. The transmission line, resonators and qubit island were defined by selectively wet etching Al (Transene Al Etchant type D). In a separate step the Josephson junction was defined by removing a short ($\sim 150 - 200$ nm) segment of Al from the nanowire. This step separation ensured a short junction length and guaranteed a good clearance of large features. The gate dielectric consisted of 20 nm Al_2O_3 deposited by atomic layer deposition in lithographically pre-defined regions. Topgates (50 nm of Al) were evaporated on top of the gate dielectric and used to tune the critical current of the JJs. In a final step, the nanowire was connected to the qubit island on one side and to the ground plane on the other side. A 150 nm thick layer of Al was used for contacting, where evaporation was preceded by RF Ar-milling to remove the native AlO_x on the MBE Al and readout circuitry Al. These contacting patches are highlighted in Fig. 5.8(a).

The devices were loaded in the dilution refrigerator to repeat the measurements performed with the first generation material (see Section 5.1.4). Several devices showed that the gatemon could be controlled by applying a gate voltage to the Josephson junction. An example is shown in Fig. 5.8(b), where the dispersive shift of a readout resonator changes as a function of gate voltage

V_G . An avoided crossing is measured at $V_G \approx -0.4$ V. This kind of measurement could be repeated for many of the fabricated devices but follow-up measurement, such as two-tone spectroscopy measurement and time domain measurements of coherent oscillations, were unsuccessful, suggesting a very short coherence time, even shorter than the coherence times observed for first generation devices. The reasons for the short coherence times are not well understood. They could be related to the sample processing, since additional steps were introduced for device fabrication, which could have reduced the semiconductor quality. The nanowire quality could also have been reduced due to modified growth process. Follow up measurements to test these hypothesis were not performed as the new material platform of selective-area-grown structures on silicon became available. While both, the selective-area-grown structures InP that are discussed in this chapter and selective-area-grown structures on silicon, share many challenges in terms of growth and device fabrication, the Si substrate offers a higher theoretical limit for coherence times due to lower dielectric losses, assuming no other processes limit qubit coherence times. The transport properties of this new material platform are discussed in Chapter 6. Gatemon devices fabricated with it are discussed in Chapter 7.

6

Electrical Properties of Si SAG

In the previous chapter, it was demonstrated that selective-area grown InAs/Al hybrid systems on InP can be used to build gate-voltage-tunable transmons. However, due to the dielectric loss of the substrate, gatemons on InP will inevitably have coherence times which are limited to a few microseconds. In this chapter, we present a novel materials system that uses selective-area grown Al-InAs hybrid structures on a Si substrate and could potentially enable coherence times similar to coherence times observed in state-of-the-art gatemons. We study the electrical properties of this hybrid system with respect to the requirements for gatemon qubits. In particular, disorder both within the semiconductor JJ channel and at the superconductor-semiconductor interface can lead to subgap states that can act as an additional decoherence channel for the qubit.

In order to characterize our system, first we extract mobilities for the semiconductor channel using field effect transistor devices (FETs). Next we probe the superconductor-semiconductor interface quality through transport spectroscopy of normal-conductor-insulator-superconductor (NIS) junctions. Finally, we characterize the quality of JJs in our material system by extracting the $I_C R_N$ product (where I_C and R_N are the JJ critical current and normal state resistance, respectively) and the junction transparency.

6.1 MATERIAL GROWTH

The growth sequence of the material differs from the growth sequences discussed in Chapter 5. Figure 6.1 illustrates the growth sequence for the selective-area grown Al-InAs hybrid structures on a 4° miscut (111) Si substrate with resistivity $\rho > 1 \text{ k}\Omega \cdot \text{cm}$ [Fig. 6.1(a)]. While growth on these substrates needed little optimization, growth attempts on (100) Si lead to discontinuous growth and an overall worse morphology of the grown InAs nanowires. As shown in Fig. 6.1(b), two global buffer layers consisting of $\sim 50 \text{ nm}$ of GaP followed by $\sim 250 \text{ nm}$ of GaAs were commercially grown using metal organic chemical vapor deposition (MOCVD) techniques [110]. These layers were chosen to bridge the lattice mismatch between Si and InAs. The total thickness of these layers was chosen to be relatively thin ($\sim 300 \text{ nm}$) to simplify integration of our superconductor-semiconductor material system with any low loss qubit circuit components that are fabricated directly on the underlying Si substrate. Thin films of AlO_x and SiO_x were deposited on the wafer using atomic layer deposition and plasma-enhanced chemical vapor deposition, respectively [Fig. 6.1(c)]. Openings in these dielectric layers were then defined by standard electron beam lithography and selective etching. First, SiO_x was removed using reactive ion etching (RIE) with process gases CHF_3 and O_2 [see Fig. 6.1(d)]. Then, using SiO_x as etch mask, AlO_x was removed with the TMAH based developer (MF321) as shown in Fig. 6.1(e). The semiconductor heterostructures were then grown selectively in the dielectric openings where the GaAs surface was exposed. Figure 6.1(f) shows a schematic of the full SAG heterostructure, which was designed to improve the overall InAs material quality. First, an Sb-dilute GaAs buffer layer with flat top facets was grown. This layer enables an elastic strain relaxation of the InAs [87] layer. $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ was grown to gradually overcome the lattice mismatch between GaAs and InAs. To help prevent surface damage from subsequent device processing steps, a top barrier layer of $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ was grown on the InAs. Finally, a blanket Al layer was deposited *in situ* to ensure a high quality interface between the Al and the semiconductor heterostructure. Figure 6.2(a) shows a more accurate schematic of the material stack that is modeled after scanning transmission electron micrographs of the material stack shown in Fig. 6.2(b).

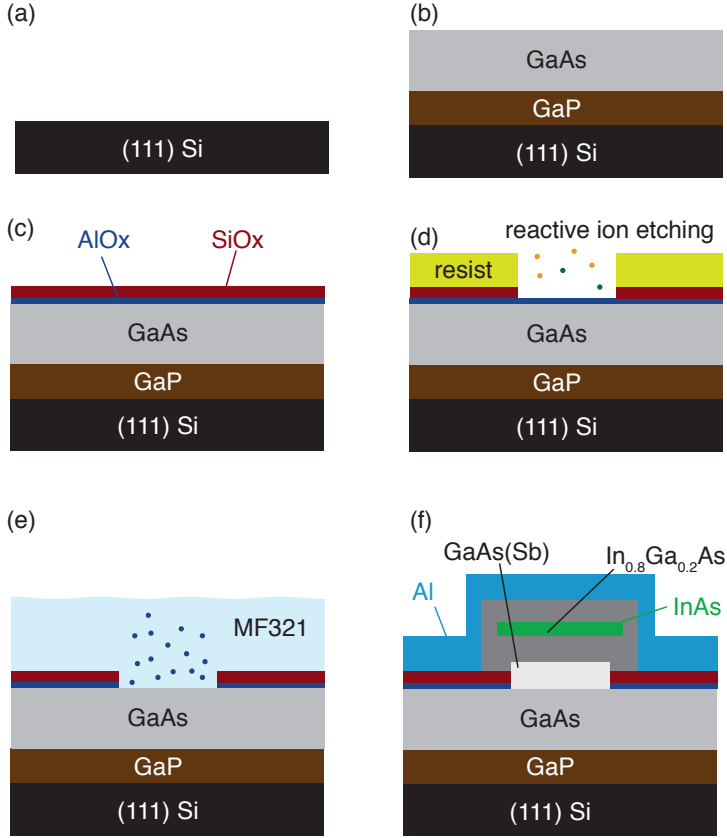


Figure 6.1: Si SAG growth sequence. (a) A 2-inch or 4-inch (111) Si wafer was used as a substrate and (b) 50 nm GaP and 250 nm were grown using metal organic chemical vapor deposition. (c) 5 nm thick AlO_x was deposited using atomic layer deposition, followed by depositing 10 nm thick SiO_x using plasma-enhanced chemical vapor deposition. (d) The growth mask was defined by selectively removing SiO_x using reactive ion etching with the process gases CHF₃ and O₂. (e) AlO_x was selectively etched using an TMAH-based developer (MF321). (f) A GaAs(Sb) buffer, a In_{0.8}Ga_{0.2}As buffer, InAs and an In_{0.8}Ga_{0.2}As top barrier were grown using molecular beam epitaxy. Al was grown globally in-situ.

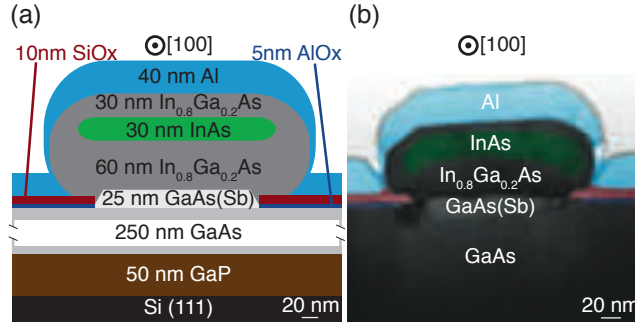


Figure 6.2: Si SAG material stack. (a) Schematic of the material stack. The InAs quantum well (green) is proximitized by the superconducting Al (blue). **(b)** False-colored scanning transmission electron micrograph of the material stack.

6.2 DEVICES

We fabricated three different types of devices to study the properties of our material system: field-effect transistors (FETs), normal-conductor-insulator-superconductor (NIS) junctions and superconductor-semiconductor-superconductor Josephson junctions (S-Sm-S JJ) (Fig. 6.3). NIS and SSmS JJ devices are used to study the superconductor-semiconductor hybrid system. In particular, the induced superconducting gap in the InAs layer is measured with NIS tunneling spectroscopy. The JJ devices are characterized by measurements of the switching current, the $I_C R_N$ -product, the excess current, and multiple Andreev reflections. The NIS and SSmS JJ devices were fabricated in pairs using a single nanowire such that both devices shared a common superconducting segment [Fig. 6.3(b)]. This was achieved by selectively etching the Al layer and depositing a normal-metal contact. The semiconducting segments were tuned by topgates, separated from the nanowire by gate dielectric.

FET devices are used to study the material quality of the conducting InAs layer exclusively. To fabricate these devices we used standard electron beam lithography. In a first step Al was removed from the nanowires by selective wet etching. Subsequently, contacts, gate dielectric, and a topgate were deposited (see Appendix E for additional device fabrication details). The length of the gated channel for all devices shown in this work is $L_{\text{FET}} = 6 \mu\text{m}$. All measurements in this work were performed at millikelvin temperatures unless

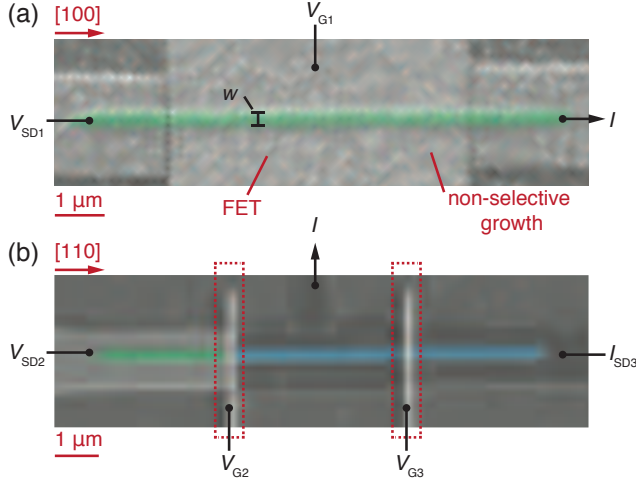


Figure 6.3: Si SAG transport devices. False-colored scanning electron micrographs of the device types measured in this work. False colors indicate nanowire segments with Al removed (green) and segments covered with Al (blue). **(a)** Field-effect transistor (FET) device. **(b)** Combined NIS spectroscopy and SSmS Josephson junction device. The middle segment serves as ground for both NIS spectroscopy and junction measurements. Non-selectively grown material sticks to the dielectric mask during growth and is visible as small grains in both SEMs.

stated otherwise.

6.3 FIELD-EFFECT MEASUREMENTS

A typical figure of merit for the quality of a semiconductor is the field-effect mobility as it is limited by defects in the semiconductor [111]. The field-effect mobility can be extracted from the transconductance dG/dV_{G1} which we obtained from measurements of the differential conductance G as a function of gate voltage V_{G1} for a total of 24 FET devices [similar to the one represented in Fig. 6.3(a)] using standard lock-in techniques. The measured nanowires were grown along the $[100]$, $[110]$ and $[1\bar{1}0]$ directions of the underlying Si substrate (Fig. 6.4 inset).

Figure 6.4 shows typical differential conductance measurements sweeping V_{G1} in both positive and negative directions. Nanowires for all different

orientations could be fully pinched-off and showed a small hysteresis of about ~ 0.05 V, indicating high-quality interfaces between the electrically active InAs channel and adjacent layers [87]. As depicted in Fig. 6.4, the mean field effect mobility μ is extracted from a fit to the linear region of the conductance with

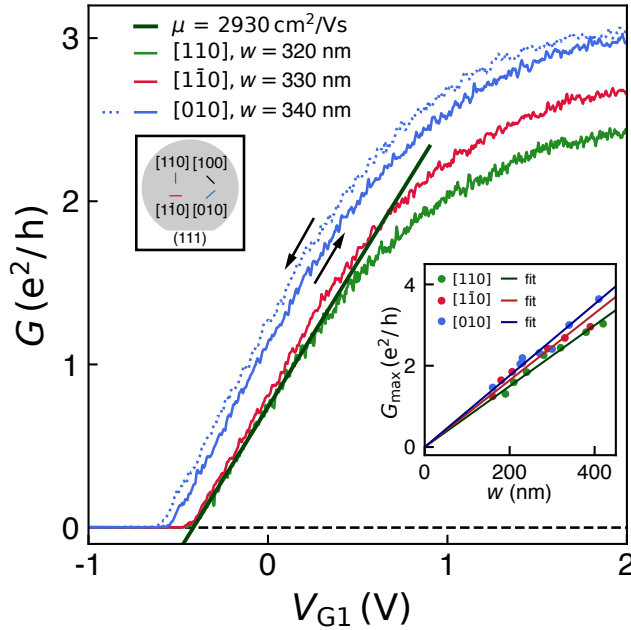


Figure 6.4: Si SAG FET data. Differential conductance G as a function of the gate voltage V_{G1} of an up- and down sweep of a single nanowire (blue) and up sweeps of two nanowires with a different orientation and similar width w . A fit to the linear region of the green pinch-off curves is added to the fit and used to determine the field-effect mobility according to Eq. 1. **Upper left inset:** schematic showing orientation of nanowires relative to the major flat of the Si-substrate. **Lower right inset:** conductance in the fully open regime as a function of w . Solid lines indicate fits of the form $G_{\max} = g' \cdot w$, where g' is the conductance per unit width of the nanowires in the fully opened regime. A line resistance of $R_{\text{line}} = 4.9 \text{ k}\Omega$ has been subtracted from all data shown in this figure.

the highest slope [74]. It can be estimated by

$$\left. \frac{dG}{dV_{G1}} \right|_{\max} = \frac{\mu C_G}{L_{\text{FET}}^2}, \quad (6.1)$$

where $L_{\text{FET}} = 6 \mu\text{m}$ is the length of the gated channel and C_G is the gate capacitance that is estimated from finite-element simulations (see Appendix D). The extracted mean value for all devices is $\mu_{\text{mean}} = (3200 \pm 300) \text{cm}^2/\text{Vs}$. Here, the uncertainty of the simulated capacitance is neglected and the given error is the statistical error of all measured devices, where up- and down sweeps of the same device were considered to be two independent measurements. The value μ_{mean} is comparable but lower than values reported for InAs nanowires grown directly on GaAs [87] and InAs VLS-nanowires that are grown strain-relaxation-free [79, 80]. Previous work has shown that the low-temperature field effect mobility of undoped III-V nanowires is typically limited by crystal defects [79, 81, 82] or surface effects [80, 81]. Further work would be needed to understand the dominant electron scattering mechanism in our material stack in order to further optimize the field-effect mobility. Based on the threshold voltages V_{th} and the volume of the conducting channel v_{ch} (Fig. 6.2) we estimate a mean carrier density at zero gate voltage using $n = C_G V_{\text{th}} / (e v_{\text{ch}})$. For the different nanowire orientations, we estimate $n_{[0\bar{1}0]} = 2.95 \cdot 10^{17} \text{cm}^{-3}$, $n_{[100]} = 3.35 \cdot 10^{17} \text{cm}^{-3}$, and $n_{[010]} = 4.79 \cdot 10^{17} \text{cm}^{-3}$. Nanowires along the [010] direction exhibit the highest charge carrier density (lowest V_{th}) and the highest conductance when the conducting channel is fully opened (for gate voltages $V_G > 2 \text{V}$) (Fig. 6.4, lower inset).

6.4 INDUCED SUPERCONDUCTING GAP

To study the interface quality between the superconducting Al and InAs and the induced superconducting gap Δ^* in the InAs, we used the NIS device introduced previously in Fig. 6.3(a) and fabricated on nanowire A. The device was measured with standard lock-in techniques with unused contacts left floating so the third segment on the nanowire did not affect the measurement. As shown in Fig. 6.5(a), we depleted the bare InAs segment by applying a negative gate voltage V_{G2} to create a tunnel barrier and measured the differential conductance G of the device as a function of voltage bias V_{SD2} . Figure 6.5(b)

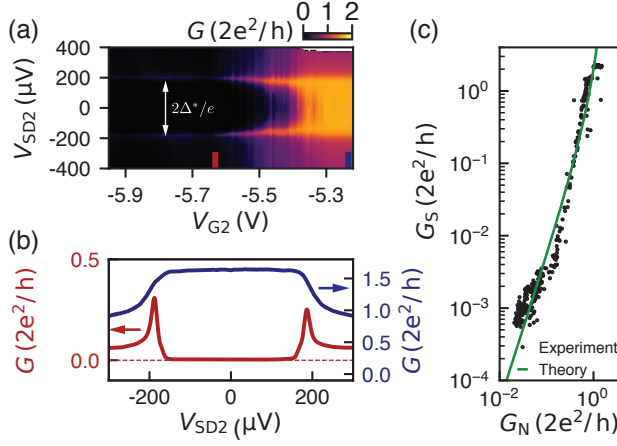


Figure 6.5: Si SAG NIS spectroscopy data. (a) Differential conductance dI/dV of nanowire A as a function of gate voltage V_{G2} and source-drain voltage V_{sd} . (b) Vertical cuts in the tunneling regime (red) and open regime (blue) at the positions indicated by the colored rectangles in (a). The induced superconducting gap $\Delta^* \approx 190 \mu\text{eV}$ is estimated from the peak-to-peak distance in the tunneling regime. (c) Averaged differential conductance at zero source-drain voltage G_S versus averaged differential conductance at finite source-drain voltage G_N ($V_{SD2} = -0.53 \text{ mV}$). The green line is the theoretically predicted conductance in an Andreev enhanced QPC with no fitting parameters (Eq. 2).

(red curve) shows a measurement of an induced hard superconducting gap in the proximitized InAs with the conductance strongly suppressed between two symmetric peaks at $|V_{SD2}| \approx \Delta^*/e$ [67]. In this configuration the differential resistance is proportional to the superconducting density of states in the InAs and the induced superconducting gap $\Delta^* \approx 190 \mu\text{eV}$ is estimated from the peak positions. At higher V_{G2} (more open barrier) the conductance at zero source-drain bias G_S is increased compared to the normal-state conductance G_N for $|V_{SD2}| \gtrsim 200 \mu\text{eV}$ (Figure 6.5(b), blue curve). Both observations, suppressed and enhanced zero-bias-conductance, can be explained in the framework of the BTK theory [50]. This theory describes the charge transfer through an NS interface by Andreev reflection using a single parameter, the dimensionless barrier parameter Z . The limit $Z = 0$ corresponds to a perfect interface where $G_S = 2G_N$ is expected as every charge carrier is Andreev reflected at the in-

interface. The limit $Z \rightarrow \infty$ corresponds to a perfect tunnel barrier where the conductance is directly proportional to the density of states in the proximitized region. Thus, changing V_{G2} in the experiment corresponds to modifying the Z -parameter. To further study the transport across the NS interface we compare the experiment to

$$G_S = 2G_0 \frac{G_N^2}{(2G_0 - G_N)^2}, \quad (6.2)$$

the theoretical prediction for a quantum point contact (QPC) with a single perfectly transmitting channel that correlates G_S to G_N [112] without any free parameters. The measurement was repeated on the same nanowire using a DC setup to measure small differential conductance values ($G_S < 10^{-2} e^2/h$). Here, the differential resistance is obtained from calculating the numerical derivative of the DC data. The result is shown in the Supplemental Material (Fig. F.1) and used to construct Fig. 6.5(c). The experimental data follows the theoretical prediction [green line in Fig. 6.5(c)]. We therefore conclude the presence of an induced hard superconducting gap in the InAs. The small deviation could be the manifestation of a non-zero normal scattering probability or the presence of a multiple of conducting channels with transmission probability below 1. The presence of multiple conducting channels is evident in the plateau region [see Fig. F.1(d)] with enhanced zero-bias conductance, G_N ($V_{G2} > -5.3$ V) in Fig. 6.5(a), that is not quantized at $2 \cdot e^2/h$, contrary to the expectations for a single perfectly transmitting channel.

6.5 NANOWIRE JOSEPHSON JUNCTIONS

We use the SSmS JJ device [Fig. 6.3(b)] to study the Josephson junction formed in the material system. We characterize the junction extracting several junction parameters, the switching current, I_{Sw} , the retrapping current, I_R , the excess current I_{exc} , the normal state resistance R_N and the superconducting gap Δ as a function of gate voltage V_{G3} and temperature T . All parameters are extracted as shown in Fig. 6.6(a) for a typical IV-curve. The junction switches to a dissipative state at switching current I_{Sw} as the bias current, I_{SD3} , is swept from zero. Sweeping I_{SD3} back towards zero, the junction switches back to the superconducting state at the retrapping current, I_R , visible as hysteretic behavior (Fig. 6.6(a), inset). The normal state resistance, R_N , and excess current,

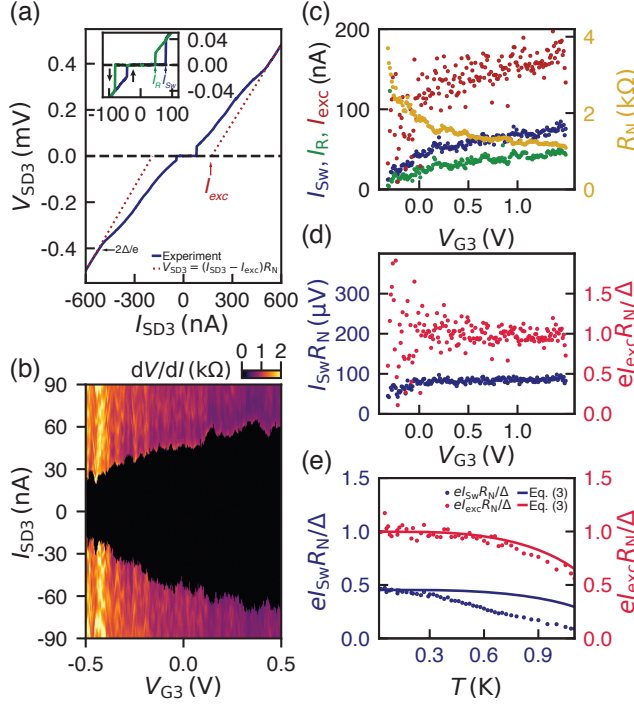


Figure 6.6: Si SAG Josephson junction data. (a) Measured voltage drop across the Josephson junction V_{SD3} as a function of applied current I_{SD3} for $V_{G3} = 1.5$ V for nanowire C. The normal state resistance R_N and excess current I_{exc} are extracted by fitting to the normal state for voltages $V_{SD3} > 2\Delta/e$. From these measurements we estimate $\Delta \approx 200 \mu\text{eV}$ at $T = 20$ mK. The inset shows the region around the superconducting plateau with an up- and down sweep of the current bias. The position of the switching current I_{SW} and retrapping current I_R are indicated by arrows. (b) Differential resistance dV/dI as a function of applied current I_{SD3} and gate voltage V_{G3} at $T = 20$ mK for nanowire C. (c) Extracted values for the R_N , I_{exc} , I_{SW} and I_R extracted for nanowire B from the dataset show in Appendix F. (d) The $I_{SW} R_N$ product and excess current I_{exc} multiplied by the ratio $e R_N / \Delta$ for $\Delta = 200 \mu\text{eV}$ extracted from (c). (e) $e I_{exc} R_N / \Delta$ and $I_{SW} R_N / \Delta$ as a function of temperature T calculated from data shown in Appendix [see Fig. F.2]. Solid lines indicate the temperature dependence expected from BCS interpolation (Eq. 3)

I_{exc} , are extracted at high current bias where $V_{SD3} > 2\Delta/e$, and the junction is driven into the normal conducting state. We estimate the superconducting

gap, $\Delta \approx 200 \mu\text{eV}$, from the visible transition to the normal conducting state. This value is similar to the estimated induced superconducting gap of the SIN device, $\Delta^* \approx 190 \mu\text{eV}$. The critical current is gate tunable as demonstrated by Fig. 6.6(b), where the differential resistance dV/dI is shown as a function of applied current I_{SD3} and gate voltage V_{G3} . Furthermore, IV curves exhibit subgap features in the resistive state for $V_{\text{SD3}} < 2\Delta/e$ that result from multiple Andreev reflections (MARs) [51, 113], discussed in the next section. Figure 6.6(c) shows the extracted junction parameters for nanowire B over a wide gate range from $V_{\text{G3}} = -0.3 \text{ V}$, where the nanowire junction is almost closed ($I_{\text{Sw}} \approx 0$), to $V_{\text{G3}} = 1.5 \text{ V}$, where the junction is fully opened. While $I_{\text{Sw}}/I_{\text{R}} \approx 1$ in the closed regime, we find ratios $I_{\text{Sw}}/I_{\text{R}} \approx 2$ for gate voltages around $V_{\text{G3}} = 1.5 \text{ V}$, indicating that the nanowire junction is underdamped [29].

To further characterize the JJ and its superconductor-semiconductor interface quality, we calculate the product $I_{\text{Sw}}R_{\text{N}}$ and the normalized excess current $eI_{\text{exc}}R_{\text{N}}/\Delta$ [62] [Fig. 6.6(d)]. Here, we use $I_{\text{Sw}}R_{\text{N}}$ as a proxy for $I_{\text{C}}R_{\text{N}}$, noting that the measured switching current can be smaller than the actual critical current of the junction due to premature switching [29] or coupling to the electromagnetic environment [114]. The normalized excess current $eI_{\text{exc}}R_{\text{N}}/\Delta$ is used to estimate the BTK barrier parameter Z for NS interface scattering [50] and is connected to the interface transparency $\mathcal{T} = (1 + Z^2)^{-1}$. Hence, a high value of the junction transparency is an indication of a high superconductor-semiconductor interface quality. For $V_{\text{G3}} > 0.1 \text{ V}$ we extract an averaged excess current $eI_{\text{exc}}R_{\text{N}}/\Delta = 0.99 \pm 0.15$ and estimate $Z = 0.58 \pm 0.06$ [62], leading to $\mathcal{T} = 0.75 \pm 0.04$. A high transparency is consistent with the enhanced zero bias conductance observed with tunneling spectroscopy and with the relatively high value of the induced superconducting gap in the InAs compared to the Al gap [50, 51]. For $V_{\text{G3}} < 0 \text{ V}$, $I_{\text{Sw}}R_{\text{N}}$ is reduced and the spread in $eI_{\text{exc}}R_{\text{N}}/\Delta$ increases. For $V_{\text{G3}} < -0.35 \text{ V}$ negative and positive values for I_{exc} are extracted. Similar observations have previously been explained by quantum dots forming in the junction, which makes the transport dominated by an interplay between superconductivity and Coulomb interactions [115, 116]. The extracted average value $I_{\text{Sw}}R_{\text{N}} = (83.3 \pm 5.8) \mu\text{V}$ is significantly smaller than the theoretical value for a short diffusive junction $2.07\Delta/e$ [61] but in good agreement with values previously measured in Al-InAs-VLS nanowires [111, 117–119] and other superconductor-semiconductor hybrid systems [114, 120, 121]. Similar to previous studies, the origin of a low $I_{\text{Sw}}R_{\text{N}}$ product in these structures is

not well understood due to an insufficient understanding of electrodynamics and dissipation mechanisms in these junctions [33].

Next we focus on the temperature dependence of junction parameters. Figure 6.6(e) shows $eI_{\text{Sw}}R_{\text{N}}$ and $eI_{\text{exc}}R_{\text{N}}$, both normalized by the gap Δ extracted at base temperature, as a function of temperature for nanowire B at a fixed gate voltage $V_{\text{G3}} = 1.5 \text{ V}$. The temperature dependence of the superconducting gap $\Delta(T)$ according to the BCS theory is also plotted against the experimental data, using the interpolation formula [97]:

$$\Delta(T) = \Delta \tanh \left(1.74 \sqrt{\frac{\Delta}{1.76k_{\text{B}}T} - 1} \right), \quad (6.3)$$

where we take $\Delta = 200 \mu\text{eV}$ extracted at $T = 20 \text{ mK}$. The good agreement for the excess current over the entire temperature range suggests that I_{exc} is dominated by Andreev reflection at the SN interfaces, as has previously been observed for VLS InAs nanowires [117]. Similarly, we would expect the temperature dependence of $I_{\text{Sw}}R_{\text{N}}$ to follow the temperature dependence of the superconducting gap given that we estimate the junction to be in the short diffusive limit, $l_e \ll L \ll \xi_{\text{diff}}$, where l_e is mean free electron path and ξ_{diff} is the superconductor coherence length, see Appendix B [33]. The stronger reduction with temperature is qualitatively consistent with predictions for long diffusive SSmS junctions ($\xi_{\text{diff}} \ll L$) [122, 123], although similar behavior has been reported before for InAs-based JJs with comparable lengths, critical currents, and mean free paths [117, 124].

6.6 MULTIPLE ANDREEV REFLECTIONS

Further evidence of a high overall junction transparency are multiple Andreev reflections (MARs), observed as subgap features in the IV curves. In highly transparent semiconducting junctions with a few conducting channels, MAR features are expected to be visible as peaks in the differential resistance [125–127]. Figure 6.7(a) shows the differential resistance averaged over a gate range $1.3 \text{ V} < V_{\text{G3}} < 1.5 \text{ V}$ as a function of the voltage across the junction, V_{SD3} , for nanowire C. The peaks are expected at voltage drops $eV_{\text{m}} = 2\Delta/m$, where m denotes the MAR order. The vertical lines in Fig. 6.7(a) indicate the peaks position and their corresponding MAR order m . From a fit to the extracted

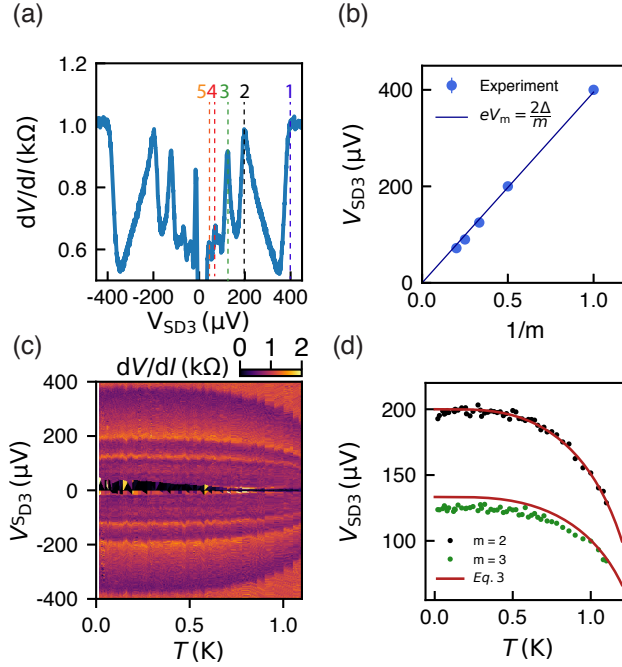


Figure 6.7: Si SAG multiple Andreev reflection data. (a) Averaged differential resistance for $1.3\text{ V} < V_{G2} < 1.5\text{ V}$. Visible MAR peak positions for orders $m = 1 - 5$ are indicated by vertical dotted lines for nanowire C. (b) Fit to the MAR peak position yielding a superconducting gap $\Delta \approx 200\text{ }\mu\text{eV}$. (c) Differential resistance dV/dI as a function of measured voltage drop across the Josephson junction V_{sd} and sample temperature T . (d) MAR peaks for $m = 2, 3$ as a function of temperature. Red lines indicated the expected MAR peak positions based $\Delta(T)$ (Eq. 3) with $\Delta = 200\text{ }\mu\text{eV}$

MAR positions, we obtain a superconducting gap $\Delta \approx 200\text{ }\mu\text{eV}$ [Fig. 6.7(b)]. This value is in good agreement with the gap we estimate from the transition to the normal conducting state (Fig. 6.6a).

We plot the temperature dependence of the differential resistance in Fig. 6.7(c) to confirm the superconducting nature of the MAR features. The MAR peak positions are extracted and separately plotted in Fig. 6.7(d) for $m = 2, 3$. The red lines show the predicted MAR position for a BCS like gap (Eq. 3). The experimental data shows good agreement with BCS theory for $m = 2$. In the case $m = 3$, the data lie systematically below the predicted position over

the entire temperature range. Similar results have been obtained in other superconductor-semiconductor structures [126, 128]. The experimental data can potentially be better described by modeling the temperature dependence of the induced superconducting gap quantitatively as in Ref. [126].

6.7 DISCUSSION AND CONCLUSIONS

We have characterized the different electrical properties of a novel superconductor-semiconductor materials system that uses selective-area grown InAs with epitaxial Al on a silicon substrate. We find field effect mobilities for the InAs channel are lower but comparable with VLS-nanowires, with the crucial advantage that the selective-area grown structures are readily scalable. We find a high quality interface between the Al and InAs as evidenced by an induced hard superconducting gap, high transparency of Josephson junctions and signatures of multiple Andreev reflections. Josephson junction exhibit a gate tunable switching current with an $I_C R_N$ product lower than the superconducting gap of the Al but comparable to Josephson junctions fabricated from other superconductor-semiconductor structures. The reduced $I_C R_N$ -product in this system and similar systems is currently not well understood.

Our material system is a promising platform for scalable and high coherence gatemon devices. The hard superconducting gap and high junction transparency indicate the absence of disorder-related subgap states that can cause decoherence. The gate-tunable critical current of ~ 50 nA is sufficiently high to make gatemons with qubit frequencies up to around 6 – 8 GHz for typical charging energies $E_C/h \sim 200 - 300$ MHz. The gatemon JJs could be fabricated on small mesa structures of the Al/III-V stack while low loss qubit capacitors and other readout and control components could be fabricated directly on the high resistivity silicon substrate. Moreover, with further improvement, this materials systems may also be suitable for other hybrid qubits, including protected superconducting qubits [129] and topological qubits [130].

7

The Si SAGmon

In the previous chapter, we discussed the DC properties of the selective-area-grown Al/InAs material system on Si and concluded that the system is a promising candidate for building gatemons. This chapter discusses the RF properties of the system and describes the gatemon fabrication. Coherent oscillations and gatemon coherence times of $T_1 \approx 500$ ns and $T_2^* \approx 20$ ns are measured. Section 7.1 presents the RF properties of the material which are investigated using secondary ion mass spectroscopy and resonator tests. Qubit device fabrication and design are discussed in Section 7.2. Section 7.3 presents qubit measurements, where Section 7.3.1 examines the improvement between consecutive device iterations, Section 7.3.2 discusses the qubit anharmonicity and Section 7.3.3 shows coherent oscillations and coherence times measurements.

7.1 RF MATERIAL PROPERTIES

Building gatemon qubits based on selective-area-grown structures on Si will potentially be advantageous compared to selective-area-grown structures on InP due to the low dielectric loss tangent of the underlying Si substrate, which, in principle, enables the fabrication of superconducting resonators with internal quality factors in the order of a million. The fabrication of high-quality

readout resonators and the integration the Josephson junction (JJ) into the superconducting circuit are discussed in this section.

It was found, that it is not sufficient to remove the buffer and consecutively pattern the resonator structures on top of the Si substrate to make high-quality resonators with the material system. Instead, ~ 250 nm of the top Si must be removed prior to device fabrication to achieve internal quality factors $Q_i \geq 10^6$. This result can be correlated to the P concentration in the Si, which was measured using secondary ion beam spectrometry (SIMS). Figure 7.1(a) illustrates the principle of SIMS, where a substrate surface is sputtered with a focused primary ion beam and the ejected secondary ions are collected and analyzed. The result is illustrated in Fig. 7.1(b) for the elements Si, P and Ga. Based on scanning transmission electron data micrographs, the GaP stack has a thickness of ~ 50 nm, but a significant P concentration is also measured in the top 250 nm of the Si substrate. Additionally, the Ga concentration increases in the top layer of the Si substrate. Both, the measured P and Ga concentration, are likely the result of thermal diffusion as the Si wafer is heated to 600°C during the selective area growth step and during the GaP/GaAs growth, where the temperature is unknown*. To acquire the SIMS data in Fig. 7.1(a) the material was sputtered from the wafer backside [see Fig. 7.1(b)] reducing the effect background concentrations of residual P and Ga ions.

To test the effect of the dopants on the RF properties of the Si, we performed resonator tests, where we used the internal quality factor Q_i as figure of merit. The resonators were fabricated on the substrate after globally removing the GaP/GaAs layer and removing some Si by reactive ion etching (RIE) with process gases Cl_2 and N_2 . From etch tests, we estimate an etch rate of (75 ± 25) nm/min of Si and an etch time of ~ 1 min being necessary to remove the GaAs/GaP stack. To make the resonators, the device chips were dipped into ammonium fluoride for 10 s before Al was evaporated. The resonators were defined by selectively etching Al using Al Etchant Transene D at 50°C . Figure 7.1(c) shows the internal quality factors Q_i as function of average photon number $\langle n_{\text{np}} \rangle$ in the resonator for different etch depths. To calculate $\langle n_{\text{np}} \rangle$ and extract both the external quality factor Q_{ext} and Q_i , we used the fit procedure described in Ref. [132]. An example fit for resonator made after etching 275 nm of Si is shown in Fig. 7.1(d).

*It is a trade secret of the company [131], which grows the GaP/GaAs buffer using metal-organic vapor phase epitaxy [110].

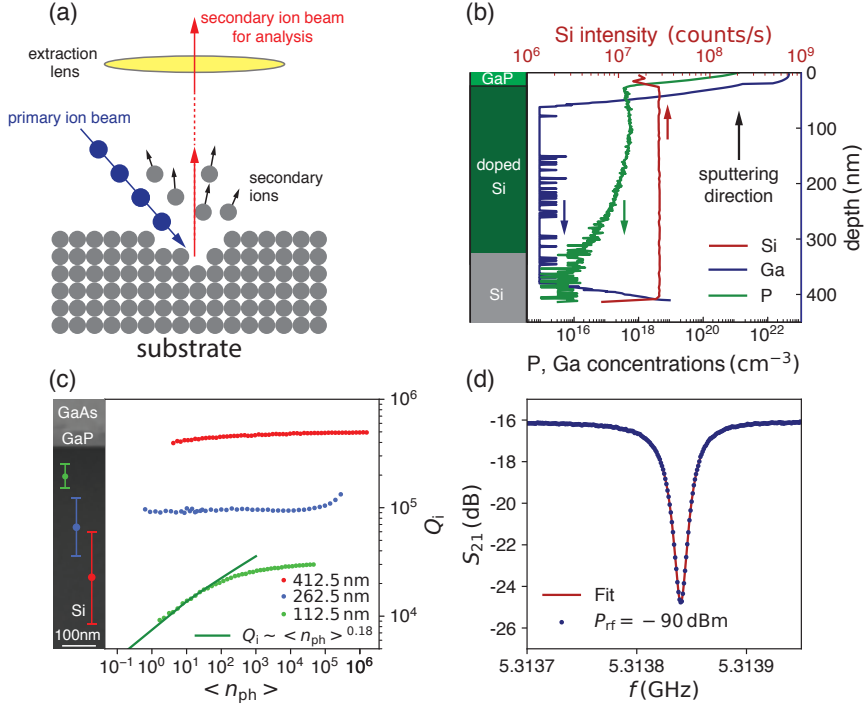


Figure 7.1: RF properties of Si SAG material. (a) Schematic showing the principle of ion mass spectrometry (SIMS) which is used to measure the concentration of Ga and P in the Si substrate. The sample surface is sputtered with a focused primary ion beam and the ejected secondary ions are collected and analyzed. (b) Measured concentration of P and Ga as a function of sputtering depth as well as Si intensity. A schematic material stack are aligned to the graph. A significant P concentration is measured in the top 200 – 300 nm of Si. (c) Internal quality factor Q_i as a function of average photon number $\langle n_{ph} \rangle$ for different etch depths indicated in the material stack on the left, which was measured using a scanning transmission electron microscope (STEM). The error bars correspond to the uncertainty of the etch rate. Q_i increases with etch depth. For etch depth 112.5 nm, a fit of the form $Q_i = A \cdot \langle n_{ph} \rangle^\gamma + C$ is added to the low photon number regime, yielding $\gamma = 0.18$, where $\gamma = 0.5$ would be expected if two-level systems were the dominant loss channel. (d) Example fit of a resonator dip with etch depth 275 nm at drive power $P_{rf} = -90$ dBm ($\langle n_{ph} \rangle \approx 4400$).

As shown in Fig. 7.1(c), the extracted Q_i increases for deeper etches. To ensure reliable fit values, Q_i was extracted from test resonators with $Q_i \approx Q_{\text{ext}}$ as the fit yields an inaccurate value for Q_i in the limit $Q_{\text{ext}} \ll Q_{\text{int}}^{\dagger}$. The Q_i for etch depths 112.5 nm and 262.5 nm was extracted from resonators with resonance frequencies $f_r \approx 7.1$ GHz with $Q_{\text{ext}} \approx 1.5 \cdot 10^4$. The Q_i for etch depths 412.5 nm was extracted from a resonator with resonance frequencies $f_r \approx 5.3$ GHz and $Q_{\text{ext}} \approx 2.8 \cdot 10^5$. To analyze the loss mechanism for these resonators, we investigate Q_i at low power P_{rf} (low $\langle n_{\text{np}} \rangle$). For losses generated by two level systems (TLS) [133], Q_i is expected to increase proportional to $P^{1/2}$ ($\langle n_{\text{np}} \rangle^{1/2}$). TLS saturate with increasing powers [109] and Q_i becomes power independent until the resonator becomes non-linear [134]. TLS could be generated when P is diffusing into the Si substrate. We extract $\langle n_{\text{np}} \rangle^{0.18}$ for an etch depth 112.5 nm and see a much weaker increase in Q_i for deeper etches. Deviations from have also been observed in Ref. [135, 136]. These observations have been explained by TLS interactions [137] and other loss mechanisms such as equilibrium quasiparticles and quasiparticles generated by infrared radiation [138].

In principle, a sufficiently high dopant concentration could create well-defined single electron islands that conduct at low temperatures, known is metal-insulator transition(MIT) [139]. For P dopants in silicon the transition occurs at a concentration $n \gtrsim 3.74 \cdot 10^{18} \text{ cm}^{-3}$, which is an order of magnitude larger than the measured concentration of $n \approx 4 \cdot 10^{17} \text{ cm}^{-3}$ in the top 200 nm of the Si. The surface conductance of the Si wafer has not been probed using DC transport after the III-V. In the existing SIMS data, only few measurements were taken close to the GaP/Si interface, leading to an uncertainty about the Ga and P concentrations and about the precise position of the Si surface. Follow up DC and/or SIMS measurements would be needed to test whether a metal-insulator occurs close to the GaP/Si interface.

Based on the resonator test results, we continued with the fabrication of gatemons devices since the relative high quality factors ($Q_i > 10^6$), enable gatemons with a coherence time well above $1 \mu\text{s}$, when ignoring other decoherence sources. Gatemon qubits are made using Josephson junctions on small isolated regions with the full buffer and Al/InAs stack (mesa), which are

[†]To be more precise, in the fit routine Q_i is inferred from other fit parameters, Q_{ext} the loaded quality factor $Q_i^{-1} = Q_{\text{ext}}^{-1} + Q_i^{-1}$ [132]. If $Q_{\text{ext}} \ll Q_i$, then $Q_i \approx Q_{\text{ext}}$, and the fit yields similar results for a relatively wide range of Q_i values.

created by etching the material around the mesa. The low loss qubit capacitors and other readout control components are made directly on Si and both parts of the circuit are connected in a final lithography step.

7.2 DEVICE FABRICATION

Gatemon devices were fabricated using a design similar to the one described in Section 4.3, with the difference that nanowires are positioned on mesas while the rest of the circuit was made on the Si substrate as shown in the optical micrograph in Fig. 7.2(a). As a consequence additional steps were introduced into the device fabrication to define these mesas. Both, sidegated

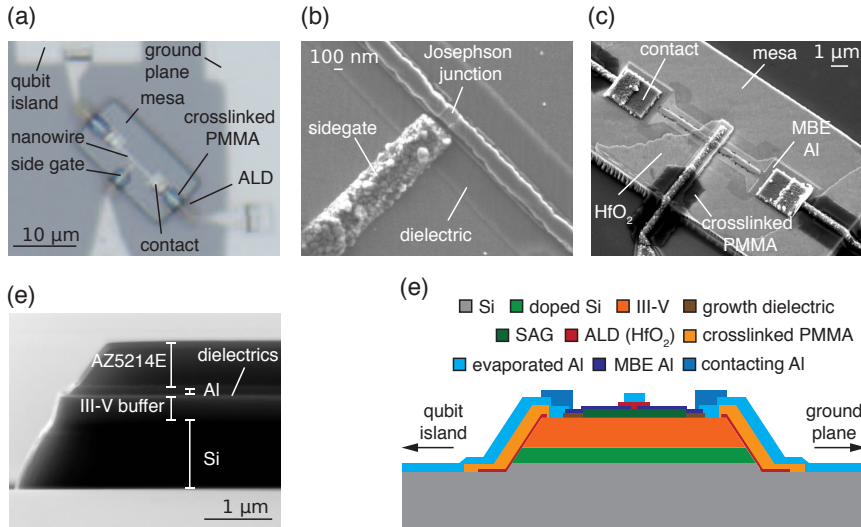


Figure 7.2: Gatemon devices fabricated with Si SAG. (a) Optical image of the area around the nanowire that is fabricated on a 1 μm high mesa and contacted to the qubit island and ground plane that are out of focus. This device is fabricated with a sidegate. Scanning electron micrographs (b) of a JJ with a sidegate and (c) a topgate device. The topgate resides on 15 nm thick HfO₂ layer and climbs the mesa on top of crosslinked PMMA bridges. (d) Scanning electron micrograph of a mesa after the reactive ion etch. The etch creates a trapezoidal profile that aids the climb of gates and contacting metal. (e) Schematic showing a side view of a topgated qubit device, identifying the different components on and near the mesa.

devices [see Fig. 7.2(b)] and topgated devices [see Fig. 7.2(c)] were fabricated on the same chip, where the sidegated devices were fabricated to avoid the use of gate dielectric that could potentially cause decoherence. Additionally, readout resonators were designed to be in the range 6.0 – 6.5 GHz to be far detuned from the dispersive feature of the TWPA feature (see Section 4.5) at ~ 7 GHz.

At the beginning of the qubit fabrication, the entire chip was covered with a 40 nm thick Al film, the dielectric layer consisting of 10 nm thick SiO_x and 5 nm thick AlO_x. As the growth mask dielectrics and III-V buffer layers are a possible source of decoherence, the device fabrication was optimized to reduce the size of the mesa and amount of dielectric around the nanowire. Since this requires small resist masks, meaning the removal of most of the resist, we used a combination of photolithography and negative e-beam resist to reduce exposure times. In a first step, Al was etched selectively on the device chips using Al Etchant Transene D, only leaving Al in dumbbell shaped areas around nanowires [see Figs. 7.2(a) and (c)]. Using the same resist stack, both SiO_x and AlO_x were etched using ammonium fluoride. The dumbbell shape offers a compromise between little dielectric and Al being left around the nanowire [see Fig. 7.2(b)] and sufficiently large MBE Al patches with an area of $\sim 1 \mu\text{m}^2$ being available to connect nanowires with the rest of the circuit. Next, the mesa was defined by protecting the area around the nanowire with photoresist (AZ5214E) while removing GaAs, GaP and ~ 400 nm of Si using two RIE steps. First, an etch with process gases Cl₂ and O₂ was used that created an almost vertical mesa profile. The second etch, which used process gases Cl₂ and O₂, created a trapezoidal mesa profile [see Fig. 7.2(d)]. This is advantageous for the evaporation of continuous Al films on top of the mesa, to form gates and contacts. Then, the JJ was defined by selectively removing a ~ 150 nm long Al segment on the nanowire using Transene Al Etchant Type D at 50 °C. Next, Al for the readout circuit and qubit island definition was evaporated with a lift-off process, where the mesas were protected by resist. The evaporation was preceded by a 10 s long dip in ammonium fluoride to remove surface oxides from the chip, to ensure high internal quality factors of resonator structures and qubit islands. The transmission line, readout resonators, qubit islands, a test resonator and gate lines (see Section 4.3) were defined by selectively removing Al with a wet-etch solution (Transene Al Etchant Type D at 50 °C). Next, 15 nm HfO₂, was grown by atomic layer deposition in lithographically

pre-defined regions on top of the JJs for topgated devices as shown in Fig. 7.2(c). Additionally HfO_2 was deposited in areas where Al would climb mesas to isolate the mesa from future Al layers. In these climbing areas PMMA "bridges" were defined by crosslinking PMMA through the exposure with 30 times the area dose that is typically used to pattern the resist [see Fig. 7.2(c)]. Next, gates (200 nm thick Al) were evaporated. These were later used to tune the critical currents of the single JJs and thereby the qubit frequencies. In addition, Al wires leading from the nanowire to qubit islands and nanowire to the ground plane were deposited. In the final step, the nanowire, qubit island and ground plane were electrically connected by creating ohmic contacts. To ensure a good contact AlO_x on the Al wires and MBE Al was removed Ar-milling prior to the deposition of a ~ 250 nm thick Al layer. The width of the Al wires on the mesa was defined to be relatively thin with ~ 400 nm. The thin wire width in combination with the PMMA bridges and ALD was used to decrease the coupling between superconducting films and the mesa. The measurements presented in the next section indicate that a decoupling from the mesa layers improves coherence times.

7.3 QUBIT DEVICES

During the course of the project the qubit device design and fabrication went through several iterations, with Section 7.2 describing the final iteration which was used to acquire the data that is presented in Sections 7.3.2 and 7.3.3. Previous iterations did not utilize PMMA bridge and showed shorter dephasing times T_2^* as will be discussed below. For all the data presented below, the qubits were driven through their respective gate line.

7.3.1 EFFECT OF PMMA BRIDGES

Figure 7.3(a) shows an optical micrograph of a device without PMMA bridges. Compared to the qubit with PMMA bridge, these devices had larger mesa structures, including larger patches of the dielectric growth mask around the nanowires[‡]. These devices showed a resonator response and measurable qubits in two-tone spectroscopy but time domain measurements were unsuccessful, likely due to the short decoherence times of less than 10 ns.

[‡]The large mesa size was chosen to account for the limited precision of the optical direct-write lithography system at that time, which was $5 - 7 \mu\text{m}$ on a $5 \text{ mm} \times 5 \text{ mm}$ large chip.

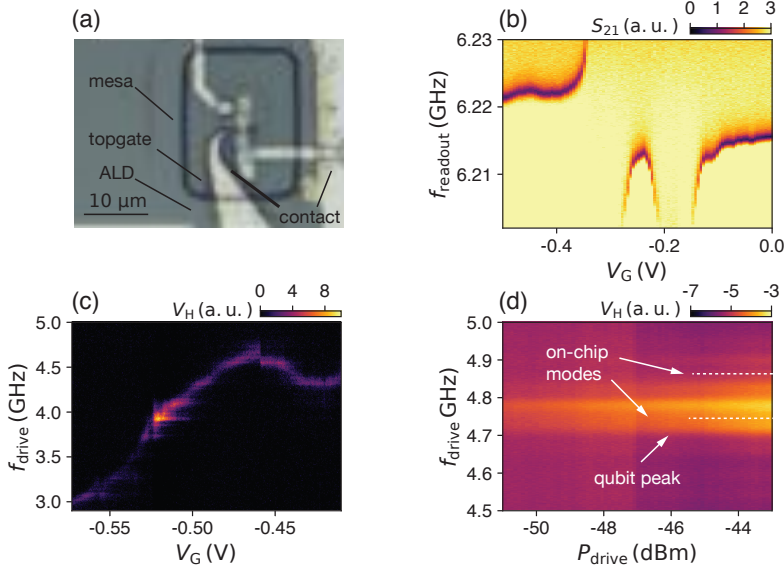


Figure 7.3: Spectroscopy data for devices without PMMA bridges. (a) Optical micrograph of a the qubit device without PMMA bridges. The design differs from the design shown in Fig. 7.2 in several aspects such as: having a larger mesa size, using a nanowire with a different orientation and the width of the metal stripes climbing the mesa. (b) Transmission amplitude S_{21} near the resonance frequency f_r as function of gate voltage V_G . f_r changes as the qubit frequency changes. An avoided crossing is visible at $V_G \approx -0.3$ V. (c) Spectroscopy signal V_H as function of V_G and spectroscopy drive frequency f_{drive} . The qubit frequency (purple and yellow) changes non-monotonically with V_G . (d) Spectroscopy signal as function of drive power P_{drive} and f_{drive} . Only a single dip is measurable. Visible equally spaced peaks can be attributed to on-chip modes.

Figure 7.3(b) shows the transmission coefficient S_{21} near the resonator frequency f_r as a function of gate voltage V_G applied to the JJ. A low readout power was applied, where the resonators showed a dispersive shift. The dispersive shift of the resonator increases as the qubit frequency f_q approaches the bare resonance frequency, with an avoided crossing being measured around $V_G \approx -0.3$ V. With f_q below the resonance frequency, we measured the qubit using two-tone spectroscopy. Figure 7.3(c) shows the amplitude of the resonator response V_H as a function of V_G and qubit drive frequency f_{drive} ,

where the qubit is visible as peak (purple and yellow color). While f_q decreases overall as V_G is lowered in the measured range of 3 – 4.8 GHz, f_Q shows a non-monotonic gate response. As discussed in Section 5.1.4, the non-monotonic behavior is typical for superconductor-semiconductor based junction [21, 26–28, 47, 104] and can be explained by mesoscopic conductance fluctuations caused by electrons scattering across the junction. Figure 7.3(d) shows the spectroscopy signal as a function of f_{drive} and qubit drive power P_{drive} for the qubit at fixed $V_G = -0.41$ V. Even at relatively high P_{drive} , the $|0\rangle \rightarrow |2\rangle$ transition is not measured. This can be explained by the large line width of the qubit, resulting in the transitions overlapping and effectively merging into a single peak. The width of the peak is comparable to the expected distance between peaks corresponding to the $|0\rangle \rightarrow |2\rangle$ and $|0\rangle \rightarrow |1\rangle$ transition of ~ 60 MHz. This estimate assumes $E_C = 240$ MHz and the presence of a few highly transmitting channels in the JJ as discussed in Section 7.3.2.

The devices with PMMA bridges showed low yield due to difficulties during the ALD lift-off step, resulting in only one out of six devices on the chip

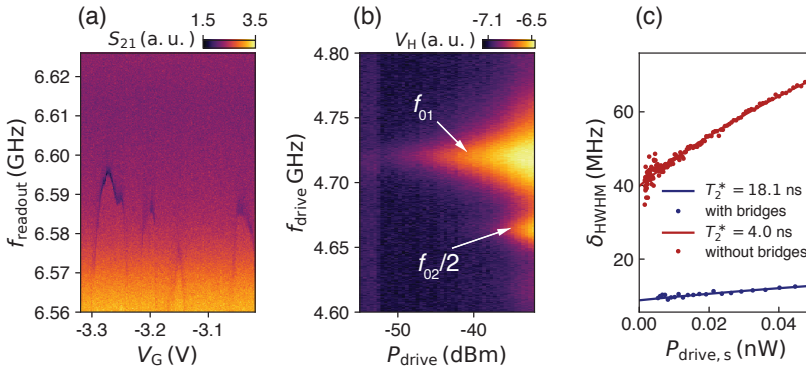


Figure 7.4: Spectroscopy data for devices with PMMA bridges. (a) Transmission amplitude S_{21} near the readout resonator as function of gate voltage V_G . The resonance frequency changes as the qubit frequency changes. (b) Spectroscopy signal as function of P_{drive} and f_{drive} . At higher power a peak corresponding to the $|0\rangle \rightarrow |2\rangle$ transition is measured. (f) Half width at half maximum extracted from a fit to a Lorentzian lineshape from (b) and and Fig. 7.3(d). The decoherence times are calculated from the intersect of the fit with the y -axis using equation $2\pi\delta_{\text{HWHM}} = 1/T'_2 = (T_2^* + n_s\omega_{\text{vac}}^2 T_1/T_2^*)^{1/2}$.

working. This qubit showed a similar gate response compared to the devices without PMMA bridges but an improved dephasing time. Figure 7.4(a) shows that the resonance frequency changes as f_q changes non-monotonically with V_G . The main difference for these devices is shown in Fig. 7.4(b), where two peaks are visible in spectroscopy, which correspond to the $|0\rangle \rightarrow |1\rangle$ and two-photon $|0\rangle \rightarrow |2\rangle$ transition. These peaks can be resolved due to increased dephasing times which results in a decreased line width.

To estimate the dephasing time, we fit a Lorentzian lines shape to the $|0\rangle \rightarrow |1\rangle$ signal. Following Ref. [100], we assume that the half width at half maximum δ is linked to the dephasing by the equation $2\pi\delta = 1/T'_2 = (1/T_2^* + n_s\omega_{\text{vac}}^2 T_1/T_2^*)^{1/2}$, where the factor $n_s\omega_{\text{vac}}^2$ is proportional to the drive power on-chip $P_{\text{drive},s}$ [§], T'_2 is the drive power dependent dephasing time and T_2^* is the dephasing time a zero drive power. By fitting the expression to the results for both qubit, we extract $T_2^* = 4\text{ ns}$ for qubits without bridges and $T_2^* = 18\text{ ns}$ for qubits with bridges. We attribute the increased T_2^* to a reduced coupling of the superconducting films to the mesa promoted by the PMMA bridges. Further tests would be needed to confirm this as the increased T_2^* can also be explained by other effects such as an improved fabrication which leaves less residue around the qubit or less dielectric being left around the nanowire junction. The short coherence times could also be a result of the qubit coupling to on-chip modes[(see Fig. 7.3(d)].

7.3.2 ANHARMONICITY

Based on the DC-transport measurements in Chapter 6, we would expect a JJ with few highly transmitting channels. As discussed in Section 2.6, this would result in a relatively low anharmonicity. Figure 7.5(a) shows the spectroscopy signal as a function of V_G , where two peaks corresponding to the $|0\rangle \rightarrow |1\rangle$ and two-photon $|0\rangle \rightarrow |2\rangle$ transition are measured. We follow the analysis from Ref. [47], that was also used in Section 5.1.4.

The frequencies of these transitions $f_{02}/2$ and f_{01} are extracted by numerically fitting two independent Lorentzian line shapes to the signal and using the position of peak maxima as transition frequencies. The anharmonicity is given by $\alpha/h = 2(f_{02}/2 - f_{01})$. We calculate the set of channel

[§]We assume $P_{\text{drive},s} = P_{\text{drive}} - 30\text{ dB}$ to account for used cryogenic attenuators, line line attenuation and filtering.

transmission $\{T_i\}$ for each value of gate voltage using $\Sigma T_i = (\hbar f_{01})^2 / (2\Delta E_C)$, where we use $\Delta = 190 \mu\text{V}$, found from transport measurements in Chapter 6, and $E_C/\hbar = 240 \text{ MHz}$ from finite-element simulations. Assuming N transmitting channels with equal transmission probability, T , the model gives $\alpha = -E_C(1 - 3E_J/(\Delta N))$. Figure 7.5(c) shows that the anharmonicity lies between the predicted value for $N = 2$ and the model assuming an ideal QPC. That is, assuming channels are filled in a staircase with at most one partially transmitting channel. Based on the fact that all measured anharmonicity fall below the prediction for $N = 2$ in Fig. 7.5(c), it can be assumed that only two channels contribute to transport. Given an equal distribution this sets a lower bound $T_{\min} > \Sigma T_i / 2 \sim 0.45$ on the junction transparency. Similar studies on gatemons with VLS InAs/Al nanowires with in-situ grown epitaxial Al in Ref. [47], where $\alpha \approx 100 - 150 \text{ MHz}$ and two to three channels with $T_{\min} = 0.4 - 0.9$ were reported.

The anharmonicity in this material systems is lower than the anharmonicity in the InP SAGmon device (see Section 5.1.4), where $\alpha/\hbar \approx 200 \text{ MHz}$ and $N > 6$ was found for a similar design, meaning a lower single channel transmis-

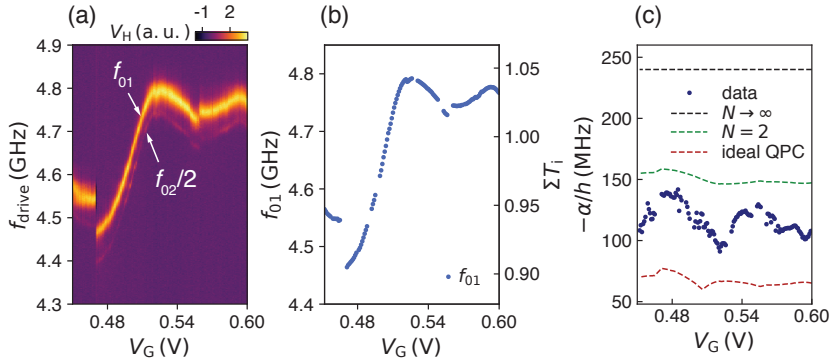


Figure 7.5: Anharmonicity of the Si SAGmon (a) Spectroscopy signal V_H as function of V_G and spectroscopy drive frequency f_{drive} . Two peaks corresponding to $|0\rangle \rightarrow |1\rangle$ and two-photon $|0\rangle \rightarrow |2\rangle$ transition are measured. (b) Extracted transition frequency f_{01} as a function of V_G . The right axis shows the sum of transmitting channels $\Sigma T_i = (\hbar f_{01})^2 / (2\Delta E_C)$. (c) Anharmonicity α/\hbar extracted for the gate sweep shown in (a). The dashed lines indicate the expected anharmonicity for an ideal QPC, two equally transmitting channels ($N = 2$) and the tunneling regime ($N \rightarrow \infty$).

sion. The reduced anharmonicity can be explained by an improved Al/InAs interface originating from an improved growth sequence. In case of the Si-SAGmon, epitaxial Al was grown in-situ after the III-V growth, resulting in a high quality interface. For the InP SAGmon, the Al was evaporated in a second growth chamber after the III-V was exposed to air. Preceding the Al evaporation, the chip was dipped into HF and the surface was cleaned using hydrogen assisted cleaning in order to improve the interface quality. The anharmonicity measurements indicate that these additional steps lead to a lower quality interface than the in-situ growth of Al.

7.3.3 COHERENT OSCILLATIONS

After studying the anharmonicity, we focused on measurements of coherent oscillations and the relaxation time. For these measurements we used the traveling waveform amplifier (TWPA) to amplify the signal at base temperature (see Section 4.8). To drive the qubit, we used the pulse sequence shown in Fig. 7.6(a), where we applied a drive pulse with variable length τ through the gate line. The readout tone was applied for $\sim 1 \mu\text{s}$ before the drive tone to account for the response time of the readout resonator τ_{res} . We estimate τ_{res} using the extracted $Q_{\text{ext}} \approx 2 \cdot 10^4$ and $Q_i \approx 2 \cdot 10^5$, for the readout resonator with resonance frequency $f_r \approx 6.6 \text{ GHz}$. Using the loaded quality factor $Q_l = (Q_i^{-1} + Q_{\text{ext}}^{-1})^{-1} = 1.8 \cdot 10^4$, we estimate $\tau_{\text{rise}} \approx Q_l / (2\pi f_r) \approx 425 \text{ ns}$. Figure 7.6(a) shows the amplitude of the demodulated cavity response V_H as a function of τ and drive frequency f_{drive} . For this measurement, a drive power $P_{\text{drive}} = -16 \text{ dBm}$ at room-temperature. These relatively high drive powers were used to drive coherent oscillation that are faster than the dephasing rate ($\sim 20 \text{ ns}$) $^{-1}$. Coherent oscillation at fixed $f_{\text{drive}} = 4.48 \text{ GHz}$ as function of P_{drive} are shown in Fig. 7.6(b). As expected, the Rabi frequency increases with increased power. The coherent oscillation lose visibility for low values of P_{drive} and long pulse times τ , which we attribute to short decoherence times. Data at fixed $P_{\text{drive}} = -24.2 \text{ dBm}$ and $f_{\text{drive}} = 4.68 \text{ GHz}$ with an added fit are shown in Fig. 7.6(c). The data can be described by a damped sinusoid, as regular Rabi oscillations, with a linear contribution ($m\tau$). We attribute the linear term to leakage to higher level transitions [14] as the used drive powers are high enough to measure the two-photon $|0\rangle \rightarrow |2\rangle$ and three-photon $|0\rangle \rightarrow |3\rangle$ transition. The linear contribution could be reduced by using lower drive

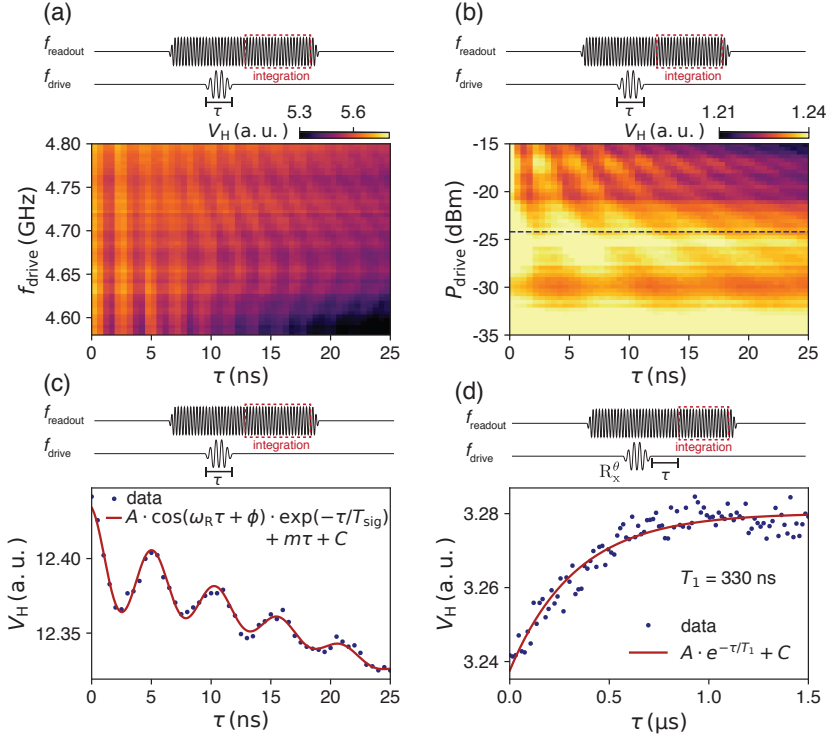


Figure 7.6: Coherent oscillations Si SAGmon. (a) Rabi oscillations as a function of drive frequency f_{drive} and schematic of the pulse sequence at fixed drive power $P_{\text{drive}} = -16$ dBm. The readout resonator is continuously driven and the readout signal is read out after a drive pulse with variable length τ . (b) Rabi oscillations as a function of P_{drive} . The Rabi frequency increases with increasing power. (c) Line cut from (b) at $P_{\text{drive}} = -24$ dBm. Additionally to the coherent oscillation, additional effects are observed that can be described with a damping term $[\exp(-\tau/T_{\text{sig}})]$ with $T_{\text{sig}} \approx 10$ ns and a linear decrease in amplitude. (d) Relaxation time T_1 measurement, where the qubit state is read out after a time τ preceded by a 50 ns long pulse R_x^θ at relatively low power $P_{\text{drive}} = -47$ dBm, which prepares the qubit in a mixed state.

powers, which also reduced the signal-to-noise-ratio. Next, the relaxation time T_1 was measured with the pulse sequence illustrated in Fig. 7.6(d), where the qubit was in a mixed state before integrating for a variable time τ . To avoid measurement artifacts as observed for the Rabi oscillations [see Fig. 7.6(c)],

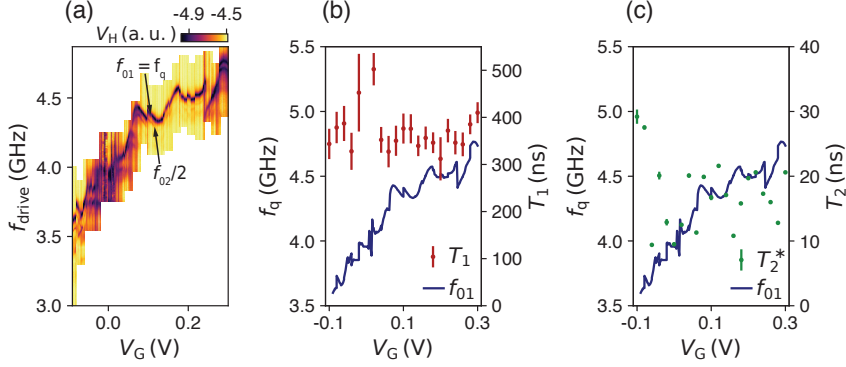


Figure 7.7: Coherence times Si SAGmon. (a) Spectroscopy signal V_H as function of gate voltage V_G and spectroscopy drive frequency f_{drive} , where the $|0\rangle \rightarrow |1\rangle$ $|0\rangle \rightarrow |2\rangle$ transitions are measured. The V_G dependent qubit $f_q(V_G) = f_{01}(V_G)$ is extracted from the data. (b) Relaxation time T_1 and (c) dephasing time T_2^* for 20 different values of V_G and $f_q(V_G)$. No correlation between T_1 , T_2^* and $f_q(V_G)$ or f_q is observed in the measured gate and frequency range.

we used a relatively low drive power $P_{\text{drive},s} \approx -70$ dBm at which $|0\rangle \rightarrow |2\rangle$ transition was no longer measured in continuous two-tone spectroscopy, and a low readout power on-chip $P_{\text{readout},s} \approx -95$ dBm, where the qubit was not AC Stark shifted. Due to the low P_{drive} value, full Rabi oscillations could no longer be performed. Instead, the qubit was driven into a mixed state with a 50 ns long pulse. Figure 7.6(d) shows data with a representative exponential fit yielding $T_1 \approx 330$ ns. T_1 measurements were repeated for different gate voltages and T_2 extracted from the line width [see Fig. 7.4(c)]. Figure 7.7(a) shows the spectroscopy signal for a gate range $-0.1 \text{ V} < V_G < 0.3 \text{ V}$, where the qubit frequency increases overall from $f_q \sim 3.5$ GHz to $f_q \sim 4.8$ GHz with raised V_G . The relaxation time T_1 is one order of magnitude larger than the dephasing time T_2^* . The measured mean values were $T_1 = 380$ ns and $T_2^* = 15$ ns. Both, T_1 and T_2^* showed no correlation with f_q or the frequency dispersion df_q/dV_G , suggesting that gate noise is not limiting the coherence times.

7.4 DISCUSSION AND OUTLOOK

The measurements in this chapter are, to the best of our knowledge, the first demonstration of a gatemon utilizing a selective-area-grown material system on a silicon substrate. The extracted relaxation time $T_1 \approx 330$ ns is comparable to the value measured for InP Sagmons ($T_1 \approx 180$ ns). The advantage of SAG on Si devices is that the internal quality factors of $Q_i \approx 2 \cdot 10^5$ already exceed the values reached on InP substrates ($Q_i \sim 6 \cdot 10^4$), giving a higher theoretical limit for the coherence times if all other sources of decoherence are ignored. The coherence times are order of magnitude lower than the coherence times reported for state-of-the-art VLS-InAs nanowire gatemons ($T_1 \approx 20$ μ s and $T_2^* \approx 4$ μ s in Ref. [25,26]). Given the the relatively high Q_i , the dielectric losses far away from the mesa are unlikely the cause for the low coherence times.

Based on the short coherence times observed in both InP SAGmon and Si SAGmon qubits, it could be concluded that the source of decoherence is correlated to the selective area growth technique. However, the growth details for both platforms differ greatly and are difficult to compare. For instance, Si SAG is grown on a GaAs surface, Si SAG uses an GaAs(Sb) buffer to promote strain relaxation while the material for InP SAGmon devices was grown without buffer. The dielectric mask was not entirely removed for the Si SAGmon but for the InP SAGmon.

Assuming coherence times could be improved Si SAG could be used for many applications and experiments in quantum computing. Follow-up experiments in which the growth, fabrication process or device design are changed can be performed to identify the source of decoherence, using coherence times as figure of merit. Possible loss mechanisms and solutions are listed below:

- **Dielectric loss due to growth mask:** More of the growth dielectric can be removed during device fabrication. HF vapor etches could be used to remove the SiO_x selectively, as HF vapor does not remove Al [140]. In this case, the AlO_x cannot be used for the growth mask.
- **Gate dielectric noise:** The amount of gate dielectric can be reduced or the use gate dielectric can be avoided by the use of a sidegate design. Devices with side gates were already fabricated but the resonators did not show a gate response.
- **Decoherence through gate line:** The decoupling between gate and JJ

can be reduced by either decreasing the overlap between topgate and JJ or by using side gates.

- **Dirt and residue on the chip:** The device fabrication can improved by standardizing the fabrication. In principle, the mesas can be defined before the dielectric growth mask is deposited. For a successful growth the size of the mesa must be comparable to the diffusion length of the grown material, typically in the order of $1\text{ }\mu\text{m}$.
- **Decoupling from GaAs, GaP and doped Si layers using concave mesa profile:** The mesa could be etched with a different dry etch chemistry or wet etching could be used to etch isotropically, leading to a concave mesa shape and an increased distance between the mesa and the residual circuit. In practice, different chemistries are used to etch III-V material and Si, meaning the layers have to be removed in separate steps.
- **Decoupling from GaAs, GaP and doped Si layers using thicker PMMA:** To decouple the qubit from the III-V buffer or Si, a thicker layer of cross-linked PMMA can be used. In principle, the PMMA could be removed after the device fabrication using O_2 plasma cleaning, although the stability of the freestanding metal layer has not been tested yet. This would reduce the capacitive coupling between circuit and mesa as PMMA has a dielectric constant of ~ 3.9 [141].

8

Conclusion and Outlook

8.1 SUMMARY

This thesis has presented selective-area-grown (SAG) InAs/Al hybrid structures as a promising platform for large scale quantum computing.

Chapter 5 introduced the InP SAGmon. Coherent oscillations were demonstrated with coherence times $T_1 \sim 180$ ns and $T_2^* \sim 10$ ns. The fact that the qubit anharmonicity was close to the charging energy ($\alpha/h \sim 0.85E_C$) demonstrated that the interface between InAs and Al was relatively poor. To improve the material quality, an As capping step between growth steps was introduced. The material properties of this second generation material were studied in DC transport using field effect transistor devices and NIS spectroscopy, finding a relatively high field effect mobility $\mu = (1190 \pm 290) \text{ cm}^2/(\text{Vs})$ and a hard superconducting gap. Despite gatemon devices showing a gate response, coherent oscillations with this updated material stack were not observed.

Chapter 6 introduced the Si SAG material system and characterized its electrical properties in terms of requirements for cQED applications. We observed a high average field-effect mobility of $\mu \approx 3200 \text{ cm}^2/\text{Vs}$ for the InAs channel, a hard induced superconducting gap, high transparency Josephson junctions with $\mathcal{T} \approx 0.75$ and signatures of multiple Andreev reflections. Josephson junctions exhibited a gate voltage tunable switching current with

$I_C R_N \approx 83 \mu\text{V}$. Based on these results, we concluded that the material system is a suitable candidate for scalable gate voltage tunable transmon devices and other superconductor-semiconductor hybrid devices fabricated directly on Si.

Chapter 7 presented the RF properties of Si SAG and showed that high quality (low loss) resonators can be fabricated on the substrate after the removal of the GaAs/GaP buffer layer and $\sim 400 \text{ nm}$ of Si. Next, the device fabrication and several considerations were discussed that led to the development of gatemons with coherence times $T_1 \approx 380 \text{ ns}$ and $T_2^* \approx 15 \text{ ns}$. From anharmonicity measurements we extract a relatively high junction transparency with a lower bound of $T_{\min} \sim 0.45$, in reasonable agreement with DC transport measurements in Chapter 6. Currently the loss mechanism(s) leading to the short coherence times are not well understood and further work is needed to improve coherence times.

8.2 OUTLOOK

Between the two material systems discussed in this thesis, Si SAG outperforms InP SAG as a platform for scalable quantum computing. First, measured junction transparencies and field effect mobilities are higher for Si SAG. Second, Si SAGmon devices showed longer coherence times. However, this comparison is specific to the growth process chosen for both systems. In the case of InP SAG, the Al layer was not grown *in-situ*, potentially leading to a poor interface quality between InAs and Al. Although InP SAG could potentially be improved, the Si SAG platform enables qubit islands with a smaller loss tangents and thus higher theoretical limits for coherence times, given other loss mechanisms are not considered. Further, Si is the standard substrate used in today's semiconductor industry, alleviating challenges of integrating potential future qubit fabrication into industrial processes. While a Si SAGmon offers potentially less crosstalk compared to the standard metallic transmons [5, 142] due to being voltage controlled [22], creating a truly competitive device beyond these initial demonstrations rests on a few key optimization tasks. First and foremost, coherence times must be increased. Changes in the design, fabrication or growth can be made to test for likely decoherence channels. On a relatively short timescale the following changes could be made: Side gates could be used instead of topgates to remove gate dielectric from the process flow. The growth dielectric around nanowires could be removed by means of

HF vapor etching or design changes. In order to decouple qubits from the lossy mesa stack, thicker PMMA bridges could be used. Alternatively, the mesa can be etched with a different dry etch chemistry or wet etched isotropically to create a concave mesa shape, leading to an increased distance and thus smaller coupling between the mesa and the residual circuit. On longer time scales, other growth strategies could be employed to bridge the lattice mismatch between Si and InAs such as the growth of Ge instead of GaP [143–145]. Other possible improvements in terms of device fabrication could be the integration of the mesa etch before the selective area growth. Here, the mesa size could potentially be reduced to $\sim 5 \mu\text{m}$ in one direction, set by the diffusion length of particles during the MBE growth. Using this approach, the readout circuit and qubit island could be made with the continuous MBE Al film, removing the need for contacting steps in the later fabrication.

Assuming coherence times could be improved to reach state-of-the-art coherence times of current gatemons ($T_1 \approx 20 \mu\text{s}$ and $T_2^* \approx 4 \mu\text{s}$ [25, 26]), Si SAG could be used for many applications and experiments in quantum computing. In addition to simply reproducing results previously achieved using superconducting qubits, future experiments could utilize the voltage-tunability or high transparency of the semiconductor based Josephson junctions. Examples are voltage tunable quantum buses [146] and storage scalable voltage-tunable quantum memory [147]. Here, Josephson junctions field effect transistors would be integrated into distributed element resonators as switches to turn interaction on or off. All of these devices could be aided by interfacing them with ultra low power cryogenic CMOS control systems that are either close to the quantum plane at 4 K or directly mounted at the millikelvin stage [148]. Si SAGmons could be used to test one long-standing claim about gatemons in context of large scale quantum computing. That is, due to being voltage controlled, gatemons are less susceptible to crosstalk between qubits and on-chip heating than flux controlled metallic transmons [22], which require milliamperic currents on the device level. An alternative pathway to enhanced qubit lifetimes are protected superconducting qubits, which have previously been realized using VLS nanowires [129]. Other approaches could utilize a suppressed charge dispersion in gatemons [149, 150].

Overall, this thesis presented characterization of the Si SAG material system and demonstrated the first gate-voltage tunable superconducting qubits based on this material. If the future steps towards increased coherence times are

realized, Si SAG could become a scalable, low footprint platform for qubit circuitry with low crosstalk, low dissipation and interfaced with ultra low power cryogenic CMOS control systems.



Material Growth InP SAGmon

This Appendix presents the pre-growth fabrication and a brief summary of the growth for the InP SAG material used in Chapter 5, which was grown by collaborators at NEST, Istituto Nanoscienze Pisa, Italy as well as Purdue University, USA, and University of Copenhagen, Denmark. While the growth process is different for the first and second generation material, the growth mask preparation is identical. Unless stated otherwise, the devices were fabricated at the Niels Bohr Institute (NBI) cleanroom. The proximity error correction (PEC) was performed using the software BEAMER version 5 from GenISys GmbH. The settings for sonication and ashing refer to the Elmasonic P 30 H ultrasonic bath and Diener asher, which are used in the NBI cleanroom.

A.1 GROWTH MASK PREPARATION

Start with pristine on a Fe-doped (100) 2 inch InP substrate, single side polished, $\rho > 10^7 \Omega\text{cm}$ from CrysTec Kristalltechnologie, wafer thickness 350 μm .

1. SiO_x deposition

- Deposition of 10 nm of SiO_x using plasma-enhanced chemical vapor deposition
- Details: SPTS Multiplex PECVD system at DTU Nanolab, Lyngby, Denmark, Recipe name: "Standard HF SiO2", temperature: 300°C

2. Growth mask patterning

- Spin coat wafer with EL9* with 4000rpm for 45s, bake for 2 min at 185°C on hotplate
- Exposure with Elionix ELS-F100 at 100 kV acceleration voltage.
 - Expose nanowire features with area base dose 380 $\mu\text{C}/\text{cm}^2$:
Details: critical feature size: 100 nm, current: 500 pA, aperture: 40 μm , write field size: 300 μm , number of dots: 60000, dwell time: 0.19 $\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
 - Expose alignment marks with area base dose 600 $\mu\text{C}/\text{cm}^2$:
Details: current: 500 pA, aperture: 40 μm , write field size: 300 μm , number of dots: 60000, dwell time: 0.3 $\mu\text{s}/\text{dot}$, no PEC.
 - Alternate between exposure of nanowire features and alignment marks to ensure sufficient alignment between layers. Reduce rotation by aligning design relative to major flat using virtual alignment marks.
- Develop resist for 45 s in MIBK:IPA 1:3 solution, rinse in IPA for 30 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100%*power*.
- Hardbake at 121 °C for 30 s on hotplate
- Wet etch mask and clean wafer
 - Rinse wafer in IPA for a few seconds, rinse wafer in MQ for a few seconds.

*9% solids of co-polymer (MMA (8.5) MAA) in ethyl lactate, from Kayaku Advanced Materials

- Dip wafer in ammonium fluoride for 2 – 3 s.
- Rinse in MQ for 10 s, rinse in a second MQ beaker for 20 s.
- Soak wafer in acetone for 15 min, sonicate for 30 s with 80 kHz at 30 %.
- Rinse and sonicate for 15 s with 80 kHz at 30 % in a second acetone beaker, two consecutive IPA beakers and MQ beaker.
- Rinse under running MQ water, blow dry with N_2 .

A.2 GROWTH FIRST GENERATION MATERIAL

A.2.1 GROWTH OF SEMICONDUCTOR LAYERS

The semiconductor layers were grown using CBE by Lucia Sorba's group at NEST, Istituto Nanoscienze Pisa, Italy.

1. CBE growth of 20 nm InP and 17 nm InAs at 440 °C.

A.2.2 GROWTH OF Al

Al was grown using MBE by the Manfra group at Purdue University.

1. SiO_x removal and wafer cleaning with 20 s using diluted HF.
2. Hydrogen assisted plasma cleaning for 20 min at 310 °C.
3. MBE growth of 40 nm Al.

A.3 GROWTH SECOND GENERATION MATERIAL

A.3.1 GROWTH OF SEMICONDUCTOR LAYERS

The semiconductor layers were grown using by Lucia Sorba's group at NEST, Istituto Nanoscienze Pisa, Italy.

1. Growth of 8 nm InP, 16 nm InP_{0.7}As_{0.3} and 29 nm InAs at 490 °C.
2. As capping of the entire substrate.

A.3.2 GROWTH OF Al

Al was grown by the Krogstrup group at the Niels Bohr Institute, Copenhagen, Denmark.

1. As removal at 500 °C with As overpressure.
2. MBE growth of 40 nm Al.

B

InP device fabrication details

This appendix presents the fabrication details for the first generation InP SAGmon devices, the second generation InP SAGmon devices and the DC test structures on second generation InP SAGmon material. Unless stated otherwise, the devices were fabricated at the Niels Bohr Institute (NBI) cleanroom. The proximity error correction (PEC) was performed using the software BEAMER version 5 from GenISys GmbH. The settings for sonication and ashing refer to the Elmasonic P 30 H ultrasonic bath and Diener asher, which are used in the NBI cleanroom. For evaporation an AJA Orion series UHV deposition tool with base pressure 10^{-8} Torr was used.

B.1 FIRST GENERATION QUBIT

1. Cleaving and cleaning:
 - Cleave wafer into 10 mm · 9.2 mm chips.
 - Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 with N_2 .
2. Josephson junction and microwave control etch
 - Spin coat with EL9* with 4000rpm for 45s, bake for 2 min at 115°C

*9% solids of co-polymer (MMA (8.5) MAA) in ethyl lactate, from Kayaku Advanced Materials

on hotplate.

- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose junction area with area base dose $280 \mu\text{C}/\text{cm}^2$:
Details: critical feature size: 100 nm, current: 1 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.0157 \mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
 - Expose large features with $420 \mu\text{C}/\text{cm}^2$:
Details: critical feature size: $2 \mu\text{m}$, current: 200 nA, aperture: $240 \mu\text{m}$, write field size: $600 \mu\text{m}$, number of dots: 20000, pitch: 30, dwell time: $1.89 \mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
- Develop resist for 30 s in MIBK:IPA 1:3, rinse in IPA for 20 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- Hardbake at 125°C for 1 min on hotplate.
- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50°C . Place one MQ beaker at room temperature.
 - Etch 8 s in 50°C etchant, stir 20 s in 50°C MQ, stir 40 s in room temperature MQ, blow dry with N_2 .
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

3. Gate dielectric deposition

- Spin coat with EL13[†] with 4000rpm for 45s, bake for 1 min at 115°C on hotplate.
- Spin coat with A4.5[‡] with 4000rpm for 45s, bake for 1 min at 115°C on hotplate.
- Exposure with Elionix ELS-125.
 - Expose with area base dose $900 \mu\text{C}/\text{cm}^2$:
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.018 \mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.

[†]13% solids of co-polymer (MMA (8.5) MAA) in ethyl lactate, from Kayaku Advanced Materials

[‡]4.5% solids of 950K PMMA in anisole, from AllResist

- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100% power.
- Atomic layer deposition of 15 nm of HfO₂ using 150 cycles at 110°C, alternating between TDMAH (tetrakis(dimethylamino)hafnium) and water vapor, using 10 h pumpdown preceding deposition.
- Lift-off overnight in acetone at room temperature or for 2 h in acetone at 50 °C.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

4. Topgate evaporation

- Spin coat with EL9 with 4000rpm for 45s, bake for 1 min at 115°C on hotplate.
- Spin coat with A4.5 with 4000rpm for 45s, bake for 3 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose features within $\sim 20\mu\text{m}$ of the nanowire with area base dose $900\mu\text{C}/\text{cm}^2$:
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120\mu\text{m}$, write field size: $500\mu\text{m}$, number of dots: 500000, pitch: 3, dwell time: $0.027\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
 - Expose features far away from the nanowire with area base dose $900\mu\text{C}/\text{cm}^2$:
Details: critical feature size: $10\mu\text{m}$, current: 100 nA, aperture: $240\mu\text{m}$, write field size: $500\mu\text{m}$, number of dots: 50000, pitch: 8, dwell time: $0.704\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N₂.
- Oxygen plasma cleaning for 1 min at 100% power.
- Evaporate 2 nm Ti with electron beam with rate $\sim 2\text{Å}/\text{s}$ and 50 nm Al with rate $\sim 1\text{Å}/\text{s}$.
- Lift-off in room temperature acetone or in 50 °C acetone for 2 h.

- Forming gas annealing 30 min at 150°C.[§]
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

5. Contacts

- Spin coat with EL13 with 4000rpm for 45s, bake for 1 min at 115°C on hotplate.
- Spin coat with A6[¶] with 4000rpm for 45s, bake for 3 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose features with area base dose 900 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 500000, pitch: 3, dwell time: 0.027 $\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N₂.
- Oxygen plasma cleaning for 1 min at 100% power.
- Kauffmann milling for 4.5 min with 300 V beam voltage, Ar pressure 1 mTorr, flow 15 sccm Discharge for 5 min and warm up for 1 min before milling.
- Evaporate 2 nm Ti with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$ and 50 nm Al with electron beam with rate $\sim 1 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone overnight or in 150 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

B.2 SECOND GENERATION QUBIT

1. Cleaving and cleaning:

[§]Forming gas annealing was introduced into the process to reduce the hysteresis in devices. Due to the limited amount of working devices after device fabrication, it could not be concluded that this step actually reduces gate hysteresis.

[¶]6% solids of 950K PMMA in anisole, from AllResist

- Cleave wafer into 10 mm · 9.2 mm chips.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

2. Global Al and SiO_x etch

- Spin coat with adhesion promoter AR300-80^{||} with 4000rpm for 45s, bake for 1 min at 185°C on hotplate. Strip adhesion promoter 2 min in 1,3-dioxolane, soak 1 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.
- Spin two layers AR-N 7520^{**} with adhesion promoter AR300-80 with 4000rpm for 45s, bake each layer for 2 min at 7520°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose features near nanowires with area base dose 75 μC/cm².
Details: critical feature size: 100 nm, current: 5 nA, aperture: 120, μm, write field size: 500 μm, number of dots: 50000, pitch: 1, dwell time: 0.015 μs/dot, PEC: 100% uniform clearing.
 - Expose features far away from nanowires with area base dose 75 μC/cm².
Details large features: critical feature size: 2 μ, current: 200, nA, aperture: 240 μm, write field size: 600 μm, number of dots: 20000, pitch: 30, dwell time: 1.89 μs/dot, PEC: 100% uniform clearing.
- Develop resist mask for 60 s in MF321, rinse in IPA for 20 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100% power.
- Hardbake at 115 °C for 1 min on hotplate.
- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50 °C. Place one MQ beaker at room temperature.
 - Etch 18 s in 50 °C etchant, stir 20 s in 50 °C MQ, stir 30 s in room temperature MQ, blow dry with N₂.

^{||}from AllResist

^{**}from AllResist

- Dry etch SiO_x using process gases O₂ and CHF₃ in III-V RIE at DTU Nanolab, Denmark, recipe: "SiO2_602".
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

3. Junction etch

- Spin coat with adhesion promoter AR300-80 with 4000rpm for 45s, bake for 1 min at 185°C on hotplate. Strip adhesion promoter 2 min in 1,3-dioxolane, soak 1 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.
- Spin coat with EL9 with 4000rpm for 45s, bake for 3 min at 185°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose with area base dose 720 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 1 nA, aperture: 120, μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.0463 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 20 s in MIBK:IPA 1:3, rinse in IPA for 20 s, blow dry with N₂.
- Oxygen plasma cleaning for 1 min at 100% power.
- Hardbake by putting the chip on a hotplate at 115 °C. Set hotplate to 125 °C and bake for 1 min after the hotplate reached 125 °C.
- Wet etch Al.
 - Prepare etchant by mixing 38 ml MQ and 2 ml MF321 at room temperature. Prepare etch stop with 1 part acetone and 1 part 2-propanol.
 - Etch 52s, stir vigorously in etch stop for 10s, soak 4 min in acetone, rinse in 2-propanol and blow dry with N₂.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

4. Al evaporation

- Spin coat with 50K^{††} with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.

^{††}12% solids of 50K PMMA in anisole, from AllResist

- Spin coat with A4.5 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose features near nanowires with area base dose 920 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.0192 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
 - Expose features far away from nanowires with area base dose 1300 $\mu\text{C}/\text{cm}^2$.
Details for features around nanowires: critical feature size: 100 nm, current: 3 nA, aperture: 240 μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.0192 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- 100 nm Al with rate $\sim 1 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone or in 50 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

5. Microwave-control etch

- Spin coat with EL9 with 4000rpm for 45s, bake for 3 min at 185°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose with area base dose 300 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 2 μm , current: 100 nA, aperture: 240 μm , write field size: 500 μm , number of dots: 50000, pitch: 8, dwell time: 0.192 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist mask for 30 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N_2 .
- Oxygen plasma cleaning for 2 min at 100% power.
- Hardbake at 125 °C for 30 s on hotplate.

- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50 °C. Place one MQ beaker at room temperature
 - Etch 18 s in 50 °C etchant, stir 20 s in 50 °C MQ, stir 30 s in room temperature MQ, blow dry with N₂.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

6. Gate dielectric deposition

- Spin coat with EL9 with 4000rpm for 45s, bake for 1 min at 115°C on hotplate.
- Spin coat with A4.5 with 4000rpm for 45s, bake for 1 min at 115°C on hotplate.
- Exposure with Elionix ELS-125.
 - Expose with area base dose 880 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.0183 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100% power.
- Atomic layer deposition of 20 nm of Al₂O₃ using 150 cycles at 90°C, alternating between TMA (trimethylaluminum(CH₃)₃Al) and water vapor, 10 h pumpdown preceding deposition.
- Lift-off overnight in acetone at room-temperature or for 2 h in acetone at 50 °C.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

7. Topgate evaporation

- Spin coat with 50k with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Spin coat with A4.5 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.

- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose features near nanowires with area base dose $500 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.0104 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
 - Expose features far away from nanowires with area base dose $500 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: $10 \mu\text{m}$, current: 100 nA, aperture: $240 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 50000, pitch: 8, dwell time: $0.32 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- Evaporate 2 nm Ti with rate $\sim 2 \text{ \AA}/\text{s}$ with electron beam and 50 nm Al with electron beam with rate $\sim 1 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone or in 50°C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

8. Contacts

- Spin coat two layers with 50k with 4000rpm for 45s, bake each for 2 min at 115°C on hotplate.
- Spin coat with A6 with 4000rpm for 45s, bake for 3 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose with area base dose $550 \mu\text{C}/\text{cm}^2$.
Details for features around nanowires: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.0115 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.

- Kaufman milling for 4.5 min with 300 V beam voltage, Ar pressure 1 mTorr, flow 15 sccm. Discharge for 5 min and warm up for 1 min before milling.
- Evaporate 2 nm Ti with electron beam with rate $\sim 2 \text{ \AA/s}$ and 50 nm Al with electron beam with rate $\sim 1 \text{ \AA/s}$.
- Lift-off in room temperature acetone or in 150 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

B.3 FET DEVICES

1. Contacts

- Spin coat two layers 50k with 4000rpm for 45s, bake each for 2 min at 115°C on hotplate.
- Spin coat with A6 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose features near nanowires with area base dose $920 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: 0.0192, $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
 - Expose large features far away from nanowires with area base dose $1300 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: $2 \mu\text{m}$, current: 100 nA, aperture: $240 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 8, dwell time: 0.832, $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- Kaufman milling for 8 min with 100 V, pressure 1 mTorr, flow 15 sccm. Discharge for 5 min and warm up for 1 min before milling.
- Evaporate 2 nm Ti with electron beam with rate $\sim 2 \text{ \AA/s}$ and 120 nm Au with electron beam with rate $\sim 2 \text{ \AA/s}$.

- Lift-off in room temperature acetone or in 150 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

2. Global gate dielectric

- Atomic layer deposition of 15 nm of HfO₂ using 150 cycles at 90°C, alternating between TDMAH (tetrakis(dimethylamino)hafnium) and water vapor, using 10 h pumpdown preceding deposition.

3. Gate evaporation

- Spin coat one layer 50k with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Spin coat with A6 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose small features near nanowires with area base dose 920 $\mu\text{C}/\text{cm}^2$.
 Details: critical feature size: 100 nm, current: 3 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.0192, $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing. Expose large features far away from nanowires with area base dose 1300 $\mu\text{C}/\text{cm}^2$.
 Details: critical feature size: 2 μm , current: 100 nA, aperture: 240 μm , write field size: 500 μm , number of dots: 200000, pitch: 8, dwell time: 0.832, $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N₂.
- Oxygen plasma cleaning for 1 min at 100% power.
- Evaporate 2 nm Ti with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$ and 120 nm Au with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone or in 150 °C acetone for 2 h.
- Sonicate for 1 min in NMP with 80 kHz and 30 %, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

B.4 NIS SPECTROSCOPY DEVICE

1. Junction etch and Al removal

- Spin coat with EL9 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose junction with area base dose 280 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 1 nA, aperture: 120, μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.0175, $\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
 - Expose larger features with area base dose 420 $\mu\text{C}/\text{cm}^2$.
Details larger features: critical feature size: 100 nm, current: 100 nA, aperture: 120, μm , write field size: 500 μm , number of dots: 50000, pitch: 16, dwell time: 1.0752, $\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
- Develop resist for 30 s in MIBK:IPA 1:3, rinse in IPA for 20 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- Hardbake by putting the chip on a hotplate with 125 °C for 1 min.
- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50 °C. Place one MQ beaker at room temperature.
 - Etch 16 s in 50 °C etchant, stir 20 s in 50 °C MQ, stir 40 s in room temperature MQ, blow dry with N_2 .
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

2. Contacts

- Spin coat two layers 50k with 4000rpm for 45s, bake each for 2 min at 115°C on hotplate.
- Spin coat with A6 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.

- Expose features near nanowires with area base dose $920 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.0192, \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Expose large features far away from nanowires with $1300 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: $2 \mu\text{m}$, current: 100 nA, aperture: $240 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 8, dwell time: $0.832, \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- RF milling with Ar for 6 min with 100 V beam voltage, Ar pressure 18 mTorr, flow 30 sccm,
- Evaporate 2 nm Ti with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$ and 120 nm Au with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone or in 150°C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

3. Global gate dielectric

- Atomic layer deposition of 10 nm of HfO_2 , 10 h pumpdown, 150 cycles at 90°C .

4. Gate evaporation

- Spin coat one layer 50k with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Spin coat with A6 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV.
 - Expose small features near nanowires with area base dose $920 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.0192, \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.

- Expose large features far away from nanowires with $1300 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: $2 \mu\text{m}$, current: 100 nA , aperture: $240 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 8, dwell time: $0.832 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 60 s in MIBK:IPA 1:3, rinse in IPA for 15 s, blow dry with N_2 .
- Oxygen plasma cleaning for 1 min at 100% power.
- Evaporate 2 nm Ti with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$ and 120 nm Au with electron beam with rate $\sim 2 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone or in 150°C acetone for 2 h.
- Sonicate for 1 min in NMP with 80 kHz and 30 %, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

C

Measurement Setup InP SAG

This appendix presents the two setups used to acquire the data presented in Chapter 5. The setup in Fig. C.1 was used for DC transport measurements of the field-effect transistor (FET) devices and NIS spectroscopy devices. Both

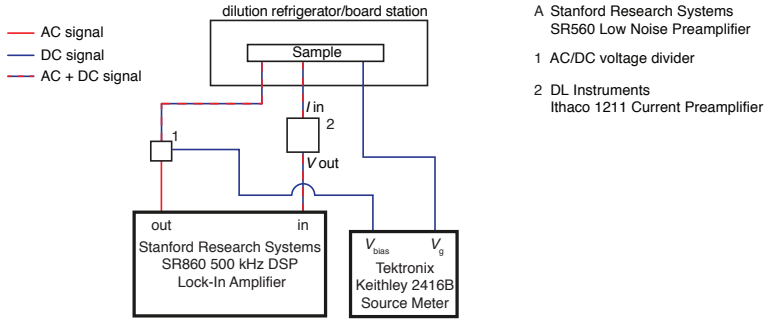


Figure C.1: Schematic of DC transport setup for InP SAG. Schematic of the setup used in Section 5.2.2 for field-effect transistor (FET) and NIS spectroscopy measurements. For FET measurements no DC bias V_{bias} was used. The sample was loaded into a board station that was cooled down to ~ 4 K. The measure NIS device was loaded into a dilution refrigerator using a puck as described in Section 4.4. These devices are DC biased with V_{bias} .

devices were glued and bonded to the PCB daughterboard shown in Fig. 4.4(c). The FET devices were loaded inside board station, which is specifically designed for these daughterboards. Using the board station, the device was cooled down to a temperature ~ 4 K. The AC (DC) signal was reduced by approximately 10^{-3} before being applied to the sample to apply a voltage $V_{AC} \sim 20 \mu\text{V}$ at the sample with frequency $f = 121.6$ GHz. No DC voltage was applied. On the measurement side the outgoing current was converted using a transimpedance amplifier into a voltage with a factor 10^6 V/A . NIS spectroscopy devices were also glued and bonded to the PCB daughterboard. The daughterboard was then loaded into the motherboard and puck [see Fig. 4.4(d)] to load it into the dilution refrigerator and cool down to ~ 30 mK. The AC (DC) signal was reduced by approximately 10^{-4} (10^{-2}) before being applied to the sample to apply a voltage $V_{AC} = 5 - 20 \mu\text{V}$ ($V_{\text{bias}} = 0 - 1 \text{ V}$),

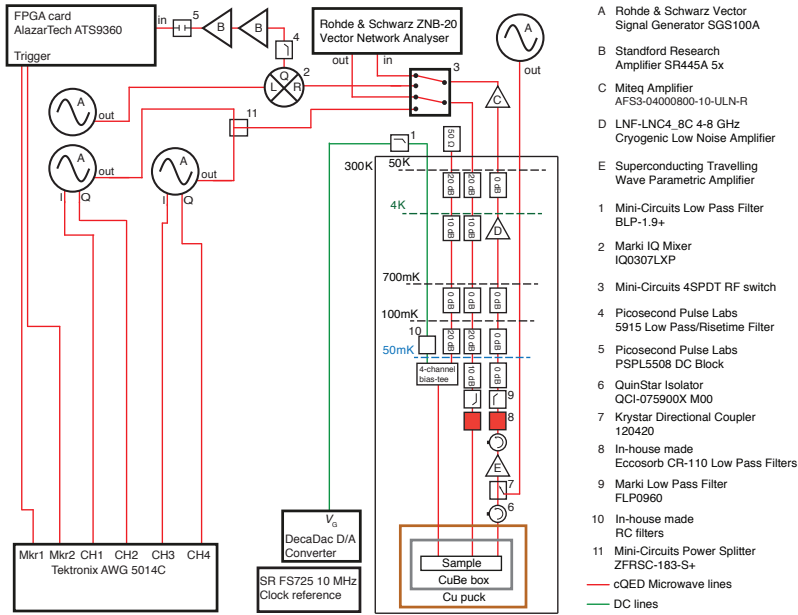


Figure C.2: Schematic of cQED setup for InP SAG. Schematic of the cQED setup used in Section 5.1.4, which is very similar to the setup described in Section 4.8. The main differences are that a different bias tee version was used and the local oscillator tone for the signal demodulation was generated by a dedicated RF source.

where the AC signal had a frequency $f = 19$ GHz. On the measurement side the outgoing current was converted using a transimpedance amplifier into a voltage with a factor 10^8 V/A.

Figure C.2 shows a schematic of the cQED setup used for the measurements discussed in Section 5.1.4. This setup is very similar to the setup discussed in Section 4.8. The two main differences are that an earlier version of bias tees with four channels was used. These bias tees were used to combine the DC signal V_G for the modulation of the critical current the junction with and RF signal for driving the qubit. These bias tees were later replaced with 6-channel bias tees with a smaller frequency dispersion between 4 and 6 GHz.

D

Gate Capacitance Simulations

This appendix presents the simulations used to estimate the gate capacitance used to extract the field effect mobility μ from field-effect transistor (FET) measurements in Chapters 5 and 6.

D.1 INP SAG SIMULATION

To calculate the capacitance between topgate and InAs C_G for the FET devices shown in Section 5.2.2, we used finite-element methods simulation from Valentina Zannier from NEST, Istituto Nanoscienze-CNR, who also grew the material. The cross section was assumed to be rectangular as shown in Fig. D.1(a), where the height of the nanowire $h = 30$ is independent of the nanowire width w . The resulting gate capacitance C_G for $6\text{ }\mu\text{m}$ long nanowires with a variable width w is shown in Fig. D.1(b). A linear function is fitted to the data yielding $C_G = w \cdot 0.06\text{ fF/nm} + 6.426\text{ fF}$, which can be used to estimate the capacitance for $w > 170\text{ nm}$.

D.2 Si SAG SIMULATION

To calculate the capacitance between topgate and InAs C_G , we modeled the system with finite-element methods using COMSOL [90]. Based on TEM

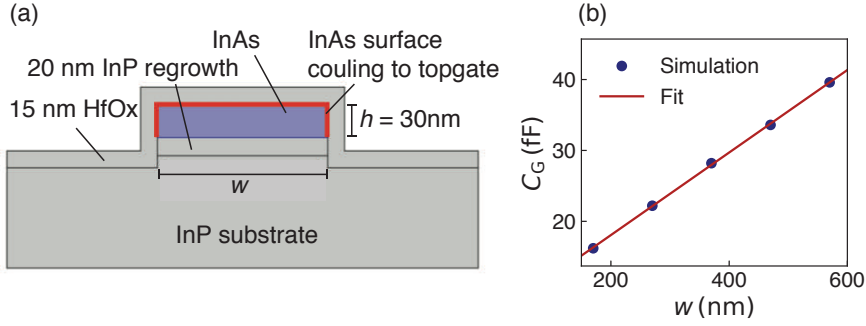


Figure D.1: Gate capacitance simulation for InP SAG. (a) Material stack used for capacitance simulation, where the red line indicates the InAs surface that couples to the topgate. The nanowire is approximated to have a rectangular cross section with wire width w . (b) Simulated C_G for different w with a linear fit yielding $C_G = w \cdot 0.06 \text{ fF/nm} + 6.426 \text{ fF}$.

images we assumed that InAs is encapsulated in the $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ matrix [see Fig. D.2(a)]. As shown in Fig. D.2(b), we approximated the wire cross section to be rectangular. Figure D.2(c) shows the resulting gate capacitance C_G for $6 \mu\text{m}$ long nanowires with different widths w . We use a linear fit to the data to estimate $C_G = w \cdot 0.02 \text{ fF/nm} + 2.203 \text{ fF}$ for any given nanowire width w over 200 nm .

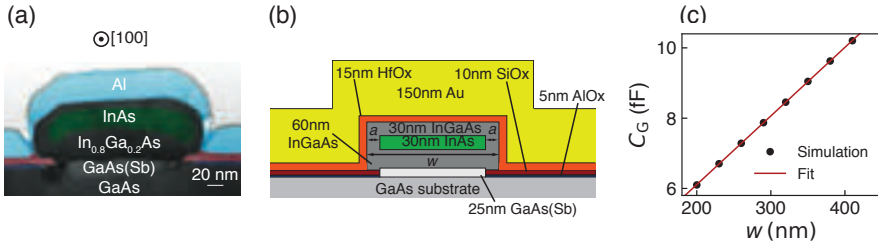


Figure D.2: Gate capacitance simulation for Si SAG (a) False-colored transmission electron micrograph of material stack. (b) Model used to simulate the capacitance between topgate and InAs layer C_G . The width of the InAs channel is assumed to be $w - 2a$, where $a = 15 \text{ nm}$. (c) Result of the simulation for different wire widths with a linear fit yielding $C_G = w \cdot 0.02 \text{ fF/nm} + 2.203 \text{ fF}$.

E

DC Measurement Setup Si SAG

This appendix presents the instrument settings used for the measurements in Chapter 6. Figure E.1 shows a schematic of the used setup, where identical instruments are numbered. The instruments settings of representative measurements are summarized below:

- Lock-in 1
 - Frequency: 212 Hz
 - Timeconstant: 100 ms
- Lock-in 2
 - Frequency: 212 Hz (following Lock-in 1)
 - Timeconstant: 100 ms
- I-to-V converter
 - Conversion: 10^6 V/A
 - Cut-off frequency: 3 kHz
- A1
 - DC coupling

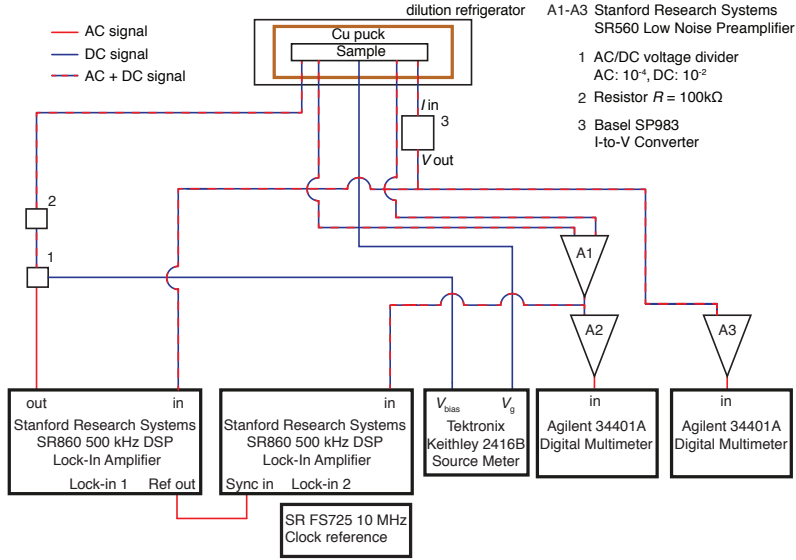


Figure E.1: Schematic of DC measurement setup for Si SAG. Schematic of the instrumentation used for four-terminal, current biased, DC transport measurements (Chapter 6). Red lines indicate cables that carry an AC signal, blue lines indicate lines that carry a DC signal and blue-red dashed lines indicate cables that carry both components. All instruments are synchronized with a 10 MHz clock reference. To measure the device in a 2-terminal voltage-bias configuration the bias resistor ($R = 100\text{k}\Omega$) is removed and only the signal after the transimpedance amplifier (Basel SP983) is measured with the lock-in amplifier to obtain the differential conductance dI/dV . Instruments are numbered to distinguish identical instruments.

- Source A-B
- Gain mode: low noise
- Gain: 10^2
- A2
 - DC coupling
 - Source A
 - Gain mode: low noise
 - Gain: 1

- cut-off frequency: 10 Hz
 - use low pass 12 kHz
- A3
 - DC coupling
 - Source A
 - Gain mode: low noise
 - Gain: 1
 - Cut-off frequency: 10 Hz
 - Filtering: Low pass at 12 kHz

F

Si SAG transport supplementary material

This appendix summarizes parts of the supplementary material from Chapter 6.

F.1 MATERIAL AND DEVICE FABRICATION

All three devices were fabricated on the same chip with standard electron beam lithography techniques. In a first step, Josephson junctions were defined by selectively wet etching $L \sim 120$ nm long segments of the ~ 40 nm thick Al film on the nanowires [Fig. 6.3(b)]. In a second step, Al was globally removed from the nanowires that were used for FET devices. Then, contacts were defined in a lift-off process. The chip was placed in an evaporation chamber and a 30s argon ion mill was performed in situ to ensure a low contact resistance followed by the evaporation of Ti/Au (5nm, 150nm). Next, 15 nm of HfO₂ was deposited globally using atomic layer deposition as gate dielectric. For the final step Ti/Au (5nm, 150nm) was evaporated to form topgates.

F.2 COHERENCE LENGTH ESTIMATE

We estimate the coherence length based on the average charge carrier density, n , and field-effect mobility, μ , values estimated from the FET measurements (see Section 6.3), considering only nanowires with the same orientation and width as nanowire B. First, we estimate the Fermi velocity, $v_F = \hbar v_F / m^*$, where we take the three-dimensional expression for the Fermi wavenumber, $k_F = (6n\pi^2)^{1/3}$, and use the bulk value for the effective electron mass in InAs $m^* = 0.023m_e$ (where m_e is the free electron mass). This gives a Fermi velocity $v_F = 1.23 \cdot 10^6$ m/s, close to the bulk InAs value $v_{F,\text{bulk}} = 1.3 \cdot 10^6$ m/s. We estimate a mean free electron path $l_e = (\mu m^* v_F) / e = 59$ nm that is shorter than the junction length $L \approx 120$ nm. The superconducting coherence length

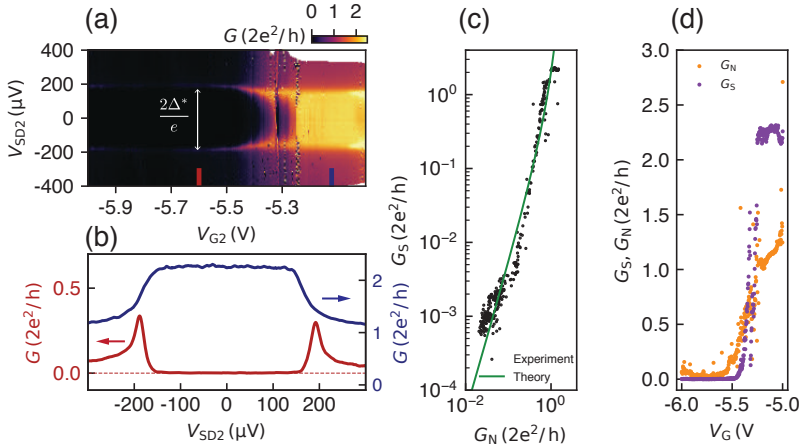


Figure F.1: Si SAG additional tunneling spectroscopy data. (a) Differential conductance dI/dV of device A as a function of gate voltage V_{G2} and source-drain voltage V_{SD2} . Vertical cuts in the tunneling regime (red) and open regime (blue) are shown in (b). To calculate the differential conductance the data was smoothed over 30 steps and the derivative of the current and voltage was calculated numerically. (c) Averaged differential conductance at zero source-drain voltage G_S versus averaged differential conductance at finite source-drain voltage G_N ($-350 \mu\text{V} < V_{SD2} < -250 \mu\text{V}$). The green line is the theoretically predicted conductance in an Andreev enhanced QPC with no fitting parameters (Eq. 2). (d) G_S and G_N as a function of V_{G2} from (a) at $V_{SD2} = -30 \mu\text{V}$ and $V_{SD2} = -350 \mu\text{V}$, respectively.

in this diffusive limit is then $\xi_{\text{diff}} = \sqrt{\hbar D/2\Delta} = 190 \text{ nm}$ [61], with diffusion constant $D = v_F l_e/3$. This implies that the junction is in the short diffusive limit ($l_e < L < \xi_{\text{diff}}$).

F.3 TUNNELING SPECTROSCOPY

In order to compare the differential resistance of nanowire A with the theoretically predicted conductance in an Andreev enhanced QPC (Eq. 2) we repeated the measurement presented in Fig. 6.5a with a DC-setup. The data is smoothed over 30 steps and the differential conductance is calculated numerically. In addition the differential resistance and the voltage drop across the device is corrected for a constant line resistance of $R_{\text{line}} = 4.9 \text{ k}\Omega$ (Fig. F.1). The in-gap conductance G_S and normal conductance G_N are calculated as the average of $G(V_{\text{SD2}})$ in the range $-60 \mu\text{V} < V_{\text{SD2}} < 60 \mu\text{V}$ and $-350 \mu\text{V} < V_{\text{SD2}} < -250 \mu\text{V}$, respectively.

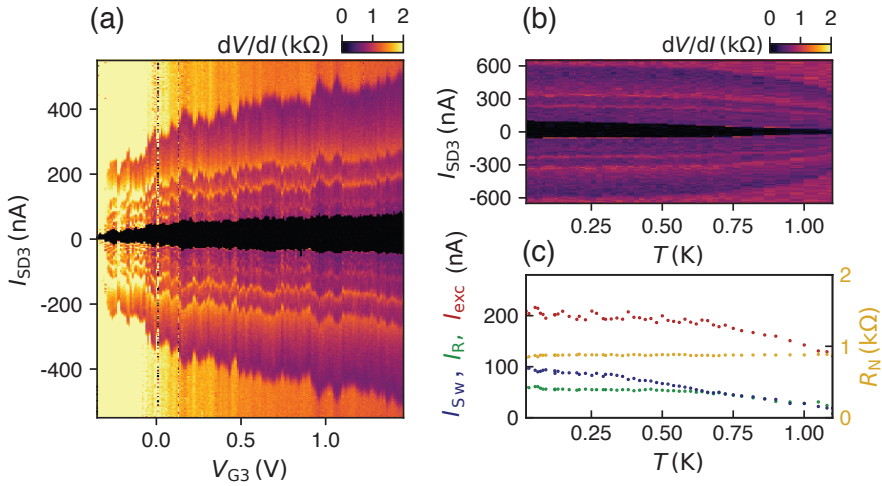


Figure F.2: Si SAG additional Josephson junction data. (a) Differential resistance dV/dI as a function of applied current I_{SD3} and gate voltage V_{G3} at $T = 20 \text{ mK}$ for nanowire C. The dataset is used to extract the junction parameters [see Fig. 6.6(c)]. (b) dV/dI as a function of applied current I_{SD} and sample temperature T for nanowire C at $V_{\text{G3}} = 1.5 \text{ V}$. Switching current I_{SW} , retrapping current I_{R} , excess current I_{exc} and normal state resistance R_{N} extracted from (b).

F.3.1 TEMPERATURE DEPENDENT IV-CURVES

IV-curves at fixed gate voltage $V_{G3} = 1.5$ V were measured and as function of temperature for nanowire C. The data was used to extract values for Fig. 6.6(e).

F.3.2 JOSEPHSON JUNCTION CHARACTERISTICS

The junction characteristics for 6 devices were measured and a summary of extracted values for $V_{G3} = 1.5$ V can be found in table F.1. Here, data in the main part of the paper were taken on nanowire A (Fig. 6.5), nanowire B [Fig. 6.6(a)-(b)] and nanowire C (Fig. 6.6(c)-(d) and Fig. 6.7). All measured devices display similar junction parameters with the exception of device A that shows a non-hysteretic I-V characteristic and device F that has a significantly lower $I_{Sw}R_N$ product. The Z – parameter and junction transparency \mathcal{T} were extracted with the normalized excess current $eI_{exc}R_N/\Delta$ following Ref. [62].

Table F.1: Characteristic Josephson junction parameters extracted for all measured devices at a gate voltage $V_{G3} = 1.5$ V.

nanowire	w (nm)	$I_{Sw}R_N$ (μ V)	$eI_{exc}R_N/\Delta$	I_R/I_{Sw}	Z	\mathcal{T}
A	245	84.6	0.69	0.98	0.71	0.67
B	325	92.1	1.01	0.56	0.57	0.75
C	210	91.5	1.05	0.65	0.55	0.76
D	240	71.8	0.91	0.47	0.61	0.73
E	210	87.2	1.18	0.56	0.51	0.80
F	310	47.5	0.59	0.51	0.75	0.64



Si SAG devices

This appendix presents the pre-growth fabrication of Si SAG devices and the gatemon devices discussed in Chapter 7. Unless stated otherwise, the devices were fabricated at the Niels Bohr Institute (NBI) cleanroom. The proximity error correction (PEC) was performed using the software BEAMER version 5 from GenISys GmbH. The settings for sonication and ashing refer to the Elmasonic P 30 H ultrasonic bath and Diener asher, which are used in the NBI cleanroom. For evaporation an AJA Orion series UHV deposition tool with base pressure 10^{-8} Torr was used.

G.1 MASK PREPARATION

The mask was prepared on 2 inch or 4 inch wafers after the global GaAs/GaP buffer growth.

1. Atomic layer deposition of 5 nm of AlO_x using ALD1 at DTU Nanolab, Denmark. Recipe name: "AL2O3", 50 cycles.
2. SiO_x deposition using plasma-enhanced chemical vapor deposition. using SPTS Multiplex PECVD system at DTU Nanolab, Denmark. Recipe name: "Standard HF SiO2".
3. Growth Mask definition

- Spin coat wafer with CSAR13* with 4000rpm for 45s, bake for 1 min at 185°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose nanowire features with area base dose 430 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 1 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, dwell time: 0.19 $\mu\text{s}/\text{dot}$, PEC: 100% optimal contrast.
 - Expose alignment marks with area base dose 640 $\mu\text{C}/\text{cm}^2$.
100 nm, current: 1 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, dwell time: 0.3 $\mu\text{s}/\text{dot}$, PEC: no PEC.
 - Alternate between exposure of nanowire features and alignment marks to ensure sufficient alignment between layers. Reduce rotation by aligning design relative to major flat using virtual alignment marks.
- Develop resist mask for 24 s in o-xylene solution, develop 5 s in concentrated MIBK, rinse in IPA for 30 s, blow dry with N_2 .
- Oxygen plasma cleaning for 2 min at 100%
- Etch SiO_x and clean wafer
 - Etch SiO_x with III-V RIE at DTU Nanolab, Denmark, recipe: "SiO2_602".
 - Soak wafer in NMP at 85°C for 1 h. Soak and sonicate at 80 kHz, 30 % in acetone, 2-propanol, and MQ for 1, min each. Rinse in flowing MQ for 30 s and blow dry with N_2 .
 - Etch AlO_x in MF321 for 3 min, rinse 1 min in MQ under sonication (80 kHz, 30 %), rinse under flowing MQ, blow dry with N_2 .

G.2 QUBIT DEVICE FABRICATION

1. Cleaning

- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

*13% solids of AR-P 6200 in anisole, from AllResist

2. Al and dielectric mask removal

- Spin coat with maN-2403[†] with 4000rpm for 45s, bake for 1 min at 110°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose areas near nanowires with area base dose 400 $\mu\text{C}/\text{cm}^2$. Details: critical feature size: 100 nm, current: 5 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, pitch: 2, dwell time: 0.02 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing. Expose areas far away from nanowires with area base dose 400 $\mu\text{C}/\text{cm}^2$. Details: critical feature size: 20 μm , current: 100 nA, aperture: 240 μm , write field size: 500 μm , number of dots: 500000, pitch: 10, dwell time: 0.02 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 70 s in MF321 with gentle movement, rinse in MQ for 30 s, blow dry with N_2 .
- Hardbake at 110°C for 30 s on hotplate.
- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50°C. Place one MQ beaker at room temperature.
 - Etch 11 s in 50°C etchant, stir 20 s in 50°C MQ, stir 30 s in room temperature MQ, blow dry with N_2 .
- Hardbake at 110°C for 30 s on hotplate.
- Etch SiO_x .
 - Rinse in 2-propanol and MQ for a few seconds, etch 10 s in ammonium fluoride, stir 11 s in MQ, stir 20 s in second MQ beaker, blow dry with N_2 .
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

3. III-V and Si etch at DTU Nanolab, Lyngby, Denmark

- Spin coat with AZ4533[‡] with 4000rpm for 45s, bake for 50 s at 100°C on hotplate.

[†]from micro resist technology

[‡]from MicroChemicals

- Exposure with MLA100 at Nanolab DTU, Denmark.
Expose areas around nanowires dose: $500 \mu\text{C}/\text{cm}^2$, defoc: 0.
- Develop resist for 2 min in TMAH, stir every 5-10s, rinse in DI for 30s, blow dry with N_2 .
- Dry etch buffer layer and Si
 - Place chip on Si carrier wafer using crystal bond.
 - Etch 3.5 min in III-V ICP with process gases Cl_2 and Ar. Recipe name: "SAGmonMesaEtchRecipe2".
 - Etch 1.5 min in III-V ICP with process gases Cl_2 and N_2 . Recipe name: "SAGmonMesaEtchRecipe1".
- Strip resist in MicroChemicals Photoresist Stripper SH5 at 40°C for 5 min, soak in MQ at 40°C for 5 min, sonicate in SH5 stripper at room-temperature with 30 % at 80 kHz, soak 2 min in acetone, 30 s in 2-propanol, blow dry with N_2 .

4. Junction etch

- Spin coat with A4[§] with 4000rpm for 45s, bake for 2 min at 185°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose with area base dose $2000 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 1 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.125 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist mask for 32 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N_2 .
- Oxygen plasma cleaning for 2 min at 100% power.
- Hardbake at 125°C for 30 s on hotplate.
- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50°C . Place one MQ beaker at room temperature.

[§]4% solids of 950K PMMA in anisole, from AllResist

- Etch 17 s in 50 °C etchant, stir 20 s in 50 °C MQ, stir 30 s in room temperature MQ, blow dry with N₂.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

5. Al evaporation

- Spin coat with EL13[¶] with 4000rpm for 45s, bake for 2 min at 185°C on hotplate.
- Spin coat with A6^{||} with 4000rpm for 45s, bake for 2 min at 185°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose features near nanowires with area base dose 1250 $\mu\text{C}/\text{cm}^2$.
Details for features around nanowires: critical feature size: 10 μm , current: 3 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.026 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
Expose features far away from the nanowires with 1350 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 10 μm , current: 100 nA, aperture: 240 μm , write field size: 500 μm , number of dots: 50000, pitch: 8, dwell time: 0.864 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 32 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100% power.
- Rinse in 2-propanol and MQ for several seconds, etch surface 5 s in ammonium fluoride, stir 10 s in MQ, stir 20 s.
- Evaporate 100 nm Al with rate $\sim 1 \text{ \AA}/\text{s}$.
- Lift-off in room temperature acetone or in 50 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

6. Microwave-control etch

- Spin coat with EL9^{**} with 4000rpm for 45s, bake for 3 min at 185°C

[¶]13% solids of co-polymer (MMA (8.5) MAA) in ethyl lactate, from Kayaku Advanced Materials

^{||}6% solids of 950K PMMA in anisole, from AllResist

^{**}9% solids of co-polymer (MMA (8.5) MAA) in ethyl lactate, from Kayaku Advanced Materials

on hotplate.

- Exposure with Elionix ELS-F125 at 125 kV
 - Expose with area base dose $430 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: $2 \mu\text{m}$, current: 100 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 50000, pitch: 8, dwell time: $0.275 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 32 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N_2 .
- Oxygen plasma cleaning for 2 min at 100% power.
- Hardbake at 125°C for 30 s on hotplate.
- Wet etch Al.
 - Heat up beakers with Transene Al etchant Type D and MQ to 50°C . Place one MQ beaker at room temperature.
 - Etch 24, s in 50°C etchant, stir 20 s in 50°C MQ, stir 30 s in room temperature MQ, blow dry with N_2 .
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N_2 .

7. Gate dielectric deposition

- Spin coat with A4 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose with area base dose $1000 \mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: $120 \mu\text{m}$, write field size: $500 \mu\text{m}$, number of dots: 200000, pitch: 1, dwell time: $0.0208 \mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 32 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N_2 .
- Oxygen plasma cleaning for 2 min at 100% power.
- Atomic layer deposition of 15 nm of HfO_2 using 150 cycles at 110°C , alternating between TDMAH (tetrakis(dimethylamino)hafnium) and water vapor, using 10 h pumpdown preceding deposition.

- Lift-off overnight in acetone at room-temperature or for 2 h in acetone at 50 °C.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

8. PMMA ramp

- Spin coat with A6 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose with area base dose 30 mC/cm².
Details: 100 nm, current: 5 nA, aperture: 120 μm, write field size: 500 μm, number of dots: 200000, pitch: 2, dwell time: 1.5 μs/dot, PEC: 100% uniform clearing.
- Soak 10 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂, inspect.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

9. Topgate evaporation

- Spin coat with EL9 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Spin coat with A4 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose features around nanowires with area base dose 1000 μC/cm².
Details: critical feature size: 100 nm, current: 3 nA, aperture: 120 μm, write field size: 500 μm, number of dots: 200000, pitch: 1, dwell time: 0.0208 μs/dot, PEC: 100% uniform clearing.
 - Expose features far away from nanowires with area base dose 1100 μC/cm².
Details for features far away from nanowires: critical feature size: 10 μm, current: 100 nA, aperture: 240 μm, write field size: 500 μm, number of dots: 50000, pitch: 8, dwell time: 0.704 μs/dot, PEC: 100% uniform clearing.

- Develop resist mask for 32 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100% power.
- Evaporate 100 nm Al with electron beam with rate $\sim 1 \text{ \AA/s}$.
- Lift-off in room temperature acetone or in 50 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

10. Contacts

- Spin coat with EL3 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Spin coat with A6 with 4000rpm for 45s, bake for 2 min at 115°C on hotplate.
- Exposure with Elionix ELS-F125 at 125 kV
 - Expose with area base dose 1200 $\mu\text{C}/\text{cm}^2$.
Details: critical feature size: 100 nm, current: 3 nA, aperture: 120 μm , write field size: 500 μm , number of dots: 200000, pitch: 1, dwell time: 0.025 $\mu\text{s}/\text{dot}$, PEC: 100% uniform clearing.
- Develop resist for 32 s in MIBK:IPA 1:3, rinse in IPA for 30 s, blow dry with N₂.
- Oxygen plasma cleaning for 2 min at 100% power.
- Kaufman milling for 4.5 min with 300 V beam voltage, Ar pressure 1 mTorr, flow 15 sccm, discharge for 5 min and warm up for 2 min before milling.
- Evaporate 100 nm Al with electron beam with rate $\sim 1 \text{ \AA/s}$.
- Lift-off in room temperature acetone or in 50 °C acetone for 2 h.
- Soak 5 min in 1,3-dioxolane, soak 2 min in acetone, rinse 30 s in 2-propanol, blow dry with N₂.

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