Experimental methods for implementing graphene contacts to finite bandgap semiconductors

A dissertation presented
by

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to
The PhD School of Science
in partial fulfillment of the requirements
for the degree of
Doctor of Philisophy
in the subject of

Nano Physics

University of Copenhagen
and
University of Chinese Academy of Sciences
March 2016

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Contents

Abstract

Present Ph.D. thesis describes my work on implementing graphene as electrical contact to finite bandgap semiconductors. Different transistor architectures, types of graphene and finite bandgap semiconductors have been employed. The device planned from the beginning of my Ph.D. fellowship was a graphene-C_{60} monolayer-graphene vertical transistor named the Carbon Burger. The fabrication of such device proved increasingly difficult to achieve and many experimental methods to handle graphene were implemented and improved in attempt to fabricate the Carbon Burger. In the end, a device platform for molecular electronics with parallel CVD graphene bottom electrodes with SiO_2 passivation was successfully fabricated and electronically characterized. A functioning Carbon Burger was not achieved.

Along the work on the Carbon Burger, the scope was broadened and focus was put on implementing graphene contacts to semiconductor nanowires, more specifically, epitaxially grown InAs nanowires. First, we tried a top down method where CVD graphene was deposited on substrate supported InAs nanowires followed by selective graphene ashing to define graphene electrodes. While electrical contact between the nanowires and graphene was achieved, the contact resistance was higher (>100 kΩ) than what is achieved for optimum metal contacts (~5 kΩ). We therefore developed a method to directly grow InAs nanowires on graphitic flakes. This was achieved by using silver seed particles for epitaxial growth of InAs nanowires on graphitic flakes. An added benefit of our growth experiment is that the entire growth system comprising graphitic flakes and nanowires can be transferred to TEM grids for a full TEM analysis of the growth system as a whole. While time did not allow for an electronic characterization of the graphene-nanowire system, the epitaxial interface may provide the ultimate electronic contact between the graphene and nanowires.

Dansk resumé

Nærværende Ph.d. tese beskriver mit arbejde vedrørende implementering af grafen som elektrisk kontakt til halvledere med endelige båndgab. Forskellige transistorer, grafentyper og halvledere med endelige båndgab er blevet forsøgt implementerede. Fra starten af Ph.d. forløbet var det planlagt at fremstille en lodret transistor bestående af grafen-C_{60}-grafen som jeg navngav Karbon Burgeren. Fabrikering af en sådan transistor viste sig at være stadigt vanskeligere og mange forskellige designs og mange forskellige eksperimentelle metoder blev anvendt og forbedrede på vejen mod at fabrikere Karbon Burgeren. Slutproduktet blev en platform til molekylær elektronik med parallelle grafenbundelektroder med SiO_2 passivering. En funktionsdygtig Karbon Burger blev ikke tilvejebragt.

I takt med at arbejdet på Karbon Burgeren skred fremad, udvidede vi horisonten og begyndte at fokusere på implementering af grafenkontakter til halvleder nanotråde i form af epitaktisk dyrkede InAs nanotråde. Først forsøgte vi os med en top-ned metode hvor CVD grafen blev deponeret på InAs nanotråde som lå på et substrat efterfulgt af selektiv foraskning af grafenen for at danne grafenelektroder. Elektrisk kontakt mellem grafen og nanotråde blev opnået, men kontaktmodstanden var væsentligt større (>100 kΩ) end hvad der kan opnås for optimale metalelektroder (~5 kΩ). Derfor udviklede vi en metode til at dyrke InAs nanotråde direkte på grafen og grafit flager. Dette opnåede vi ved at anvende sølv partikeler som katalysator for epitaktisk dyrkning af InAs nanotråde på grafen og grafit flager. En yderligere fordel ved vores dyrkningsmetode er at hele dyrkningssystemet, inklusiv grafen/grafit flage og nanotråde, kan overføres til TEM gitre hvilket muliggør en fyldestgørende TEM analyse af hele dyrkningssystemet. Den begrænsede tid til rådighed muliggjorde ikke elektronisk karakterisering af grafen-nanotråd kontakten. Dog er det ud fra andre tidligere forsøg sandsynligt at den epitaktiske kontakt mellem nanotråde og grafen kan give den ultimative elektriske kontakt mellem nanotråde og grafen.

Acknowledgements

First I would like to thank Sino-Danish Centre for Education and Research (SDC) for funding my Ph.D. including the interesting and educational trips to China. Many people without whom present Ph.D. thesis would not exist deserve a thank you. Indeed I would very much also like to thank my wife Lise Meyer-Holdt, who has been a constant source of support and inspiration. I would also like to thank my friends and family for always being there for fun and support. Among people taking active part in the research or advising I would like to thank my dear friends and collaborators at The National Center for Nanoscience and Technology (NCNST): Rui Wang and Shengnan Wang. We had many joyful hours in the lab and around Beijing. Also from NCNST I would like to thank my friendly collaborators Xiaowei Wang and Xingbin Jiang. I am also deeply grateful for the warm welcome and fruitful discussions with my Chinese supervisor Xiaohui Qiu from NCNST. Also Qingxin Tang from Northeast Normal University, China has been a valuable collaborator. For collaboration on Raman spectroscopy and much valued friendship and conversations I would like to thank Nini Elisabeth Abilgaard Reeler. I would also like to thank my impressively contributing and friendly former students Thomas Kanne Nordqvist, Joachim Elbeshausen Sestoft and Martin Kühnel. My supervisors Bo Wegge Laursen, Peter Krogstrup and Jesper Nygaard indeed also deserve a big thank you for competent guidance through the long and challenging journey that my Ph.D. has been. I would also like to thank Per Hedegård and Charles M. Marcus for their source of inspiration and knowledge. Finally I want to thank all the members of Center for Quantum Devices and Danish-Chinese Center for Molecular Nano-Electronics for being inclusive, friendly and inspiring.

1. Introduction

1.1. State of the art of electronics

Today we have smart phones with much more computing power than all of NASA did when it put the first men on the moon in 1969[1]. And not only is the power available to almost anyone, it comes in a handy device featuring a high resolution and precision touch screen, sensors to precisely record your every movement, antennas and transmitters enabling tracking of orbiting satellites as well as communication with almost any and all other smartphones and computers. If up to the industry, this point in time in no way marks the peak of electronics. During the last year, the biggest computer and electronics companies spend more than 167 billion USD on research and development – the heaviest research and development spending industry of all[2]. The majority of this research still goes into Si based technology. However, this might change.

At the heart of the silicon based technology are the silicon complementary metal–oxide–semiconductor (Si CMOS) transistors. These face fundamental limits in the continued pursuit for smaller devices and faster operation[3]. In CMOS technology size and speed optimization is largely the same, i.e. for several decades faster operation has been achieved by shortening the transistor channel length. As the channel length decreases a main limiter is intrinsic transistor leakage such as drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling[4]. As Roy *et al.*[4] mention, several routes to overcome these limiters within the Si CMOS technology may exist. However, speed and size isn't everything. There is a lot more to be desired from the next generation of electronics. For instance, it could be a 30 inch piece of electronic paper that can show what ever desired, can be folded away in the pocket and is waterproof and durable so it can survive anything from a muddy music festival to a kite surfing trip. While doing all of that it should be environmentally friendly. For this device we need new materials. This thesis is about implementing exactly that: experimental methods for incorporating novel materials in electronic devices.

1.2. Graphene in electronics

In 2004 a new material was born. From birth it came with a high carrier mobility[5] (defined as $\mu = v_d/E$ where v_d is the carrier drift velocity and E is the electric field) of 10,000 $cm^2/V \cdot s$, optical transparency, flexibility, great strength, atomic thickness and the name graphene[6]. This thesis centralizes around graphene implementation in electronic devices. Derived from graphite abundantly present in nature, graphene is potentially cheap and does not put strain on the environment. The carrier mobility value enables near terahertz switching rates of graphene field effect transistors (FETs) with channel lengths on the µm scale[7], see Figure 1 for a schematic of a graphene FET. Such graphene FETs may very well be suited for detection of atoms and molecules adhering to the graphene surface[8] but the non-existing bandgap of graphene yields on-off ratios far below the useful limit of 10^4 - 10^7 for digital logics[9]. Graphene is a zero-bandgap semiconductor so a low on-off ratio in graphene FETs is no surprise and the first solution that popped in to many scientists' heads to increase the ratio was logically to induce a bandgap.

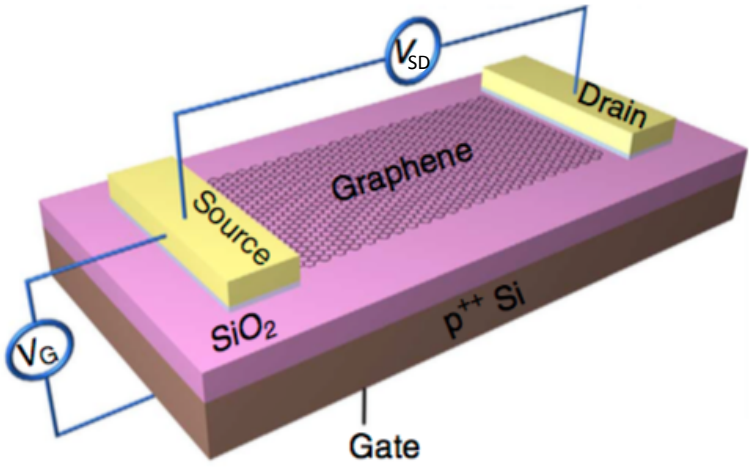

Figure 1. Schematic of a FET with graphene as active semiconductor channel, SiO_2 dielectric material and a p-doped Si gate. Figure adopted from Zhang *et al.*[10]

Bandgap introduction in graphene is possible with a variety of techniques. One technique is quantum confinement introduced in graphene nanoribbons. They do however, suffer from edge state scattering leading to lower carrier mobility[11]. Another candidate is graphene nanomesh with controlled size and position of holes or antidots in the graphene lattice. This can be done by removing[10] or by hydrogenating carbon atoms[12]. Although a full transport gap is theoretically

achievable[13] there is still no high performance graphene nanomesh transistors. Other bandgap engineering methods exist but they introduce significant fabrication complexity and almost always degrade the mobility[14].

1.3. Graphene as electrode

We suggest to work with the existing graphene properties rather than against them by trying to change its zero-gap band structure. We attempt to interface graphene with semiconductors having a suitable bandgap to create novel high performance transistors. In the thesis I present work on implementing graphene in four main devices: a graphene-C_{60}-graphene vertical field-effect transistor (VFET) named the Carbon Burger (Section 4) depicted in Figure 2, a vertical molecular device with metal bottom electrode and graphene top electrode (Section 5), a lateral graphene-nanowire-graphene (G-NW-G) FET (Section 6) and epitaxially grown, silver catalyzed InAs NWs on graphite and graphene (Section 7).

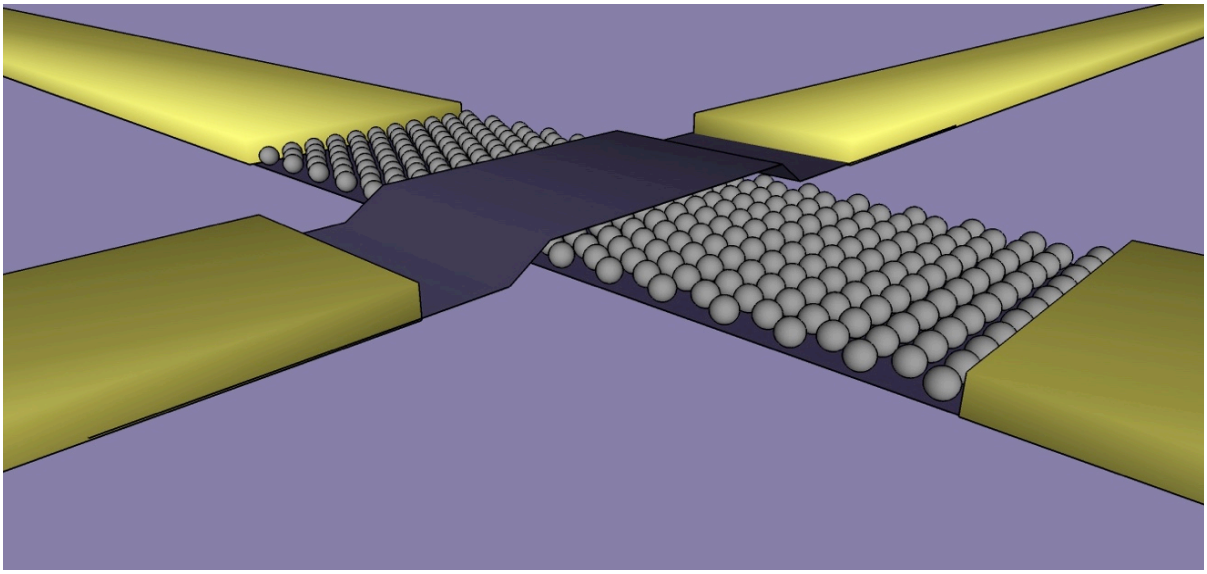

Figure 2. Model of the pure Carbon Burger with gold electrodes. The bright purple background is the SiO_2/Si^{++} substrate, the darker purple sheets are single layer graphene (SLG), the grey balls are C_{60} molecules and the gold coloured slabs are Ti/Au electrodes. Model not to scale.

During my Ph.D. other implementations of graphene as electrode in semiconductor devices emerged. Similar for all studies presented in this paragraph is the use of novel two-dimensional (2D) materials with most of them presented first by

Novoselov *et al.* in 2005[15]. Seven years later, Britnell *et al.*[16] presented the first two vertical field-effect tunneling transistors (Figure 3 a)) very similar to the Carbon Burger. Between the graphene sheets was either a few layer thick crystal of hexagonal boron nitride (h-BN) or molybdenum disulfide (MoS_2) instead of C_{60} as in the Carbon Burger. Transistors showed on-off ratios up to ≈50 with h-BN and close to 10^4 with MoS_2. The paper attracted much attention with 558 citations between February 2012 and August 2015. Later in 2012 Yu *et al.*[17] presented a VFET with a MoS_2 semiconducting channel sandwiched between a graphene source electrode and metal top as seen in Figure 3 c). It exhibits on-off ratios $> 10^3$ and a high current density up to 5,000 A cm^{-2}. The authors furthermore fabricate an elegant vertical logic inverter with both an n- and p-type FET in the stack. Interestingly, the backgate field can effectively penetrate the first FET to also modulate the second FET. In other creative use of the new 2D material family, Lee *et al.*[18] and Yoon *et al.*[19] present flexible and transparent transistors with MoS_2 semiconductor channels and graphene used as either gate in the first study and source drain electrodes in the second. The devices excel not in transistor performance but in taking advantage of the optical and mechanical properties of the novel 2D materials, properties just as intriguing as performance numbers.

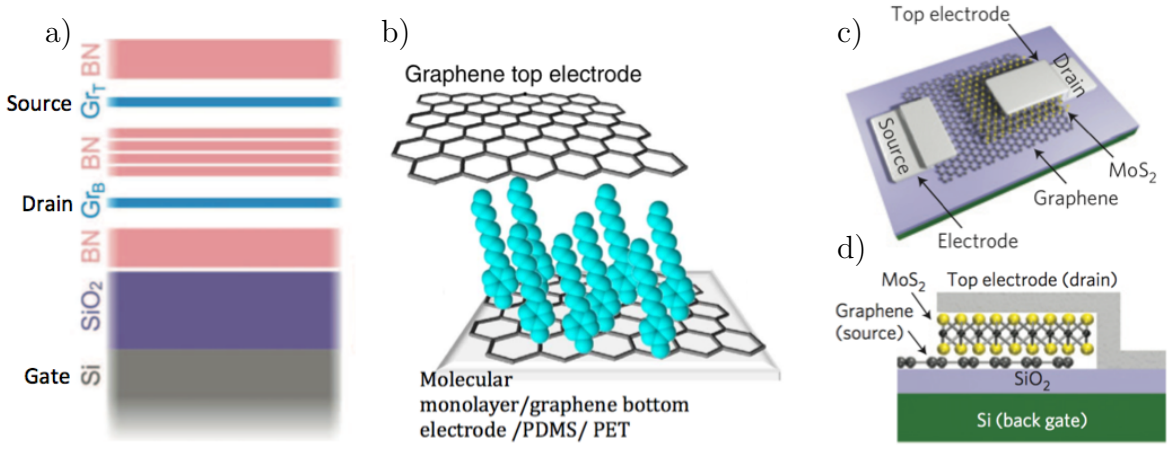

Figure 3. The three most relevant devices presented by others during my Ph.D. In a) is the tunneling VFET with an insulating layer between graphene source-drain electrodes presented by Britnell et al.[16]. Next is the photo-switchable monolayer anchored between graphene electrodes by Seo et al.[20] in b). In c) and d) are the VFETs with MoS2 semiconductor channel, graphene source electrode and metal top electrode by Yu et al.[17]. Figures adopted from respective references.

In 2013, Seo *et al.*[20] demonstrated the combination of a self-assembled monolayer (SAM) and two-terminal graphene top and bottom electrodes as illustrated in Figure 3 b). All devices are fabricated on transparent and flexible substrates. As a control, the authors confirm the dependence of tunneling current on tunneling barrier length with three types of SAMs of varying thicknesses. In their main attraction, the graphene sandwiched SAM can be optically switched between two modes of different conductance to create a transparent photo-switchable transistor. The SAMs are chemically bound to the bottom graphene electrode rendering approximately every ninth graphene carbon atom sp^3 hybridized and thus non-conducting. This could be part of the reason why the authors report a current density orders of magnitude lower than earlier reported insulating SAMs of similar length[21]. I believe deploying bilayer graphene as bottom electrode could largely eliminate the effect. With a switching time of 45 minutes Seo *et al.*'s transistors have no immediate application potential but serves as a nice demonstration of photo switching transistors with graphene electrodes.

1.4. Publications

During my Ph.D. studies I have co-authored three papers:

i) Li, T., Jevric, M., Hauptmann, J. R., Hviid, R., Wei, Z. M., Wang, R., Reeler, N. E. A., Thyrhaug, E., Petersen, S., Meyer, J. A. S., Bovet, N., Vosch, T., Nygård, J., Qiu, X. H., Hu, W. P., Liu, Y. Q., Solomon, G. C., Kjaergaard, H. G., Bjørnholm, T., Nielsen, M. B., Laursen, B. W. & Nørgaard, K. "Ultrathin Reduced Graphene Oxide Films as Transparent Top-Contacts for Light Switchable Solid-State Molecular Junctions". *Advanced Materials* **25**, 4164-4170, (2013).

ii) Wang, R., Wang, S. N., Wang, X. W., Meyer, J. A. S., Hedegård, P., Laursen, B. W., Cheng, Z. H. & Qiu, X. H. "Charge Transfer and Current Fluctuations in Single Layer Graphene Transistors Modified by Self-Assembled C-60 Adlayers". *Small* **9**, 2420-2426, (2013).

iii) Ryuzaki, S., Meyer, J. A. S., Petersen, S., Nørgaard, K., Hassenkam, T. & Laursen, B. W. "Local charge transport properties of hydrazine reduced monolayer graphene oxide sheets prepared under pressure condition". *Applied Physics Letters* **105**, 093109, (2014)

Furthermore I am the first author of a paper, which will be submitted shortly.

iv) Meyer-Holdt, J., Kanne, T., Sestoft, J., Gejl, A., Johnson, E., Nygård, J., Krogstrup, P. "Transferable Graphite Flakes with As-Grown Silver-Seeded InAs Nanowires". *To be submitted*

These papers are referred to as i), ii), iii) and iv) throughout the thesis. My contributions to i), ii) and iv) are described in relevant sections of the thesis. My main contribution to iii) was primarily done during my Master's study and will not be described in further detail here.

1.5. Organization of this thesis

Present thesis is divided into eight chapters including present introduction and a conclusion and outlook. Experimental results on the five different types of devices developed are presented in independent chapters. Each experimental chapter is written as a complete story with relevant experimental methods and relevant theory presented as they become necessary for the understanding of the presented work.

Some results presented in present thesis are also described in my Master's thesis[22]. More specifically, C_{60} spray coating on graphene was developed and described in my Master's thesis. Raman and Atomic Force Microscopy (AFM) characterization of C_{60} thin films with monolayer regions on graphene were done during my Master's study. We established that the morphology of the C_{60} thin film depends on the thickness of the graphene flake the film is deposited on. We used Raman spectroscopy to infer the charge transfer between graphene and deposited C_{60} molecules and saw a small but significant p-doping of graphene upon deposition of C_{60} thin films. This doping effect was also seen in a single, single layer graphene (SLG) FET.

However, during my Ph.D. I have conducted more C_{60} spray coating experiments on graphene in order to optimize the thin film formation as well as to deduct the underlying growth mechanism. I have also performed more Raman studies on C_{60} coated graphene in order to get more statistics on the initial results from my Master's thesis. I have also fabricated many more SLG FETs covered by C_{60} thin films and characterized them in collaboration with my Chinese collaborators.

For coherence of present thesis I present some the results described above from my Master's thesis where they are relevant for the work done during my Ph.D. Whenever results from the Master's thesis is mentioned a citation to it is given: [22].

2. Review of graphene's properties relevant to next generation electronics

This chapter serves as a review of graphene's electronic, mechanical and optical properties and why the material is relevant to implement in future electronic technology. For a thorough derivation of the electronic properties of graphene I refer to a review paper by Castro Neto *et al.*[23].

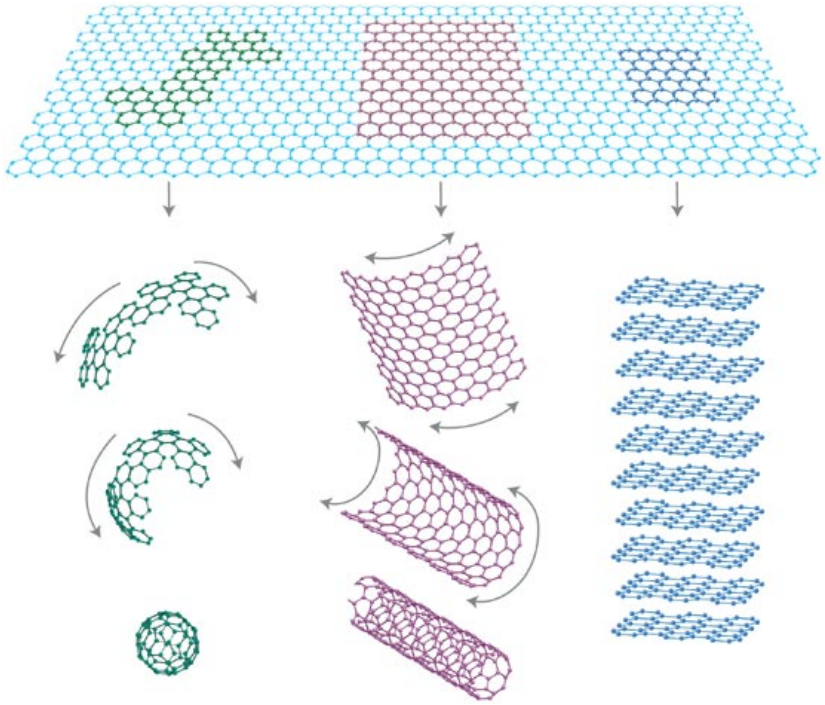

Figure 4. Illustration of the fact that all graphitic allotropes can be derived from graphene. Figure adopted from Geim and Novoselov[24].

2.1. Intrinsic graphene properties

Graphene is a two-dimensional carbon allotrope with a honeycomb lattice and two-atom unit cell as illustrated in Figure 5 a). From graphene all other graphitic allotropes can be derived[24] as illustrated in Figure 4. Graphene is the strongest material ever measured, the thinnest, highly flexible, optically transparent as well as

transparent to electrical fields[24,25]. All carbon atoms are sp^2 hybridized with filled σ bonds responsible for the robustness of the lattice structure and a half filled π bonds conducting the current in graphene[23]. Every atom in graphene is inherently a surface atom and the π bonds responsible for electronic transport live above and below the carbon lattice. This makes electronic transport in graphene extremely susceptible to changes in its immediate environment. In the case where high carrier mobility is desired, the perturbation of the π electrons must be minimized. This can be done by e.g. suspending graphene in vacuum[26] or by depositing it on atomically flat material with no dangling bonds such as h-BN[27]. However, the physical accessibility of the graphene carriers can also be utilized to detect changes in conducted current as even individual molecules are adsorbed on the surface[28]. Graphene has also proven successful at detecting various biomolecules including deoxyribonucleic acid (DNA) when applied in electrochemical sensors[8].

Eigenstates and eigenenergies of graphene

Briefly[23], the Hamiltonian of graphene near the K and K' points of the first Brillouin zone (see Figure 5 b)) remarkably resembles that of massless Dirac Fermions. The solution to the Hamiltonian near the K point is given by

$$\psi_{\pm,K}(\mathbf{k}) = \frac{1}{\sqrt{2}} \begin{pmatrix} e^{-i\theta_{\mathbf{k}}/2} \\ \pm e^{i\theta_{\mathbf{k}}/2} \end{pmatrix}$$

with eigenenergies $E_{\mathbf{k}} = \pm \nu_F \mathbf{k}$ as illustrated in the zoom-in of Figure 5 c) and zero bandgap. Hence, graphene is referred to as a zero bandgap semiconductor. The $\pm$ sign refers to states in the π and π^* bands respectively and $\theta_{\mathbf{k}} = \arctan(q_x/q_y)$, q_x and q_y being the momentum in the x and y direction, respectively.
The solution to the Hamiltonian near the K' point is given by

$$\psi_{\pm,K'}(\mathbf{k}) = \frac{1}{\sqrt{2}} \begin{pmatrix} e^{i\theta_{\mathbf{k}}/2} \\ \pm e^{-i\theta_{\mathbf{k}}/2} \end{pmatrix}.$$

The eigenstates at K and K' are also eigenstates of the quantum mechanical operator for chirality, each with two eigenvalues, one in the direction of the momentum and one against the direction of the momentum. These chirality

eigenvalues are associated with a pseudospin distinct from the spin of the electron. Accordingly, the current in graphene is carried by massless chiral Dirac fermions and have the highest intrinsic mobility of any known material[23].

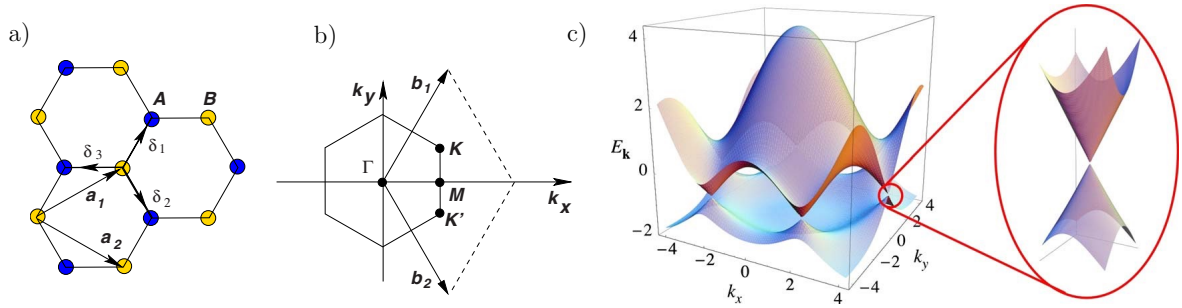

Figure 5. In a) the honeycomb lattice structure of graphene is presented. The unit cell consists of two atoms labeled A and B, the lattice vectors being a_1 and a_2. In b) the first Brillouin zone of graphene with reciprocal lattice vectors b_1 and b_2 as a function of k_x and k_y is presented. In c) the band structure of graphene is presented with a zoom-in on the linear regime found near points *K* and *K'* at the edge of the first Brillouin zone as labeled in b). Figure adopted from Castro Neto *et al.*[23].

2.2. Graphene transistors

In electronics, the extremely high carrier mobility holds promise for very fast switching rates of graphene transistors[5]. However, as discussed en detail below the lack of a bandgap and the difficulty of introducing one have so far hindered the demonstration of graphene FETs with high mobility and an on-off ratio sufficient for implementation in digital logics[9]. As a consequence it is believed that the most important property of graphene for implementation in logic circuits relate to its thickness. This is because the single atom thickness might prove a solution to what is commonly known as short-channel effects in current CMOS technology[3]. In present thesis we focus on utilizing graphene's electrical conductivity as well as flexibility and transparency to photons and electric fields. These properties enable new vertical FETs (VFETs) build with graphene electrodes combined with electrostatically or optically switched channels.

Here I will discuss the importance of different properties of graphene for transistor applications with a focus on VFETs. In general, graphene can be applied in two

types of transistors: radio-frequency (RF) transistors and FETs for logic circuits. This section will only discuss the latter.

2.2.1. State of the art CMOS technology

In 2007, the first graphene metal-oxide-semiconductor field effect transistor (MOSFET) was presented by Lemme *et al.*[29]. But before going in to this and other graphene MOSFETs I will spend some lines on FET basics. A FET consists of a gate and an active semiconductor channel connecting source and drain electrodes as illustrated in Figure 1. An insulating dielectric barrier separates the gate and active channel. Two knobs on a ready-made FET exist: the source-drain voltage V_{SD} and gate voltage, V_G. V_G supplies an electric field tuning the conductance of the active semiconductor channel and thus the current running from source to drain. The FET is turned off when the Fermi energies of source-drain electrodes are aligned with the bandgap of the semiconductor. Conversely the FET is turned on when the Fermi energies of source-drain electrodes are aligned with either the valence band (p-type) or conductance band (n-type). The energy of the states in the channel are raised or lowered relative to the source-drain electrodes by an electric field provided by V_G on an electrostatic gate. V_{SD} is the voltage drop across the semiconductor and thus determines the current as a function of the channel resistance.

Frank Schwierz has written two papers on graphene MOSFETs and their possible application in electronics[3,9]. From these I summarize important figures of merit for logic transistors and why the electronic industry is looking for new materials. For FETs some of these are on-off ratios and switching rates. The on-off ratio is the ratio between the current when the FET is on, I_{on} and off, I_{off}. In Si CMOS technology, logic transistors are designed so that in steady state only the very small I_{off} current runs. This offers ultimately low power dissipation. The battery life and cooling need in any digital device is determined by its power dissipation. For this reason Si CMOS technology has superseded all competing logic technologies. Any successor to Si CMOS technology must have transistors capable of switching off. The rate at witch a FET changes between on and off is called the switching rate. It is determined by how fast the source-drain current can be stopped and started. This is largely determined by the channel length and carrier mobility. The great advances

in Si CMOS switching rates have mainly been achieved by downsizing while the material and thus carrier mobility hasn't improved significantly. With the newest Intel® Core™ i7-5557U Processor the channel length is down to 14 nm. At this scale further downsizing will eventually become impractical. Then higher carrier mobility and thus new materials will be imperative to further performance increase.

2.2.2. Graphene bandgap engineering

Bandgap introduction in graphene is possible with a variety of techniques. One technique is quantum confinement introduced in graphene nanoribbons. Although the confinement successfully introduces a bandgap it also gives rise to significant scattering from edge states[11]. Another technique to obtain a bandgap is by introducing an ordered array of holes or antidots with specific shape, size and density in the graphene plane. This structure is named graphene nanomesh and was first published in 2010 [30]. The co-polymer etching technique used does not leave completely well defined antidots and the achieved mobility is far from that of pristine graphene. If atomic control of also the antidot orientation is achieved it would even enable evasion of Klein tunneling and thus create a full transport gap.[13] Although this is very intriguing there is of yet no experimental technique to obtain this. The antidot lattice was also achieved using selective hydrogenation.[12] Hydrogenation leaves the targeted carbon atoms sp^3 hybridized and thus non-conducting. Successful transfer of the material from the metallic iridium substrate hydrogenation happens on to an insulating substrate such as Si/SiO_2 has proven difficult and has not been achieved since the discovery in 2010. Other bandgap engineering methods exist but they introduce significant fabrication complexity and almost always degrade the mobility and lead to lower switching rates.[14]

2.2.3. Optical and electric field transparency of graphene

The optical transparency of graphene is defined solely by the fine structure constant as $\alpha = e^2/\hbar c$ where e is the electron charge, $\hbar$ is the Planck's constant and c is the speed of light[31]. The resulting 2.3 % absorption of incident photons is although high for a single atomic layer still quite low for transparent electrodes as seen in Figure

6[32]. Here the optical transmission as a function of electrical conductivity is plotted for various transparent and conducting materials. The state of the art is indium tin oxide (ITO) with a maximum visible transmittance of $T \approx 0.81$ at a resistivity of $R_s \approx 3\ \Omega/\square$. The resistivity of single layer graphene is reported at $R_s \approx 200\ \Omega/\square$. The optical transmittance of graphene is $T = 1 - \alpha \approx 0.977$ (graphene reflects <0.1 % of visible light)[31] and decreases linearly for layer numbers less than six[33]. This means that few layer graphene (FLG) six layers thick has larger optical transmittance (~0.86) than state of the art ITO. The shaded region in Figure 6 b) marks theoretical values of optical transmittance and sheet resistance at varying graphene mobility and carrier density. This marks a theoretical possibility of graphene outperforming state of the art ITO in both optical transmission and sheet resistance. The mobility and carrier concentration can be tuned by proper choice of graphene substrate[27,34]. It is thus believed by some that graphene's biggest potential lies in the field of transparent conductive electrodes[35].

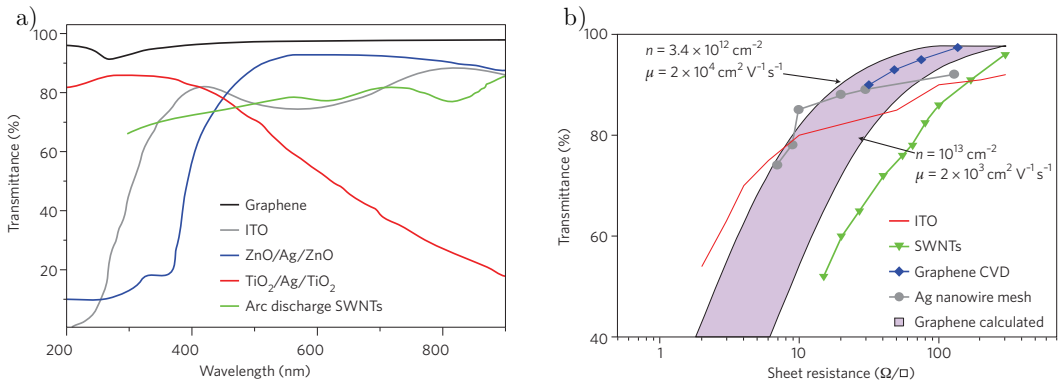

Figure 6. Optical transmittance as a function of photon wavelength a) and as a function of sheet resistance b) compared to alternative materials. Figure adopted from Bonaccorso *et al.*[32].

2.2.4. Vertical graphene heterostructure FETs

Before the discovery of graphene, VFETs did not exist. In VFETs the semiconductor channel is sandwiched between source and drain electrodes (see Figure 2 and Figure 3). This means that the electric field from a top or backgate must penetrate an electrode before it can modulate the chemical potential of the semiconductor channel. Graphene is the first material with high electric conductivity and low enough screening to allow for effective modulation of the sandwiched semiconductor[17].

Relevance of graphene quality

The switching of a graphene VFET happens by bringing the graphene source-drain electrodes in and out of resonance with the conductance or valence band of the semiconductor channel. As mentioned earlier, the mobility is defined as $\mu = v_d/E$ where v_d is the carrier drift velocity and E is the electric field. The higher v_d the faster the current starts and stops when the semiconductor channel is opened or closed. As E is constant, μ determines the switching rate. As graphene is gapless, the graphene electrodes are never depleted of carriers. A carrier in the source graphene electrode enters the semiconductor channel the moment it opens and the electrons stop entering the moment the channel closes. Just like metal electrodes on a Si CMOS FET. Therefore the switching rate of the VFET is independent of the carrier mobility in graphene. However, as described above, heat and current dissipation in electronic devices is extremely important. For graphene VFETs this translates to a desired minimization of inelastic scattering leading to self-heating in the graphene electrodes. As derived independently by Perebeinos & Avouris[36] and Price *et al.* [37] the substrate plays by far the biggest role in self-heating of graphene transistors. Perebeinos & Avouris suggest using a substrate with high thermal conductivity, scaled down insulator thickness and a low graphene/substrate contact thermal resistance. The authors mention h-BN as a promising candidate. Price *et al.* point to remote interfacial phonons in the SiO_2 substrate as a major cause of heat dissipation. They theoretically compare graphene on h-BN, silicon carbide (SiC), SiO_2 and hafnium oxide (HfO_2) and find the lowest surface polar phonon scattering for graphene on h-BN, slightly higher than for suspended graphene. Both papers thus point towards h-BN as the optimum substrate for graphene FETs. This is confirmed by the unprecedented high carrier mobility of graphene on h-BN when compared to any other supported graphene FETs[27,38].

3. Graphene transistors modified by self-assembled C_{60} thin film

In the first part of the Ph.D. project a lot of my efforts went into depositing C_{60} thin films on graphene in our efforts towards creating a vertical FET with a C_{60} thin film sandwiched between graphene source-drain electrodes described in Chapter 4. To characterize the molecule/graphene interactions I fabricated and characterized C_{60} covered graphene FETs in close collaboration with then Ph.D. fellows Shengnan Wang, Rui Wang, Xiaowei Wang and professor Xiaohui Qiu in Beijing. To get the most information from the FETs, Rui and Xiaohui (mainly) came up with the idea of measuring current flicker noise in the same graphene FETs before and after C_{60} deposition. This chapter is about the resulting paper[ii)] to which my main contributions are development and understanding of C_{60} deposition on graphene, Raman spectroscopy analysis of graphene with and without C_{60} and discussion of flicker noise analysis and interpretation.

3.1. Introduction

As all atoms in graphene are surface atoms it is extremely sensitive to changes in its immediate environment. Moreover, the low density of states at the Dirac point and intrinsic low current noise enables detection individual adsorbed molecules[28]. However, as described below the effect of C_{60} molecules on graphene is detectable though small when characterized by Raman spectroscopy and FET characterization. Also, scanning tunneling microscopy (STM) studies by Cho *et al.*[39] and Zhou *et al.*[40] show very small charge transfer between adsorbed C_{60} molecules and graphene on silicon carbide and ruthenium. To get a clearer signature we study how C_{60} adlayers changes the current flicker noise in graphene FETs combined with Raman spectroscopy and direct current (DC) measurements. Flicker noise usually induced by environmental perturbations arises from fluctuations in source-drain current and is significantly enhanced in devices with low carrier density[41,42,43,44]. Flicker noise is a general term used for all types of source-drain current fluctuations that show a $1/f^{\alpha}$ dependency and may arise from such different underlying phenomena as

quantization of charge in low current samples to trapping and detrapping from surface states[41]. By quantitative analysis of flicker noise, the underlying phenomena may be deduced. Here the method is deployed to prove itself as a standard for detecting even weakly interacting species on graphene.

3.2. C_{60} spray coating

As a prerequisite for the study of charge transfer between C_{60} and graphene we studied C_{60} thin film formation on mechanically cleaved graphene and highly oriented pyrolytic graphite (HOPG)[22]. We used a C_{60} spray coating technique developed for HOPG[45] and extended it to C_{60} on graphene during my Master's study[22]. Spray coating is done from a nebulizer* mounted approximately 20 cm above the sample to be spray coated. The nebulizer is tilted slightly away from the vertical direction and sprays microliter droplets of C_{60} dissolved in toluene onto the sample, where the droplets dry up to form C_{60} thin films with thicknesses down to a single layer. Spraying times of 5-20 seconds were generally used.

During my Master's[22] we established a layer dependent C_{60} thin film formation on graphene. That is, with increasing thickness of graphene flake we had increasing C_{60} coverage and monolayer/multilayer ratio as seen in Figure 7 c). In addition, we studied C_{60} deposition on several both n-doped and p-doped graphene samples (NG and PG) in Figure 7 c) and Figure 7 d), respectively[22]. P-doped graphene was achieved by deposition on SiO_2 while graphene on NH_2-silane modified SiO_2 yielded n-doped graphene as showed previously by Wang *et al.*[34]. As showed in Figure 7 c) and Figure 7 d) we see very similar C_{60} thin film formation with monolayer regions on both n- and p-doped graphene. This illustrates the small effect of graphene doping level on thin film formation.

Possible reasons for layer dependent growth

My Master's thesis[22] did not contain a detailed explanation of the possible origin of layer dependent C_{60} thin film growth on graphene. This explanation is derived in this thesis. The C_{60} is dissolved in toluene when sprayed on the graphene surface. As the droplet dries up a C_{60} thin film is formed on the graphene interpreted as due to

* A commercially available Meinhard nebulizer TR-30-K1 connected to an argon gas supply (p = 2 bar).

a capillary flow on the sample surface[45]. We do not investigate the exact kinetics and mechanism of the drying droplet and C_{60} thin film formation. However, the following arguments serve as a plausible, though not necessarily complete or concluded explanation. The evaporation rate of a drying droplet has been shown to influence the morphology of the deposited thin film[46]. The evaporation rate strongly depends on the droplet contact angle[47] and thus the wettability of the surface. Graphene exhibits wetting transparency decreasing with the number of graphene layers[48] indicating a different contact angle between toluene and SLG and BLG on SiO_2. In addition, it is possible that the relatively higher roughness of SLG than BLG on SiO_2 affects the C_{60} thin film growth[49]. In any case, for this particular study we use SLG FETs with no BL regions and thus do not see layer dependent growth on our transistors.

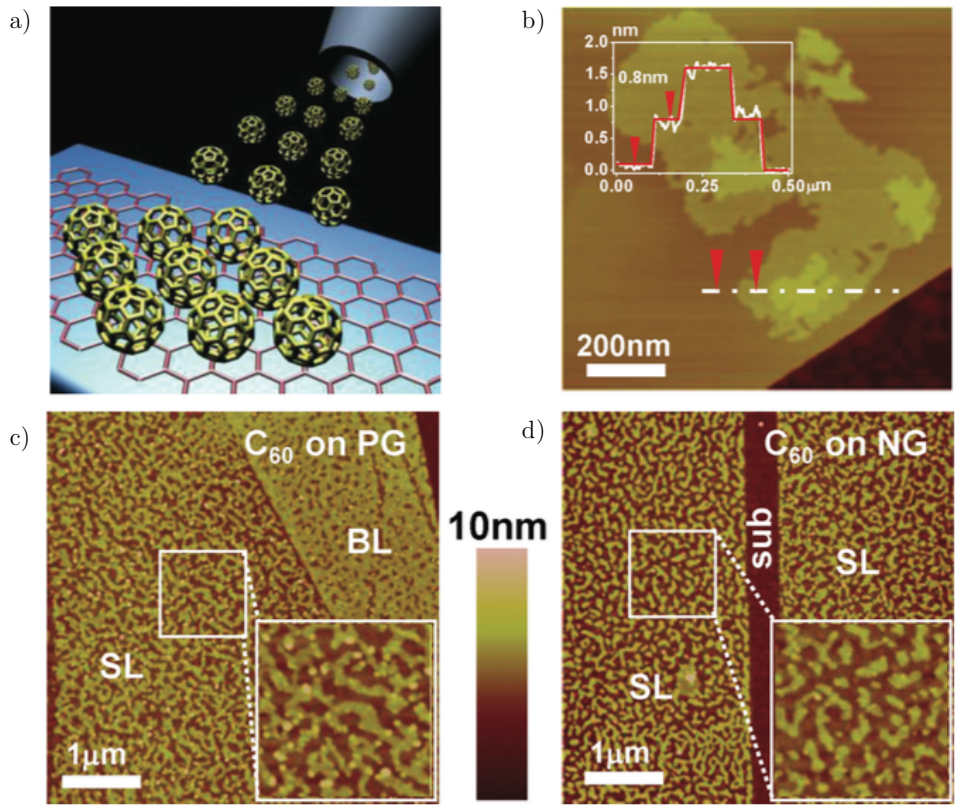

Figure 7. C_{60} spray coating. In a) is a schematic of C_{60} spray coating from a nebulizer onto a SiO_2 supported SLG. b) is an AFM image of a C_{60} island formed on HOPG by spray coating. c) is an AFM image of C_{60} thin film on p-doped SLG and BLG regions, note the much more coherent C_{60} film on the BLG region as compared to on the SLG region. The AFM image in d) shows a C_{60} thin film on n-doped SLG with a morphology similar to that observed on p-doped SLG. Figure adopted from ii).

3.3. Graphene to C_{60} charge transfer studied by Raman spectroscopy

The majority of the Raman spectroscopy on C_{60} coated graphene was done during my Master's thesis[22]. This section serves as a review of those results as they are relevant for the noise experiments presented in section 3.6. Raman spectroscopy is a powerful tool for characterizing carbon materials capable of determining graphene layer number, defect content, doping level and intrinsic stress[50]. In short, Raman spectroscopy relies on inelastic scattering between probing photons and sample phonons. The Raman spectrometer then detects reflected photons having interacted with the sample[†]. From the difference in energy between probing photons and reflected photons, allowed phonon excitations are deduced. Because a change in phonon states in graphene causes a change in electronic states in graphene, Raman spectroscopy is able to provide information about electronic states of graphene as well.

Figure 9 summarizes the Raman peaks observed before and after deposition on p-doped graphene (PG) and n-doped graphene (NG). The top graph in Figure 9a) shows the Raman spectrum recorded on a C_{60} micron sized crystallite deposited on SiO_2. The peak positions matches the values recorded by Kuzmany *et al.*[51] for C_{60} ~1426 cm^{-1} (Ag(2)), ~1426 cm^{-1} (Hg(7)) and ~1574 cm^{-1} (Hg(7)). We therefore conclude that we have indeed C_{60} on the substrate. However, in the spectra recorded on C_{60} covered NG and PG below we do not clearly see the C_{60} peaks resolved. This is must likely due to the very small amount of C_{60} in the probed areas[22]. We then turn our attention to the charge transfer between C_{60} and graphene. A systematic study by Das *et al.*[52] correlates the doping level of graphene with phonon spectra recorded by Raman spectroscopy. To infer the doping level of graphene, Das *et al.* analyze G peak position Pos(G), 2D peak position Pos(2D), G peak full width half maximum (FWHM) and the intensity ratio of the 2D and G peak I(2D)/I(G) as plotted in Figure 8 and correlate these values with the doping level of the studied SLG. In the following we use said correlation to infer the graphene doping level from Raman spectrum analysis.

[†] The Raman spectrometer filters out reflected photons with a wavelength similar to the wavelength of probing photons.

In Figure 9 a) we plot Pos(G) and I(2D)/I(G) for a PG sample and an NG sample before and after C_{60} deposition. To unambiguously determine the doping effect by means of Das *et al.*'s analyzes[52] one needs the initial graphene doping level. These are predicted by earlier work on NG and PG prepared exactly the same way[34]. In Figure 9 b) we do statistical analysis of Raman spectra on five NGs and five PGs. We observe G peak blue shift for C_{60} covered PG and red shift for C_{60} covered NG. Additionally, I(2D)/I(G) decreases for C_{60} covered PG and increases for C_{60} covered NG. Comparing with the results of Das *et al.*[52] we qualitative conclude that C_{60} p-dopes both NG and PG[22]. The conclusion is consistent with results from studies on C_{60}/carbon nanotube and C_{60}/reduced graphene oxide heterostructures[53,54]. To further infer the charge transfer between C_{60} and graphene we fabricate NG and PG FETs and characterize them before and after C_{60} deposition described below.

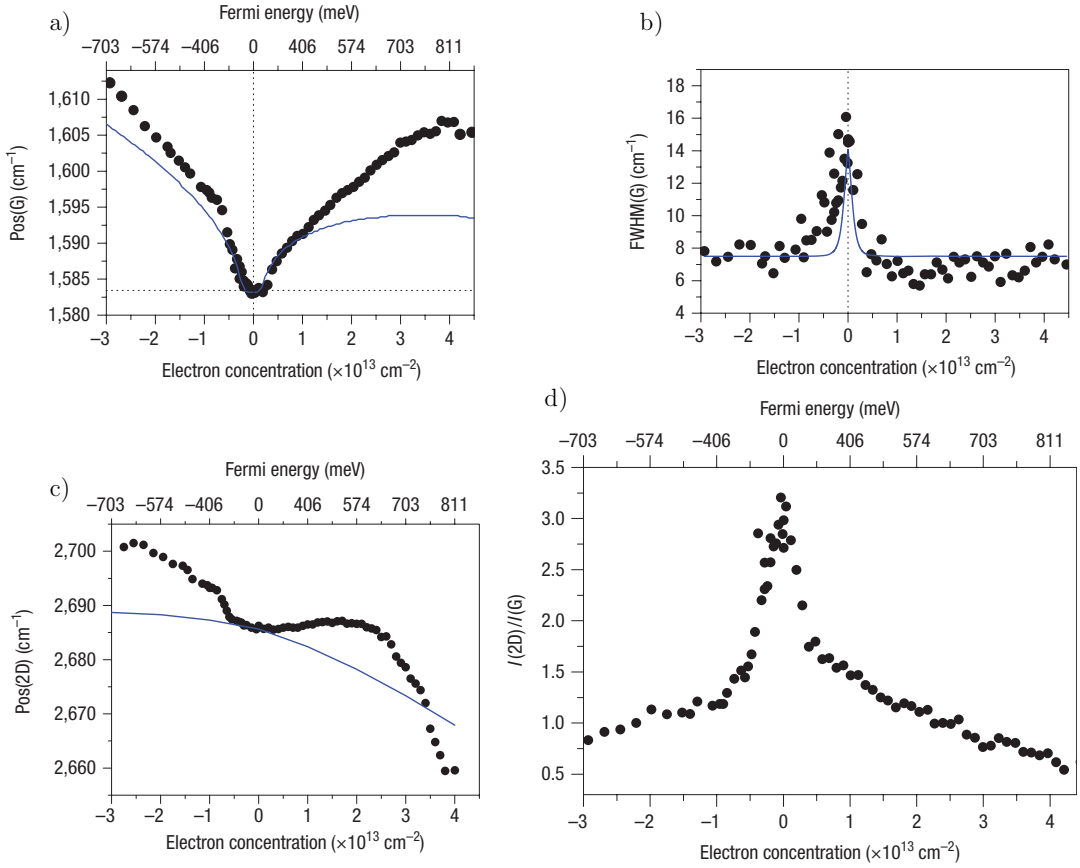

Figure 8. Various Raman peak figures of merits are plotted against graphene doping level. Recorded data is plotted as dots while theoretical predictions are plotted as lines. In a) the recorded G peak position is plotted, in b) it is the full width half maximum (FWHM) of the G peak position, in c) it is the position of the 2D peak (Pos(2D)) and in d) it is the intensity ratio between the 2D peak and the G peak (I(2D)/I(G)). Figure adopted from reference [52].

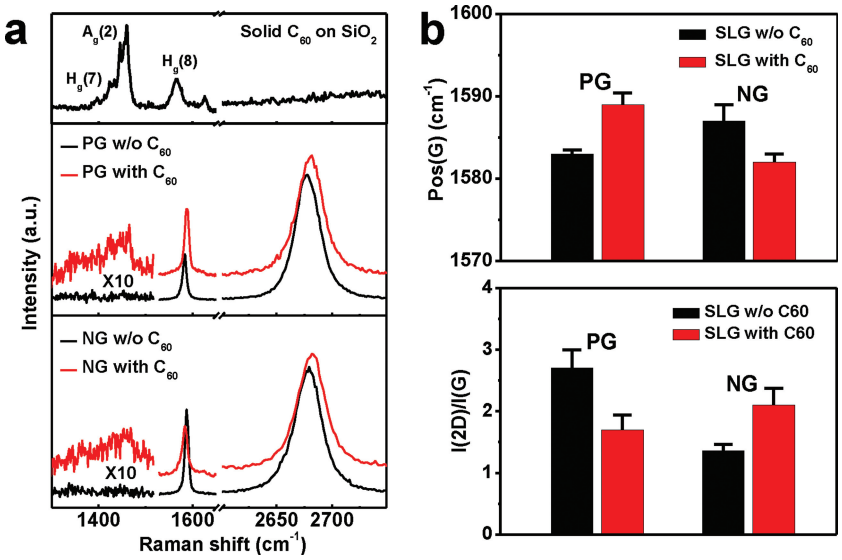

Figure 9. Raman spectrum analysis. In a) we plot recorded Raman spectra. In the top panel is a spectrum recorded on solid C_{60} on SiO_2, peaks associated with C_{60} are labeled. In the middle panel a spectrum recorded on PG without C_{60} (black line) and spectrum recorded on PG with C_{60} (red line) are plotted. The bottom panel shows a spectrum recorded on NG without C_{60} (black line) and spectrum recorded on NG with C_{60} (red line). The top panel in b) compares the G peak position recorded before (black) and after C_{60} deposition (red) for five NG samples and five PG samples, while the bottom panel compares the intensity ratio between the 2D peak and the G peak (I(2D)/I(G)) for five PG samples and five NG samples. Figure adopted from ii).

3.4. Graphene transistor fabrication

The objective of studying SLG FETs is to infer the doping effect of C_{60} on PG and NG by fabricating and electronically characterizing PG and NG FETs before and after C_{60} deposition. We first mechanically exfoliate graphene/graphite[31] on a doped Si wafer with 285 nm thermally grown SiO_2 for optimum visibilty[55] and gate response. Before deposition, the wafers are oxygen plasma ashed for 5 minutes. SLGs are located with an optical microscope and with Raman spectroscopy we confirm single layer flake thickness[56]. We then define thermally evaporated Cr/Au (5 nm/40 nm) source drain electrodes using standard e-beam lithography. After lift-off we anneal the devices above 120° C in vacuum for three hours to remove water and other solvent residues. A standard device is depicted in Figure 10 with an overview to the left and a zoom-in on the contacted SLG to the right.

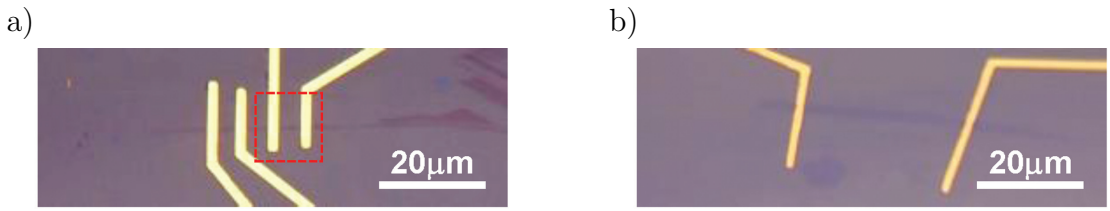

Figure 10. Optical images of a representative SLG FET with an overview in a) and zoom-in in b). The substrate is a doped silicon wafer with 285 nm of thermally grown SiO_2. Images adopted from ii).

3.5. SLG FETs with and without C_{60} adlayers

3.5.1. Measurement setups

The device characteristics of our SLG FETs were measured in a liquid helium cooled 4-probe station at ~10^{-6} mbar. To vary the temperature during measurements we deployed a Lakeshore 331 temperature controller with temperature fluctuations <0.1 K. For DC measurements we used a Keithley 4200SCS to supply a source drain bias (5-50 mV) and gate voltage (-80–80 mV). When using the electrical noise as a probe it is important to minimize external 50 Hz noise sources. Therefore for these measurements the source drain bias is supplied by a dry battery connected *via* a voltage divider. The current through the SLG FET was amplified by a low noise preamplifier and recorded by a Labview controlled acquisition card connected to a battery driven laptop.

3.5.2. DC measurements on pristine and C_{60} covered SLG FETs

To further investigate the charge transfer between graphene and deposited C_{60} molecules we perform DC measurements with gate sweeps on SLG FETs as the one presented in Figure 10. Figure 11 a) and b) show device characteristics for two representative SLG FETs before and after C_{60} deposition. The measurements are performed on NG in a) and PG in b) with constant source-drain voltage, V_{sd} and varied gate voltage, V_g. The resistance maximum indicates the gate voltage at which the carrier concentration in the SLG FET is at a minimum i.e. the chemical potential is at the Dirac point. We label this gate voltage the Dirac voltage, V_{Dirac}.

NG before C_{60} deposition has V_{Dirac} = -60 V and C_{60} deposition changes it to V_{Dirac} = -42 V. For PG we have V_{Dirac} = 50 V and V_{Dirac} = 58 V, respectively. From these numbers we can immediately conclude that C_{60} molecules accept electrons from both NG and PG. Also, C_{60} molecules accept more electrons from NG than from PG. Quantitatively we can calculate the carrier concentration n from V_{Dirac} and V_G as $n = \alpha \left| V_g - V_{Dirac} \right|$, where $\alpha = 7.2 \cdot 10^{10}$ cm^{-2}/V is a constant related to the geometrical capacitance[5]. The doping effect in units of energy (chemical potential, ς) can be deduced from the carrier concentration by the relation $\varsigma = \hbar v_F \sqrt{\pi n}$, where $v_F = 1.1 \cdot 10^6$ m/s is the Fermi velocity in graphene and $\hbar$ is the Planck's constant[5,52]. The chemical potential shift at $V_g = 0$ is thus $\varsigma = \pm \hbar v_F \sqrt{\pi \alpha \left| \pm V_{Dirac} \right|}$. Before C_{60} deposition this is $\varsigma \approx$ -267 meV for NG and $\varsigma \approx$ 244 meV for PG. The chemical potential shifts due to C_{60} deposition at $V_g = 0$ is $\varsigma \approx$ -146 meV for NG and $\varsigma \approx$ -97 meV for PG. These results are consistent with the Raman results showing that C_{60} accepts electrons from both NG and PG. Also, we see that more electrons in NG can overcome the transfer energy barrier to C_{60} than in PG. An earlier theoretical calculation along with a more recent STM study shows that the Dirac point of graphene lies much closer to C_{60}'s lowest unoccupied molecular orbital (LUMO) as compared to its highest occupied molecular orbital (LUMO) predicting p-doping[39,57]. The graphene carrier density change is estimated as $\Delta n = \alpha V_{Dirac} \approx 0.6 \cdot 10^{12}$ cm^{-2} for PG and $\Delta n \approx 1.3 \cdot 10^{12}$ cm^{-2} for NG. With approximately one C_{60} molecule per 80 nm^2 in a close packed hexagonal lattice[45,58] this gives ~0.01 electron accepted by each C_{60} molecule on average. Before turning to the current noise analysis we note that C_{60} deposition does not introduce a significant bandgap in graphene as evidenced by the linear I/V plots before (black circles) and after (red circles) C_{60} deposition as shown in Figure 11 c). This small amount of charge transfer agrees with the earlier reported weak coupling between C_{60} and graphene reported in an STM study by Cho *et al.*[39]

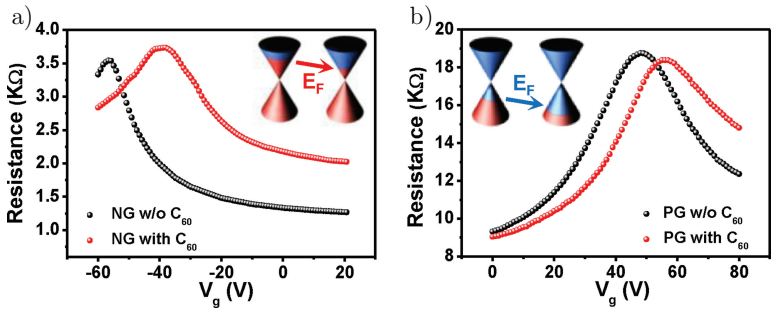

Figure 11. Gate sweeps of an NG FET in a) and a PG FET in b) before C_{60} deposition (black dots) and after C_{60} deposition (red dots). Figure adopted from ii).

3.6. Current fluctuations in single layer graphene transistors

To further investigate the dynamics of charge transfer between C_{60} and graphene we analyze the source drain current noise, $\partial I(t)/I$ in graphene FETs before and after C_{60} deposition. More specifically, we investigate flicker noise or $1/f$ noise[42,59] as a function of temperature. The analysis eventually leads to determine the nature of the added noise by C_{60} and help us understand the C_{60}-graphene interactions. $1/f$ noise has previously been deployed to understand noise in several devices including liquid-gated graphene FETs[60], FETs with graphene of varying thickness and defect density[61] and single walled carbon nanotubes[62]. Whereas these and other records mainly focused on understanding $1/f$ noise to find methods to minimize it, we investigate $1/f$ noise to better understand the C_{60}-graphene interaction and to explore the relevance of $1/f$ noise as a probe to detect absorbents on graphene FETs.

Current noise in graphene FETs

Before we investigate the effect of C_{60} we present the framework for analyzing noise measurements on bare graphene FETs as those presented in Figure 12. The first measurement presented in Figure 12 a) is the traditionally reported source drain current, I_d and resistance, R_d as a function of gate voltage, V_G. From this we can establish the Dirac voltage, V_{Dirac} = -18 V and the intrinsic graphene doping level, ς as described above. We then measure the current at constant gate voltage, V_g and source-drain voltage, V_{sd} in 10 seconds intervals. To quantize the current noise we define the parameter $\partial I(t)/I$, where $\partial I(t)$ is the instantaneous current at any given time, t and I is the current averaged over the time interval. We plot $\partial I(t)/I$ for five

different values of V_g in Figure 12 b). The curves are separated by an offset for clarity. The current fluctuations are largest for the curves recorded at $V_g = 0$ V and V_g = -30 V. Remembering that V_{Dirac} = -18 V tells us that these are the curves recorded at lowest carrier concentration. This is qualitatively in accordance with Hooge's empirical relation $A = \frac{\alpha_H}{N}$, where A is the noise amplitude, α_H is the device specific Hooge's parameter and N is the total number of carriers[41,59,62].

To further analyze the noise data we turn our attention to the frequency dependency of the current noise. More specifically, we calculate the spectral density function, $S_I(f)$ of the current with respect to frequency. $S_I(f)$ is a quantitative measure of the amount of variance contributed to *I(t)* by noise of frequency f. Hooge's empirical relation tells us that[41,59,62]

$$\frac{S_I(f)}{I_d^2} = \frac{\alpha_H}{Nf^\beta} = \frac{A}{f^\beta} \qquad (1)$$

with $\beta \approx 1$ indicating $1/f$ noise behavior. To observe this dependency on f we normalize the spectral density function and plot $S_I(f)/I^2$ as function of f in a double logarithmic plot in Figure 12 c). The color code corresponds to the same gate voltages as in Figure 12 b) and the dashed plot line in c) indicates the slope expected for $1/f$ dependency, which is parallel to linear fits of all measurements in c). Fits of equation 1 to the data in c) gives $\beta = 1 \pm 0.2$ and we conclude that we do indeed have $1/f$ noise. We also extract the noise amplitude A from the fits and plot it as a function of gate voltage, V_g in Figure 12 d). The "$\frown$" shaped curve confirms Hooge's relation predicting the noise amplitude being inversely proportional to the carrier concentration. This behavior is consistent with graphene's observed ability to screen charged impurities at different gate voltages[63].

Effect of C_{60} on room temperature noise in graphene FETs

Having established the nature of current noise in pure graphene FETs we expand our scope to include the effect of C_{60} on the current noise. In Figure 13 a) we plot the normalized noise spectral density functions, $S_I(f)/I^2$ at the Dirac voltage for the same graphene FET before and after C_{60} deposition. In both cases we observe $1/f$ behavior. Interestingly, fits to equation 1 show that the amplitude, A decreases 2-3

times when C_{60} is deposited. In contrast, a previous report by Kaverzin *et al.*[64] showed that the addition of water molecules to bare SLG FETs significantly increased the noise amplitude.

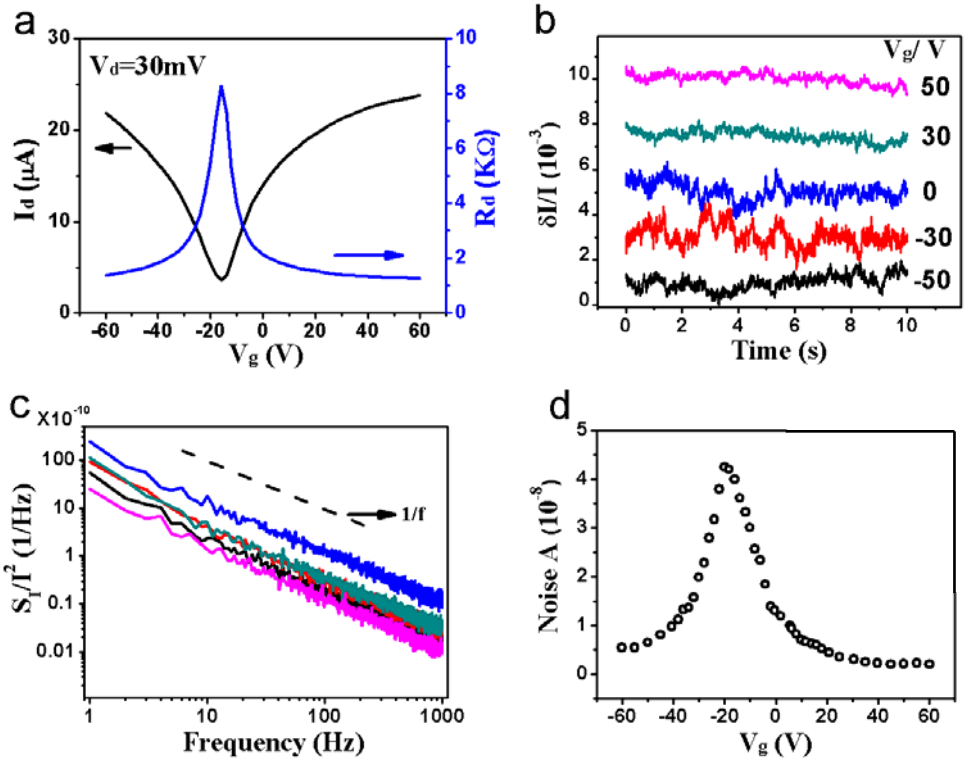

Figure 12. All data in this figure is recorded on a pristine graphene FET at room temperature. In a) we plot source drain current, I_d (black) and resistance, R_d (blue) as a function of gate voltage, V_g. b) is current fluctuations, $\partial I/I$ recorded for 10 seconds at various gate voltages. c) is the normalized spectral density, $S_I(f)/I^2$ of the measurements in b) with the same color code and a dashed line indicating the slope of $1/f$ dependency. d) shows the noise amplitude, A as a function of gate voltage, V_g. Adopted from ii).

To further investigate the effect of C_{60} we plot the room temperature gate dependence of the noise amplitude before and after C_{60} deposition in Figure 13 b). Without C_{60} the "⌒" shaped curve consistent with Hooge's relation is observed just as observed for the device in Figure 12 d). However, the addition of C_{60} completely changes the gate dependency to form an "M" shaped curve. The amplitude is no longer a monotonic function of carrier concentration. A noise minimum at the Dirac voltage is flanked by two local maxima beyond which the noise amplitude decreases again. The behavior is somewhat reminiscent of the results obtained on disordered[61] and liquid gated graphene transistors[60]. This suggests the presence of spatial charge inhomogeneity and time dependent charge fluctuations in the vicinity of the graphene channel. Hooge's empirical relation fails to account for the "M" shape

behavior as the parameter, α_H changes as a function of carrier density. The clear difference in noise characteristics before and after C_{60} deposition is far more noticeable than the relatively small effect of C_{60} on graphene doping level. The noise analysis thus shows potential as a probe to detect even weakly interacting species adsorbed on graphene.

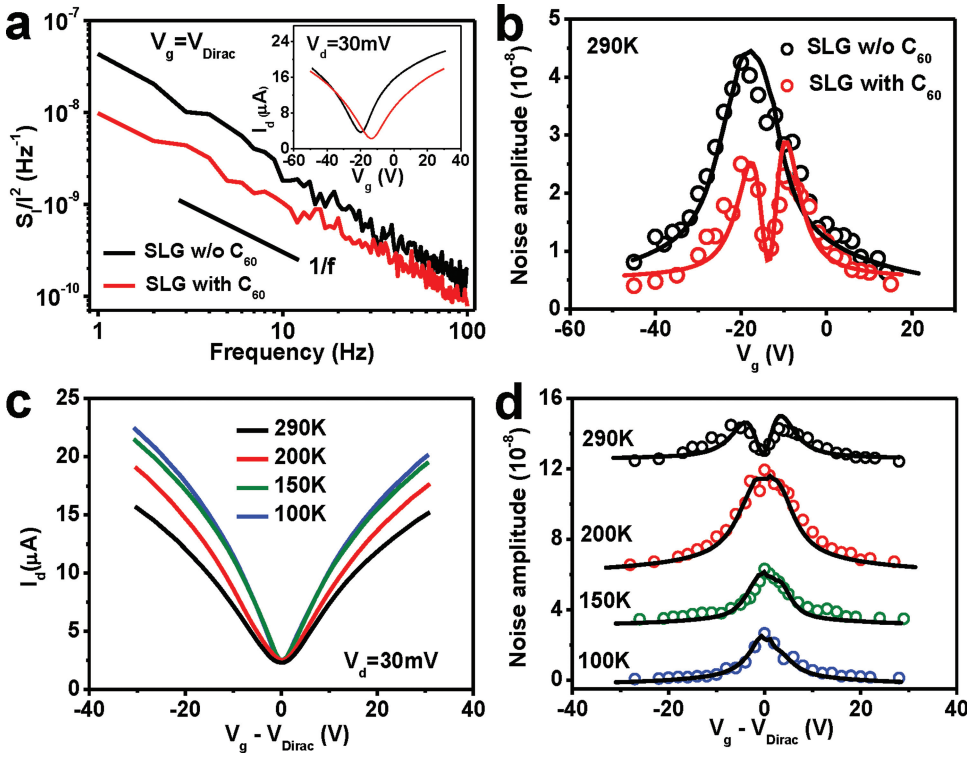

Figure 13. In a) we plot $S_I(f)/I^2$ at the Dirac voltage for the same graphene FET before (black) and after C_{60} deposition (red). The inset shows their respective gate sweeps. b) is the noise amplitudes plotted before (black circles) and after C_{60} deposition (red circles). c) and d) show current and noise amplitude, respectively as a function of $V_g - V_{Dirac}$ for a C_{60} covered graphene FET at different temperatures. The datasets in d) are vertically offset. The solid lines in b) and d) are fits based on equation 2. The figure is adopted from ii).

Temperature dependence of noise modification in graphene FETs

In order to further explain the noise behavior of our devices we cooled down and characterized a C_{60} covered graphene FET. At various temperatures we recorded the current and noise amplitude as function of gate voltage plotted in Figure 13 c) and d), respectively. We plot I_d vs. $V_g - V_{Dirac}$ to ease comparison. An apparent feature is that the minimum conductance at V_{Dirac} does not change for the plotted temperatures ranging from 100 K to 300 K. The implication that the mobility at V_{Dirac} is temperature independent is consistent with long-range Coulomb scattering

dominated transport according to a theoretical work by Adam *et al.*[65]. In contrast, the sub-linear I_d/V_g plot at room temperature becomes more linear with decreasing temperature as shown in Figure 13 c). The causes of the sub-linearity are contact resistance and short-range scatterers such as natural point defects and phonons. Effects that are both suppressed with decreasing temperature are thus the linear I_d/V_g plot is restored at lower temperatures[66].

Let us now turn to the temperature dependency of the noise amplitude, A as plotted in Figure 13 d). The gate dependence changes completely from an "M" shape at 290 K to a slightly perturbed "$\frown$" shape at 100 K. The low temperature curve thus resembles the noise characteristics before C_{60} deposition. While the transition temperature various significantly from device to device it usually appears at moderately low temperatures of 150 K or above which is consistent with other findings[61,64,67]. To interpret our results we deploy a two-level model. Professor Per Hedegård developed this model in collaboration with Rui Wang for the purposes of present study. The starting point of the model is one energy level on graphene and one on individual C_{60} molecules. The probability of an electron jumping between levels is temperature dependent due to thermal excitations. Such an event changes the channel carrier concentration and thus current. An added effect is that an electron absorbed by a C_{60} molecule acts as a scattering center or local gate to the graphene channel and gives rise to graphene carrier mobility modulation. Pal *et al.*[61] recently developed a similar model to explain the noise behavior of transistors with graphene of different thickness and quality[61]. We assign the total of current noise to two components: firstly, charge transfer between graphene and its immediate environment such as fullerene molecules or SiO_2 charge traps. The change leads to carrier exchange noise, N_{ex} in the graphene channel yielding a term $N_{ex} \sim (d(\ln(I_d))/dV_g)^2$. Secondly, there are random scatterings induced by long-range Coulomb scattering and short-range scatterers such as phonons or lattice defects. This type of noise is governed by the screening capability of graphene and gives the term $N_{sc} \sim \left|V_g\right|^{\gamma}$, similar to Hooge's empirical relation with the complexity that γ depends on band structure and scattering type. Considering graphene, $\gamma > 0$ for short-range scattering and $\gamma < 0$ for long-range Coulomb scattering[61,64]. The total normalized noise amplitude is thus

$$A = B\left(T\right)\left(\frac{d\left(\ln\left(I_d\right)\right)}{dV_g}\right)^2 + C\left(T\right)\left|V_g\right|^{\gamma}. \qquad (2)$$

From fits we can determine the purely temperature parameters $B(T)$ and $C(T)$ and thus the type of scattering causing the recorded noise. The solid lines in Figure 13 b) and d) represent fits of equation 2. The values obtained from the fits are listed in Table 1.

Condition	$B(T)$	$C(T)$	γ
T = 290 K no C_{60}	$8.0 \cdot 10^{-7}$	$7.3 \cdot 10^{-8}$	-0.56
T = 290 K with C_{60}	$2.0 \cdot 10^{-6}$	$1.2 \cdot 10^{-8}$	-0.60
T = 200 K with C_{60}	$1.6 \cdot 10^{-6}$	$6.8 \cdot 10^{-8}$	-0.58
T = 150 K with C_{60}	$7.2 \cdot 10^{-7}$	$2.4 \cdot 10^{-8}$	-0.57
T = 100 K with C_{60}	$3.5 \cdot 10^{-7}$	$3.2 \cdot 10^{-8}$	-0.61

Table 1 Fitting parameters $B(T)$, $C(T)$ and γ from equation 2 fitted to the data in Figure 13 b) and d) for the same graphene FET at various temperatures with and without C_{60},

The nature of the $1/f$ noise is deduced from the ratio of $B(T)$ and $C(T)$, B/C and the γ parameter. Before C_{60} deposition we have "^" shaped behavior with $B/C \approx 11$ and $\gamma \approx -0.56$ indicating that long-range coulomb scattering (mainly from charge traps in the SiO_2 substrate) is the dominant contribution to the $1/f$ noise. After C_{60} deposition B/C increases to ~167, i.e. more than a factor of 15. The addition of C_{60} thus significantly adds to the charge exchange noise, N_{ex} given by $(d(\ln(I_d))/dV_g)^2$. This is the cause of the observed "M" shape. Then, as temperature decreases $B(T)$ gradually diminishes by a factor of ~8 while $C(T)$ shows no clear temperature dependence. At 100 K we are almost back to the values before C_{60} deposition with $B/C \approx 11$ and the "^" shape is restored. The most plausible explanation for this is that charge transfer between C_{60} and graphene is a thermally activated process. In the two-level model, the transfer rate is theoretically predicted to be $\eta \sim \exp\left(-\frac{\Delta E}{K_B T}\right)$ with ΔE being the energy difference between the chemical potential of graphene and the energy level of the trapper, while K_B is the Boltzmann constant[41,42]. The charge transfer is thus strongly temperature dependent

and suppressed at low temperatures. Also, as described above the Coulomb scattering depends weakly on temperature and everything thus points to the charge exchange noise being the significant noise contribution from C_{60}.

In conclusion, the current noise analysis establishes that C_{60} dramatically changes the $1/f$ noise behavior of graphene FETs. Noise amplitude plots changes shape from "$\frown$" to "M" at room temperature. We also saw that C_{60}'s noise contribution is thermally activated charge exchange noise. In principle, we can deduct the energy spacing between graphene and the LUMO level of C_{60}, ΔE from the transition temperature given $\eta \sim \exp\left(-\frac{\Delta E}{K_B T}\right)$. However, as mentioned above this temperature varied so much from device to device that it doesn't provide a meaningfully precise number for ΔE. In the end, the $1/f$ noise analysis proved to be a powerful method to obtain a clear signal from the addition of weakly interacting molecule on a graphene transistor.

3.7. Summary and outlook

The results presented and analyzed in chapter 3 serves to infer the electronic interaction between adlayers of C_{60} molecules and graphene. Raman spectroscopy and SLG FET analysis consistently showed a small but significant charge transfer from graphene to C_{60} molecules. Analysis of dynamic current fluctuations showed a drastic change in gate voltage dependency of current fluctuations with decreasing temperature. This change is associated with an energy barrier for transfer of electrons from graphene to C_{60}. While the results did not yield a number for said energy barrier, they illustrated the power of current fluctuation analysis to reveal even weakly interaction absorbents on graphene. The energy barrier would be useful for design of a graphene-C_{60}-graphene based vertical FET, the Carbon Burger, which will be presented in the next chapter.

4. Carbon Burger

4.1. Introduction

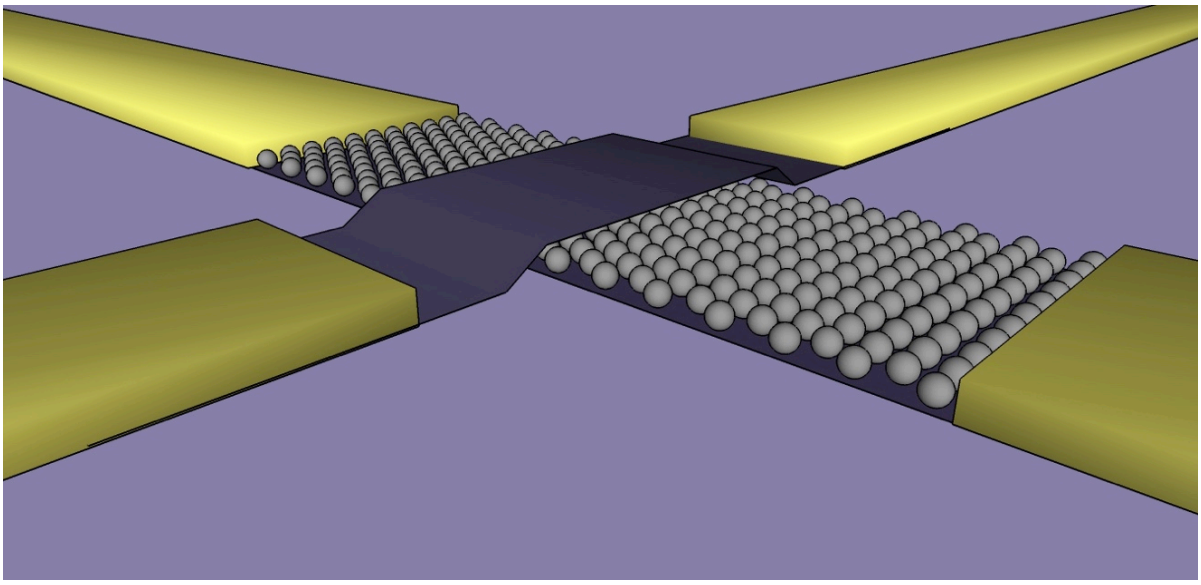

Figure 14. Model of the pure Carbon Burger with gold electrodes. The bright purple background is the SiO_2/Si^{++} substrate, the darker purple sheets are SLGs, the grey balls are C_{60} molecules and the gold coloured slabs are Ti/Au electrodes.

Graphene transistors are capable of achieving extremely high switching rates[7,68]. However, although it is possible to introduce a bandgap in graphene it almost always leads to switching rate degradation[14]. Instead of trying to introduce a bandgap we use graphene as electrode in a molecular transistor, the Carbon Burger illustrated in Figure 14. It is comprised of a C_{60} monolayer sandwiched between two graphene sheets. Earlier experiments on C_{60} thin film transistors show very large on-off ratios of 10^6, sufficient for reliable logic circuit operations[69]. Because the graphene sheet is only one atom thick it is penetrable by electric fields[25] and it is thus possible to gate a semiconductor between two graphene sheets as described above in section 2.2.3. This chapter is about my efforts towards fabricating the first graphene/molecular vertical FET, the Carbon Burger. To actually fabricate the Carbon Burger has proven significantly more challenging than first expected. In fact, the pursuit for a working device has lead to the design of four different generations of devices. A step in the fabrication of each of the first three generations has each let

to a change in design and fabrication strategy. This resulted in a large diversity in deployed device architectures and fabrication techniques. Before we get to the experimental work I will present a motivating prediction of the Carbon Burger's transistor properties.

4.2. Prediction of transistor properties

The band structure of alternating monolayers of C_{60} and graphene i.e. stage-1 C_{60} intercalated graphite was calculated back in 1994[70]. The band structure of C_{60} is practically superimposed on that of graphene preserving the electronic properties of both graphene and C_{60}. Also, the Dirac point of graphene is placed almost in the middle of the 2 eV C_{60} bandgap. This yields an effective transport barrier of 1 eV suitable for CMOS-like logics[3]. Now, that transport barrier is calculated for the bulk structure of stage-1 C_{60} intercalated graphite. The actual barrier in the vertical transistor has to be measured experimentally. For a monolayer C_{60} film the distance between top and bottom SLG electrodes is ~1.3 nm[70] and thus some tunnel transistor behavior is expected as in the device by Britnell *et al.*[16]. However, the thicker the C_{60} film the closer the barrier gets to that of solid C_{60}. Hence, the 1 eV barrier is likely to be retained with thicker C_{60} films. To get a better idea of the influence of C_{60} film thickness on transistor properties we take a further look at study on graphene-MoS_2 VFETs by Yu *et al.*[17]. The authors fabricated transistors from patterned CVD graphene bottom source electrodes, mechanically exfoliated MoS_2 semiconductor channels and Ti/Au top drain contacts. A cross section of the device is sketched out in Figure 15 a). Among other things, the study investigates the influence of MoS_2 layer thickness on transistor on-off ratio as presented in Figure 15 b). It clearly shows an exponentially increasing on-off ratio with MoS_2 thickness. What is not visible in the plot is that the on-current depends weakly on thickness. Thus only the off current diminishes significantly. This implies that the on-state conductivity of MoS_2 does not limit the on-current. Meanwhile, the exponential dependence of off current on thickness could very well be caused by a tunneling contribution to the off current as tunneling probability decreases exponentially with tunneling distance. Another factor is the metal top contact that effectively pins the MoS_2 chemical potential near the electrode. This gives a chemical potential in the active channel that varies as a function of distance from the top contact. As the

authors also discuss, this leads to additional thickness dependent gate modulation capability. Single layer MoS_2 has a direct bandgap of 1.9 eV, bilayer an 1.6 eV indirect bandgap and bulk indirect bandgap of 1.29 eV[71]. For comparison monolayer C_{60} has a predicted 2 eV bandgap[70], while C_{60} crystals have a bandgap of 1.5 eV[72]. In terms of bandgaps the two semiconductors are then very similar and we can expect somewhat similar characteristics for the Carbon Burger and Yu *et al.*'s[17] transistors.

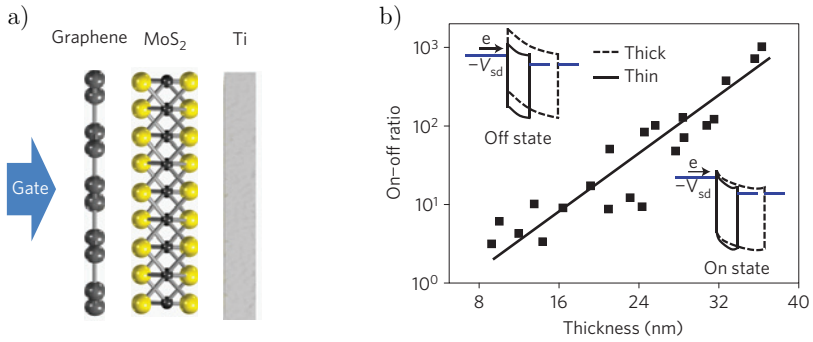

Figure 15. A study on a graphene-MoS_2 VFET. A schematic of the device cross section is shown in a) while the on-off ratio is plotted as a function of MoS_2 thickness in b). Figure adopted from Yu *et al.*[17]

4.3. Generation 1: Pure Carbon Burger

The original design for the Carbon Burger is depicted in Figure 16 d). Three main components comprise the device: a bottom SLG electrode, a sandwiched C_{60} thin film and a top SLG. This is the first and simplest design we have pursued. The C_{60} film is to cover the entire bottom SLG so as to avoid any short circuiting pinholes. However, while graphene has proven extremely flexible[73] the deposition technique employed provides tolerance of C_{60} thin film holes as will be described in more details below. We also have in mind that at least to contacts to top and bottom SLGs are desired. By knowing the transport properties of the individual graphene sheets we can isolate the graphene-C_{60}-graphene resistance.

Fabrication outline

The substrate of choice is a doped Si wafer with 285 nm SiO_2 to provide a backgate and optimum visibility of graphene[55]. The fabrication involves four major steps and is illustrated in Figure 16. First, deposit and locate a ~100 µm long pristine bottom SLG on the substrate. Then cover it with a few-layer C_{60} thin film using spray coating[45,74]. Third, deposit and align the top SLG using wet graphene transfer

described below and depicted in Figure 17[75]. Finally, use the poly(methyl methacrylate) (PMMA) covering the top graphene sheet as e-beam resist to lithographically define metal contact areas to both ends of the two graphene sheets.

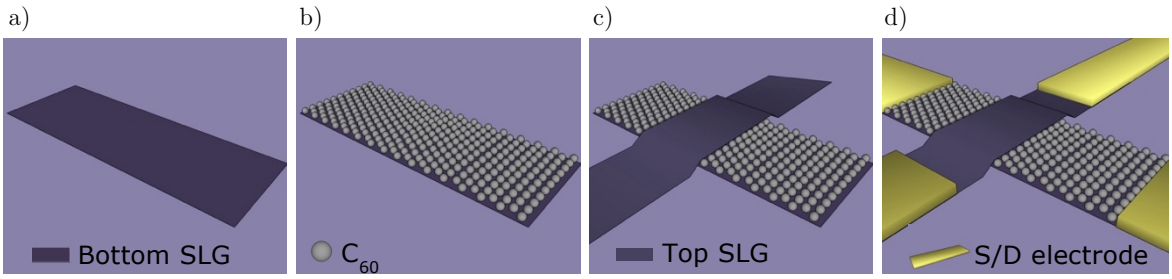

Figure 16. Fabrication of the Carbon Burger illustrated. In a) the bottom SLG is mechanically exfoliated and located on the SiO2 substrate and in b) it is spray coated with a thin film of C60. In c) the top SLG is positioned across the bottom SLG with C60. Top electrodes to bottom and top SLG are deposited simultaneously in d) using EBL and E-gun evaporation.

4.3.1. Wet graphene transfer and alignment by hand

The first thing to establish is the transfer of graphene sheets from one substrate to another. The first method of choice is a wet transfer method involving ultrapure water and PMMA supported graphene. The process involves six steps as illustrated in Figure 17. The technique is inspired by one originally developed by my collaborators Ph.D. students Shengnan Wang and Rui Wang. The current technique was developed by me in collaboration with my former bachelor students Joachim E. Sestoft and Thomas K. Nordqvist.

The steps go as the following. First, spin and hard bake PMMA resist on the wafer containing the graphene sheet to be deposited. Then immerse it in 1 M NaOH to etch away the SiO_2 as depicted in Figure 17 a). The optimum etching is done in shallow NaOH barely covering the hydrophobic PMMA. This minimizes the distance the PMMA travels in liquid and thus ensures as flat and wrinkle free graphene/PMMA as possible, depicted in Figure 17 b). Next step, Figure 17 c) is spoon transfer of the graphene/PMMA from the NaOH etch solution to ultra pure water in Figure 17 d). This is done to minimize the amount of ions in the later formed interface. Then, using clean tweezers, grab the wafer containing the C_{60} covered bottom SLG and pick up the graphene/PMMA floating on water, Figure 17 e). Use a second pair of tweezers to fixate the graphene/PMMA while picking it up.

Finally, place the assembly in an optical microscope as depicted in Figure 17 f). The top and bottom SLGs are visible through the lens of the optical microscope. The graphene/PMMA floating on water is mobile and can be positioned as shown in Figure 17 f) with tweezers by hand while the water evaporates. The position must be correct when the last water evaporates as the PMMA sticks to wafer as soon as the interface is dry. If more time is needed for positioning, water can be added to the interface using a syringe. During the last phase of evaporation the graphene/PMMA can slightly dislocate due to non-planar shape of the water droplet. That is, if one part of the PMMA is fixated on the sample while water is still trapped other places, strain is created in the membrane. This strain might move the top SLG relative to the bottom SLG and thus disrupt alignment. If the displacement is too large and the bottom SLG is not covered by some graphite flake the process can be repeated after the PMMA is dissolved.

With this hand aligned wet graphene transfer it is possible to achieve surprisingly high precision. However, the PMMA/graphene membrane moves during evaporation of water between itself and Si wafer. Consequently, it takes many correctional "pokes" with the tweezers (or preferred tool) are needed. Because of large hysteresis in the movement of the membrane one should overcorrect the membrane position and let it relax at the hopefully correct position. Usually I would add water 3-10 times and spend a couple of hours on one alignment. In section 5.1 I present examples of a 5 µm wide graphene sheet deposited on a well 2 µm in diameter aligned by hand. In Figure 18 we present an example of successful wet graphene transfer. We have transferred several parallel naturally formed micro ribbons of pristine, mostly single layer graphene on to a pristine bottom SLG. There is no C_{60} in the device. After transfer we have e-beam lithographically defined an electrode pattern in the PMMA used for transfer. Figure 18 a) is a bright field optical image of the bottom electrode graphene sheet with a ~90 µm long SLG region. In Figure 18 b) and c) we have done wet graphene transfer as described above. Several SLG ribbons are deposited across the bottom SLG. After deposition, we have written a contact pattern in the transfer PMMA using e-beam lithography. The images after transfer and lithography contain many different colors. The deep purple color represents two things: bare SiO_2 where we defined the electrodes in thin lines and a fold in the PMMA causing it to suspend over the SiO_2 in this region. These folds are

a result of wrinkles introduced during handling of the transfer PMMA. In b) the orange arrow indicates the developed end of an otherwise undeveloped electrode pattern. Most likely it is undeveloped due to the lack of focused substrate induced electron backscattering where the PMMA is suspendend[76]. The most abundant green/yellow color in Figure 18 b) and c) is PMMA covered SiO_2 with the slightly darker nuances being single or few layer graphene. In this example we have succeeded in transferring SLGs onto another SLG. Unfortunately, wrinkles in the PMMA made it impossible to successfully contact the device shown in Figure 18. Having established graphene transfer the next thing we focus on is to optimize our C_{60} coating technique of choice.

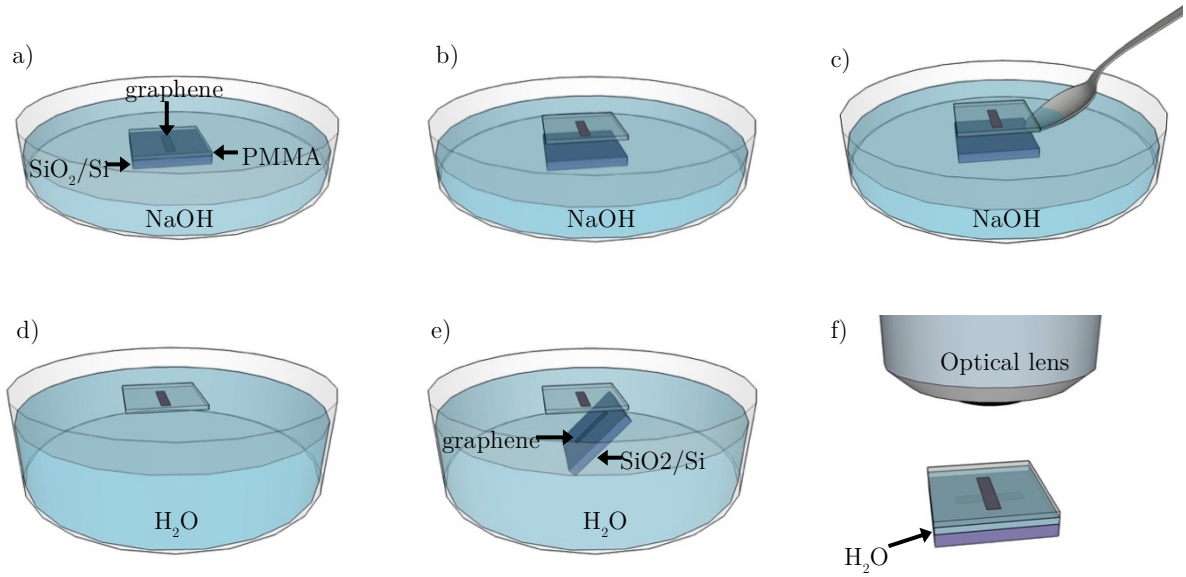

Figure 17. Wet graphene transfer and alignment. In a) the SiO_2 is etched to release the supported graphene sheet seen floating in b). In c) the supported graphene sheet is picked up by a spoon and transferred to a water bath in d). Then in e) the supported graphene sheet is picked up with the bottom-SLG containing wafer followed by alignment by hand under an optical lens as illustrated in f).

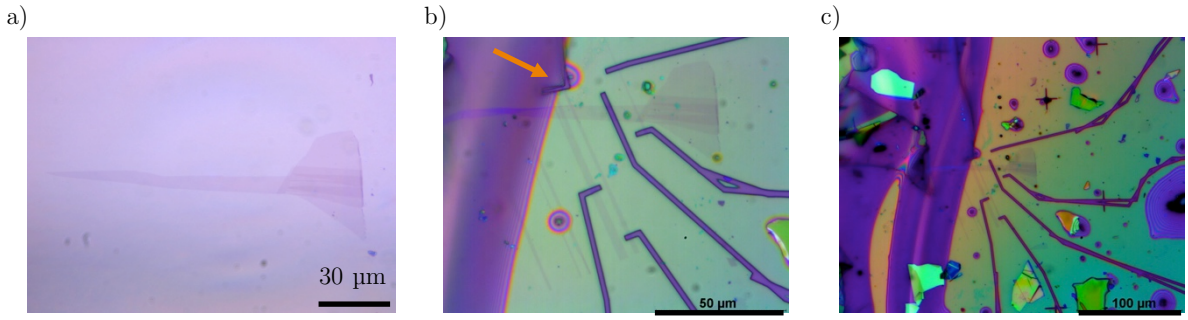

Figure 18. Wet graphene transfer. In a) is an optical image of the top-SLG prior to transfer, while the optical images in b) and c) show the top-SLG transferred on to an number of bottom-SLGs after an electrode pattern was formed in the PMMA used for transfer.

4.3.2. C_{60} spray coating optimization

Spray coating is done by spraying C_{60} molecules dissolved in toluene onto the graphene sample by use of a nebulizer with a distance from the nebulizer outlet to the sample of 20 cm. The sample is sprayed in 5 seconds intervals until a droplet hits the desired graphene sheet. A dried up C_{60} containing toluene droplet leaves a ring of mainly C_{60} at the pinned perimeter of the droplet[77]. We started by testing the simple assumption that spray coating more will increase C_{60} coverage. In Figure 19 we show optical images and in Figure 20 AFM images of the same graphene sheet after consecutive spraying intervals. In Figure 19 a) and Figure 20 a) the bi-layer graphene sheet (BLG) is spray coated $3 \cdot 5$ seconds. The black arrow in the optical image indicates a C_{60} ring near the left side of the graphene sheet. Further investigation of the AFM image reveals that roughly half of the images graphene sheet is covered by C_{60} (slightly brighter color in Figure 19 a). Interestingly, the molecules are deposited on the side facing the ring deposit. This agrees with the predicted flow during evaporation with a pinned droplet perimeter and is thus a highly that the droplet evaporates with a pinned droplet perimeter as described by Deegan *et al.*[77].

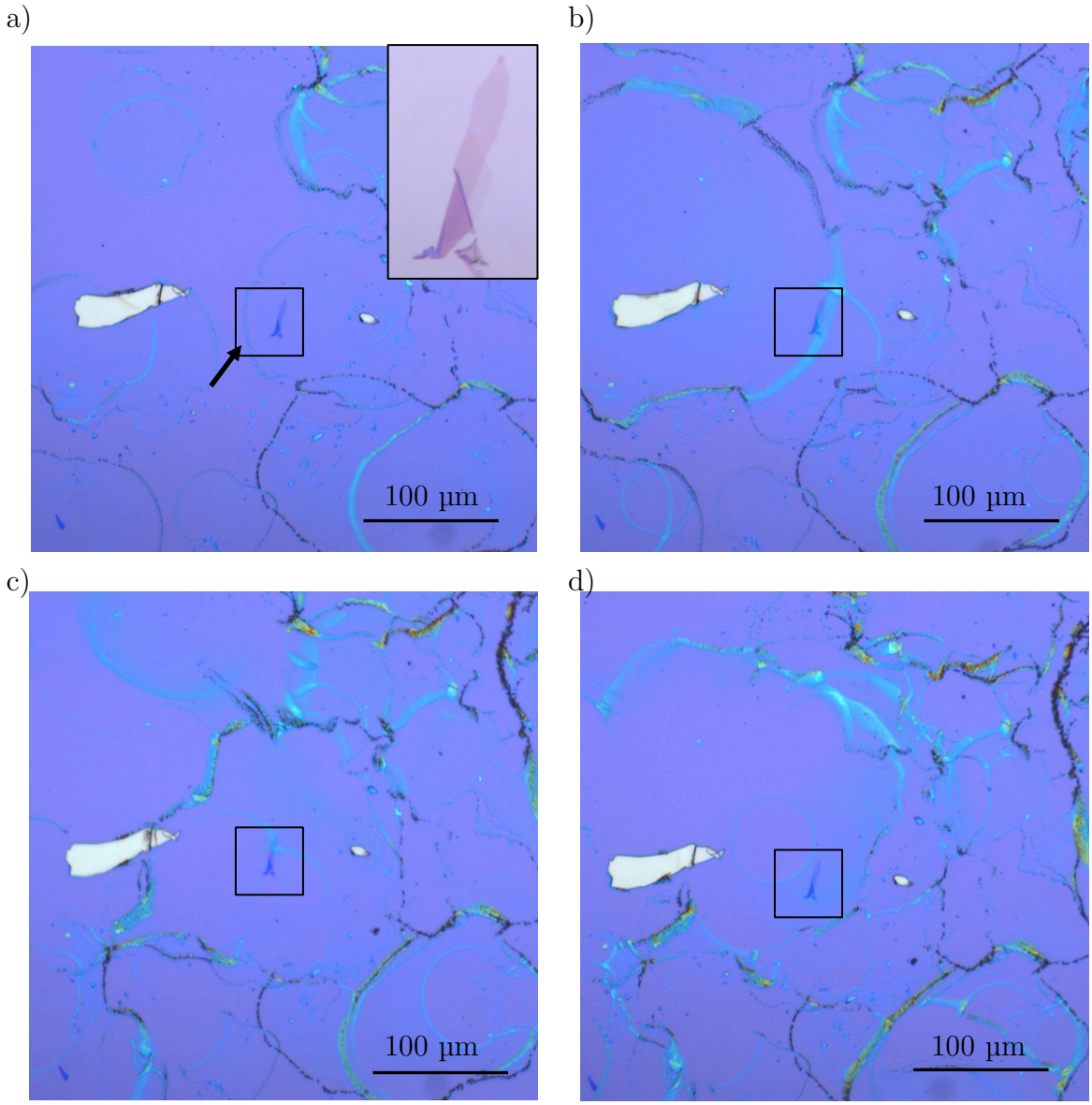

Figure 19 a) 15 s C_{60} spray coating, b) 20 s C_{60} spray coating, c) 20 s C_{60} and 20 s toluene and d) 20 s C_{60} and 40 s toluene. The black arrow marks a sediment ring while the black boxes mark the graphene sheet of interest.

After additional spray coatings with C_{60} containing toluene and pure toluene no rings cover the BLG as shown in Figure 19 d) and Figure 20 b). The C_{60} coverage in the graphene area imaged in Figure 20 b) was calculated from height distribution analysis to be > 95 %. Height profiles show that the maximum film hole diameter is around 150 µm in the same area. The coverage and small hole size is the best we have seen for any spray coated C60 thin film on graphene. While it may be good enough for a working device we have not been able to reproduce the film quality.

Further C60 spray coating on the sheet in Figure 19 d) reduced C60 coverage. I believe the reason is to be found in the different surface energy between the aromatic solid C60 and toluene and hydrophilic SiO_2 and water insoluble toluene. I have observed that incident toluene droplets do not dissolve C60 clusters above a certain size in agreement with the finite solubility of C60 in toluene[78]. Toluene has a thermodynamically driven preference for C60 clusters over the SiO2 substrate and consequently I hypothesize that cluster growth and not thin film growth happens when the clusters are large enough to be immobilized. Accordingly, it seems unlikely that C_{60} spray coating can produce completely coherent C_{60} thin films on SiO_2 supported graphene.

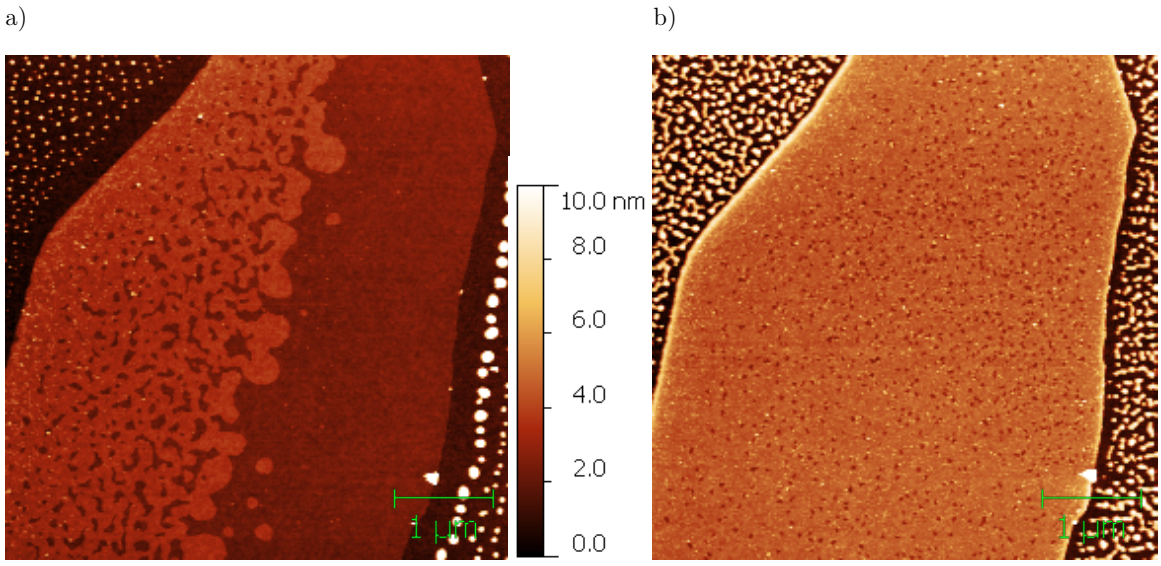

Figure 20. AFM images of a C_{60} spray coated BLG. In a) the BLG has been sprayed with C_{60} in toluene for 15 s corresponding to Figure 19 a). In b) the BLG has been sprayed first 20 s with C_{60} in toluene and then 40 s with pure toluene corresponding to Figure 19 d). Both images are 5 · 5 µm² with a 10 nm false color scale bar.

We continue further fabrication of the Carbon Burger with the C_{60} thin film quality in Figure 20 b) as a benchmark for the achievable C_{60} thin film quality. Now, for a finished device to work the C_{60} thin film must retain its quality during the final fabrication steps. As further fabrication requires wet graphene transfer, the C_{60} coverage cannot be significantly decreased by water flow. The next section investigates the effect of water flow on C_{60} thin film morphology.

C_{60} thin film exposed to water

To test the effect of water flow on C_{60} thin film morphology we spray coat HOPG with C_{60} as described in the previous section. We characterize the resulting C_{60} thin film morphology by AFM presented in Figure 21 a). To get a quantitative measure of the coverage and homogeneity of the film we record and analyze a height distribution recorded in the area marked by the green frame in Figure 21 a) and present the data in a histogram in Figure 22 a). The height distribution peaks mainly around two x values corresponding to measured heights. The first peak is assigned to the graphitic substrate and the other to the C_{60} thin film. The solid blue line represents a fitted Gaussian function with two peaks. The distance between the two peaks of ~1 nm is the expected height for C_{60} adsorbed on graphite[79]. At the local minimum between the two peaks we split the data and assign all points lower than that to the substrate and the ones above to the C_{60} thin film. Summation gives a C_{60} coverage of 67 % in the analyzed area.

We expose the C_{60} thin film to water by dripping ultra pure water (resistivity > 15 $M\Omega \cdot cm$) on the sample until it is completely covered by water. To remove the water and induce a flow we absorb the water in a dust free tissue from the top of the area depicted in Figure 21 a). The AFM image of the same area after water removal is presented in Figure 21 b). Visual inspection of the AFM images reveals C_{60} reorganization in the time between the images were recorded. Again, we record and analyze a height distribution recorded in the area marked by the green frame in Figure 21 b) and present the fitted data in Figure 22 b). The first thing to notice from the new height distribution is the significantly broader Gaussian peak assigned to the C_{60} thin film. This indicates a rougher thin film. Secondly, the coverage is now 64 %, smaller than the previous 67 %. So for this particular area the coverage is decreased 3 % while the film becomes significantly rougher. Both effects are undesired and judging from the AFM images the trend is true for more than just the analyzed area. Therefore we conclude that a dry transfer and alignment method is needed for the successful completion of the Carbon Burger.

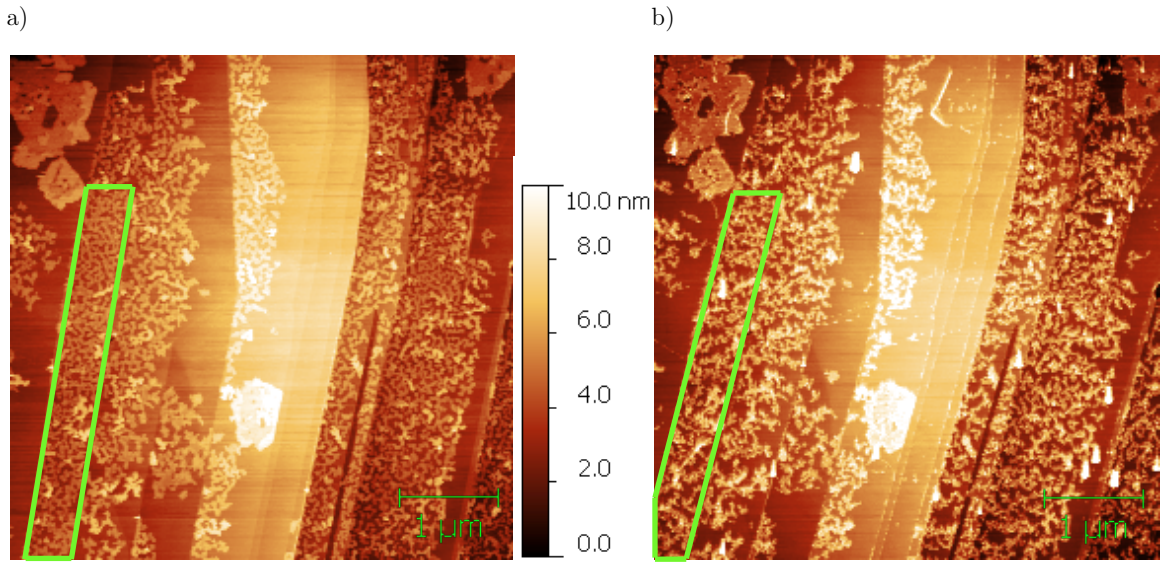

Figure 21. AFM images of a C_{60} thin film spray coated on HOPG. a) is the pristine C_{60} film and b) is the film after short exposure to a water droplet, which dried towards the top of the image. The black boxes indicate where the height distributions in Figure 22 are recorded. Both images are 5 · 5 µm² with a 10 nm false color scale bar.

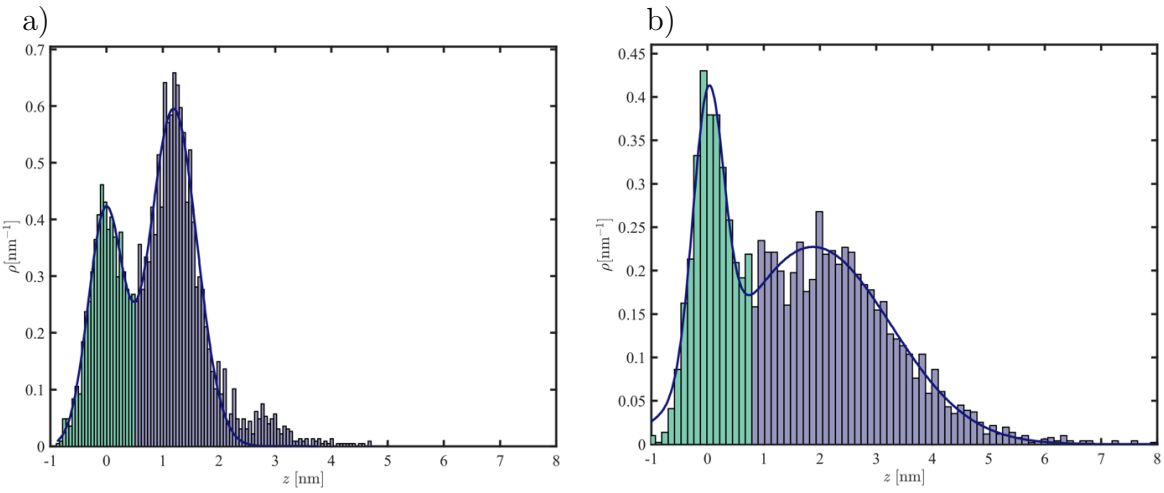

Figure 22. Height distribution analyses from images in Figure 21 a) and b). The coverage is calculated to be in a) 67 % before water exposure and b) 64 % after water exposure.

4.3.3. Dry graphene transfer and alignment

While wet graphene transfer allows for accurately aligned deposition, the water flow involved in the process has undesirable effects on the C_{60} thin film needed in a working device as described above. Therefore we set out to implement a dry

graphene transfer method. Dean *et al.*[27] developed dry graphene transfer and alignment using a PMMA support and a micromanipulator for graphene deposition on h-BN in 2010. To implement the method we introduced several modifications in our procedure. We first deposited mechanically exfoliated graphene on a clean SiO_2/Si wafer, covered it with PMMA and dissolved the SiO_2 in shallow 1 M NaOH and transferred the floating graphene/PMMA to a water bath as described in Section 4.3.1. The following steps unique to dry transfer are illustrated in Figure 23. First the PMMA with graphene facing upwards must be flipped over done in step a) to b) of Figure 23. The technique proving most effective is to pin a glass slide at the edge of the membrane and then force the membrane on to the glass slide with the graphene pointing away from the slide. The PMMA/graphene is then released on the water with graphene facing upwards. Then we pick up the PMMA/graphene and suspend it over a window in a sand-blown glass slide as illustrated in Figure 23 c) and d). Next we mount the glass slide on a micromanipulator for µm-precision alignment. Then we place the graphene sheet to be deposited facing the target substrate under a long working distance optical lens as illustrated in Figure 23 e). We found that the best way to make the graphene/PMMA stick to the substrate is to force the membrane down with airflow (N_2) through the glass slide window.

In Figure 24 we present an example of successful dry graphene transfer and alignment performed by Ph.D. student Xiaowei Wang. Prior to transfer, we spray coated the bottom FLG with C_{60} as seen on the optical image in Figure 24 a). Then the top FLG seen in b) is dry transferred to create the Carbon Burger shown in c). Finally, we contact the top and bottom graphene sheets with e-beam lithographically defined metal electrodes as shown in d). Below we present data on the local morphology of the assembled device with focus on the state of the C_{60} thin film as well as device characteristics at room temperature and 90 K.

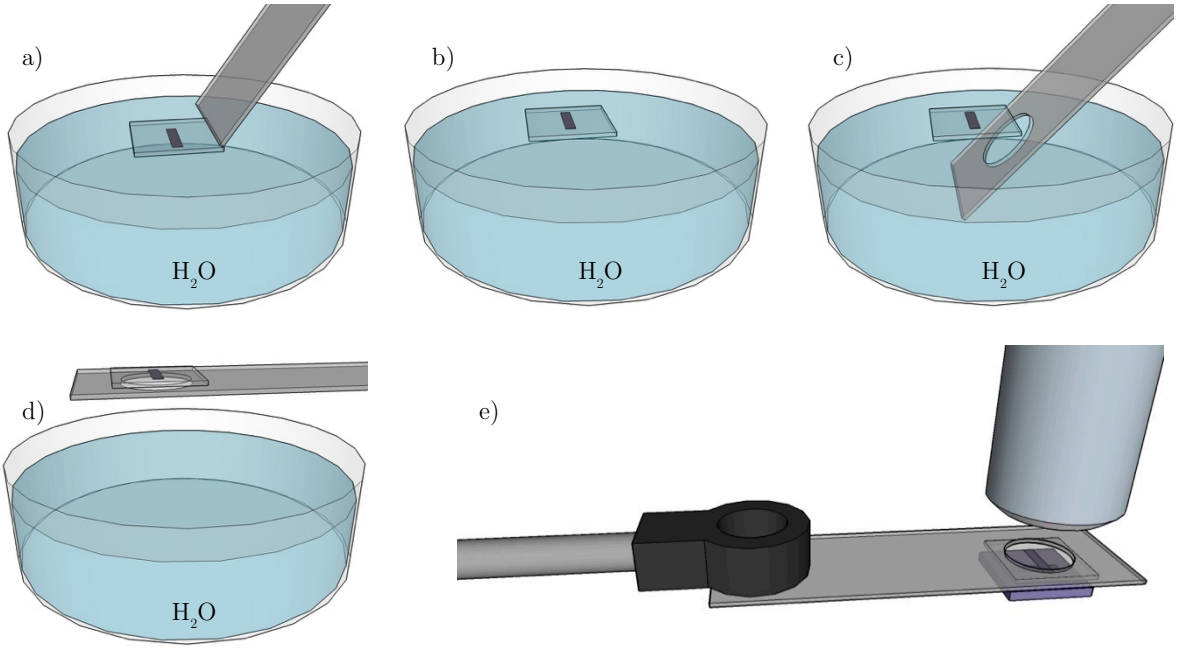

Figure 23. Dry graphene transfer and alignment. In a) the supported graphene sheet is flipped to leave the graphene sheet facing upwards as in b). Then in c) the supported graphene sheet is aligned on a hole in glass slide and picked up as shown in d). The glass slide is mounted on a micromanipulator for alignment and deposition in an optical microscope as illustrated in e).

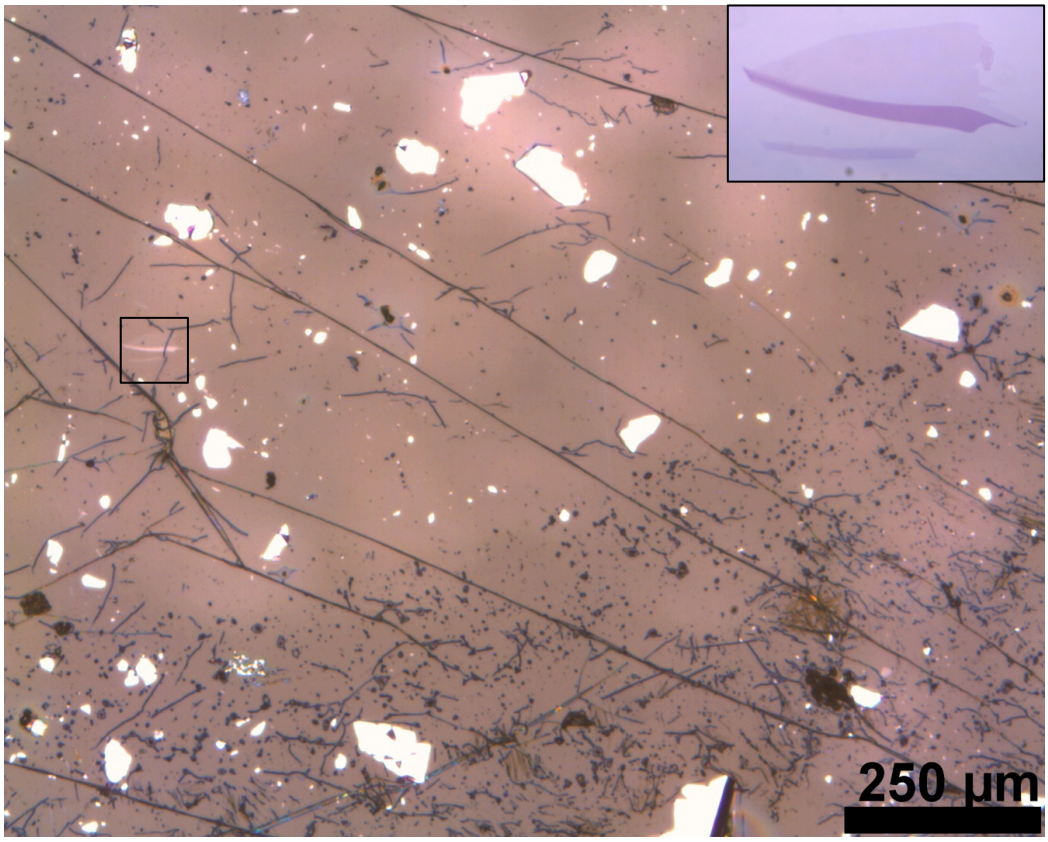

Figure 24. Optical image of graphene (marked by the black box) and graphite flakes (brightest areas) on suspended PMMA membrane with wrinkles observed as black lines. Inset shows the pristine graphene sheet before it was lifted off the SiO_2/Si substrate.

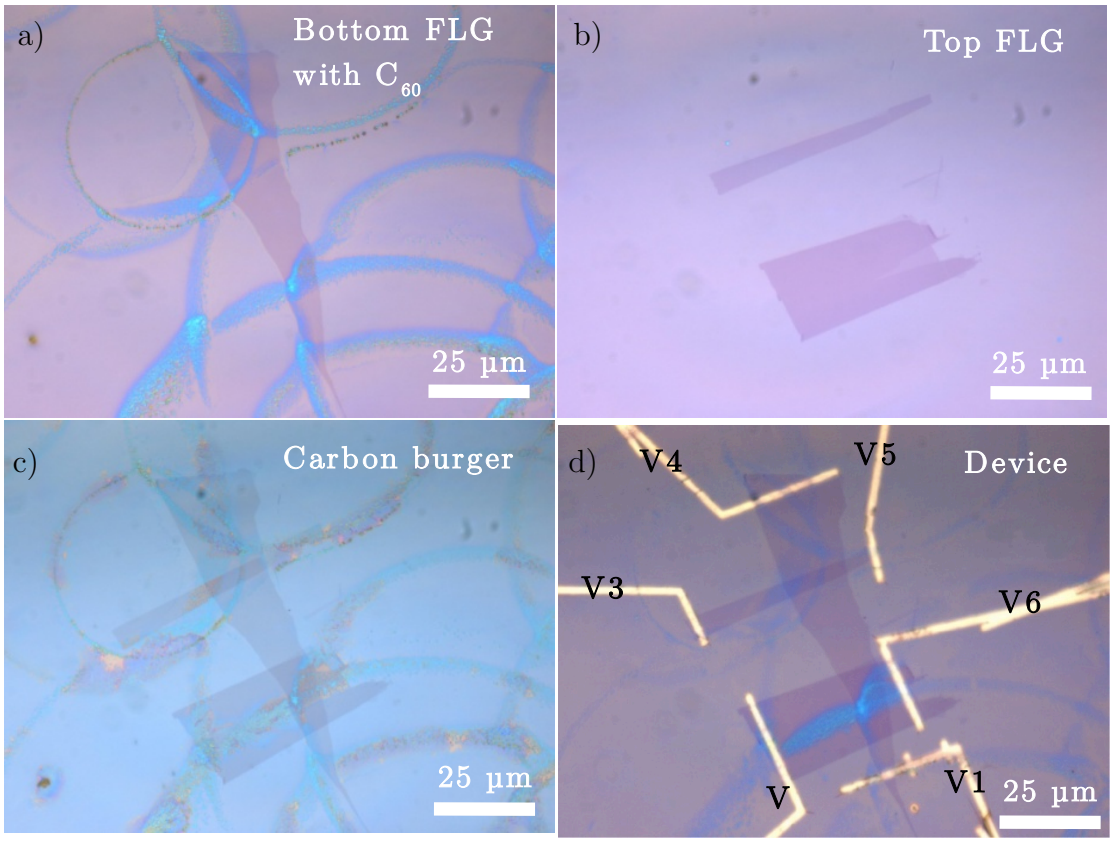

Figure 25. The bottom FLG is imaged in a) after C_{60} spray coating. The pristine top FLG is imaged in b). The assembled Carbon Burger is shown in c). Finally, the finished device is imaged in d). Images courtesy of Xiaowei Wang.

Device characteristics

In Figure 26 we present current measurements on the device presented in Figure 25 d). The gate sweeps presented in Figure 26 a) with source-drain electrodes on the same graphene sheet (intralayer) and source electrode on top FLG and drain electrode on bottom FLG reveals no transport gap between top FLG and bottom FLG. Neither at room temperature nor at 90 K. Similarly, linear curves from source-drain sweeps in Figure 26 b) indicates no transport gap between FLG electrodes.

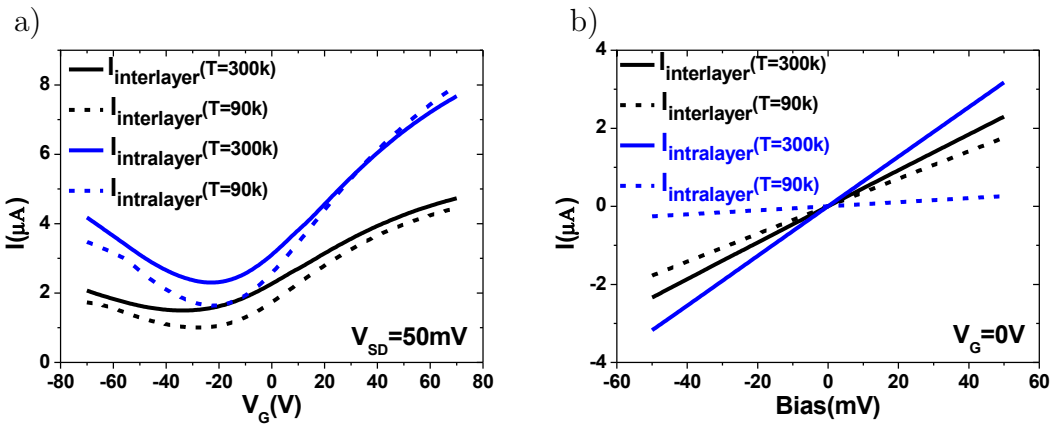

Figure 26. Device characteristics of Carbon Burger presented in Figure 25 d). In a) interlayer and intralayer gate sweeps performed at 300 K and 90 K are presented. Measurements of source-drain sweeps for the same devices are presented in b). Figure is a courtesy of Xiaowei Wang.

The effect of lift-off on C_{60} thin film

As we just saw, the device characteristics in Figure 26 does not indicate any transport gap between the top and bottom graphene sheets. To investigate the reason for this we recorded AFM images of the intersection of say graphene sheets. In Figure 27 we present an optical and AFM images of the pristine C_{60} thin film and in the finished device measured in Figure 26. The AFM image in Figure 27 b) is recorded on the pristine C_{60} thin film marked by the black box in a). From the profile recorded along the dashed white line, shown in the inset we find the expected C_{60} thin film height[80] of ~1 nm. In c) and d) we present the optical and AFM image recorded on the finished device. We know from AFM scans (not shown here) that the dashed white line in d) marks the edge of the top sheet with top and bottom layers situated as indicated by the labels. As indicated by the black dashed line the C_{60} thin film between the graphene sheets is located in separate islands. Furthermore, none of the C_{60} islands extent to the border of the top graphene sheet and the bottom graphene sheet is very sparsely covered by C_{60}. With so large contact area between the graphene sheets we do not expect to see any effect of the C_{60} except for perhaps an increase in resistance compared to a clean graphene-graphene interface. From the AFM image in Figure 27 b) we know that the C_{60} thin film was coherent before deposition of the top graphene sheet. The new morphology thus indicates that either the deposition of the top graphene sheet or metal lift-off has removed C_{60} between the graphene sheets. Considering the sparse amount of C_{60} on the bottom

graphene sheet not covered by the top graphene sheet it seems safe to assume that the C_{60} removal is related to the lift-off process.

We then thought of ways to protect the formed C_{60} thin film from exposure to the lift-off process. These efforts are described in the sections to come beginning with efforts towards NW lithography defined oxide trenches on the bottom graphene sheet.

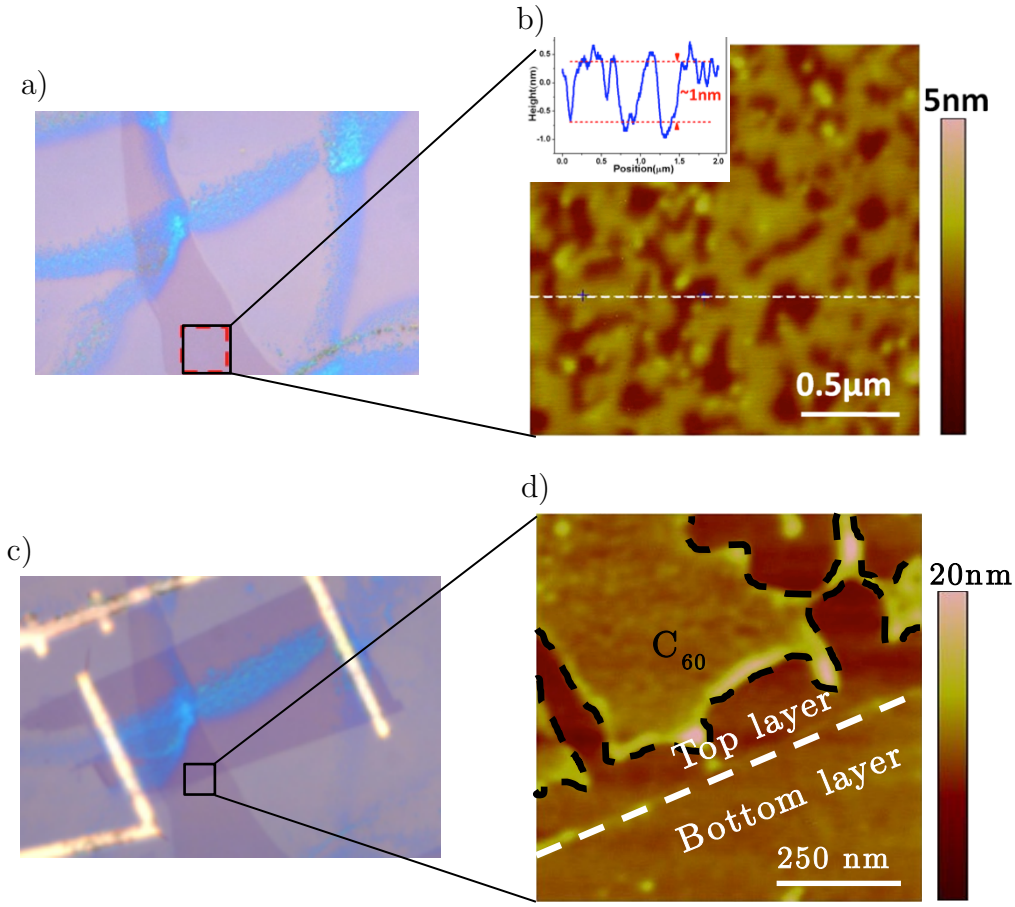

Figure 27. The as spray coated bottom FLG is presented in an optical image in a) and AFM image in b), while the finished device is imaged optically in c) and by AFM in d). Images courtesy of Xiaowei Wang.

4.4. Generation 2: Nanowire lithography

At the end of the last section we concluded that efforts should be made to shield the C_{60} thin film from exposure to solvents and especially acetone. Inspired by another project I worked on, i) we decided to define an oxide trench on the bottom graphene sheet prior to C_{60} deposition. More specifically a tin dioxide (SnO_2) nanowire (NW) was to be used as a shadow mask during atomic layer deposition (ALD) of aluminum oxide (Al_2O_3). This way, the C_{60} needed for an operational device would be separated from any solvents by the top graphene sheet extending past the oxide trench. The procedure we set out for is illustrated in Figure 28 and is significantly different from that in i). It goes as follows (steps labeled as in Figure 27):

a) Mechanically exfoliate a bottom SLG on a SiO_2/Si wafer.
b) Align a NW across the SLG.
c) Use e-beam lithography to define metal contacts on the bottom SLG and do lift-off.
d) Deposit Al_2O_3 with ALD.
e) Remove the NW to form the oxide trench.
f) Spray coat C_{60} and make sure the trench is fully covered.
g) Deposit top SLG using dry graphene transfer.
h) Use e-beam lithography to define metal contacts on the top SLG and do lift-off.

Before I go into the experimental details I want to explain the reasoning of the suggested procedure. The main goal is to ensure the graphene-C_{60}-graphene interfaces are as clean as possible. This is achieved by shielding the area on the bottom SLG contacting the semiconducting C_{60} thin film up until C_{60} deposition. The SEM image in Figure 29 reveals a rectangular cross-section of an as grown SnO_2 NWs we use for NW lithography. This shape maximizes the graphene-NW contact area and thus minimizes solvent and polymer exposure of the NW covered graphene part. Before actual device fabrication we want to establish ALD oxide deposition on graphene and test if the NW can shield the covered graphene from oxide deposition. Also we want to see how much of the oxide film is removed upon NW removal.

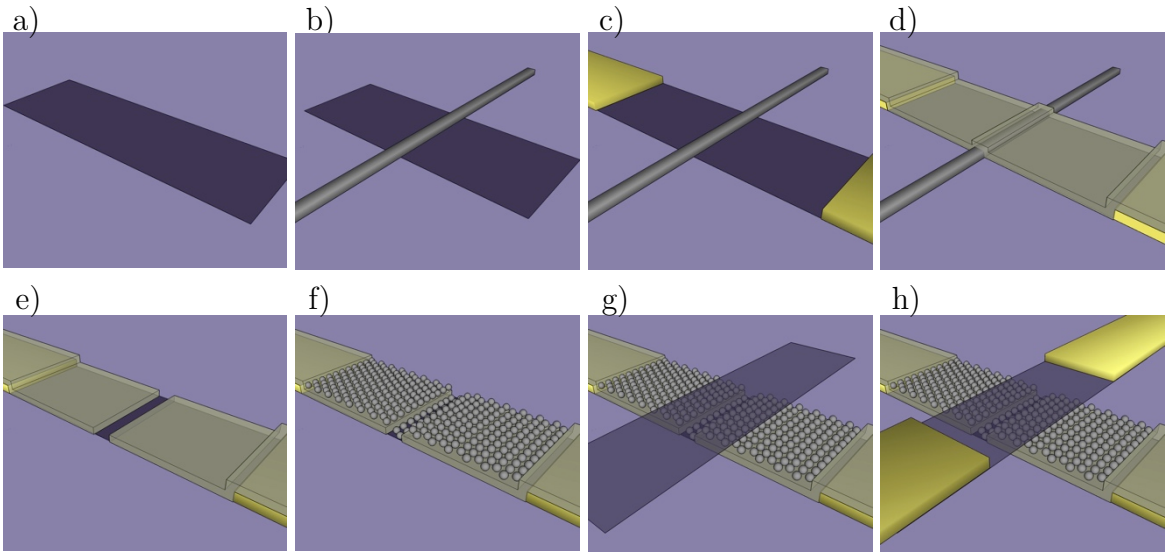

Figure 28. NW lithography defined oxide trench for Carbon Burger. The pristine bottom SLG in a) is partly covered by a positioned SnO_2 NW in b). In c) e-beam lithographically defined metal electrodes are deposited on the bottom SLG followed by Al_2O_3 ALD in d) (Al_2O_3 is not shown on ubstrate for clarity. In e) the trench is formed by removal of the nanowire followed by C_{60} deposition in f), top SLG deposition in g) and deposition of e-beam lithographically defined metal contacts to the top SLG in h).

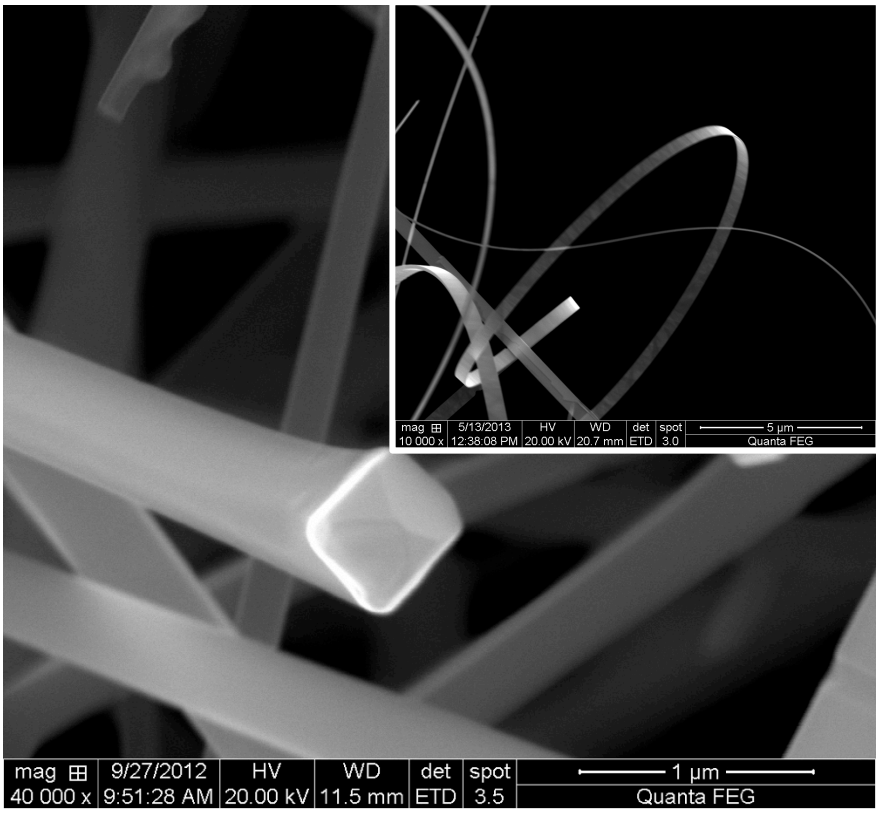

Figure 29. SnO_2 NWs with square cross-sections for NW lithography. Images courtesy of Qingxin Tang.

ALD of Al_2O_3 on pristine graphene

In ALD of Al_2O_3 a precursor is used to facilitate nucleation of atomically thin layers one layer at a time in a reaction chamber. The temperature in the reaction chamber is variable that can be tuned for specific deposition requirements. It is a non-directional deposition method contrary to evaporation of material from a source in vacuum[81].

To grow oxides by ALD on graphene has proven difficult due mainly to the inability of commonly used H_2O precursor to bind hydrophobic graphene[82]. Many different approaches to overcome this barrier have been presented. Early examples include functionalization with NO_2[83] inspired by results on carbon nanotubes (CNTs)[84], coating with perylene tetracarboxylic acid and pre-ALD deposition of 1-2 nm Al[85]. For the current study I consulted Hugh O. H. Churchill, former student of Charles M. Marcus. Hugh's method for ALD of Al_2O_3 involved two sets of cycles at ~30° C and 250° C using water and trimethylaluminum (TMA) precursors. He proved it effective on several CNT devices and one suspended graphene sample. A paper by Zhang *et al.* from 2014 (two years after our ALD experiments) investigates the temperature dependence of Al_2O_3 ALD also using water and TMA[86]. They speculate that low temperature deposition at 50° C relies of physisorption of water molecules on the graphitic plane. Going to even lower temperatures at 30° C therefore quite likely also involve water physisorption on graphene.

In Figure 30 we show optical images and AFM images with step height analysis of an FLG before ALD (left column) and after ALD (right column). More specifically, we ran 150 cycles at 30° C (required a fan blowing on the reaction chamber) and subsequent 50° cycles at 250° C. The black arrow in Figure 30 b) points to a winding bright line formed on a large graphitic flake. This line was not present before ALD as seen in a). Also the color of the SiO_2/Si substrate has gone from purple in a) to greenish in b) indicating a different oxide thickness after ALD. This line formation on large flakes and substrate color change is consistent with my observations on >5 samples. Turning to the AFM images in c) and d) they look very similar at first glance. This immediately suggests that if material was added to sample it was added uniformly. However, the profiles in e) and f) recorded across the FLG edge show an increase of step height from 4.1 nm to 7.4 nm. Also, the

roughness on the FLG changed from 0.47 nm to 0.62 nm confirming increased roughness as expected from the ALD process on graphene. As the sample has only been exposed to the ALD chamber between images it seems safe to assume that the deposited material is indeed Al_2O_3 consistent with the findings of Zhang *et al.*[86]. We tried changing the number of cold cycles to 100 and 250. With 100 cold cycles the Al_2O_3 film was had cracks with very rough edges on even small FLGs while 250 cold cycles yielded results very similar to those obtained with 150. In the following we went ahead with 250 cycles at 30°C and 50 cycles at 250° C.

NW lithography

The NW lithography was done in close collaboration with the group of Professor Qingxin Tang from Northeast Normal University, Changchun. His group grew and positioned the SnO_2 NWs on mechanically exfoliated graphene while I subsequently grew the oxide. The method earlier proved useful for mechanical positioning of nanobelt contacts[87]. After NW lithography proof of concept we planned for me to learn NW positioning from Professor Tang's student in Changchun.

In Figure 31 we present AFM images of an FLG crossed by a positioned NW before and after Al_2O_3 ALD. The as deposited NW is 102 nm high and around 200 nm wide there are no immediate signs of damage caused by the NW alignment. In b) we have run 250 cycles at 30° C and 50 cycles at 250° C. From the AFM image it is immediately obvious that the oxide film has cracks both along the NW and perpendicular to the NW. In optical images not shown here the cracks appear similar to the line marked by the black arrow in Figure 30 b) and we now assume that structure to be an oxide crack. An interesting feature is that the local position of the NW changed after ALD. The NW stuck to opposite sides of the oxide walls in different segments. This change of shape means that the oxide film once touching both sides of the NW pulled it in different directions and caused the NW to move. Interestingly, the oxide film must thus have had completely coverage at one point. Also, the different crystal planes of the FLG are still visible through the oxide. The crystal planes are also visible in the bottom of formed cracks. It should therefore in principle be possible to correlate the position of visible graphene basal planes with the contours of the formed oxide film. In Figure 30 b) we mark two lines on the FLG and two lines on the oxide film. From analyzing additional contours in the

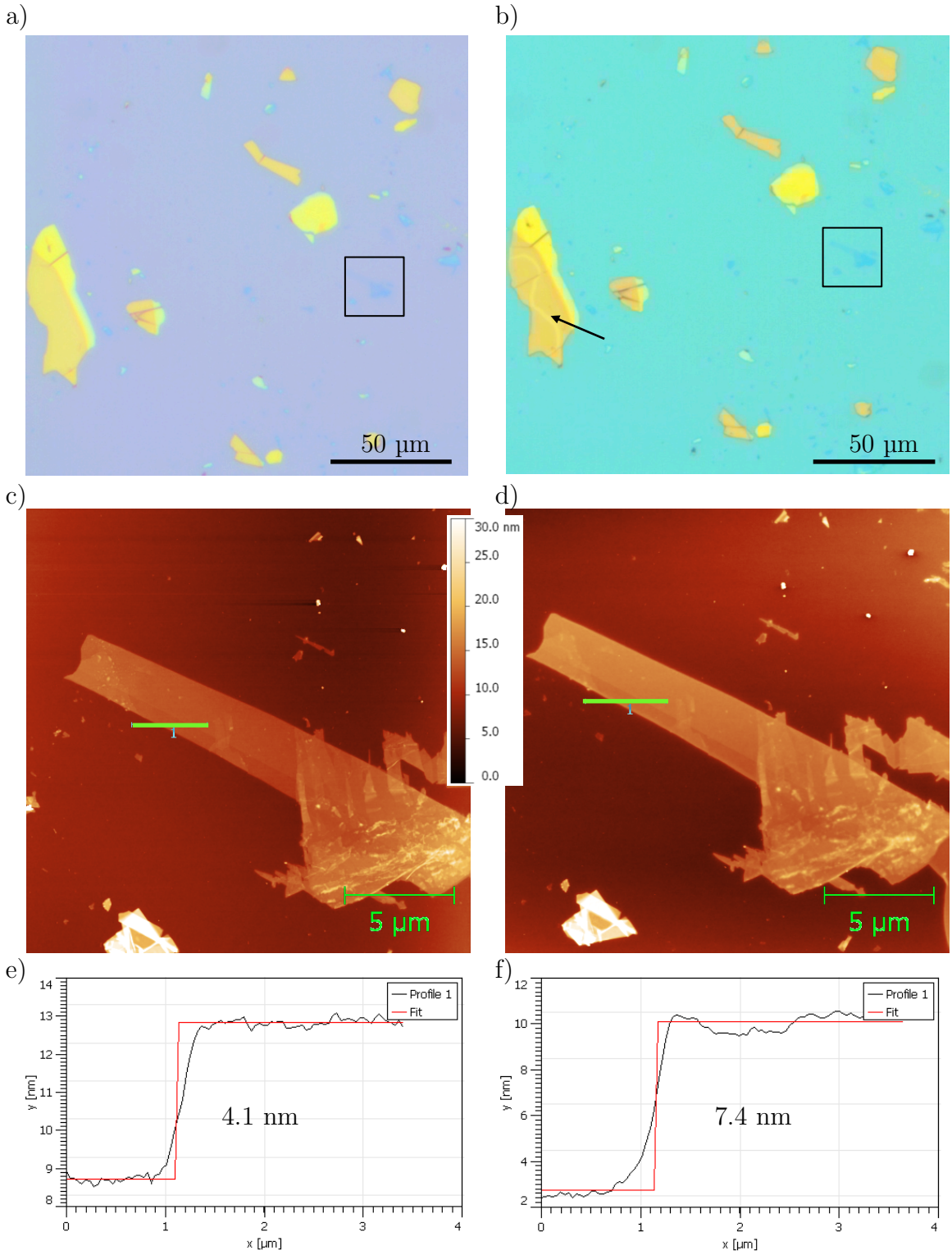

Figure 30. Al_2O_3 ALD on pristine FLG. An optical image of an FLG captured before ALD is presented in a) with the same area imaged in b) after ALD. Similarly an AFM image c) with corresponding height profile e) captured before ALD is compared with an AFM image d) with corresponding height profile in f).

crack and on the oxide we can conclude that the lines in the oxide once coincided with those on the FLG. This highly suggests that the oxide film was solid at the time it cracked.

After we confirmed oxide growth, I shipped the sample back to Professor Tang for removal of the NW. His student effectively removed it and returned the sample for my characterization. In Figure 32 we present AFM images of the oxide covered FLG after NW removal. In the overview image in a) we can clearly see that the NW removed a small part of the oxide film almost in the middle of the image. As the part is so small I do not expect it to be a problem for any future devices. Additionally, the zoomed-in image in Figure 32 b) reveals no significant difference between areas previously covered by the NW and the bottom of oxide cracks. Thus the NW has not introduced any structural defects in the graphene large enough for the AFM to detect (AFM tip nominal radius of ~10 nm). The roughness of the bare FLG in Figure 32 b) is 0.51 nm and the roughness of the oxide film is 1.4 nm. The thickness of the film is 28 nm. A more important parameter than the oxide roughness is if it has any pinholes. From >10 profiles recorded on the oxide film in b) we see a maximum depth of 10 nm. So at least there are no pinholes big enough for the AFM tip to penetrate. In the Carbon Burger we deposited the top graphene contact using PMMA support as described above. The rigidity of the PMMA will most likely ensure separation of the graphene sheets where the oxide film is present. However the top graphene sheet will be unsupported in the finished device. Thus only device measurements can confirm if the quality of the oxide film is sufficient for avoiding short circuits.

The exposed FLG after NW removal and oxide crack formation has small dots on the graphene basal plane. This looks somewhat similar to results obtained by Wang *et al.* in 2008 for Al_2O_3 ALD on pristine graphene with one set of cycles at 100° C[88]. At these conditions the authors only observe oxide growth on graphene step edges and defects. The authors argue that the ALD process needs dangling bonds to grow. Perhaps this growth process is similar to the lines and dots we observe on the FLG in Figure 32 b). While it may suggest that the remaining FLG is clean we cannot conclude that from present results.

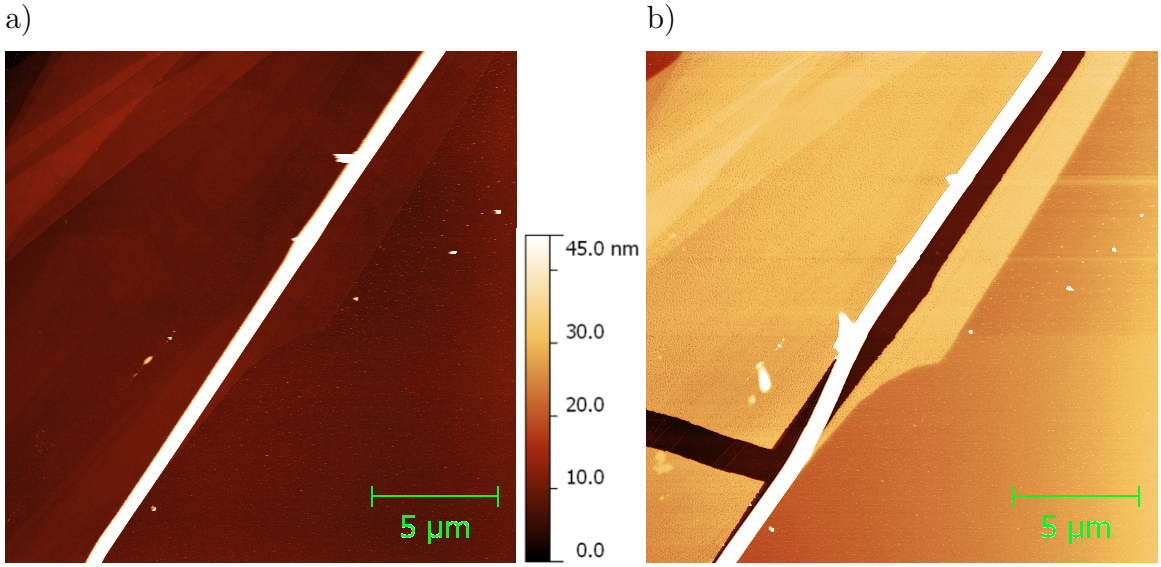

Figure 31. AFM images of a) a pristine FLG with a positioned SnO_2 NW and b) the same FLG and NW after AlO_2 ALD. The NW grew from 102 nm high before to 125 nm high after ALD. The height of the AlO_2 is 24 nm.

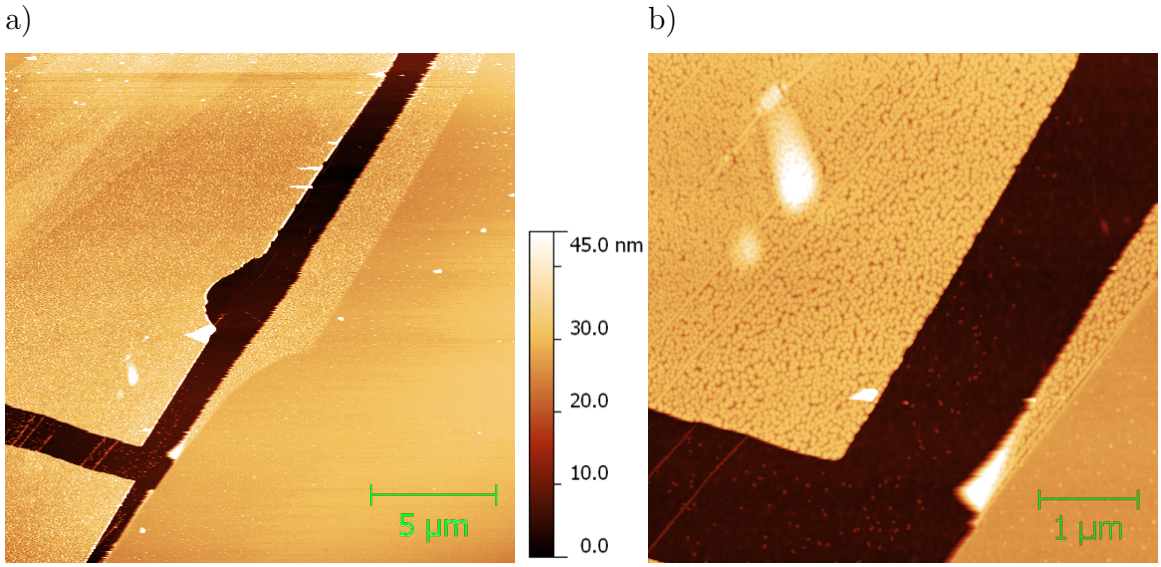

Figure 32 Same FLG as in Figure 31 after NW removal. a) is the exact same $20 \cdot 20$ µm² area as depicted above while b) is a $5 \cdot 5$ µm² zoom in on the T section in a). As evident from a) the NW has cracked off a small piece of the Al_2O_3 film. The roughness of the oxide film is apparent in b). The deepest holes in the 28 nm high film are 10 nm from height distribution analysis.

To further study the effects observed on the FLG in Figure 31 and Figure 32 we present results on an additional FLG presented in Figure 33. The two FLGs were on the same sample and therefore experienced exact same ALD conditions. In Figure 33

the NW crossed an SLG and BLG region as confirmed by AFM step heights of ~1 nm and ~1.3 nm recorded on the pristine image in a). In b) we show the same area after ALD and NW removal. Again, the NW has chipped off a small part of the oxide film. The surface roughness of this oxide film is 1.5 nm while the averaged roughness of the exposed SLG and BLG regions is 0.45 nm agreeing very well with the roughnesses observed in Figure 32. Interestingly, we do not observe oxide film cracks in apart from that caused by the NW in Figure 33. This is quite likely because of its smaller size.

No cracks in the Al_2O_3 oxide film were observed on the SiO_2 substrate. It thus seems safe to assume the graphene/graphitic substrate plays a role in oxide film crack formation. The cracks do not selectively form at the perimeter of graphene/graphite flakes. Also, graphene adheres very strongly to SiO_2 shown by Lee *et al.*[89]. So most likely the oxide film cracks are formed on graphene and graphite because of a expansion/retraction of the oxide film enabled by relatively low friction between the ALD grown oxide film and graphitic surfaces. Further optimization of ALD cycle temperatures might enable elimination of cracks.

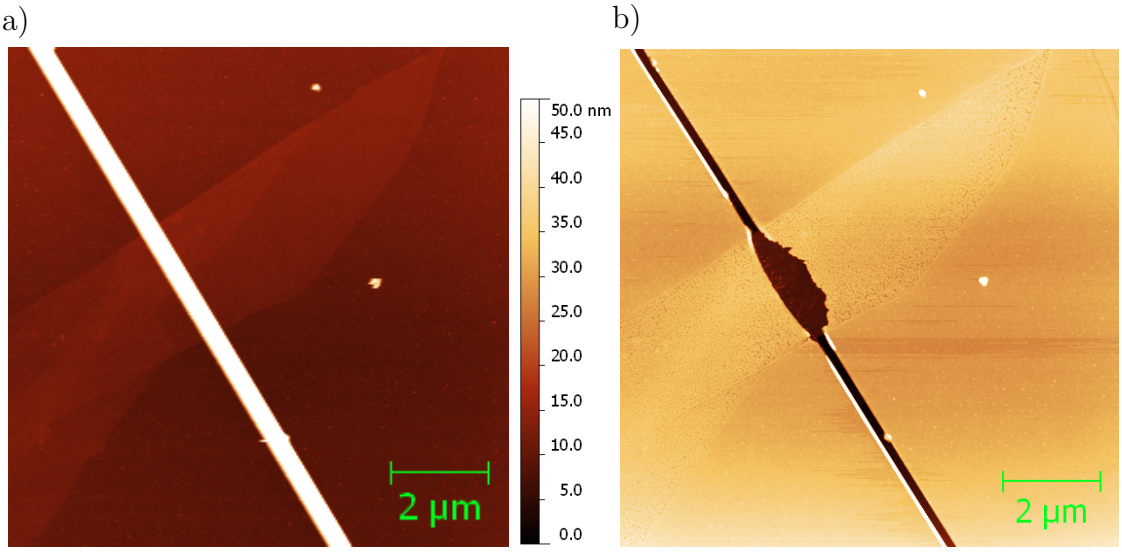

Figure 33. NW lithography for Al_2O_3. In a) a SnO_2 crosses an SLG and BLG region of graphene flake. In b) Al_2O_3 has been grown and the NW removed. No cracks in the oxide are observed except for the region having been covered by or in contact with the NW.

In conclusion, we can produce trenches in ALD grown oxide films on graphene by NW lithography. We obtained similar results on both an FLG and SLG (SLG data not shown here for conciseness). The oxide film has no pinholes observable by AFM. Pinholes with a diameter around 10 nm or less may exist. These are not expected to be an issue with in a finished Carbon Burger with a PMMA supported top SLG. However, on some graphene and graphite flakes the oxide film had cracks. These cracks might be eliminated by further ALD cycle temperature optimization. The NW lithography method developed here, might prove relevant also in other applications where lithography processes are unwanted. However, due to limited time and considering the many subsequent fabrication steps described in the beginning of present section we decided to go for a faster approach. We thought up a new device architecture and fabrication scheme presented as Carbon Burger generation 3 in the next section.

4.5. Generation 3: E-beam defined oxide wells

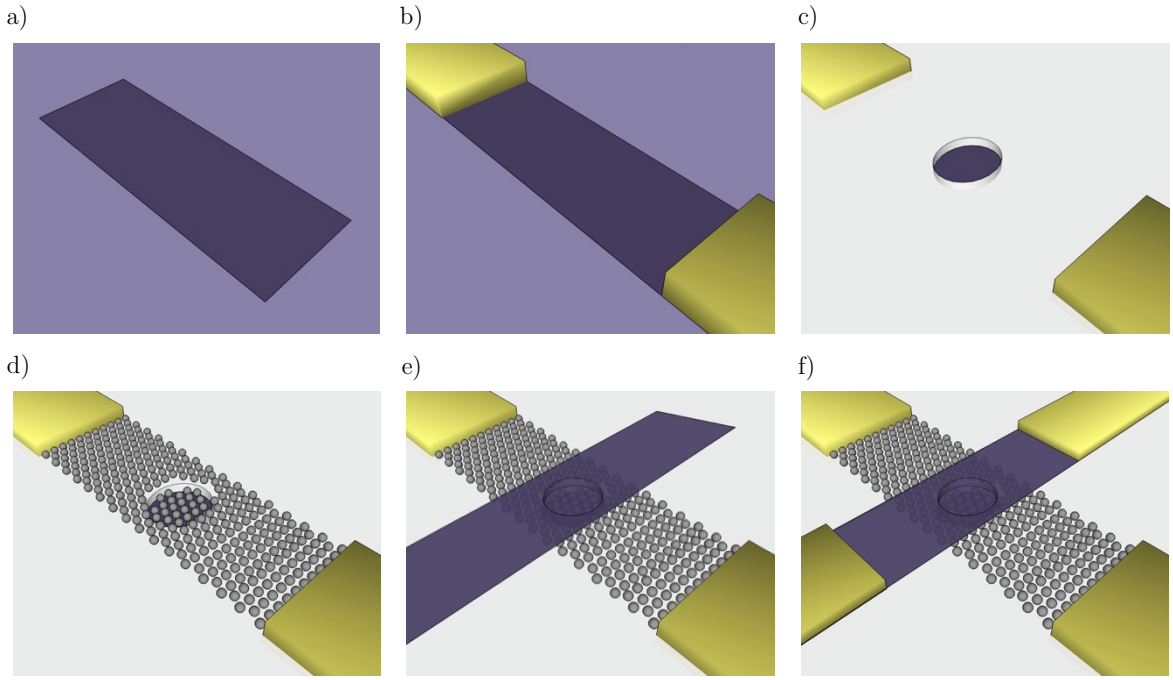

Figure 34. Fabrication of the Carbon Burger with a protective oxide film. The clean bottom SLG in a) is contacted with e-beam lithographically defined source-drain electrodes in b). In c) e-beam lithographically defined oxide wells are formed by HF etching followed by C_{60} deposition in d). In e) the top SLG is deposited by dry graphene transfer. The device is finished by forming source drain electrodes on the top SLG in f).

Following our development of NW lithography for ALD on graphene we set out for a simpler in house fabrication scheme. The processes are sketched out in Figure 34. We still use mechanically exfoliated graphene as shown in a) and deposit e-beam lithographically defined metal contacts as shown in b). We now deposit an e-gun evaporated SiO_2 film and use e-beam lithography and wet etch to define an oxide well on the bottom SLG as shown in c). In d) C_{60} deposition is done by spray coating as described above (the C_{60} film is only displayed on the SLG for clarity). Then using dry graphene transfer and alignment we deposit the top SLG as illustrated in e). Finally we use e-beam lithography to define metal contacts to the top SLG as seen in f). The complete fabrication scheme is expected to be less time consuming and with higher yield than Generation 2 described above.

4.5.1. E-gun evaporated SiO_2 on graphene

The first new step to be established and characterized is the SiO_2 e-gun evaporation on graphene. SiO_2 evaporation on graphene was done previously by Russo *et al.* to achieve double-gated graphene based devices[90]. The authors found that the breakdown voltage of their e-gun evaporated SiO_2 dielectric degraded significantly if the oxide film was exposed to air before deposition of the top gate metal. Unfortunately, we cannot avoid air exposure with the present fabrication scheme. However, we apply a source-drain voltage on the millivolt scale across the thin SiO_2 dielectric as compared to gate voltages of several volts applied by Russo *et al.*[90]. Also, Russo *et al.* use 15 nm SiO_2 compared to our planned 30 nm. Whether or not we can effectively backgate-switch the finished Generation 3 Carbon Burger without reaching the breakdown field of the SiO_2 between the graphene electrodes is to be tested experimentally.

a) b)

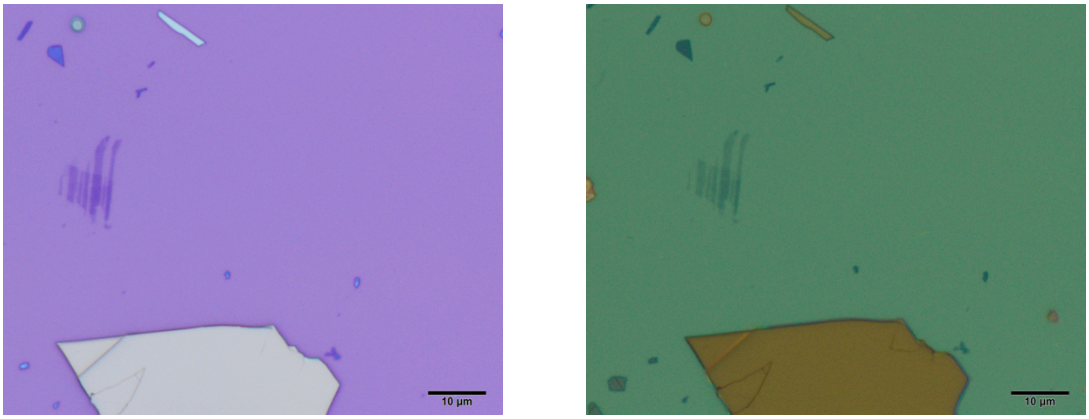

Figure 35 Optical image of an FLG before ALD a) is compared with an image of the same FLG after ALD. Notice the clear change in color indicating a change in SiO_2 thickness.

The optical images in Figure 35 show an FLG before and after SiO_2 evaporation. There is a clear color change on the both the substrate and graphene/graphite flakes. This is a clear sign of oxide deposition as the optical interference and thus observed color depends on oxide thickness[91]. In Figure 36 we present AFM images before and after SiO_2 deposition on another FLG with SLG and BLG regions. We compare both height and phase images for the thermally cleaned FLG and the FLG with 30 nm e-gun evaporated SiO_2 on top. The height of the SLG step grows from 0.7 ± 0.2 nm to 1.2 ± 0.1 nm as estimated from profile analysis. The roughness of the imaged FLG area is 0.3 nm before evaporation and 0.4 nm. These small differences are signs of homogeneous SiO_2 deposition. We now turn the AFM phase images before and after 30 nm SiO_2 evaporation in Figure 36 c) and d) respectively. Before evaporation there is a clear phase contrast between some graphene basal planes. This difference disappears with SiO_2 deposition. Because AFM phase contrast relates to surface properties[92] the suppressed phase contrast indicates that the surface is composed of a similar material in the imaged region. This is further evidence of homogeneous SiO_2 deposition across the sample.

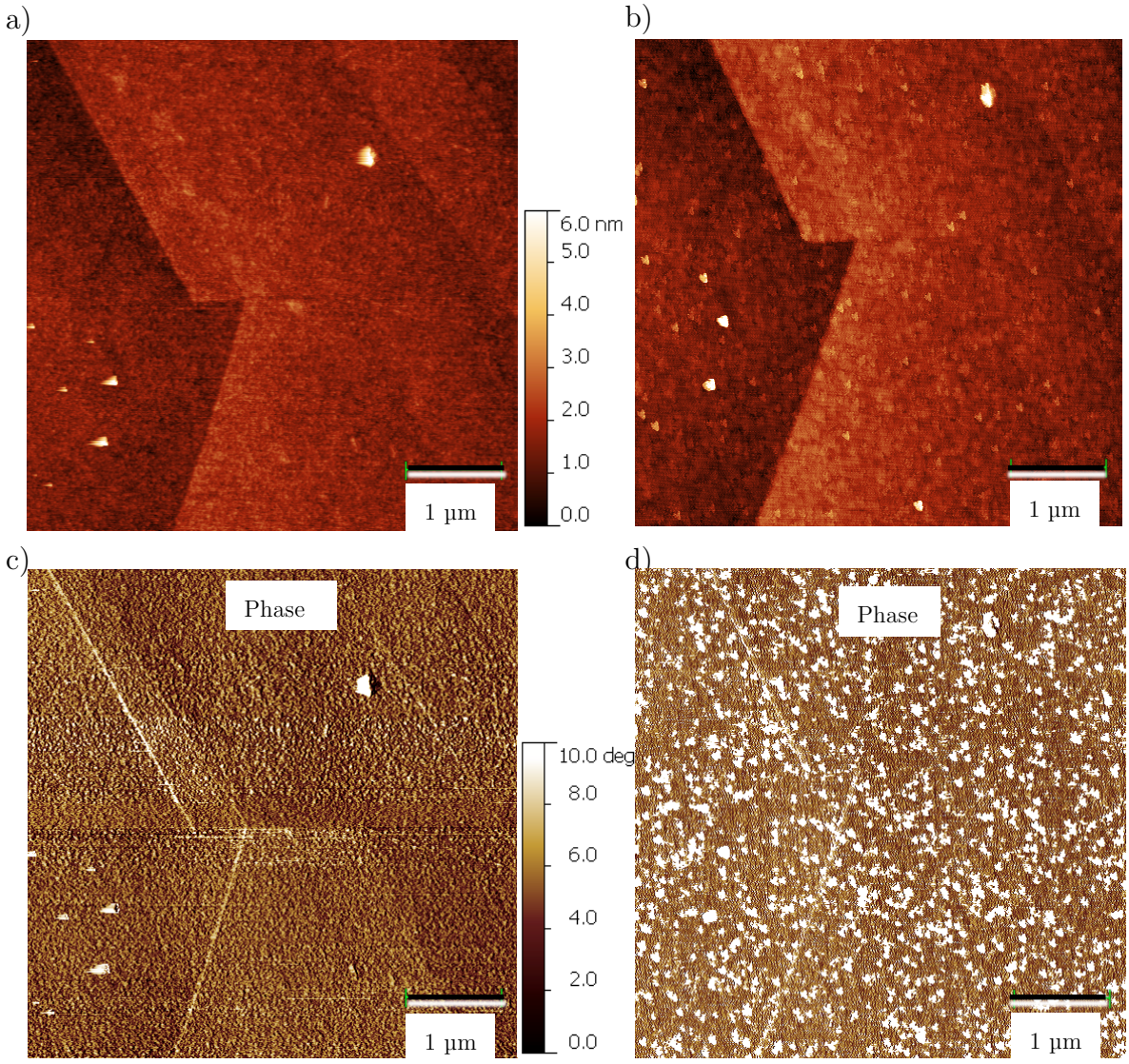

Figure 36. Same SLG a) and c) before and b) and d) after deposition of 30 nm E-gun evaporated SiO_2. a) and b) are height images with a 6 nm false color scale bar. The roughness of the graphene sheet is in a) 0.37 nm and in b) 0.48 nm. c) and d) are phase difference images.

4.5.2. SiO_2 well formation by wet etch

The next step is to form wells in the deposited 30 nm thin SiO_2 film on graphene. We use e-beam lithography to define holes in PMMA through which we selectively wet etch the oxide film on graphene using buffered hydrogen fluoride (HF). We have previously seen from Raman spectroscopy analysis of an HF exposed SLG that HF does not damage graphene (data not shown). As a starting point we chose to define 2 µm diameter holes in the 30 nm thin SiO_2 film based on experience with deposition of PMMA supported graphene on oxide wells with similar dimensions on gold

electrodes described in section 5.1. After we e-gun evaporated 30 nm of SiO_2 on the graphene sample, we spun on 4 % PMMA and hard baked it. Then we used e-beam lithography to expose the PMMA in circles of 2 µm in diameter. Alignment in the e-beam system was done to large and thick graphite flakes always present on unmodified wafers with mechanically exfoliated graphene. After development, we exposed the entire wafer to buffered HF to wet-etch the exposed SiO_2. To avoid undesired SiO_2 in the defined wells we etched 15-20 % longer than the time required according to the given etch rate. However, from AFM analysis we see a consistent well depth of approximately 30 nm. This could be because the graphene acts as an etchant barrier in hinders HF from reacting with the underlying substrate, which will be discussed in further detail below.

In Figure 37 we present AFM images of a SiO_2 well etched on a graphene surface. To clearly visualize the surface of the evaporated SiO_2 film as well as the exposed graphene at the bottom of the well, we show two representations of the same image with different height scales. Figure 37 a) and c) are the same image captured around a SiO_2 well after HF etching and removal of the PMMA resist using acetone at 60 °C for 1 h followed by 1 h annealing at 350 °C in N_2. Even with this annealing step we still see residues, possibly PMMA, on both the SiO_2 and graphene. The measured height of the SiO_2 film is around 35 nm. Before annealing (image not shown) both areas had even more residues. In order to further clean the sample we were inspired by the works of Lindvall *et al.*[93] and Goossens *et al.*[94] to mechanically clean our samples by scanning the area of interest with contact mode AFM. To apply mechanical cleaning of the oxide well shown in Figure 37 a) and c), we first scanned it three times in contact mode to clean it and once in tapping mode to image it. The tapping mode AFM image is shown Figure 37 b) and d) with different height scales. The mechanically annealed exposed graphene in Figure 37 b) is clearly more flat with practically no leftover residues supporting the effectiveness of the method. In the tapping mode image in Figure 37 d), the area inside the black square has been scanned three times in contact mode, while the area outside the black square has only been scanned in tapping mode. The measured SiO_2 film thickness is approximately 35 nm as it was before mechanical annealing. Again, the area scanned in contact mode appears with much less residues than before mechanical annealing of the SiO_2 film. Also, near the edge of the area scanned in contact mode we see

large residue gatherings most likely consisting of residues pushed picked up and left there by the contact mode AFM tip. In accordance with Lindvall *et al.*[93] and Goossens *et al.*[94] we scanned at various tip to sample forces but saw no difference in the effectiveness of the method with changing force.

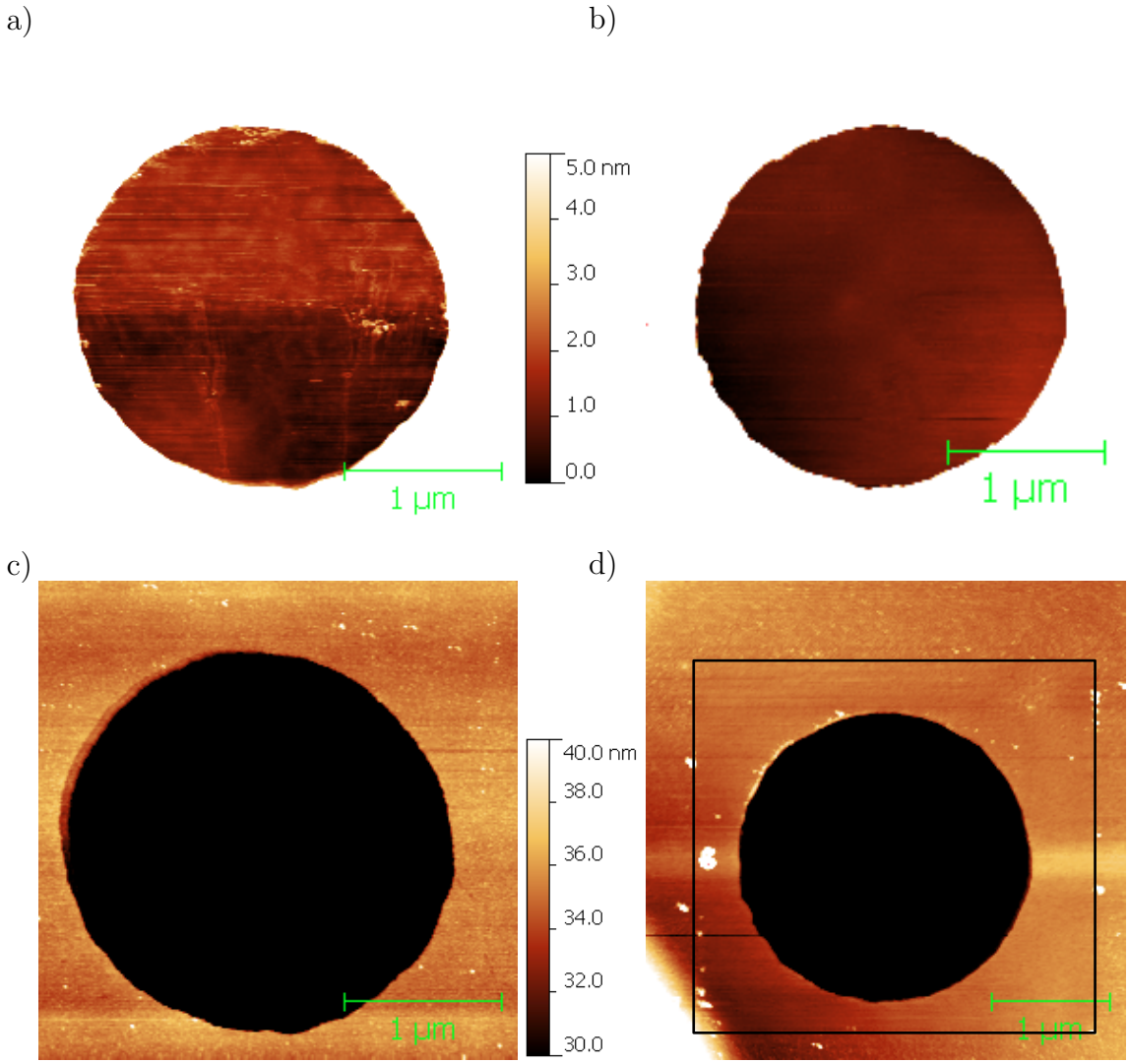

Figure 37. AFM images of the same HF etched SiO_2 well on an SLG. In a) and c) the PMMA was removed at 60 °C for 1 h in acetone and the sample annealed for 1 h at 350 °C in N_2. In b) and d) the well and surrounding area marked by the grey box in d) has been scanned three times in AFM contact mode to clean the area.

4.5.3. Graphene as etching barrier

Interestingly, we saw that wells defined in SiO_2 on graphene were always 30-35 nm deep although we have often observed the actual etch rate and depth to vary significantly on pure SiO_2. To see this effect more clearly, we etched a well in the SiO_2 film with a region on graphene and a region on the thermally grown SiO_2 substrate. The result is AFM imaged after removal of the PMMA in acetone in Figure 38 a). In the upper left part of the well, the graphene sheet is seen as a brighter region as compared to the adjacent region of the well. To compare the SiO_2 film thickness on graphene with the well depth in pure SiO_2 we record two profiles along the lines marked 1 and 2 in Figure 38 a) and plot them in b). The step height of Profile 1 recorded from SiO_2 film to exposed graphene is ~30 nm while the step height in Profile 2 is ~65 nm. So we etch 35 nm further down in the pure SiO_2 than in the graphene protected area. In addition, we observe cracks and see that the SiO_2 film follows the graphene sheet down in the etched area. This implies that the graphene sheet is under etched. On the same wafer we etched SiO_2 wells on two other graphene sheets. The height of the SiO_2 film was ~35 nm on both these graphene sheets having been exposed to the exact same experimental conditions. Thus these results show the effectiveness of graphene as an HF etching barrier.

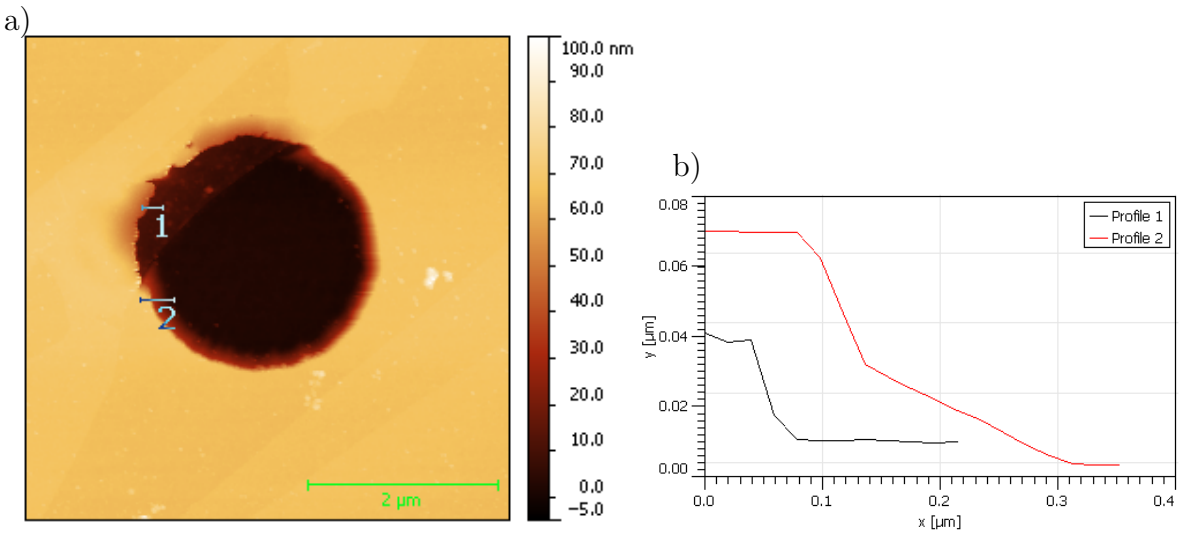

Figure 38. In a) an AFM image shows a SiO_2 well with a region on graphene and a region on SiO_2 substrate. In b) a graph shows the two height profiles recorded along the lines labeled as 1 and 2 in a), respectively.

4.5.4. Effect of SiO_2 deposition on graphene

Having described the morphology of the evaporated SiO_2 film and SiO_2 wells we wish to investigate any changes in graphene quality caused by the SiO_2 deposition. To do this we record Raman spectra of the same graphene sheet before and after evaporation.

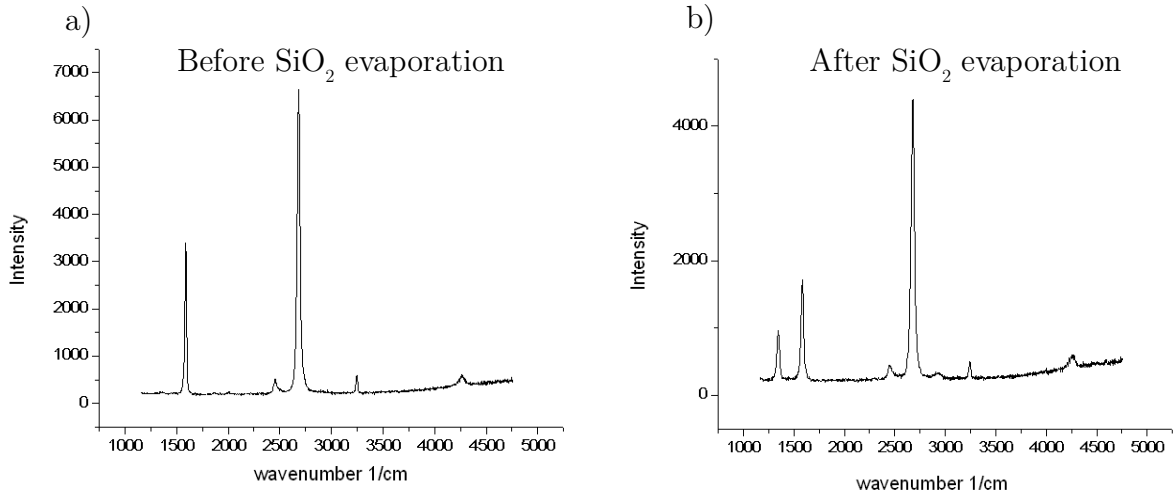

Figure 39. Raman spectra before a) and after b) SiO_2 evaporation. The spectrum in a) has now D-peak expected at ~1350 cm^{-1}, while b) has a significant D-peak.

Figure 39 shows two Raman spectra recorded on the SLG sheet before and after SiO_2 evaporation. In the pristine spectrum in Figure 39 a) we see no defect related D peak, indicating that the graphene sheet is practically defect free. Conversely, after SiO_2 evaporation a D peak immerges with an intensity at almost half the G peak intensity.

Cançado *et al.*[95] have quantified point defect detection in graphene by Raman spectroscopy. By applying their established relation between D peak intensity and the carrier mean free path, L_D in graphene we obtain $L_D \approx 15$ nm. This is less than a typical value of $L_D \approx 25$ nm for CVD graphene grown on cobber (results not shown). As CVD graphene can be readily ordered and delivered on SiO_2 from e.g. graphenesupermarket.com, we choose to deploy CVD graphene in the Carbon Burger as described in the next section.

4.6. Generation 4: CVD Carbon Burger - parallel devices using CVD graphene

In the previous section we established that SiO_2 evaporation on graphene introduces defects in the graphene lattice. Moreover, the amount of point defects introduced by SiO_2 evaporation on mechanically cleaved graphene is larger than what is usually found in CVD graphene grown on copper. Also, as described in section 2.2.4 on the relevance of graphene properties for vertical transistor performance, the mobility in the graphene electrodes is not predicted to affect the switching rate of vertical transistors. Monolayer CVD graphene is currently readily available on the centimeter scale on insulating substrates from Graphene Supermarket. Thus, using CVD graphene may make fabrication of many Carbon Burgers in parallel on a single chip feasible.

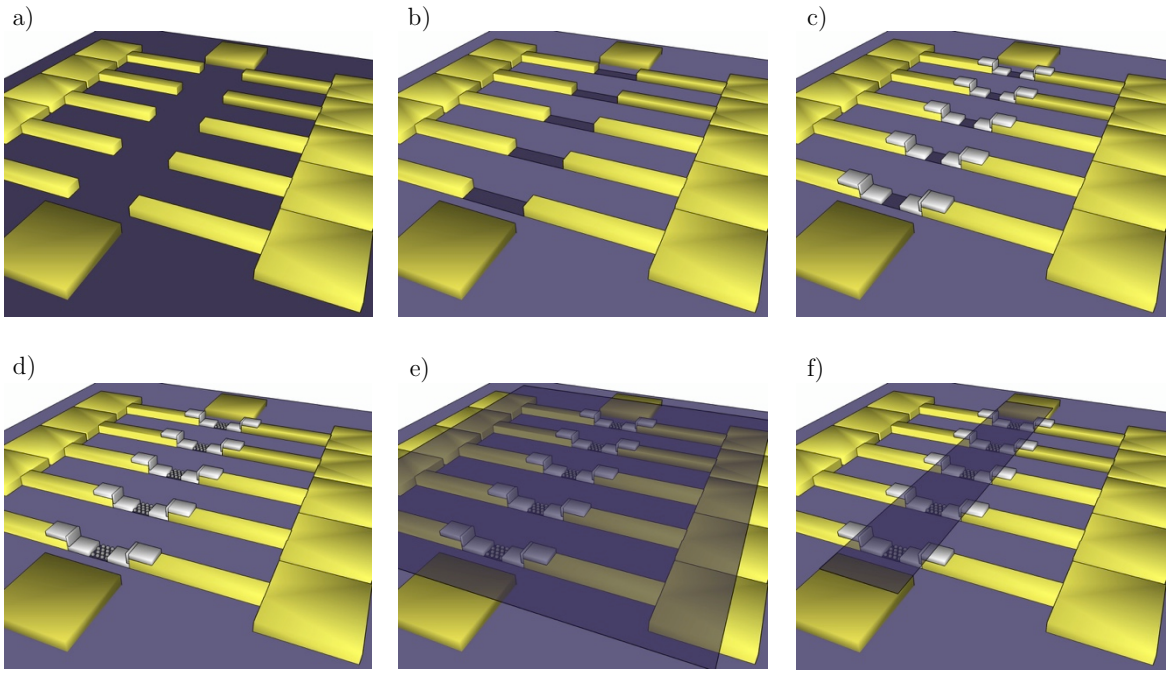

Figure 40. Carbon Burgers in parallel using CVD graphene. In a) metal source-drain electrodes are e-beam defined on a CVD graphene covered silicon wafer. In b) e-beam lithography us define graphene ribbons by plasma ashing. In c) SiO_2 is evaporated on to select areas of the graphene ribbons. In d) C_{60} is deposited followed by dry transfer of a top graphene sheet on to the sample. Finally in f), e-beam lithography is deployed to ash the top graphene sheet.

In Figure 40 we outline the fabrication scheme for parallel Carbon Burger devices fabricated with CVD graphene. Each graphene-C_{60}-graphene junction in the finished

device in Figure 40 f) has many similarities with that presented in Section 4.5. The bottom CVD SLG (drain electrode) is covered by SiO_2 everywhere except a specific area left bare to allow contact between the bottom SLG and deposited C_{60} molecules. The C_{60} molecules are contacted from above by a top CVD SLG (source electrode) and gated through the drain electrode by a global back gate in the Si substrate. With reference to Figure 40 the proposed fabrication steps are:

a) E-beam lithographically defined Ti/Au electrodes deposited in an E-gun chamber
b) E-beam lithographically defined graphene µ-ribbons by plasma ashing
c) E-beam lithographically defined SiO_2 trenches deposited in an E-gun chamber
d) Deposition of C_{60} molecules by spray coating or sublimation
e) Dry graphene transfer of CVD top SLG without microscopic alignment
f) E-beam lithographically defined plasma ashing of top SLG

During fabrication, it quickly became clear that the switch from mechanically exfoliated graphene to CVD graphene is not straightforward. While a lot of effort and development went into fabrication, experimental challenges and time did not allow the completion of a finished CVD Carbon Burger. However, successful completion of bottom CVD graphene electrodes with SiO_2 trenches was accomplished. This section is thus dedicated to describe the development and characterization of the parallel CVD graphene bottom electrodes with SiO_2 trenches.

4.6.1. Fabrication

The fabrication scheme for the CVD Carbon Burger is illustrated in Figure 40. Monolayer CVD graphene is obtained on doped Si wafers with 285 nm SiO_2. The oxide thickness allows for both gating and optical visibility of the graphene. No transfer step is then needed for the bottom SLG electrode. Prior to device fabrication, the as received CVD graphene is annealed at 600° C for at least 30 minutes to clean the graphene from polymer residues and possibly improve graphene pinning to the substrate[96].

The order of fabrication steps was found to be extremely important. Depositing metal electrodes a) first, effectively pins the CVD graphene to the Si substrate during subsequent lithography steps. Alternatively, evaporating SiO_2 on the entire graphene covered sample first, would also pin the graphene to the substrate. This fails in several ways. First, subsequent HF wet etching of SiO_2 where it is not needed, e.g. in the exposed graphene trenches, would be necessary. As opposed to the results on mechanically cleaved graphene in Section 4.5.3, CVD graphene used in this study does not act as an effective etching barrier. Areas exposed to HF wet etching have many different colors representing varying SiO_2 substrate thicknesses beneath the graphene. Electrode morphology is known to have an impact of molecular device characteristics and should thus be as consistent for all electrodes as possible[97]. Also, the evaporated SiO_2 was sometimes partly removed by lithographical steps needed after SiO_2 evaporation. So as is evident from the recipe above, HF wet etch is avoided and SiO_2 is deposited as late in the process as possible.

Also the distance between the metal electrodes en electrode pairs has been optimized. At distances above 25 µm, lithographical processes often removed the graphene between metal electrodes. An example of a finished set of parallel CVD graphene electrodes with SiO_2 trenches is presented in Figure 41. The zoom in image presented in Figure 41 b) shows an intra electrode pair distance of 20 µm and an inter electrode distance of 34 µm. Also, the deposited SiO_2 extends to cover and surround parts of the metal electrodes. As the SiO_2 is deposited at a 30° degree angle, it covers the electrode sides so as to avoid short circuits between the metal electrodes and the later deposited to graphene electrode.

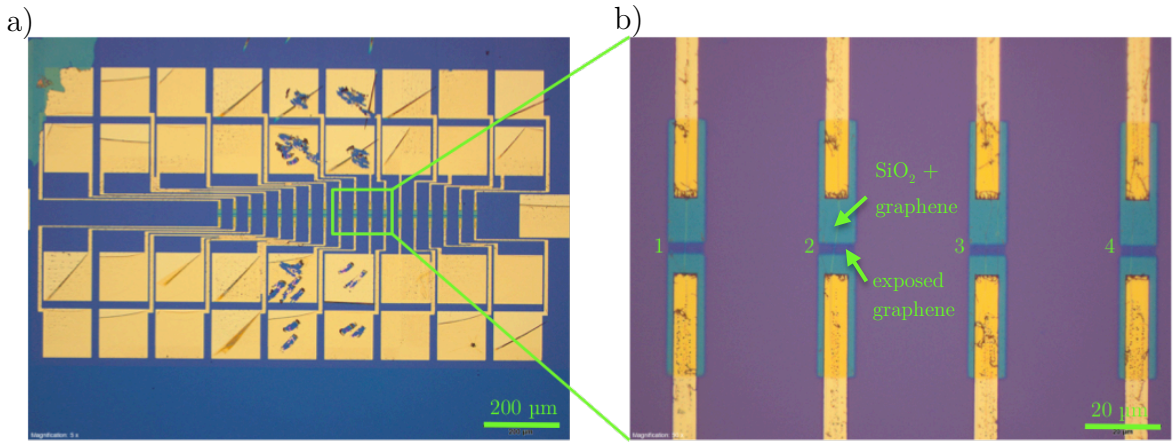

Figure 41. Optical images of finished bottom CVD SLG electrodes with SiO_2 wells. The overview in a) shows visible signs of wear on the bonding pads used for measuring conductance in a probe station. The zoom-in in b) shows graphene µ-ribbons with trenches defined in SiO_2 extending onto the Ti/Au electrodes.

4.6.2. Electronic characterization

Figure 42 a) shows a representative room characterize temperature gate sweep performed between device 1 and device 2 in Figure 41 b). There is effectively zero current with no gate dependence between the two electrode pairs. This illustrates that the graphene between the two electrode pairs has been removed or oxidized sufficiently to render the graphene non-conducting. The same result was obtained between all measured electrode pairs.

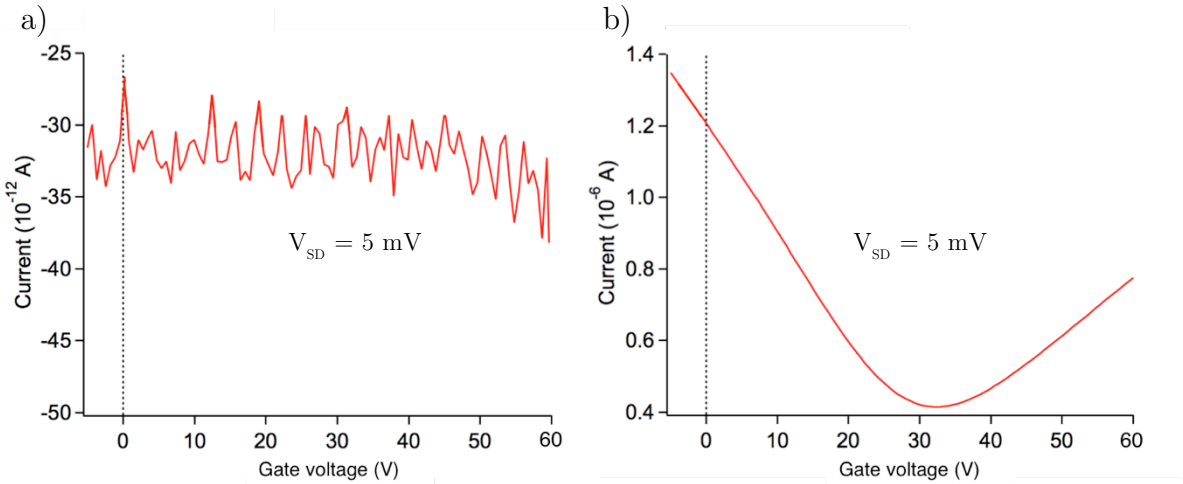

Figure 42. Conductance measurements as a function of gate voltage V_G on graphene µ-ribbons shown in Figure 41. In a) the current is between top electrodes in device 1 and 2, Figure 41 b). The current is practically zero and gate independent. In b) the current is measured across device 1 in Figure 41 b). The Dirac point is reached at $V_G = 32$ V with a minimum current of 0.42 µA.

In Figure 42 b) we present a room temperature gate sweep, i.e. I_{SD}/V_G in vacuum of device 1 shown in Figure 41 b). The source-drain voltage is kept constant at $V_{SD} = 5$ mV, while the gate voltage is swept from V_G = -5 V to V_G = 60 V. The representative gate sweep in Figure 42 a) of device 1 in Figure 41 b) exhibits a minimum current, $I_{Direac} = 0.42$ µA at a gate voltage of, $V_{Dirac} = 32$ V. To extract the mobility we use the Drude model in the form of[5,98] $\mu = \frac{t}{\varepsilon_0 \varepsilon_r} \cdot \frac{\mathrm{d}\sigma}{\mathrm{d}V_G}$, where t is the dielectric thickness, ε_0 is the permittivity of vacuum, ε_0 is the relative permittivity of the dielectric and σ is the conductivity. You might notice the rounded shape of the I_{SD}/V_G curve around $V_G = V_{Dirac}$. This is to be expected from thermal excitation of carriers around the Fermi energy. Also, local dopants in the form of residues from lithography or charge traps in the substrate may give rise to a different V_{Dirac} for different regions of the graphene sheet. Accordingly, the mobility, μ is proportional to the slope of an I_{SD}/V_G plot in the linear regions as presented in Figure 42 b).

From the measurement on device 1 presented in Figure 42 b) we find $\mu_1 = 940$ $cm^2V^{-1}s^{-1}$ and device 1-3 have mobilities around 1000 $cm^2V^{-1}s^{-1}$. Point defects introduced by evaporation of SiO_2 onto our graphene electrodes are expected to lower the mobility as compared to unmodified CVD graphene. Indeed, these values are approximately a factor of 2 lower than the mobility reported by Venugopal *et al.*[99] for a similarly grown CVD graphene sheet without deposited SiO_2. However, as discussed previously the mobility of graphene electrodes in a VFET is of relatively low importance.

In a finished VFET, a more important parameter is the on-current in graphene sheet resistance at the gate voltage applied in the on-state, V_{G_on} of the VFET. Solid C_{60} has a predicted bandgap of ~2 eV with the Dirac point of graphene predicted in the middle of the C_{60} bandgap. However, as described by Yu *et al.*[17], the effective transport gap of the VFET will depend on the thickness of the sandwiched semiconductor channel, in our case the C_{60} thin film. We will thus not predict V_{G_on} for the Carbon Burger but note that the measured conductance of our graphene bottom electrodes is $\sigma \approx 0.6$ mS at V_G = -5 V and that it can be significantly increased at large negative gate voltages (at $V_G = 0$, the graphene sheet is already p-doped and thus the largest conductivity can be achieved at negative gate voltages less than the break down voltage of the 285 nm dielectric SiO_2, at least -80 V).

4.6.3. Outlook

The bottom CVD graphene electrodes with SiO_2 trenches were developed for application in the Carbon Burger. Unfortunately, time did not allow an attempt to finalize fabrication with C_{60} deposition and deployment of top graphene electrode. However, the developed bottom CVD graphene electrodes with SiO_2 trenches may be of great value in serving as a testbed for finding molecules suitable for molecular VFETs. Indeed the design of the electrodes was inspired by a set of metal bottom electrodes used in switchable vertical molecular transistors in a study I contributed to i). In that study, a multilayer reduced graphene oxide top contact was deployed. With the addition of a graphene bottom electrode, the vertical molecular transistor may be transparent to light and flexible when fabricated on a suitable substrate, while the graphene bottom electrodes also enable deployment of a back gate. To the best of my knowledge there is presently no example of graphene bottom electrodes with oxide trenches having reproducible characteristics for molecular electronics - perhaps because of the many obstacles on the way to achieve them.

To avoid the complication of adding the top SLG one might consider evaporating metal directly on top the C_{60} thin film instead of adding the top SLG. Of course this would limit the flexibility and transparency of the device but it might serve as a nice proof of concept. For this device to be successful however, the C_{60} thin film must retain complete coverage during metal evaporation to avoid pinhole formation. Yu *et al.* presented a similar idea in 2012[17]. Their device consists of a graphene bottom source electrode, a MoS_2 crystalline semiconductor channel and a metal top drain electrode. The top metal Ti/Au electrode is evaporated directly on the MoS_2 crystal. The integrity of the MoS_2 is confirmed by Transmission Electron Microscopy (TEM) images and confirmed transistor characteristics of finished devices. However, the covalently bound MoS_2 is stronger than the van der Walls bound C_{60} thin film. As a start, I would suggest a 5-10 layer thermally evaporated C_{60} thin film.

4.7. Thermal synthesis of Carbon Burger

This section is primarily based on the work presented in Martin Kühnel's master thesis[100]. The project is based on my idea and I took active part in the experiments while supervising the project.

4.7.1. Introduction

As is evident form the previous section, step-by-step fabrication of the Carbon Burger is far from trivial. As alternative, we were inspired by an early study on thermal intercalation of C_{60} in graphite by Gupta *et al.*[101]. The authors present results on stage-1 C_{60} intercalated graphite obtained by heating C_{60} and graphite powder to 600° C for two weeks in vacuum. Stage-1 refers to the fact that there is one graphitic layer between each intercalated C_{60} monolayer as shown in Figure 43.

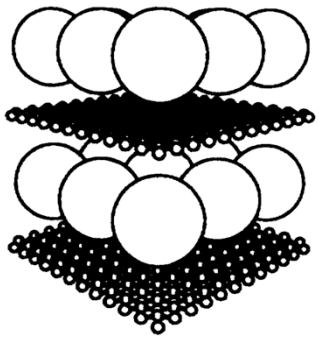

Figure 43. Sketch of stage-1 C_{60} intercalated graphite. Each C_{60} monolayer is separated by a single graphitic monolayer. Figure adopted from Saito and Oshiyama[70].

If stage-1 intercalation of C_{60} in graphite is possibly, it should be possible to intercalate a monolayer of C_{60} molecules in bilayer graphene. We thus propose to thermally intercalate C_{60} in mechanically exfoliated bilayer graphene to obtain the Carbon Burger.

Gupta *et al.*[101] worked with graphite undergone previous treatment to expand and break up the graphite in order to facilitate eased intercalation. The procedure is developed and described in detail by Chen *et al.*[102]. It involves oxidation and expansion by first treatment with sulfuric acid and nitric acid followed by rapid thermal annealing at 1050° C and extended sonication of the product in ethanol to obtain what the authors termed graphite nanosheets. The nanosheets are 30 – 80 nm in thickness and 5-20 µm in diameter. The diameter corresponds well with that

obtainable by mechanical exfoliation of graphite. The much-reduced thickness of bilayer graphene as compared to the nanosheets, is not expected to reduce the likelihood of intercalation. However, holes introduced by oxidation and expansion of the nanosheets might ease intercalation as compared to close to defect and hole free mechanically exfoliated bilayer graphene. We will present experiments on both pristine bilayer graphene and acid treated expanded graphite.

4.7.2. Device architecture and fabrication

In a finished working Carbon Burger, as described above electrical contacts are needed to both the top and bottom graphene electrodes. In a thermally synthesized Carbon Burger, the starting point is a bilayer graphene flake. Source and drain metal electrodes should thus contact to individual graphitic layers in bilayer graphene. The simplest way to obtain individual contact to the bottom layer would be to deposit the bilayer on a prefabricated metal electrode, which is our approach. Contact to the top layer is less trivially obtained. It could be done by evaporating SiO_2 in select areas, as demonstrated in Section 4.6.1, to expose only the center of the top layer to a later lithographically defined top metal electrode. As an initial approach we choose an AFM needle as a top contact. During my Master's study I set up a conducting probe AFM for local conductance mapping of chemically reduced graphene[103]. The setup was chosen for this study as well.

The procedure proposed by Gupta *et al.* to obtain C_{60} intercalated graphite involves two weeks of heating to 600° C. For this reason we chose platinum (Pt) for bottom metal electrodes. Initial results showed that the height of the metal electrodes should be close that of the SiO_2 substrate. This is done by wet etching 35 nm down in the substrate before depositing 35 nm of metal as illustrated in Figure 44. Standard UV lithography is used to define the electrodes. They are designed to be parallel, several mm long and 5 µm wide 30 µm apart. Numbers for a coordinate system are fabricated in parallel with the electrodes to allow for later identification and relocation of individual graphene flakes as shown in Figure 45 a). In Figure 45 b) we the result of mechanical exfoliation of graphite on a wafer with prefabricated Pt bottom electrodes. The red circle marks a bilayer graphene sheet, confirmed by

AFM to extend onto the Pt electrode (AFM image not shown). Note that the sheet is clearly visible on the SiO_2 substrate, while it is invisible on the Pt electrode as might be expected using white light optical microscopy[55].

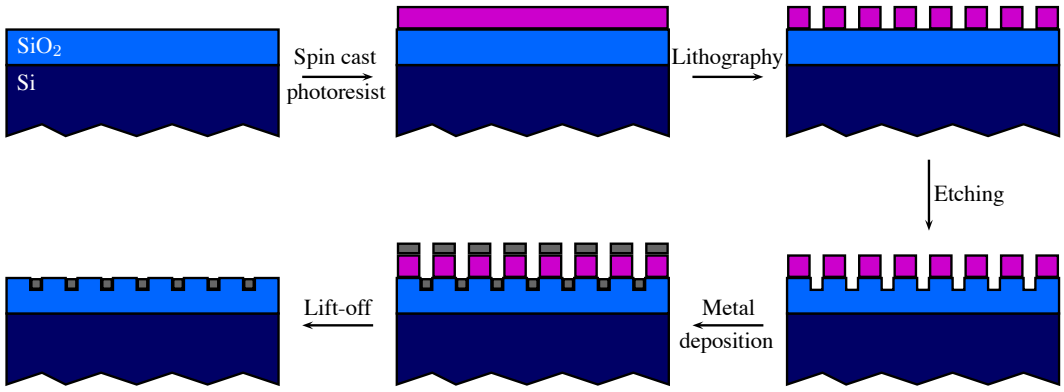

Figure 44. Schematic of fabrication steps to obtain bottom metal electrodes level with the substrate. Standard UV lithography is used to define the area of the electrodes. Before metal evaporation, wet etching is used to etch down an amount similar to the amount of metal evaporated. Schematic adopted from reference [100].

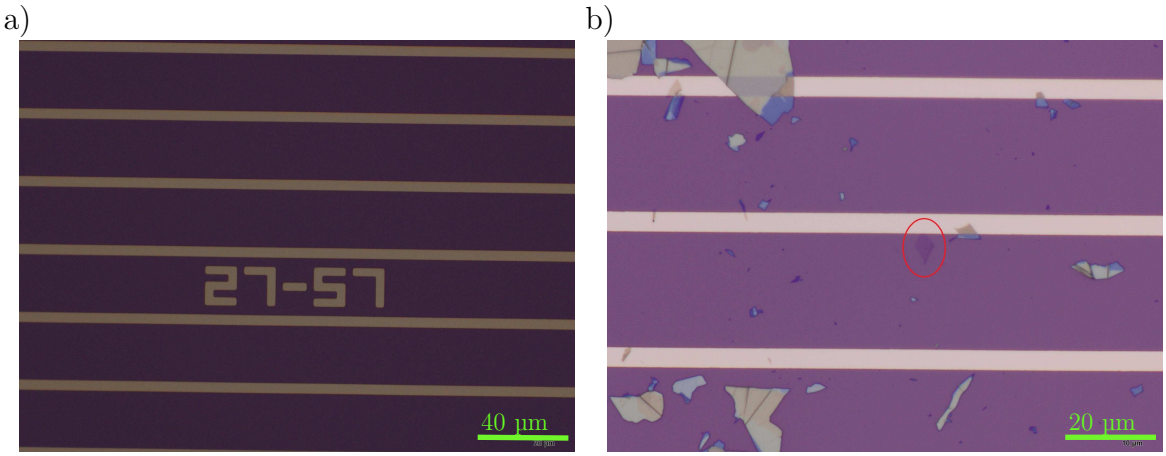

Figure 45. Clean bottom Pt electrodes with coordinate system in a) and similar Pt electrodes after mechanical exfoliation of graphene onto the wafer in b). The red circle in b) marks a small bilayer graphene sheet clearly visible on the Si/SiO_2 substrate but invisible on the Pt electrode. Images adopted from reference [100].

4.7.3. Thermal intercalation of C_{60} in bilayer graphene

As described above with reference to Gupta *et al.*[101], thermal intercalation of C_{60} in graphite requires heating the graphite and C_{60} powder to 600° C for two weeks. Our procedure is as follows: first prepare wafer with bottom Pt electrodes and coordinates, then mechanically exfoliate and locate bilayer graphene on the wafer, put the graphene covered wafer and a few mg C_{60} in a quartz tube, pump out the quartz tube to reach a pressure $< 10^{-5}$ mbar and seal the quartz tube with an oxy-propane burner as shown in Figure 46. Then leave the sealed gas tube in an oven at 600° C for two weeks. Finally, turn off the oven and let leave the quartz tube to cool down slowly with the oven.

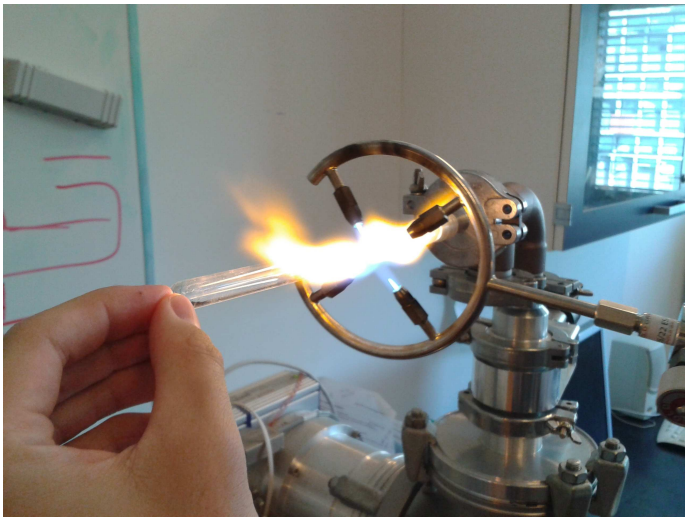

Figure 46. Sealing of a quartz tube containing a graphene covered wafer and C_{60} powder. The interior of the tube is simultaneously being pump down to a pressure below 10^{-5} mbar. Image adopted from reference [100].

The first attempt of thermal intercalation of C_{60} in FLG is shown in. The optical image in Figure 47 a) recorded before C_{60} intercalation reveals several small and large graphitic flakes. An FLG flake is singled out and imaged by AFM in Figure 47 c) to record an inter-plane step height of 0.7 ± 0.2 nm. This height indicates a step height of 2 – 3 graphitic planes. After the intercalation attempt, the optical image in Figure 47 b) shows a lot of dark formations as compared to the image of the pristine sample.

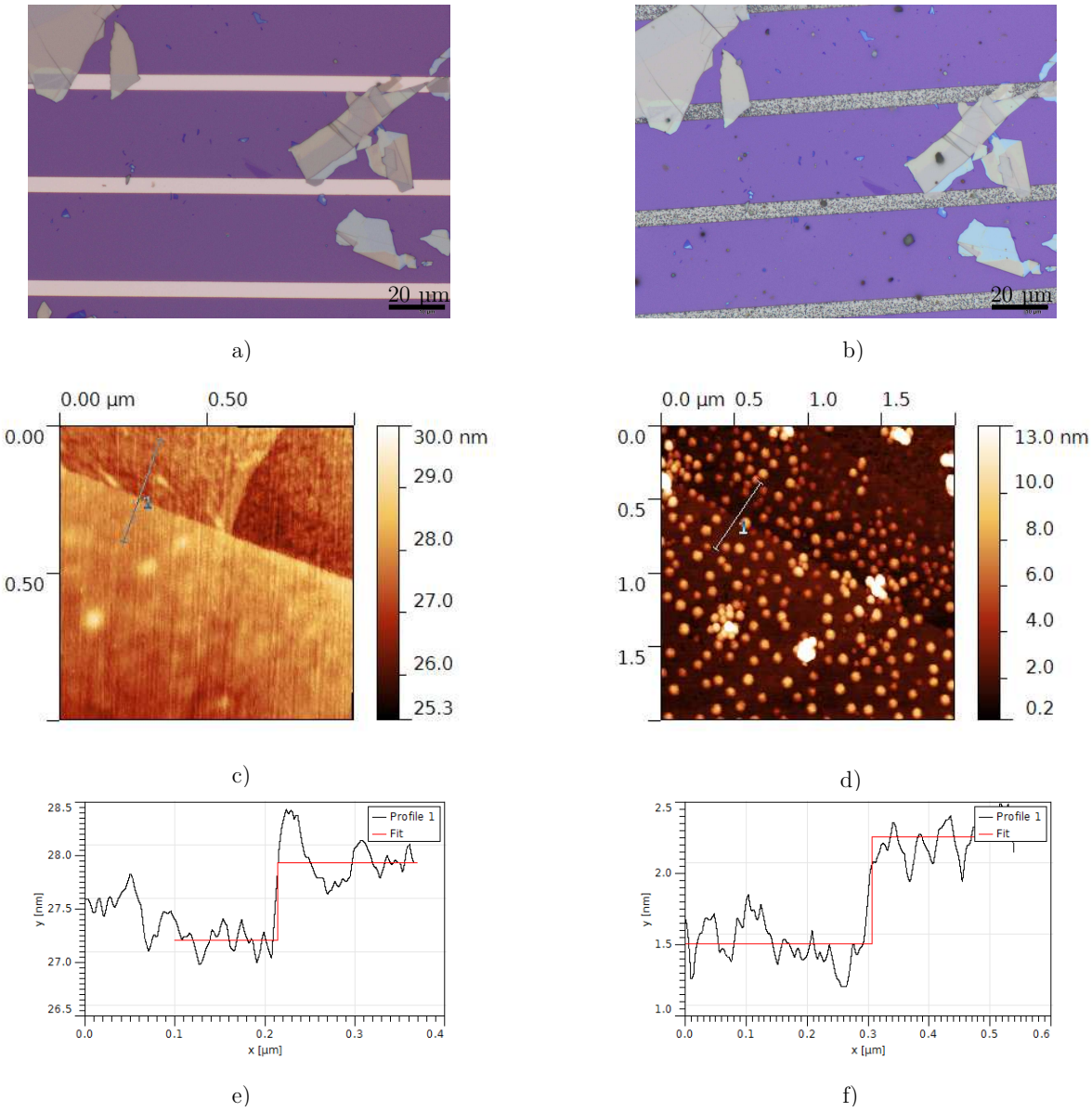

Figure 47. Optical and AFM images of first C_{60} intercalation attempt in FLG. A pristine FLG flake is imaged by optical microscopy in a) and AFM in c) with a height profile from the AFM image presented in d). The step height calculated from the height profile marked by the grey line in c) and plotted in e) is 0.7 ± 0.2 nm. The same FLG flake is imaged after C_{60} intercalation in b). An AFM recorded after thermal annealing is presented in d) with corresponding AFM height in f). The calculated step height after intercalation attempt is still 0.7 ± 0.2 nm. Figure adopted from reference [100].

AFM imaging of the sample directly after intercalation attempt proved difficult, as the AFM tip was unstable due to a very rough surface and most likely also accumulation of C_{60} molecules on the AFM tip. In an attempt to desorb C_{60} molecules from the surface of the FLG, we annealed the sample at 400° C for 1 hour in nitrogen. C_{60} molecules are predicted to desorb from graphene at 350° C as shown

by Jee *et al.*[104], while a first approximation would predict that de-intercalation of a C_{60} molecule would require around twice the thermal energy, as two graphene sheets would bind the molecule. Indeed, after thermal annealing, the FLG was again imageable and the AFM image of the FLG after intercalation and annealing is presented in Figure 47 d). A large number of small clusters are present in the imaged FLG, while the recorded step height is still 0.7 ± 0.2 nm. If complete intercalation had occurred the expected height gain would be 1.8 – 2.7 nm. We can thus effectively rule out that complete monolayers of C_{60} exist between the graphitic planes. We cannot however, completely rule out that intercalated molecules were removed by the thermal annealing.

In order to rule out the possibility of de-intercalation during a post-intercalation annealing step, we came up with a different approach. Instead of leaving the quartz tube in the oven during cool down, it is removed for rapid cool down in air. In this way, the tube walls cool down quicker than the wafer. Sublimed C_{60} molecules floating inside the tube are thus preferably captured by the relatively cold tube walls. In Figure 48 we present before and after intercalation images of an FLG flake. The post intercalation optical image of the sample from the rapidly cooled quartz tube in Figure 48 b) show far less cluster formation on the Pt electrodes as compared to the sample from the slowly cooled quartz tube in Figure 47 b). Also, AFM imaging is indeed possible without a prior thermal annealing step. AFM data analysis in Figure 48 e) show a step height from substrate to FLG of 3.3 ± 0.4 nm before intercalation. The same step height is found to be 4.5 ± 0.4 nm after intercalation. Thus we see a height increase of ~1.2 nm upon intercalation attempt. This is very close to the expected height of ~1 nm of C_{60} on graphite[45] and implies no stage-1 intercalation as would be expected from Gupta *et al.*[101] The height increase is thus most likely due to the addition of a single monolayer of C_{60}. Whether the monolayer is on top of the FLG or intercalated (most likely at the SiO_2/FLG interface) is not clear at this point. The simplest way of determining this is probably to scan an area on the FLG with contact mode AFM and see if any C_{60} molecules are removed. We do note however, that previous STM studies of C_{60} on graphite show that islands with more layers of C_{60} are always present when the C_{60} molecules have been evaporated on to the graphite[105,106].

Gupta *et al.*[101] used oxidized and expanded graphite with a considerate amount of holes in the graphitic lattice; while we tried with close to defect free mechanically exfoliated FLG. To test if the type of graphite caused the intercalation attempts to be unsuccessful, we decided to work with graphite similar to that used by Gupta *et al.*[101].

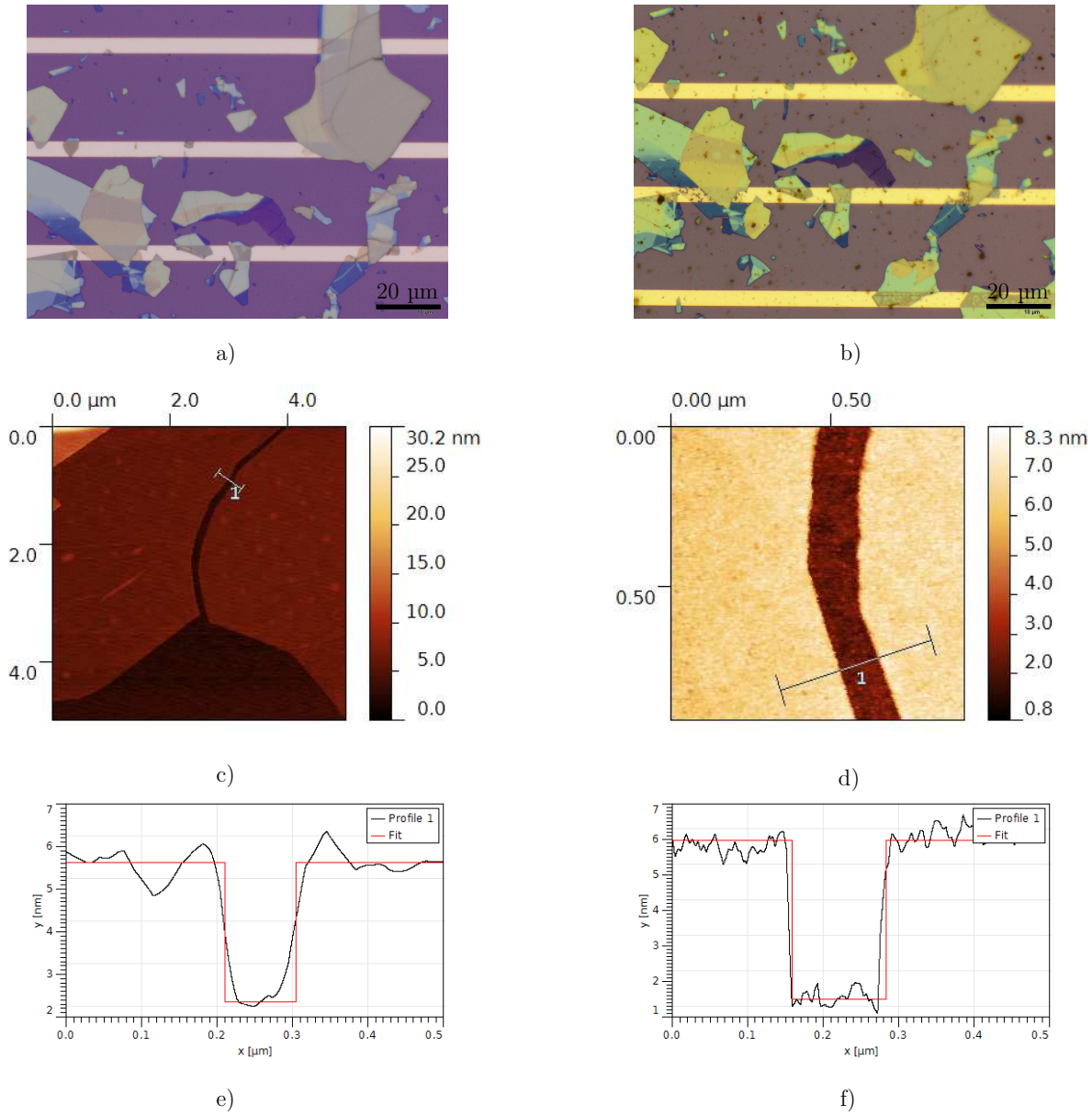

Figure 48. Optical and AFM images of a C_{60} intercalation attempt with rapid cool down. Optical images before a) and after intercalation b) show the addition of many darker spots after intercalation. c) and d) are AFM images before and after intercalation, respectively with the corresponding height profiles presented in e) and f). The step height from substrate to FLG grew from 3.3 ± 0.4 nm to 4.5 ± 0.4 nm after C_{60} intercalation. Figure adopted from reference [100].

4.7.4. Intercalated expanded graphite

As mentioned above, Gupta *et al.*[101] worked with a kind of expanded graphite developed by Chen *et al.*[102]. Their procedure involves an initial step of oxidation and expansion by treatment with sulfuric acid and nitric acid. This highly oxidizing mixture is expected to oxidize our Pt electrodes and instead we decide to use fuming sulfuric acid as it is also expected to intercalate the graphite[107]. Our acid treatment thus consist of 12 – 16 hour soaking in concentrated fuming sulfuric acid, followed by rinsing in Milli-Q water and drying in air.

Initial expansion experiments on mechanically exfoliated graphite/graphene on wafers proved useless, as all graphite/graphene was removed from the wafer by the acid treatment. Most likely it was removed due to intercalation between the substrate and graphite/graphene. Instead we chose to work with solid graphite. First step was then to confirm acid intercalation. Simply weighing the graphite before and after acid treatment showed that the mass consistently doubled by acid treatment. To further confirm the result, we deployed X-ray scattering characterization before and after acid treatment (spectra not shown). Pristine graphite showed the expected 3.34 Å basal plane spacing. After acid treatment, the basal plane spacing was measured to be 3.52 Å, while the spacing was less well defined indicating a broader distribution of basal plane spacings. The increased plane spacing indicates intercalation, while the broader plane spacing indicates that intercalation was not complete.

Prior to C_{60} intercalation, the acid treated graphite was heated to 600° C in nitrogen in order to expand the graphite by de-intercalating the acid molecules. Indeed X-ray characterization showed that the original basal plane spacing for 3.34 Å was retained in correspondence with Chen *et al.*[102]. Unfortunately, the same basal plane distance of 3.34 Å was observed after a C_{60} intercalation attempt. Thus there is no sign of C_{60} intercalation.

4.7.5. Potassium and C_{60} co-intercalated in graphite and FLG

As an alternative to the direct form of C_{60} intercalation suggested by Gupta *et al.*[101], we here investigate co-intercalation of potassium and C_{60} in graphite and FLG. Fuhrer *et al.*[108] suggest co-intercalation with thermal intercalation of potassium to form the precursor C_8K (1 potassium atom per 8 C atoms in the graphitic lattice), followed by solution phase C_{60} intercalation. We tried to reproduce these results but found it impossible to transfer the C_8K precursor to the solution for C_{60} intercalation without rigorous reaction between potassium on the sample surface and the air. The resulting potassium oxide and potassium hydroxide etched into the SiO_2 substrate and made further experimental analysis difficult.

Instead we came up with a co-intercalation scheme done solely in vacuum. It is a two-step thermal intercalation process. The wafer with graphene/graphite is sealed in a quartz tube pumped down below 10^{-5} mbar with solid potassium and C_{60}. The first step is potassium intercalation at 300° C without breaking the vacuum, the quartz tube is heated to 600° C for the second step being C_{60} intercalation. In Figure 49 we present optical images of the result. From before and after images, it is clear that a reaction has occurred. The color of the substrate is completely changed and graphitic flakes have all changed color as well. However, the contrasts observed before co-intercalation due to varying graphite flake thicknesses is gone. Particularly, the large flake at the center of Figure 49 a) and b) had blue and yellow regions before, while the whole flake is turquoise after co-intercalation. If only intercalation had occurred, some contrast due to different flake thicknesses is expected to remain. It thus seems likely that the color of the graphitic flakes stem from a film covering substrate and graphite flakes. It cannot however, be completely ruled out from this simple analysis that co-intercalation had also occurred. Unfortunately, time did not allow further characterization of the sample.

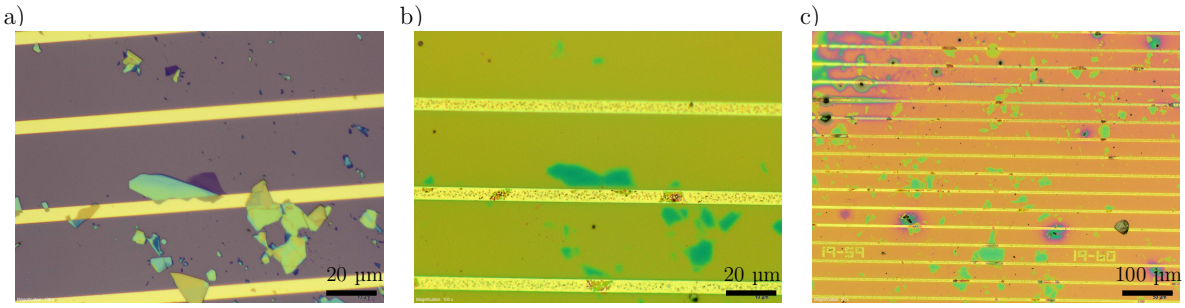

Figure 49. Thermal co-intercalation of potassium and C_{60} in graphite attempt. In a) the sample is imaged before intercalation, while b) and c) show the sample after the co-intercalation attempt. A clear color change is observed for both substrate and graphite flakes after intercalation attempt. Images adopted from reference [100].

4.7.6. Summary and Outlook

Despite having tried several different techniques, we were not able to conclusively intercalate C_{60} in graphene or graphite. Even when we followed procedures very close to those published in the literature as working. As discussed in the following, we find those previous reports less likely to be conclusive now. For example, Gupta *et al.*[101] present a TEM image (shown in Figure 50) as one of their main evidences for successful C_{60} intercalation. The image supposedly shows graphitic planes separated by monolayers of C_{60} molecules. However, with closer inspection and the guide of the hand drawn hexagon in Figure 50, we find that the distance between all C_{60} molecules is roughly the same at 1.5 nm independent of whether or not the molecules are separated by a graphene sheet. This along with the fact that Fuhrer *et al.*[108] explicitly state that they could not make direct thermal intercalation of C_{60} in graphite work, leave us doubtful as to the correctness of Gupta *et al.*'s results[101].

The results obtained by Fuhrer *et al.*[108] show successful co-intercalation of potassium and C_{60} in graphite on the basis of electronic conductance measurement. The intercalated compound with stoichiometry $C_{32}K_4C_{60}$ is predicted to be superconducting[70], which is confirmed by Fuhrer *et al.*[108]. However, Fuhrer *et al.* find a critical temperature of $T_c = 19.5$ K, remarkably close to that found for potassium intercalated solid C_{60}, K_3C_{60} at $T_c = 19.8$ K found by Xiang *et al.*[109]. Fuhrer *et al.* rule out the possibility of K_3C_{60} being responsible for the observed superconductivity. They reason that potassium is present in excess, which enables formation of non-superconducting K_6C_{60}. Before C_{60} intercalation, potassium is present as intercalate

and on the surface of the graphite. Why Fuhrer *et al.* is so sure this amount of potassium is enough to ensure that potassium is in excess, even when they state, "The samples prepared for resistance measurements were exposed to C_{60} concentrations well in excess of the proposed stoichiometry", I don't know. We cannot rule out that K_3C_{60} is responsible for the superconductivity observed by Fuhrer *et al.*[108] and as such there is still no solid evidence of C_{60} ever having been intercalated in graphite.

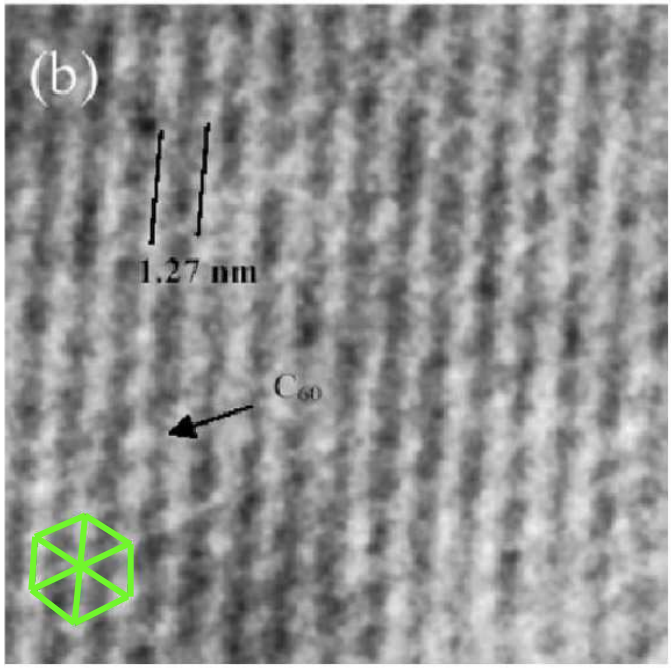

Figure 50 TEM image of C_{60} intercalated graphite adopted from Gupta *et al.*[101]. The green hexagon is a guide to the eye drawn between neighboring C_{60} molecules.

5. Graphene contacts to SAMs grown on gold

In the field of molecular electronics, an often used device geometry is one in which a self assembled monolayer (SAM) of molecules is sandwiched between two metal electrodes[110]. In an effort towards shielding the SAM from penetrating metal from an evaporated top contact[111], previous efforts in the group of my co-supervisor, Bo Wegge Laursen were on deploying reduced graphene oxide (rGO) as a top contact to SAMs[112]. The device architecture is outlined in Figure 51 and consists of a bottom metal electrode passivated with aluminum oxide everywhere but a small well. In the well a SAM is grown and on top of the SAM a top rGO electrode is deposited. Thus a current can run from the source bottom metal electrode, through the SAM to the top rGO electrode. The rGO electrode is fabricated by spin coating and is generally 5-7 nm thick with an electrical conductivity up to 25000 S/m. However, at cryogenic temperatures the rGO becomes insulating[113]. Also, electrostatic gating through 5-7 nm of rGO is expected to be very ineffective[25]. As a further development, we therefore propose to deploy mechanically exfoliated graphene or CVD graphene as top contact for SAMs grown on metal bottom electrodes.

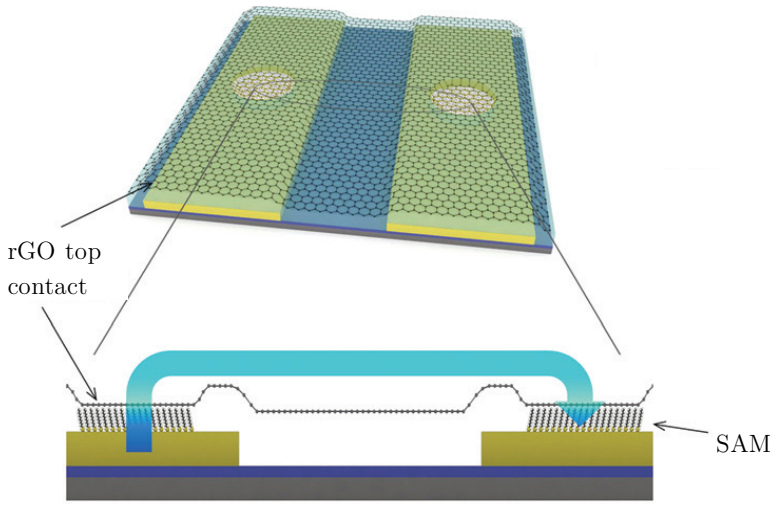

Figure 51 Molecular electronics test bed with a SAM sandwiched between a bottom gold electrode with oxide passivation and a top contact of rGO. Adopted from Li *et al.*[21]

5.1. Mechanically exfoliated graphene top contact

Wet graphene transfer on metal electrodes

The starting point of the experiment is bottom metal electrodes with Al_2O_3 wells fabricated with a combination of UV and E-beam lithography by Ph.D. Rune Hviid. The well diameter is 2 µm, with a distance of 12 µm between neighboring wells. The minimum length for top contact graphene sheets is thus around 25 µm. For statistics more molecular junctions are favorable and in Figure 52 we present images of a +60 µm long BLG aligned on oxide wells. The transfer technique is wet graphene transfer, where the PMMA supported graphene sheet floats on water while alignment is done by hand, as described in further detail in Section 4.3.1. Electrical measurements revealed no contact between the metal electrodes and graphene sheet before or after removal of the supporting PMMA membrane. AFM measurements (not shown) done on the PMMA covered sample indicated that the PMMA had an ordered rippled structure coinciding with the underlying electrode pattern. As seen in Figure 52 b), only BLG parts on top of the electrodes are left after PMMA removal. We believe this is because the BLG and PMMA only had contact to the electrodes and floated over the connecting substrate. To avoid this, we changed from using 1 µm thick PMMA to ~100 nm thick PMMA. In the mean time we also changed deposition technique to dry graphene transfer, as the SAMs were found to reorganize in water.

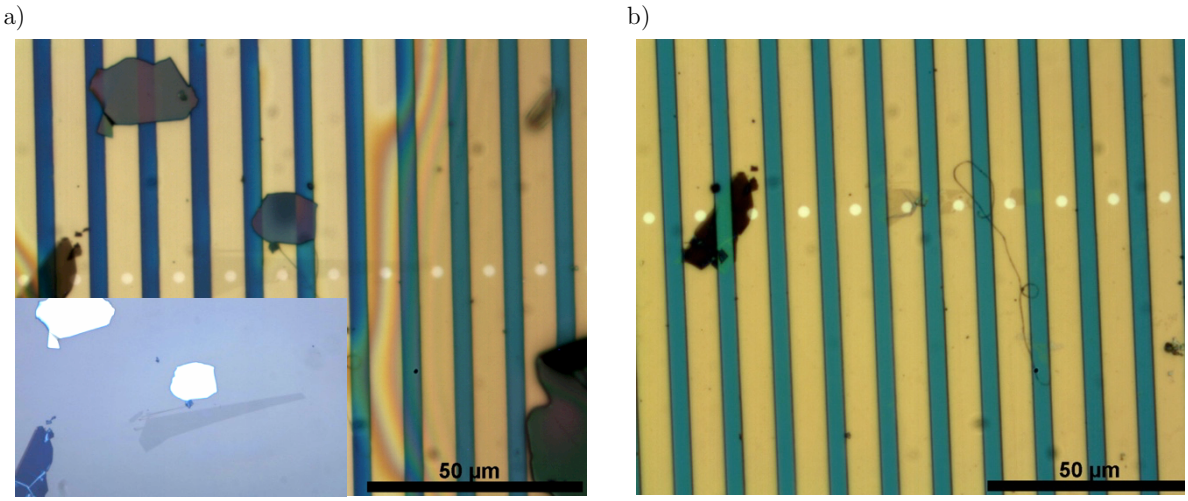

Figure 52. Mechanically cleaved BLG aligned by wet graphene transfer onto metal bottom electrodes. In a) the PMMA used for transfer is still on the sample, while it has been dissolved in acetone in b). The inset in a) shows the 63 µm long bilayer graphene sheet before transfer.

Dry graphene transfer on metal electrodes

In efforts towards deploying mechanically cleaved graphene on metal bottom electrodes, we deposited the biggest mechanically cleaved graphene sheet we have ever made on metal bottom electrodes as shown in Figure 53 with the PMMA removed by acetone. The graphene has an SLG region around 150 µm long and is around 180 µm in total length and was produced using thermal release Nitto Denko tape and naturally occurring large flakes of graphite, as were the majority of mechanically exfoliated graphene presented in the thesis. SAMs of dodecanethiol molecules were grown in the wells prior to graphene deposition. The white lines in Figure 53 serve as a guide to the eye, as the boarder of the SLG region is hard to see in the image.

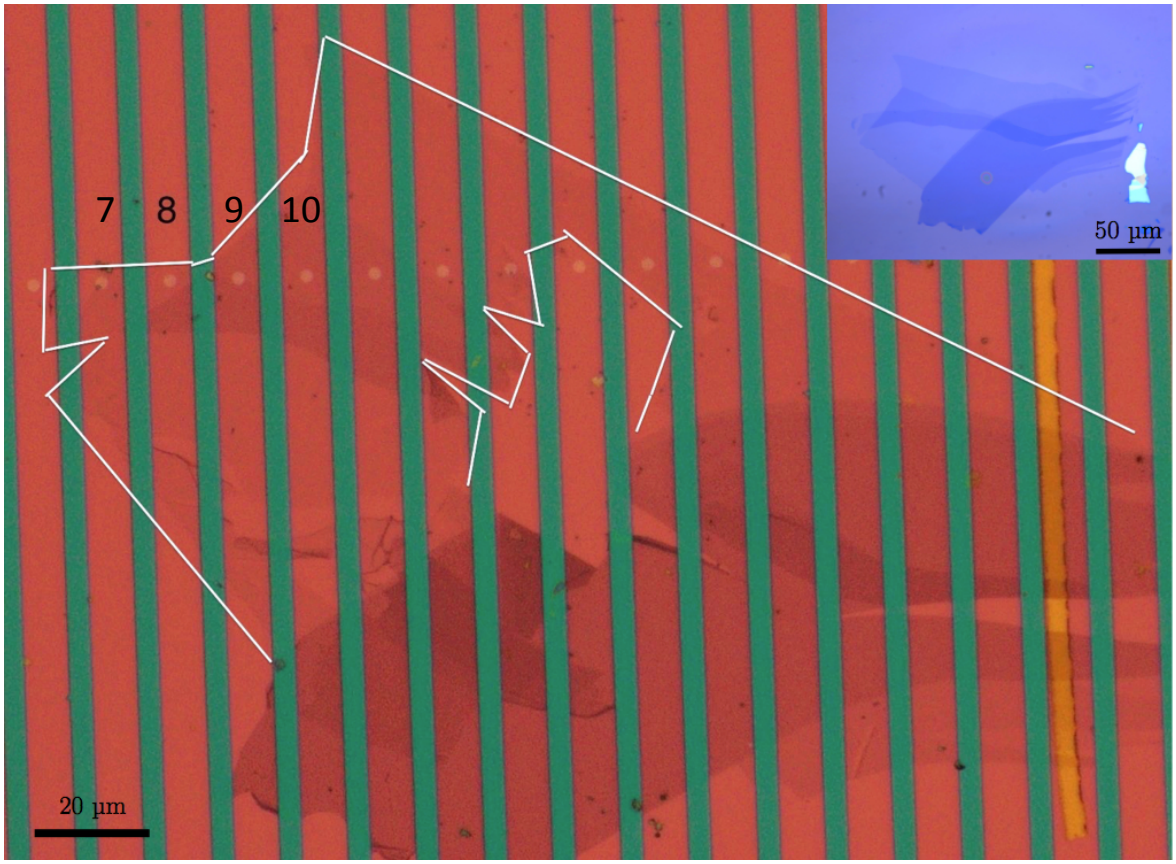

Figure 53. Top mechanically cleaved graphene electrode deposited on SAMs grown on gold electrodes. Electrodes are labeled with numbers for identification. White lines guide the eye to the outer edge of the SLG region. The inset shows the graphene sheet as cleaved on a Si wafer.

In Figure 54 we present resistance measurements and an AFM image of SAMs contacted by the top graphene electrode. Only measurements on metal electrodes 7-9 are presented, as only they had electrical contact to the graphene electrode. The I/V

curves (not shown) were linear and yielded resistances between 4.7 kΩ and 6.5 kΩ. The measured resistances did not show a linear dependence on electrode separation. This indicates that the contact resistances and not the sheet resistance dominated the measurements. For neighboring electrodes, Li *et al.*[112] found an average resistance of 400 kΩ, about a factor 100 larger than ours. They report a rGO film conductivity of 10,000 – 25,000 S/m. With 12 µm between neighboring electrodes this gives around 3 – 8 Ω contributed by the rGO to the series resistance. The resistance discrepancy between the studies can thus not simply be assigned to the difference in top contact. Li *et al.* also measure the resistance on neighbors of electrodes without SAMs. This is reported at 300 Ω. It therefore seems likely that the SAMs in our junctions are partially removed. If our deposited graphene electrode does not effectively isolate the SAMs their surroundings, acetone used to remove the PMMA for graphene transfer may have removed parts of the SAMs as well.

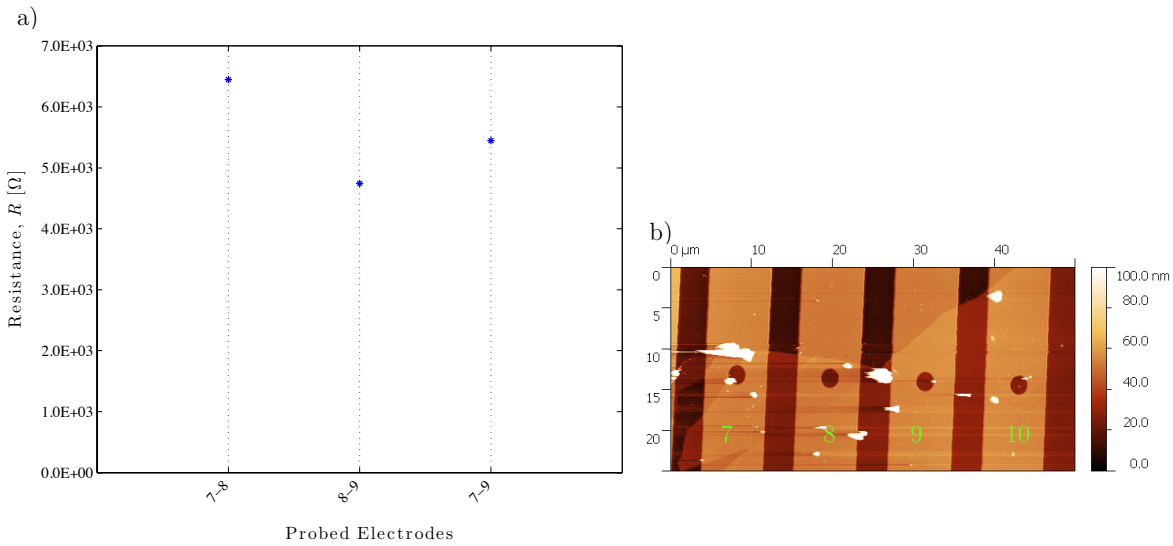

Figure 54. Resistance measurements on SAMs with graphene top electrode in a) and AFM image in b) of the measured electrode pairs.

Due to limited time and other focus areas, this part of the study was not further investigated. If someone is to continue it, I propose to never remove the PMMA used for graphene transfer. Also, the first thing to establish is consistent contact between the top graphene electrode and clean metal electrodes before studying the effects of SAMs in the junctions. Present study does however provide the necessary techniques and a preliminary proof of concept.

5.2. CVD graphene top contacts

We now turn our attention to efforts on deploying CVD graphene as top contact to SAMs grown on bottom gold electrodes. CVD graphene, predominantly single layered, can be readily obtained in large quantities (cm scale)[‡]. Thus precise alignment is not needed and CVD graphene has previously proven it self in vertical transistors[17]. Figure 55 presents a picture of CVD graphene deposited on gold electrodes with SAMs of dodecanethiol grown in aluminum oxide wells. Dry graphene transfer described above is just to deposit the CVD graphene electrode. After deposition, a silicon mask is placed to cover the electrodes imaged in Figure 55, where after the sample is ashed to remove PMMA and graphene on surrounding bonding pads. In the final step, remaining PMMA is removed with acetone. While the graphene membrane has some holes, it is largely intact.

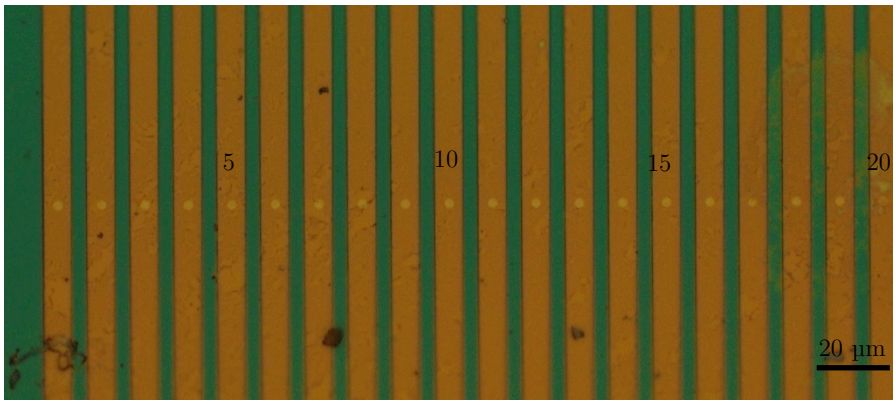

Figure 55. CVD graphene top contact on SAMs grown on gold bottom electrodes. 100 nm thick PMMA used for transfer was removed with acetone.

Figure 56 shows the resistance for six different electrode pairs as a function of temperature. The room temperature values are all between 25 kΩ and 52 kΩ. This is a factor of 5 – 10 higher than for our mechanically cleaved graphene devices and roughly a factor of ten lower than reported for rGO contacts[21]. Again, we do not see any distance dependence and the contact resistance must therefore still be dominant. However, due to the relatively small resistances measured, we cannot rule out that parts of the SAMs are removed by e.g. acetone.

[‡] The graphene supermarket provides many different types of graphene including single layer CVD graphene here: https://graphene-supermarket.com

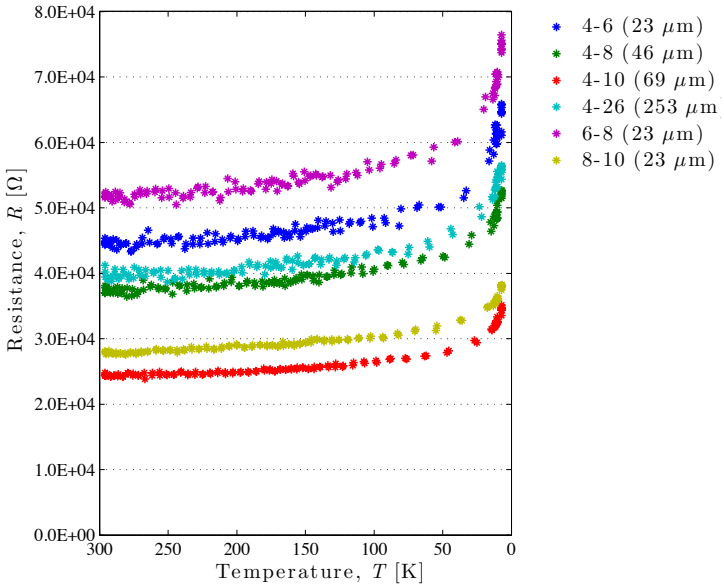

Figure 56. Resistance as a function of temperature for six different electrode pairs. Temperature was lowered to around 10K. The resistance consistently rises with falling temperature for all measured junctions.

5.1. Summary and outlook

For detailed characterization of molecules in a solid-state junction, it is desirable to cool down samples to eliminate thermal vibrations effecting the electronic measurements. To test the applicability of CVD graphene as electrode for cryogenic electronics, we measure the resistance as a function of temperature starting at 300 K going down to 10 K. Noticeably, the resistance consistently increase by less than a factor of 2 going from 300 – 10 K. This is in stark contrast to the measurements on rGO by Hauptmann *et al.*[113]. In their setup, metal is evaporated on top of the rGO film to create vertical Au/SAM/rGO/Au junction. Even with this nm long transport through rGO they see a resistivity increase of around two orders of magnitude going from 300 K to 10 K. Our measurements thus adds to the promise of CVD graphene as electrode in cryogenic molecular electronics. Unfortunately time did not allow a rigorous study to fabricate gate switchable molecular devices with metal bottom electrode. However, my knowledge and experience gained from this project contributed to a paper I am co-authoring on deploying light-switching molecules in a vertical solid-state junction using rGO as top electrode, see paper i) in Section 1.4. Besides general discussions, I particularly contributed to analyzing Kelvin probe force microscopy data presented in the paper.

6. Graphene contacts to nanowires

6.1. Introduction

Semiconducting nanowires (NWs) are often described as effectively being one dimensional due to their nm-scale width and the resulting quantum confinement in the transverse direction. While the width may be down to a few tenths of nanometers the NWs can reach several tenths of µm. Present chapter is concerned with inorganic group III-V NWs.

Semiconducting NWs have shown excellent properties for logic transistor devices and are also considered a candidate for future CMOS application[114]. In addition, NWs can be bend significantly without breaking[115,116] and are thus excellent candidates for high-performance flexible electronics[117]. With graphene as electrode it is possible to obtain not only flexible but also highly transparent electronics due to the optical transparency of graphene. In this section, efforts towards developing a method for connecting indium arsenide (InAs) NWs in parallel using graphene are presented.

A previous example of contacting graphene and NWs is presented by Kierdaszuk *et al.*[118] who deposited CVD graphene on gallium nitride (GaN) NWs and GaN epilayers. Using Raman spectroscopy they found a change a graphene strain and carrier concentration caused by the NW. Furthermore, contactless microwave electrical transport measurements shows a smaller coherence length in graphene on GaN NWs than on the GaN epilayer. However, the authors do not discuss that difference in coherence length is possibly caused by the flatness of the GaN epilayer as compared to the forest of 1 µm high NWs. While the electrical measurements are non-conclusive as to the origin of increased scattering in graphene on GaN NWs, the Raman study do indicate electrical contact between the NWs and graphene. However, Kierdaszuk *et al.*[118] did not deploy source and drain electrodes to fabricate solid-state devices. A method for that is developed here.

6.2. InAs NW growth and band structure

InAs NWs are generally n-type semiconductors, meaning that a bandgap exist between the valence and conductance band while carriers in the conductance band are electrons. The size of the bandgap is found to depend on the diameter of the NW[119]. For the specific cases of InAs NWs with a diameter of 10 nm, 20 nm or 30 nm the bandgaps are found to be ~530 meV, ~440 meV and 403 meV, respectively. The results are explained with size quantization effects and from the above diameter dependence we roughly estimate the bandgap of our 80 nm diameter NWs to be in the vicinity of 300 meV.

InAs NWs similar to the ones used in this study have previously shown near-ballistic transport in InAs NW transistors[120]. Thus the on-current in finished transistors are defined by the ballistic conductance of $G_0 = 2e^2/h$, where e is the charge of an electron and h is the Planck's constant[121]. Chuang *et al.*[120] obtain 80 % ballistic transport from the first conduction band giving a minimum conductance of $G = 0.8 \cdot 2e^2/h \approx 31$ µS for a single NW with 26 nm diameter and ~60 nm channel length. With a channel length of 510 nm the conductance is 7.5 µS.

InAs NWs used in this study are grown by Peter Krogstrup using gold-assisted molecular beam epitaxy (MBE)[122] in a Varian GEN-II MBE system. Via the vapor-liquid-solid (VLS) mechanism[123] InAs NWs are grown from gold particles on the surface of the InAs(111)B substrate. The gold droplets stem from an in-situ deposited gold film, which is annealed in to droplets at elevated temperature. During growth the gold droplets are in the liquid phase and absorb indium and arsenic atoms from the vapor phase. This continues until the gold droplets are super-saturated and indium and arsenide atoms nucleate from the droplets to form solid NWs beneath them. Hence the growth mechanism is termed the vapor-liquid-solid mechanism. For a more thorough description and a theoretical framework for NW growth mechanism see e.g. Krogstrup *et al.*[123]. The particular NWs used in this study have a diameter around 80 nm and are 15 – 20 µm long.

6.3. Device architecture and fabrication

First step in the fabrication is to deposit gold bonding pads and alignment marks on a Si wafer with 285 nm SiO_2. We use e-beam lithography to define bonding pads and alignment marks and evaporate 5 nm titanium and 90 nm gold using e-gun evaporation. The alignment marks work in conjunction with a program written by Ph.D. student Anders Jellinggaard that automatically import and align optical images to a DesignCAD file for later contact designing. For NW deposition, InAs NWs are dispersed in solution by sonication of a mm sized piece of the growth substrate containing NWs in isopropanol for 60 s. NWs are then deposited by drop casting followed by blow-drying with nitrogen. The procedure is repeated until a satisfactory concentration of NWs is achieved.

Initial graphene deposition was done by first dipping the NW containing wafer in a buffered HF solution for 3 – 5 seconds to remove the native oxide on the NWs. The wafer was then quickly moved to a beaker with PMMA supported CVD graphene floating on Milli-Q water. Then we simply picked up the PMMA supported graphene and blew the wafer dry with nitrogen. However, using this procedure, almost all NWs were removed from the substrate. Over several iterations we came out with the final fabrication scheme (steps illustrated in Figure 57):

a) Deposit gold bonding pads and alignment marks on a silicon wafer.
b) Deposit NWs on said wafer using drop casting.
c) Spin coat ~100 nm of ZEP resist[§] and use e-beam lithography to remove ZEP where final graphene contacts are to be.
d) Deposit a single drop of buffered HF on the wafer and leave it for 2 – 3 seconds and immediately after pick up PMMA supported graphene from a water bath (diluting the HF droplet).
e) Then spin-coat 1 µm thick PMMA on the wafer.

[§] We used a ZEP 520A : anisole, 1 : 3 solution spun for 45 seconds at 4500 rpm.

f) Remove PMMA (and ZEP) where graphene is not desired using e-beam lithography and plasma ash the wafer until the exposed graphene is removed/electrically isolating (required time varies significantly form plasma oven to plasma oven).

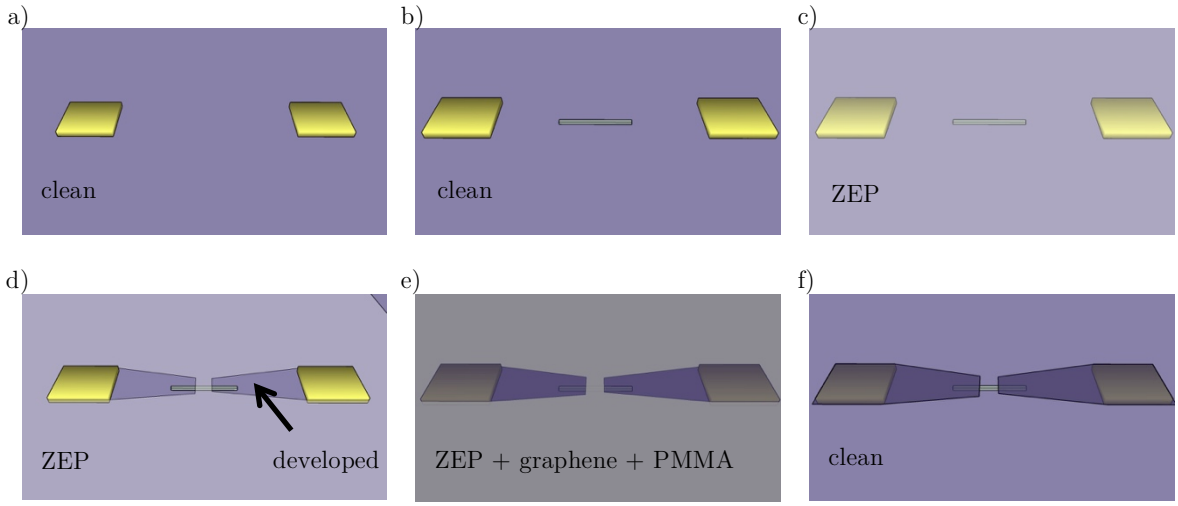

Figure 57. Graphene contacts to NW fabrication scheme. In the first step a) gold bonding pads are formed using e-beam lithography. In the second step, b) NWs are deposited with drop casting from an isopropanol solution. Then ZEP resist is spin-coated on the hole wafer c), followed by e-beam lithography and development of ZEP resist in areas where graphene contacts are desired d). In e) NW ends are de-oxidized with HF, immediately followed by wet transfer of PMMA supported graphene and an extra layer of PMMA is spin-coated on the sample. Finally in f), the area where graphene is not desired is developed using e-beam lithography and the sample is plasma ashed to leave the graphene intact only in the regions defined by the graphene contacts.

Thus after the final step, graphene with PMMA on top covers respective bonding pads and extend on the wafer to make contact to the ends of the NWs as illustrated in Figure 57 f) and images of finished devices in Figure 58. At this point, the rest of the wafer is clean and all ZEP resist has been removed. Important features of the device design is deposition of a ZEP thickness slightly larger than the diameter of the NWs in step c), a maximized contact area between the graphene and NWs in step d), HF de-oxidation of NWs immediately followed by submersion in de-gassed water, deposition of PMMA in e) thick enough to withstand plasma ashing for a duration long enough to render graphene electrically isolating where graphene is not desired.

The optical image of a finished device in Figure 58 a) shows several different device designs. From the top there are two control devices with wide graphene strips connecting two bonding pads each. These devices serve to confirm contact between graphene and bonding pads. Second from the top are top control devices with two wide graphene strips ashed in 8 µm wide valleys. Thus if contact between graphene and bonding pads is confirmed, these devices can confirm the effectiveness of plasma ashing. Below them, 2-point probe (Figure 58 b)) and 4-point probe (Figure 58 c)) graphene contacted InAs NW devices are shown. These devices will be characterized and described in further detail below.

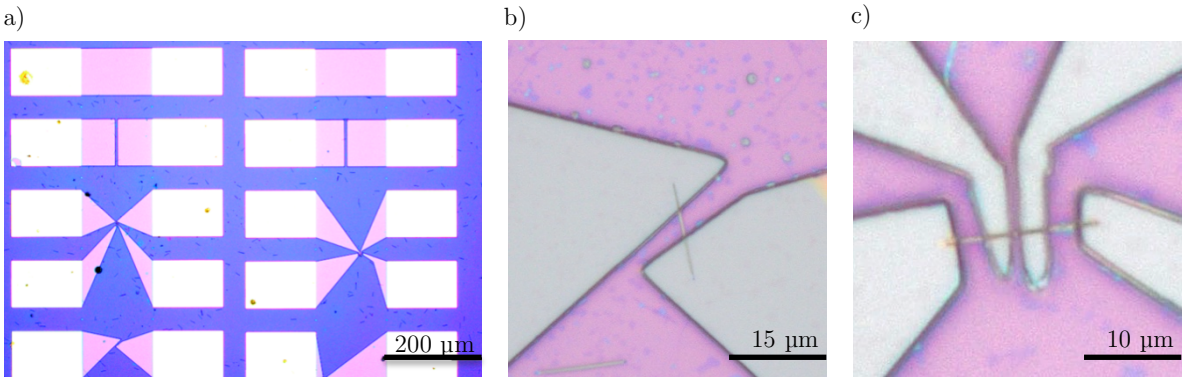

Figure 58. Finished graphene contacts to NWs with bonding pads. In the finished device, graphene only covers the bonding pads, the path between bonding pads and NWs and the ends of the NWs. In a) an overview shows from the top, two control devices with graphene extending between two sets of bonding pads. Second from the top are two control devices with graphene ashed in a region between two sets of bonding pads. Below them are two NWs contacted by 4-point probe graphene contacts. In the bottom, two NWs are contacted by 2-point probe graphene contacts. b) shows a two-point graphene contacted NW with conductance measurements presented below and c) shows a 4-point graphene contacted NW with no observed electrical contact.

6.4. Electronic transport

As shown in Figure 58 a) many devices were fabricated in parallel on a single chip. Each chip contained two types of control devices as well as 2-point and 4 point graphene contacted NW devices.

Graphene only devices

The contact between graphene and bonding pads were confirmed on the two graphene only devices in the top of Figure 58 a) with unbroken 150 µm wide graphene ribbons contacting two bonding pads. On these devices we measured two-

point resistances of ~1.3 kΩ and ~1.4 kΩ with the I/V curves shown in Figure 59 a). From gate sweeps in Figure 59 b) we extracted an electron mobility of 545 $cm^2V^{-1}s^{-1}$ for both samples and hole mobilities of 1350 $cm^2V^{-1}s^{-1}$ and 1550 $cm^2V^{-1}s^{-1}$. Mobilities were calculated using the Drude model[5,98], $\mu = \frac{t}{\varepsilon_0 \varepsilon_r} \cdot \frac{d\sigma}{dV_G}$, where t is the dielectric thickness, ε_0 is the permittivity of vacuum, ε_0 is the relative permittivity of the dielectric and σ is the conductivity. The hole mobilities are almost a factor of two higher than for the graphene ribbons with SiO_2 on top in section 4.6.2 and close to those reported by Venugopal *et al.*[99] for a CVD grown graphene sheet of similar dimensions without deposited SiO_2. Evidently, our wet graphene transfer method does not significantly reduce the mobility of the CVD graphene. The two test samples with the graphene ribbons cut over as seen second from the top in Figure 58 a) conducted no current at 5 mV confirming that ashing rendered the exposed graphene insulating.

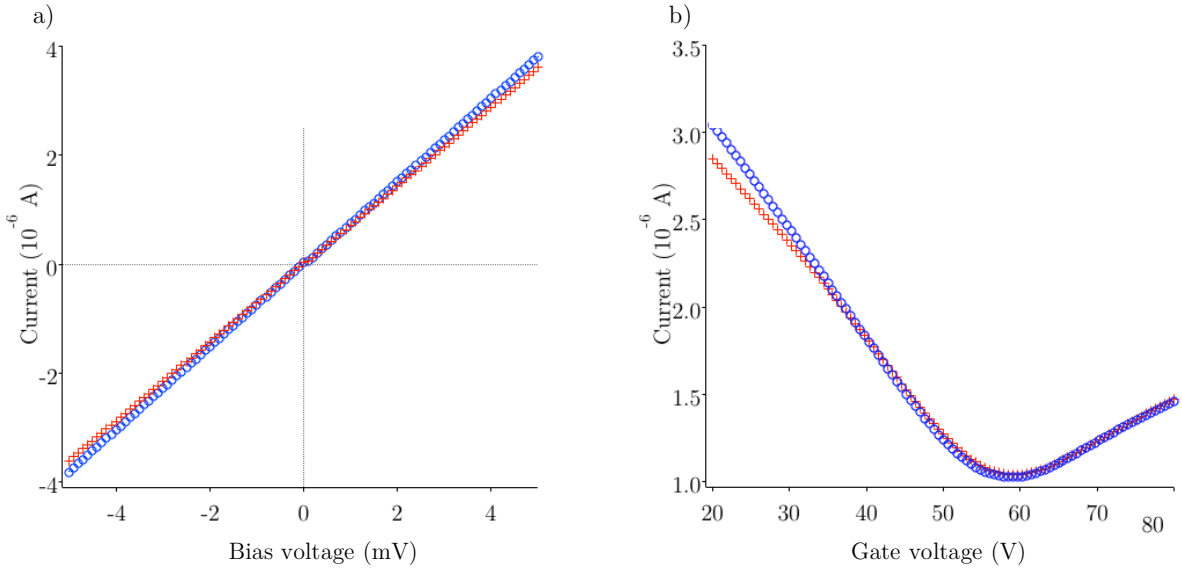

Figure 59. Conductance measurements on the two control graphene devices shown in the top of Figure 58 a). The source-drain voltage is swept in a) and the gate voltage is swept in b). The blue circles stem from the left device and the red crosses stem from the device to the right.

Graphene-NW-Graphene devices

For graphene contacted InAs nanowire devices measurements are less conclusive. On the sample shown in Figure 58 we measured the conductance of 10 2-point probe devices after 90 seconds ashing and again after 60 seconds more ashing (no 4-point probe devices worked). After 90 seconds, nine out of ten devices showed linear

source-drain I/V curves with resistances of 150 $\pm$ 35 kΩ. However, gate sweeps where non-conclusive due to back-gate leakage. After 60 seconds additional ashing, the measured resistance and mobility did not change for the control devices. However, only one graphene-NW-graphene device (shown in Figure 58 b)) retained a linear source-drain I/V curve with and a resistance of 159 kΩ. This device had an insignificant back-gate leakage and the recorded data is presented in Figure 60. The observed uniformly decreasing current with increasing positive gate voltage is inconsistent with the recorded gate leakage current, which showed increasing current with increasing gate voltage. Neither does it resemble the graphene conductance gate dependency as presented in Figure 59 b) with an increase in current as a function of gate voltage for gate voltages above 60 V. Nor does it match the expected behavior of an n-type semiconducting InAs NW as described above with an expected increase in current with increasing gate voltage. One possible explanation, while not confirmed in present study, might be that the observed gate dependency of our graphene-NW-graphene device may stem from a gate dependent contact resistance between the graphene contacts and the NW as observed for other low-dimensional systems[124,125,126]. In this case the measurements as a function of gate voltage describes the electronic properties of the contact interface rather than the intrinsic properties of the gated materials.

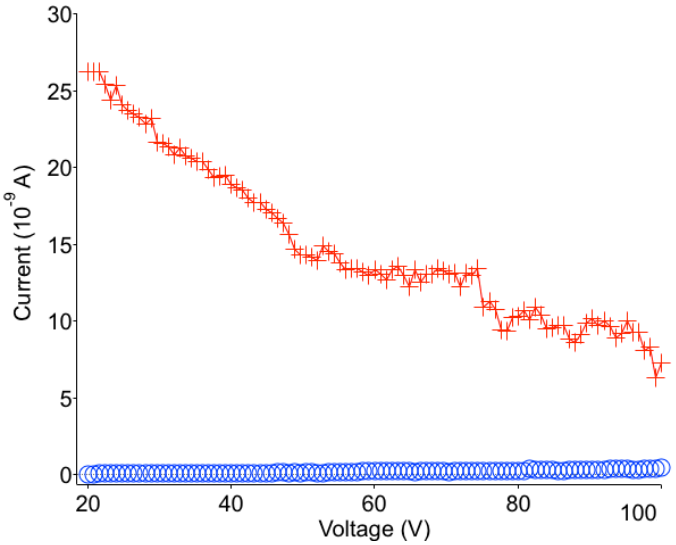

Figure 60. The red curve is a gate sweep of an InAs NW contacted by CVD graphene electrodes with a source-drain voltage of 5 mV. The blue curve is the current recorded between the drain electrode and the gate electrode and is thus similar to the gate leak current.

6.5. Summary and outlook

We developed a method for transferring and patterning CVD graphene on NWs for fabrication of novel lateral graphene-NW-graphene transistors. While electronic contact between graphene and NWs was most likely achieved, we did not obtain a solid proof of this. Additional device fabrication and characterization in accordance with the presented fabrication scheme would allow for such confirmation. An advantageous modification is to introduce an addition step of adding more PMMA for the ashing step and increase the ashing time. In order to ensure optimum contact between NWs and graphene we propose to epitaxially grow NWs directly on graphite/graphene as done in the following chapter.

7. Silver seeded InAs nanowire growth on graphitic flakes for epitaxial graphene contacts

Recently, results from our group showed that in-situ growth of aluminum contacts on InAs NWs can indeed give epitaxial contact[127] and that this give rise to exceptionally good electronic contact between the superconducting aluminum and the semiconducting NWs[128]. Following the many efforts towards contacting semiconductors with graphene presented in the previous chapters, we finally decided on an entirely different strategy: to epitaxially grow semiconducting NWs directly on graphene. Self-catalyzed InAs NWs have previously been grown on CVD graphene by Mohseni *et al.*[129], while many of the remaining reports of InAs NW growth on graphene show very low aspect ratio NWs[130]. There also examples of Au seeded GaP NWs grown on graphite[131] and self-catalyzed GaAs NWs and graphite and few layer graphene[132].

In this proof of concept study we show that InAs NWs can indeed be grown with high aspect ratio on graphitic flakes and very likely also on graphene by use of silver-seed particles. Furthermore, we show that silver catalysis may be key to grow high aspect ratio InAs NWs on graphitic substrates – even in growth conditions similar to those for gold catalyzed InAs NW growth on InAs substrates. The graphitic flakes with as grown NWs are transferred mechanically to transmission electron microscopy (TEM) grids and insulating substrates suitable for device fabrication.

I planned the experiments to be carried out, designed the InAs NW-graphene system, prepared growth substrates and did the SEM analysis. Peter Krogstrup determined growth parameters and carried out MBE growths. Thomas Kanne Nordqvist did all the TEM and TEM related characterization and analysis. A paper[iv)] is soon to be submitted as described in section 1.4.

7.1.1. Silver deposition and droplet formation

Prior to actual NW growth attempts we studied silver deposition and droplet formation on graphite and few layer graphene (FLG). Graphene/graphite flakes were deposited on SiO_2/Si wafers using mechanical exfoliation with thermal release tape from Nitto Denko. 1 nm silver was e-gun evaporated on the samples followed by thermal annealing in nitrogen. We annealed samples at 600° C or 700° C for 15 min and saw no detectable difference in droplets formed at these two temperatures. SEM images of the result of annealing at 700° C is shown in Figure 61. As is evident from Figure 61 a) the droplet density varies from flake to flake. From the thickness of the flakes apparent from the SEM image, it seems that the density on the thinnest flake in the middle of the image is larger than the density on the thickest flake in the top left corner of the of the image. While this effect is not at all confirmed, it could be related to different diffusion coefficients for silver on different flake thicknesses as observed for gold by Zhou *et al.*[133].

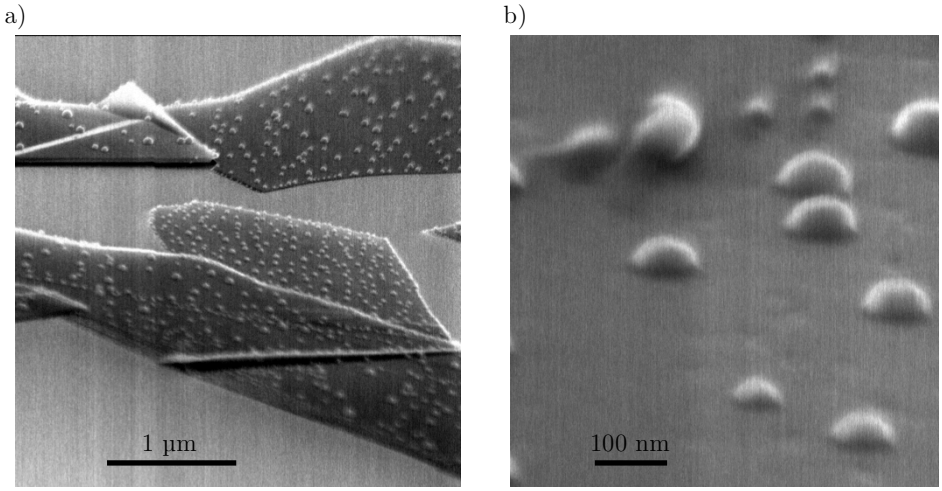

Figure 61. Silver droplet formation on graphite and FLG. 1 nm e-gun evaporated silver annealed for 15 min at 700° C. Silver on graphite/FLG flakes of various thicknesses in a) and silver on FLG in b).

7.1.2. Silver seeded InAs NWs on FLG growth attempt

Having confirmed silver particle formation on graphite and FLG, we performed a NW growth attempt with SEM images of resulting structures presented in Figure 62. Graphite/graphene was deposited on SiO_2/Si wafers by mechanical exfoliation, followed by ex-situ silver deposition. We tested silver thicknesses of 0.5 nm, 1 nm, and 5 nm, the 5 nm sample being presented in Figure 62. All samples including a test sample of InAs(111)B, commonly used for MBE growth of InAs NWs[122,134], with 1 nm ex-situ deposited silver were exposed to the same growth session. Substrates were annealed in-situ at 600° C for 10 min followed by growth at 600° C with a Ga/In ratio of ~73 and a projected planar growth rate of 0.2 µm/hour. As evident from the SEM images of the graphite/FLG sample with 5 nm silver presented in Figure 62 there are multiple elongated structures on the graphite flakes after growth. All other samples from the same growth had less elongated structures. Several of the structures in Figure 62 have particles on top possibly indicating seeded growth. Also, the density of elongated structures is highest on the imaged graphite/FLG flakes with lowest height as observed for silver particle formation above. While structural analysis has not been performed, we suggest that the elongated structures do indeed consist of InAs and the particles on top are silver particles. The size of particles after growth varies a lot but are similar in size (mean diameter around 100 nm) to the particles observed after an annealing step presented in Figure 61. Interestingly, no elongated structures are observed on the SiO_2 substrate. This can be because of the increased mobility of silver and or InAs particles on graphite/FLG as compared to SiO_2 and/or because of a better lattice match between InAs and graphite/FLG than between InAs and the somewhat disordered SiO_2. Indeed, graphite and FLG have no dangling bonds in their pristine forms while SiO_2 has a surface terminated by various oxide groups with dangling bonds and charge puddles[27].

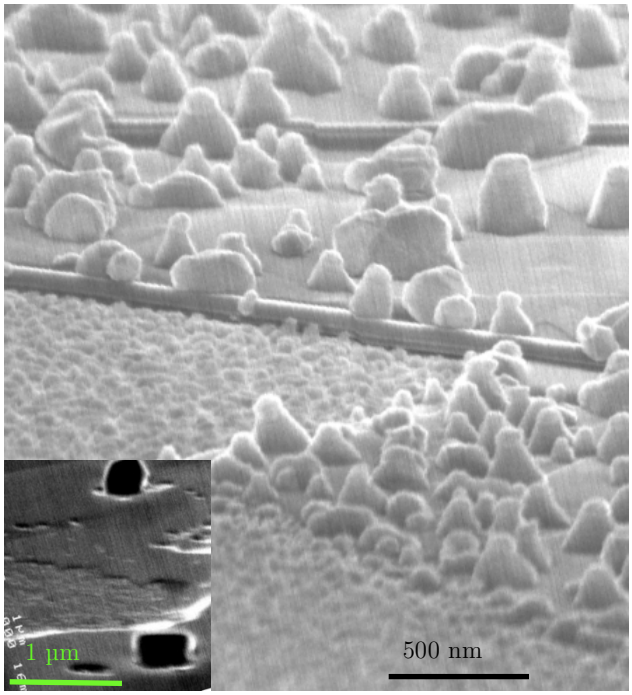

Figure 62. Silver seeded InAs NW growth attempt on graphite and FLG (5 nm silver deposited ex-situ). On graphite/FLG we see many elongated shapes with apparent particles on top. The density of elongated particles is seemingly relatively large on the thinner flake in the lower right part of the image. There is no obvious formation of elongated particles on the SiO_2 substrate. In comparison we see much fewer and thicker particles on InAs(111)B as shown in the inset. The two samples are from the same growth.

7.2. Silver seeded InAs NW growth on graphite and FLG

Following the growth of elongated InAs structures on graphite we designed another growth with a build in control experiment as illustrated in Figure 63 a). Graphite and graphene flakes were mechanically exfoliated directly on two different clean InAs(111)B substrates conventionally used for InAs NW MBE growth[122,134]. Thus both samples also serve as test samples. Graphite and graphene is mechanically exfoliated directly on a single piece of InAs (111)B substrate, which is subsequently cleaved to form to identically prepared samples. Then 1 nm Silver is deposited on one substrate and both substrates are fastened to a wafer mounted on the MBE sample holder. On both samples 0.5 Å gold is deposited in situ. Thus one substrate had just gold deposited and the other had both silver and gold deposited as illustrated in Figure 63 a). Substrates were annealed in-situ at 600° C for 10 min before growth. For this growth the growth temperature was 417° C, the Ga/In ratio

was ~15 with a projected planar growth rate of 0.6 µm/hour. These values in the growth window are far from those chosen in the growth described in the previous section.

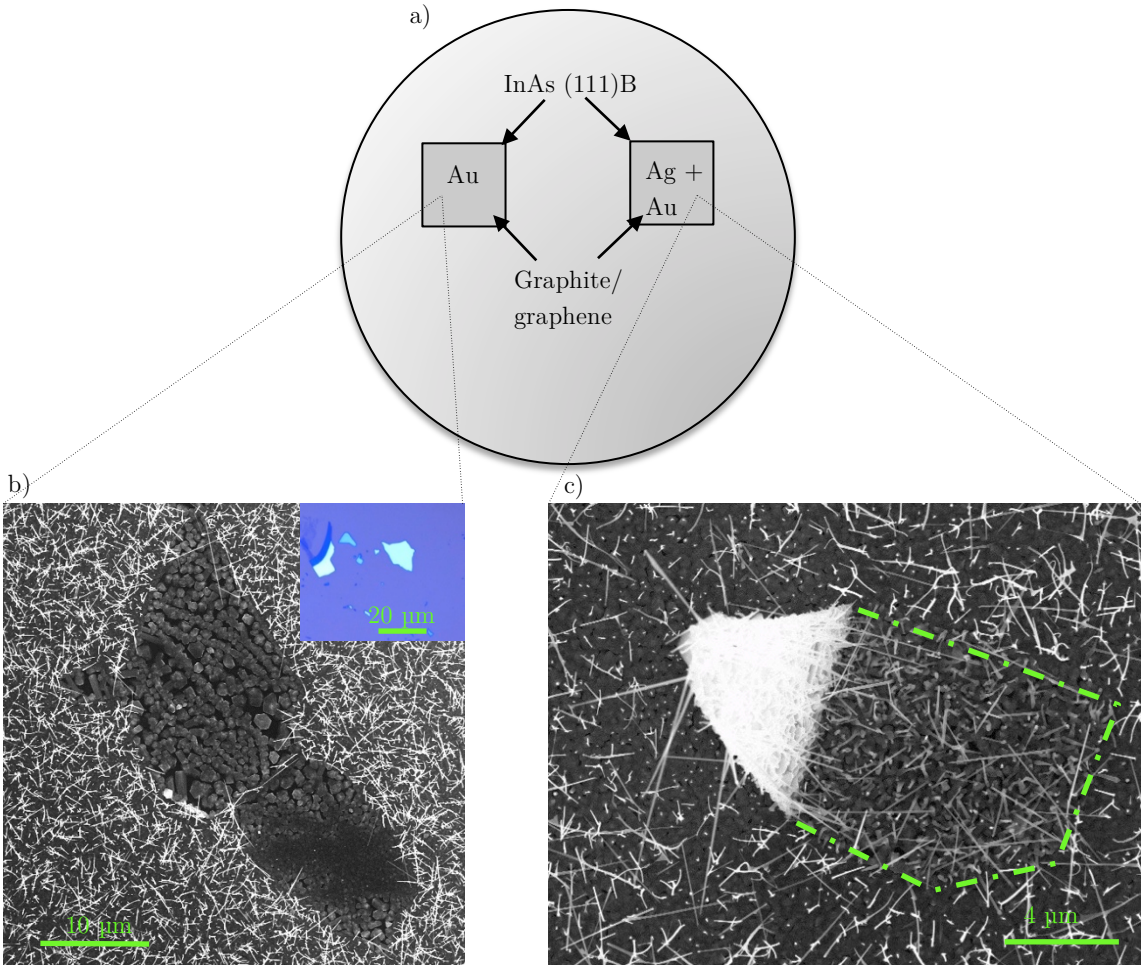

Figure 63. Single growth with two growth substrates mounted on the same sample holder. Graphite and graphene is mechanically exfoliated directly on a InAs (111)B substrate, the substrate is cleaved in two and 1 nm silver is deposited on one substrate. Both substrates are fastened to the same wafer and mounted on the MBE sample holder followed by in situ gold deposition as illustrated in a). An SEM image of a graphitic flake on the growth substrate without silver is presented in b) with an inset of an optical image of a representative graphitic flake on SiO_2. In c) an SEM image of a graphitic flake with pre-growth deposited silver comprising a free-standing part on the growth substrate is presented. The green dashed line indicates the expected perimeter of the graphitic flake.

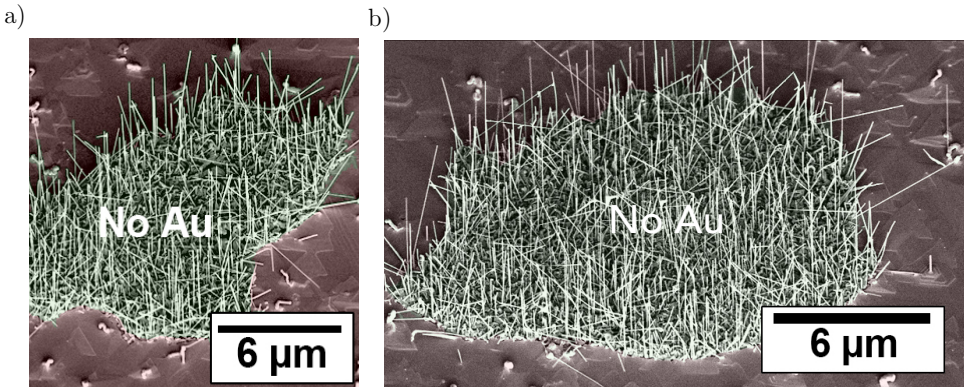

Figure 64. From the same growth as described in Figure 63. On this part of the growth substrate, 1 nm silver and no gold was deposited. NW growth is observed only on the graphitic flakes as shown in a) and b). Red color is added to the InAs (111)B substrate to add contrast to the graphitic flakes with NWs having a green color added.

The SEM images of graphitic flakes without and with pre-deposited silver presented in Figure 63 b) and c), respectively reveal a striking difference in NW growth on graphitic flakes. During SEM characterization, we additionally found that part of the silver containing substrate had not received any gold due to a shadow from the sample holder during gold deposition. On the sample with no silver, no NWs were observed in many areas on the growth substrate interpreted to comprise graphitic flakes as illustrated by the representative SEM image in Figure 63 b). Conversely, NW growth was observed on graphitic flakes with pre-growth deposited silver. This is particularly clear on free-standing graphitic flakes as observed in Figure 63 c). Furthermore, the growth from the substrate with silver only reveals NW growth from the graphitic flakes but not the surrounding InAs substrate as shown in Figure 64. This clearly indicates that the InAs NWs grown from the graphitic flakes are indeed silver-seeded and that silver does not catalyze InAs NW growth on InAs (111)B under these growth conditions.

Gold seeded growth attempt on InAs and graphite

A representative image of growth from the substrate with deposited gold only, is presented in Figure 65. The image shows substantial NW growth on the InAs substrate but no growth on areas similar in shape to commonly observed graphite and graphene flakes on SiO_2 as illustrated by the inset. Many NW free areas similar to that in Figure 65 were observed with a density similar to that commonly observed for mechanically exfoliated graphite and graphene on SiO_2. Furthermore the NW free areas contain grain like structures, whereas the surrounding area has a more coherent structure of the substrate. The missing two-dimensional growth in the NW

free areas corresponds well with the expectation that dangling-bonds-free graphite/graphene[80,135] exerts lower friction on ad atoms as compared to InAs(111)B[136]. The NW free areas are thus interpreted to have graphite or graphene flakes covering the InAs substrate. We note that single layer graphene does not completely screen properties of the substrate such as wetablity[137] and friction[133] and that it is not impossible that structures growing on single layer graphene would be affected by the atomic structure of the InAs substrate. In this case we would expect regions with NW density larger than zero but lower than on the InAs substrate. While this phenomenon is observed on Figure 66, it remains unconfirmed whether or not an SLG or FLG covers the InAs substrate in this area. Experimental proof of such phenomenon would have fundamental implications for the nature of graphene transparency.

After our experiments were performed we realized that gold seeding InAs NW growth on graphite had been presented just before our studies were conducted[138]. While a direct comparison of growth parameters is not possible as they use metal organic vapor phase epitaxy growth and we use MBE growth, we do note that their InAs NWs have a substantially tapered structure and lengths below 1 µm.

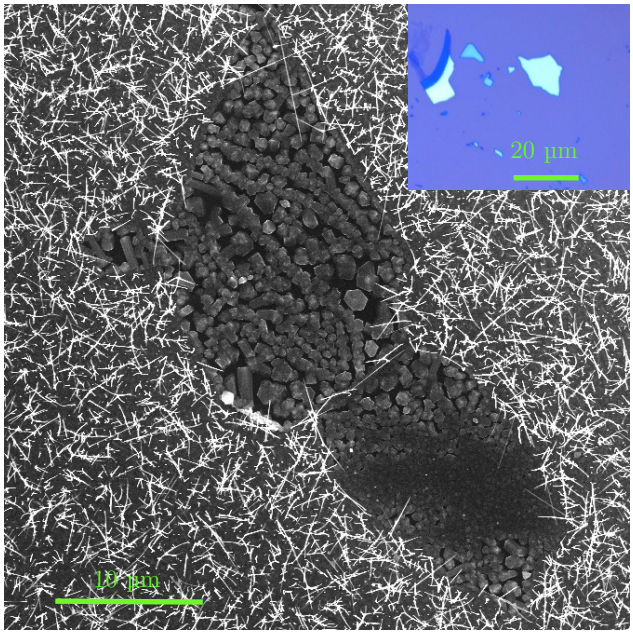

Figure 65. SEM image of gold seeded NW growth from substrate with graphite/FLG flakes mechanically exfoliated on InAs(111)B. The top view image shows abundant NW growth in the area surrounding similar to commonly observed graphitic flakes as the ones shown in the inset.

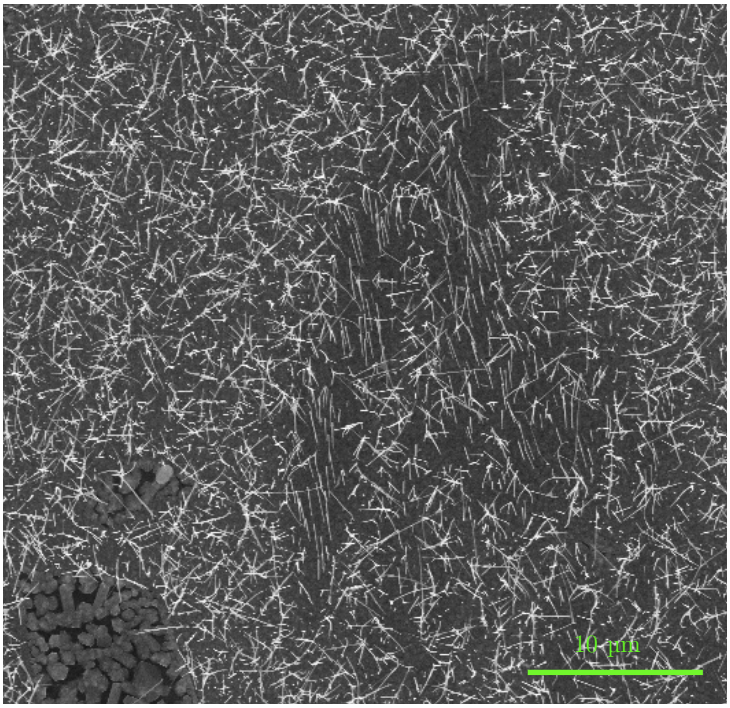

Figure 66. SEM image of gold seeded NW growth from substrate with graphite/FLG flakes mechanically exfoliated on InAs(111)B. An area in the right part of the image has lower NW density than the surrounding substrate.

Silver seeded NW growth on crystalline graphitic flakes

To investigate seed particle compositions on NWs grown in different areas, we transferred graphitic flakes with as-grown NWs as well as NWs grown on the InAs (111)B substrate to TEM grids. This was enabled by use of a micromanipulator to pick up individual flakes and deposit the NW decorated flakes on TEM grids using the micromanipulator.

In Figure 67 we present TEM images and energy dispersive X-ray (EDX) analytical analysis of NWs grown on a graphitic flake in b) and on the InAs (111)B substrate in c). The EDX spectrum recorded on the seed particle on a NW grown on a graphitic flake shows a peak where the Kα peak of silver is expected and essentially a flat line where the Lα peak of gold is expected. For a seed particle on a NW grown on the InAs (111)B substrate the EDX data shows quite the opposite: gold is detected and silver is not. This data confirms that NWs grown on the graphitic flakes are silver seeded and NWs grown on the InAs (111)B substrate are gold seeded – even when both gold and silver were present on either substrate before growth.

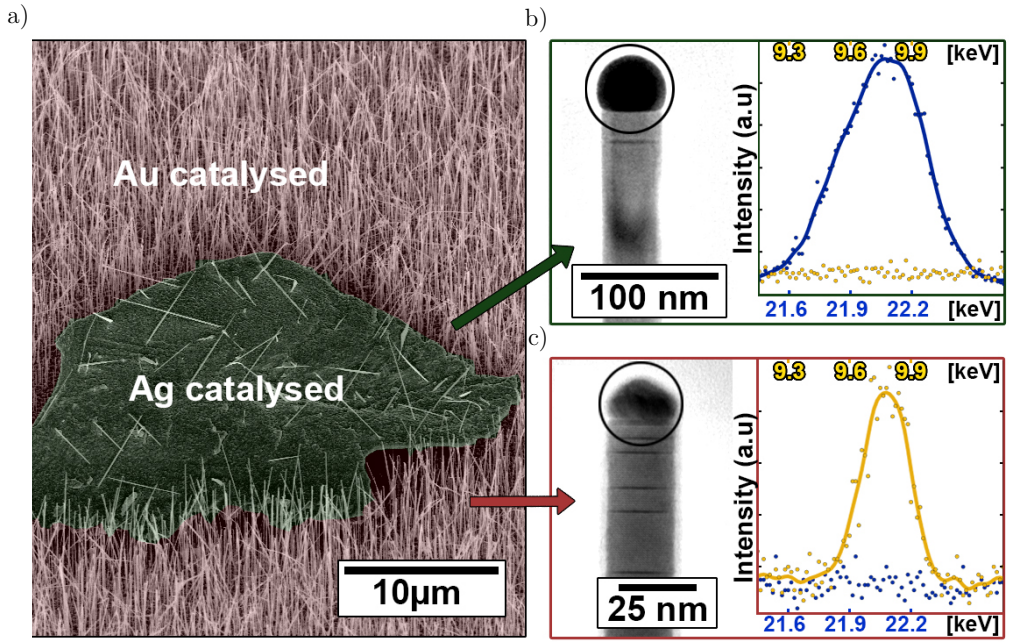

Figure 67. NWs grown on graphitic flakes with silver seed particles and NWs grown on InAs (111)B with gold seed particles. The SEM image in a) shows NWs grown from a graphitic flake with a thickness of several microns as well as NWs grown from the InAs (111)B substrate. In b) a TEM image of a NW from a graphitic flake clearly shows a seed particle terminated NW and the EDX spectrum recorded on the seed particle exhibits a peak at 22 keV where the Kα peak of silver is expected (blue dots and scale), while there is no sign of gold at the Lα peak of gold at 9.7 keV (yellow dots and scale). In c) the seed particle of a NW grown from the InAs (111)B substrate is confirmed by EDX to contain gold (yellow dots and scale) but not silver (blue dots and scale).

Substrate epitaxy

As epitaxial NWs grow in distinct direction corresponding to individual crystal orientations depending on the crystal orientation of the growth substrate, the growth direction depends on substrate crystal orientation. In Figure 68 we observe NWs grown on a more than 1 µm thick flake and a relatively thin flake well below 100 nm (the exact thickness is unknown but may later be determined by e.g. Raman spectroscopy or AFM analysis). Qualitatively, NWs grown on the thin flake predominantly have a growth direction perpendicular to the graphitic substrate. Conversely, the NWs grown on the thick graphite flake grow in a direction not perpendicular to the graphitic substrate. The observed preferred growth direction confirms that the NWs are indeed grown epitaxially.

Further analysis is needed to confirm the graphite thickness growth direction dependency. However, the observed phenomenon indicates that the thin flake may be transparent to the epitaxy of the InAs (111)B substrate. Previously, it has been shown that the hydrophilicity of a substrate shines through sufficiently thin graphitic flakes[139]. It has also been shown that the friction coefficient changes for gold on graphitic flakes of various thicknesses[133]. It is thus reasonable to assume that a similar epitaxy transparency of graphene could be observed for epitaxial NW growth.

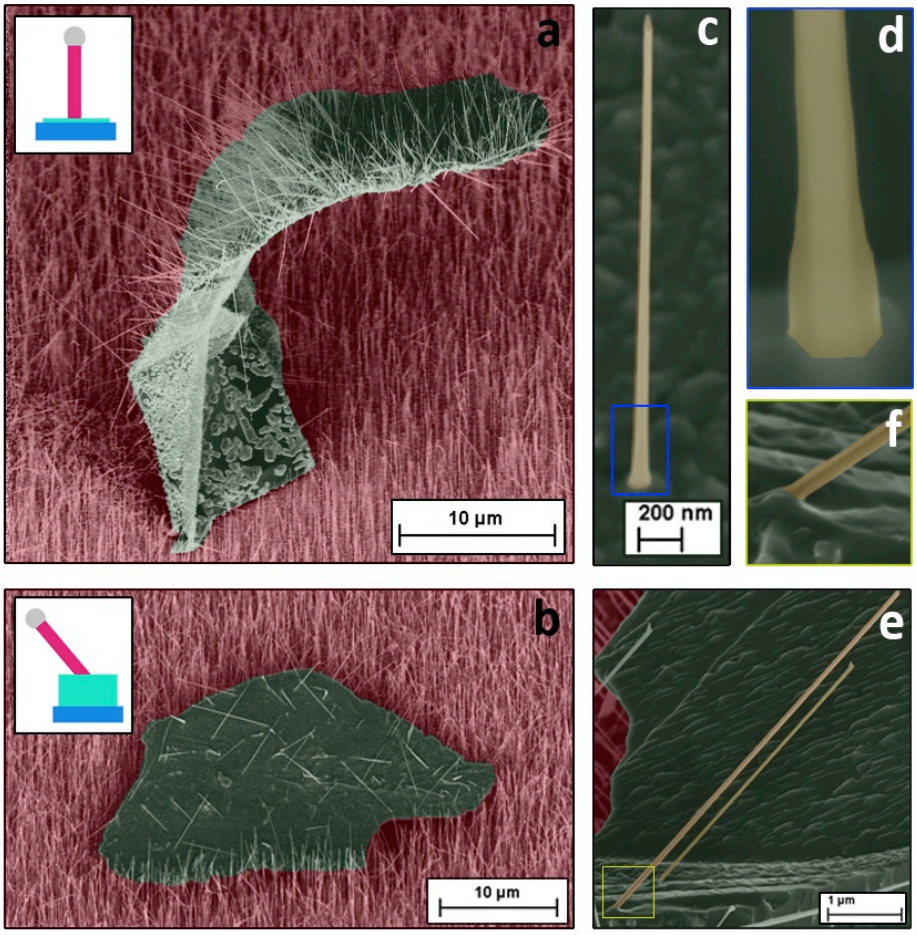

Figure 68. SEM images of NW growth on graphitic flakes recorded at 45° tilt angle. In a) a thin layer of graphite is imaged after it was picked up and dropped by a micromanipulator. Most of the nanowires grow perpendicular from the graphitic flakes like they do from the InAs (111)B substrate. In b) NWs grown on a more than 1 µm thick flake grow in a direction not perpendicular to the graphite flake. c) and d) are zoom ins on wires on the thin graphitic flake in a) and e) and f) are zoom ins of wires on the thick graphitic flake in b).

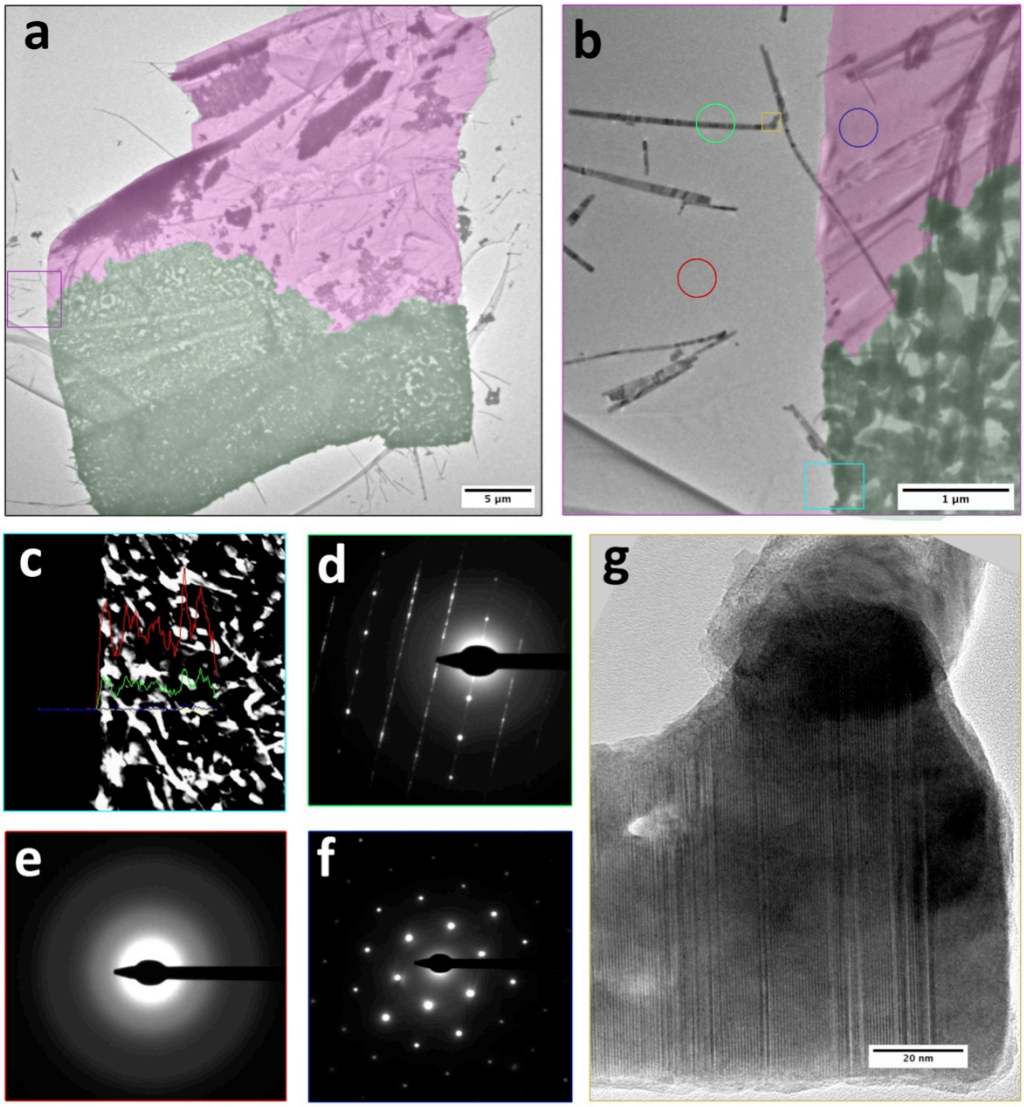

Figure 69. Figure a) and b) show TEM images of the growth substrate with NWs. The purple color is added to segregate the exposed graphitic from the substrate growth from the substrate growth material covered part market by a green color. The substrate growth material has most likely pealed off the now exposed graphitic flake during mechanical transfer to the TEM grid. In c) a HAADF-STEM image with an EDX line scan is presented. In the EDX line scan, the red curve is As, the green curve is In and the blue curve is Ag. A SAED (Selected Area Electron Diffraction) pattern of an Ag-seeded nanowire is presented in d). It shows signs of zinc blende and wurtzite crystal structure observed along a [110] and a [$\bar{2}\bar{1}\bar{1}0$] direction, respectively. In e) is a convergent beam electron diffraction pattern of the amorphous carbon film (TEM-grid). In f) a SAED pattern of the growth substrate shows the signature pattern of the hexagonal graphitic crystal lattice. Finally, g) is an HR-TEM image of the top of a silver seeded NW showing irregular crystal growth.

TEM analysis of growth system

As described above, we transfer entire graphitic flakes with grown NWs onto TEM grids. This allows for an unprecedented ability to study the entire growth system in

TEM. In Figure 69 we present TEM analysis of the growth system comprising the graphitic growth substrate with attached epitaxially grown NWs and separate NWs. The TEM images in Figure 69 a) and b) reveal parts of the growth substrate with substrate growth material. High angle annulling dark field (HAADF) scanning transmission microscopy (STEM) images combined with an EDX line scan in Figure 69 c) show that the substrate growth material is InAs with no signs of silver. Furthermore, we analyze electron diffraction patterns recorded on a NW, the amorphous carbon TEM grid membrane and the growth substrate presented in Figure 69 d), e) and f), respectively. From the diffraction pattern in d) we see that the NW crystal structure is a mixture of zinc blende and wurtzite, which is also confirmed in the high resolution (HR) TEM image in g). The diffraction patterns in e) and f) show the amorphous structure of the carbon TEM grid membrane and show the signature diffraction of a perfect hexagonal graphitic crystal lattice, respectively.

The just presented analysis confirms the hypothesis of our growth method providing the possibility to perform a full TEM analysis of the growth system.

Transfer to device fabrication substrate

The versatility and applicability of the present growth method is further emphasized by the possibility of transferring the graphitic flakes with as grown NWs to an insulating substrate for device fabrication. In the case where the flakes are transferred to substrates with prefabricated bottom source and drain electrodes, the use of solvents and lithographical processes on the flakes and NWs may be avoided entirely. Here, as a proof of concept we transfer a graphitic flake with as grown InAs NWs to a Si substrate with 285 nm SiO_2. As is evident from the SEM image in Figure 70, the NWs remain attached to the graphitic flakes and attain their upright orientation.

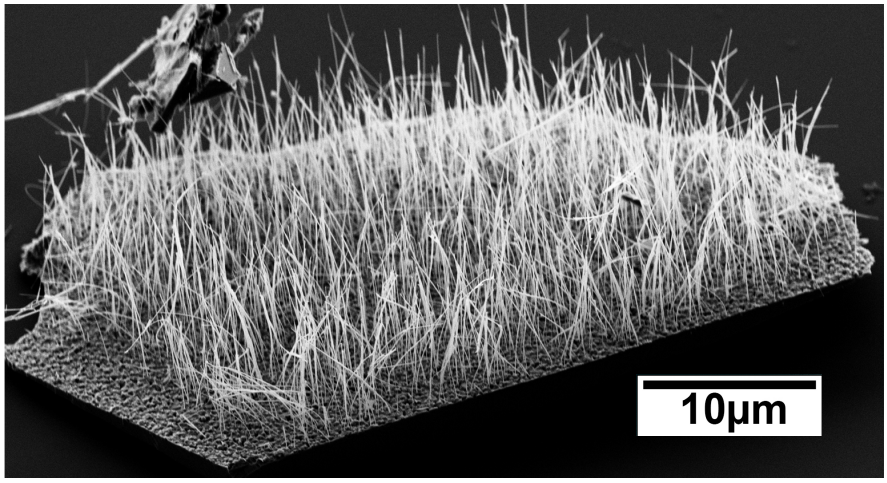

Figure 70. SEM image of a graphitic flake with as grown InAs NWs transferred to a Si substrate with 285 nm insulating SiO_2 recorded at 45° tilt angle. The NWs remaining attached to the flake are generally vertically aligned.

7.3. Discussion and outlook

We have shown for the first time InAs nanowires can be grown on graphitic flakes by silver seeded MBE growth, likely epitaxially. Also, we report for the first time InAs NWs with a uniform morphology and high aspect ratios (>250) on graphitic flakes in general. Under the same growth parameters, silver-seeded NWs are grown from graphitic flakes and gold-seeded NWs are grown from InAs (111)B. Furthermore, NWs are not grown from graphitic flakes in the absence of silver and NWs are not grown from the InAs (111)B substrate in the absence of gold. This allows for selective growth in particular areas by deliberate choice of substrates and seed particle materials. Also, observations suggested that thin graphitic flakes might be transparent to the epitaxy of InAs substrate. To confirm this observation, a growth with graphitic flakes of different known thicknesses should be carried out.

Time did not allow for any electronic characterization of present InAs NW graphite system. However, as discussed in the introduction, epitaxial growth of metal on NWs has proven effective in providing optimum electrical contact between the NWs and metal. We thus hypothesize that present epitaxial interphase contacts can provide optimum contact between the semiconducting NWs and graphitic flakes highly relevant for future integration of graphene as contact to finite bandgap semiconductors.

From a NW growth optimization and fundamental material science point of view our method for making the entire growth system available for full TEM analysis holds great promise for future discoveries.

8. Conclusion and outlook

As is evident from the previous chapters, I have pursued many different routes towards achieving graphene contacts to finite bandgap semiconductors. The initial goal of making a functioning Carbon Burger vertical transistor was not met. However, the experimental techniques developed along the way towards the Carbon Burger might prove useful for implementation of graphene as contact to molecular thin films in general. Transfer of graphene with precise alignment was optimized for both a wet and dry transfer method. Indeed, the wet transfer of CVD graphene proved very gentle on the graphene retaining the mobility after transfer. NW lithography proved useful for defining oxide trenches on graphene and enabled solvent free definition of nm-scale features on a graphene flake. The most important result perhaps was the development of CVD graphene bottom electrodes formed in parallel with oxide passivation everywhere but a predefined exposed area for contact with molecules of choice. These bottom graphene electrodes might prove useful as a testbed for molecules to be employed in graphene based molecular devices. With the bottom electrodes defined in CVD graphene, vertical transistors comprising such electrodes may be flexible and transparent to light on a suitable substrate, while the graphene allows for deployment of a backgate. As far as I know, the graphene bottom electrodes with oxide wells presented in this study are the first of their kind. The next step would be to explore varies molecules deposited on these bottom electrodes and deposit top CVD graphene electrodes on promising molecular films to fabricate molecular vertical transistors.

If a vertical transistor with graphene as electrode is to be realized, I propose a device partly anticipated by Yu *et al.*[17]. The authors present a vertical transistor with a CVD bottom electrode, MoS_2 finite bandgap semiconductor and metal top electrode as described above. I simple propose to employ a CVD graphene top electrode instead of the metal top electrode to achieve a transparent and flexible vertical transistor. Such a device was actually fabricated by Yu *et al.* for photocurrent generation[140]. Also, memory cells based on graphene and MoS_2 heterostructures have

been demonstrated by Bertolazzi *et al.*[141] completing the list for a future self-powering, all graphene/MoS_2 based computer.

As another approach towards achieving graphene contacts to finite band gab semiconductors, we developed a fabrication scheme for lateral graphene-NW-graphene devices. Such devices in them selves would also be flexible and optically transparent. While fully functional devices were not achieved, I believe it is merely a matter of repetition and little optimization before such devices could be realized.

The method developed for epitaxial growth of InAs NWs on graphitic flakes can prove to be central for the development of novel graphene/NW heterostructure devices. The expected optimum electrical contact between the NWs and graphene can, if confirmed, aid the development of ultra-sensitive optical sensors as energy loss due to NW-contact resistance is minimized. Also, with controlled growth of InAs NWs comes the possibility of tuning the NW diameter and hence bandgap to absorb light of almost any desired wavelength. Furthermore, NW growth on graphitic flakes enables extensive TEM analysis of entire growth systems. This new characterization possibility might serve to bring new advances in the field of NW growth and materials science in general. The transfer of graphitic flakes with as grown NWs to other substrates further enables device fabrication without the need to expose the NWs or their contacts to any solvents or lithographical processes. This in turn may ensure optimum conditions for utilizing the inherent properties of said materials. Moreover, the growth method present several advantages over the state of the art with the highest aspect ratios achieved for semiconducting NWs on graphitic flakes, transferable growth systems and the possibility of positioned NW growth with the use of silver seed particles. Additionally, the growth parameters used are compatible with those for the well-known growth of gold-seeded InAs NWs grown on InAs substrates. As it turns out, the parameter space that has been well explored for InAs NWs grown on InAs substrates might prove applicable for silver-seeded InAs NW growth on graphitic flakes.

To continue the NW growth on graphitic flakes study, I would suggest depositing the graphitic flakes on for example SiO_2/Si substrates prior to growth. This would enable post-growth deposition of a polymer followed by wet etching to selectively

etch away the SiO_2 without damaging wires or graphitic flakes. At this point, the wet and dry graphene transfer methods developed for the Carbon Burger enables convenient transfer and precise alignment on a desired substrate. Alignment on prefabricated bottom electrodes would then be straightforward.

Throughout the thesis several viable routes towards achieving graphene contacts to finite band gab semiconductors have been developed and presented. The final result of direct growth of InAs NWs on graphitic flakes stands as the most promising and viable route towards optimum electrical contact between graphene and finite band gab semiconductors. Having concluded my Ph.D. thesis, I still believe the most promising future for graphene in tomorrow's electronics is as contact to other semiconductors acting as active components in transistors, memory cells and photo-current generators.

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