UNIVERSITY OF COPENHAGEN
FACULTY OF SCIENCE

PhD Thesis

Quantum transport in hybrid nanostructures

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Submitted: October 2, 2022

This thesis has been submitted to the PhD School of The Faculty of Science, University of Copenhagen

ABSTRACT

In recent years a new material platform — a semiconductor nanostructure with a superconductor shell — has grown to become an important player in the field of electronic quantum transport. This, so-called *hybrid material*, embodies the characteristics of both constituent materials and is now widely used to study complex quantum phenomena. A particularly prosperous example of today is the semiconductor/Al nanowire. This work presents three experiments seeking to expand beyond the by-now established hybrid semiconductor/Al nanowires.

The first experiment concerns an unexplored type of superconductor within the context of hybrid nanowires – that is Pb. We probe InAs/Pb nanowires in a tunnel configuration and find that the Pb thin film superconducts up to a critical temperature of 7 K and exhibits a pairing energy of 1.25 meV which persists in parallel magnetic fields beyond 8.5 T. Andreev bound states and Yu-Shiba-Rusinov states are investigated in magnetic fields showing similar behavior to their Al-based equivalents. In addition, we expose hybrid Pb-based islands to large magnetic fields and find a variety of expected as well as more exotic ground state parity transitions.

The second experiment revolves around microtomy, the technique of cutting thin lamellas of materials embedded in a resin. We use microtomy on arrays of InAs and InAs/Al nanowires and find that we can fabricate electronic devices on arrays of nanowire off-cuts still embedded in their resin. Once cooled to cryogenic temperatures, the devices show quantized phenomena such as conductance quantization, single-electron charging and wave interference. As both vapour-liquid-solid growth of nanowires and microtomy are techniques capable of large through-put production, we argue that the combination of these techniques is a promising alternative route for scalable production of quantum devices. As an outlook, we show how the platform could be extended to networks forming looping and crossing geometries.

The third experiment is a comparison between Al junctions on InAs nanowires formed by ex-situ etching versus in-situ shadowing. From high-resolution electron microscopy we find that the most commonly

used etching protocol results in atomic-scale roughening of the nanowire surface. Electronic transport on symmetric transistor devices with both shadowed and etched junctions shows a reduction in carrier mobility across the etched junctions likely linked the surface roughening. In addition, we provide a set of more advanced in-situ shadow geometries which could aid in bringing hybrid device fabrication further in-situ. In the end, we give examples of devices based on junctions formed in-situ showing signs of ballistic transport and superconducting quantum interference.

DANSK RESUMÉ

I de seneste år er en ny materialeplatform — en halvleder-nanostruktur med en superledende ydreskal — blevet en vigtig aktør inden for elektronisk kvantetransport. Dette, såkaldte *hybridmateriale*, udviser begge materialers egenskaber og anvendes nu i vid udstrækning til at studere komplekse kvantefænomener. I dette arbejde præsenteres en række eksperimenter, der forsøger at udvide udover de allerede etablerede InAs/Al- og InSb/Al-hybridnanotråde.

Det første eksperiment omhandler en uudforsket type superleder i forbindelse med hybride nanotråde, nemlig Pb. Vi undersøger Pb/InAs-nanotråde i en tunnelkonfiguration og finder, at den tynde Pb-film er superledende op til en kritisk temperatur på 7 K og udviser en parringsenergi på 1.25 meV, som vedvarer i parallelle magnetfelter ud over 8.5 T. Tunnelleringsresonanser af Andreev-bundne tilstande og Yu-Shiba-Rusinov-tilstande undersøges i høje magnetfelter og udviser lignende adfær som deres Al-baserede ækvivalent. Desuden undersøger vi hybride Pb-baserede øer under høje magnetfelter og finder en række forventede og mere eksotiske grundtilstandsparitetsovergange.

Det andet eksperiment drejer sig om mikrotomi, en teknik til at skære tynde lameller af materialer indlejret i en resin. Vi anvender mikrotomi på rækker af InAs- og InAs/Al-nanotråde og viser, at vi kan fremstille elektroniske kredsløb på store rækker af nanotrådeafskæringer, der stadig er indlejret i den omkringliggende resin. Når kredsløbene nedkøles, viser de kvantiserede fænomener såsom kvantiseret ledningsevne, enkeltelektronopladning og bølgeinterferens, hvilket lover godt for en alternativ rute til højkapacitets-produktion af elektroniske kvanteenheder. Tilslut viser vi, hvordan platformen kan udvides til netværk af vertikalt fusionerede nanotråde, der danner sløjfe- og krydsningsgeometrier.

Det tredje eksperiment fokuserer på en strukturel og elektronisk sammenligning mellem superledergab dannet i hybride InAs/Al-nanotråde ved hjælp af ex-situ ætsning og in-situ skygning. Ved højopløsningselektronmikroskopi finder vi, at den typisk anvendte ætsningsprotokol resulterer i ujævnheder på atomar størrelsesorden i nanotrådsoverfladen. Elektronisk transport på symmetriske transistorkredsløb med både skyg-

gede og ætsede gab viser en reduktion af ladningsbærermobiliteten i de ætsede gab, hvilket sandsynligvis er forbundet med den ætsningsinducerede perturbation af overfladen. Følgende fremsættes der ideer til mere avancerede in-situ-skyggegeometrier, som kan bidrage til at bringe fremstillingen af hybride kredsløb helt in-situ. Til sidst giver vi eksempler på højkvalitetsgab fremstillet in-situ, som udviser ballistisk transport og stabil superledning ved lave temperaturer.

ACKNOWLEDGEMENTS

I will start this section out by breaking tradition. Instead of mentioning my supervisor first, I give **Thomas Kanne** my first and deepest expression of gratitude. We met already a week before the start of our first semester at a *brush-up* course hosted by the UCPH. Already during that week I got the feeling that this might be one of those special friendships that you stumble across only a few times in life. I was right. From 2011 to 2022 beer and cigarettes on Tuesdays turned into long hours at the lab, and I know that I will miss our daily match of 'idea-ping-pong' when our lives aren't centered around the second floor anymore.

Returning to etiquette, I want to extend my sincerest gratitude and congratulations to my supervisor, **Jesper Nygård**. First, I want to thank you for absorbing me into your group – for a second time. I thrive under a long leash and an open door policy, both of which you have facilitated in stellar fashion. Second, I want to congratulate you for the way you run a highly successful lab without ever loosing the human touch. That is no small feat.

In the spring of 2020 a skateboarding accident left me with a badly broken wrist. Little did I know that the accident coincided perfectly with **Aske N. Gejl** spending his environmental exchange at QDev. I want to extend my deepest gratitude, not only for literally becoming my right hand for 6 weeks, but also for our close friendship and deep talks throughout the years. Never has a broken hand felt sweeter.

I want to thank **Kasper Grove-Rasmussen** for being a fantastic guide further into the realm of quantum devices. Your positive and kind spirit combined with your deep wealth of knowledge is one-of.

Also, I want to thank the next generation scientists within our small group, **Oskar Leiva Perstølen**, **Daniel Kjær** and **Daniel Ross** - the last two also known as *double D(aniel)* or *Daniel*^{2}. Your curiosity and hands-on attitude is inspiring, and I'm sure both traits will serve you well in the future. For what its worth, I'm happy to have been your guide.

Talking about the next generation, now is a great time to deeply thank my good friend and colleague, **Rino**. The origin of your name is still a mystery to me, but I nonetheless expect our tradition to repeat itself about 3 years from now. Everybody could learn a thing or two from you – be it your wealth of knowledge on Italian coffee grinders or your beautifully underplayed demeanor.

Whenever I was in dire need for a second opinion about fabrication or a tip about the fridge, **Alexandros Vekris** never failed to deliver. Thanks for *everything* and I hope your post-graduation gaming PC lives up to your high demands. kek!

When I was in the lab only to chat to people, T12 was always a stop on the line. A deep-felt gratitude goes out to **Dags Olsteins** – I enjoyed all our talks massively. Either fun or deep, they were always great.

I want to thank **Asbjørn Drachmann** for being the kind-hearted, good-spirited and hard-working person you are. Also, I want to thank you for that high-five 10 months ago when I told you I had just quit coffee cold-turkey. I needed it.

I also want to thank the amazing technical staff of **Claus B. Sørensen, Lars Lemming, Jesper Kock, Nader Payami, Inger Nielsen, Karolis Parfeniukas** and **Martin Bjergfelt** for always keeping the lab running like Swiss clockwork.

Also, a very special thanks goes out to the wizards behind the science that are our administrative staff. **Maria Batista** and **Katrin Hjorth**, you've probably had the biggest impact on my work here in QDev without me knowing about it. Your efficacy, professionalism and good spirits have never been less than amazing.

I want to thank the following people in random order: **Alexander Whiticar, Sangeeth Kallatt, Joost van der Heijden, José Manuel Chávez-Garcia, Will Lawrie, Martin Espiñeira Cachaza, Erik Cheah, Serwan Asaad, Shivendra Upadhyay, Damon Carrad, Davydas Razmadze, Alisa Danilenko, Saulius Vaitiekėnas, Fabio Ansaloni, Gunjan Nagda, Fabrizio Berritta, Michaela Eichinger, Zhenhai Sun, Kian Gao, Oscar Erlandsson, Lazar Lakic, Lukas Stampfer, Andreas Pöschl, Harry Lampadaris, Juan Carlos Saldana, Christian Petersen, Steffen Zelzer, Joeri de Bruijckere, Rawa Tanta, An-**

ders Kringhøj, Fuffi, Antonio Fornieri, Sabbir Khan, Jordan Kang, James Mingchi, Xiangyu Lin, Robert McNeil, Liv Nørgaard, Denise Puglia, Miķelis Marnauza, Keita Ohtani, Mohana Rajpalke, Katrine Rasmussen, Tomaš Stankevič, Karolis Parfeniukas, Martin Bjergfelt, Katrine Rasmussen, Merlin von Soosten, Elizabeth Knipschildt and **Judith Suter**. Thank you for making the small moments magical, be it a coffee break, a lunch (mediocre tasting at best) or a power cut.

Talking about magic, I cannot let the skate crew consisting of **Mads G. Andersen, Emil Hyldahl, Martin Hallberg, Jonas Ehlers Nilsson** and **Anders P. Olsen** go unmentioned. Our chats on nonsensical skateboard-trivia and the mysterious ways of life have always brought me back into balance.

I want to extend my deepest feelings of gratitude to the close friends unrelated to my studies. I want to thank **Theodor Thiele, Thobias Thiele, Peter Rohde, Anders P. Olesen, Andreas Henriksen, Daniel Ross** and **Sebastian Jezewski**. You will probably never read this, and for exactly that, I am truly grateful.

Last, I would like to extend my innermost gratitude to my father **Hans**, my mother **Gunhild**, my brother, **Jakob** and my sister in law **Fanny** and their lovely kids. I want to thank you all for being the loving and peculiar family you are. It is hard to explain in words how much your help, understanding, strength and love, means to me. Tak for alt.

Joachim E. Sestoft
Copenhagen
October 2022

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CHAPTER 1

MOTIVATION & INTRODUCTION

THE *information age* was ignited in the mid 20th century as traditional industries were surpassed by a rapidly evolving economy based on information.[1] At the heart of this economy was storing and manipulation of information, which in a more practical sense, was enabled by the transistor – an electrical device which could be turned ON and OFF. The vast scale of the information-based economy can perhaps best be understood if one were to count all transistors ever made, and it turns out, such estimates exist. The number of transistors produced between 1955 and 2014 (Fig. 1.1) amounts to more than a sextillion (that is, a number followed by 21 zeroes), arguably making the transistor the most numerous man-made object of all time.[2]

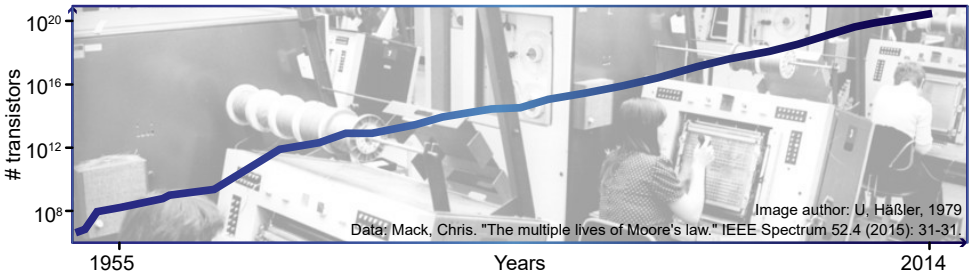

Figure 1.1: Estimation on total cumulative number of transistors from 1955 to 2014. *Artwork: Women working the assembly stations in Dresden, Germany in 1979 (U. Häßler)*

In search for an answer on how such vast numbers were achieved technically we can turn to a prediction described by George Moore in 1965. Moore's law, as it was later dubbed, proposed that the number of transistors placed on integrated circuits would double approximately every two years. Naturally, this lead to transistors shrinking over time.[3] As the years passed leading industry experts kept failing to predict the ending of Moore's law, and tran-

sistors have now reached the atomic scale. At these sizes quantum mechanical effects start to govern, and to give an example, transistors on the order of 10 nm experience quantum tunneling between their gate electrodes.[2] As we are operating at the limits of the classical laws and the *information age* demands ever-increasing computational capabilities, it seems the time is right to start exploring quantum mechanical laws to manipulate information and tentatively enter the *quantum information age*. And indeed, technologies enabling this will be the overarching theme of the thesis — quantum mechanical effects in transistor-like devices.

The coming of the quantum information age is not news to scientists, especially not theoretical physicists and computer scientists who have proposed many different types of quantum bits (qubits) and quantum algorithms over the years. In fact, already in the 1980s Richard Feynman predicted how the laws of quantum mechanics could be wielded to produce computational bits the sizes of atoms.[4] A physical structure which seemed to meet most forth-put requirements was the *semiconductor nanostructure*. Candidly, this sparked a flourishing interest in nanostructures such as nanowires, self-assembled quantum dots and carbon nanotubes, among many other types.

Lately, nano-scaled crystals combined with superconductors, we call them *hybrid materials*, have been getting increasing traction as they facilitate studies of many interesting quantum phenomena. Their appeal lies in how the properties of both materials spill into each other, as sketched in Fig. 1.2 **a**. Here a region between a slab of semiconductor and a slab of superconductor can exhibit characteristics of both materials. Specifically, the hybrid semiconductor/Al-based nanowires stand out as they have provided the necessary platform for many new insights.[5, 6, 7, 8] They uniquely combine sets of physical properties (*superconductivity, large spin-orbit coupling, high carrier mobilities, high g-factors, quasi-one-dimensionality*) with the capacity to being specifically tailored morphologically and structurally (*width, length, radial composition, axial composition, networks*). This concoction of ingredients provides a highly engaging playing field for the condensed matter physicist. In Fig. 1.2 **b** we plot the number of articles concerning hybrid materials versus time, showing the beginning years of a research field which has expanded ex-

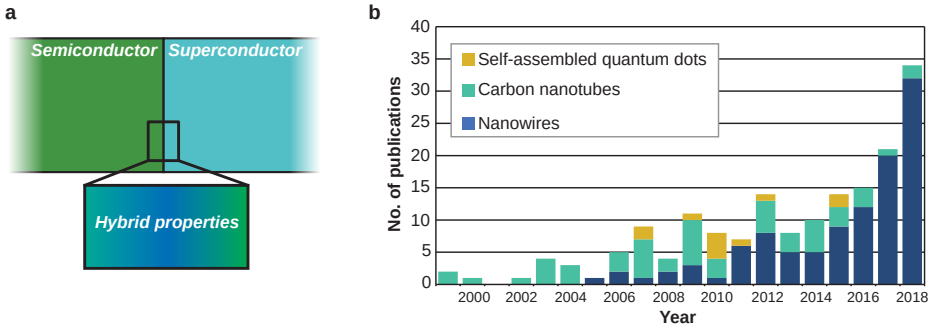

Figure 1.2: **Hybrid materials and their evolution.** **a**, A slab of semiconductor and a slab of superconductor in close proximity. Zoom-in illustrates a region around the interface exhibiting properties of both materials. **b**, Number of publications related to quantum wires joined with superconductors over time.

ponentially since the discovery of Al grown epitaxially on InAs in 2015.[9, 10]

Projecting into the future, we are likely going to find that advances in quantum technologies are tightly bound to improvements in material design and quality, and perhaps even being at its mercy. From this foothold, it seems important to investigate other avenues beyond the by-now established Al-based nanowires and unearth new experimental tools and insights enabling challenging and fascinating future ideas.

1.1 Thesis walk-through

This thesis presents a set of experiments performed on different hybrid nanostructures – with the basis for all studies being the InAs nanowire.

First, Chapter 1 is continued by introducing the theoretical basics that distinguish semiconductor crystals from other types of materials. Next, we move to the other component of the hybrid nanostructure, the superconductor. Here we introduce the main concepts of the Bardeen-Cooper-Schrieffer theory before the discussion is extended to Andreev reflection and electronic transport of *superconductor-normal metal* tunnel junctions.

In the second half of the introduction we move to Coulomb spectroscopy in superconducting islands. Here floating superconducting islands are described from the foothold of the ground state model developed for single electron transistors.

Chapter 2 briefly introduces the experimental work-flow from material growth to the applied transport measurement techniques. First, we go through the basics of vapour-liquid solid growth of nanowires before we turn to in-situ superconductor deposition. Afterward, we give a basic overview of device fabrication, preparation of devices for fridge loading and the fundamental workings of its cooling processes. Finally, the measurement setup is presented.

Chapter 3 is a reprint of the article called *'Epitaxial Pb on InAs for quantum devices'* published in Nature Nanotechnology in 2021. Here the novel hybrid InAs/Pb nanowire is presented from an offset in material science. The superconducting Pb film is found to be epitaxially matched to the InAs nanowire core, in addition to being atomically flat and single crystalline. In tunnel probe devices we find a superconducting critical temperature of 7 K and a superconducting pairing energy of 1.25 meV which is not quenched in parallel magnetic fields up to 8.5 T. In addition, we present superconducting island devices where $2e$-dominated transport is transitioned to $1e$ similar to experiments conducted on InAs/Al hybrid islands.

Chapter 4 serves as an extension to the previous chapter. Here, follow-up experiments and according data serve as a backdrop surrounding the previous chapter showing additional transport phenomena. Tunnel devices fabricated on in-situ double-shadowed InAs/Pb/Au devices show a hard induced super-

conducting gap, complex Andreev bound state spectra and Yu-Shiba-Rusinov states. Island devices show signs of odd $2e$ ground state transitions and tunable ratios of charging energy versus pairing energy.

In the subsequent two chapters (p)reprints of other manuscripts related to this work are presented. There will be no clear narrative arch between these as they are only loosely connected by the overall topic of the thesis. Here they are listed:

- Chapter 5 is a reprint of the article called *'Scalable platform for nanocrystal-based quantum electronics'* published in Advanced Functional Materials in 2022. Here we use a microtome to cut thin sections of arrays of InAs nanowires embedded in a resin. We fabricate electronic devices on the off-cut InAs nanocrystals and find that we can produce electronic devices with good yield. Moreover, we show the ability of the single nanocrystal devices to hold quantized phenomena such as single electron charging, conductance quantization and wave interference. Finally, we outline how this platform can be extended to networks by growing vertically connected nanowires providing new means to fabricating high-throughput hybrid nanocrystals in alternative geometries. Further details related to this article are presented in the appendix (Chapter 8) as they might be of interest but are too lengthy to include in the main body of the thesis.

- Chapter 6 presents a preprint of the article called *'Shadowed and etched superconductor-semiconductor junctions in Al/InAs nanowires'* which is a manuscript in preparation. Here we compare the structural and electronic properties of Al-junctions on InAs nanowires formed by shadowing versus etching. From high-resolution electron microscopy we infer that typical etching procedures lead to atomic-scale surface roughening likely causing a reduction in electron mobility. Further, we discuss more advanced shadowing geometries that could aid in the efforts towards building hybrid devices entirely in-situ. In the end, we give examples of shadowed junctions measured at low-temperatures that show high-quality quantum transport phenomena, giving the future road of in-situ shadowing additional merit.

Finally, in Chapter 7 the thesis is rounded off with a tentative outlook and conclusion. The word *'tentative'* is used here intentionally as the field of hybrid quantum devices is vigorously expanding and branching and it is hence too speculative to conclude or predict anything for certain. However, what we can say, is that the future of hybrid nanostructures looks *very* interesting.

1.2 Semiconductor crystals

Certain materials are neither good conductors nor insulators, and they have therefore inherited the fitting name, *semiconductors*. Typically, they exhibit insulating properties at room temperature, and their resistivities (resistance in units of area divided by length) lie between that of a conductor and an insulator.[11] At first impression this property of being neither a good conductor nor insulator sounds discouraging. However, it provides a great starting point from which one can engineer and control the conductivity by adding suitable impurities to the semiconductor crystal. This flexibility in controlling the material property is arguably the main reason why semiconductor microchips have become the most produced man-made object of all time. Typical examples of semiconductors are silicon, germanium and carbon.

A particularly useful way to gain an understanding of solid state materials and their characteristic properties, such as electrical resistivity or optical absorption, is by *band theory*. By investigating the quantum mechanical wave function of electrons in solids (in this context, large repeating arrays of atoms), band theory can predict certain energy ranges of allowed or forbidden states that can be occupied. In Fig. 1.3 a sketch of the typical band structure of a metal, semiconductor and insulator is shown. The upper parabolae illus-

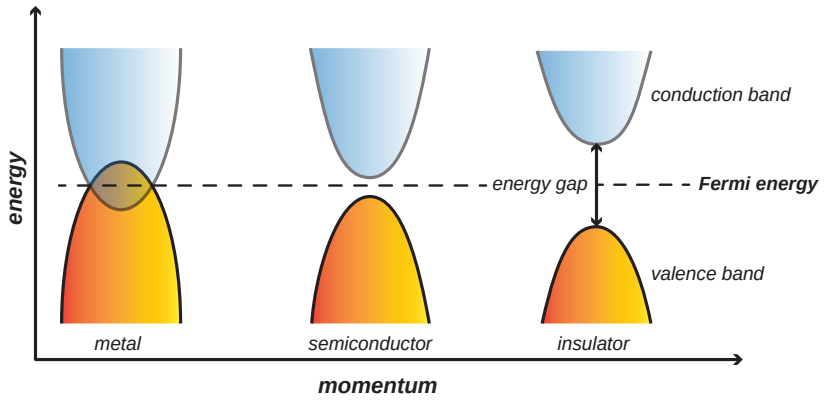

Figure 1.3: **Sketch of band gap for metals, semiconductors and insulators.**

trate the *conduction bands* which is the range of permitted energy states of which an electron can access and freely carry a charge in the material. On the contrary, the lower parabolae called the *valence bands*, represent the range of permitted energy states of which an electron can access and still be bound to the atom of a solid, i.e. not carry a charge freely in the material.[12] In between the two bands we find the Fermi energy, E_{F} which by convention is located energetically in the middle of the band gap at temperature, $T = 0$. The Fermi level, which is closely related to the Fermi energy, of a solid is directly related to the voltage on the solid, as measured with a voltmeter and is often referred to as the chemical potential. The Fermi level is in contrast to the Fermi energy defined for all temperatures and accounts for the total level of the kinetic and potential energy.[13]

Much of the work involved in measuring quantum transport in semiconductor nanostructures revolves around reducing the temperature of the sample as much as possible. The technicalities of this is discussed further in Chapter 2, but we ought to introduce the *Fermi function* already now since it is a fundamental concept. We write the Fermi function as,

$$f(\mathrm{E}) = \frac{1}{e^{(E-E_{\mathrm{F}})/k_{\mathrm{B}}T} + 1} \tag{1.1}$$

where $f(\mathrm{E})$ is the probability of a particle having the energy E, $k_{\mathrm{B}}T$ is the Boltzmann constant multiplied by the temperature, E_{F} is the Fermi energy and E is the energy of the particle. In Fig. 1.4 we plot the Fermi-Dirac distribution for Au ($E_{\mathrm{F}}^{\mathrm{Au}} = 5.53$ eV) for three different temperatures.

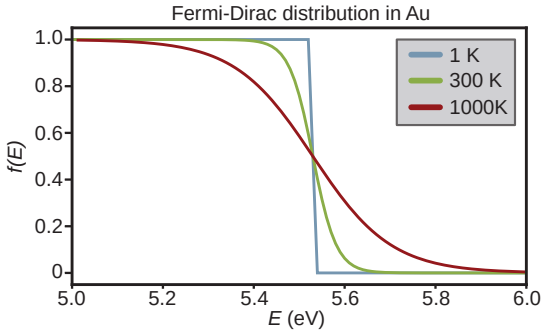

Figure 1.4: **Temperature dependent Fermi-Dirac distribution of Au.**

In the extreme when $T \to 0$ the function becomes a step-function and returns $f(\mathrm{E}) = 1$ for carriers with energies below the Fermi energy and $f(\mathrm{E}) = 0$ for carriers with energies above. As the system temperature is increased the abrupt transition smoothens and carriers above and below E_F are allowed in an increasingly wider distribution. The consequences of this behavior becomes apparent if one considers the energy scales of a desired experiment. If the carriers populate a spread in energy that is larger than the energy scale of interest, any measurable information will be lost due to the thermal broadening. Hence, one could think of cooling as increasing energetic resolution.

Conventional band theory operates under the assumption that the atomic ordering of the material is highly periodic, repeats for a large number of atoms and that the electronic states are not interacting with lattice vibrations, other electrons or light. This is great news for us as many semiconductors fulfil all these requirements, at least to a good first approximation.

Field effect in semiconductors

A crucial aspect of controlling electronic quantum devices is the field effect response in semiconductors. As the electron density in semiconductors is low compared to metals, we can modulate the electrical conductivity by exposing it to an external electric field. This we typically refer to as 'gating'.

In Fig. 1.5 we show how the conduction/valence bands of a semiconductor are bent towards the Fermi level of the metal gate in close proximity to the semiconductor due to an external field originating from the gate. We show the case of $V = 0$ in panel **a** and the case of $V > 0$ in panel **b**. As a positive bias voltage is applied to the metal its electric field penetrates into the surface of the semiconductor enabled by low screening of its charge carriers. This bends the bands downwards.[14] The opposite is true for negative bias voltages. Below the Fermi level electronic states are likely to be occupied turning the insulating semiconductor conducting. Thus by placing gates in close proximity we can manipulate carriers in the semiconductor locally.

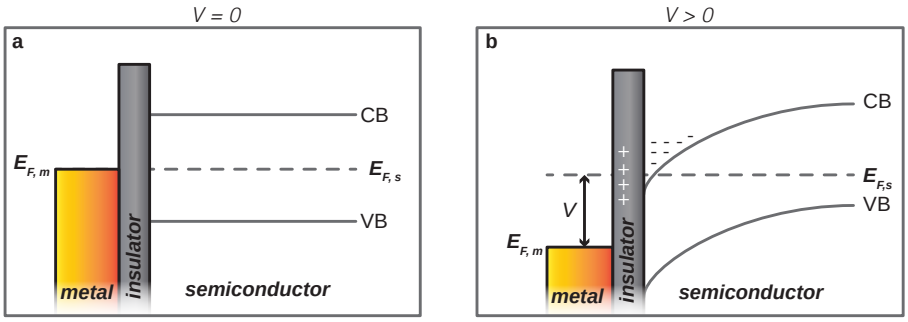

Figure 1.5: **Electrostatic field effect on semiconductors. a**, No applied voltage between the metal and the semiconductor. Only band bending of the conduction band (CB) and valence band (VB) arises from surface band bending. **b**, A positive voltage on the metal gate bends the conduction band below the Fermi level populating the conduction band with carriers.

In the subsequent part we will dial up the level of complexity and switch gears from carriers in semiconductors to coupled electrons in superconductors.

1.3 Introduction to superconductivity

When typing these lines 111 years have passed since H. Kamerlingh Onnes discovered the first hallmark of superconductivity, namely perfect conductivity. Since the year of 1911 physicists learned how to harness the properties of superconductors to aid society all the way from the health sector to public transport. Still many years and landmarks later, the topic hasn't seized to amaze researchers. This section is based on Refs.[15, 16, 17] and inspired by topically related dissertations.[18, 19]

1.4 Bardeen-Cooper-Schrieffer theory

After Kamerlingh Onnes findings' the scientific community had to wait until 1957 before a self-consistent microscopic theory explaining superconductivity was presented. This theory is called the *Bardeen-Cooper-Schrieffer theory* and this is where we take off.

Cooper presented in 1957 the idea that we could couple two electrons through weak attraction into a quasiparticle. This quasiparticle is now called a *Cooper pair* and consists of two electrons with opposite spin and momentum $(k, \uparrow)$ and $(-k, \downarrow)$ that are coupled via some attractive force. In Figure 1.6 the attraction is illustrated as phonon-mediated electron-electron coupling typical for s-wave superconductors.

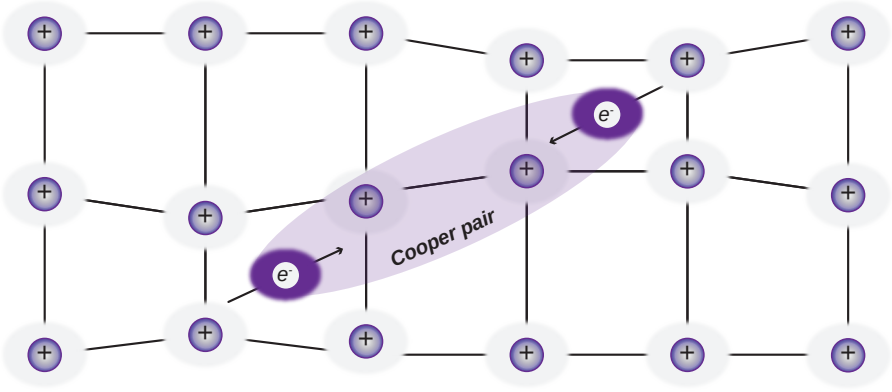

Figure 1.6: **Phonon-mediated Cooper pair.** Two electrons with opposite spin and momentum attractively coupled via crystal lattice deformations.

Here lattice distortions arise due to electrostatic interaction between the negatively charged electrons and the positively charged nuclei. Local volumes of net positively charged regions arise where the electrons just passed by which attracts other electrons thus coupling them into pairs. These vibrations are washed out due to thermal vibrations, and the temperature at which the pair bonding breaks down is known as the critical temperature, T_{C}.

The phonon-mediated electronic correlations of the whole system can be described by a mean field as $\Delta_{\mathrm{k}} = \langle c^{\dagger}_{k\uparrow} | c^{\dagger}_{-k\downarrow} \rangle$, where we denote the creation operator of the fermion as $c^{\dagger}$. By using a mean field description (a mathematical way of describing systems with very large dimensions), we describe all interactions to one particle as an effective or average interaction instead. We now apply this mean field to the free electrons by adding it to the Schrödinger Hamiltonian to obtain what is known as the Bogoluibov-de Gennes (BdG) equations

$$\begin{pmatrix} H_k & \Delta_k \\ \Delta_k & -H_k \end{pmatrix} \begin{pmatrix} u_k \\ v_k \end{pmatrix} = E \begin{pmatrix} u_k \\ v_k \end{pmatrix}. \tag{1.2}$$

Now we assume that the pairing amplitude (Δ_{k}) of the quasiparticles in the superconductor is evenly distributed ($\Delta_{\mathrm{k}} \rightarrow \Delta$). This evenly distributed pairing amplitude, Δ, is the superconducting energy gap, which defines the

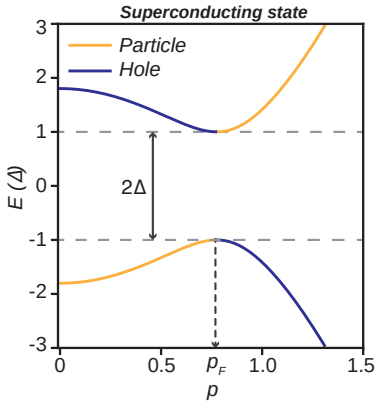

Figure 1.7: **Energy spectrum of single particle states.** Energy spectrum of the superconducting state plotted from Eq. 1.3.

energy it costs to break up a Cooper pair. From this we can now find the eigenvalue,

$$E = \pm\sqrt{\epsilon_k^2 + |\Delta|^2}, \quad \text{where} \quad \epsilon_k = \left(\frac{\hbar^2|k|^2}{2m^*} - \mu\right) \tag{1.3}$$

where μ is the chemical potential, $\hbar$ is the reduced Planck constant, m^* is the effective mass and k is the wave vector. The sign indicates either hole $(-)$ or particle excitation $(+)$. If the energy dispersion of the single particle energy relation is plotted (Fig. 1.7) we can see that a gap of size Δ appears. Here we see how particles and holes mix in the superconducting state, which was directly observed experimentally in 1996 by means of angle-resolved photoemission spectroscopy.[20]

Considering the probability of exciting a quasiparticle, u_0 and v_0, we note that they obey the condition for normalization, namely $u_0^2 + v_0^2 = 1$. When we combine the BdG equation (1.2) with the quasiparticle excitation energy (1.3) we obtain the probability of exciting a particle/hole as a function of the energy,

$$u_0^2 = \frac{1}{2}\left(1 + \frac{\sqrt{E^2 - |\Delta|^2}}{E}\right) \tag{1.4}$$

$$v_0^2 = 1 - u_0^2 \tag{1.5}$$

We can use the pairing energy (1.3) to find the density of states of the superconducting (DOS_S) from the density of the normal states ($DOS_\mathrm{N} = \frac{dN}{d\epsilon_k}$),

$$DOS_S = \frac{dN}{d\epsilon_k}\frac{d\epsilon_k}{dE} = DOS_N \frac{E}{\sqrt{E^2 - |\Delta|2}}. \tag{1.6}$$

We have now arrived at a good first-hand description of the superconducting density of states. We plot this in Fig.1.8 and see that a gap of 2Δ appears in the single particle density of states within $\pm\Delta$. However, in order to probe the density of states in a superconductor, we want to create an experiment where we can inject carriers into the superconductor while knowing their energy. In other words, we want to create a normal metal-superconductor tunnel junction, and these are best understood from the point of view of *Andreev reflection*.

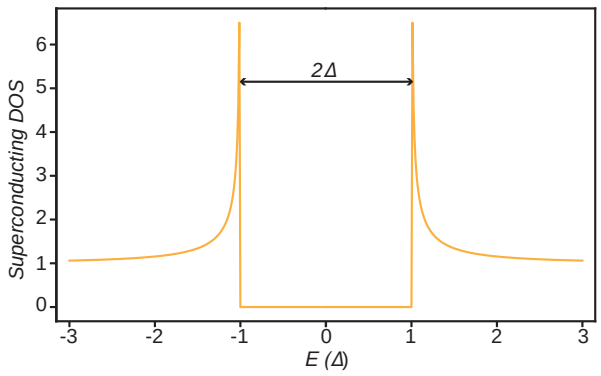

Figure 1.8: **BCS density of states.** The superconducting density of states plotted versus electron energy. Plot is generated from Eq. 1.6.

1.5 Spectroscopy across normal metal-superconductor junctions

In this section we will investigate what happens when a normal metal is brought in close proximity to a superconductor. We will start with a description where the carriers tunneling into the superconductor experience no barrier and later add a barrier to the formalism to usher closer to experiments.

Andreev reflection

If an electron with $E > \Delta$ impinges on to the superconductor the single particle continuum above $|\Delta|$ will accept the carrier and nothing more interesting happens. On the other hand, if the impinging particle carries $E < \Delta$ there are no available states in the superconductor and it will undergo a scattering event losing its momentum and reversing its wave vector. We call this *normal reflection*.

From before, however, we know that superconductors hold Cooper pairs. So if we imagine the normal metal donating not one, but two electrons with opposite spin and momentum, the electrons can continue into the superconductor. However, this would violate momentum conservation. Instead the first electron (with $-k$) is thought to retro-reflect as a hole (with $+k$) instead. We will refer to this as *Andreev reflection* from now on. This process is por-

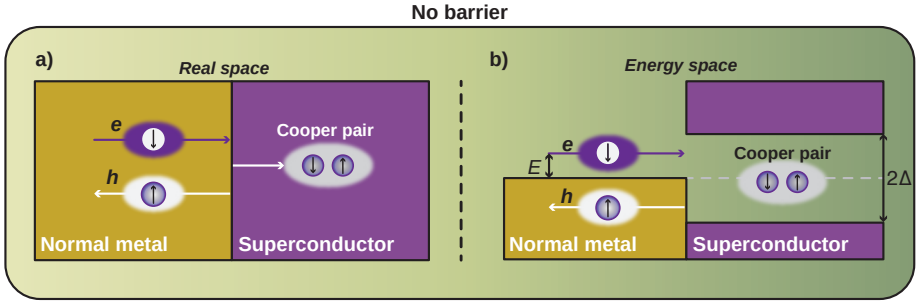

Figure 1.9: **Andreev reflection process without barrier.** Real space (**a**) and energy space (**b**) sketch of the Andreev reflection mechanism without a barrier.

trayed in Fig. 1.9. In addition, the hole will return along the same path as the original electron since the group velocities of electrons and hole are opposites.

1.6 The BTK formalism

In order to add a barrier (Z) to the Andreev reflection picture we turn to the *Blonder-Tinkham-Klapwijk* (BTK) formalism. The BTK formalism accounts for three additions to the simpler picture from before. Going from left to right in Fig. 1.10 **a**:

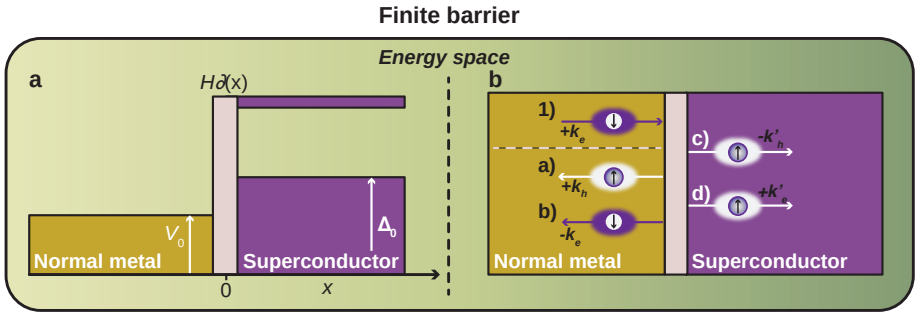

Figure 1.10: **Andreev/normal reflection process with barrier. b**, Energy space sketch of the same process with a barrier.

- **Left**, we add a potential barrier to the junction to account for Fermi

velocity mismatch between the two materials. This we write as: $V(x) = V_0\ \Theta(-x)$, where V_0 is the potential and Θ denotes the step function.

- **Middle**, we add a δ-function between the normal metal and the superconductor to represent a barrier. This we write as: $H\delta(x) = \hbar v_F Z\delta(x = 0)$, where v_F denotes the Fermi velocity.

- **Right**, we assume that the pairing potential, Δ, increases abruptly $\Delta(x) = \Delta e^{-i\theta}\Theta(x)$, with $\Theta(x)$ denoting a step function.

We can now change the BdG equation accordingly, and rewrite its scalar potential to

$$U_{BdG}(x) = \hbar v_F Z\delta(x = 0) + V_0\Theta(-x). \tag{1.7}$$

Assuming the plane-wave ansatz we look for solutions of the incoming electron in shape of $\Psi_\mathrm{incoming} = \begin{pmatrix}1\\0\end{pmatrix} e^{ik_e x}$. An incoming electron now has 4 options also illustrated in Fig. 1.10 **b**. It can either reflect back as an electron, retroreflect as a hole (Andreev reflect),

$$\Psi_\mathrm{reflect} = \underbrace{a\begin{pmatrix}1\\0\end{pmatrix} e^{ik_h x}}_{\text{reflect electron}} + \underbrace{b\begin{pmatrix}0\\1\end{pmatrix} e^{-ik_e x}}_{\text{Andreev reflect}} \tag{1.8}$$

or transmit an electron or a hole,

$$\Psi_\mathrm{transmit} = \underbrace{a\begin{pmatrix}1\\0\end{pmatrix} e^{ik'_e x}}_{\text{transmit electron}} + \underbrace{b\begin{pmatrix}0\\1\end{pmatrix} e^{-ik'_h x}}_{\text{transmit hole}}. \tag{1.9}$$

Now we can find the wave numbers from finding the eigenenergies of the BdG equation as,

$$k_e = \sqrt{k_{FN}^2 + (2m^*/\hbar^2)E}, \tag{1.10}$$

$$k_h = \sqrt{k_{FN}^2 - (2m^*/\hbar^2)E}, \tag{1.11}$$

$$\tilde{k_e} = \sqrt{k_{FS}^2 + (2m^*/\hbar^2)\sqrt{E^2 - \Delta_0^2}}, \tag{1.12}$$

$$\tilde{k_h} = \sqrt{k_{FS}^2 - (2m^*/\hbar^2)\sqrt{E^2 - \Delta_0^2}}. \tag{1.13}$$

	$A(E)$	$B(E)$
$Z = 0$		
$E < \Delta$	1	0
$E > \Delta$	$\frac{v_0^2}{u_0^2}$	0
$Z > 0$		
$E < \Delta$	$\frac{\Delta^2}{E^2 + (\Delta^2 - E^2)(1 + 2Z^2)^2}$	$1 - A(E)$
$E > \Delta$	$\frac{u_o^2 v_0^2}{\gamma^2}$	$\frac{(u_o^2 - v_0^2)^2 Z^2 (1 + Z^2)}{\gamma^2}$

Table 1.11: **Table of transmission and reflection coefficients.** $A(E)$ denotes the Andreev reflection probability, and $B(E)$ denotes the ordinary reflection. In addition, and along the lines found in Ref. [15] we write $\gamma = u_0^2 + (u_0^2 - v_0^2)\ Z^2$.

The Fermi wave number of the semiconductor is represented in k_{FN} and as k_{FS} for the superconductor. Solving the Schrödinger equation with the step function potential (Eq. 1.7) at the boundary condition of $x = 0$ yields the probability amplitude for the normal, $A(E)$, and Andreev reflection processes $B(E)$. The appropriate findings are listed in Table 1.11 obtained from Ref. [15]. Note that the barrier has been modified to yield Z with dimensionless units as $Z = H\frac{m_e}{\hbar k_{Fs}}$.

Based on the table values we plot the reflection probabilities for a number of different effective barrier strength in Fig. 1.12. For perfect interfaces ($Z = 0$) we observe perfect Andreev reflection probability. This means that all electrons impinging on the interface with $E < \Delta$ are retroflected as holes and that a Cooper pair is added to the superconductor. At no point do we observe normal reflections as electronic transmission takes over for electrons with $E > \Delta$ (not shown in the plot). For increasing barrier strengths ($Z > 0$) we observe that the probability for retroreflection decreases and is represented in growing chance to reflect normally. An exception to this trend is observed at $E = \Delta$, where we due to the δ-peak nature of the BCS coherence peaks

always see perfect Andreev reflection - at least in this model.

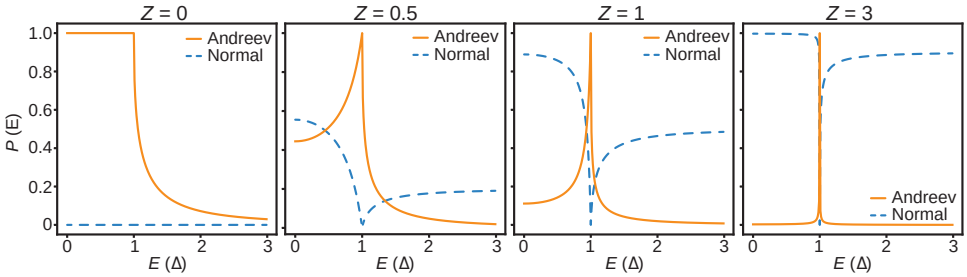

Figure 1.12: **Andreev/normal reflection process with and without barrier.** **a**, Reflection coefficients, P(E), plotted versus the energy of the incoming electrons for a selection barrier strengths (Z) for Andreev reflection (solid line) and normal reflection (dashed line). Plots generated using table 1.11.

Current across a metal-superconductor tunnel junction

To move from probabilistic theoretical physics to experiments we need to bridge between reflection amplitudes and some measurable quantity. The quantity we chose to measure is current, I, against a voltage, V, applied across the metal-superconductor junction. To do this we start by considering electronic transport running from one reservoir through a constriction to another reservoir. Both reservoirs are described by equilibrium Fermi functions offset by an energy shift arising from an accelerating potential. We write this as,

$$I = 2\,N(0)\,e\,\nu_F \cdot \mathcal{A} \int_{-\infty}^{\infty} \Big[f(\mathrm{E})_{\rightarrow} - f(\mathrm{E})_{\leftarrow} \Big] dE \tag{1.14}$$

where $\mathcal{A}$ is the effective area of the constriction and $N(0)$ corresponds to one-spin density of states at the Fermi energy and e is the elementary charge. We now assume that the carriers travelling from the superconductor to the normal reservoir retain the ordinary Fermi function ($f(\mathrm{E})_{\rightarrow} = f_0(E - eV)$), whereas carriers travelling from the normal side into the superconductor obey the probabilistic picture described above. This we write as,

$$f(\mathrm{E})_{\leftarrow} = A(E)[1 - f_{\rightarrow}(-E)] + B(E) f_{\rightarrow}(E) + [C(E) + D(E)] f_0(E) \tag{1.15}$$

where $C(E)$ and $D(E)$ are the transmission amplitudes that we brushed over earlier. Now we put these right and left moving carriers into Eq. 1.14 and reshuffle it assuming that $A + B + C + D = 1$, that $A(E) = A(-E)$ and that $f_0(-E) = 1 - f_0(E)$ and obtain the current crossing the normal metal junction as,

$$I_{\mathrm{NS}} = 2\,N(0)\,e\,\nu_F \cdot \mathcal{A} \int_{-\infty}^{\infty} \Big[f(\mathrm{E}) - f(\mathrm{E} - eV) \Big] \Big(1 + A(\mathrm{E}) - B(\mathrm{E}) \Big)\, dE. \tag{1.16}$$

From this model we can see that Andreev reflection, $A(E)$ will increase the current across the junction while normal reflection $B(E)$ reduces it.

Now if we numerically integrate Eq. 1.16 we can plot the current across the normal-superconductor junction as a function of voltage at $T = 0$. We plot the current for different effective barrier strengths in Fig. 1.13 **a**. Note

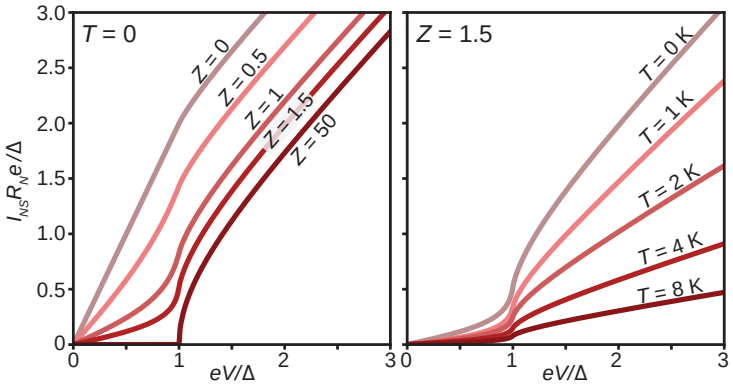

Figure 1.13: **Calculated current across an NS-junction.** **a**, Current versus incoming electron energy plotted at fixed temperature (T = 0) for a selection of barrier strengths. **b**, Current versus incoming electron energy plotted versus temperature for $Z = 1.5$. Plots generated using Eq. 1.16 and 1.17.

that as we are normalizing the current by the normal state current ($A(E) = 0$) and using that $1 - B = (1 + Z^2)^{-1}$ so Eq. 1.16 turns into

$$I_{\mathrm{NN}} = \frac{2\,N(0)\,e\,\nu_F \cdot \mathcal{A}}{1 + Z^2} \cdot V \equiv \frac{V}{R_{\mathrm{N}}} \tag{1.17}$$

where R_{N} is defined as the normal state resistance when $Z = 0$. Inspecting the graph we notice that the current is heavily influenced by the barrier strength and for $Z > 10$ the model is nearly identical to the classical tunnel junction models.

In Fig. 1.13 **b** we plot the current across the junction for a fixed effective barrier strength ($Z = 1.5$) and vary the temperature. Here we observe that the current is reduced as temperature is increased, which is explained by the Fermi functions shifting the reflection and transmission probabilities.

The strong influence of the barrier strength is even more vivid if we plot differential conductance, dI/dV, as a function of the incoming electron energy and Z as seen in Fig. 1.14. In panel **a** we choose to display Z in $\log_{10}$-scale to highlight the transition around $Z \sim 1$. Line cuts obtained at different Z-values are plotted at values indicated by the five symbols (**b-f**). As we approach $Z = 0$, we observe an increasing in-gap enhancement of the differential conductance

saturating at twice the conductance quantum of $2e^2/h$. This is known as perfect Andreev enhancement.

For increasing Z-values we observe rapidly decreasing differential conductance within the superconducting gap and a quickly growing coherence peak at $eV = \Delta$. In Fig. 1.14 **g** we plot the differential conductance versus incoming electron energy at fixed barrier height ($Z = 1.5$) and modulate the temperature. Similarly to before, we observe differential conductance above and below the gap diminishing as well as a rapidly decreasing coherence peak.

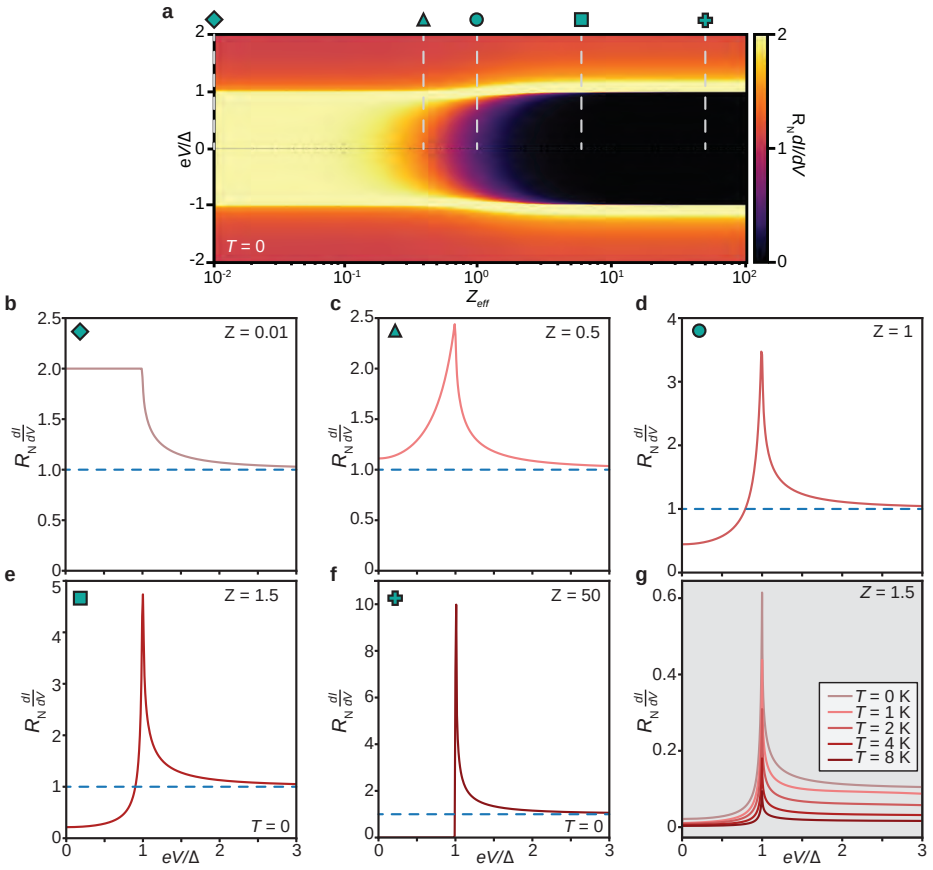

Figure 1.14: **Calculated differential conductance across an NS-junction.** **a**, Differential conductance versus incoming electron energy and barrier strength. Line cuts are shown in **b-f** for select barrier strengths (Z = 0.01, 0.5, 1, 1.5 and 50). **g**, Differential conductance versus incoming electron energy plotted for varying temperature and fixed barrier (Z = 1.5). Plots generated using Eq. 1.16 and 1.17.

1.7 Andreev bound states

A particular sort of bound states can arise at the interface of a superconductor called Andreev bound states (ABS). In the case already discussed, an impinging electron has only one interface to reflect from or transmit across. However, if two barriers are present, we obtain a certain probability of the reflection process to repeat itself off of the second barrier. We have now arrived at a situation where multiple boundaries at the superconducting interface can trap quasiparticle states. And, in analogy to the particle-in-a-box example from introductory quantum mechanics - this leads to energy quantization of the trapped states. If we now mirror our NS junctions from before over the normal side, we arrive at superconductor-normal-superconductor (SNS) junction, as seen in Fig. 1.15 **a**.

We now want to find the conditions needed for quantization. We do this by computing the energy of the bound states within $|E| < \Delta$ for transparent

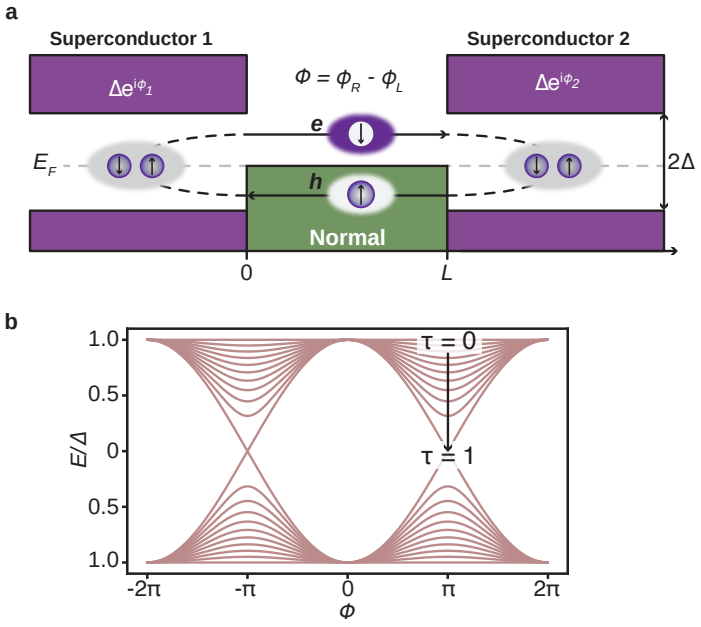

Figure 1.15: **Quantization of states trapped between two superconductors. a**, **b**. Bound state energy (E) plotted versus relative phase between the two superconductors for varying normal transmission, τ. Plot is generated from Eq. 1.19.

interfaces, assuming that the pairing energy is much lower than the chemical potential ($\Delta \ll \mu$). This yields,[6]

$$2\pi n = \phi - 2\arccos\Big[E(\phi)/\Delta\Big] - 2\frac{E(\phi)}{\Delta}\frac{L_N}{\zeta}. \tag{1.18}$$

where, n is an integer number, L_N is the junction length, and ζ is the superconducting coherence length (how long the Cooper pairs remain coherent inside the normal junction) and, ϕ, is the phase difference. If we now consider 3 things: (i) there are multiple modes present in the junction, (ii) the transparency is not perfect and (iii) the superconducting coherence length is greater than the junction length, we can find explicit energies of the individual modes. These come in the form of,

$$E^{ABS} = \pm\Delta\sqrt{1 - sin^2\left(\frac{\phi}{2}\right)\tau^i}. \tag{1.19}$$

Here τ^i is the normal transmission for each individual mode inside the normal junction. We plot the energies of the modes versus phase difference in Fig. 1.15 **b**. From the plot we see that bound states arising between perfectly in-phase superconductors exhibit unity energy no matter the transmission coefficient. As we bring the superconductors out of phase and increase transmission the bound states energy will continuously decrease. At perfect transmission and completely out-of-phase superconductors the ABS energy is nul.

In the following we switch gears from tunnel junctions to single electron charging of metallic islands.

1.8 Coulomb spectroscopy on superconducting islands

In this section we switch our focus from Andreev reflections across single tunnel junctions to Andreev reflection across isolated superconducting islands. To ease into this topic, we start with a short introduction on single electron transistors before extending the model to account for Cooper pair transport. The first part has a foothold in the review by *Kastner, M. A.*[21], whereas the extension accounting for superconductivity is based on the paper by *Tuominen* et al. and *Higginbotham* et al.[22, 23]

Single electron transistor

Charging effects in isolated metallic islands was first discussed by C.J. Gorter who sought to find *"A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strengths"*, which is also the title of the article explaining his work.[24] He was the first to formulate a possible connection between the increase of a thin film resistance at low temperatures to the energy cost of bringing charged particles close to each other - in other words - overcoming the Coulomb energy. His work, however, was based on considerations of large ensembles of metallic grains and described more or less the physics related to overcoming the Coulomb energy in an averaged way, at best. We, on the other hand, are more interested in finding the specific energy associated with adding a single electron to a metallic island weakly coupled to two leads. Conveniently this can be understood (initially) in a purely classical way.

The schematic in Fig. 1.16 **a** shows a metallic island coupled via two tunneling resistances (R_S, R_D) to the source (S) and drain (D) contacts. Typically for single-electron transistors the current/voltage relation is non-linear due to the large charging energy, E_C, of the island. In quite the same way as storing energy on a capacitor it involves work to transport charge from one capacitor plate to the other while overcoming the electrical forces. When charge is built up in the charging process each following element, dq, requires more work to make it onto the other capacitor plate. If we sum over all these

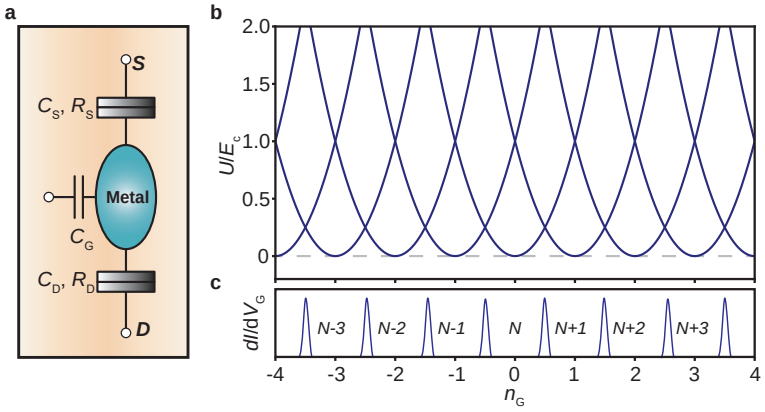

Figure 1.16: **Single electron transistor.** **a**, Schematic of the single electron transistor. **b**, Charging energies plotted versus gate-voltage for a series of charges. Plot is generated from Eq. 1.20. **c**, Illustration of differential conductance as a function of effective island charge showing conductance resonances whenever $U^N \leftrightarrow U^{N\pm1}$.

individual charging events, we find $E_C = \int_0^Q \frac{q}{C}\, dq = \frac{Q^2}{2C}$. Now we replace Q for the electron charge e and assume that charging events come in integer numbers, n, and we can write the charging energy as $E_C = n\frac{e^2}{2C_\Sigma}$ where C_Σ is the capacitance to the source (C_S), drain (C_D) and gate electrode (C_G) summed. Given the right circumstances we can observe e-periodic charging events induced by the gate electrode. If we call this the potential difference of the isolated metal slab and gate electrode, then the electrostatic energy of the island can be written as, $U = -QV_G + \frac{Q^2}{2C}$. Here the attractive interaction between the gate and the metal slab is accounted for in the first term, whereas the second term accounts for Coulomb repulsion. This relation can modified into

$$U = \frac{(Q - Q_0)^2}{2C} \tag{1.20}$$

using that $Q_0 = C_G V_G$, which is the charge minimizing the energy of the island by modulating V_G. As the charge on the island is modulated in integer units of the electron charge, $Q_0 = Ne$, the addition energy on the island changes in units of $\frac{e^2}{C}$.[25]

In Fig. 1.16 **b** we plot the island energy versus effective island charge (Eq. 1.20) where we write the effective charge on the island as $n_G = C_G V_G$. Here

we observe that at half-integer values of charge ($Q_0 = (N + 1/2)e$) the states holding Ne and $(N + 1)e$ are degenerate allowing for charge to traverse the island. Said in other words, we observe transport when the parabolas cross which entails two charge states being degenerate in order to minimize the island energy. In Fig. 1.16 **c** we sketch these transport features (Coulomb resonances) in differential current versus effective charge number at half-integer units of n_G.

Experimentally, a set of requirements needs to be fulfilled in order to measure this effect. They are:

- The thermal energy of the system must be smaller than the charging energy ($k_{\mathrm{B}}T \ll E_{\mathrm{C}}$), or electrons may traverse across the island via thermal excitations.

- The tunneling resistances, need to be larger than $\frac{h}{e^2}$. This entails that the tunneling time is negligible compared to the other time-scales. Typical tunneling resistances larger than $\sim$ 25 kΩ suffice to isolate single charges on the island, and exclude other effects like co-tunneling.

- The chemical potential applied to the island must be lower than the charging energy.

In the following we shall extend this description to account for superconductivity.

Superconducting islands

Now we swap the normal metal out for a chunk of superconductor, as illustrated in Fig. 1.17 **a**. At sufficiently low temperatures and low voltages quasiparticle tunneling events occur only rarely and electrons now come in pairs of two (Cooper pairs) bound by the pairing energy, Δ, as described in section 1.4. This lifts the energy of the odd states by Δ, at least in a first hand description and we can extend Eq. 1.20 to,

$$U = \frac{(Q - Q_0)^2}{2C} + \Delta p_{\mathrm{N}}, \tag{1.21}$$

where $p_{\mathrm{N}} = 1$ for even n and $p_{\mathrm{N}} = 0$ for odd N.

In Fig. 1.17 **b** we plot this parity relation assuming $\Delta > E_{\mathrm{C}}$. In this case for transport to occur the charge states $N \leftrightarrow \pm 2N$ need to be degenerate as illustrated in Fig. 1.17 **b** and **c**.

A model accounting more accurately for the behavior of superconducting islands at elevated temperatures is already developed.[22, 23] Here excitations for superconducting particles above the ground state is accounted for in even and odd states. As temperature is increased the energy difference between both excitations diminishes due to entropy contributions and the

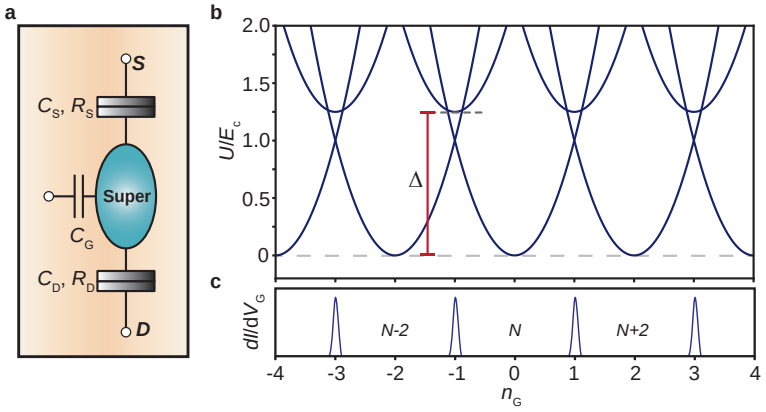

Figure 1.17: **Superconducting island.** **a**, Schematic of the superconducting island. **b**, Charging energies plotted versus effective island charge where odd-numbered parabolas are lifted by Δ. Plot is generated from Eq. 1.21. **c**, Sketch of differential conductance as a function of effective island charge showing conductance resonances whenever $U^{n_{even}} \leftrightarrow U^{\pm 2n_{even}}$.

single-electron transistor model from before is obtained. As we only operate the island devices of this work at very low temperatures we are not going further into this.

This concludes the theoretical section of the thesis, which sought to provide a brief introduction to some of the topics covered in the manuscripts presented later. In the following section we will shift gears and describe some of the fundamental tools that provide the foundation for all of the above experiments, namely, the materials, the devices and the measurement setup.

CHAPTER 2

MATERIALS & MEASUREMENT SETUP

This chapter revolves around most of the first-hand work that is required to measure quantum phenomena in nanowire devices at low-temperatures. As most specific details are covered in the articles related to this work or can be found in their methods sections, we aim to keep this chapter brief and only related to topics not detailed in these publications.

First, we go through the basics of how to grow InAs nanowires, before we describe what it takes to (selectively) coat these with a superconducting shell. Finally, the basics of the measurement setup are discussed. All nanowires and related shadow techniques used during this work were grown and developed by Thomas Kanne.

2.1 Growth of nanowires

The variety of available tools for producing nano-structured materials today is truly extensive. Just to name a few, while ignoring the vast field of etched and self-assembled nano-materials, there are chemical vapor deposition, pulsed laser deposition, magnetron sputtering, flame transport synthesis and physical vapor deposition. The techniques used most widely for growth of elongated InAs crystals are metal-organic-vapor-phase-epitaxy[26] and molecular beam epitaxy (MBE).[27] In the following we shall focus only on the latter as this has been the technique applied to produce the InAs nanowires used for this work. To be specific, this section we will focus on vapour-liquid-solid (VLS) growth within an MBE system.

In 1964 the VLS mechanism was proposed as the rudimentary explanation of how Si nanowires could grow from liquid metal droplets planted on a Si substrate under a gaseous phase of Si.[28] In Fig. 2.1 we show the basic principles of VLS growth. A small metal particle (in our case Au) is positioned on a substrate (**a**). Positioning of these droplets can be achieved by a number

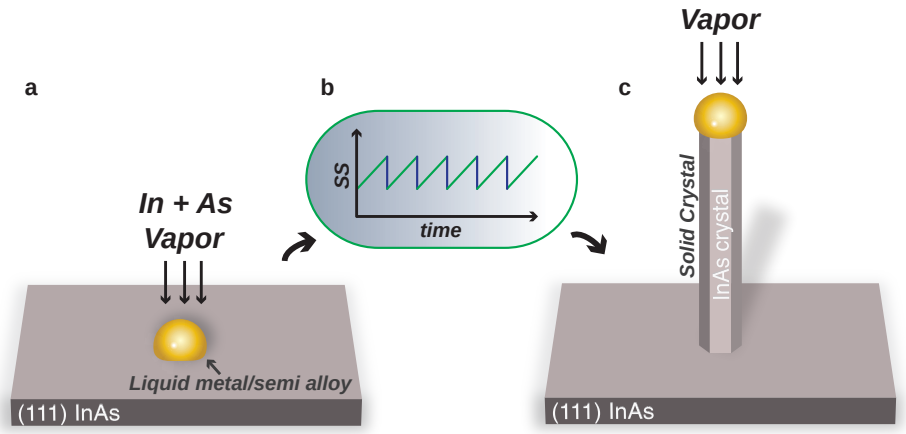

Figure 2.1: **VLS growth of InAs nanowires.** **a**, Liquid Au droplet positioned on InAs (111) epi-ready substrate. **b**, Supersaturation (SS) versus growth time. **c**, InAs nanowire with liquid droplet at the tip growing out from the InAs substrate.

of ways with each their own advantage. For instance, a metal film can be deposited in-situ and heated in order for the film to liquify into nano-scaled particles. The particle volume distribution and position are hard to control but the process introduces very few contaminants, as the growth substrate has not been exposed to any processing prior to growth. Another popular way of placing metal particles is to expose the growth substrate to a metal colloid suspension ex-situ. The advantage of this technique are processing costs, at the expense of control of particle position and volume. In our case, we process the growth substrate with standard electron beam lithography (EBL) procedures prior to growth. This provides a number of advantages over the other two techniques, namely, high control over position and volume of the nano-particles which, to some degree, comes at the expense of cleanliness.

Typically the nano-particles are placed on (111)B substrates as this orientation is the preferred low energy orientation for nanowire nucleation.[29] The substrates are loaded into the MBE chamber, before they are heated liquefying the metal particles. The system holds a series of effusions cells which are highly controllable and efficient deposition sources which are used to introduce a flow of precursor material. The liquid particle collects material from

the newly introduced vapor to the point of complete saturation. If a steady income of material is present a repeating process is initiated where the particles are supersaturated and a 2-dimensional layer is formed to rid the droplet of the excess material. This process is sketched in Fig. 2.1 **b**, where a saw-tooth like pattern shows the repeating process of liquid particle supersaturation resulting in 2-dimensional mono layer growth. Over a given time period a large number of layers between the substrate/metal particle are formed resulting in vertical nanowire growth as seen in Fig. 2.1 **c**. The nanowires used in this work are wurtzite InAs nanowires grown along the [0001]B direction with $\{1\bar{1}00\}$ facets on InAs (111)B substrates, with typical lengths ranging from 3 to 10 µm. Details of solidification, collection areas contributions, defect formation et cetera will be omitted as this falls outside the scope of this work. All these details can be found in the recent thesis by Thomas Kanne.[30]

2.2 Superconductor deposition

After nanowire growth is terminated, the growth substrate holding the arrays of InAs nanowires, is moved from the growth chamber to a separate deposition chamber of the growth system without breaking vacuum. The stage is cooled ($T_{\text{sub}} \sim 120$ K) by circulation of liquid nitrogen, before electron beam evaporation is used to deposit a metal thin film on the nanowires. In the following we use Pb as an example.

This process is sketched in Fig. 2.2 **a** where a Pb thin film is deposited on two facets of a hexagonal InAs nanowire. As the evaporated atoms, or clusters of atoms meet the surface of the nanowires they will after a certain diffusion length become trapped by a surface potential.[32] We will call these atoms now residing on the surface of the crystal for adatoms, where they can be thought of as opposites of surface vacancies. These adatoms may diffuse and interact resulting in formation of small nucleation clusters, which is a reversible process up to a given cluster size. Typically the thermodynamic energy of the formation of these clusters (which determines the cluster size) relies on the balancing of the binding energy between the adatoms and the surface energy of the cluster.[33, 34] As the substrate temperature is continuously reduced the thermal energy of the system is lowered resulting in critical cluster size

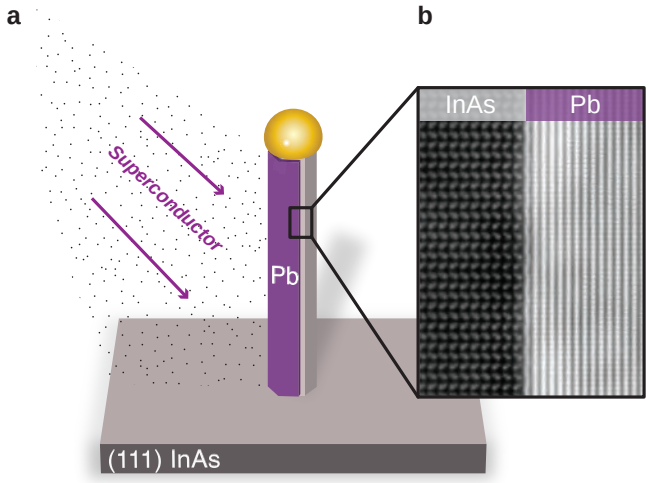

Figure 2.2: **Superconductor deposition on InAs nanowires. a**, Electron beam evaporation of a superconductor material at an angle with respect to the growth substrate normal. A Pb thin film is sketched as an example. **b**, High-angle annular dark-field scanning TEM image of an InAs/Pb interface along the axial direction, showing a near-perfect epitaxial match between the InAs nanowire and Pb film. TEM image is reproduced from the featured Ref.[31].

reduction. Or put in other words, if the substrate is sufficiently cold one may form clusters containing as little as just a few atoms. Under a constant in-flux of atoms, the isolated clusters grow in lateral size to a certain point where they merge if their crystal orientation is identical. If the clusters are of differing crystal orientation two different scenarios can come into play. In the first case, they recrystallize and merge obtaining either of the two cluster orientations. In the second case, the two clusters meet and are kinetically locked forming a common grain boundary. By measuring the in-coming beam flux with a piezo-crystal monitor the desired thickness of the thin film deposition can be estimated. Figure 2.2 **b** shows a high-angle annular dark-field scanning TEM image of an epitaxial Pb film grown on an InAs nanowire. The other superconductor shell structure investigated in this thesis is Al, and is deposited under similar conditions.

2.3 Selective superconductor deposition

Recent works have investigated how to remove the post-growth etching procedure by 'masking' part of the subsequently deposited superconductor in-situ either by the as-grown structures[35, 36, 37, 31] or by growing the nanostructures on a substrate with pre-defined masks [38, 39]. These studies have produced promising outlooks for devices based on in-situ shadowed hybrid structures especially in terms of device stability. Hence, there are good arguments for moving increasingly towards in-situ selective superconductor deposition. Here we show an example of in-situ masking technique which could aid further in moving ex-situ fabrication steps in-situ. Figure 2.3 **a** is a sketch of a two-step evaporation process which allows for depositing two materials on the same nanowire while varying their geometries. This case is exemplified using Pb and Au on InAs nanowires.

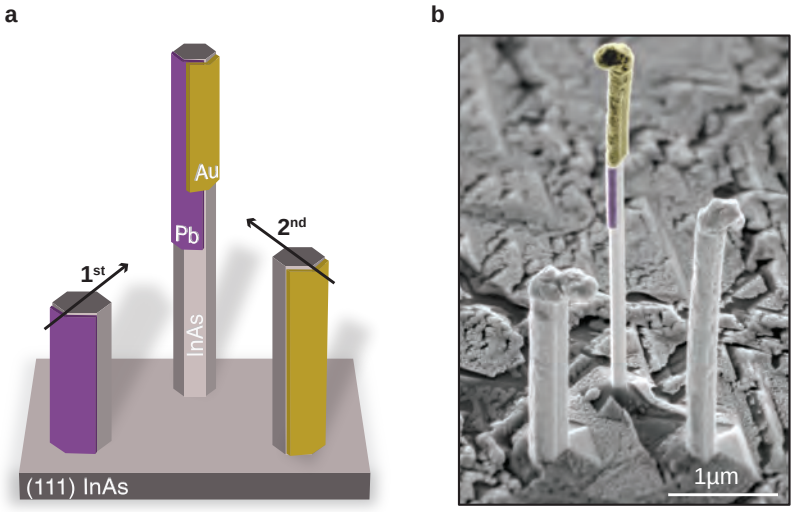

Figure 2.3: **In-situ selective masking of multiple thin films.** **a**, Schematic of the evaporation principles. Three nanowires of varying height and width are positioned as illustrated. Two evaporations are carried out at two differing angles resulting in selectively masked thin films of varying morphology. Yellow, Au; purple, Pb; grey, InAs. **b**, False-colour SEM image of a two-step evaporated nanowire. Nanowires were grown by T. Kanne and SEM image was recorded by Rasmus D. Schlosser.

Three catalyst particles are placed precisely via electron beam lithography in a triangular pattern (panel **a**). Controlling the volume of the particles, the diameter/height of the resulting nanowires are tuned such that two thick, short wires (still of different height) are placed in close proximity around a tall, narrow nanowire. The shorter wires will then act as local masks for thin film deposition under evaporation at an angle. By tuning these angles and the nanowire height to the present evaporation system one can manufacture hybrid nanowires with multiple thin film depositions of differing lengths. In Fig. 2.3 **b** we show an example of this technique after growth. Tunnel probe measurements on such hybrid InAs/Pb/Au nanowires are presented in Chapter 4 and similar shadow techniques are detailed in Chapter 6.

2.4 Accessing the nanowires electrically

After the hybrid nanowires are grown they need to be accessed electrically. The nanowires are first moved to a Si/SiO_2 substrate by a micro manipulator needle with a tip diameter of $\sim$ 100 nm. These substrates are based on highly doped Si wafers which are covered by a thermally grown oxide with thicknesses on the order of 200-500 nm. They contain pre-designed Ti/Au patterns used for recognition marks which have been fabricated by standard electron beam lithography techniques. Additionally, they contain 'bonding pads' which are extending Au electrodes that serve to translate between the sub-micron sized device contacts and the wire bonder thread which is on order of tens of microns. The bonding process is described in the next section.

Using the alignment marks the nanowires are located and imaged using an

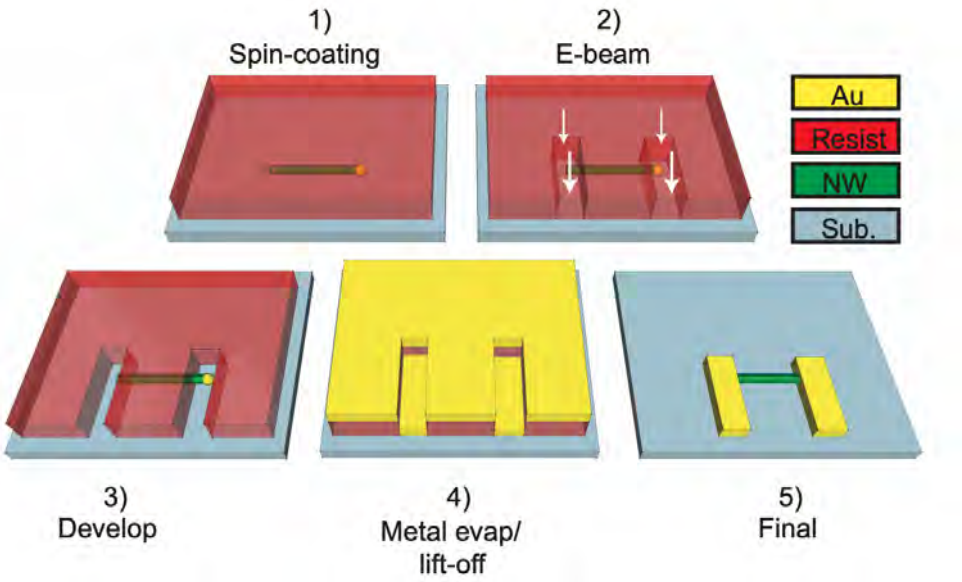

Figure 2.4: **Electron beam lithography process flow.** 1) A resist in spun onto the substrate after nanowire deposition. 2) Desired regions of the polymer are exposed to an electron beam. 3) The exposed regions are removed by a developer solution. 4) A metal (e.g. Au) is deposited on the entire sample using e-beam evaporation. 5) Using a solvent all remaining resist is removed, leaving only the metal at the designed locations. The figure is adapted from my Master's thesis.[40]

SEM with a laser-controlled stage for high-precision. After the images have been loaded into a computer aided design (CAD) software the desired device design is drawn. Employing an electron beam lithography tool the design (e.g. the contacts) is exposed in a pre-spun polymer. Following, the exposed polymer regions are flushed away by holding the sample in a developer solution before the sample is mounted in a electron beam evaporation chamber. Inside this chamber the native oxide of the semiconductor is removed by milling the surface of the sample with ionized argon atoms who are accelerated in a RF field for a few minutes. In the following step the desired metal films (eg. Ti, Au, Al or others) are evaporated onto the sample. We typically use Ti/Au for normal metal leads and Ti/Al for superconducting leads. The metal residing on the polymer is lifted off by exposing the sample to a solvent for a given time leaving only the designed patterns. The entire process flow is sketched in Fig. 2.4.

The entirety of the fabrication process can in some cases be very extensive, however, in this work only limited time was spent on optimizing fabrication recipes as the standard fabrication protocols worked sufficiently well for the desired device designs. The generic recipe used for fabricating contacts and side gates on nearly all devices is presented in Table 2.1.

Step No.	Task
1	*Spin one layer of PMMA A6 at 4000 RPM for 45 sec.*
2	*For InAs/Al devices: Bake the sample at 185 C for 2 min.* *For InAs/Pb devices: Pump on the sample for 1 hour.*
3	*E-beam exposure.* *Dose: 1200 $\mu C/cm^2$* *Write field size: 600 μm x 600 μm* *No. of pixels: 240.000* *Resulting resolution: 2.5 nm*
4	*Develop in MIBK/IPA for 60 sec.* *Rinse in IPA for 30 sec.*
5	*8 min RF mill at 18 mTorr and 15 Watts.*
6	*Deposit 5 nm Ti and 200 nm Au.* *If the sample contains Pb use a slow rate of* < 1.5 *Å/s.*
7	*Lift off in warm NMP at 50 C for 15 min.* *Rinse with IPA and blow dry with N2.*

Table 2.1: **Standard device fabrication recipe for leads and side gates.** The abbreviations of the utilized chemicals are as follows: NMP, N-Methyl-2-pyrrolidone; PMMA, poly(methyl methacrylate); MIBK, methyl isobutyl ketone; IPA, isopropyl alcohol.

2.5 Wire bonding and fridge loading

With the finished devices ready to measure, we need to connect the (sub)-micron scaled device circuitry to macroscopic measurement equipment. In lack of a better analogy, we can think of the following process as packing a series of *babushka dolls* – a small piece is put into a repeatedly growing piece.

First, the finished chip is glued onto a printed circuit board (PCB) daughter-board hosting 48 DC lines lines with the help of silver paste. The ensemble is left to dry in air with reduced particle count, although this was done prior in atmospheric air successfully also. The daughter-board is mounted in a wire bonder where the before-mentioned bond pads (which are connected to the devices by EBL-defined Ti/Au leads) are hooked-up to the 48 lines of the daughter-board by a series of Al threads. See Fig. 2.5 **a-b** for an example of

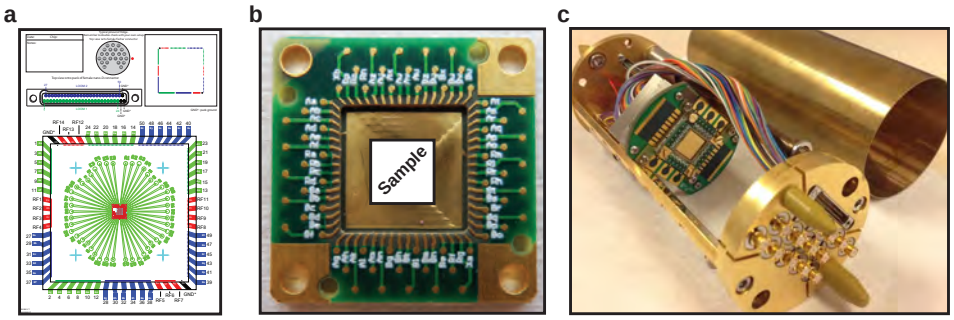

Figure 2.5: **Sample mounting. a**, Example of a pin-out sheet used to track the Al threads connecting the sample to the daughter-board. **b**, Daughter-board with white box indicating the sample placement. **c**, Open Triton puck with both mother board and daughter board mounted. The design and production has been developed by Ferdinand Kuemmeth and Morten Madsen and is referred to as QDev boards. Image courtesy F. Kuemmeth.

a sheet used for cross-referencing which device leads are connected to which lines in the fridge. Following, the daughter-board (panel **b**) is mounted into a complementary mother-board, which depending on the refrigeration setup is either contained by a Triton puck (panel **c**) or sitting inside the fridge.

In the Heliox system each of the 48 DC lines now extend through the fridge and are wired to a piece of hardware called the break-out box. From here macroscopic measurement equipment can be hooked up the nano-scaled devices via BNC break-outs.

The Oxford Triton fridge is loaded by mounting the daughter-board into the mother-board this time sitting inside the puck. The puck is a cylindrical piece of copper which can be loaded into the Triton fridge idling at a temperature on the order of tens of Kelvin. This step omits the need to disassemble the fridge for device exchange and the need for a full room-temperature warm-up saving a significant amount of time between sample changes. After the puck is loaded into the fridge, similar to before, the device can be accessed electrically via a break-out box.

2.6 Measurement setup

This section covers the basics of device cooling and the measurement setup used through-out most of this work.

Cooling the sample

To energetically resolve typical condensed matter quantum phenomena, the thermal energy of the carriers in the sample needs to be smaller than the energy scales of interest ($k_BT<E$). Two different types of fridges (the Heliox and Triton) have been utilized for the presented measurements, both of which are cryo-free/dry, meaning that no extraneous cryogenic liquids are needed for operation.

The Heliox

The first cooling stage of the Heliox system relies on vapor-compression refrigeration, in which a cooling agent (^{4}He) is compressed leading to an increase in pressure and temperature. The now heated gas is moved through a condenser where excess energy is removed allowing the gas to cool. Next, the gas is moved through an expansion valve which allows for a rapid drop in pressure lowering the temperature below its initial value. The cold gas is now moved to a region where cooling power is desired. Returning from the cooling site the gas is routed back to the compression circuit and the cycle repeats. For a given system the base temperature is obtained when the heat-load on the system and cooling power equilibrate. If the Heliox is operated only with the compressor, the temperature at the sample mounted on the cold-finger on the Heliox settles at about 2.6 K.

The system can be cooled further by engaging the so-called sorption pump of the system. The sorption pump is a porous material which condenses ^{3}He stored within the fridge as the system is cooled by a compressor. Next, by the help of a local heating element the condensed ^{3}He is released providing additional cooling power. Following, the gas is recondensed and moved through the circuit by a low pressure obtained by re-cooling the sorption pump. This

process can keep the system at a temperature of about 300 mK for roughly 2 days.

The Triton

In broad terms, the near-perpetual cooling power of a Triton unit is made up by a two-part process. A pulse tube refrigerator cools a stage within the system to about 4 K to which a mixing chamber is thermally connected.[41] This is the chamber to which the sample is thermally connected after loading. As the system approaches $T \sim 10$ K another process initiates in which ^{3}He and ^{4}He are continually mixed inside the mixing chamber. The ^{3}He-pure phase is run through a diluted phase composed of 6.6% ^{3}He and 93.4% ^{4}He. This mixture has a finite solubility even as the temperature converges towards 0 K and is separated by a phase boundary.[42] The energy needed for the ^{3}He to cross the phase boundary and become diluted in the ^{3}He-^{4}He-mixture is extracted from the environment providing the cooling power. As long as the entire refrigerator is in good shape, a base temperature of tens of mK can be maintained for extended periods of time. A deeper explanation of this requires Fermi and Bose statistics of the half-integer and integer spin He isotopes and we will be omitted due to brevity.

Having brought the sample to temperatures where thermal smearing is significantly smaller than the energy scales of interest, we are ready to measure.

Voltage-bias

This section goes over the basics of the two-probe voltage-bias setup used for most devices discussed in this work (Fig. 2.6). A Stanford Research SR830 lock-in amplifier sources an AC voltage in the range of $f \sim$ 70-200 Hz, avoiding higher harmonics of the 50 Hz frequency of the in-house electrical grid. In addition, a DC signal is sourced from a digital-analog-converter (either a Harvard DECADAC or Keithley SMU). Both signals are mixed in a custom-made voltage divider and their amplitude is down-converted by a factor determined by the ratio between the chosen in-line resistance and a resistance going to ground. The effective amplitude of the AC signal depends on the balance between obtaining a good signal-to-noise ratio and minimizing any signal broadening of the relevant experimental parameter, such as the superconducting gap ($\Delta_{\mathrm{Pb}} = 1.2$ meV) or the addition energy of a typical nanowire quantum dot (E_{add} ~1-20 meV). Typically, the AC signal is reduced by a factor 10000 yielding excitation voltages of ~1-20 µV. A low-frequency of the excitation voltage is chosen such that any phase shifting from the fridge filters is minimized but should be large enough to obtain low integration times. To avoid operating the DC signal at the limit of the bit resolution we divide the signal by a factor 1000 providing a resolution of approximately 30 nV.

In order to record the differential current the signal outputted from the

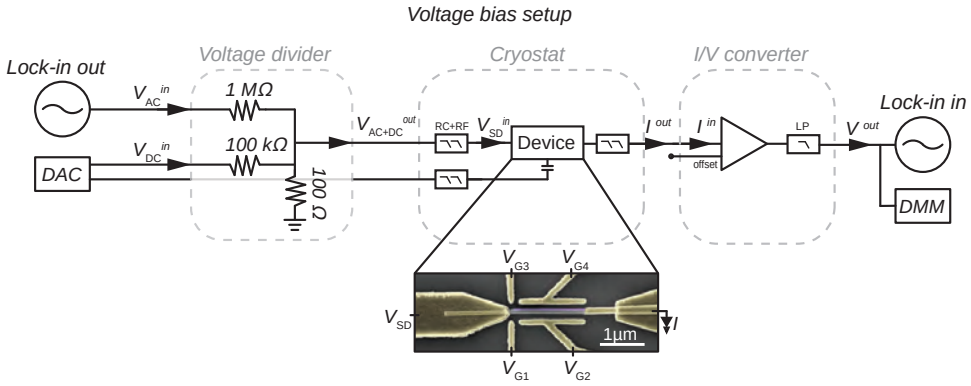

Figure 2.6: **Generic voltage bias setup.** Two-probe voltage bias setup used for most experiments.

sample is converted by a Basel I/V converter which also amplifies the signal (typical ranges are $10^5 - 10^7$). The AC current is recorded by the lock-in and converted into differential conductance (dI/dV) whereas the DC current is measured by a digital multi-meter. The voltage applied to the gates of the devices is typically controlled by a DECADAC, Keithley SMU or a QDAC.

This concludes the introductory chapter on material growth, device fabrication and measurement techniques. In the subsequent we shall focus on the manuscripts related to this work.

CHAPTER 3

EPITAXIAL PB ON INAS NANOWIRES FOR QUANTUM DEVICES

T. Kanne, M. Marnauza, D. Olsteins, D. J. Carrad, **J. E. Sestoft**, J. de Bruijckere, L. Zeng, E. Johnson, E. Olsson, K. Grove-Rasmussen, J. Nygård, 2021. *'Epitaxial Pb on InAs nanowires for quantum devices'.*
Nature Nanotechnology, pp.1-6.

Semiconductor-superconductor hybrids are widely used for realising complex quantum phenomena such as topological superconductivity and spins coupled to Cooper pairs. Accessing new, exotic regimes at high magnetic fields and increasing operating temperatures beyond the state-of-the-art requires new, epitaxially matched semiconductor-superconductor materials. The challenge is generating favourable conditions for heterostructure formation between materials with the desired properties. Here, we harness increased knowledge of metal-on-semiconductor growth to develop InAs nanowires with epitaxially matched, single crystal, atomically flat Pb films with no axial grain boundaries. These highly ordered heterostructures have a critical temperature of 7 K and a superconducting gap of 1.25 meV, which remains hard at 8.5 *T, thereby more than doubling the available parameter space. Additionally, InAs/Pb 'island' devices exhibit magnetic field-driven transitions from Cooper pair to single electron charging; a pre-requisite for use in topological quantum computation. Semiconductor-Pb hybrids potentially enable access to entirely new regimes for an array of quantum systems.*

Contributions: Thomas Kanne, Mikelis Marnauza and Dags Olsteins developed the nanowire materials. Transmission electron micrographs (TEM) were recorded by Mikelis Marnauza. Material handling and device fabrication was developed by Dags Olsteins. High-angle annular dark-field scanning TEM micrographs were recorded by Lunjie Zeng. Measurements and device fabrication for the tunnel probe devices were performed by Damon Carrad. My contributions were fabrication, measurements and analysis of the island devices with assistance of Joeri de Bruijckere.

3.1 Introduction

The development of high-quality semiconductor-superconductor heterostructures underlies the pursuit of new types of quantum bits based on exotic physics arising at the hybrid interface [5, 10, 43, 44, 45, 46, 47, 48]. Aside from the ability to host novel two-level systems [49, 50, 51, 52, 53], when the underlying materials exhibit strong spin-orbit coupling, a high g-factor and 'hard gap' induced superconductivity[9], they are ideally suited for supporting topological superconductivity under applied magnetic field[54, 55, 43, 46, 56, 44, 45, 5, 53]. Signatures of topological superconductivity in these systems have been studied almost exclusively using Al and Nb(TiN) as the superconductor and InAs or InSb as the semiconductor, with the large spin-orbit coupling and g-factor ensuring the suitability of these semiconductors[5]. By contrast, there is strong interest in improving the superconductor material to broaden the scope of hybrid applications[57, 58, 47], since Al has a relatively low critical temperature, T_C and field B_C [9], while the soft gap of Nb-based hybrids has thus far prevented isolated hybrid segments supporting Cooper pair charging [56, 57, 59, 47, 60]; a crucial requirement for topologically protected qubit schemes[61]. While other superconductors – e.g., Pb[62] – have been used to make devices through ex-situ deposition methods, such an approach is ultimately not suitable since these devices contain interface impurities – which prevent obtaining hard gap superconductivity required for topological quantum bits [9, 47, 56] – and the necessity of depositing thick superconductor layers prohibits obtaining $B_C > 1$ T. The main goal is therefore development of epitaxial hybrids exhibiting a large, hard gap resilient to high

magnetic fields and elevated temperatures[57, 58, 47].

In this article we present hybrid nanowires utilising Pb as the superconductor, which possesses the highest bulk T_C and B_C of all elemental type-I superconductors, vastly extending the hybrid parameter space. We achieve hybrid structures with a single Pb crystal on each InAs facet with no axial grain boundaries. All previous semiconductor-superconductor nanowire heterostructures exhibited axial grain boundaries and/or polycrystallinity[10, 63, 57, 58, 47]. In addition to depositing the Pb films without breaking vacuum after InAs nanowire growth[10, 63, 57, 58], achieving this unprecedented quality of hybrid epitaxy required employing carefully controlled, theoretically motivated growth conditions which promote strong thermodynamic driving forces towards single crystal formation with a low energy domain match. The single crystal Pb suppresses the potential for impurity-generated discontinuity of the hybrid wavefunction[46], which may occur in granular films[63, 57, 58, 47]. Further, the theoretical description used to optimise the epitaxial structures through consideration of thermodynamic driving forces and structural factors leads to increased understanding of metal/semiconductor epitaxy. The epitaxial InAs/Pb structure yields a hard induced superconducting energy gap of $\Delta \sim 1.25$ meV, corresponding $T_C \sim 7$ K, and B_C exceeding 8.5 T, the highest reported values for epitaxial semiconductor-superconductor hybrids. In addition, InAs/Pb 'island' devices support Cooper pair charging due to the hard gap. At finite magnetic field, this evolves into single electron transport through a bound state[56, 59, 57, 60, 64, 47]; a crucial feature demonstrating the hybrid nature of the system. The elimination of axial grain boundaries and dramatic enhancement of the accessible parameter space represented by InAs/Pb hybrids make them prime candidates for use in a wide range of semiconductor-superconductor hybrids based on nanowires[43, 46, 49, 51, 50], selective area grown networks[65, 66], and planar heterostructures[67, 68]. Further, Pb possesses features that distinguish it from other elemental superconductors, such as two-band, strong-coupling superconductivity and a large spin-orbit coupling, which may lead to the emergence of new phenomena in semiconductor-superconductor physics [5, 53, 69, 70, 48, 49, 51].

3.2 InAs/Pb epitaxy

Aside from the attractive physical properties, the choice of Pb was based on analytical considerations of the central stages in metal film growth on different semiconductor nanowires. To do this, we theoretically assessed structural stability in combination with estimates of the interplay between the four contributions to the overall excess energy, which determine the thermodynamic driving forces and kinetic limiting factors. A full description is given in Supplementary Section 1 and an additional 12 elemental superconductors on InAs nanowires are theoretically studied in Supplementary Section 2. For low temperature depositions ($T < 150$ K) it is energetically favourable for Pb to grow in a single crystallographic orientation with respect to InAs. Combined with the high grain boundary mobility of Pb, this suggests that growth of Pb on InAs would result in large crystals with an epitaxial match to the nanowire. In contrast, epitaxial Al grows in 2 or 4 orientations on InAs depending on thickness[10], and other superconductor materials employed so far feature no long-range order[57, 58, 63, 47], consistent with our findings in Supplementary Section 2. These findings suggest that InAs/Pb is structurally the optimal material combination for hybrid III-V semiconductor single element superconductor devices. Although we focus on InAs/Pb nanowires in this article, Pb may be compatible with other semiconductors (see Supplementary Section 3.2), and our results should translate to InAs-based planar heterostructures[68, 67] and selective area grown networks[65, 66]. Further, the framework presented in Supplementary Section 1 is instructive in developing the range of semiconductor-metal epitaxial structures.

Figure 6.1a shows a scanning electron microscope (SEM) micrograph of a hexagonal InAs nanowire with Pb deposited on two facets. The wurtzite InAs nanowires were grown along the [0001]B direction using molecular beam epitaxy (MBE), with flat $\{1\bar{1}00\}$ facets. The hexagonal morphology was optimised as outlined in Methods and Supplementary Section 3. After the nanowires were grown the wafer was transferred without breaking ultra-high vacuum to a second chamber where the substrate was placed on a liquid nitrogen cooled substrate holder, $T \sim 120$K, for several hours, before Pb was deposited using e-beam evaporation[57, 58, 63]. The inset in Figure 6.1a

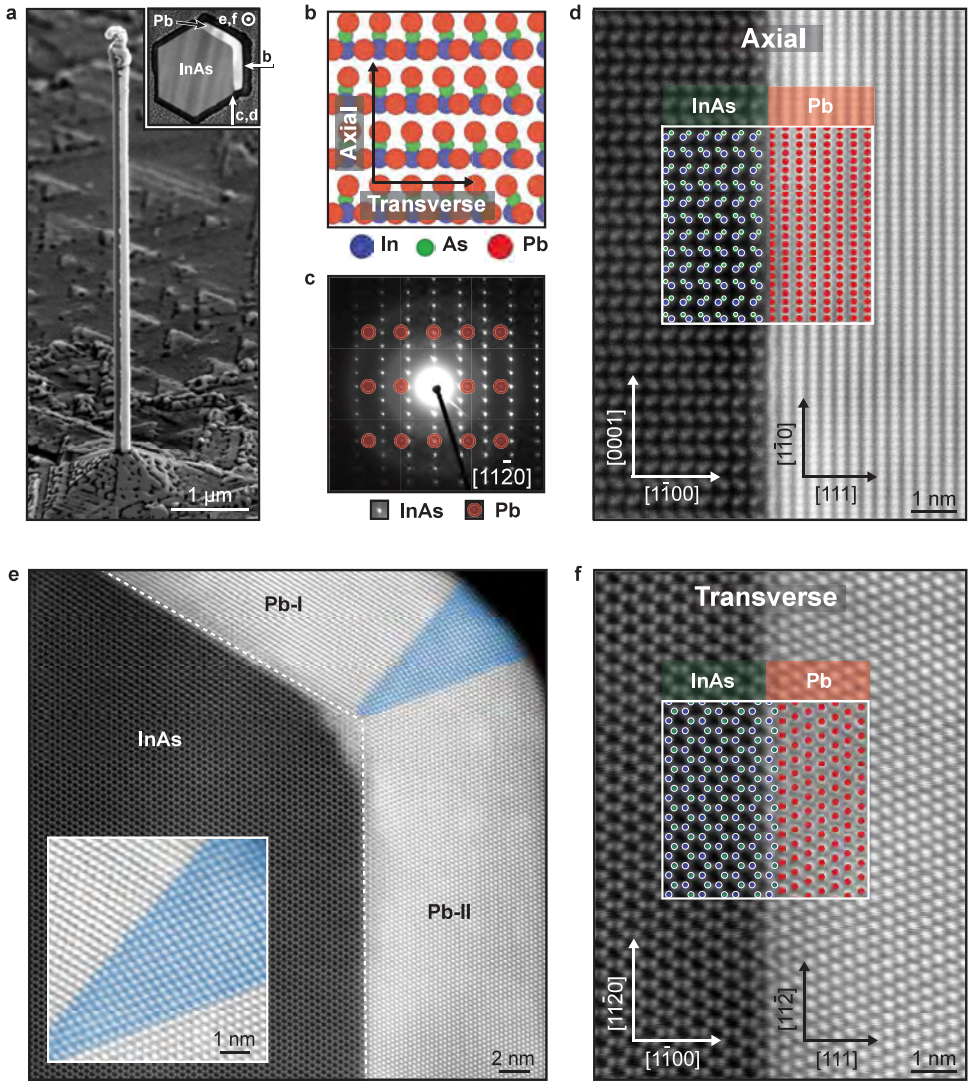

Figure 3.1: **InAs/Pb bi-crystal interfacial match.** **a**, Scanning electron micrograph of an InAs nanowire with a 10 nm Pb thin film on two facets. Inset shows a HAADF STEM micrograph of a cross-sectioned InAs/Pb/Si heterostructure. **b**, Simulated relaxed bi-crystal match between InAs (blue, green) and Pb (red) viewed normal to the nanowire facet. **c**, Selected area electron diffraction pattern of an entire nanowire along the $[11\bar{2}0]/[11\bar{2}]$ direction. Pb diffraction peaks are marked with red semi-transparent circles. **d**, Atomic resolution HAADF STEM micrograph of the InAs/Pb interface along the $[11\bar{2}0]/[11\bar{2}]$ direction parallel to the nanowire facet. Simulated relaxed bi-crystal interfacial match overlayed and marked with a white box. **e**, HAADF STEM micrograph along the $[0001]/[1\bar{1}0]$ direction of the corner between two adjacent facets, highlighted with white dotted lines. Two single Pb crystals are connected by a wedge shaped single crystal (false coloured blue). **f**, Atomic resolution HAADF STEM micrograph of the InAs/Pb interface viewed along the transverse direction as in **e**. Theoretically relaxed bulk bi-crystal interfacial structure superimposed on interface.

shows a low magnification high angle annular dark field scanning transmission electron microscope (HAADF STEM) micrograph of a cross-sectioned InAs/Pb/Si heterostructure. Figure 6.1a shows the modeled relaxed hetero-epitaxial match along $[1\bar{1}00]$(InAs)/[111] (Pb) directions and the arrows indicate the axial and transverse direction. Figure 6.1c shows a selected area electron diffraction (SAED) pattern of an entire nanowire, oriented along the $[11\bar{2}0]/[11\bar{2}]$ direction parallel to the nanowire facet. Notably, only one Pb orientation relative to the InAs nanowire facet is observed (red circles), confirming the hypothesis that a Pb thin film forms a single crystal along an entire nanowire facet. Transmission electron microscopy of nanowires from more than 10 growths, with varying growth conditions, contained no evidence of axial grain boundaries.

Figure 6.1d shows a high resolution (HR) HAADF STEM micrograph of the InAs/Pb interface where the orientation is similar to that of Fig. 6.1c. The inset in Fig. 6.1d shows how the theoretically predicted, strain relaxed, hetero-epitaxial match fits to the observed interface. From this, a particularly small bi-crystal interfacial domain is found along the $< 0001 >/< 1\bar{1}0 >$ nanowire growth direction, with two planes of Pb for each plane of InAs and a bulk residual mismatch of only 0.35%. From HR TEM investigations of the entire nanowire length no edge-dislocations were found, indicating that the small strain needed to obtain the epitaxial domain is absorbed. Figure 6.1e presents a HAADF STEM micrograph of the cross-sectioned InAs/Pb nanowire shown in Fig. 6.1a (inset). The two grains (I, II) form single crystals along their entire nanowire facet, and are merged by a wedge-shaped single-crystalline domain, false coloured blue. The inset in Figure 6.1e shows how the wedge-shaped grain accommodates two coherent grain boundaries and thus reduces the grain boundary energy between the single I and II crystals. Strain in InAs and Pb along the transverse direction is observed by comparing the STEM micrograph and the predicted strain relaxed hetero-epitaxial match in Figure 6.1f. By utilizing the average $\{1\bar{1}00\}$ plane spacing as a scale to measure the relative stress in the structure, Pb along the $< 11\bar{2} >$ direction was measured to be compressively strained by $\sim$ 1.7 % whereas InAs along $< 11\bar{2}0 >$ direction was found to be tensile strained by $\sim$ 0.7 %. Assuming that the InAs $\{1\bar{1}00\}$ planes are not heavily influenced by the

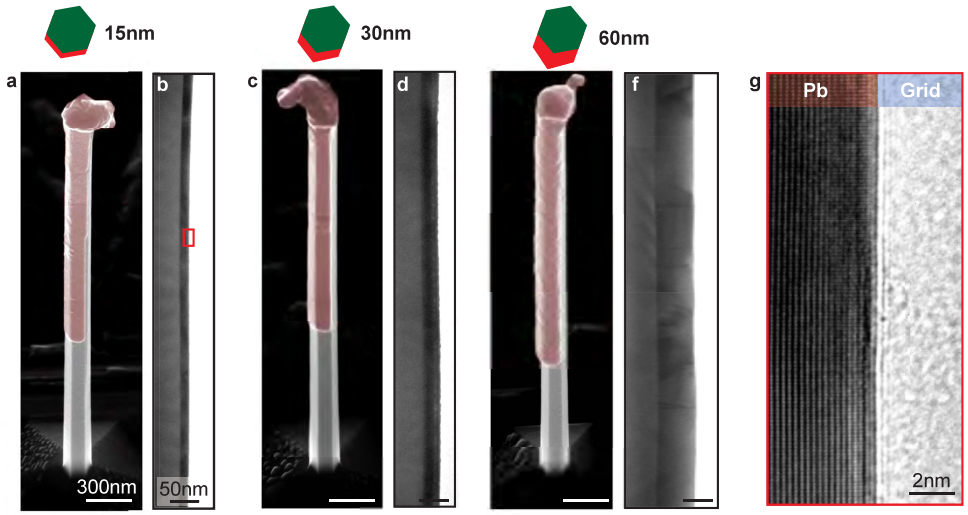

Figure 3.2: **Pb thickness dependent morphology.** Pb grown on two facets of the InAs nanowires masked by adjacent nanowires. **a**,**c** and **e** show surface sensitive SEM micrographs of 14 nm, 28 nm and 60 nm in-situ deposited Pb films, respectively. The micrographs have the same scale, shown in **a**. **b**,**d** and **f** present LR-TEM micrographs of same thicknesses and same scale shown in **b**. **g** HR-TEM micrograph of the terminating layer of a 14 nm thin film marked with a red square in **b**. Note the contrast changes observed in **f** are due to bending contours, and that no axial grain boundaries were observed in any Pb film on InAs nanowires. Some Pb rugosity is evident, likely due to the high deposition rate (3 Å/s), which was necessary to ensure a high initial cluster density (see Supplementary Section 1).

interface, the compressed Pb and expanded InAs indicate that the transverse bi-crystal interfacial match seeks a domain of two interface planes of InAs for three planes of Pb. More detail is provided in Supplementary Section 3.1. The presented single crystal nature and epitaxial relation relative to the InAs nanowire facets was found for all investigated Pb thicknesses (5-60 nm) and Pb thus appears robust against stress driven terms such as incoherent grain boundaries. Additional TEM data is provided in Supplementary Section 3.2.

To study the Pb film morphology, surface sensitive scanning electron microscopy (SEM) micrographs of InAs/Pb hybrids are shown in Figs 6.2a,c,e for 14, 28 and 60 nm Pb films, respectively. Patterning of the Pb coatings was implemented to enable comparative analysis of core/shell morphol-

ogy and achieved by adjacent nanowires acting as shadow masks during Pb deposition[36, 35, 47]. Figures 6.2b,d,f show bright field TEM micrographs for the different Pb thicknesses, and Fig. 6.2g shows a HR TEM micrograph of the terminating planes of a 14 nm film of Pb marked with a red square in Fig. 6.2b. The Pb morphology is continuous and atomically flat for most of the investigated film thicknesses (5 nm - 28 nm). However, above a critical thickness (in our case $\sim$ 50 nm), dependent on the growth conditions, the surface becomes more rough (Fig. 6.2e). In Fig. 6.2f, bending contours and contrast changes are observed, indicative of strain fields in the Pb film. This may be caused by the increased strain imposed by the grain boundaries between the adjacent facets or a slight bending of the nanowires, likely due to either thermal expansion coefficient differences or axial strain [10, 58].

Alongside the intrinsic interest in obtaining a single crystal superconductor on a single crystal semiconductor, such structures are attractive for hybrid and topological applications to ensure that boundaries of the quantum system coincide with the geometrically defined ends of the superconducting segment, rather than, e.g., at an impurity[46]. Achieving the structures presented here required detailed understanding of how to control and promote epitaxial growth, via thermodynamic and grain growth kinetics considerations. We focus specifically on Pb, with more general explanations provided in Supplementary Section 1-3. The aim during the initial phase of Pb thin film growth is to promote layer-by-layer-like growth. For island growth this is achieved by decreasing the critical cluster size and thereby increasing the initial concentration of critical clusters [71]. Experimentally, this is done by lowering the substrate temperature and increasing the material flux. After the initial clusters have been established they start to grow. In this phase, interface and strain energy may result in recrystallization of the clusters in a kinetically limited process due to the thermodynamic driving forces. In a later stage the clusters start to impinge and coalesce into a single crystal, which is now strongly dependent on the main contributions to the overall excess energy [72, 73]. We find it especially important to have very well defined nanowire facets to decrease the interface and strain energy (Supplementary Section 1.2). The micrographs in Figs 6.2a,c suggest that after a continuous Pb film has grown, the growth switches to layer-by-layer mode. Here, small

islands on the completed atomically flat layer act as nucleation sites for the next layer. Upon warming to room temperature and subsequent exposure to oxygen the Pb thin film may dewet since it grows far from thermodynamic equilibrium[74]. Dewetting was eliminated by keeping the substrate on the cold holder for approximately 10 hours after terminating growth, which ensured that continuous Pb films with no axial grain boundaries were obtained. Dewetting and oxidiation of Pb thin films could potentially also be prevented by growing a capping layer with a lower dewetting probability.

3.3 Tunneling spectroscopy of InAs/Pb junctions

Having obtained epitaxial InAs/Pb heterostructures free of interface impurities, we expect hard gap superconductivity with the inherited properties of the Pb film[9]. To characterise this we performed electron transport measurements on normal metal-superconductor (NS) tunnel junctions with the device geometry shown in Fig. 3.3a. Prior to normal metal contact deposition, the Pb was selectively etched using H_2O, such that a bare InAs segment remained between the normal metal and superconductor (Methods and Supplementary Section 5). This segment acts as a tunnel barrier, tunable using side-gate voltage V_G[9, 43]. Figure 3.3b shows differential conductance, g, normalised to the normal state conductance, $g_N = g|_{V_{SD}=2mV}$, as a function of source-drain bias voltage V_{SD} at zero magnetic field (red) and finite parallel magnetic field, $B_\parallel = 7.5$ T (blue). The strong g suppression observed for $|V_{SD}| < 1.25$ mV reflects the superconducting energy gap, Δ, in the single-particle density of states of the InAs/Pb nanowire. The hard gap is a result of an extremely low interface impurity density and transparent electrical contact, enabled by the epitaxial InAs/Pb interface. The 'hardness' value of 100 is similar to that reported in III/V nanowires with epitaxial Al[9, 35, 64], polycrystalline Sn[47] and amorphous Ta[57], albeit here with a much larger Δ. Gate voltage-dependent bias spectroscopy for seven devices (Supplementary Section 4.1) shows that the gap is highly robust in V_G, excluding the possibility that the features attributed to Δ in Fig. 3 are due to e.g. Coulomb blockade.

The evolution of the superconducting gap in a parallel magnetic field, $B_\parallel$, is shown in Fig. 3.3c. The gap remains hard over the entire 8.5 T range ac-

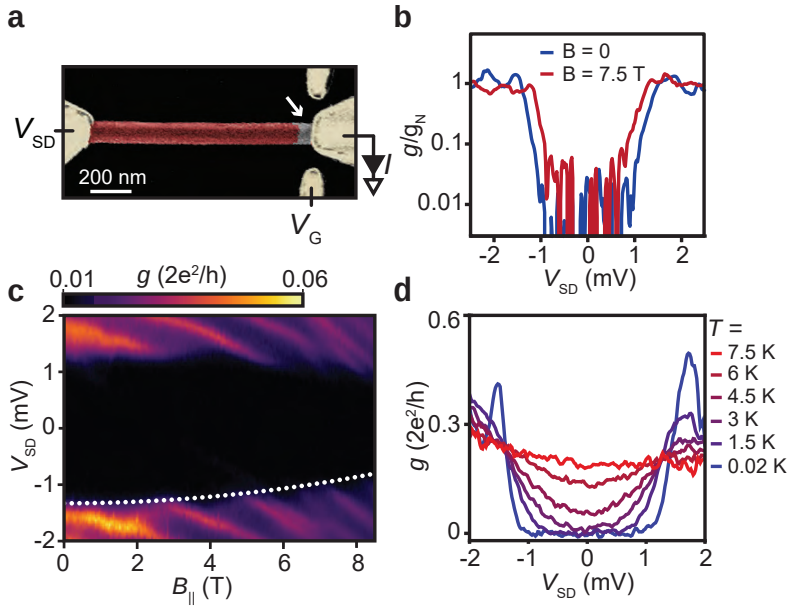

Figure 3.3: **Hybrid InAs/Pb tunnel spectroscopy.** **a**, False coloured SEM micrograph showing the InAs/Pb hybrid nanowire tunnel spectroscopy device with Ti/Au contacts and gates (yellow), 9 nm thick Pb (red) and bare InAs nanowire segment (grey; also indicated by white arrow). The measurement circuit consists of source-drain bias V_{SD}, measured current I, and the gate voltage V_{G}, used to control the tunnel barrier. **b**, Differential conductance, g, normalised to the normal state conductance, $g_{\mathrm{N}} = g|_{V_{\mathrm{SD}}=2\mathrm{mV}}$, as a function of V_{SD}, showing 100-fold conductance suppression within $\pm\ \Delta\ \sim\ 1.25$ meV at $B = 0$ (blue) and $\pm\ \Delta\ \sim\ 1.1$ meV for $B_{\|} = 7.5$ T (red). **c**, g as a function of V_{SD} and parallel magnetic field, $B_{\|}$, showing the persistence of highly suppressed conductance until 8.5 T. Dashed white lines serve as guide to the eye. **d**, g as a function of V_{SD} recorded at increasing T from 0.02 to 7.5 K.

cessible in our cryostat, highlighted by the blue trace in Fig. 3b. The above-gap resonances likely arise from device-specific states in the tunnel barrier, which in this measurement obscured the coherence peaks (see Supplementary Fig. S15). Measurements from devices with varying Pb thickness revealed $B_C > 3$ T for 19 nm thick Pb, and $B_C = 0.8$ T for 50 nm thick Pb (Supplementary Fig. S16). Figure 3.3d shows the temperature dependence of the superconducting gap. As temperature, T, is increased, Δ decreases and the edges broaden, up to the critical temperature $T_C \sim 7$ K. Notably, the gap remains hard at $T = 1.5$ K, and is still prominent at $T = 4.5$ K. The values for Δ, T_C and B_C of the hybrid InAs/Pb nanowires are each more than four times larger than for state-of-the-art Al-based hybrid devices[9, 57, 64, 35], and exceed the metrics reported for InSb/Sn hybrids[47]. Josephson junctions with ex-situ fabricated Pb/Ti contacts on InAs nanowires showed supercurrent operation up to 4.5 K and applied field around 0.3 T[62], thus utilizing the high T_C and large gap properties of Pb, but at significantly lower field than demonstrated here. Moreover, ex-situ Pb-based contacts have been successfully implemented in carbon nanotube devices[75]. In Supplementary Fig. S16 we show magnetic field dependencies for different Pb film thicknesses, illustrating that thin films (~ 10 nm) are required to obtain the highest B_C.

3.4 Coulomb blockade spectroscopy of InAs/Pb islands

Essential requirements for semiconductor-superconductor heterostructures in the context of topological qubit development are for isolated hybrid segments – 'islands' – to host quantised charge in units of $2e$, and the observation of single electron transport through bound states in finite $B_{\parallel}$ [56, 59, 60, 47, 64, 76, 61, 59]. Figure 4a shows an InAs/Pb island device, with the Pb selectively removed at either end and contacted by Ti/Au. The side gates control the island-contact coupling and the middle gate adds charge in discrete units. Spectroscopic operation is demonstrated in Fig. 4b, with g plotted versus V_{SD} and V_{G} (see Methods and Supplementary Section 4.3 for a discussion on the simultaneous operation of the two plunger gates which defines V_{G}), revealing periodic Coulomb diamonds due to the sequential addition of charge in units of $2e$ with an addition energy of ~ 1.8 meV, which corresponds to $8E_{\mathrm{C}} = (2e)^2/C$ [59]. The regions of negative differential conductance below Δ indicate the onset of long-lifetime quasiparticle tunneling[56, 59, 60]. For $|V_{\mathrm{SD}}| > 1.2$ mV, the Coulomb diamond periodicity doubles in V_{G}, since above-gap quasiparticle states support $1e$-periodic transport.

The $2e$-periodicity for $e|V_{\mathrm{SD}}| < \Delta$ in hard gap hybrids arises due to the odd charge states being lifted in energy by Δ compared to even charge states (Fig. 4c, top panel inset). For soft gap hybrids[77, 78] the finite density of states within the gap may enable single electron tunneling and $1e$-periodicity at zero bias. The importance is that proposed topological qubit architectures rely on magnetic field induced zero energy bound states[61], and the topologically-protected qubit operation potentially offered by these devices is obviated if soft-gap states are present. Therefore, observing both zero-field $2e$-periodic transport and bound-state-induced $1e$-periodic transport are highly important steps in hybrid material development.

The magnetic field dependent behaviour of the same InAs/Pb island was studied using a gate voltage configuration giving a smaller addition energy of ~ 1.2 meV (Fig. 4c). At $B_{\parallel} = 0$ (top panel), $2e$-periodic charging is observed below Δ. Increased $B_{\parallel} = 1.1$ T (Fig. 4c middle panel) causes a bound state to move towards zero energy[46, 56, 59, 60], and fall below E_{C}. Odd-state

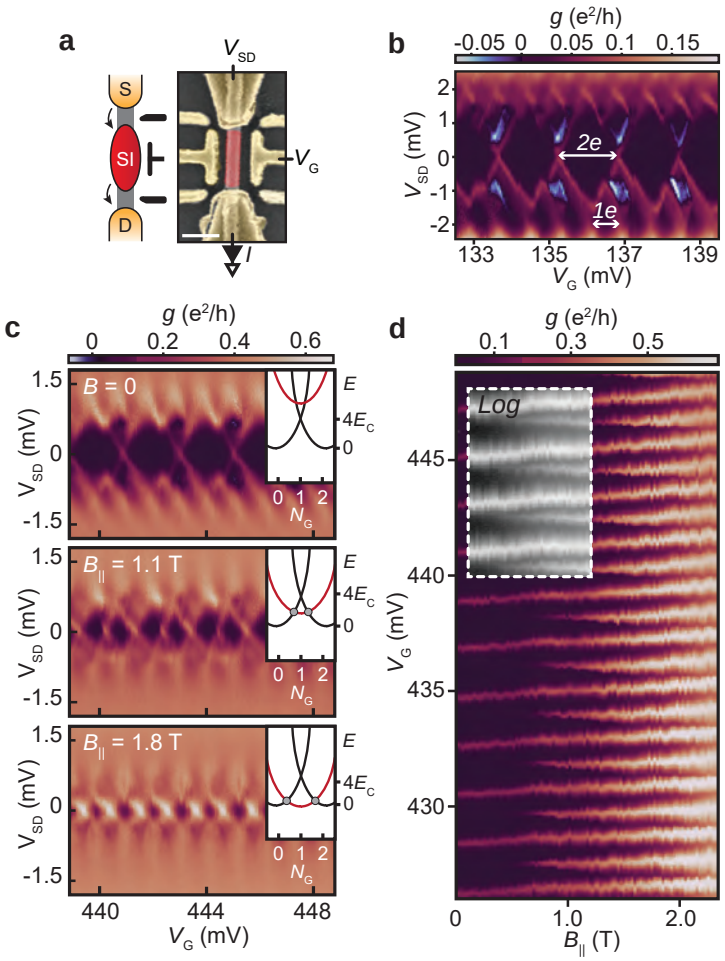

Figure 3.4: **Hybrid InAs/Pb island. a,** Schematic of a hybrid island device. Source, drain and superconducting island are denoted S, D and SI, respectively, with the black electrostatic gates used to control single electron (or Cooper pair) tunnelling events, illustrated by the arrows. False coloured electron micrograph of a InAs/Pb island device featuring Ti/Au contacts and gates (yellow), 14 nm thick Pb etched segment (red) and narrow bare InAs segments (grey). Scale bar is 500 nm. **b,** g vs V_G and V_{SD} showing Coulomb diamonds with spacing proportional to $2e$ ($1e$) for $|V_{SD}|$ less than (greater than) $\Delta/e \sim 1.2$ mV, indicative of Cooper pair (single electron) charging. **c,** g vs V_{SD} and V_G for $B_{||} = 0$, 1.1, and 1.8 T. Insets: Island energy, E, as a function of normalised gate voltage, N_G. Black (red) parabolas indicate even (odd) ground state energies, E_{even} and E_{odd}. Top panel: Cooper pair charging energy, $4E_C < E_{odd}$. Middle panel: $0 < E_{odd} < 4E_C$. Bottom panel: $E_{even} = E_{odd} = 0$. **d,** Zero-bias conductance as a function of V_G and parallel magnetic field. Coulomb resonances split from a regular $2e$ spacing ($4E_C < E_{odd}$), to even/odd ($0 < E_{odd} < 4E_C$) to a regular $1e$ spacing ($E_{even} = E_{odd} = 0$) as a function of parallel magnetic field. Inset: Conductance plotted on logarithmic scale ($\log_{10}(g)$) to increase visibility of the low magnetic field behavior.

occupation is now enabled (Fig. 4c middle panel inset), with the differing even/odd charging energies producing parity-dependent, even/odd spacing of Coulomb diamonds. Further increasing $B_{\parallel} = 1.8$ T (lower panel) brings the bound state close to zero energy.

Figure 4d presents the $B_{\parallel}$-dependence of g versus V_G at zero bias, corresponding to the data in Fig. 4c. The $2e$-periodic peaks split with increasing $B_{\parallel}$ — highlighted in the inset by the logarithmic greyscale plot — with varying even/odd spacing (see Supplementary Fig. S18). The peak intensity asymmetry between even and odd peaks can be attributed to a difference in the electron-like and hole-like components of the bound states [79, 59, 47]. These data indicate the emergence of a zero energy hybrid bound state in the InAs/Pb island, consistent with the charging model presented in the insets of Fig. 4c, and previous experiments using Al- and Sn-based hybrids[56, 60, 65, 59, 57, 47]. We observed similar features in four devices (Supplementary Fig. S17). These results encourage future work including, e.g., island-length-dependent studies[56, 60] or demonstrations of braiding[61], which may give indications of topological modes in InAs/Pb hybrids.

Discussion

The formation of a flat, epitaxially matched single crystal along the entire nanowire confirms the expectations from theoretical considerations of thermodynamic driving forces and structural stability of Pb on InAs. The framework used to investigate elemental superconductor growth on semiconductor nanowires can be extended to other metals and semiconductors, providing increased scope for development of metal/semiconductor epitaxy. In addition to the structural perfection, the epitaxial InAs/Pb hybrids provide a large and hard induced superconducting gap, with corresponding high T_C and B_C, offering a greatly extended experimental parameter space compared to current Al-based materials.[5, 57, 63, 9, 35]

The observation of $2e$-periodicity and bound-state-induced $1e$-periodic transport in an InAs/Pb island represents an important step in the development of large Δ, high B_C hybrid quantum devices[47], and encourages further experiments to evaluate the ability of the new hybrids to support topological

modes[46, 43, 56, 60, 53, 61, 5]. The absence of grain boundaries in the transport direction may prove critical to fabrication of increasingly ideal devices, by eliminating a potential source of decoherence[46]. Furthermore, the high field superconducting regime accessible in hybrids based on Sn [47] and in particular Pb may be advantageous for obtaining ballistic nanowires, bringing experiments closer to ideal Majorana models. Implementing Pb in future devices may also benefit from the strong intrinsic spin-orbit coupling of this heavy element superconductor, which has been used to induce spin-orbit coupling by proximity in, e.g., graphene[80, 81] and ferromagnets[82, 83]. Effects including reduced spin-orbit interaction from metallisation in Al-based devices[84] and trivial near-zero-bias bound states emerging near B_C provide continuing uncertainty surrounding whether commonly observed zero bias peaks truly constitute a signature of topological superconductivity[53]. Finally, recent scanning probe experiments on Pb-based topological systems[83, 85] may be complemented by exploring the strongly-coupled, two-band[86] superconducting nature of Pb — features that are still to be observed in hybrid devices.

3.5 Methods

The InAs nanowires were grown in a two step growth-process in a solid-source molecular beam epitaxy system. The nanowires were catalysed from electron-beam-lithography-defined Au particles and grown via the vapour-liquid-solid method. In the first step, InAs was grown axially for 30 minutes along the [111]B direction using As_4 and a substrate thermocouple temperature (T_{sub}) of 447°C, resulting in nanowire lengths ~ 7 μm. Growth was then interrupted to increase the As cracker temperature from 500°C to 800°C, yielding As_2, and the substrate temperature was lowered to (T_{sub}) to 350°C over 20 minutes. The second growth step proceeded under these conditions, radially overgrowing the nanowires for 30 minutes. The overgrowth step produced well-defined InAs nanowire facets, and also contributes to the 'bulky' shape of the top of the nanowires.

After nanowire growth, the substrate was transferred to an attached chamber with a precooled stage without breaking ultra high vacuum (pressures $\sim 10^{-10}$ Torr). The substrate was mounted on the cold substrate stage for 3

hours before any subsequent metal deposition to ensure a stable temperature (T_{sub}) of $\sim$ 120 K. We note that less time on the cold substrate holder is preferred due to the possible unwanted deposition of foreign materials from the system. To enforce in-situ nanowire masking and only two facet depositions, as shown in Figs 2a,c,e, the wafer was aligned relative to the pre-defined nanowire array. Pb was deposited with a shallow angle and rate (3 $\mathrm{\AA s^{-1}}$) using electron beam evaporation. After the metal deposition the substrate was kept cold on the substrate holder for more than 10 hours to limit dewetting, and produced films with flatter morphology.

SEM micrographs were produced by combining signals from the surface sensitive secondary electron detector and the atomic weight sensitive backscatter electron detector since Pb forms a flat film which is only seen clearly when using an atomic weight sensitive technique. STEM images were acquired using an FEI Titan 80-300 TEM equipped with a probe Cs corrector and operated at 300 kV. HAADF STEM images were taken with a beam convergence semi angle of $\sim$ 17.5 mrad. The inner and outer collection semi angle of the HAADF detector was set to 54 and 270 mrad, respectively. Cross section specimens of the nanowires were prepared using an FEI Versa 3D focused ion beam scanning electron microscope (FIB SEM), following Pt deposition to protect the nanowires. A final polish of the TEM specimens in FIB SEM with a 2 kV and 27 pA ion beam was used to minimize the damage caused by the Ga ion beam. The micrograph in Fig. 1d was produced by drift correcting and summing the amplitude of 100 HR HAADF STEM micrographs with a short acquisition time. The STEM micrographs in Figs 1e,f were noise reduced by removing the Fourier spectrum background amplitude. The structural simulation of the hetero-epitaxial interface in Fig. 1 was performed using the software program Vesta[87]. For Fig. 2 the Pb film thicknesses were measured on TEM micrographs of more than 5 different nanowires with a measured thickness divergence of $\pm$ 1 nm (for 14,28 nm) and $\pm$ 5 nm (for 50 nm). This may relate to slight misalignment and focus in the TEM and uncertainties related to scale calibrations.

Devices (Figs 3 and 4) were fabricated using electron beam lithography and lift off techniques, with Ti/Au (5 nm/250 nm) thin films for contacts and gates. H_2O (MilliQ with resistivity $\rho > 15$ MΩ) was used as a selective etchant

to remove Pb from the semiconductor surface, and Ar^+ milling used prior to contact deposition to remove native InAs oxides. Full details are given in the Supplementary Information. Standard voltage-biased lock-in techniques were used to measure the conductance of the devices in a dilution refrigerator with a base temperature of 25 mK. Prior to collecting the presented data on island devices (Fig. 4), the cross-coupling of the gates was measured. To collect the presented data, the gates were swept simultaneously according to the measured proportionality factors to ensure that V_G only altered island occupation and did not appreciably alter the island-lead coupling, or the chemical potential of the InAs segments (see Supplementary Section 4.3 for a more detailed discussion). The sensitivity of Coulomb-blockaded devices to nearby impurity (dis)charging can cause small offsets between successive V_G traces, as visible in Fig. 4d. Although much larger offsets are customarily corrected for[56, 59], we have chosen to present our uncorrected data 'as is', since such offsets do not influence the underlying physics. The measurements presented in Figs 3,4 were chosen as those with the best signal/noise ratio, low number – or absence – of impurity-related offsets, and provided the clearest evidence which led us to the main conclusions of our manuscript. Supplementary Section 4 presents data from a further 12 devices, and details regarding fabrication and yield.

CHAPTER 4

CONTINUED INAS/PB EXPLORATION

The subsequent section serves as an extension and data-backdrop to the previous chapter on hybrid InAs/Pb devices. As hybrid Pb-based devices currently are in their infancy and according material understanding and device operation are still in the works, we choose to present additional and less well-understood data to paint a fuller picture of this new structure. In certain passages the language is purposely vague as deep analysis and rigid understanding of all these data fall outside the scope of this more exploratory section.

4.1 Shadowed InAs/Pb/Au junctions tunnel junctions

Motivated by issues regarding contact formation to Pb, stemming from the unstable nature of the nano-scaled Pb films[31], efforts were made to move critical ex-situ fabrication in-situ. This spawned a so-far unexplored shadow technique of which growth details have been discussed in Chapter 2.3. Here Au films shadow evaporated locally on Pb serve as a contact platform omitting the need for ex-situ contact fabrication directly to the Pb film. This section describes data obtained from shadowed hybrid InAs/Pb/Au devices.

Hard induced superconducting gap

To form our tunnel junction device (Fig. 4.1 **a**) we first grow Au-seeded InAs nanowires in a molecular beam epitaxy system (MBE) and without breaking vacuum deposit Pb on two of the six facets via electron beam deposition. This evaporation is selectively shadowed by a proximal nanowire resulting in a clean gap in the superconductor and omits the need for etching. Next, the growth substrate is rotated and Au is evaporated from a different angle using a second and taller 'shadow nanowire' thus forming an in-situ metal

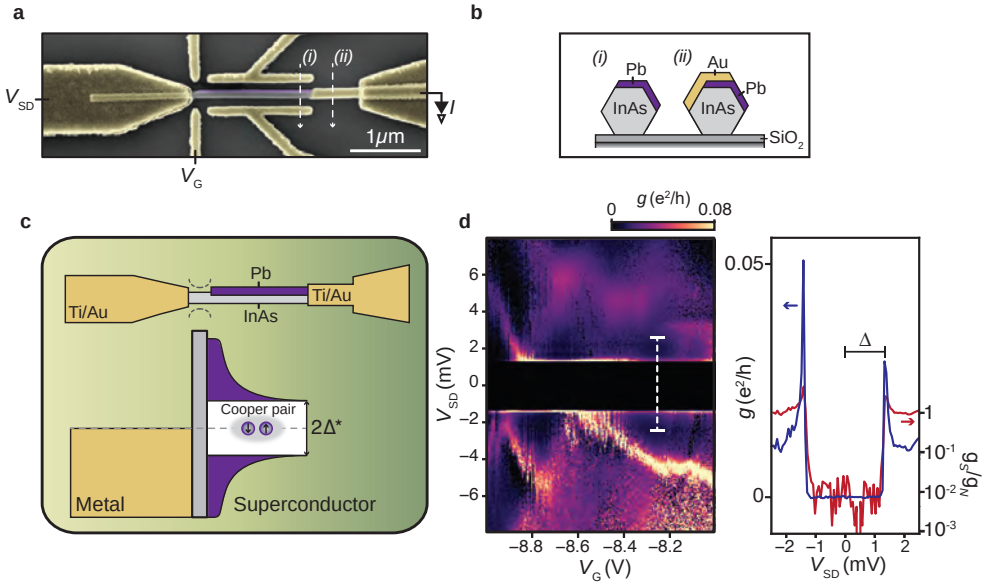

Figure 4.1: **InAs/Pb/Au tunnel junction device. a**, False-coloured SEM image of the measured device. Setup: source-drain bias, V_{SD}, measured current, I, and the gate voltage, V_{G}. *i, ii* show the cross-sectional cuts displayed in **b**. **b**, Cross-section schematic of the InAs/Pb/Au nanowire. **c**, Real-space (*top inset*) and energy-space (*bottom*) schematic of the device. **d**, Colour-map of differential conductance versus V_{SD} and V_{G}. **e**, Line-cut plotted on a linear and log-scale taken from **d** specified by the dashed white line.

contact to the Pb. The resulting thin film layer sequence along two positions of the nanowire is sketched in cross-sectional views in Fig. 4.1 **b**. After growth electron beam lithography is used to define normal metal (Ti/Au) leads to the bare InAs nanowire and the Au/Pb film. To ensure good ohmic contacts we deploy Ar^+-ion milling immediately prior to metal evaporation. The measured device is shown in Fig. 4.1 **a**.

The device is mounted in a dilution refrigerator which operates at a base temperature of $T \sim 30$ mK. The differential conductance, g, is measured across the device using a voltage-bias setup. By tuning the gate-voltage, V_{G}, we deplete the carrier density in the bare InAs section between the normal metal contact and the superconducting Pb. This creates an effective barrier, or a finite Z-value to use the same language from Section 1.6. The tunnel junction setup is shown in Fig. 4.1 **c** (top). By sweeping the source-drain bias, V_{SD}, we can modify the chemical potential and control the energy of the electrons

impinging on the interface and tunnel into the superconductor. Above the superconducting gap $|E| > \Delta^{\mathrm{Pb}}$ electrons are predominantly normal reflected or transmitted into the continuum of available state in the superconductor. For $|E| < \Delta^{\mathrm{Pb}}$ electrons are mostly Andreev reflected and quasiparticle transport across the interface is dominated by Cooper pairs. We sketch this process in Fig. 4.1 **c** (bottom). This setup now allows us to probe the density of states of the superconductor as the differential conductance is proportional to the density of states of the system in the tunneling limit.

In Fig. 4.1 **d** we show g as a function of V_{G} and V_{SD}. Here we observe strongly suppressed differential conductance between $V_{\mathrm{SD}} = \pm 1.25$ mV corresponding to a superconducting pairing energy of the Pb of $\Delta^{\mathrm{Pb}} = 1.25$ meV. Outside the gap diamond shaped structures suggest the presence of parasitic quantum dots.

The differential conductance normalized to the normal state conductance ($g_{\mathrm{N}} = g|_{\mathrm{V_{SD}=2mV}}$) is plotted in Fig. 4.1 **e** showing a suppression of the differential conductance inside the gap by a factor 100. This is comparable to state of the art superconductor-nanowire hybrids based on Al, Sn and Ta[9, 64, 38, 88]. In relation to the BTK model (Sec. 1.6) these data likely correspond to probing the superconducting density of states across a large effective barrier of strength $Z \gg 1$. The novelty of this section is ascribed to the demonstration of superconductivity in the InAs/Pb/Au nanowire device.

Andreev bound states

Here we give an example of Andreev bound states emerging in the same device. As described in Section 1.7 quantized states can emerge at an NS or SNS interface and their energy can be inferred from in-gap states by applying a bias voltage across the interface. The gate settings applied to the device are specified in Fig. 4.2 **a**.

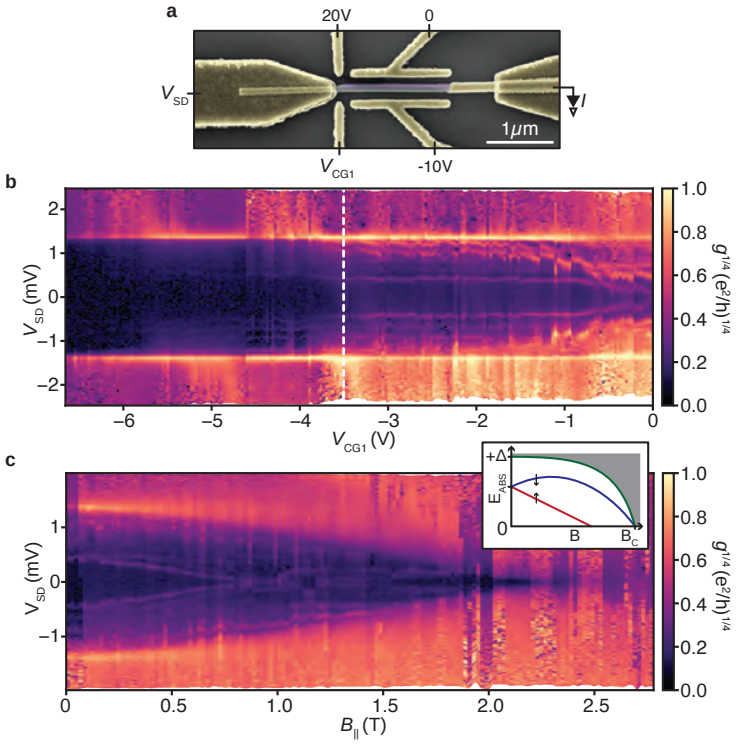

Figure 4.2: **Bound states in magnetic field. a**, False-coloured SEM image of device, with gate-settings noted. **b**, Bias spectroscopy using the junction gate, V_{CG1}. **c**, Differential conductance as a function of source-drain bias and parallel magnetic field at the gate voltage indicated by the white dashed line in **b**. Inset: In-gap states affected by level repulsion with the continuum.

From the bias spectrum shown in Fig. 4.2 **b** we observe a series of in-gap states located originating from repeated Andreev reflection whose symmetry around zero energy arise from the particle/hole symmetry. As the junction gate, V_{CG1}, is swept the states move in energy as their boundary conditions are influenced, although the effect is quite subtle. The subtleness could stem

from either weak gate coupling or repeating switches in the device creating local repetitions of the same gate sweep. Close to $V_{\mathrm{CG1}} = 0$, however, the slope of the bound state with lowest energy is quite pronounced indicating a finite gate coupling strength.

In Fig. 4.2 **c** the states are evolved in a parallel magnetic field, $B_{\parallel}$, at the gate-configuration specified by the white dashed line seen in panel **b**. As the field is increased we observe that the lowest energy state splits and moves as they host both spin-species. The weak magnetic field dependence of the spin-species moving towards the coherence peaks is attributed to the level repulsion effect from the continuum.[89, 90, 91, 92] We sketch the level repulsion from the continuum in the inset of Fig. 4.2 **c**. In contrast to the spin-down states, the energy of the spin-up states is decreased retaining a larger g-factor while merging at and oscillating around $V_{\mathrm{SD}} = 0$. The behavior of the higher order states is too complex to discern for certain, but seem to follow similar trends, albeit for the oscillating behavior around $E = 0$. We acknowledge that the intensity and trends of these peaks are weak and that a close inspection might be required to identify the described trends. Similar effects have been observed in a multitude of Al-based devices.[9, 64, 46]

Yu-Shiba-Rusinov states

An interesting case of Andreev bound states is known as *Yu-Shiba-Rusinov* states. In contrast to the picture described above, we now probe the density of states of the hybrid nanowire through a quantum dot with a finite charging energy, U.

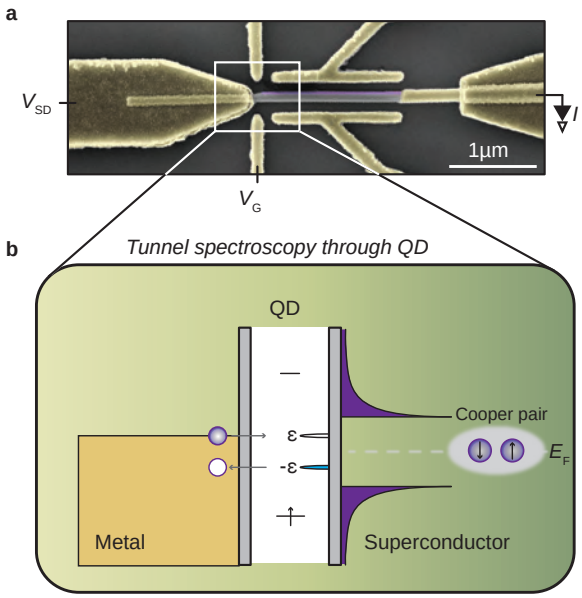

Figure 4.3: **InAs/Pb/Au tunnel junction device with a quantum dot.** **a**, False-coloured SEM image of the device. The setup consists of source-drain bias, V_{SD}, measured current, I, where the gate voltage is controlled by sweeping the back-gate. V_{BG}. **b**, Energy-space diagram of the *normal metal-quantum dot-superconductor* configuration.

As quantum devices are tuned with electrostatic gates non-homogeneous field lines might create local potential wells resulting in formation of quantum dots[93] especially for InAs nanowires with electrons accumulating at the surface.[94, 95] The device is shown in Fig. 4.3 **a** which is the same as above. This setup allows us to study unpaired spins (a spin-doublet) in close proximity to a superconductor as seen in Fig. 4.3 **b**.

Considering first the quantum dot in the junction. In Fig. 4.4 **a** we show a schematic of the bias spectroscopy signature (Coulomb diamonds) of an archetypal quantum dot. Inside the diamonds current is suppressed (white) and outside a finite current flows (magenta). We do not include excited states

in this picture. At the gate-voltage values where the Coulomb diamonds touch, two charge states become degenerate (e.g. n and $n+1$) and a finite current is observed at zero bias. We plot the pairing energy as horizontal black lines to visualize $U > \Delta$. Keeping this schematic in mind, we move to the phase diagram shown in Fig. 4.4 **b**. We plot the coupling of the quantum dot to the superconductor Γ in units of the charging energy $U = \frac{e^2}{2C}$.[96]

First we examine the case of weak coupling where $\Gamma/U \ll 1$ and an odd number of electrons on the dot. Here the groundstate is the single spin doublet illustrated by the blue part of the phase diagram. The spin is isolated enough from the superconductor to avoid any screening effects.

Now we increase the coupling to the superconductor ($\Gamma/U \sim 1$) and the

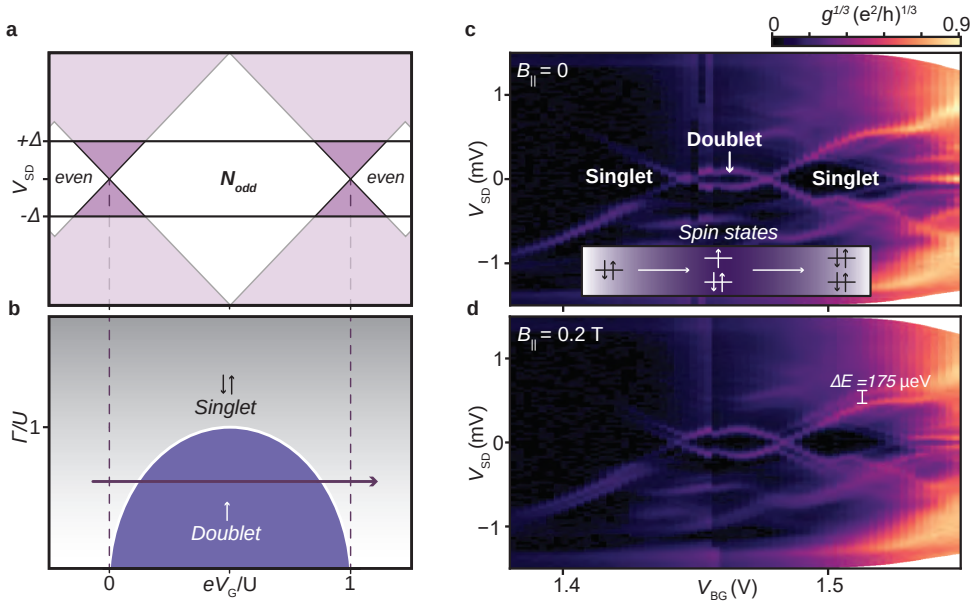

Figure 4.4: **InAs/Pb/Au tunnel junction device with a quantum dot.** **a**, Typical differential conductance transport features of a quantum dot. White indicates blockaded current and magenta indicates flowing current. Opaque overlay represents the quasiparticle continuum with a gap of Δ. **b**, Sketched phase-diagram of the singlet and doublet states plotted for normalized gate voltage and superconductor/quantum dot coupling, Γ. **c-d**, Colour-map of g versus V_{SD} and V_{BG} at $B = 0$ and $B_{\parallel} = 0.2$ T. *Inset*: spin-occupancy of the quantum dot coupled to the superconductor. The white arrows in **d** highlight the splitting.

system undergoes a phase transition (blue → grey). Here the single spin doublet is partially screened by the quasiparticles in the superconductor. Or said differently, the spin doublet is paired with quasiparticles from the superconductor transitioning it from a doublet to a singlet.

In Fig. 4.4 **c-d** we plot the differential conductance versus bias voltage and backgate voltage at $B = 0$ and $B_{\parallel} = 0.2$ T. The lines occuring below the gap arise from Andreev reflections at chemical potentials that correspond to the energy difference between the ground state and excited state of the dot, making them appear symmetrically around $V_{\mathrm{SD}} = 0$. As we modulate V_{BG} the parity of the dot is changed resulting in the characteristic 'eye'-shape of the *singlet-doublet-singlet* transitions. This transition is illustrated by the horizontal black arrow on the phase-diagram. At finite magnetic field ($B =$ 200 mT) we observe a splitting of the spin up and spin down of the degenerate doublet excited states. Assuming that a shift in Zeeman energy of $\Delta E_Z = 175$ μeV arises from the applied magnetic field we can extract the g-factor from the Zeeman relation, $E_Z = g\mu_B B$, were μ_B is the Bohr magneton, g is the Landé g-factor and B is the applied magnetic field. We obtain $g = 15$, which is comparable to g-factors obtained from similar measurements in InAs/Al hybrid devices.[97]

4.2 Additional data from InAs/Pb island devices

In the subsequent section we shift gears from shadowed tunneling devices to etched island devices. The following data is a bi-product of the island studies carried out as a part of Chapter 3. See the methods section of Chapter 3 and the supporting information of Ref.[31] for fabrication details.

An immense effort has been put into research on the magnetic field dependence of the Coulomb resonance peak spacing[56, 59, 57, 64, 47, 60], as this gives insight into the existence of bound states in the hybrid semiconductor/superconductor system. The origin of these states can be explained by trivial bound states arising at the interface, states arising from coupling to a spin-impurity or topological zero modes. Motivated by the desire to show the diversity of states in a InAs/Pb hybrid system we investigate the field evolution of the peak-spacing in the following.

Exploring ground state evolutions in magnetic field

We investigate three different types of ground state transitions induced by a magnetic field in a hybrid InAs/Pb island (Fig. 4.5). For all scenarios we sketch a slowly decreasing superconducting pairing energy for increasing parallel magnetic fields. Within $\pm\Delta$ we consider a single subgap state sitting at the lowest energy, $\pm E_0$. At $B_\parallel = 0$ the state is spin-degenerate and splits for increasing fields as the energy of the two spin species is modulated. In panel **a** we show the *first case*, where E_0 decreases only slightly over the range of applied field such that it remains larger than the charging energy, $E_0 > E_C$, for all field values. This is sketched according to panel **b**, where we present the ground state energies versus island charge number, $N_\mathbf{G}$. Here, the odd-charged ground state (red parabola) energy decreases, but never crosses E_C, ensuring that the odd charge state does not contribute in low energy transport. Panel **c** shows zero-bias conductance plotted for gate-voltage and parallel magnetic field recorded for the InAs/Pb island device. For the full range of measured magnetic field the number of Coulomb resonance remain constant indicating that no ground state parity change has occurred. The data is an excerpt from a larger data set where other gate-voltage regions showed peak-splitting within $B_\parallel < 3$ T confirming that the peak spacing in the shown region corresponds to

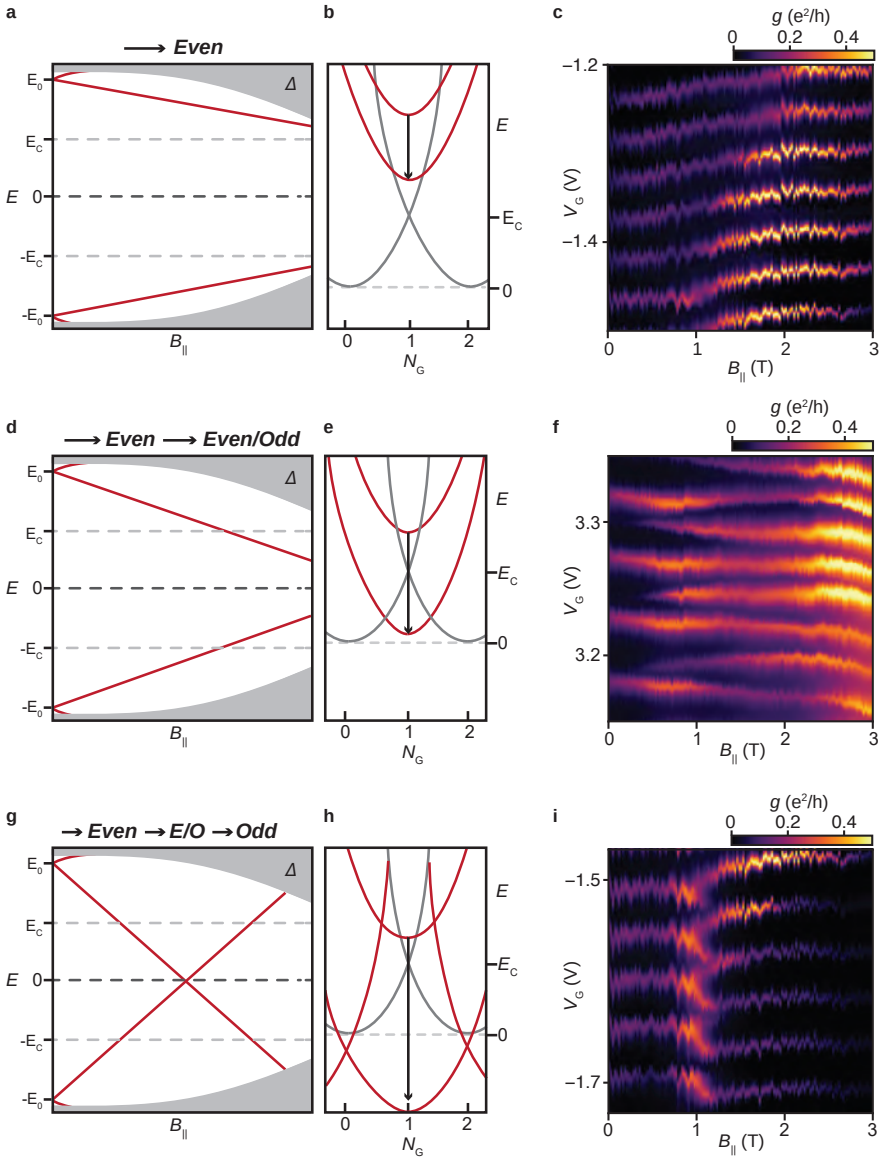

Figure 4.5: **Different ground state transitions in InAs/Pb islands. a, d, g**, Energy spectrum as a function of parallel magnetic field. E_0, subgap energy; E_C, charging energy; Δ, superconducting pairing energy. **b, e, h**, Energy spectrum plotted for electron occupancy normalized to gate voltage. **c, f, i**, Zero bias conductance as a function of gate voltage and parallel magnetic field showing three different ground state transitions for the same magnetic field range.

transport resulting only from degeneracy between even-charged ground states.

In Fig. 4.5 **d** we sketch the *second case*. Here E_0 is decreased to a moderate degree and evolves from $E_0 > E_C \rightarrow 0 < E_0 < E_C$. As E_0 is brought below E_C the odd-charged ground state passes E_C resulting in added degeneracy points between both ground state types, as illustrated in panel **e**. We provide the low-energy transport data in panel **f**, where we observe alternating smaller/larger peak spacings for increasing parallel fields. The small valleys correspond to odd parity and the big valleys corresponds to even parity for $E_0 > 0$. The peak intensity fluctuation are not well-understood, but could be related to bound states residing at different energies at the junctions suppressing conductance.[98]

The *third case* is sketched in Fig. 4.5 **g**. In this example as the field is increased E_0 is reduced first crossing E_C providing degeneracy points between both the even and odd ground states. Increasing the field further provides a scenario where the subgap state briefly resides at zero energy ($E_0 = 0$) resembling the non-superconducting single-electron transistor-case where all ground states are equal energy. At even larger fields the subgap energy becomes negative switching the valley parity (even $\rightarrow$ odd and odd $\rightarrow$ even), before the subgap state energy eventually becomes smaller than $-E_C$ providing degeneracy points now only between the odd-charged ground states. This sequence of events is illustrated in Fig. 4.5 **h**. In panel **i** we show the low energy transport where the Coulomb peak spacing shifts from $2e$-spaced even parity transport into $1e$-spaced even/odd and eventually modulates into $2e$-spaced odd parity transport. This is the first report of $2e$-spaced Coulomb resonances stemming from degeneracy between odd-charged ground states in hybrid islands not based on Al.[59]

Peak space analysis

In the following we give an example of a more quantitative analysis of the evolution of the Coulomb resonances operated at large magnetic field values showing signs of zero modes. Further, we will quantitatively compare the evolution of the valley between the Coulomb resonances in field between the parallel and perpendicular orientation.

In Fig. 4.6 **a** we show the raw data of a zero-bias conductance measurement recorded as a function of gate-voltage and parallel magnetic field of the InAs/Pb island device. During the initiating of the peak-splitting at $B \sim 1$ T we observe a pronounced reduction in the peak intensity lasting up to $B_{\parallel} \sim 5$ T, which is commonly observed in superconducting hybrid islands albeit at lower fields.[56, 59, 57, 64, 47, 60] The origin of the intensity drop likely arises from bound states residing at each tunnel junction residing at differing energies suppressing the conductance exponentially.[98] We overlay the data plotted in $\log_{10}$ of one of the resonances to provide further insight into the peak motion in the low intensity regions.

Each zero bias line trace is fitted with a function composed of several Gaussian functions on a constant background in order to precisely locate the peak position in gate space as seen in Fig. 4.6 **b**. The pronounced intensity difference observed during the onset of the peak splitting (see data plotted in $\log_{10}$ in **a**) prevents us from accurately determining the position of the fainter peak at $B_{\parallel} < 2$ T. In the remaining range we find all peak positions which are marked by blue circles, and use these to calculate the average peak spacing of the even ($S_{\mathrm{e,avg}}$) and odd ($S_{\mathrm{o,avg}}$) ground states. We show the magnetic field evolution of the average peak spacings of the even and odd ground states in Fig. 4.6 **c**. In the range from $B_{\parallel} = 2 \rightarrow 6$ T both flavours of peak spacing are modulated completing a full oscillation. We note that the oscillatory motion might continue for even larger fields, however, these data were not recorded.

The oscillatory motion in field indicates that the doubling of the Coulomb peak spacing arises from some other phenomenon than quasiparticle poisoning or superconductivity being quenched. For these effects a uniform $1e$-spacing is predicted.[99]

For panels **d-f** we repeat the exercise on the same set of Coulomb reso-

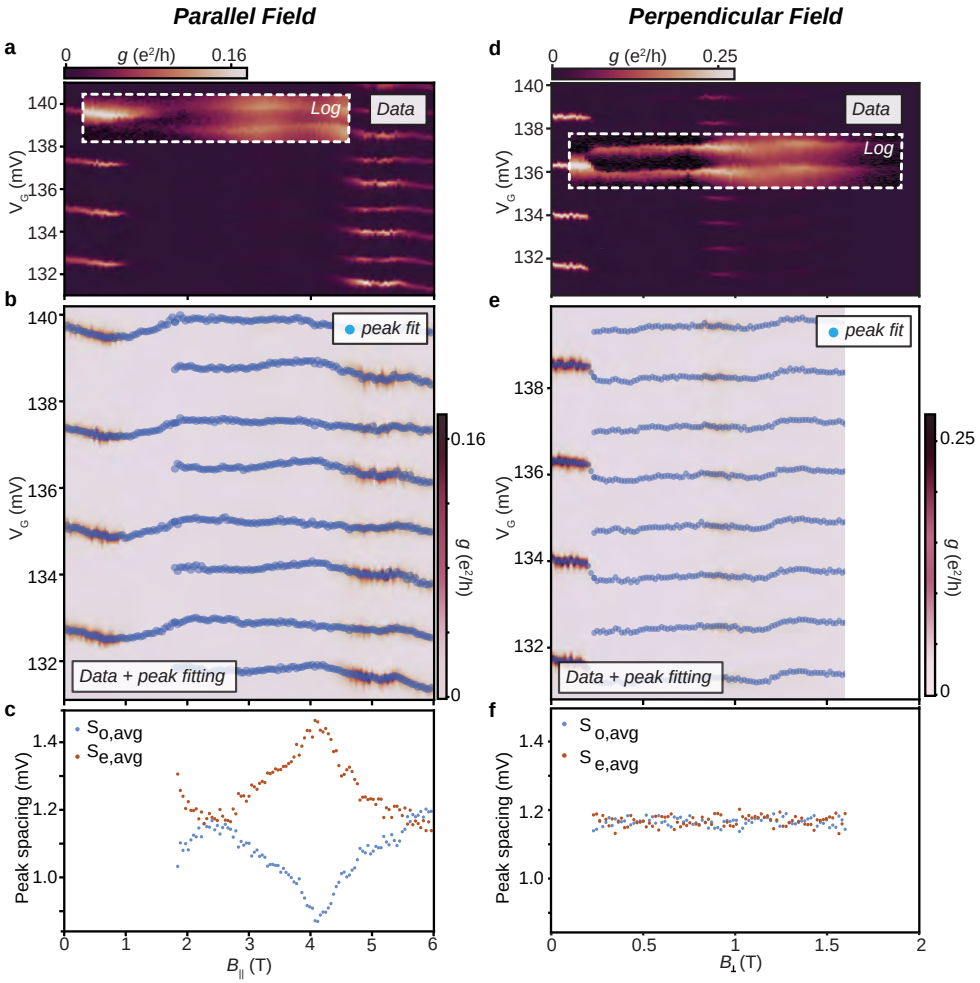

Figure 4.6: **Analysis of Coulomb resonance peak motion in magnetic field.** **a**, Zero-bias differential conductance recorded as a function of gate voltage and parallel magnetic field. *Inset*: Same data plotted in $\log_{10}$. **b**, Multiple Gaussian fit applied to the data seen in **a** to infer peak positions. Blue circle indicates the estimated peak position. **c**, Peak spacing calculated from the fit of the even and odd ground state versus parallel magnetic field. **d**, Zero-bias differential conductance recorded as a function of gate voltage and perpendicular magnetic field. *Inset*: Same data plotted in $\log_{10}$. **e**, Multiple Gaussian fit applied to the data seen in **a** to infer peak positions. Blue circle indicates the estimated peak position. **f**, Peak spacing calculated from the fit of the even and odd ground state versus perpendicular magnetic field.

nances (with a subtle shift in gate-space) for *perpendicular* magnetic fields. In this field orientation the splitting of the $2e$-spaced Coulomb resonances occurs at significantly lower values ($B_{\perp} \sim 220$ mT) and we observe the same pronounced intensity drop at initiation of the splitting. For this data set the fitting procedure works for the whole recorded range likely due to overall larger conductance intensities. In the same manner as before, we calculate the even/odd peak spacings from the Gaussian fits and plot these versus perpendicular field. In contrast, we observe no modulation of the peak spacing as perpendicular field is increased. The constant $1e$-spacing can arise either from superconductivity being quenched or bound state coalescing at zero energy.[65, 59, 97].

Charging energy versus pairing energy

The charging energy of the island can be modified by device design and gate voltage, whereas the pairing energy can be modified by magnetic field. In the following three distinct scenarios, namely, (**a**) $E_C < \Delta$, (**b**) $E_C \approx \Delta$ and (**c**) $E_C > \Delta$, will be presented.

In the first case (Fig. 4.7 **a**, top panel) we see an even numbered ground state at any given n_G when $B = 0$. As $\Delta > E_C$ the even ground state energies are degenerate at odd-integer values of n_G, here indicated by the black circles. As previously discussed this effect stems from the island charge changing continuously as $N \rightarrow N \pm 2$ as Cooper pairs traverse the island, which results in evenly spaced Coulomb resonances at $B = 0$ as seen in the bottom panel. As the magnetic field is increased the peak spacing stays constant until $B_{\parallel} \sim 900$ mT, after which we observe a splitting of the peaks. A significant measure of field is required to initiate peak splitting probably arising from a asymmetric ratio of Δ versus E_C in favor of Δ.

The second case (Fig. 4.7 **a** top panel) can be difficult to distinguish from the previous, as E_C and the odd ground state energy (likely) reside at similar energies. We observe evenly $2e$-spaced Coulomb resonances for any given n_G when $B = 0$, as seen in the bottom panel. However, we find that the peaks

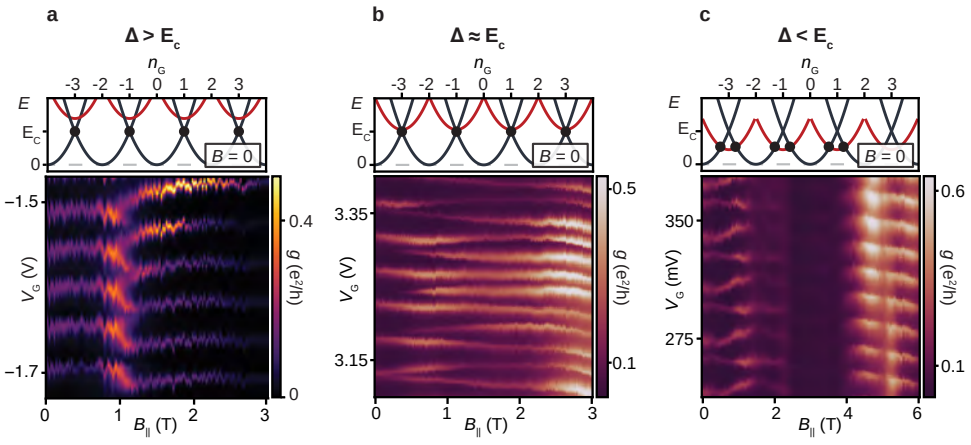

Figure 4.7: **Ground state evolution in magnetic fields.** Evolution of Coulomb resonances measured at zero zero bias in parallel magnetic field where (**a**) $\Delta > E_C$, (**b**) $\Delta \approx E_C$ and (**c**) $\Delta < E_C$.

split almost instantaneously evolving into an even/odd pattern when small parallel magnetic fields are applied.

In the last case (Fig. 4.7 **c**, top panel), where $E_C > \Delta$, the charging energy has been tuned such that the odd-numbered ground state becomes energetically available already at $B = 0$. In the corresponding data, we observe an even/odd pattern of zero bias Coulomb resonances evident at $B = 0$. As we ramp the field in the direction parallel to the nanowire, the peak positioning starts to move/oscillate until $B_{\parallel} \sim 4$ T when the spacing settles at a seemingly constant value.

In closing, we note that the complex behavior across all three examples might be confounded with trivial coupling to a semiconductor quantum dot, or that the gate dependence of the InAs/Pb hybridization modulates the effective g-factor affecting the field behavior as previously observed in Al-based devices.[97]

Partial conclusions

This chapter has presented a number of follow-up experiments carried out after the initial work described in Chapter 3 and should be viewed as a snapshot of the current state of Pb-based hybrid devices at our lab. A zoo of more complicated data did not make the cut as they were deemed too complex and hence non-essential. As a small side note, it should be mentioned that a significant amount of work has been devoted to measurements on *shadowed* Pb island (as opposed to the etched ones presented here), that failed to produce any convincing superconducting transport features. These data are also not shown.

Related to the findings from Chapter 3, we conclude that Pb-based hybrid devices behave similarly to their Al-based equivalents and surpasses these on a number of material dependent properties.[5, 9, 38, 63, 64] They exhibit:

- A large superconducting gap of $\Delta = 1.25$ meV.
- Large critical fields up to $B_{\mathrm{C},\parallel} > 8.5$ T.
- A large critical temperature of $T_{\mathrm{C}} \sim 7$ K.

These findings provide for a bright future perspective for Pb-based devices as they might allow for experimentation at parameter spaces not hitherto achievable. Further, they could provide a route to studying proximitized spin-orbit coupling as similarly done in graphene[80, 81] and ferromagnets.[82, 83]

However, as the lack of clearer data of this chapter perhaps suggests, Pb-based devices do come with some challenges. Here are a few remarks given as to why Pb-based devices might be complicated to work with. First, Pb oxide is unstable and can be removed simply by water.[31] This might simplify etching procedures as InAs nanowires are unperturbed by water, but makes storing and fabrication of devices cumbersome as atmospheric air contains trace amounts of water. The second remark concerns the superconducting coherence length of Pb which is on the order of 80 nm.[100] As the nanowires we use typically exhibit diameters of about 100-150 nm, parts of the semiconductor nanowire hosting the Pb film will be left un-proximitized. This could perhaps result in a parallel channel running along the device hosting normal

state conductance which in turn could complicate the understanding of the recorded data.

The possible parallel channels in InAs/Pb could be avoided by growing nanowires with diameters smaller than 80 nm ensuring that the proximity effects covers the entire width of the structure. Additional explorations could investigate the use of Sb-rich semiconductors as their surface band bending is away from vacuum[101] as opposed towards vacuum for InAs[101, 102]. This would would make the nanostructure less sensitive to any surface perturbations and further mitigate any possible parallel conduction channels as transport will be limited predominantly to the core. Additional suggestions on how to improve InAs/Pb hybrid devices are presented in Chapter 7.

Comparing both types of devices, a large advantage of the Al-based hybrids is probably owed to the self-terminating oxide engulfing the thin film providing protection during device fabrication. An additional benefit could probably be ascribed to the superconducting coherence length of Al being on the order of 1.6 µm.[100] This ensures that all parts of the Al-based hybrid nanowires are proximitized and eliminates any potential parallel normal state conductance. Hence, for InAs/Pb hybrid devices to seriously challenge the state-of-the-art Al-based devices, a sizeable effort in terms of material optimization, device performance and research efforts needs to be devoted in the future.

CHAPTER 5

SCALABLE PLATFORM FOR NANOCRYSTAL-BASED QUANTUM ELECTRONICS

J. E. Sestoft*, A. N. Gejl*, T. Kanne*, R. D. Schlosser, D. Ross, D. Kjær, K. Grove-Rasmussen, and J. Nygård, 2022. *'Scalable Platform for Nanocrystal-based Quantum Electronics'.*
Advanced Functional Materials, 2112941.

Unlocking the full potential of nanocrystals in electronic devices requires scalable and deterministic manufacturing techniques. A platform offering compelling paths to scalable production is microtomy, the technique of cutting thin lamellas with large areas containing embedded nanostructures. This platform has so far not been used for fabrication of electronic quantum devices. Here, we combine microtomy with vapor-liquid-solid growth of III/V nanowires to create a scalable platform that can deterministically transfer large arrays of single and fused nanocrystals — offering single unit control and free choice of target substrate. We fabricate electronic devices on cross-sectioned InAs nanowires with good yield and demonstrate their ability to exhibit quantum phenomena such as conductance quantization, single electron charging, and wave interference. Finally, it is devised how the platform can host rationally designed semiconductor/superconductor networks relevant for emerging quantum technologies.

Contributions: The idea was developed between myself, Thomas Kanne, Aske N. Gejl, Kasper Grove-Rasmussen and Jesper Nygård. Thomas Kanne was responsible for growth of the materials. Daniel Kjær and Daniel Ross operated the microtome and recorded the TEM and AFM images. I fabricated the devices and performed the measurements with assistance from Aske N. Gejl and Rasmus D. Schlosser. The manuscript was written by me with inputs from all authors.

5.1 Introduction

Processing of nanocrystals (NCs) in scalable and deterministic ways is critical for their use in research fields ranging from new types of transistors[103, 104, 105] to biosensors,[106, 104, 107] optoelectronics[104, 108, 109, 110] and modern quantum devices.[6, 111, 112]

Generally, there are two approaches to scalable processing of NCs. One route is substrate dependent; here the NCs are either grown or etched from specific substrates, which also support later fabrication steps (e.g. circuit manufacturing). The second method is predominantly transfer-based; here the NCs are first synthesized and then later transferred to a specialized substrate. The techniques favored for the substrate specific approaches are vapour-liquid-solid growth (VLS), metalorganic vapour-phase-epitaxy, selective area epitaxy, Stranski-Krastanov growth, anisotropic etching or flame transport synthesis[113, 114, 115, 116]. These techniques achieve excellent crystal quality and good control of position, but since devices are fabricated on the growth substrates, device performance can suffer from substrate-induced strain, substrate/NC dislocations, short-circuiting or sub-optimal conditions for heterostructure growth. Promising transfer-based approaches are Langmuir-Blodgett deposition,[117, 118] nanocombed deposition,[119] dry transfer printing[120] and capillary force assembly[121] which allow for high precision placement and good yield. However, they are often solution-based and depend on preparation of the target substrates which influences device architectures and inhibits tracking of individual units.

An alternative route seeking to combine the best of both approaches is nanoskiving - the technique of embedding materials in a resin and cutting

extremely thin samples by an ultramicrotome. Prior works have yielded several attractive and scalable nanostructures for use in optical and electrical applications.[122, 123] As an example, the fabrication of complex optically active nanostructures covering areas of several mm^2 has been demonstrated,[124] and also, nanoskiving was combined with etching of core-shell nanowires to form AlGaAs nanocylinders with tunable dimensions for optical devices.[125] Nevertheless, nanostructures produced by nanoskiving have not been implemented into quantum electronics.

In this work, we present a flexible platform for transferring and positioning of arrays of high quality NCs and NC networks to almost any substrate - achieved by combining microtomy with VLS growth of III/V nanowires. We measure electronic NC devices operated as field effect transistors (FETs) and find excellent mobilities as expected for InAs-based transistors, as well as quantum transport signatures when devices are operated at cryogenic temperatures. We show how the platform can be extended to host complex networks and semiconductor/superconductor devices with the prospect to realize many new types of gate-tunable superconducting qubits.[6, 126, 127, 111] In addition, our invention may allow for alternative routes in research fields such as deterministic placement of quantum dots for realization of the Hubbard model,[128, 129] layering of optoelectronic structures/devices, foldable electronics, wireless single-electron logic controlled by electrical fields[130] and single photon sources based on III/V quantum dots.[131]

5.2 Scalable nanocrystal platform

In Figure 1 we show the principles of the scalable NC device platform. InAs nanowires are grown on (111)B InAs substrates by the VLS process where the position of the nanowires are controlled by placing Au catalyst particles via electron beam lithography (EBL). Following growth the substrate is cleaved into pieces that are compatible with the microtome setup and embedded in a resin. The resin block containing the positioned nanowires is detached from the growth substrate and is mounted and aligned in the microtome setup. This work flow is illustrated in Figure 1a. Using the microtome setup we cut thin (∼70-100 nm) slices of resin (lamellas), containing positioned NCs as seen

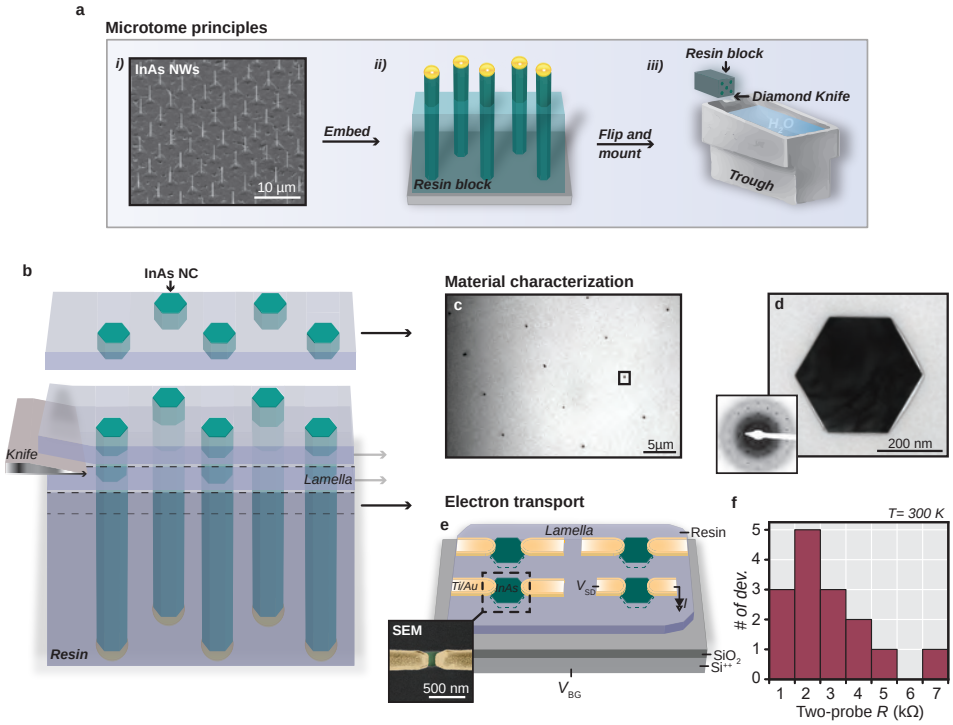

Figure 5.1: **Scalable nanocrystal platform.** a) Illustrated microtome principles. *i*) SEM image of array of as-grown InAs nanowires. *ii*) Array of nanowires after embedding. *iii*) The resin block containing nanowires mounted next to the knife/trough. b) Zoom in on (*iii*) showing how subsequently cut lamellas can be transferred to different substrates (e.g. a Si substrate and a TEM grid). c) Low-magnification TEM micrograph of array of NCs transferred to a TEM grid. Black box indicates a single NC in the array. d) TEM image of a single NC. Inset: SAED pattern showing the intact crystallinity of the transferred NC. e) Schematic showing a lamella transferred to a Si/SiO_2 substrate, where four transferred NCs are contacted. Inset: False-colored SEM image of a measured device. Green, InAs; Yellow, Ti/Au. f) Histogram of resistances (R) recorded on 15 conducting devices at $T = 300$ K.

schematically in Figure 1b. We find that the NCs typically extend ∼60 nm out from the lamella. The lamellas can be transferred to almost any type of substrate via the liquid medium in the trough (knifeboat). Figure 1c shows a bright-field (BF) transmission electron microscope (TEM) image of an array of NCs whose relative location is translated from the growth substrate to the TEM grid. A close-up TEM micrograph of an individual NC with a clear hexagonal morphology is seen in Figure 1d. The inset shows the selected area

electron diffraction (SAED) pattern where the regularly spaced spots indicate that the crystal remains intact after the sectioning/transfer process, and the grey rings correspond to the amorphous carbon grid. Additional information on the use of a ultramicrotome to create lamellas with arrays of NCs can be found in the Supporting Information, Section 1.

Following the initial transfer to a TEM grid, we transfer the subsequently cut lamella to a Si^{++}/SiO_2 substrate. The NCs in the lamella are contacted electrically using standard cleanroom fabrication techniques as seen schematically in Figure 1e, where an array of four NCs are contacted. Details on fabrication can be found in the Methods section. The NCs sit in plane with the lamella and the Ti/Au contacts are placed on top of the resin, resulting in the NCs being electrically accessed from the top cut facet. Since the resin is insulating the NCs are electrically isolated from each other and one can apply a voltage bias, V_{SD}, across the individual NCs and measure the current, I. The inset in Figure 1e shows a false-colored scanning electron microscope (SEM) image of one of the measured devices. In Figure 1f we show a histogram of the two-probe resistances of 15 working devices out of 17 measured at room temperature. The resistances are mostly similar in the few kΩ-regime showing that ohmic contacts can be reproducibly fabricated. Further analysis of the cut face quality and compression effects can be found in the Supporting Information, Section 2.

Concluding on this section, we expect the scalable NC platform to be easily extended to a large number of materials relevant for fabrication of quantum devices. Materials such as Si, GaAs, BiTe, Al, AlO_2, Cu and Au have already been investigated by commercial ultramicrotome manufacturers,[132] and highly relevant materials such as Al, Pb, Sn, As, In, Ga, Ge, Sb, Bi, SiO_2 among many others are either proven or predicted to be intact after microtoming.[123]

5.3 Nanocrystal FETs

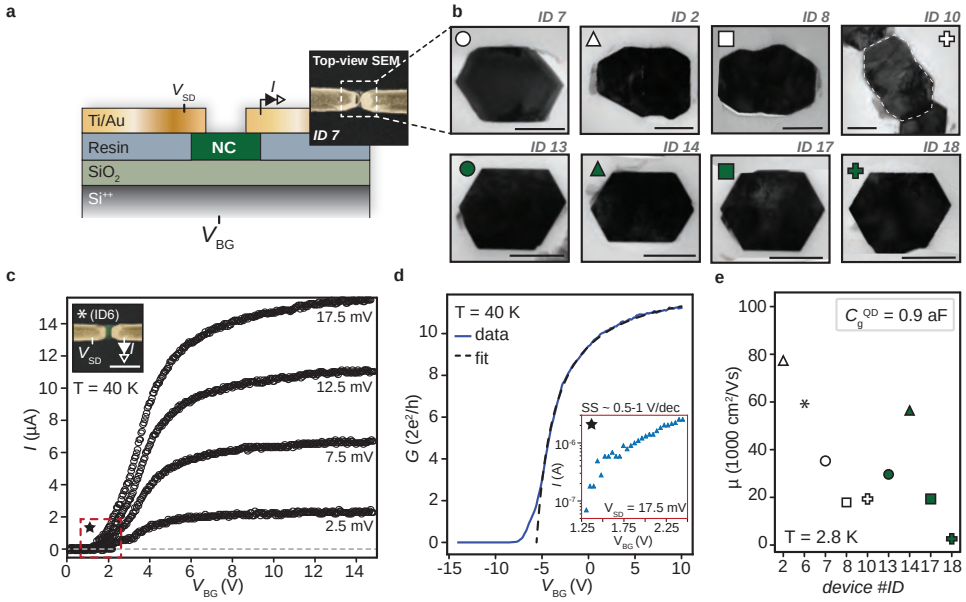

Figure 5.2: **Nanocrystal FET behavior.** a) Side-view illustration of a NC FET device. False-colored SEM image of a NC device. Yellow, Ti/Au contacts; green, NC; V_{SD}, the applied voltage bias; I, measured current; V_{BG}, backgate voltage shifting the chemical potential of the NC. b) TEM images of corresponding NCs from a lamella cut before the lamella used for fabrication of FETs. All scalebars are 200 nm. c) Current as a function of V_{BG} recorded at V_{SD} = 2.5, 7.5, 12.5, 17.5 mV. Corresponding device has ID 6. d) FET model (dashed line) fitted to the linear conductance (G) swept as a function of V_{BG} (blue). Inset: I plotted vs V_{BG} on a semi-logarithmic scale. Trace marked by a star in (c). d) Estimated FE mobilities for all gateable devices.

Having demonstrated the scalable device platform we explore the field effect behavior in a series of individual and merged InAs NCs. In Figure 2a we show a cross-section schematic of a single NC FET device with an inset showing a false-colored SEM image of one of the measured devices. At cryogenic temperatures 9 of the 15 devices were still conducting and exhibited a field effect response. In Figure 2b we show the TEM images of the NCs corresponding to the device-NCs of which transport data is presented. As an example, we show the SEM image of a device fabricated on a NC (ID7) and a TEM image of a NC from the same nanowire. We investigate both NCs sectioned

from single nanowires (ID6, 7, 13, 15, 17, 18), as well as devices that were fabricated on two or more merged NCs (ID2, 8, 10). One NC (ID6) is not shown due to unfortunate lamella placement on the TEM grid. The merged NCs were cut from nanowires that were deterministically grown together during a radial growth step as described in the final section. Details can be found in the Methods section and recently published work.[133] The hexagonal shapes of the single NCs appear somewhat irregular, which is an artifact from the close spacing of the single nanowires grown under unoptimized conditions. As inter-nanowire spacings decrease local growth parameters change due to temperature fluctuations and variations in shared collection areas.

In Figure 2c we show current measured as a function of backgate voltage, V_{BG}, at different bias voltages, V_{SD}, of a NC device (ID6) at low temperature, $T = 40$ K. We choose this temperature since most conductance resonances are averaged out by thermal effects as shown in Supporting Information, Section 3. By sweeping V_{BG} we modulate the number of carriers in the semiconductor and change the current flowing across the NC, bringing the device through three distinct regions. In the range V_{BG}= 0–2 V no current is running corresponding to an OFF state. From V_{BG} = 2–4 V the current increases linearly, while the current saturates above V_{BG} = 4 V. The saturation current increases linearly with V_{SD} implying that high quality ohmic contacts to the NCs have been fabricated, as expected from n-type InAs-based electronic devices.[134]

We now shift our focus towards the mobility of the NCs. The FET mobility is estimated using a commonly used expression for nanowire FETs[135]. Details on fitting are found in Supporting Information, Section 5. We apply this model to underline the overall FET behavior of NC devices. Figure 2d shows the linear conductance measured (G) as function of V_{BG} where the corresponding fit follows the behavior of the FET excellently until close to pinch-off. The inset shows a zoom-in on the subthreshold swing, SS, of the I/V_{BG} curve at V_{SD} = 17.5 mV from Figure 2c. Depending on the chosen range, the SS varies between ∼0.5-1 V/dec which is significantly lower than state-of-the-art nanowire FETs.[136, 137] This behavior may be explained by the extremely short distance between the contacts resulting in short channel effects which are known to reduce the SS in ultra short devices.[138] Additional hysteresis plots are shown in the Supporting Information, Section 4, and are

comparable to other types of nanowire-based FETs fabricated on Si^{++}/SiO_2 substrates.[135]

We have estimated the low temperature mobilities for all 9 NC FETs as seen in Figure 2e ($T = 2.8$ K). Output measurements and linear conductance traces with according fits are shown in the Supporting Information, Section 5. We observe no noticeable trend between the estimated mobilities obtained from NCs cut from a single nanowire or merged nanowires indicative of no significant barrier in the merged NCs. This may be explained by specific growth conditions causing the merged NCs to effectively act as a single crystal, hence suggesting that formation of larger networks based on current growth parameters is feasible. The estimated mobilities seem comparable to or larger than values found in SAG and VLS grown InAs and InSb nanowires,[135, 139] although they vary across the different devices. These variations may be attributed to variations in gate capacitance and small device dimensions. For one, large variances in effective gate-capacitance may produce different mobility estimations. In addition, the model accounts for diffusive transport whereas some device lengths are comparable to or smaller than the mean free path of InAs nanowires (∼150 nm).[140] Hence, we use the FET model mainly to highlight the predictable field effect behavior of the NC devices. We note that any unevenness in the hexagonal shape of some of the single NCs seen in Fig. 2b, stems from down-stream effects of nanowires grown in close proximity. As the inter-nanowire spacing is smaller than the mean diffusion length of the growth material the substrate adatom population will be uneven, resulting in adjacent nanowires having different adatom contributions and hence varied effective flux ratios. In particular, this can influence the growth dynamics in the axial nanowire growth phase resulting in local diameter variations. In summary, this section shows that the NC transfer platform can host ultra-small FET devices and that these behave predictably in electrostatic fields, which is a fundamental requirement for control of complex electronic quantum devices.

5.4 Quantum transport in single nanocrystals

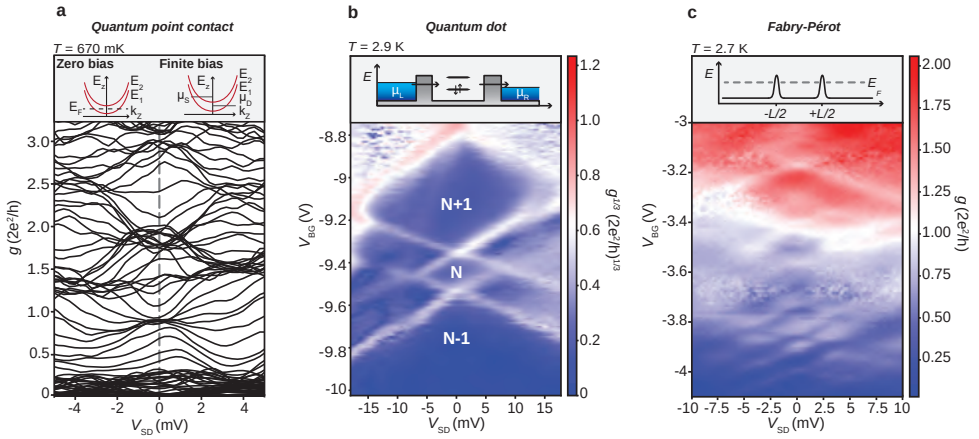

Figure 5.3: **Quantum behavior in nanocrystal devices.** a) Zero-field waterfall plot of differential conductance, g, as a function of V_{SD} and V_{BG} showing an approximate bunching of curves at (half) integer values of $2e^2/h$ at $V_{\mathrm{SD}} = 0$ ($|V_{\mathrm{SD}}| > 2$ mV). Inset: Zero-bias and finite bias band diagram of a one-dimensional quantum point contact. b) Color-plot of g versus V_{SD} and V_{BG} showing a series of Coulomb diamonds. The conductance is plotted in the third root to emphasize low values. Inset: Energy diagram of the quantum dot charging process. c) Colour-plot of g as a function of V_{SD} and V_{BG} showing Fabry-Pérot oscillations. Inset: Energy diagram with opaque barriers and position of Fermi energy, E_{F}.

A prerequisite for using the NC platform for quantum-based applications is the capability to hold quantized phenomena in single NCs. Here we show a series of quantum effects that emerge around liquid He temperatures in a set of devices based on single NCs.

We plot differential conductance, $g = dI/dV_{\mathrm{SD}}$, as function of V_{SD} and V_{BG} in a waterfall plot for device ID7 as seen in Figure 3a. As we sweep V_{BG} and V_{SD} we observe a bunching of the individual traces close to the first few units of twice the conductance quantum ($2G_0 = 2e^2/h$) around zero bias. At larger bias voltages ($|V_{\mathrm{SD}}| \sim 3$–4 mV) this bunching effect is no longer observed at integer values but instead at half-integer values. These effects are discussed based on the inset shown in Figure 3a where a schematic of the parabolic dispersion relation of the first few sub-bands in an ideal one-dimensional quantum point contact (QPC) is seen. This textbook example

assumes that the device length is much smaller than the mean free path ($l_{\mathrm{D}} \ll l_{\mathrm{mfp}}$), that the temperature of the system is smaller than the subband spacing ($k_{\mathrm{B}}T \ll E_2 - E_1$) and that the Fermi wavelength is comparable to the width of the constriction ($\lambda_{\mathrm{F}} \sim W$). Changing the Fermi level in the case with zero bias ($\mu_{\mathrm{L}} = \mu_{\mathrm{R}}$) will modulate the energetically accessible modes supported by the QPC in an integer fashion where right and left moving carriers are kept in equilibrium thus increasing conductance in steps of $2G_0$. Conversely, by applying an offset in the bias ($\mu_{\mathrm{L}} \neq \mu_{\mathrm{R}}$) another mode can now be accessed exclusively by e.g. left moving carriers resulting in an increase in conductance by only one G_0.

We find that the distance between the contacts (determined by SEM to $W < 100$ nm) is smaller than the experimentally determined mean free path in InAs nanowires ($l_{\mathrm{mfp}}^{\mathrm{InAs}} \sim 150$ nm[140]) and that the thermal energy of the system ($k_B T \sim 0.06$ meV) is much smaller than the estimated zero-field subband spacing ($E_2 - E_1$) of ∼3-5 meV. However, as the width of the NC-device is larger than the Fermi wavelength typically found in InAs nanowires ($\lambda_{\mathrm{F}}^{\mathrm{InAs}} \sim$ 20-30 nm[141]), the system is likely only quasi one-dimensional. We note that as we sweep V_{BG} the confinement potential of the electron path through the device may be changed. Hence by operating V_{BG} at negative voltages and taking into account screening from the leads a saddle-shaped confinement potential with a width that is comparable to $\lambda_{\mathrm{F}}^{\mathrm{InAs}}$ may be formed in the device. This behavior and the quality of data is comparable to measurements on quantum point contact-like devices based on InAs nanowires.[142, 140, 143, 144] A total of three devices show zero-bias traces with according behavior as seen in the Supporting Information, Section 6.

When operating at larger negative V_{BG} the device is brought into the tunneling regime, likely due to opposing fields from the contacts acting as barriers for low carrier densities.[93] In Figure 3b we show a color plot of g versus V_{SD} and V_{BG} obtained from device ID7 at $T = 2.9$ K. Here we observe diamond shaped conductance resonances with the dark blue regions inside the diamonds corresponding to transport being suppressed by Coulomb blockade. In the inset in Figure 3b we show an illustration of an energy diagram for a quantum dot (QD) tunnel-coupled to a source and a drain contact. When the chemical potential is modulated in the zero-bias case ($\mu_{\mathrm{L}} = \mu_{\mathrm{R}}$, not shown in

illustration) single quantum mechanical states in the QD are accessed as the charging energy (E_C) determined by the electrostatic force of the system is overcome. Applying a bias offset ($\mu_L \neq \mu_R$) to this model allows us to measure the addition energy (E_{add}) as the source and drain potentials are aligned with the energy of the quantum state where the conductance resonances are observed. From the shape of the diamonds we extract the charging energy, $E_C = 7.5$ meV, total capacitance, $C_{tot} = 22$ aF, gate capacitance, $C_g = 0.9$ aF and lever arm $\alpha_g = 0.03$. The quantum confinement energy is tentatively estimated to $\Delta \sim 12.5$ meV. These findings are similar to values found in literature for a variety of self-assembled and nanowire-based InAs quantum dots.[142, 145, 93, 146, 147] Quantum dot-like structures were also observed in device ID 6. Additional data on excited states are shown in Supporting Information, Section 7.

In Figure 3c we show conductance spectroscopy of device ID6 where a checker-board pattern on a background of conductance is seen. When electronic waves are backscattered from a set of opaque barriers (as seen in the inset in Figure 3c), likely residing at the NC/contact interface, resonant conductance features may appear as either the chemical potential or the potential landscape of the device is changed. This is analogous to the transmission/reflection of light waves in Fabry-Pérot cavities. By converting C_G extracted from Figure 3b into capacitance per unit length ($C_G^L = 6$ pF/m), and taking the spacing between the oscillations at zero bias, $\Delta V_{BG}^{FP} = 250$ mV, we can estimate the length of the Fabry-Pérot system to be $L = \frac{2e}{C_G^L \Delta V_{BG}^{FP}} \sim 215$ nm,[148] which is comparable to the width of the NC measured by SEM. As we sweep V_{BG} the finite conductance background is modulated and a large variation in ΔV_{BG}^{FP} is observed suggesting that the number of Fabry-Pérot modes present in the NC device changes. Similar behavior was observed in device ID2. These findings are comparable to electronic Fabry-Pérot interference found in nanowires[149, 93, 143] and nanotubes.[150, 151]

Concluding on Figure 3, we demonstrate the ability of the NC devices to hold three fundamental types of electronic quantum phenomena.

5.5 Networks and hybrid devices

Recently, controlled growth of merged superstructures of nanowires has been demonstrated,[133] as well as semiconductor/superconductor nanowire heterostructures composed of III/V materials and Sn, Pb, and Al, known as hybrid devices.[9, 35, 64, 38, 37, 88, 31] These emerging materials are in high demand as they are proposed to serve as a foundation for emerging quantum information technologies.[6, 111, 112] Here we show how to extend the presented NC platform to these new material combinations and complex device architectures.

In Figure 4a a schematic of a growth substrate is presented where the dashed lines indicate a coordinate system. By use of standard EBL processes, catalyst particles can be placed on the growth substrate in predetermined patterns, and when VLS growth is initiated nanowires are formed at the locations of the catalyst particles.[133] Given the conditions under standard VLS growth (see Methods for details) the nanowires grow predominantly in the vertical direction with respect to the InAs (111)B substrate, and only minimally in their radial directions $\{1\bar{1}00\}$. Controlling the design of the catalyst particle placement, this can result in extremely closely spaced single nanowires, as illustrated in the cross-section view in Figure 4a (*i*). From arrays of individual nanowires, one can merge nanowires along their growth directions in order to form networks (see Figure 4a (*ii*) for cross-section schematic) in two ways.

With the first approach, single nanowires are grown with a small separation ($\sim 50-160$ nm) from large volume seed particles. As the seed particle volume determines the width of the nanowires, this ensures that the nanowires are rigid. After reinitiating growth in a second growth step (see Methods) the nanowires grow predominantly in the radial directions. Depending on the placement of the single nanowires, we can merge two or more nanowires into networks, and control the extent of which they merge. In Figure 4a (*ii*) and Figure 4b, we show a cross-section schematic and an SEM image of an example of three nanowires merged during radial overgrowth, respectively.

With the second approach, nanowires are also grown with a small separation but from smaller volume seed particles, such that the resulting nanowires are thin. Local vibrations and van der Waals forces then make the nanowires

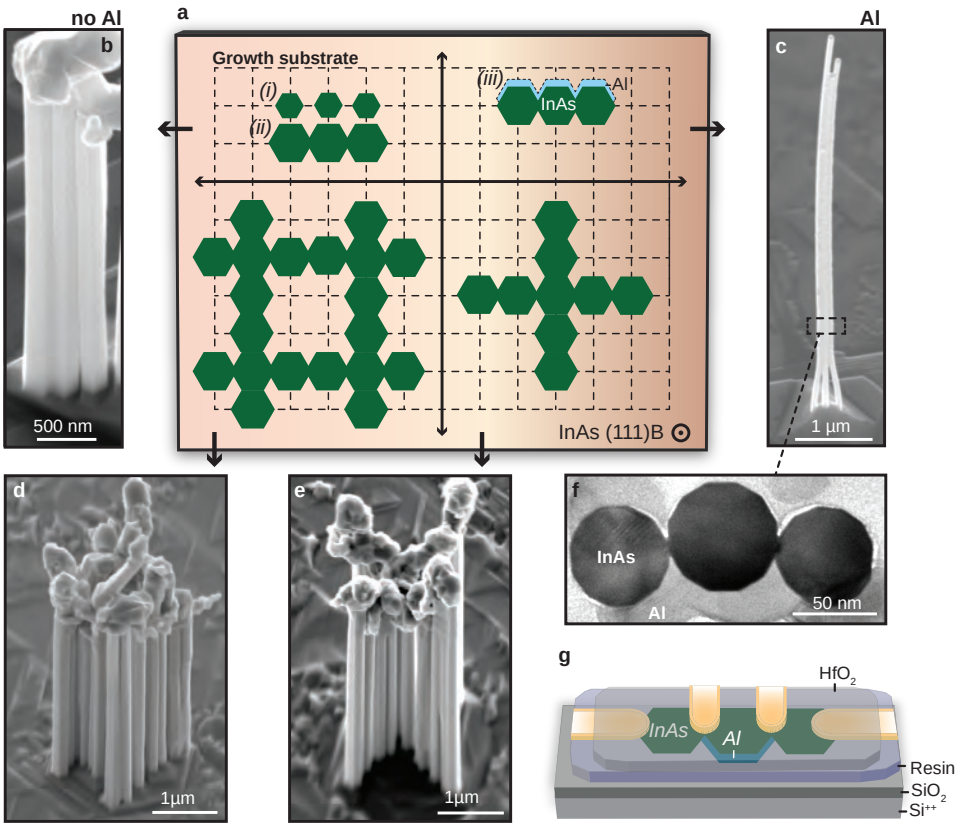

Figure 5.4: **Nanocrystal networks and superconductors.** a) Schematic of an imagined growth substrate coordinate system. Top-view placement of the green hexagons illustrate where InAs nanowires can be (over)grown in order to form complex NC networks. b,c) SEM images of three merged nanowires without and with epitaxially grown Al, respectively. d) SEM image showing a series of merged nanowires forming a loop-structure. e) SEM image of merged nanowires that form a cross. f) Cross-section view TEM image of three merged NCs with epitaxially grown Al. g) Illustration of a hybrid InAs/Al NC device suited for superconducting quantum electronics.

touch and stick during the first growth phase, and allow the small amount of radial growth still present during the VLS mechanism to merge the individual nanowires. We provide examples of this in the SEM and cross-section TEM image shown in Figure 4c and d.

After growth, these structures are embedded and sectioned as already described, creating networks of connected or disconnected semiconductor islands. Additionally, they can be grown with a superconductor (Al) as seen in the il-

lustration in Figure 4a (*iii*) and the TEM image in Figure 4f.

Based on the first scheme, we have designed and grown complex nanowire network structures as seen in Figure 4d and e. We highlight these particular structures as combinations of these after sectioning can form myriads of complex NC-based device structures, simply by controlling the placement of the seed particles. The erratic growth on the nanowire ends can be alleviated by optimization of growth parameters. In Figure 4g we showcase how the presented platform can be used to assemble a type of device (superconducting hybrid island) that has obtained widespread attention lately for research into Majorana physics in semiconductor/superconductor nanostructures.[6, 111, 112]

5.6 Conclusion and Outlook

We combine two well-established techniques – growth of nanowires and microtromy – to make a scalable platform for production of electronic quantum devices. The platform is generic in that it is not limited to VLS grown nanowires, but can be extended to other growth or etching-based techniques allowing the platform to use a broad range of materials. Based on the placement of catalyst particles and controlled crystal overgrowth, we show how this platform can be extended to NC networks of unprecedented shapes and be merged with semiconductor/superconductor technologies to build complex superconducting quantum devices. We expect the NC-transfer platform to be ideal for realizing large arrays of quantum dots with specifically tailored tunneling barriers. This is an interesting new route for quantum information technology and fundamental studies, such as development of lattice-based quantum simulators and wireless single-electron logic controlled by AC-fields.[128, 130]

During device fabrication, selected lamellas can be used as samples for quality control by e.g. AFM, TEM and SEM, which is expected this to become a desirable feature when transitioning technologies from prototype to high-throughput manufacturing.

Future work should investigate alignment optimization between the nanowire high symmetry crystal axes and the microtome knife cut plane to improve crystal cleaving and NC morphologies. In addition, different routes for improving transport signatures should be explored such as atomic layer deposition of

high-κ dielectric materials prior to microtoming, removal/change of the resin and in-situ deposited contacts. Additional routes not investigated here involve growth of radial heterostructure p-n NCs embedded in a transparent resin for production of optoelectronic devices. Additionally, stacking of multiple lamellas containing NCs with deliberately tuned p-n junctions could be used for high efficiency tandem solar cells. This principle could be further extended for extreme down-scaling inter-pixel pitch between RGB sub-units for ultra high resolution monitors.

In conclusion, this platform provides a new approach to nanoscaled device engineering with prospects for scalable fabrication and opens up new ways to integrate nanomaterials into emerging technologies within the fields of optics, optoelectronics, electronics and quantum devices.

5.7 Experimental details

Nanowire growth. A molecular beam epitaxy (MBE) system is used to grow Au-seeded wurtzite InAs nanowires along the [0001]B direction on InAs (111)B substrates using the vapour-liquid-solid mechanism. Arrays of Au catalyst particles are placed via standard EBL with particle radius r_{Au} = 20-120 nm and height h_{Au} = 10-50 nm. After substrate annealing at As overpressure at T = 500 C° for 5 min used to remove the native oxide of the substrate, predominantly vertical nanowire growth is initiated at growth temperatures ranging from T_{growth} = 445-450 C°. Axial nanowire growth is carried out for a duration of 10-120 min before a short break (5 min) is introduced and the As_4/As_2 ratio is increased.

After vertical nanowire growth is concluded, we switch to growth conditions favoring radial growth. First, we introduce a short pause (5 min) before the temperature of the growth substrate is lowered steadily to T_{growth} = 350 C° over about 15 min. After an additional pause (5 min) the nanowires are radially overgrown for 1-20 min depending on the desired amount of overgrowth and distance between Au particles. An exhaustive description can be found in recently published work.[133]

Microtomy. InAs growth substrates are cleaved into smaller pieces con-

taining the as-grown free standing nanowire arrays. The wafer pieces are placed into silicone molds with the growth substrate facing the bottom, such that the nanowires are orientated towards the mold opening. Next, the embedding solution is prepared using the SPURR Low-Viscosity resin applying the 'hard' epoxy recipe. Ten samples are created from mixing 4.10 g ERL 4221 (cycloaliphatic epoxide resin), 0.95 g diglycidyl ether of polypropylene glycol, 5.90 g nonenyl succinic anhydride and 0.10 g dimethylaminoethanol. The mold is then filled with the solution before it is baked for eight hours at 70°C to harden the resin. Now the growth substrate is removed from the sample using a razor blade leaving the nanowires embedded, before the block-face dimension is trimmed to accommodate our device blanks (∼250 x 250 μm). The trimmed samples are mounted in a Leica Ultracut UCT UltraMicrotome and sectioned with a DiATOME Ultra 45° diamond knife at a clearance angle of 6°. After sectioning the lamellas are floating on top of the fluid (ultra-pure water) contained by the knife boat. The desired substrate is partially submersed, the lamellas are guided to the desired location and the substrate withdrawn now containing the deposited lamellas. In our case lamellas were transferred to Si^{++}/SiO_2 substrates, glass slides and TEM grids.

Microscopy. TEM characterization of the NCs in the lamellas was performed using a 200 kV Philips-FEI CM20 large tilt TEM. The plane waves are aligned parallel to the [0001] zone axis of the NCs. High-resolution TEM images were obtained using a Jeol 300F microscope. SEM characterization of the substrates with as-grown nanowires were carried out with a Jeol 7800F SEM using acceleration voltages in the range of V_{acc} = 1-20 kV. A Raith Eline system was used to obtain SEM images of the deposited lamellas containing NCs and finished devices using acceleration voltage, V_{acc} = 10 kV. The cut-face quality of the NCs post-sectioning was inspected by AFM using a Bruker Dimension Icon PT AFM in PeakForce Tapping mode.

Device fabrication and measurement. All devices are fabricated on highly doped Si^{++} substrates covered by 200 nm of thermal oxide. Prior to device fabrication we use SEM to verify the position of the NC and that the morphology remained intact after microtoming. Metallic leads to the NCs

were fabricated by electron beam lithography. RF ion (Ar+) milling was performed in the metal deposition chamber prior to e-beam metal deposition of Ti and Au (5/∼200 nm) to create transparent ohmic contacts to the NCs. Standard low-frequency (<200 Hz) lock-in measurements where performed to measure differential conductance ($V_{\mathrm{exc}} \sim$ 5-20 μV). No data correction was performed on the electrical data.

Note: The supporting information providing many details not covered in the main article are presented in the appendix in Chapter 8.

CHAPTER 6

SHADOWED AND ETCHED SUPERCONDUCTOR-SEMICONDUCTOR JUNCTIONS IN AL/INAS NANOWIRES

J. E. Sestoft*, M. Marnauza*, D. Olsteins, T. Kanne, R. D. Schlosser, I. Chen, and J. Nygård, 2022. *'Shadowed and etched superconductor-semiconductor junctions in Al/InAs nanowires'*.

Manuscript in preparation.

Hybrid semiconductor-superconductor nanowires have recently become a staple in modern quantum devices. Integrating such nanowires into hybrid devices typically requires extensive post-growth processing which may affect device performance unfavorably. Here we present a technique for in-situ shadowing superconductors on nanowires and compare the structural and electronic properties of Al-junctions formed by shadowing versus etching. Based on high-resolution electron microscopy we find that typical etching procedures lead to atomic-scale surface roughening. This surface perturbation may lead to a reduction of the electron mobility as demonstrated in transport measurements. Further, we display advanced shadowing geometries aiding in the pursuit of bringing fabrication of hybrid devices entirely in-situ. Finally, we give examples of shadowed junctions exploited in various device geometries which exhibit high-quality quantum transport signatures.

Contributions: The shadowing technique was developed by Mikelis Marnauza, Dags Olsteins and Thomas Kanne. Growth substrates were prepared by Dags Olsteins. Electron microscopy was carried out by Mikelis Marnauza. Device fabrication and low temperature transport experiments were carried out by myself, Rasmus D. Schlosser and I-Ju Chen. The manuscript was written by myself and Thomas Kanne with inputs from all authors.

6.1 Introduction

Semiconductor-superconductor hybrid nanowires are a promising new fundamental unit in emerging research topics such as gate-tunable Josephson junctions in gatemon and Andreev qubits, and topological superconductivity.[5, 6, 7] Implementing these structures in devices typically requires extensive post-growth processing which may be detrimental to device performance. Generally, hybrid nanostructures are integrated into devices by removing parts of the superconductor by selective wet etching.[9, 152, 153, 154, 155, 156, 157, 158] Recent alternative approaches employ a technique of shadowing superconductors in-situ either by as-grown structures[36, 159, 37, 160] or by growing the nanostructures on a substrate with pre-defined shadow masks.[161, 39, 162] These studies provide enticing prospects for devices manufactured entirely in-situ, however, the quality of the semiconductor surface in relation to ex-situ shell removal and its effects on device performance is still unclear.

Here we investigate Al shell junctions formed on vapour-liquid-solid (VLS) grown InAs nanowires where one junction is formed by in-situ shadowing and the other via chemical etching. These structures are used to make a comparative analysis of the influence of shadowing versus etching structurally and electronically. By transmission electron microscopy (TEM) analysis we find that the Al etchant induces atomic scale roughening of the InAs nanowire surface. We compare the field effect mobility obtained from transistor devices with both shadowed and etched junctions and observe a factor of $\sim$2 reduction in carrier mobility across the etched junctions. Seeking to extend the toolbox of shadow junctions formed on VLS grown nanowires, we present new approaches to in-situ shadowing. By predetermining the size and position of the nanowire catalyst particle before growth we harness the shadowing

effect without any change to growth parameters or any extensive substrate etching.[35, 37] We find that the Al transition shape caused by the shadowing changes relative to the size of the terminating grain and has a weak dependence on the distance to the shadow mask. We discuss this phenomenon in relation to the two extremes - full thermodynamic equilibrium and kinetically limited processes. We propose these tendencies to be dependent on the binding energy of the shadowed material as a function of substrate temperature. Based on these considerations, the transition region of some materials such as Nb, Ta and V are proposed to be influenced by the shadowing distance whereas other materials such as Pb, Al and Sn are less dependent. These insights are highly relevant for shadowed heterostructure growths as they put forward limitations on the junction morphology if short and well-defined transitions are required. Following, we show a selection of more advanced in-situ grown heterostructures showing some of the next steps required to move towards full in-situ hybrid nanowire-based device engineering also enabling the utilization of superconductors with poor etching selectivity. Finally, we give two examples of shadowed nanowires in Josephson junctions and superconducting interference devices, showing stable and controlled transport signatures, providing further promise that in-situ shadowing is a viable scientific route when up-scaling of devices requires ever more reliable components.

6.2 In-situ shell shadowing

Wurtzite InAs nanowires are grown along the [0001]B direction with $\{1\bar{1}00\}$ facets on InAs (111)B substrates. The nanowires are catalyzed by electron beam lithography (EBL) defined Au particles and grown with conditions that ensure the nanowire dimensions to be highly dependent on the initial Au particle volume (see supplementary information section 1). In the simplest case, in-situ shadowing of subsequently deposited materials can be achieved by placing a large catalyst particle in front of a smaller one with respect to the deposition source (see Fig. 6.1(a)).

The inter-wire distance and volume is controlled by EBL techniques providing high control over both parameters. The size of the Au particles is tuned by a number of single electron beam shots (details in see supplementary sec-

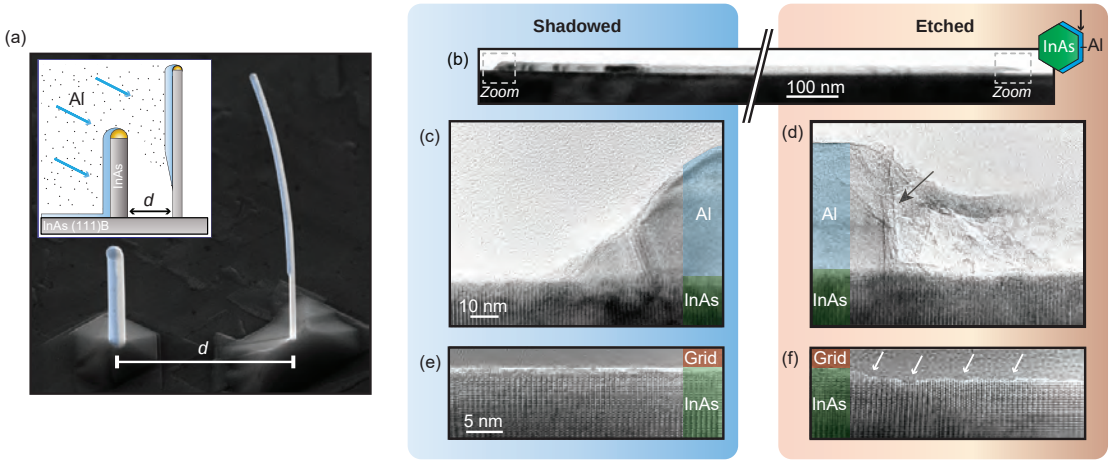

Figure 6.1: **In-situ shell shadowing scheme.** a) Schematic (inset) and SEM of a short and thick nanowire placed in front of a long and narrow nanowire. Interwire distance, $d = 2.5$ µm. (b) Low-magnification TEM micrograph InAs/Al nanowire with a shadowed (left) and etched (right) shell junction. (c-d) HR-TEM micrograph of the shadowed and etched Al junction. Shadow junction exhibits gradual thickness change in Al as opposed to a more step-like profile (indicated by the black arrow) obtained from etching. Oxide residues are visible close to the transition of the etched junction. Scale bar is the same for (c-d). (e-f) Zoom-in of the InAs nanowire surface on the shadowed and etched side of the nanowire. Background is partially colored to highlight the nanowire surface/vacuum interface. Atomic defects on the etched surface are indicated by white arrows. Scale bar is the same for (d-e). All the micrographs are obtained with the nanowire aligned to the $\langle 2\bar{1}\bar{1}0\rangle$ direction parallel to the nanowire facet.

tion 1 or related Ref.[163]). After initiating growth conditions (see methods for details) short and thick (3 m/210-250 nm) nanowires along with taller and thinner (6-7 m/85-100 nm) nanowires are grown from catalyst particle of differing volumes ($\sim 2.2 \cdot 10^5$ nm^3 and $\sim 1.1 \cdot 10^4$ nm^3). After nanowire growth is terminated the substrate is transferred to a metal deposition chamber without breaking vacuum. Here the substrate temperature is lowered to 120K by a liquid nitrogen cooled stage in order to minimize any adatom mobility. Next, the substrate is oriented with respect to the deposition source and a shadowed junction is formed during the subsequent metal evaporation. Details on this process and according yield ($> 90\%$) is presented in supplementary

section 1 and 2. The large diameter of the shadowing nanowire reduces possible misalignment between the nanowires caused by catalyst particle diffusion prior to growth or minor misalignment of the growth substrate with respect to the metal source. An outline of the geometrical limitations is provided in supplementary information section 3. We find that for our InAs/Al system an optimal interwire distance is < 0.5 µm at substrate temperatures of 120 K. In cases of larger interwire distances we observed Al grains on the front of the shadowed nanowire arising due to geometrical effects laid out in the supplementary information section 3.

We now attend to the structural comparison of Al junctions obtained by in-situ shadowing to those fabricated by etching. The chosen etchant is *Transene Al etchant type D* since it is highly selective towards Al on Si and As-rich compounds and is therefore a representative choice in regards to general semiconductor nanowire fabrication.[9, 153, 152, 154, 155]

Four shadowed nanowires were transferred from the growth substrate to a Si/SiO_2 substrate before the top of the nanowire was etched for 10 s with the etchant kept at 50°C. Hereafter the nanowires were picked up again using a micro-manipulator needle and placed on transmission electron microscopy compatible grids in order for a direct comparison between the etched and shadowed junctions on the same nanowires.

In Fig. 6.1 (b) a bright-field (BF) TEM micrograph of a typical InAs nanowire is shown with an Al junction formed by in-situ shadowing on the left and etching on the right side. High-resolution (HR) TEM micrographs of these regions recorded along the $\{2\bar{1}\bar{1}0\}$ direction are shown in Fig. 6.1 (c) and (d). On the junction formed by in-situ shadowing the Al remains highly ordered and crystalline throughout the transition without apparent defects with the Al transition generally trailing off smoothly with local grain dependent shape variations. On the etched side of the nanowire an abrupt transition (indicated by the black arrow) is observed, where the abruptness of the transition suggests that the etching rate is grain boundary dependent. In addition, we observe residues presumably originating from unetched and collapsed Al oxide likely caused from unequal etch rates of Al and Al oxide.

High-resolution micrographs of the nanowire surface proximal to the junctions are shown in Fig. 6.1 (e-f). The InAs surface remains pristine and

uniform on the shadowed part of the nanowire as opposed to the etched side. Here we observe atomic scale roughening along the length of the etched region (highlighted by the white arrows). We note that the magnitude of the roughening effect appears to small and hence might be beyond the resolution of standard scanning electron microscopy techniques (see supplementary information section 4). In the supplementary section 5 we show surface sensitive SEM micrographs of the etched region of nanowires placed on TEM grids and find that small beads of Al residues from the etching process remain on the nanowire. We note that other etchants not investigated in this work might provide less structural damage to the semiconductor and/or remove the remaining oxide completely. Nonetheless, this etching procedure is considered as state-of-the-art and is widely used fabrication method for quantum transport experiments based on in-situ Al on InAs nanowires. [9, 153, 152, 154, 155]

6.3 Comparing field effect mobilities

The low temperature mobility of a material is related to the mean free path of its carriers and is thus a metric for disorder. For nanowires the field effect mobility can be estimated from charge transport measurements using a field effect transistor geometry and is mainly governed by crystal defects[164, 165, 166] and surface roughness [167, 168]. In the following we investigate the field effect mobility in InAs/Al nanowire transistors composed of symmetric shadowed and etched shell junctions.

We show an SEM micrograph of one of the measured devices in Fig. 6.2 (a). The top of the nanowires are etched using the same recipe as described above whereas the bottom part with the shadowed junction is left pristine. After etching, standard EBL is used to place one contact on the center of the InAs/Al nanowire contacting the Al shell and two other contacts on the ends of the nanowire ensuring that the shadowed and etched junctions of bare InAs are of equal length. Across the devices, we vary the junction length, L, from 0.5 to 1 µm. A 12 nm HfO_2 gate oxide is grown by atomic layer deposition before defining the top-gate electrodes. These gates covered the entire bare nanowire segments. Figure 6.2 (b) shows the linear conductance measured as a function of gate voltage of the shadowed (blue trace) and etched (green trace)

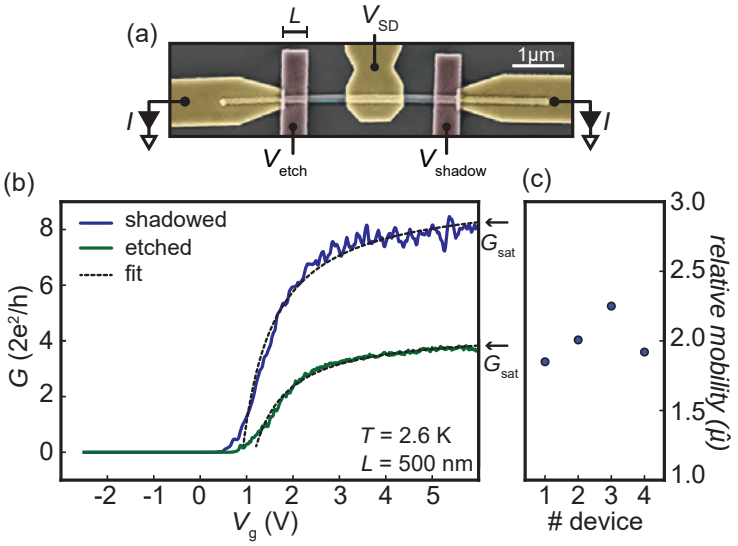

Figure 6.2: **Field effect mobilities for shadowed and etched InAs/Al nanowire transistors.** (a) SEM micrograph of a symmetric transistor device composed of an InAs/Al nanowire with a shadowed and etched Al junction. Yellow, Ti/Au contacts; Blue, Al; Grey, InAs; Pink, HfO_2/Ti/Au. Electrical setup is composed of source-drain bias, V_{SD}, measured current, I, and the gate voltage, $V_{g,shadow/etch}$. (b) Linear conductance as a function of gate voltage, V_g, for the shadowed (blue trace) and etched (green) part of device #3 measured at $T \sim 2.6$ K. We estimate the FET mobility from the fit (dashed black traces). (c) Relative mobilities, $\hat{\mu} = \mu_{shadow}/\mu_{etch}$, extracted from the gate traces performed on the shadowed and etched junctions plotted for four devices.

junction of device 3 (out of a total of 4 devices). All presented measurements are recorded at $T \sim 2.6$ K.

In order to extract the field effect mobility, μ, we fit a commonly used expression for nanowire field effect transistors to the conductance measured as a function of applied gate voltage, $G(V_G) = (R_S + \frac{L^2}{\mu \cdot C(V_G - V_{th})})^{-1}$.[169, 170] Here R_S is the series resistance, W is the width of the junction and C is the total capacitance of the nanowire, dielectric and gate electrode. In the supplementary information section 5 we provide details on the capacitance estimations, fitting and additional data on the other devices. We estimate field effect mobilities on the order of 2500-4500 cm^2/Vs for the etched junctions and 4500-10500 cm^2/Vs for the shadowed junctions. These values lie within comparable ranges of similar III/V nanowire transistors.[170, 139] We

observe a saturation conductance (G_{sat}) that is 3-6 times larger in the shadowed junctions compared to the etched junctions. This corresponds to a larger interface resistance on the etched junctions which is accounted for by R_{S} and is assumed to be independent of mobility.[170] By investigating representative samples of InAs/Al nanowires via high-resolution TEM we expect the junctions to be stacking-fault free and the mobility should therefore be mainly limited by surface roughness.

However, we emphasize that this way of extracting the field effect μ is dependent on the model, fitting approach and estimated capacitances and that we use it in this study mainly to find relative mobilities between the etched and shadowed junctions. In light of this we only compare the mobility of the etched and shadowed junction directly on the same device and plot this as $\hat{\mu} = \mu_{\mathrm{shadow}}/\mu_{\mathrm{etch}}$ in Fig. 6.2 (c) for all measured devices. Here we find that all devices show approximately a factor of two larger field effect mobility on the shadowed junctions compared to the etched junctions. These findings are consistent with the carriers in the shadowed junctions experiencing less disorder induced by surface scattering compared to etched junctions.

6.4 Al transition morphology

Evaporating materials from a finite source through a shadow mask produces regions of partial shadowing that resides between a non-shadowed and fully shadowed section. The morphology of the in-between region depends on the evaporated material, shadowing geometry and growth conditions. Typically two limits determine the overall shape of the junction morphology of as-deposited thin films, namely formation at thermodynamic equilibrium (Fig. 6.3(a)) and in the kinetically limited regime (Fig. 6.3(b)). The Al junctions formed by the shadow technique are examined using electron microscopy in order to investigate the post-growth Al shape and transition lengths as function of the distance to the shadowing-wire. Figure 6.3 (c-e) show BF-TEM micrographs of the film termination for shadows formed with interwire distance, $d_{1\text{-}3}$ = 0.5, 1.5 and 2.5 µm. The transition length L was measured between the region with constant Al thickness and the fully shadowed region as indicated by the white dashed lines. The measurement of L was performed

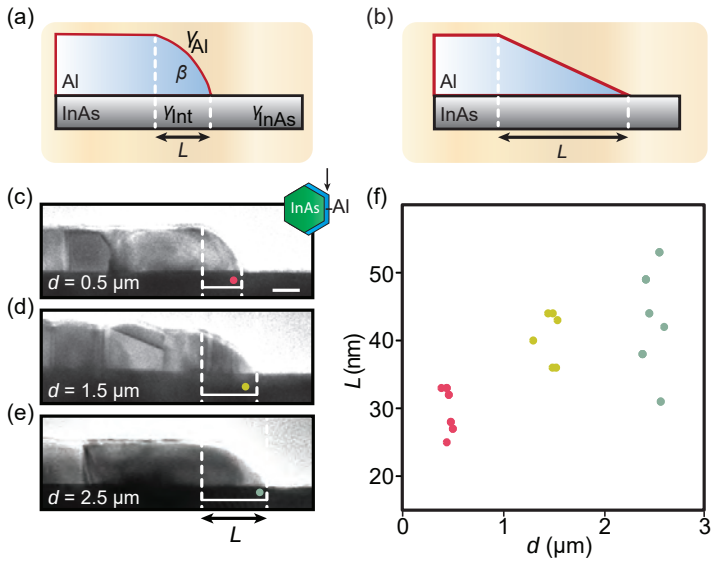

Figure 6.3: **Morphology of the shadowed Al transition.** Schematic of the shell junction morphology in thermodynamic equilibrium (a) and in the kinetically limited regime (b). The contact angle is denoted β, and γ_{Al}, γ_{InAs} and γ_{Int} corresponds to the surface energies of the Al, the InAs and their interface. (c-e) Low magnification TEM micrographs of three Al junctions with the viewing direction indicated by the black arrow in the inset in (c). The inter-nanowire distances are 0.5 µm in (c), 1.5 µm in (d) and 2.5 µm in (e). Scale bar is 20 nm for micrographs (c-e). Dashed lines indicate the transition length. (f) Al transition lengths for nanowires plotted versus inter-nanowire separation.

on 6 nanowires for each distance and plotted in Fig. 6.3 (f). Here we observe a slight increase in transition length as the interwire distance increases.

We relate this behavior to the two phenomenological scenarios accounting for the shadow geometry alongside different growth regimes. Materials with low binding energies relative to the substrate temperature, such as Al,[37] are expected to have a transition length and morphology primarily determined by the thermodynamic driving forces, Fig. 6.3 (a). In contrast, materials with larger binding energies, such as Nb,[161] will exhibit a transition morphology dependent mainly on the effective material flux, 6.3 (b). Large binding energies prevents the deposited material from migrating either due to kinetically limiting binding or because the activation energy for surface diffusion is too large. The weak dependence in the distance between the shadowing nanowires

for Al in our case may result from growth conditions residing in between the two extremes. The success of more complex in-situ shadow designs will likely rely on considerations of the shadow geometry and the specific material deposited.

6.5 Advanced geometries

Designs taking advantage of more advanced placements of catalyst particles, catalyst particle diameters and altered growth direction can be applied to design more complex in-situ grown hybrid wires and from these more complex quantum devices.[161, 159, 37, 160] Here we show-case additional examples of specialized hybrid nanowires.

If full-shell geometries are desired, we find that the nanowire positioning is precise enough for multi-directional depositions as shown in Fig. 6.4. Panel (a) shows a top-view sketch of a single thin and tall nanowire placed centrally of six surrounding thicker, lower nanowires. As indicated by the colored arrows, evaporating at six different angles enables the shadowing of shell depositions all around the central nanowire. We show an SEM image of this geometry after growth in panel (b). Extending on this approach, one could envisage depositing a series of different materials at different angles to create multi-layered structures in combination with shadow junctions.

In Fig. 6.4 (c-d) we discuss how the introduction of an altered growth direction can be deployed to create several gaps in the deposited material. In panel (c) we present a sketch of such a layout. In addition to the small and thick shadowing nanowire utilized above, we place a series of thinner, taller nanowires as depicted. After vertical nanowire growth is terminated a change in growth conditions is introduced making it favorable for the catalyst particle to be positioned on the facets of the nanowires. Reintroducing initial growth parameters continues nanowires growth now along one of the six side facets.[171, 36] This placement gives rise to shadows e.g. at a nanowire junction/kink (Fig. 6.4(d)) or along the nanowire (Fig. 6.4(d) inset). A limitation to this design is the random selection of the nanowire kinking direction as indicated in the schematic in Fig. 6.4 (c). Here only three of the six possible kinking directions are desired in this scheme (marked by red arrows) which

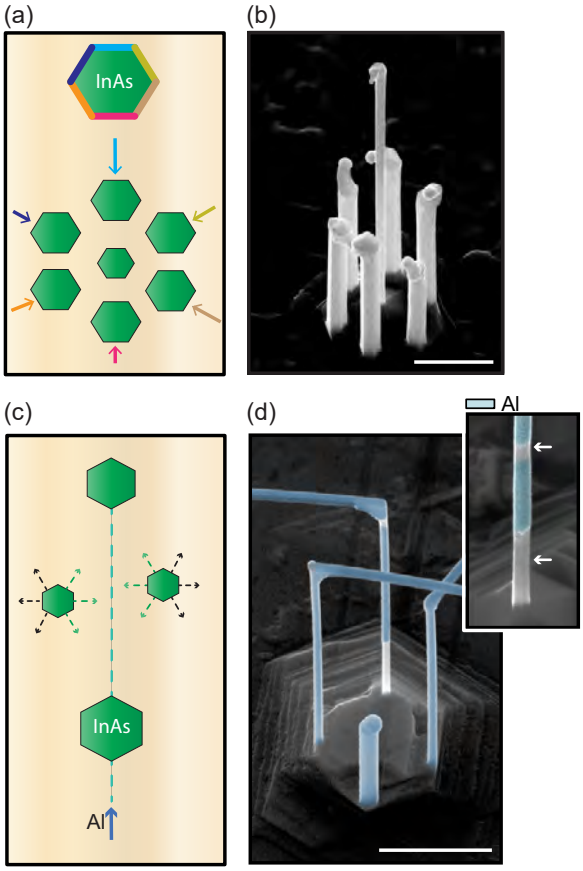

Figure 6.4: **Advanced in-situ shadowing geometries.** (a-d) Schematic of the nanowire positions on the growth substrate (left) and corresponding SEM image after growth (right). Green hexagons illustrate the nanowires and colored arrows indicate placement of the deposition source (a) and nanowire kinking directions (c). Inset in (d): Shadow junction placed along a nanowire stem. All scale bars are 1 µm.

may be surmounted by incorporating further kinking shadowing wires. In addition, one can may control the junction lengths by tuning the distance to the shadowed wire according to the trend displayed in Fig. 6.3.

6.6 Quantum transport in shadowed wires

In the following we give two examples of electronic quantum transport recorded in shadowed hybrid InAs/Al nanowires, both relying on the scheme shown in Fig. 6.4 (c-d). In Fig. 6.5 (a) a single nanowire is contacted by by two metallic leads (Ti/Au) and measured using voltage biased lock-in techniques (Fig. 6.5(a)). The junction length is approximately 100 nm, chosen from an array of shadowed nanowires with junction lengths on the order of ∼100-300 nm. In Fig. 6.5 (b) we plot the distribution of the junction lengths. The

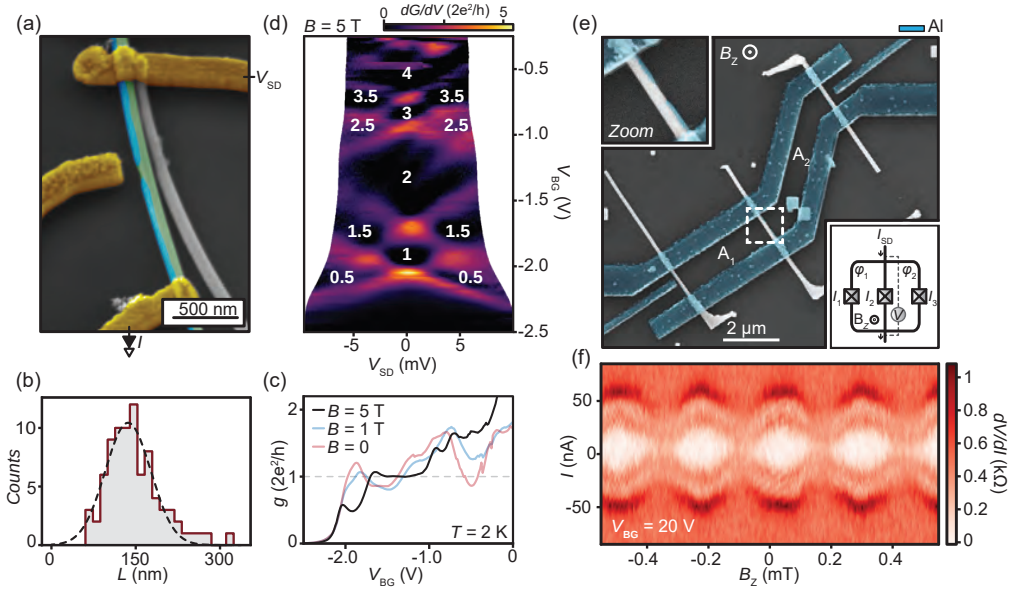

Figure 6.5: **Quantum transport in shadowed InAs/Al devices.** (a) False-colored electron micrograph of the measured device. Yellow, Ti/Au contacts; Blue, Al; Green, InAs. (b) Distribution of the junction lengths. (c) Linear conductance versus backgate voltage for $B = 0, 1$ and 5 T. Data is corrected for the series resistance. (d) Transconductance as a function of bias voltage and backgate voltage showing conductance quantization within the diamond shaped dark regions. The annotated values correspond to conductance values in units of e^2/h. (e) False-colored SEM micrograph of the measured triple junction interferometer device. Top inset: Zoom-in on the junction indicated by the white dashed square. Bottom inset: Schematic of the current-bias setup. (f) Differential resistance plotted as a function of perpendicular magnetic field and current showing critical current modulations.

right-skewedness of the distribution is attributed to the selected nanowires being grown from arrays favoring thicker shadowing nanowires which in turn produce longer junctions. The device is operated at $T = 2$ K, above the critical temperature of Al in order to suppress superconductivity so that the Al shell acts as an in-situ defined normal contact. In Fig. 6.5 (c) we plot linear conductance traces as a function of backgate voltage, V_{BG}. These traces are plotted in Fig. 6.5(c) for a series of magnetic fields, $B = 0$, 1 and 5 T. At $B = 5$ T we find well-defined conductance plateaus around 0.5, 1 and 1.5 $G_0 = 2\mathrm{e}^2/\mathrm{h}$, after subtracting the series resistance. At high magnetic fields, coherent backscattering is suppressed and conductance quantization is more pronounced than at zero field.

Remaining at large magnetic fields, we now turn to investigations of the sub-bands in the bare InAs junction. Fig. 6.5(d) shows the transconductance (dG/dV) as a function of bias voltage and backgate voltage. Here clear diamond-like patterns emerge when transconductance is suppressed indicating regions of conductance plateauing. Individual subbands are annotated in units of e^2/h and from these the sub-band energy spacing from the first to the second and the second to the third plateau is estimated to 5 meV and 10 meV, respectively. The transport behavior is highly stable and in accordance with behavior in ballistic conductance through a one-dimensional channel. Similar behavior has been observed in non-hybrid InAs nanowires of short junction lengths.[168, 167, 172]

The second device is comprised of three similar Josephson junctions (JJ) placed in a superconducting interferometer geometry (SQUID). Each of the three nanowires are picked up using a micromanipulator needle and placed in close proximity, before defining the Ti/Al loop structure and gates (5/200 nm), 6.5(e). The insets shows a zoom-in of a junction (top left) and the four-probe current-bias setup used to measure the sample (bottom right). Figure 6.5(f) shows differential resistance plotted as a function of perpendicular magnetic field and direct current. Here we observe periodic modulations in the critical current as the field is swept, which is in accordance with behavior observed in superconducting quantum interferometer devices. From the oscillation period of $\phi \sim 0.26$ mT we infer the area of the loop to be of 7.85 $\mu\mathrm{m}^2$ corresponding to the area of the outer loop (see inset). Summing up, the shadow platform

can be applied to direct fabrication of multi-nanowire JJ devices, e.g. in superconducting diode geometry.[173]

6.7 Conclusion

In conclusion, we utilize a new in-situ shadow technique to form Al junctions on InAs nanowires and compare these to etched junctions. The shadow technique yields smooth junction transitions in contrast to the etched junctions which are abrupt and display Al oxide residues. Etching-induced surface roughening is correlated with a lowering of electronic carrier mobility. Further shadow techniques alongside high-quality exemplary devices employing shadowed nanowires are shown. As up-scaling of technologies requires highly reliable components it seems shadow-based engineering is the most viable approach since any etching-induced perturbations are effectively circumvented. In addition, effectuating algorithm-based tuning of quantum devices in the future will put high demand on stable and non-hysteretic device performance.[174] Taking all findings into account we argue that it is advantageous to move further from ex-situ fabrication towards devices engineered entirely in-situ.

6.8 Methods

Nanowire growth. A molecular beam epitaxy (MBE) system is used to grow Au-seeded wurtzite InAs nanowires along the [0001]B direction on InAs (111)B substrates using the vapour-liquid-solid mechanism. Arrays of Au catalyst particles are placed via standard EBL with particle radius r_{Au} = 20-120 nm and height h_{Au} = 10-50 nm. After substrate annealing at As overpressure at T = 500 C° for 5 min, predominantly vertical nanowire growth is initiated at growth temperatures ranging from T_{growth} = 445-450 C°. Axial nanowire growth is carried out for a duration of 10-120 min before a short break (5 min) is introduced and the As_4/As_2 ratio is increased.

After vertical nanowire growth is concluded, we switch to growth conditions favoring radial growth. First, we introduce a short pause (5 min) before the temperature of the growth substrate is lowered steadily to T_{growth} = 350

C° over about 15 min. After an additional pause (5 min) the nanowires are radially overgrown for 1-20 min depending on the desired amount of overgrowth and distance between Au particles.

Microscopy. TEM was performed using a 200 kV Philips-FEI CM20 large tilt TEM. High-resolution TEM images were obtained using a Jeol JEM3000F microscope. SEM characterization of the as-grown nanowires were carried out with a Jeol 7800F SEM using acceleration voltages in the range of V_{acc} = 1-20 kV.

Device fabrication and measurement. All devices are fabricated on highly doped Si^{++} substrates covered by 200 nm of thermal oxide. Metallic leads to the nanowires were fabricated by electron beam lithography. RF ion (Ar+) milling was performed in the metal deposition chamber prior to e-beam metal deposition of Ti and Au (or Al) (5/∼200 nm) to create transparent ohmic contacts to the nanowires. Standard low-frequency (<200 Hz) lock-in measurements where performed to measure differential conductance ($V_{\mathrm{exc}} \sim$ 5-20 μV).

CHAPTER 7

OUTLOOK

The goal of this section is to explore interesting new ideas – some of which could be 'easily' attained whereas others might require larger efforts. These ideas are spawned between various people, so I am not looking to claim sole ownership, but rather collect and document. The first section presents ideas based on the principles of microtoming and how one could apply these to nanowires to build new types of electrical and optical devices. The second section offers a few natural next-step experiments of Pb-based hybrid nanostructures. The third section demonstrates some interesting device geometries based on multiple nanowires, before a few conclusive remarks rounding off this thesis are presented.

7.1 Cross-sectioned nanowires

Within the past 10 years microtome techniques have improved with regards to sectioning quality, transferring capabilities and alignment procedures. This development has increased the range of compatible materials to include compounds such as cemented carbides and semiconductors, providing a highly interesting outlook for future device explorations.[175] Specifically for semiconductors, we provide in the following an extension on the possible routes forward harnessing and combining the unique traits of VLS grown nanowires and microtomy.

Arrays of quantum dots with tunable coupling

The first idea is perhaps the hardest and revolves around building arrays of coupled quantum dots. In Fig. 7.1 **a** we show a schematic of a hypothetical device based on cross-sectioning of a series of nanocrystal segments merged during growth. The superstructure is contacted by metallic leads (not shown in the sketch), and in addition metal gates have been defined in close prox-

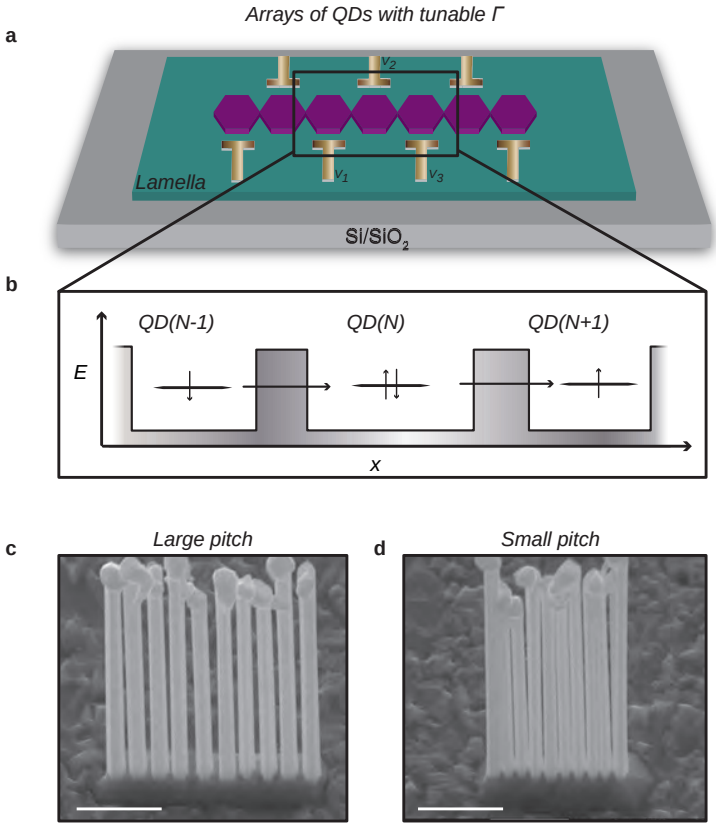

Figure 7.1: **Arrays of QDs with tunable coupling.** **a**, Hypothetical device design for seven merged nanocrystals (magenta). Yellow represents electrostatic gates used to modify the potential in the individual parts of the network structure. **b**, Energy diagram of the quantum dot charging process. **c,d**, SEM micrograph showing an array of nanowires with large (**c**) and small pitch (**d**). Scale bar is 1 µm. SEM images are reproduced from the featured publication.[176]

imity. The gates are used to apply externally controlled electrical fields that adjust the electrochemical potential of the semiconductor locally. By balancing the electrostatic fields right these individual segments are brought into the tunneling regime where each nanocrystal is sequentially charged by single electrons. This is schematically illustrated in Fig. 7.1 **b**. At first hand the coupling, Γ, between adjacent quantum dots is thought to be controlled by adding additional narrow gates (not shown) close to the bridging of the nanocrystals.

However, further control of Γ could be obtained by controlling nanowire pitch and time of radial overgrowth. In Fig. 7.1 **c-d** we show examples of nanowires grown in line with different pitches controlled by EBL. Radially overgrowing these structures is thought to govern Γ by the amount of overlap between adjacent nanowires. Taking into account that charge accumulates at the surface of InAs-based systems due to Fermi level pinning at vacuum[101, 102] other materials (such as InSb[101]) which are less sensitive to surface disorder could be favored for growth controlled couplings. Considering the tunability of the overgrowth and control of the electrostatic environment of the sample, the presented technique could deliver the infrastructure needed for new applications of nanostructures. In the context of quantum computation this technique could be used to realize simulations based on e.g. the Hubbard model, large arrays of quantum dots, and the Su-Schrieffer-Heeger model.[128, 177]

In order to engineer such devices, one needs to consider how to go from arrays of nanocrystals to coupled qubits. A possible route could entail qubit read-out by e.g. spin blockade, charge sensing or dispersive read-out techniques via local gates.[178] To implement charge sensing, nanocrystals are positioned in close proximity to the active device region, simply achieved by controlling catalyst particle placement. During later lithography procedures (the same as for the 'qubit'-device) the electrostatic gates, coupling leads and contacts are fabricated constituting a quantum dot-based charge-sensor. A

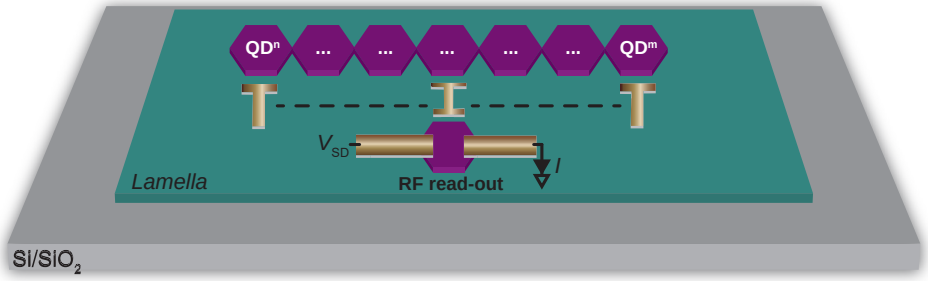

Figure 7.2: **Charge sensor read-out geometry.** Quantum dot-based charge sensors could be integrated into the device design already during the growth phase.

schematic of this idea is presented in Fig. 7.2.

An additional up-shot to this idea is that once an optimized growth recipe is established, multiple lamellas containing the desired nanocrystal-based infrastructure can be transferred a repeated number of times. This number will depend on the nanowire lengths after growth and the desired lamella thickness. An estimate assuming nanowire lengths on the order of several micron and lamella thicknesses between 50-100 nm would under optimized microtome operation give 50 to 500 lamellas from one microtome bullet.

The challenges regarding this idea are likely restrained mostly on how to keep the structures intact over large arrays during sectioning. As array sizes increase the larger impact of stress and strain might compromise the linkage between the nanocrystals. At the moment we are microtoming three joined nanowires successfully, and with further optimization we plan to up-scale to ten in the near future. If this is achieved, the so-called 'perfect transfer'-technique can transfer large lamellas with near 100% yield to any desired substrate.[175]

A concern about device stability might be raised, as the nanoscrystals at the current state of fabrication are surrounded by a resin, which has not been optimized for electronic quantum transport. However, as we show in the appendix (Section 8.4) hysteresis at low temperatures seems manageable. In addition, if hysteresis or other effects do become detrimental to device performance, we have shown that the resin can be effectively removed by oxygen plasma ashing (Setion 8.8), which is a promising alternative route forward which we have not investigated so far.

Stacking lamellas

In general, microtoming allows for stacking of multiple lamellas. This section provides a few examples of the potential use of stacking.

Due to the optical transparency of the lamellas, multiple layers of optically active devices can be combined as seen in Fig. 7.3 **a-b**. For instance light emitting diodes of different wavelength can be stacked to form red, green and blue (RGB) pixels. By controlling lamella alignment, this technique could facilitate the reduction of individual pixel sizes and pixel pitches beyond the current commercial state-of-the art, provided that the necessary infrastructure for electrical contacting is present. Recent advances in lamella alignment utilize orientation by nano-scaled magnets providing accuracies on the order of ± 10 µm.[179] With regards to pixel sizes and pitch, this precision is *not* sufficient and is probably the bottleneck for downsizing using this approach.

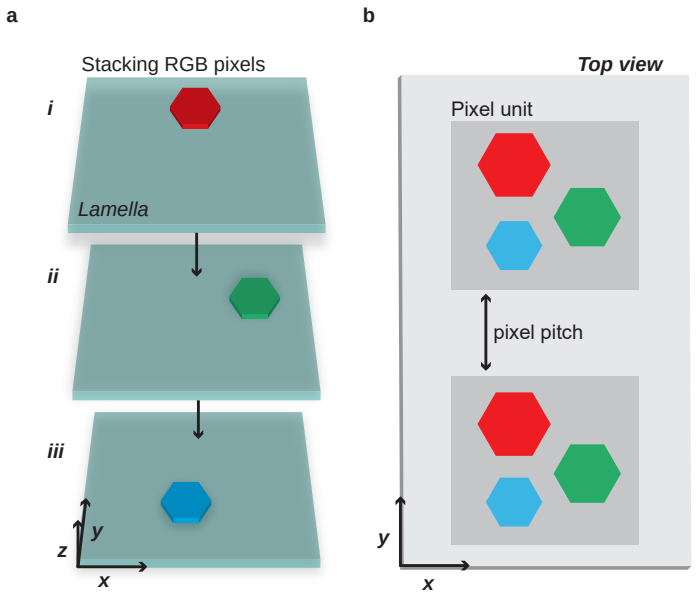

Figure 7.3: **Stacking of lamellas. a** Side-view schematic of the stacking of optically inert lamellas containing cross-sectioned nanostructures with diode properties. **b**, Top-view schematic of stacked lamellas arranged to pack light emitting diodes (red, green, blue) efficiently. The individual diode distances within one pixel unit are expected to be on the order of 100 nm and the distance between adjacent pixel units can be tuned by controlling the nanowire growth pitch.

Further, this method could allow for combining of optimized diode materials (e.g. InGaN for emitting blue) as different nanowire species can be mixed and matched for e.g. maximizing light intensity, colour truth or power consumption.

In similar fashion, this method could be utilized to realise high-efficiency tandem solar cells. Here pn junction materials with various bandgaps are embedded in different lamellas to optimize harvesting of different wavelengths of the solar radiation. These stacks could likely be tested already with current alignment procedures.[175]

In even broader strokes, the stacking approach could be used to pack devices vertically for higher device densities or experiments requiring a vertical design.[180]

Zero-dimensional 'Majorana-like' experiment

Microtoming of nanowires allows for manufacturing of quasi zero-dimensional equivalents of quasi one-dimensional hybrid structures. In the following this approach is related to Majorana zero modes.

A special class of quasiparticle is proposed to appear in strong spin-orbit coupled and quasi-one dimensional hybrid semiconductor nanowires under parallel magnetic fields.[181, 5, 54] These states are dubbed Majorana zero modes. If theoretical predictions are sound, these modes are predicted to form at the boundaries of a so-called topological phase - that is, at the ends of the wire. They are proposed to be detectable via tunneling spectroscopy where they under the right conditions (parallel magnetic field and chemical potential) should form a zero bias peak within the superconducting gap. In addition, from the basis of a Little-Parks experiment[182], it has been proposed that flux-induced phase windings inside a superconductor surrounding a semiconductor nanowire should give rise to Majorana zero modes.[183]

Here we propose an experiments where all the same ingredients are present *except* the one-dimensionality. Both the tunnel experiment and the Little-Parks experiment could be reproduced testing the implications of the zero-dimensional nature of the device in relation to Majorana physics. By microtoming InAs/Al nanowires we obtain cross-sections of structures similar to

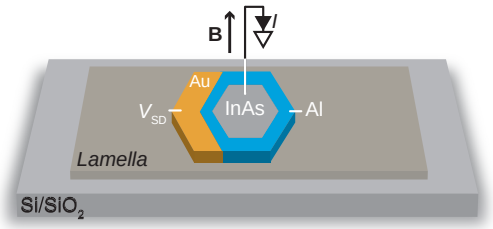

Figure 7.4: **Zero-dimensional InAs/Al 'Majorana' unit.** Lamella containing an InAs/Al/Au nanocrystal in a tunnel junction configuration. The source is connected to an in-situ grown piece of Au shorted to the Al shell, and the core is contacted through a hole etched in an oxide (not shown).

previous experiments, albeit with comparable widths and the lengths, making the structures quasi zero-dimensional. In the case that similar measurements yield similar results, a possible implication could be that previous experiments were merely probing *trivial* effects. Along these lines the proposed experiment could serve as the 'negative' control experiment. In Fig. 7.4 we show a sketch of how such a device might look like.

This paragraph discusses how to carry out this experiment specifically. First full-shell InAs/Al hybrid nanowires are grown before Au is deposited in-situ from a fixed angle. Following, the nanowires are microtomed before standard EBL procedures are used to fabricate tunnel junction/interferometer devices. Potential fabrication complications are likely related to electronic access to the semiconductor core without shorting to the Al shell. After contact has been made to the shell, one could grow an oxide over the entire sample and locally etch the oxide at the core of the nanocrystal. In a subsequent step, electronic access only the semiconductor core could be manifested.

A note of concern might be raised in relation to formation of the Au/Al interface. Here one might be at the potential risk of unfavorable alloy formation at high temperatures ($\sim 400^{\circ}$C) called 'purple death'[184]. This might be detrimental to the experiment as 'purple death' and its related forms vary from being non-superconducting to poorly conducting. These alloying effects could be omitted by choosing different semiconductor/superconductor combinations, avoiding any high-temperature processing techniques or growing an asymmetrically thick superconductor shell and using the larger segment as

contact. The latter could be achieved by first evaporating Al under rotation of the nanowires, then stopping the rotation and continuing the deposition resulting in a local thickness variation.

7.2 Future experiments of Pb-based nanowires

As the development of Pb-based hybrid nanowires is still in its infant stage it is natural to test and compare Pb-based devices against the state-of-the-art experiments of Al-based devices. In of itself, repeating most of these experiments with a high-B_C superconductor is interesting. To name a few Pb-based experiments, who are also likely low-hanging fruits, Josephson junctions, superconducting quantum interference devices, residual resistivity ratios and Little-Parks experiments come to mind. However, as fabrication yield of Pb-based devices is not up to par with conventional Al-based ones, it seems reasonable to first look further into materials development.

The reason Al-based devices are easy to fabricate can probably be attributed to mainly one thing – its self-terminating oxide layer, Al_2O_3. Aluminium oxide is a well-understood ceramic and it is used as a dielectric in many devices due to its stable nature. However, the oxide formed on Pb films does not provide the same kind of stability. From this stand point, naturally, growth of multiple superconductors springs to mind. Figure 7.5 sketches a nanowire covered by both Pb and Al deposited in a double-step evaporation. Here the large Δ, B_C and T_C of the inner Pb film is combined with the stable oxide of the outer Al shell.

Other coatings than Al could be explored, but the advantage to this is that recipes optimized for Al processing could be transferred directly to the new InAs/Pb/Al devices or at least serve as a good foundation for further device exploration. If device quality still suffers during post-growth processing one

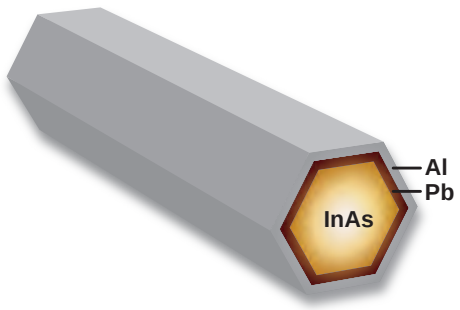

Figure 7.5: **Pb/Al tandem deposition on an InAs nanowire.**

could imagine moving as many fabrication steps in-situ MBE as possible. The first steps following this path are already shown in Section 2.3, Section 4.1 and Chapter 6.

7.3 Multi-nanowire geometries

Since the origin of the (semiconductor) nanowire, there has been extensive interest in building multi-wire networks and devices.[185] Moving forward we present two interesting potential future studies within the context of hybrid multi-nanowire devices.

Diode effect in shadowed Josephson junction interferometers

As of lately, the interest in the 'Josephson diode effect' has grown due to the promise of bringing superconducting neural networks with low power consumption and isolated signals within experimental reach.[186] A particularly accessible idea has recently been proposed which relies on two or more Josephson junctions placed in a superconducting interferometer geometry.[173] It relies on only two requirements, that is, (1) a high-harmonic content in the current phase relation which is tunable and (2) breaking of time-reversal symmetry. As opposed to other proposed types of Josephson diodes it omits the need for Rashba spin-orbit coupling and Zeeman splitting. The diode effect is achieved by balancing the transparency of the junctions by applying local electrostatic gate potentials and tuning the harmonic content. A particularly promising feature of this proposal is that the diode efficiency scales with the number of Josephson junctions potentially enabling efficiencies up 75% for 10 junctions.

In Fig. 7.6 we show a functional prototype device comprised of three Josephson junction based on hybrid InAs/Al nanowires, which fulfils all requirements for realizing this proposal. Panel **a** illustrates the four-probe current-biased setup used to measure the sample. Each Josephson junction is based on InAs nanowire with Al deposited in-situ similar to the one shown in Fig. 7.6 **b**. These wires are selectively shadowed using the technique presented in Chapter 6. After growth the wires are placed using a micromanipulator needle in close proximity of each other on a typical Si/SiO_2 oxide substrate, before standard clean-room processing is used to define the Ti/Al loop structures and gates (5 nm/200 nm). In Fig. 7.6 **c** an SEM image of the measured device is shown.

After the transparencies of the junctions are increased by applying a

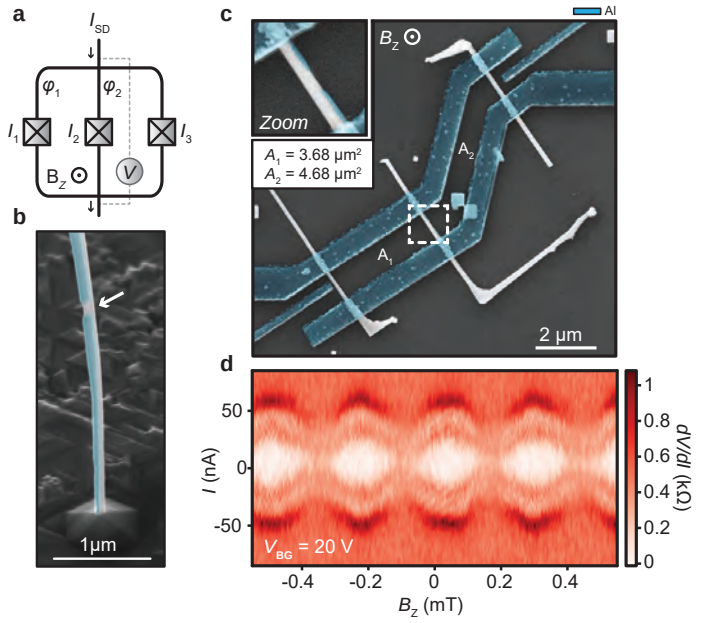

Figure 7.6: **Hybrid nanowire-based triple Josephson junction interferometer. a**, Schematic of the current biased four-probe setup with three JJs in a loop geometry. **b**, Side-view SEM micrograph of a typical in-situ shadowed InAs/Al nanowire used for devices. White arrow indicates the junction. **c**, Top-view SEM micrograph of the measured device. The Al on the nanowires is deposited in-situ MBE, whereas the loop geometry is fabricated by ex-situ evaporation of Ti/Al contacts. **d**, Differential resistance versus perpendicular magnetic field and current showing critical current modulations. The period of $\phi \sim 0.26$ mT corresponds to an area of 7.85 µm^2 matching the sum of both areas.

positive backgate voltage ($V_{\mathrm{BG}} = 20$ V) we probe the device under magnetic fields. In Fig. 7.6 **d** the differential resistance is plotted as a function of current and perpendicular magnetic fields. Here the critical current is modulated in a periodic manner as the field is swept. The period of these modulations ($\Delta B_{\mathrm{Z}} = 0.26$ mT) corresponds to an increase of one magnetic flux quantum ($\Phi_0 = \mathrm{h/2e}$), from which we find the area of the loop to be $A = \Phi_0/0.26\mathrm{mT} \sim 7.85$ µm^2. This corresponding to the area of the outer loop. Natural next-steps following the verification of superconducting quantum interference, would entail tuning of the individual junction transparencies with the side-gates and backgate voltage. Here one would tune the transparen-

cies of the three junctions asymmetrically while monitoring for changes in the diode efficiency.

In the following we present some experimental considerations for further realization of this study. A potential complication of this proposal is its need to tune each junction individually, which comes with two experimental hurdles. The first is related to fabrication of devices of two or more junctions. As each junction needs individual tuning, a gate electrode has to be placed inside the loop proximal to the junction without shorting to the superconducting loop. Here are two proposed fabrication strategies: (1) The desired hybrid wires are placed on pre-fabricated local bottom gates prior to defining the loop geometry. An oxide grown in an intermediate step would ensure electrical isolation between the gates and the loop. (2) One could reverse the order of option (1) and deposit an oxide after the loop has been defined and defining top-gates crossing the loop structure hereafter.

The second problem relates to the scaling of this experiment. As the number of junctions grows an increased demand on junction quality and stability is demanded. As discussed in Chapter 6, however, reproducible hybrid nanowire junctions are likely better formed in-situ rather than ex-situ, and with this in mind, it would seem that the shadowed hybrid nanowire platform presented here, is already a good starting point.

A potential third obstacle could be the degree of precision to which the junction transparency needs to be controlled. For example, it is probably of little concern to tune a two-junction device into a sufficiently asymmetric configuration, where one junction is very transparent and the other less. However, already a 10-junction device puts forth stricter requirements on the precision of the tuning of each junction, in order to optimize the diode effect. A potential remedy might entail handing over the bulk of the tuning work to an algorithm adjusting junction transparencies while optimizing for diode efficiency.

Scalable arrays of Andreev spin qubits

We now switch gears to a possible future experiment which currently sits at a much less developed experimental stage than the one discussed previously. In what follows, we provide some initial steps towards a recent theoretical proposal on Andreev spin qubits coupled via superconductors.[187] The proposal suggests a scalable network of superconducting spin qubits in arrays of parallel aligned semiconductor nanowires with superconducting contacts.

In a nutshell, the proposed geometry relies on parallel semiconductor nanowires with tunable Josephson junctions placed in close proximity. The nanowires are shorted together by superconducting leads and electrostatic gates forming quantum dots inside the Josephson junctions and providing spin-1/2 states. In Fig. 7.7 we show how current state-of-the-art growth techniques[37, 133, 176] can be modified to provide the first-steps towards investigating the proposal experimentally. Panel **a** shows an SEM image of an in-situ shadowed InAs/Al hybrid nanowire. Here the growth direction of the nanowires is modulated by substrate etching ensuring that individual nanowires act as shadow masks for the superconductor evaporated under an angle in a later processing step. In panel **b** an SEM image of an array of 10 nanowires grown in close proximity is presented. One could imagine combining both growth techniques (panel **c**) and forming arrays of closely spaced InAs nanowires with multiple Josephson junctions. Naturally a question regarding transferring arises: How do you move such an ensemble collectively to a device substrate without losing the ordered nature and alignment?

One approach could entail embedding the structures in a polymer and defining openings in the polymer by lithography and later removing the polymer blocks with embedded nanowires by mechanical manipulation with a needle. Alternatively one could expose the substrate to liquid nitrogen after embedding and detach the polymer blocks by the differing thermal expansion coefficients of the polymer and the growth substrate. Following, the blocks are transferred to a desired substrate by a mechanical needle before the polymer is removed by oxygen plasma ashing leaving behind an ordered array of shadowed nanowires.

Investigating other approaches, one could completely avoid the transferring

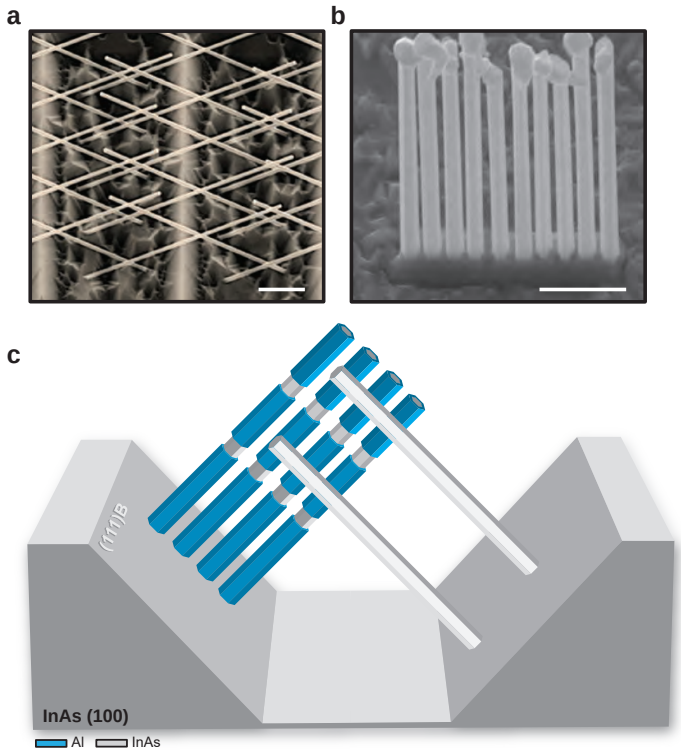

Figure 7.7: **Array of InAs nanowires for scalable Andreev spin qubits.** **a**, SEM micrograph showing arrays of InAs nanowires grown from grooves etched into an InAs substrate. Scale bar is 2 µm. The image is reproduced from Ref.[37] **b**, SEM micrograph of an array of 10 InAs nanowires grown in close proximity. The image is reproduced from the featured publication.[176] **c**, Sketch of the growth techniques from **a** and **b** are combined in order to create large numbers of in-situ shadowed parallel nanowires suitable for Andreev spin qubits.

complications, by utilizing a recently developed selective-area-grown (SAG) platform.[162] Here a two-step growth approach is deployed to grow both the semiconductor nanostructures and the shadowing structure while still enabling in-situ shadowing. A potential drawback to this method, however, is the semiconductor quality difference between the SAG grown and VLS grown nanostructures. In contrast to VLS grown nanowires who can freely strain relax, the crystal structure of SAG structures is highly dependent on the substrate/nanowire interface and is thus more prone to exhibiting unfavorable crystal perturbations affecting electronic transport unfavorably.[139]

7.4 Final remarks

This thesis has explored various new types of hybrid nanostructures and their electronic transport using InAs nanowires as the basic unit.

Chapter 3 and Chapter 4 discuss data from hybrid InAs/Pb(/Au) nanowire devices measured using tunnel junctions and island geometries. They behave comparably to hybrid InAs/Al nanowires and surpass these on a number of material dependent metrics. We find a superconducting critical temperature of 7 K and a superconducting gap of 1.25 meV which remains hard in parallel magnetic fields up to 8.5 T. In the island devices we find a transition from $2e$-dominated transport to $1e$ charging events similar to experiments conducted on semiconductor-Al hybrids. Given these findings, the InAs/Pb nanowire naturally poses as a strong alternative to the Al-based structures. However, as the complex data presented in Chapter 4 suggests, harnessing the full potential of this new hybrid platform still requires a sizeable push in material development/device optimization and more experiments providing further insight.

Chapter 5 investigates the use of microtomy for production of (hybrid) quantum devices, among others. We find that one can produce electronic devices on cross-sectioned InAs nanoscrystals embedded in a resin with good yield, and in addition, that these devices are capable of exhibiting electronic quantum phenomena. As both the microtome platform and growth of VLS nanowires are inherently scalable techniques, we propose the combination of both as a path towards fabrication of scalable quantum devices with a lot of new degrees of freedom with respect to device design and geometries.

Chapter 6 extends on the tool-boox of in-situ shadowing techniques using VLS grown nanowires. We find that control over nanowire radius/height allows us to selectively deposit a superconductor shell (Al) on parts of the nanowires with high yield. Using this technique we structurally and electronically compare junctions formed by shadowing versus etching. From TEM analysis we find atomic scale roughening of the InAs surface which has been in contact with the etchant. This is not observed for the shadowed nanowires. Moreover, we compare electronic transport in InAs/Al nanowire transistors with both junction types. Here we find a factor two reduction in field ef-

fect mobility across the etched junctions. Following, we provide a selection of more advanced shadowing techniques that could aid the field to move further towards fully in-situ engineered devices. In the end, we give examples of quantized conductance and superconducting interference effects measured using shadowed InAs/Al nanowires.

This wraps up the presented work on electronic (quantum) transport in new hybrid nanostructures. As interest and monetary investments in quantum technologies only seem to grow, the need for ever advancing technologies is only rising with it. It is hence essential to explore new techniques, material combinations and experimental ideas providing the tools to investigate ever more challenging and fascinating ideas. This work presents my contribution to this end.

CHAPTER 8

APPENDIX

The appendix presents extended data from the article reprinted (*Scalable platform for nanocrystal-based quantum electronics*) in Chapter 5.

8.1 From nanowires to nanocrystal arrays

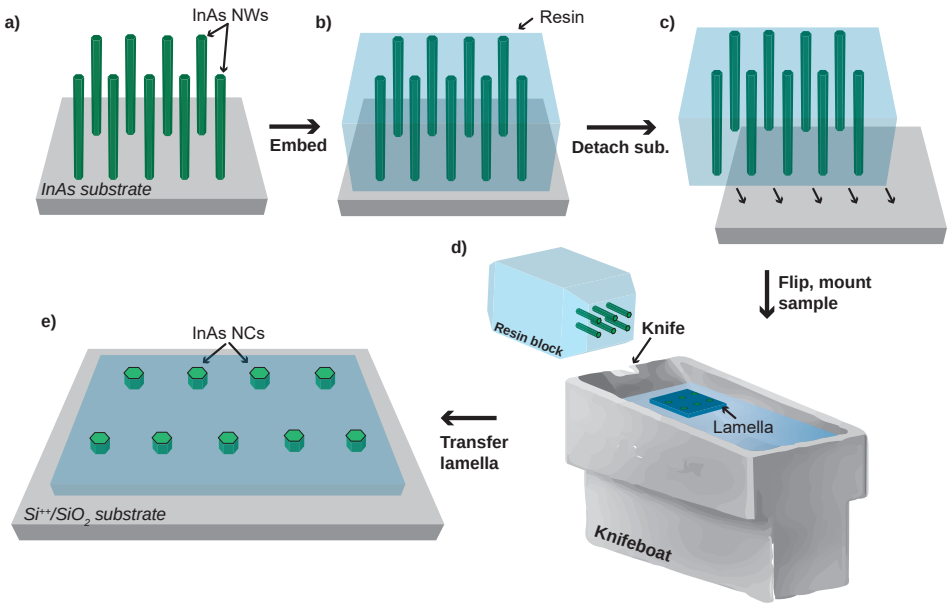

Figure 8.1: **Manufacturing nanocrystals from nanowires.** a) Array of InAs nanowires grown on a (111)B InAs substrate. b) Following growth a piece of the substrate is embedded in a resin and hardened. c) By manipulation of a razor blade (and sometimes liquid nitrogen) the substrate is detached from the resin block. d) The resin block is mounted in the microtome with the exposed nanowires facing the knife. The resin block is advanced in small increments toward the knife, cutting thin sections (lamella) which float on the surface of the medium contained by the knifeboat. e) A device substrate (e.g. Si^{++}/SiO_2) is partially submersed into the knifeboat fluid and gently lifted such that the floating lamella is transferred onto the substrate.

The resin block held by the microtome is advanced in small increments and moved over the knife cutting thin sections (lamella) on the order of 50-200 nm. After sectioning, the lamellas float on the fluid (H_2O) surface suspended in the knifeboat. (Figure 1d). Another substrate (eg. carbon grid or Si^{++}/SiO_2) is then submersed into the fluid and used to gently lift-up the floating lamella containing arrays of NCs (Figure 1e). Fluid residues trapped between the substrate and lamella are removed by pumping before any further processing. Further details on the general use of ultramicrotomes and other related processes can be found in a review by the Whitesides group[123].

The expected mechanism for successful nanocrystal sectioning relies on crystal cleaving, rather than cutting. If the angle of the knife and the (111)/(0001) plane of the crystalline nanowire is adequately aligned, we believe it is favorable for the nanowires to cleave along the high-symmetry axis. In Supp. Fig. 8.2 **a** we show an example of a successfully sectioned nanocrystal where the top cut facet exhibits a root-mean-square roughness on the order of 1 nm. We

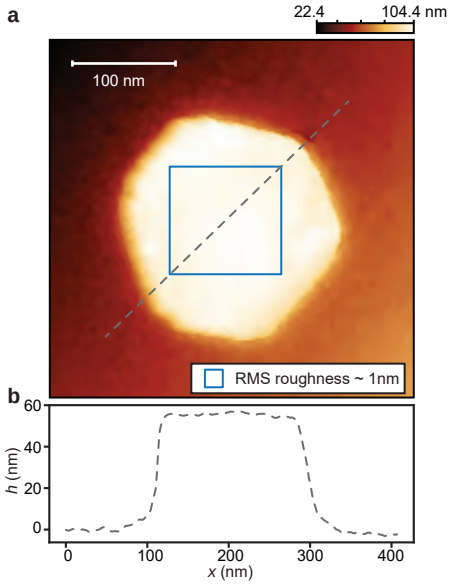

Figure 8.2: **AFM image of successfully sectioned/cleaved NC.** a) AFM image of NC extending $\sim$ 60 nm out from the lamella. The region marked by the blue square indicates the area from which the RMS roughness is calculated. b) Height versus path indicated by dashed line in **a** showing a flat topology of the NC.

plot the line trace indicated by the dashed line in Supp. Fig. 8.2 **b** which shows the flat topology of the top of the NC. In addition, we find that the NC extends about 60 nm from the lamella. We note that that this 'extension' effect might arise from extensive local exposure to electron beams from e.g. recording SEMs resulting in the lamella shrinking locally.

8.2 Nanocrystal inspection across multiple lamellas

In Section 2 we show how individual NCs can be tracked across multiple lamellas before we discuss the cut face quality.

Scanning electron microscope (SEM) images of a series of arrays of NCs are seen in Figure 8.3a-e. As all the nanowires were grown in predetermined arrays before sectioning we can track the locations of the single NCs found in the previous or following lamellas. This is done by counting columns and rows in the different arrays and sub-arrays from a given reference point.

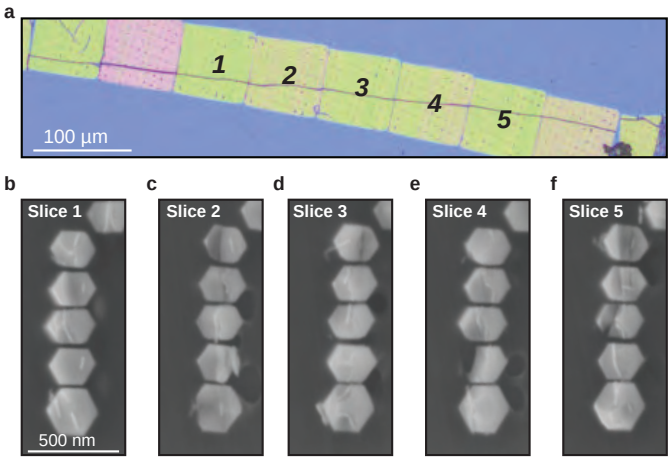

Figure 8.3: **Identifying single NCs across multiple sections.** a) Optical image of the 5 chosen lamellas deposited on a Si^{++}/SiO_2 substrate. Nanocrystal arrays and their according lamellas are indicated by numbering. b-f) SEM images of arrays of single NCs obtained from 5 consecutively cut lamellas where individual NCs originate from the same nanowire. Scalebar is the same for all images.

The individual lamellas are indicated by numbering in the optical image

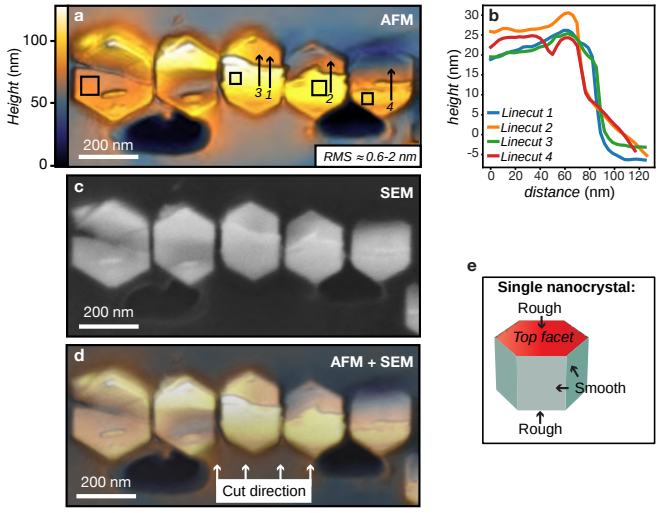

Figure 8.4: **AFM inspection of the cut face quality.** a) AFM image of a series of closely spaced NCs fixated in a lamella. Black boxes indicate where the RMS roughness of 0.9-2 nm is obtained. b) Height versus distance showing the profile along the linecuts in (a). c) SEM image of the same structure shown in (a). d) A combination of the AFM image shown in (a) and the SEM image shown in (c). White arrows illustrate cutting direction. e) Illustration of a single NC where top and bottom facets are roughened after sectioning and the six other remain pristine.

shown in Figure 8.3. By e.g. depositing every 10^{th} lamella on a different substrate dedicated for AFM, SEM or transmission electron microscope (TEM) inspection, this approach can be used to control the quality of NC-based devices. We believe that running this approach under highly optimized microtome conditions (resin, resin hardness, knife type, knife-angle etc.), it may be used for quality controlling of electrical and optical (quantum) devices for large scale manufacturing processes.

We now move on to inspecting the cut faces of NCs from a single array. The five NCs seen in Figure 8.4 show a outtake of lower quality of the cut-face of the NCs after sectioning with the current embedding and microtoming recipe. The structures are shown in an AFM image (Figure 8.4a), an SEM image (8.4c) and a combination of both images (Figure 8.4d). Apart from the few larger steps on the top facet ($\delta height \sim$ 20-30 nm, see line-scan from Figure 3a plotted in b) the local root-mean-square (RMS) roughness after sectioning (areas indicated by the black boxes) is on the order of 0.9-2 nm,

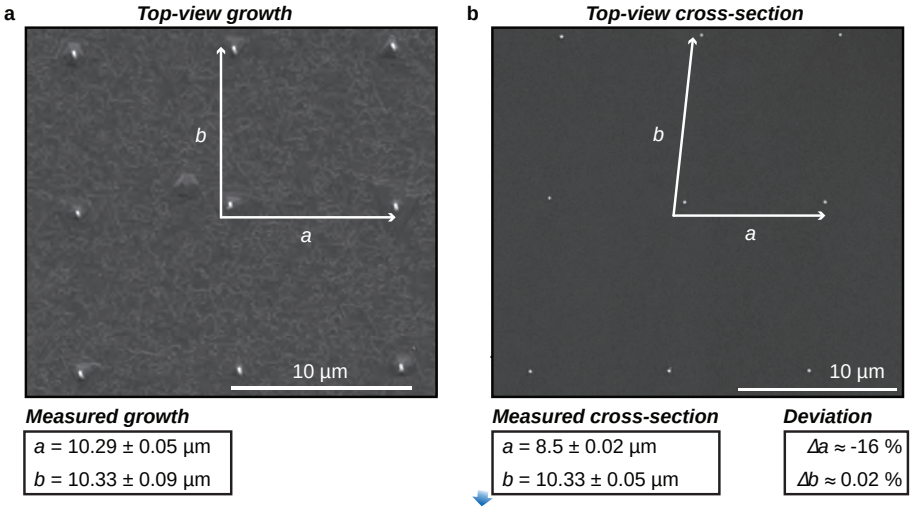

Figure 8.5: **Compression effects of the lamella during sectioning.** a) Top-view SEM image of as-grown nanowires. b) Top-view SEM image of the according nanocrystals after sectioning. The information boxes show the measured distances before/after sectioning and their deviation.

suggesting that large portions of the nanowires cleave and form NCs along a high-symmetry crystal axis. We speculate that the larger steps are an artefact from non-optimal alignment of the crystal axes of the nanowires with respect to the cutting plane of the knife. Likely any misalignment will result in the crystals breaking locally instead of cleaving along a crystal axis. This is further supported by the fact that the ridges formed after cleaving are predominantly perpendicular to the cutting direction of the knife, as similarly observed in alumina samples[188]. The cutting direction of the knife is indicated by white arrows in Figure 8.4d.

Taking into account that the top and bottom facets of the NCs at this point appear somewhat irregular (see Figure 8.4e), we stress that out of the total of eight facets likely the six side facets remain pristine. In addition, we note that commercial ultramicrotome manufacturers are sectioning many different materials (e.g. Si, GaAs, BiTe, Al, AlO_2, Cu and Au)[132] and large portions of the periodic table are predicted to be intact after sectioning[123], hence achieving even more uniform structures in our case is likely a matter of optimization of the cutting angle.

In the following paragraph we investigate any compression effects that can

occur during the microtome process due to the knife deforming the resin. In Fig. 8.5 we measure the spacing of arrays of single nanowires before (**a**) and after (**b**) sectioning. Based on the given values we estimate a compression of about -16% mainly in one direction for this sample. Other samples show similar behavior with slightly lower values (10-15%). These positional shifts do not pose any hindrance to device fabrication as the position of each individual nanocrystal is recorded by SEM with respect to a pre-defined grid of alignment marks. We highlight that these effects can be alleviated by optimizing the rigidity of the resin and/or cooling the samples prior to sectioning.

8.3 Temperature dependence of conductance resonances

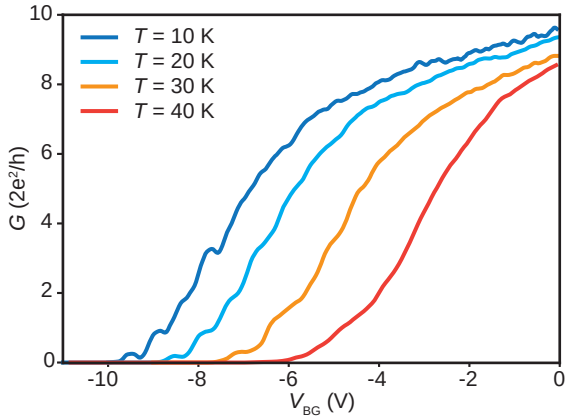

Figure 8.6: **Electronic transport resonances evolved in temperature.** Linear conductance, G, recorded as a function of backgate voltage, V_{BG}, repeated for T = 10, 20, 30 and 40 K. For increasing temperatures the conductance resonances start to smooth and disappear. Presented data originate form *Device* 6. Traces are offset in V_{BG}.

Here we present a representative example of temperature dependent conductance resonances occurring in our devices. Linear conductance, G, recorded as a function of backgate voltage, V_{BG}, for a series of different temperatures is shown in Figure 8.6. At low temperatures (T = 10 K) we observe pronounced resonant behavior which smooths and disappears as the temperature is increased to T = 40 K.

8.4 Nanocrystal device stability

In this section we investigate the stability of two NC field effect transistor devices, namely *device* 6 and 7, as seen in Figure 5. At cryogenic temperatures ($T = 3$ K) both devices show resonant behavior when sweeping the zero bias conductance (G) as a function of backgate voltage (V_{bg}). More specifically *Device* 7 shows pronounced plateauing of the conductance traces at one and two integer values of $G_0 = 2e^2/h$ at zero magnetic field and without applying any fitting of the contact resistances. This behavior is stable over more than 20 consecutive up and down sweeps. Taking also into account the waterfall plot shown in Figure 3a in the main article, this suggests that *device* 7 behaves as a quantum point contact under given electrostatic fields. The behavior

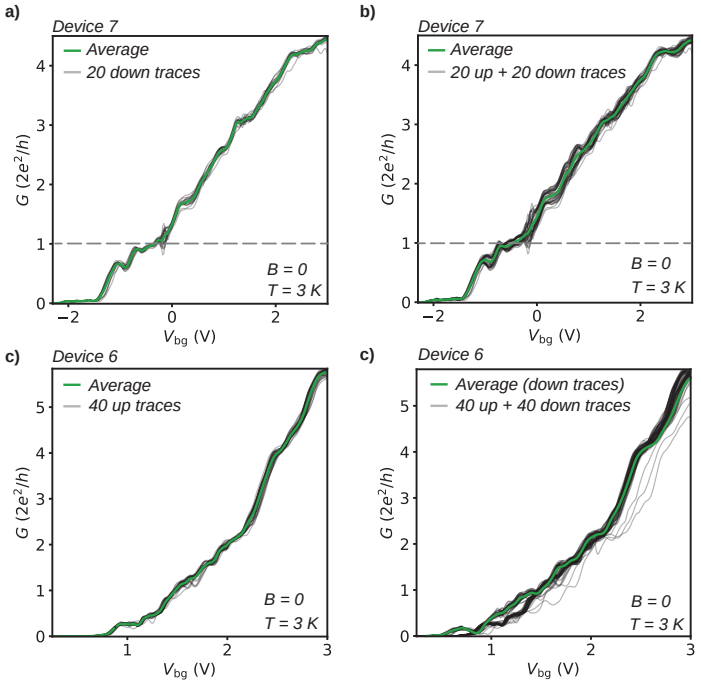

Figure 8.7: **Nanocrystal device stability.** a) Zero-bias conductance (G) traces swept as a function of backgate voltage (V_{bg}) of *device* 7 showing pronounced plateauing close to 1 and 2 $G_0 = 2e^2/h$. The sweep is repeated 20 times and the average plotted as a green line. b) 20 consecutive up and down traces plotted together showing a high degree of reproducibility for the same device as shown in **a**. c, d) Same as **a, b** for *device* 6 showing a high degree of reproducibility and somwewhat hysteretic behaviour.

and data quality is consistent with other InAs nanowire-based quantum point contacts[142, 140, 143, 144]. The G/V_{bg} traces of *device* 6 are almost as stable as for *device* 7, however with somewhat more pronounced hysteresis. Generally, the other devices show a field effect response which is similar or slightly more hysteretic than the two devices presented here.

8.5 Extended data on field effect transistor fits

In this section we show a variety of I/V curves of the measured devices (Fig. 8.8) and all the field effect transistor (FET) mobility fits used in main article (Fig. 8.9).

All FET data are recorded at $T = 2.8$ K explaining the resonant behaving as discussed also in Supporting Section 3. The FET mobility is estimated using a commonly used expression for nanowire FETs[135],

$$G(V_{\mathrm{BG}}) = \left(R_{\mathrm{s}} + \frac{W^2}{\mu \cdot C_{\mathrm{G}} \ (V_{\mathrm{BG}} - V_{\mathrm{th}})} \right)^{-1}$$

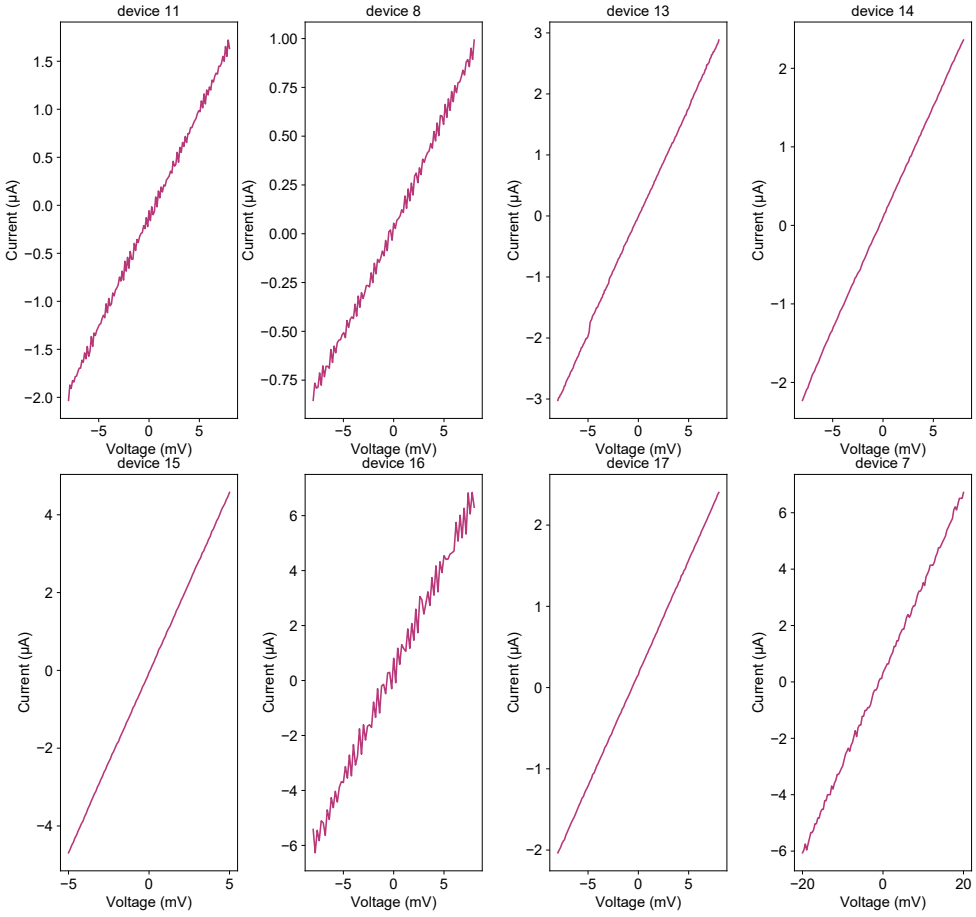

Figure 8.8: **I/V curves of the FET devices.** Recorded I/V curves for device 7, 8, 11, 13, 14, 15, 16, 17 showing good ohmic response in the few kΩ-range.

, here $G(V_{\mathrm{BG}})$ is the linear conductance, R_{s} is the series resistance, W is the distance between the contacts, μ is the FET mobility, C_{G} is the gate/NC capacitance and V_{th} is the threshold voltage. We use μ, R_{s} and $\mathrm{V_{th}}$ as the free fit parameters, and estimate C_{G} from the slopes of the Coulomb diamond

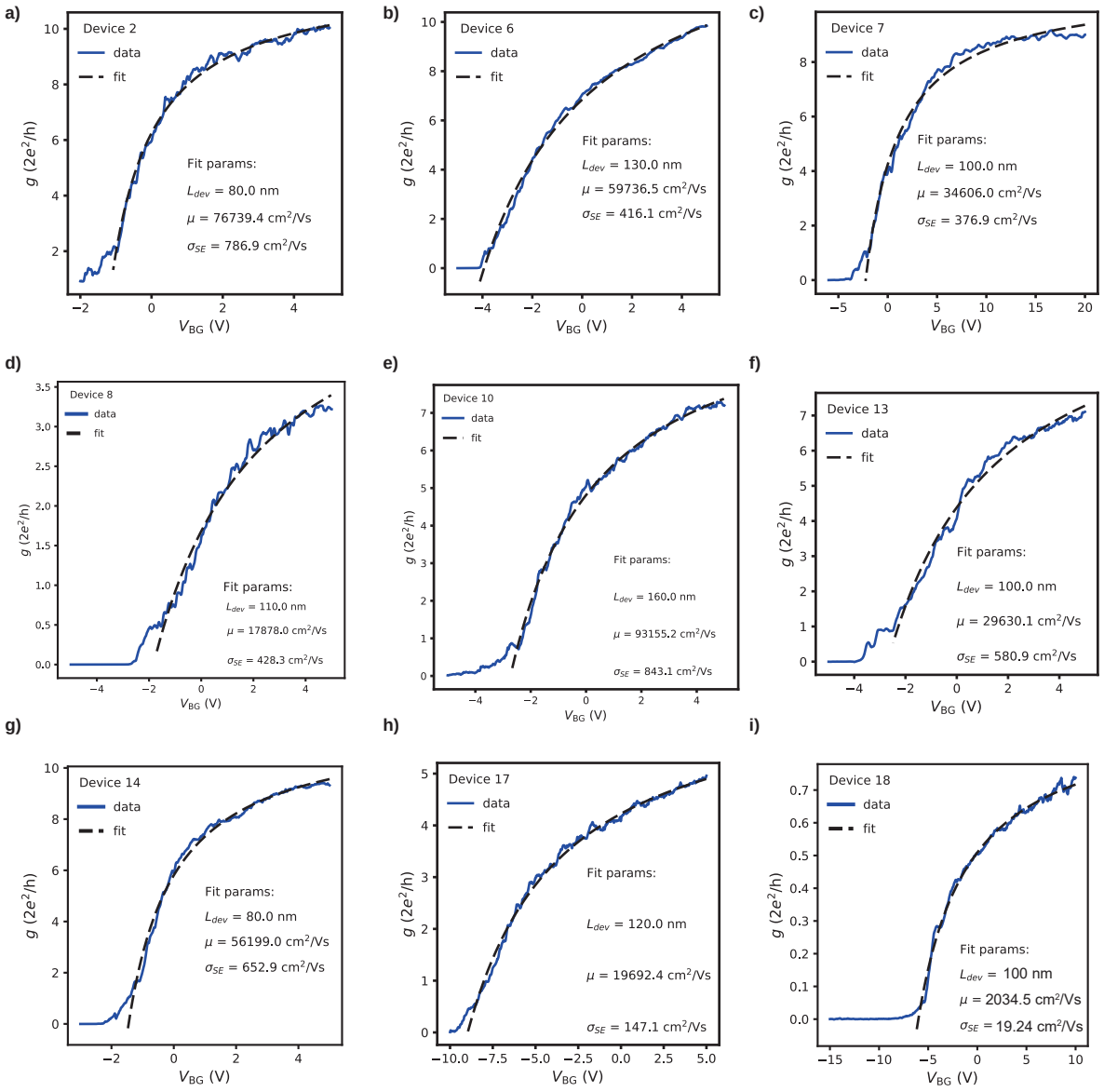

Figure 8.9: **Extended data on FET fits.** a-i) Zero-bias pinch-off traces of conductance (g) as a function of backgate voltage (V_{BG}) with according FET fits and their standard error. Data is recorded at $T = 2.8$ K.

shown in in the main article (Figure 3b, this value is used across all measured devices) and measure the distance between the contacts, W, by SEM.

8.6 Extended data on quantum point contact-like behavior

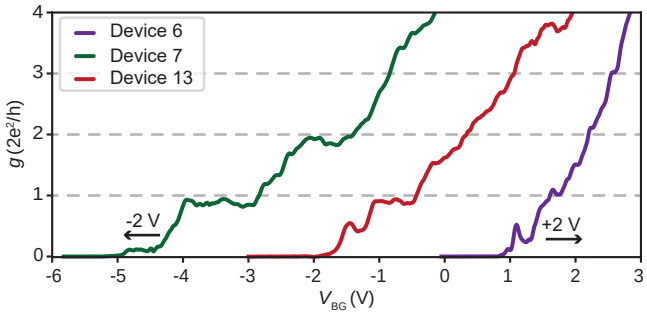

Figure 8.10: **Additional data on plateau-like conductance effects.** Zero-bias conductance (g) plotted versus backgate voltage (V_{BG}) for *Device* 6, 7 and 13, showing plateauing-effects. *Device* 6 and 7 are off-set by $V_{\mathrm{BG}} = \pm$ 2 V.

In this section we show extended data on the quantum point contact (QPC)-like behavior of *device* 6, 7 and 13. All data are recorded with no applied magnetic field and plotted without any processing or fitting. The conductance trace for *Device* 7 shows strong plateauing-effects for the first two integer values of $2G_0 = 2e^2/h$. *Device* 13 shows a similar effect at $2G_0$, whereas device 6 shows weak signs of conductance plateauing at the first 3 integer values of $2G_0$.

Except for the waterfall plot shown in Figure 3a of the main article (*device* 7), the data become noisy at large finite bias voltages which is why we show only the zero-bias traces. Based on this, we only use the data from *device* 6 and 13 to suggest QPC-like behavior. We note that observations of increased noise in quantum devices at larger bias voltages is not an uncommon phenomenon.

8.7 Excited states in a nanocrystal quantum dot

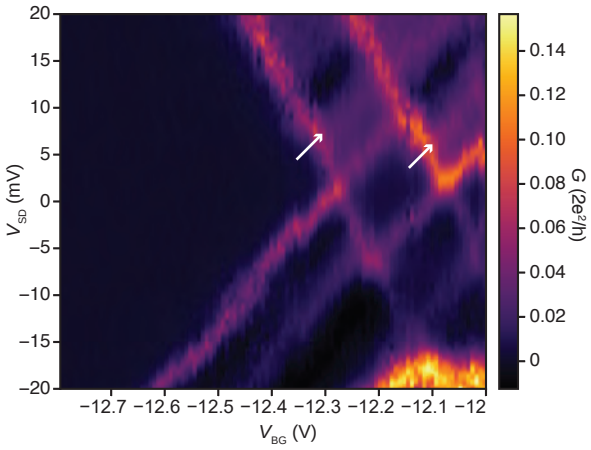

Figure 8.11: **Excited states in a NC quantum dot.** Differential conductance ($G = dI/dV$) plotted versus backgate voltage (V_{BG}) and bias voltage (V_{BG}) for *Device* 7. Potential excited states are indicated by the white arrows.

8.8 Ensemble sectioning and lamella removal

Here we show how a large number of consecutively cut lamellas can be placed in ribbons without overlap and collectively transferred in a single step. After having prepared a sample, trimmed the block face and mounted it in the microtome, the resin block is ready for sectioning. During sectioning the lamellas adhere on the edge of the diamond knife connecting with a previous section and pushing it along the diamond knife. Continuous sectioning thus creates ribbons of lamellae. We find that this effect is best achieved with a square block face shape. This process can be repeated for a desired number of times before the ensemble is moved to the knife boat fluid. In Figure 8.12a and b, we show optical images of 18 individual sections, of which 15 remained in contact after transferring the whole ensemble in a single step covering an area

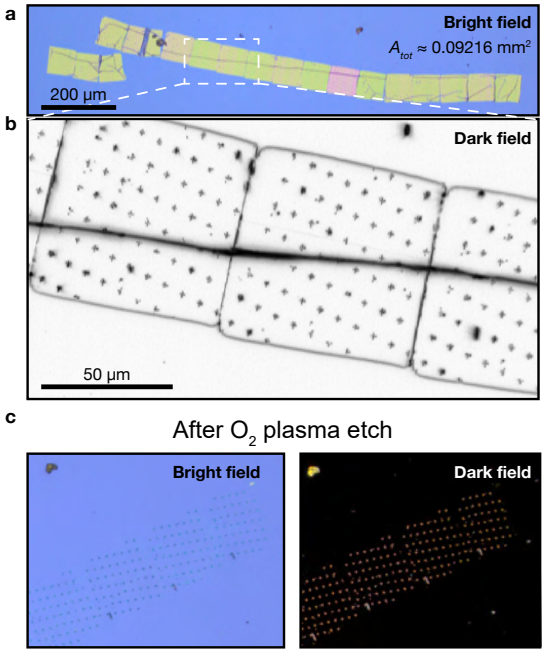

Figure 8.12: **Ensemble sectioning and transferring of lamella ribbons.** a) Bright field optical image of 18 lamellas transferred to a Si^{++}/SiO_2 substrate in a single step. The three left-most lamellas detached themselves from the ensemble during transfer. b) Dark field optical image of a zoom-in of the NC array structures held in the lamellas. c) Dark field/bright field optical image of arrays of NCs after oxygen plasma ashing.

of $\sim$ 0.1 mm^2. In this particular case we were investigating how to produce single lamellas with small areas ($\sim$ 70 x 70 μm). We note that this approach may be extended both in terms of number of lamellas cut consecutively and also their individual area. This is also shown and further discussed in recent work.[125].

In Figure 8.12c we show the effects of oxygen plasma ashing on the resin after 18 min of ashing at 100 W. In comparison to panel a) the resin is seemingly removed leaving only minimal residue. This approach has not been further investigated in this work, but is a compelling approach to the future applications of the presented platform where resins are undesirable.

8.9 Growth of nanowires in close proximity

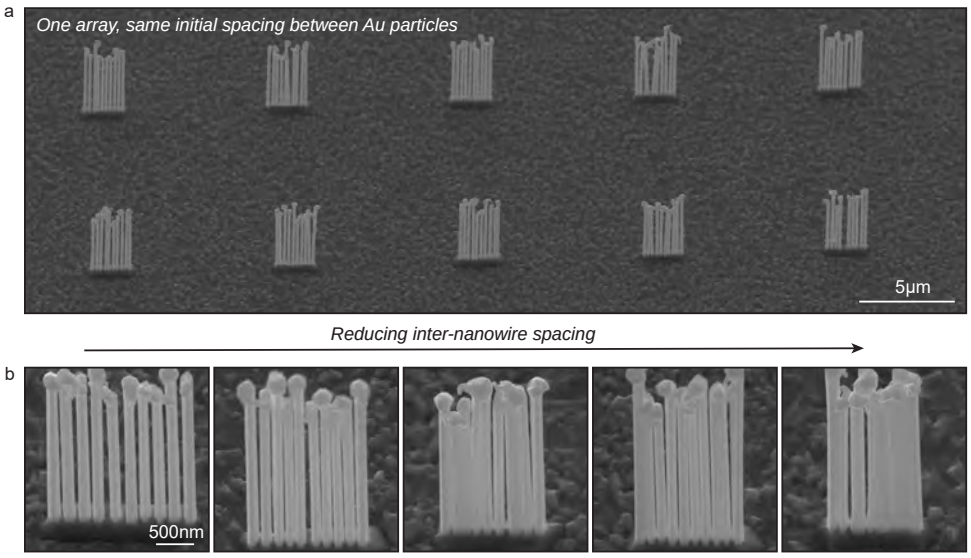

Figure 8.13: **Growth of nanowires in close proximity.** **a**, Arrays of 10 adjacently grown nanowires. **b**, Zoom-in of different nanowire arrays with decreasing inter-nanowire spacing. Scale bar is the same for all panels.

If nanowires are positioned with an inter-nanowire distance that is closer then the mean diffusion length of the evaporated material, in this case indium, the substrate adatom population will be uneven. This can for instance imply that during growth of multiple nanowires (see Supp. Fig. 8.13) the nanowires

will have different adatom contributions and thus varied effective V/III flux ratios in the catalyst. In particular, this influences the growth dynamics in the axial nanowire growth phase, where e.g, the diameter of the outermost nanowires is observed larger then the center nanowires. In the radial growth step, the uneven adatom population from the substrate combined with flux shadowing effects give rise to asymmetric radial overgrowth. We note that optimization of growth parameters can alleviate any unwanted asymmetries and control the extend to which the nanowires are grown together.

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2. **J. E. Sestoft***, A. N. Gejl*, T. Kanne*, R. D. Schlosser, D. Ross, D. Kjær, K. Grove-Rasmussen, and J. Nygård, 2022. *'Scalable Platform for Nanocrystal-based Quantum Electronics'*.
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3. **J. E. Sestoft***, M. Marnauza*, D. Olsteins, T. Kanne, R. D. Schlosser, I. Chen, and J. Nygård, 2022. *'Shadowed and etched superconductor-semiconductor junctions in Al/InAs nanowires'*.
Manuscript in prep.

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